



**THE DATASHEET OF  
AMC1306M05QDWVRQ1**



# AMC1306M05-Q1 Automotive, High-Precision, $\pm 50$ -mV Input, Reinforced Isolated Delta-Sigma Modulator

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
- **Functional Safety-Capable**
  - [Documentation available to aid functional safety system design](#)
- Linear input voltage range:  $\pm 50$  mV
- Low DC errors:
  - Offset error:  $\pm 50$   $\mu\text{V}$  (max)
  - Offset drift:  $1$   $\mu\text{V}/^{\circ}\text{C}$  (max)
  - Gain error:  $\pm 0.2\%$  (max)
  - Gain drift:  $\pm 40$  ppm/ $^{\circ}\text{C}$  (max)
- High CMTI:  $100$  kV/ $\mu\text{s}$  (min)
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Safety-related certifications:
  - $7070$ - $V_{\text{PEAK}}$  reinforced isolation per DIN VDE V 0884-11: 2017-01
  - $5000$ - $V_{\text{RMS}}$  isolation for 1 minute per UL1577

## 2 Applications

- Shunt-resistor-based current sensing and isolated voltage measurements in:
  - [Traction inverters](#)
  - [Onboard chargers](#)
  - [DC/DC converters](#)
  - [HEV/EV DC chargers](#)

## 3 Description

The AMC1306M05-Q1 is a precision, delta-sigma ( $\Delta\Sigma$ ) modulator with the output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to  $7070 V_{\text{PEAK}}$  according to the DIN VDE V 0884-11 and UL1577 standards, and supports a working voltage up to  $1.5$  kV $_{\text{RMS}}$ . The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from voltages that can cause electrical damage or be harmful to an operator.

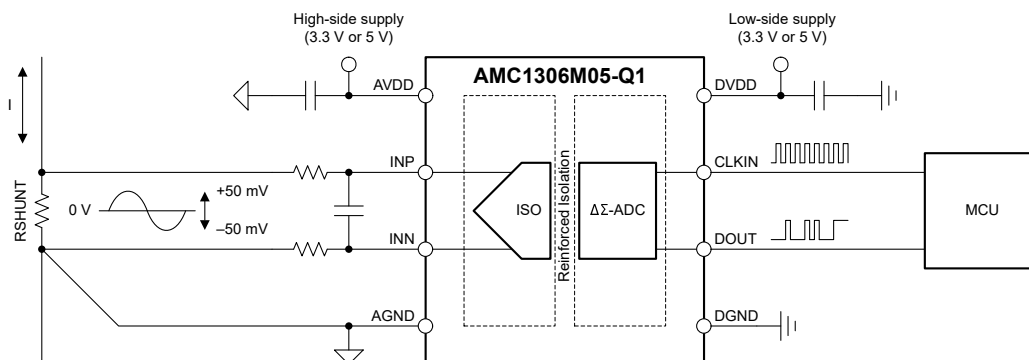
The input of the AMC1306M05-Q1 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The excellent DC accuracy and low temperature drift supports accurate current control in onboard chargers (OBC), DC/DC converters, traction inverters, or other high-voltage applications. By using an integrated digital filter (such as those in the [TMS320F2807x](#) or [TMS320F2837x](#) microcontroller families) to decimate the bitstream, the device can achieve 16 bits of resolution with a dynamic range of 85 dB at a data rate of 78 kSPS.

The AMC1306M05-Q1 is offered in a 8-pin, wide-body SOIC package, is AEC-Q100 qualified for automotive applications, and supports the temperature range from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1306M05-Q1	SOIC (8)	5.85 mm $\times$ 7.50 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application



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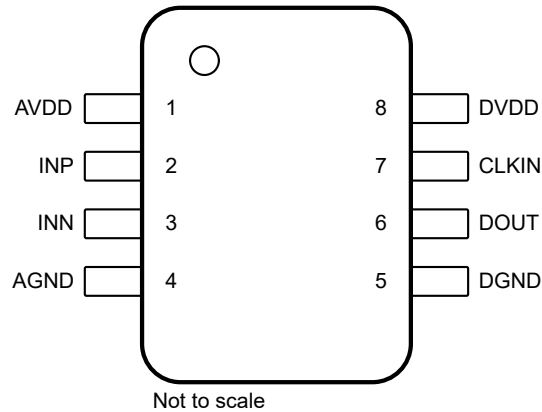
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2022	*	Initial Release

## 5 Pin Configuration and Functions



**Figure 5-1. DWV Package, 8-Pin SOIC (Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AVDD	High-side power	Analog (high-side) power supply <sup>(1)</sup>
2	INP	Analog input	Noninverting analog input
3	INN	Analog input	Inverting analog input
4	AGND	High-side ground	Analog (high-side) ground reference
5	DGND	Low-side ground	Digital (low-side) ground reference
6	DOUT	Digital output	Modulator data output
7	CLKIN	Digital input	Modulator clock input with internal pulldown resistor (typical value: 1.5 MΩ)
8	DVDD	Low-side power	Digital (low-side) power supply <sup>(1)</sup>

(1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

see<sup>(1)</sup>

PARAMETER		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	-0.3	6.5	V
	DVDD to DGND	-0.3	6.5	
Analog input voltage	INP, INN	AGND - 6	AVDD + 0.5V	V
Digital input voltage	CLKIN	DGND - 0.5	DVDD + 0.5	V
Digital output voltage	DOUT	DGND - 0.5	DVDD + 0.5	V
Input current	Continuous, any pin except power-supply pins	-10	10	mA
Temperature	Junction, T <sub>J</sub>		150	°C
	Storage, T <sub>stg</sub>	-65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> , HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification level C6	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
<b>POWER SUPPLY</b>							
AVDD	Hgh-side power supply	AVDD to AGND		3	5.0	5.5	V
DVDD	Low-side power supply	DVDD to DGND		2.7	3.3	5.5	V
<b>ANALOG INPUT</b>							
V <sub>Clipping</sub>	Differential input voltage before clipping output	V <sub>IN</sub> = V <sub>INP</sub> - V <sub>INN</sub>			±64		mV
V <sub>FSR</sub>	Specified linear differential full-scale voltage	V <sub>IN</sub> = V <sub>INP</sub> - V <sub>INN</sub>		-50		50	mV
V <sub>CM</sub>	Operating common-mode input voltage	(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to AGND		-0.032		AVDD - 2.1	V
<b>DIGITAL I/O</b>							
V <sub>IO</sub>	Digital input / output voltage			0		VDD	V
f <sub>CLKIN</sub>	Input clock frequency	4.5 V ≤ AVDD ≤ 5.5 V		5	20	21	MHz
		3.0 V ≤ AVDD ≤ 5.5 V		5	20	20	
t <sub>HIGH</sub>	Input clock high time			20	25	120	ns
t <sub>LOW</sub>	Input clock low time			20	25	120	ns
<b>TEMPERATURE RANGE</b>							
T <sub>A</sub>	Specified ambient temperature			-40		125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		AMC1306M05-Q1		
		DWV (SOIC)		UNIT
		8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	112.2	°C/W	
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	47.6	°C/W	
R <sub>θJB</sub>	Junction-to-board thermal resistance	60.0	°C/W	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	23.1	°C/W	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	60.0	°C/W	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	°C/W	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P <sub>D</sub>	Maximum power dissipation (both sides)	AVDD = DVDD = 5.5 V	87	mW
P <sub>D1</sub>	Maximum power dissipation (high-side supply)	AVDD = 3.6 V	31	mW
		AVDD = 5.5 V	54	
P <sub>D2</sub>	Maximum power dissipation (low-side supply)	DVDD = 3.6 V	17	mW
		DVDD = 5.5 V	33	

## 6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
<b>GENERAL</b>				
CLR	External clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
		Material group	According to IEC 60664-1	I
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 1000 V <sub>RMS</sub>	I-III	
<b>DIN VDE V 0884-11: 2017-01<sup>(2)</sup></b>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	At AC voltage	2120	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V <sub>RMS</sub>
		At DC voltage	2120	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification test)	7070	V <sub>PK</sub>
		V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production test)	8480	
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 60065, 1.2/50-μs waveform, V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> = 12800 V <sub>PK</sub> (qualification)	8000	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a, after input/output safety test subgroups 2 & 3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s, V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s, V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s, V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.5 V <sub>PP</sub> at 1 MHz	~1.5	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500 V at T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V at 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		40/125/21	
<b>UL1577</b>				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> = 5000 V <sub>RMS</sub> , t = 60 s (qualification), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 6000 V <sub>RMS</sub> , t = 1 s (100% production test)	5000	V <sub>RMS</sub>

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier are tied together, creating a two-pin device.

## 6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition program
Reinforced insulation	Single protection
Certificate number: pending	File number: pending

## Safety Limiting Values

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	R <sub>θJA</sub> = 112.2°C/W, AVDD = DVDD = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			203	mA
		R <sub>θJA</sub> = 112.2°C/W, AVDD = DVDD = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			309	mA
P <sub>S</sub>	Safety input, output, or total power <sup>(1)</sup>	R <sub>θJA</sub> = 112.2°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			1114	mW
T <sub>S</sub>	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where T<sub>J(max)</sub> is the maximum junction temperature.

$P_S = I_S \times AVDD_{max} + I_S \times DVDD_{max}$ , where AVDD<sub>max</sub> is the maximum high-side voltage and DVDD<sub>max</sub> is the maximum controller-side supply voltage.

## 6.8 Electrical Characteristics

minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $DVDD = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $INP = -50\text{ mV}$  to  $50\text{ mV}$ ,  $INN = 0\text{ V}$ , and sinc<sup>3</sup> filter with  $OSR = 256$  (unless otherwise noted); typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $CLKIN = 20\text{ MHz}$ ,  $AVDD = 5\text{ V}$ , and  $DVDD = 3.3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
<b>ANALOG INPUTS</b>								
$V_{CMov}$	Commonmode overvoltage detection level	$(INP + INN) / 2$ to AGND			$AVDD - 2$	V		
$C_{IN}$	Single-ended input capacitance	INN = AGND			4	pF		
$C_{IND}$	Differential input capacitance				2	pF		
$R_{IN}$	Single-ended input resistance	INN = AGND			4.75	k $\Omega$		
$R_{IND}$	Differential input resistance				4.9	k $\Omega$		
$I_{IB}$	Input bias current	INP = INN = AGND, $I_{IB} = I_{BP} + I_{BN}$			-97	-72	-57	$\mu\text{A}$
$I_{IO}$	Input offset current				$\pm 10$		nA	
CMTI	Common-mode transient immunity				100	150		kV/ $\mu\text{s}$
CMRR	Common-mode rejection ratio	INP = INN, $f_{IN} = 0\text{ Hz}$ , $V_{CM\ min} \leq V_{IN} \leq V_{CM\ max}$			-99		dB	
		INP = INN, $f_{IN}$ from 0.1 Hz to 50 kHz, $V_{CM\ min} \leq V_{IN} \leq V_{CM\ max}$			-98			
BW	Input bandwidth				800		kHz	
<b>DC ACCURACY</b>								
DNL	Differential nonlinearity	Resolution: 16 bits			-0.99	0.99	LSB	
INL	Integral nonlinearity <sup>(2)</sup>	Resolution: 16 bits, $4.5\text{ V} \leq AVDD \leq 5.5\text{ V}$			-4	$\pm 1$	4	LSB
		Resolution: 16 bits, $3.0\text{ V} \leq AVDD \leq 3.6\text{ V}$			-5	$\pm 1.5$	5	LSB
$E_O$	Offset error <sup>(1)</sup>	$T_A = 25^\circ\text{C}$ , INP = INN = GND1			-50	$\pm 2.5$	50	$\mu\text{V}$
$TCE_O$	Offset error temperature drift <sup>(3)</sup>				-1	$\pm 0.25$	1	$\mu\text{V}/^\circ\text{C}$
$E_G$	Gain error	$T_A = 25^\circ\text{C}$			-0.2%	$\pm 0.005\%$	0.2%	
$TCE_G$	Gain error temperature drift <sup>(4)</sup>				-40	$\pm 20$	40	ppm/ $^\circ\text{C}$
PSRR	Power-supply rejection ratio	INP = INN = AGND, AVDD from 3.0 V to 5.5 V, at DC			-108		dB	
		INP = INN = AGND, AVDD from 3.0 V to 5.5 V, 10 kHz / 100 mV ripple			-107			
<b>AC ACCURACY</b>								
SNR	Signal-to-noise ratio	$f_{IN} = 1\text{ kHz}$			78	82.5		dB
SINAD	Signal-to-noise + distortion	$f_{IN} = 1\text{ kHz}$			77.5	82.3		dB
THD	Total harmonic distortion <sup>(5)</sup>	$4.5\text{ V} \leq AVDD \leq 5.5\text{ V}$ , $f_{IN} = 1\text{ kHz}$ , $5\text{ MHz} \leq f_{CLKIN} \leq 21\text{ MHz}$			-98		-84	dB
		$3.0\text{ V} \leq AVDD \leq 3.6\text{ V}$ , $f_{IN} = 1\text{ kHz}$ , $5\text{ MHz} \leq f_{CLKIN} \leq 20\text{ MHz}$			-93		-83	
SFDR	Spurious-free dynamic range	$f_{IN} = 1\text{ kHz}$			83	100		dB

## 6.8 Electrical Characteristics (continued)

minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $DVDD = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $INP = -50\text{ mV}$  to  $50\text{ mV}$ ,  $INN = 0\text{ V}$ , and sinc<sup>3</sup> filter with  $OSR = 256$  (unless otherwise noted); typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $CLKIN = 20\text{ MHz}$ ,  $AVDD = 5\text{ V}$ , and  $DVDD = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CMOS LOGIC WITH SCHMITT-TRIGGER</b>						
$I_{IN}$	Input current	$DGND \leq V_{IN} \leq DVDD$	0		7	$\mu\text{A}$
$C_{IN}$	Input capacitance			4		$\text{pF}$
$V_{IH}$	High-level input voltage		$0.7 \times DVDD$		$DVDD + 0.3$	$\text{V}$
$V_{IL}$	Low-level input voltage		-0.3		$0.3 \times DVDD$	$\text{V}$
$C_{LOAD}$	Output load capacitance			30		$\text{pF}$
$V_{OH}$	High-level output voltage	$I_{OH} = -4\text{ mA}$	$DVDD - 0.4$			$\text{V}$
$V_{OL}$	Low-level output voltage	$I_{OL} = 4\text{ mA}$			0.4	$\text{V}$
<b>POWER SUPPLY</b>						
$I_{AVDD}$	High-side supply current	$3.0\text{ V} \leq AVDD \leq 3.6\text{ V}$		6.3	8.5	$\text{mA}$
		$4.5\text{ V} \leq AVDD \leq 5.5\text{ V}$		7.2	9.8	
$I_{DVDD}$	Low-side supply current	$2.7\text{ V} \leq DVDD \leq 3.6\text{ V}$ , $C_{LOAD} = 15\text{ pF}$		3.3	4.8	$\text{mA}$
		$4.5\text{ V} \leq DVDD \leq 5.5\text{ V}$ , $C_{LOAD} = 15\text{ pF}$		3.9	6.0	
$AVDD_{UV}$	High-side undervoltage detection threshold	AVDD rising	2.45	2.7	2.9	$\text{V}$
		AVDD falling	2.4	2.6	2.8	
$DVDD_{UV}$	Low-side undervoltage detection threshold	DVDD rising	2.2	2.45	2.65	$\text{V}$
		DVDD falling	1.75		2.2	

- (1) This parameter is input referred.
- (2) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
- (3) Offset error temperature drift is calculated using the box method, as described by the following equation:  

$$TCE_O = (E_{O,MAX} - E_{O,MIN}) / TempRange$$
where  $E_{O,MAX}$  and  $E_{O,MIN}$  refer to the maximum and minimum  $E_O$  values measured within the temperature range ( $-40$  to  $125^\circ\text{C}$ ).
- (4) Gain error temperature drift is calculated using the box method, as described by the following equation:  

$$TCE_G (\text{ppm}) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$$
where  $E_{G,MAX}$  and  $E_{G,MIN}$  refer to the maximum and minimum  $E_G$  values (in %) measured within the temperature range ( $-40$  to  $125^\circ\text{C}$ ).
- (5) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.

## Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_H$	DOUT hold time after rising edge of CLKIN	$C_{LOAD} = 15\text{ pF}$	3.5			ns
$t_D$	Rising edge of CLKIN to DOUT valid delay	$C_{LOAD} = 15\text{ pF}$			15	ns
$t_r$	DOUT rise time	10% to 90%, $2.7\text{ V} \leq DVDD \leq 3.6\text{ V}$ , $C_{LOAD} = 15\text{ pF}$		2.5	6	ns
		10% to 90%, $4.5\text{ V} \leq DVDD \leq 5.5\text{ V}$ , $C_{LOAD} = 15\text{ pF}$		3.2	6	
$t_f$	DOUT fall time	10% to 90%, $2.7\text{ V} \leq DVDD \leq 3.6\text{ V}$ , $C_{LOAD} = 15\text{ pF}$		2.2	6	ns
		10% to 90%, $4.5\text{ V} \leq DVDD \leq 5.5\text{ V}$ , $C_{LOAD} = 15\text{ pF}$		2.9	6	
$t_{START}$	Device start-up time	AVDD step from 0 to 3.0 V with $DVDD \geq 2.7\text{ V}$ to bitstream valid, 0.1% settling		0.5		ms

## 6.9 Timing Diagrams

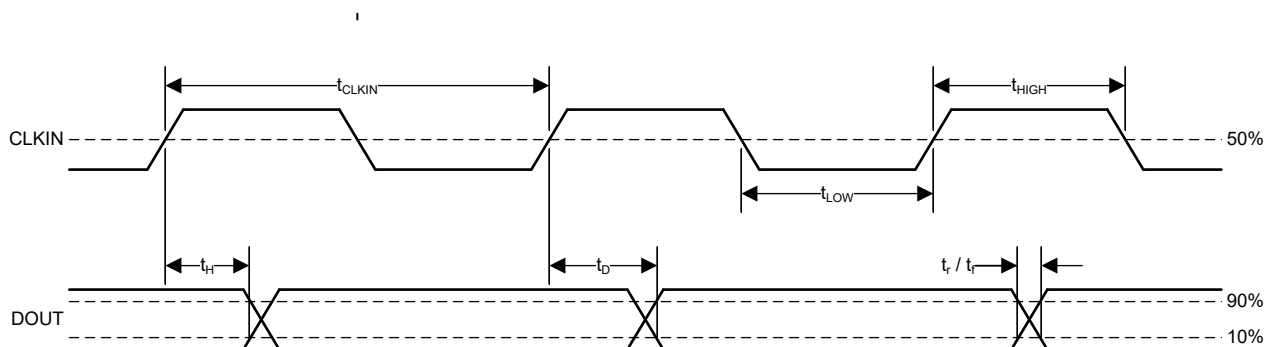


Figure 6-1. Digital Interface Timing

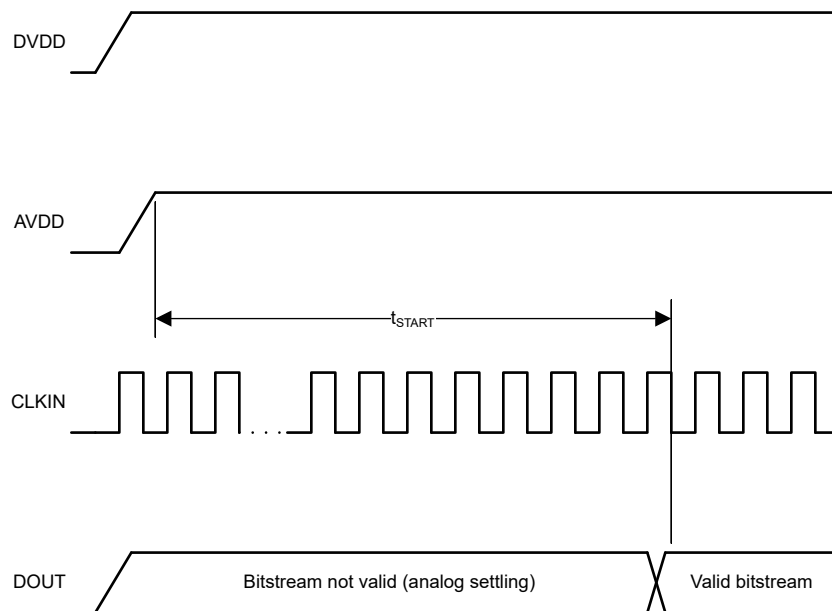
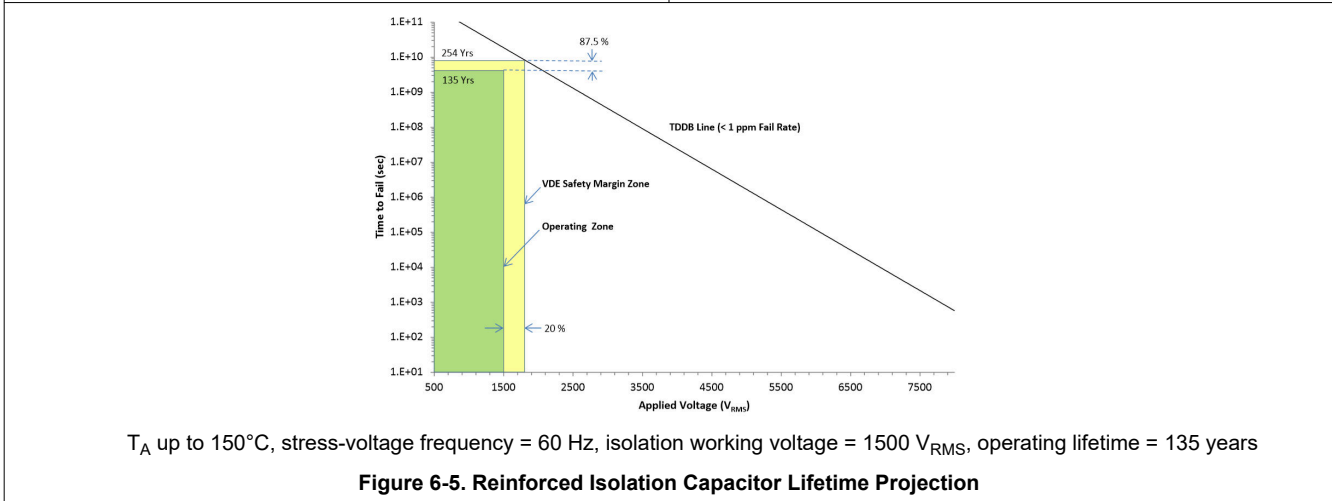
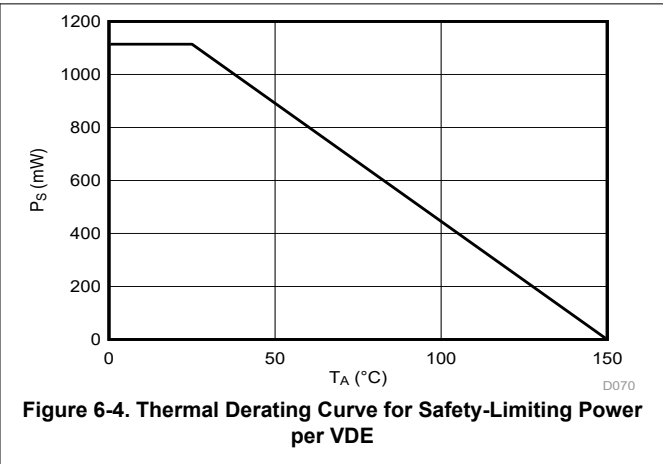
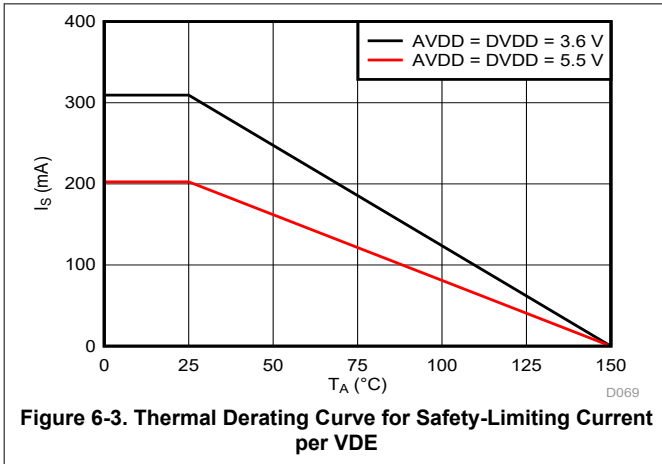


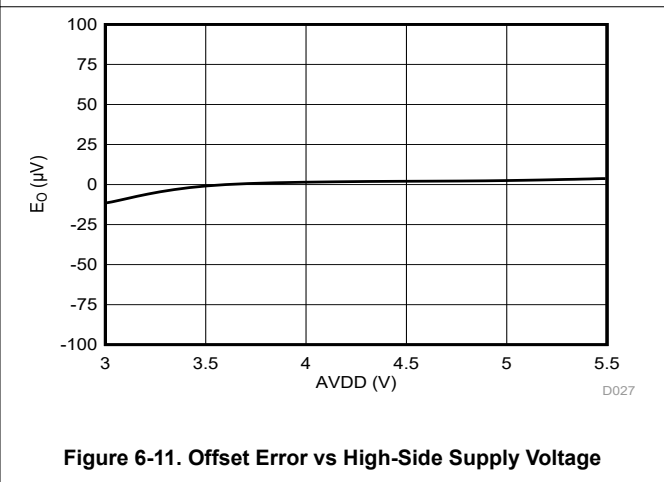
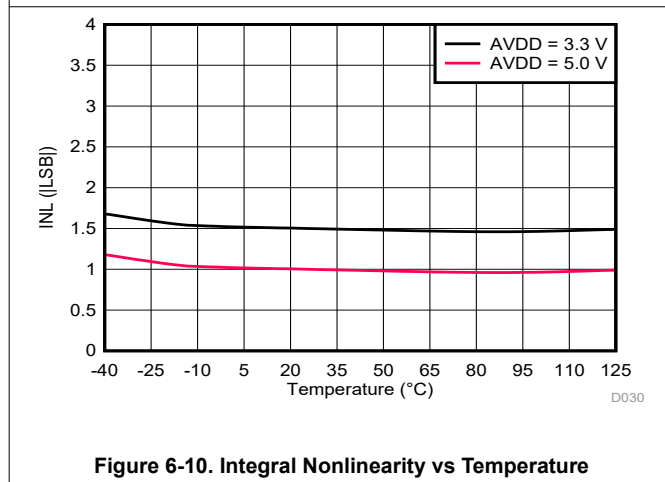
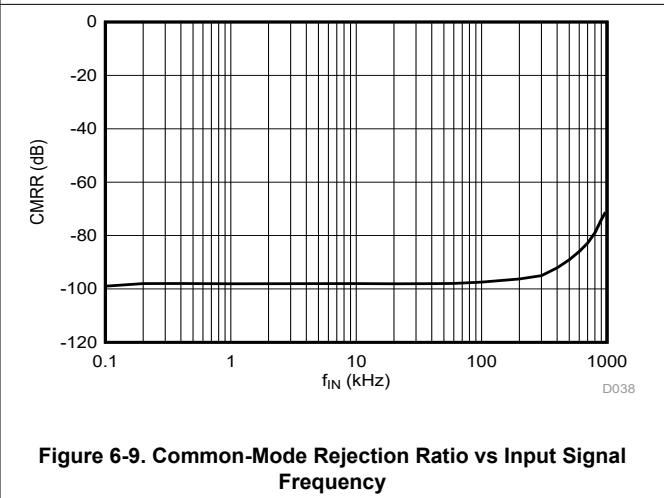
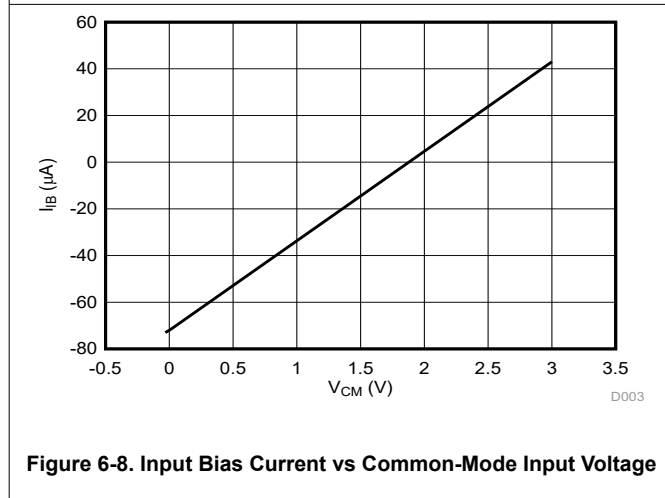
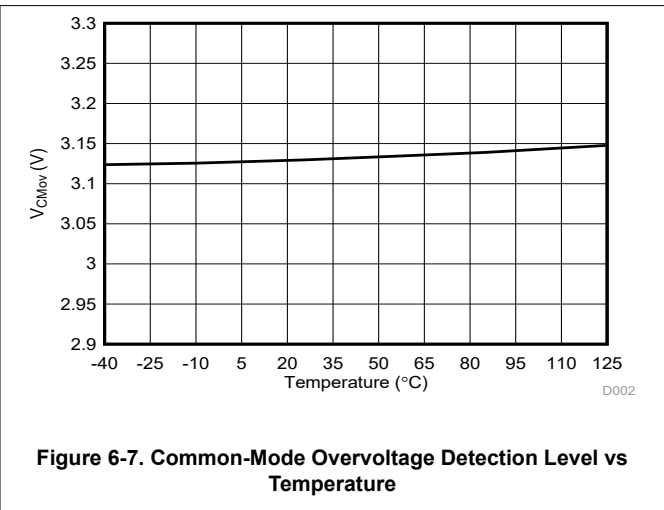
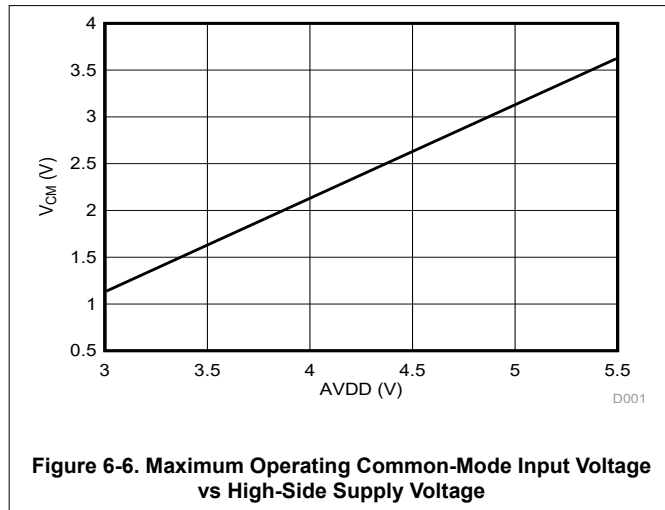
Figure 6-2. Device Start-Up Timing

### 6.10 Insulation Characteristics Curves



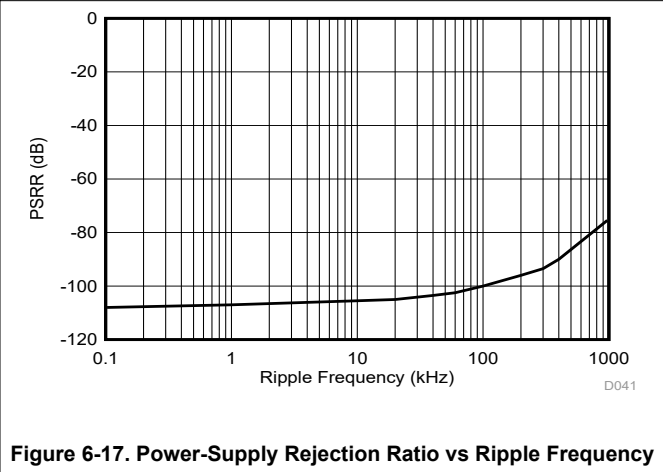
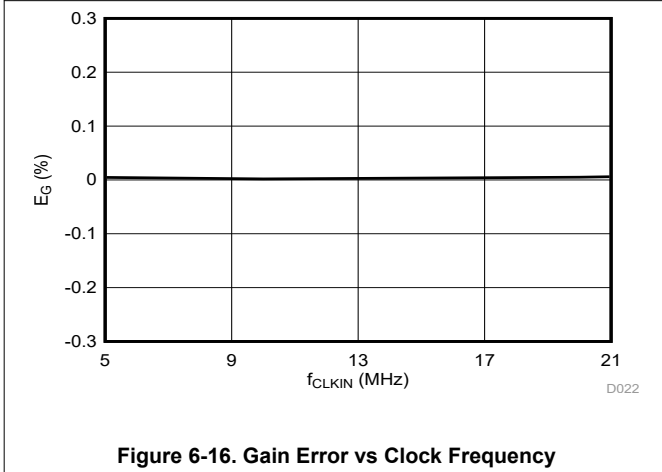
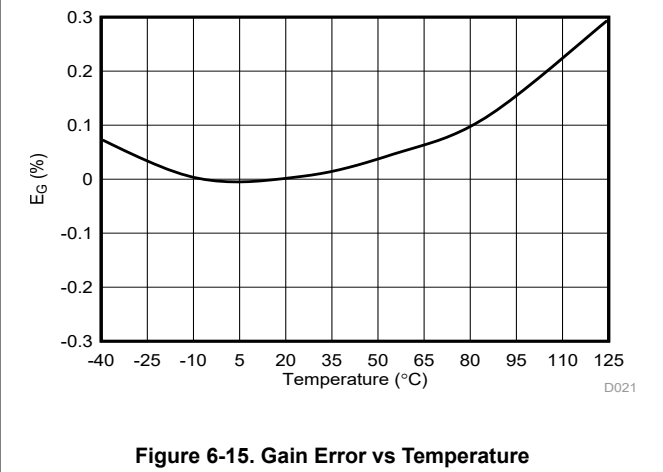
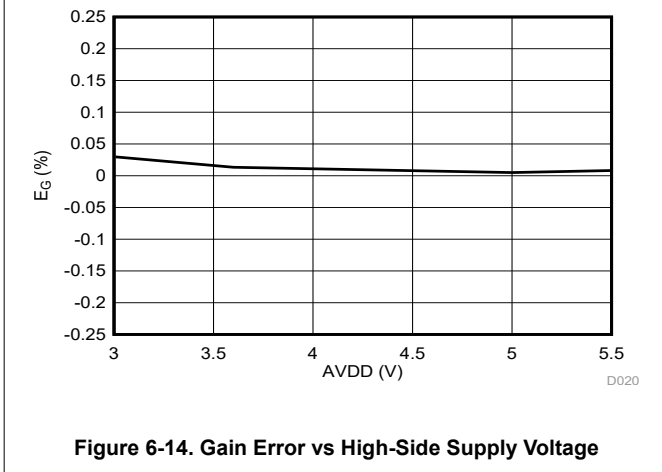
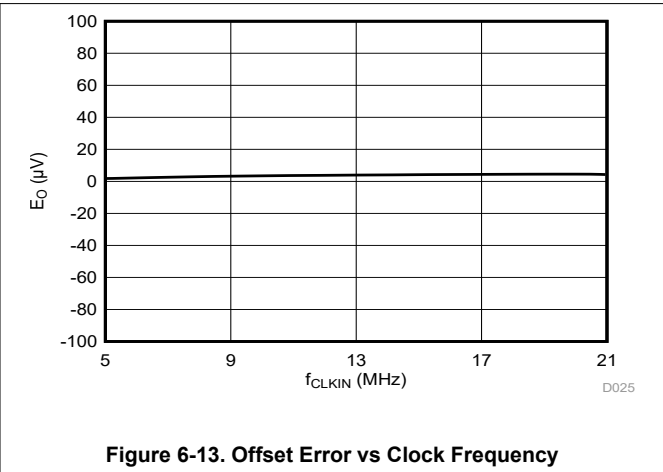
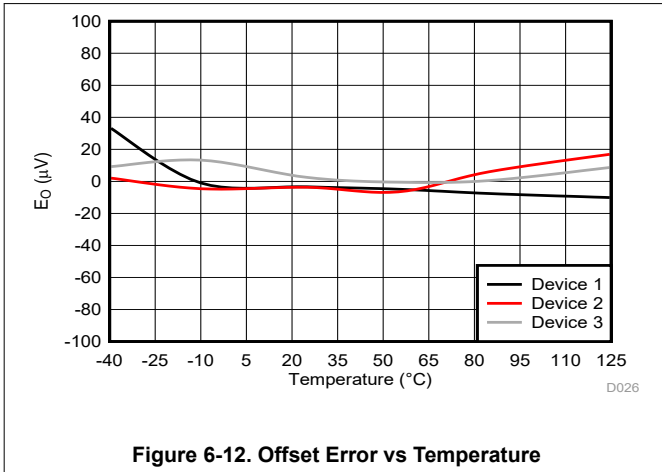
## 6.11 Typical Characteristics

at AVDD = 5 V, DVDD = 3.3 V, INP = -50 mV to 50 mV, INN = AGND, f<sub>CLKIN</sub> = 20 MHz, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)



### 6.11 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = -50 mV to 50 mV, INN = AGND, f<sub>CLKIN</sub> = 20 MHz, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)



## 6.11 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = -50 mV to 50 mV, INN = AGND,  $f_{CLKIN} = 20$  MHz, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)

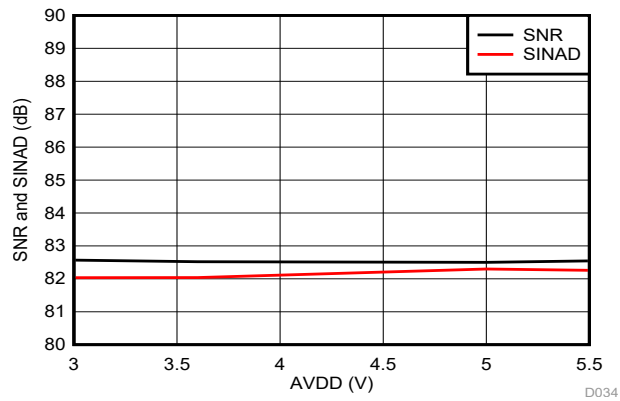


Figure 6-18. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs High-Side Supply Voltage

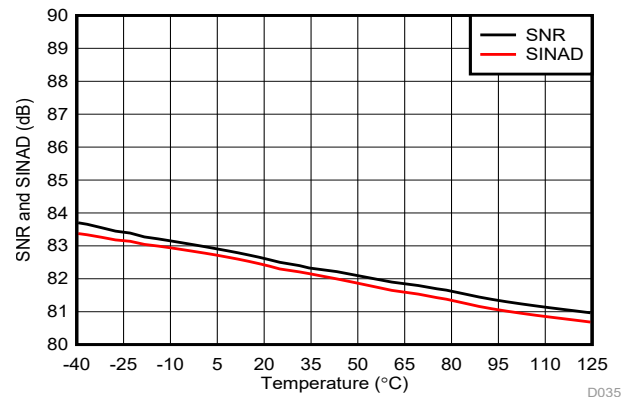


Figure 6-19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

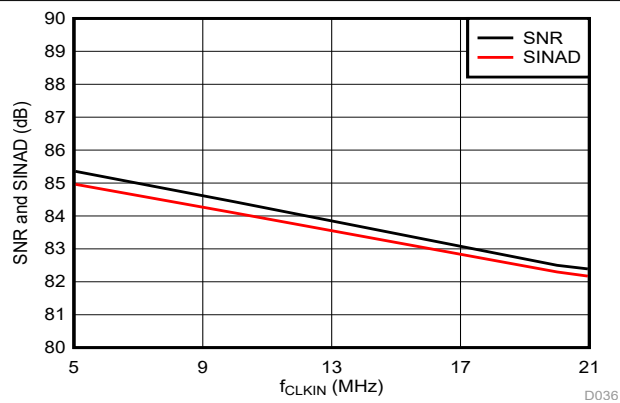


Figure 6-20. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency

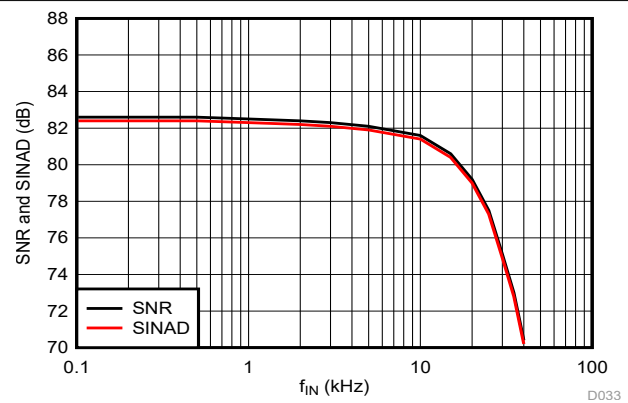


Figure 6-21. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

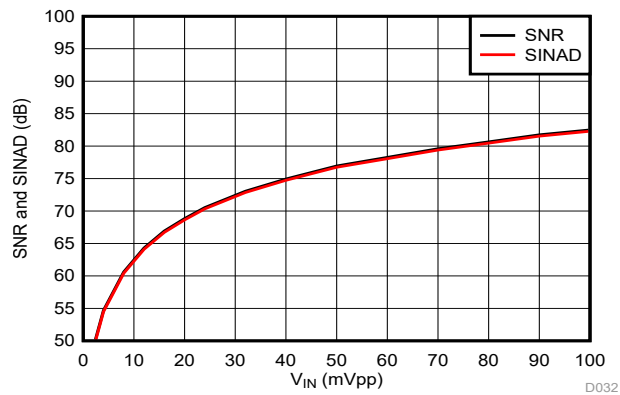


Figure 6-22. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

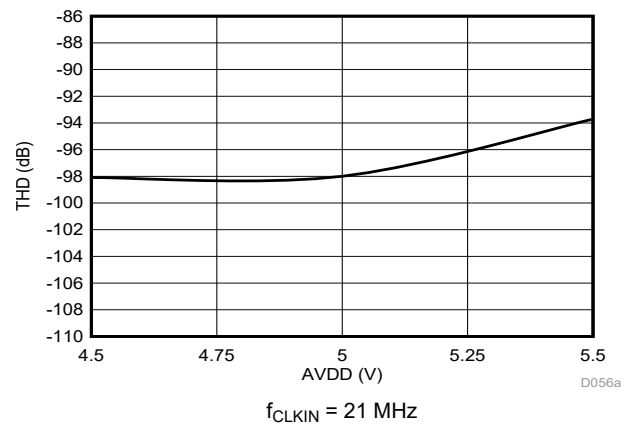
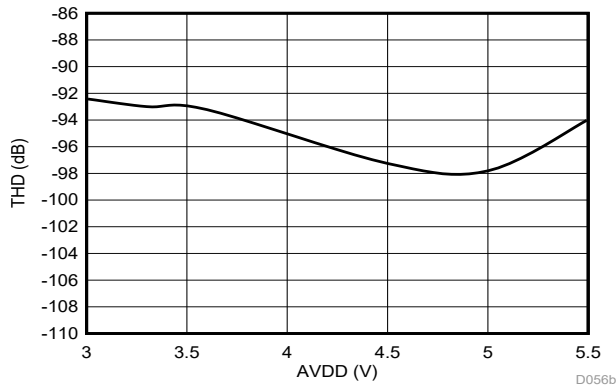


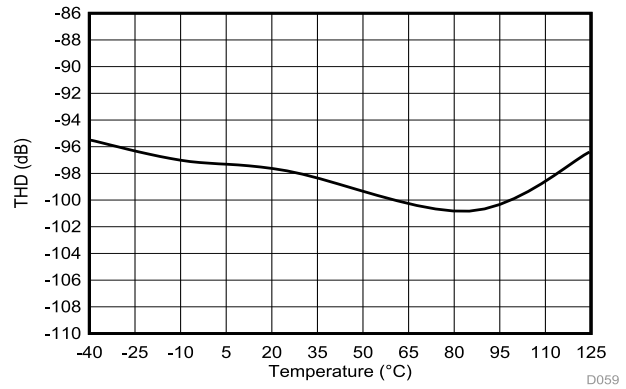
Figure 6-23. Total Harmonic Distortion vs High-Side Supply Voltage (5 V, nom)

### 6.11 Typical Characteristics (continued)

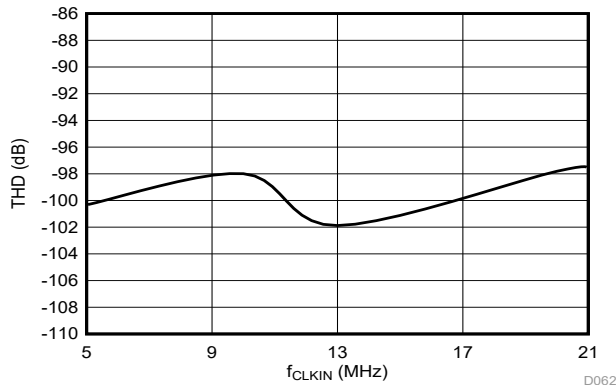
at AVDD = 5 V, DVDD = 3.3 V, INP = -50 mV to 50 mV, INN = AGND, f<sub>CLKIN</sub> = 20 MHz, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)



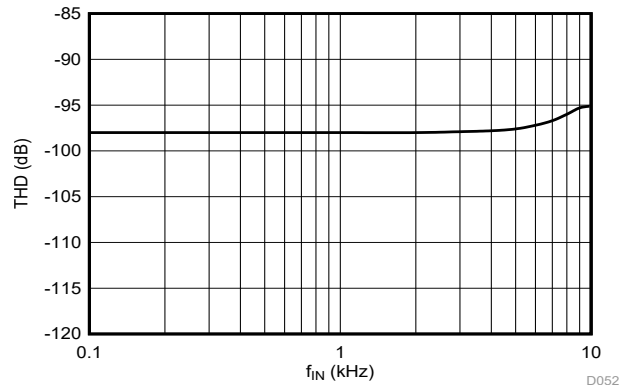
**Figure 6-24. Total Harmonic Distortion vs High-Side Supply Voltage (3.3 V, nom)**



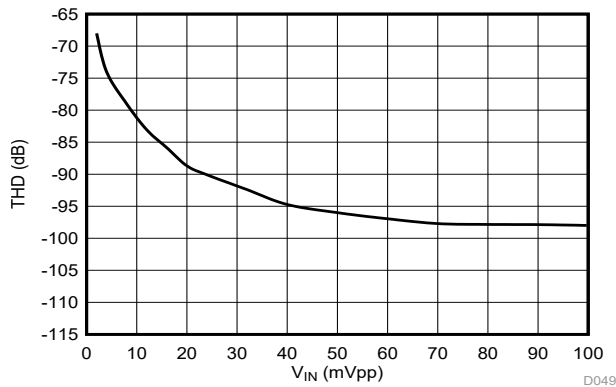
**Figure 6-25. Total Harmonic Distortion vs Temperature**



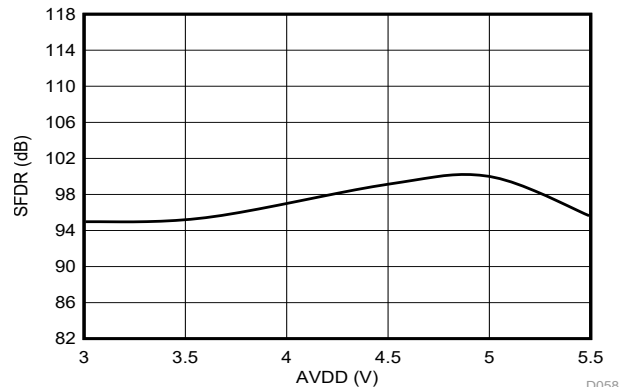
**Figure 6-26. Total Harmonic Distortion vs Clock Frequency**



**Figure 6-27. Total Harmonic Distortion vs Input Signal Frequency**



**Figure 6-28. Total Harmonic Distortion vs Input Signal Amplitude**



**Figure 6-29. Spurious-Free Dynamic Range vs High-Side Supply Voltage**

## 6.11 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = -50 mV to 50 mV, INN = AGND,  $f_{CLKIN} = 20$  MHz, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)

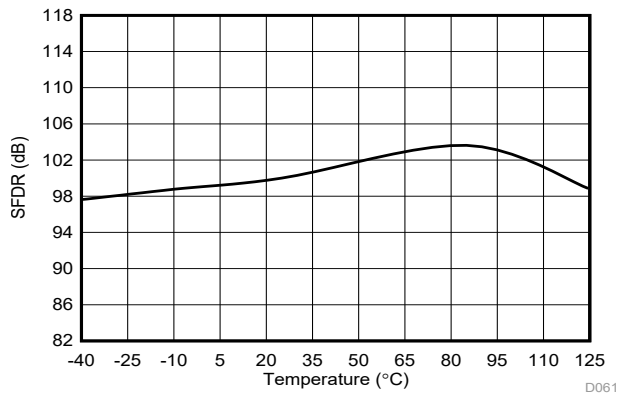


Figure 6-30. Spurious-Free Dynamic Range vs Temperature

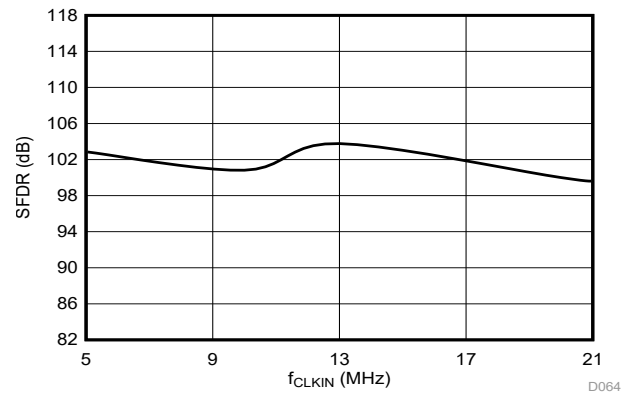


Figure 6-31. Spurious-Free Dynamic Range vs Clock Frequency

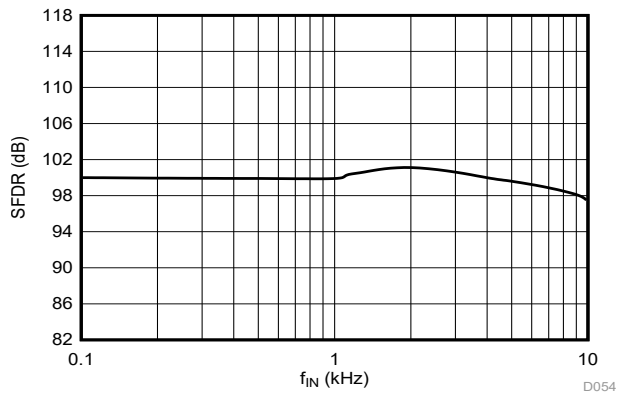


Figure 6-32. Spurious-Free Dynamic Range vs Input Signal Frequency

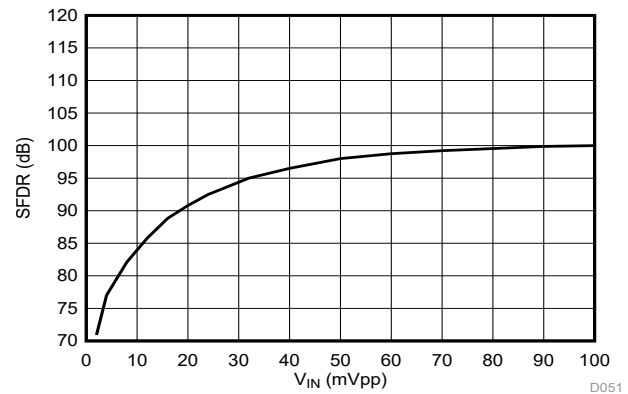


Figure 6-33. Spurious-Free Dynamic Range vs Input Signal Amplitude

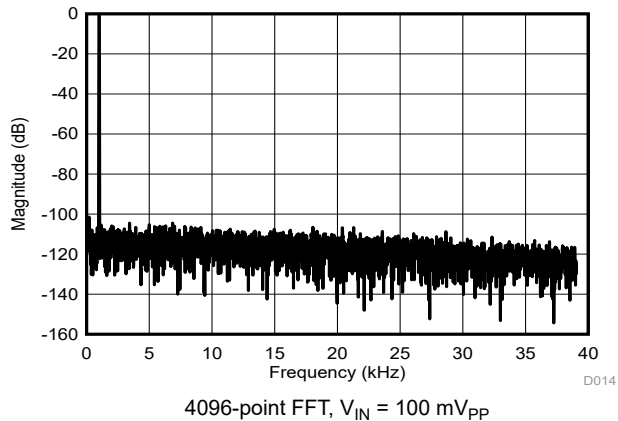


Figure 6-34. Frequency Spectrum With 1-kHz Input Signal

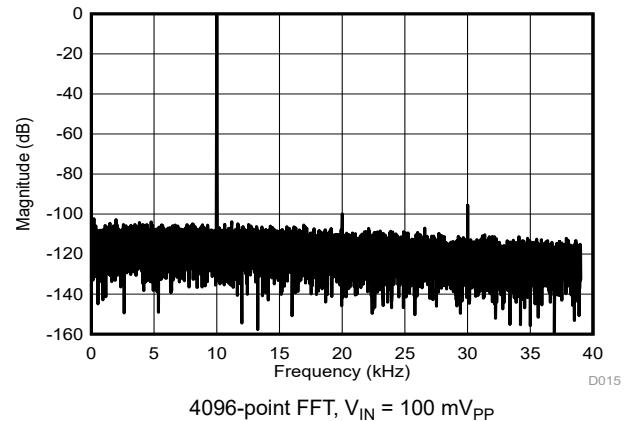


Figure 6-35. Frequency Spectrum With 10-kHz Input Signal

### 6.11 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = -50 mV to 50 mV, INN = AGND, f<sub>CLKIN</sub> = 20 MHz, and sinc<sup>3</sup> filter with OSR = 256 (unless otherwise noted)

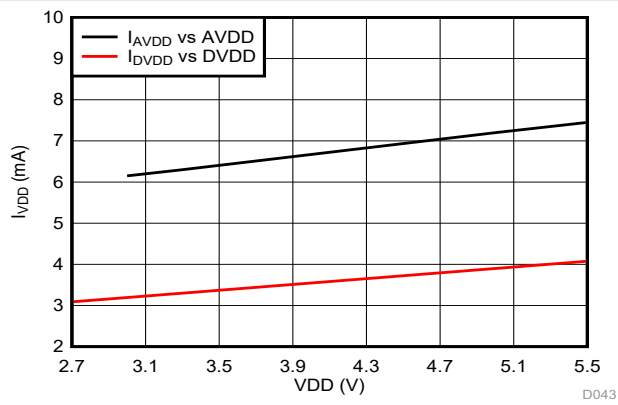


Figure 6-36. Supply Current vs Supply Voltage

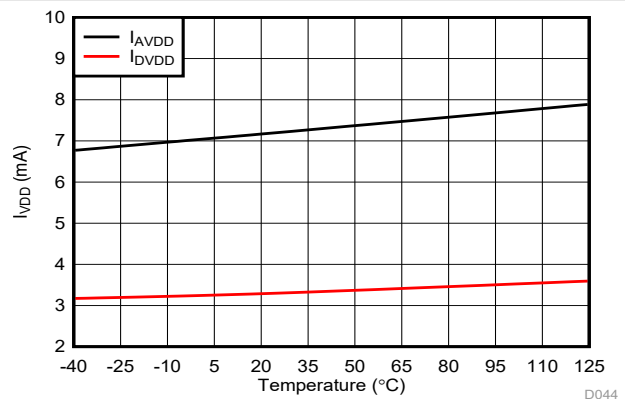


Figure 6-37. Supply Current vs Temperature

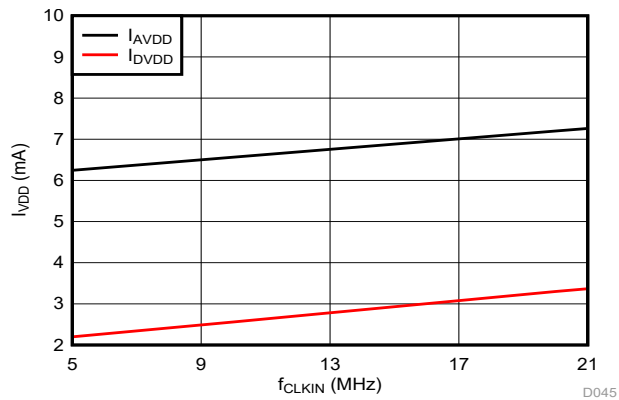


Figure 6-38. Supply Current vs Clock Frequency

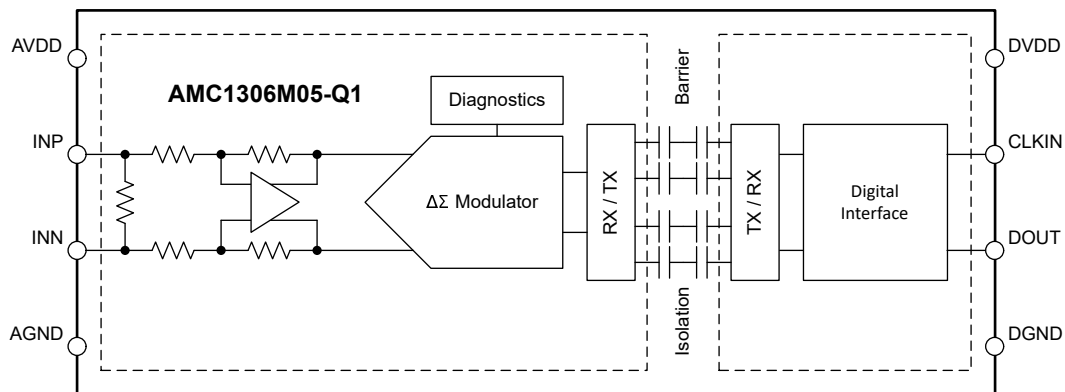
## 7 Detailed Description

### 7.1 Overview

The input stage of the AMC1306M05-Q1 consists of a fully differential amplifier that feeds the switched-capacitor input of a second-order, delta-sigma ( $\Delta\Sigma$ ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. The isolated data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the externally provided clock source at the CLKIN pin. The time average of this serial bitstream output is proportional to the analog input voltage. The external clock input simplifies the synchronization of multiple current-sensing channels on the system level.

The silicon-dioxide ( $\text{SiO}_2$ ) based capacitive isolation barrier supports a high level of magnetic field immunity as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application report](#). The digital modulation used in the AMC1306M05-Q1 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

### 7.2 Functional Block Diagram

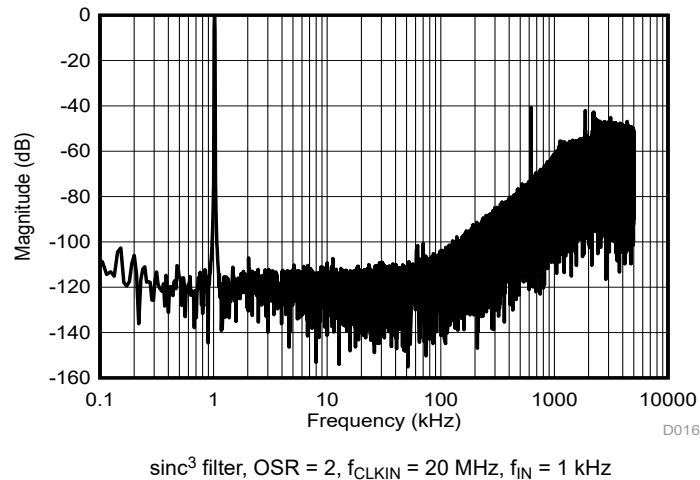


## 7.3 Feature Description

### 7.3.1 Analog Input

The differential amplifier input stage of the AMC1306M05-Q1 feeds a second-order, switched-capacitor, feed-forward  $\Delta\Sigma$  modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of  $R_{IND}$ . The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the [Isolation Channel Signal Transmission](#) section.

For reduced offset and offset drift, the differential amplifier is chopper-stabilized with the switching frequency set at  $f_{CLKIN} / 32$ . As shown in [Figure 7-1](#), the switching frequency generates a spur at 625 kHz.

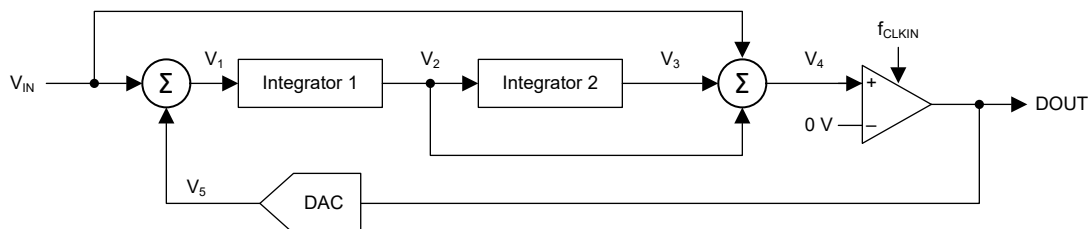


**Figure 7-1. Quantization Noise Shaping**

There are two restrictions on the analog input signals INP and INN. First, if the input voltages  $V_{INP}$  or  $V_{INN}$  exceed the range specified in the [Absolute Maximum Ratings](#) table, the input currents must be limited to the absolute maximum value because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range ( $V_{FSR}$ ) and within the common-mode input voltage range ( $V_{CM}$ ) as specified in the [Recommended Operating Conditions](#) table.

### 7.3.2 Modulator

[Figure 7-2](#) conceptualizes the second-order, switched-capacitor, feed-forward  $\Delta\Sigma$  modulator implemented in the AMC1306M05-Q1. The analog input voltage  $V_{IN}$  and the output  $V_5$  of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage  $V_1$  at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage  $V_3$  that is differentiated with the input signal  $V_{IN}$  and the output of the first integrator  $V_2$ . Depending on the polarity of the resulting voltage  $V_4$ , the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage  $V_5$ , causing the integrators to progress in the opposite direction, and forcing the value of the integrator output to track the average value of the input.



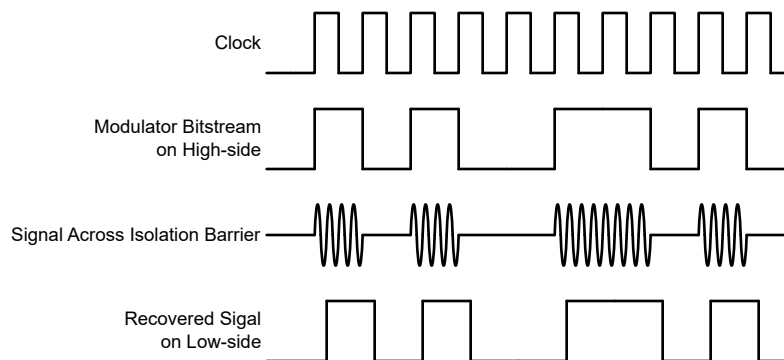
**Figure 7-2. Block Diagram of a Second-Order Modulator**

The modulator shifts the quantization noise to high frequencies, as illustrated in [Figure 7-1](#). Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's [C2000™](#) and [Sitara™](#) microcontroller families offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1306M05-Q1. Alternatively, a field-programmable gate array (FPGA) or complex programmable logic device (CPLD) can be used to implement the filter.

### 7.3.3 Isolation Channel Signal Transmission

The AMC1306M05-Q1 uses an on-off keying (OOK) modulation scheme, as shown in [Figure 7-3](#), to transmit the modulator output bitstream across the SiO<sub>2</sub>-based isolation barrier. The transmit driver (TX) shown in the [Functional Block Diagram](#) transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1306M05-Q1 is 480 MHz.

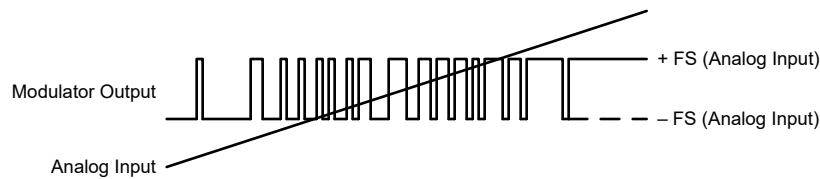
The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and produces the output. The AMC1306M05-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.



**Figure 7-3. OOK-Based Modulation Scheme**

### 7.3.4 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 50 mV produces a stream of ones and zeros that are high 89.06% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58368. A differential input of –50 mV produces a stream of ones and zeros that are high 10.94% of the time and ideally results in code 7168 with 16-bit resolution. These input voltages are also the specified linear range of the AMC1306M05-Q1. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior as the quantization noise increases. The output of the modulator clips with a constant stream of zeros with an input less than or equal to –64 mV or with a constant stream of ones with an input greater than or equal to 64 mV. In this case, however, the AMC1306M05-Q1 generates a single 1 (if the input is at negative full-scale) or 0 (if the input is at positive full-scale) every 128 clock cycles to indicate proper device function (see the [Output Behavior in Case of a Full-Scale Input](#) section for more details). [Figure 7-4](#) shows the input voltage versus the output modulator signal.



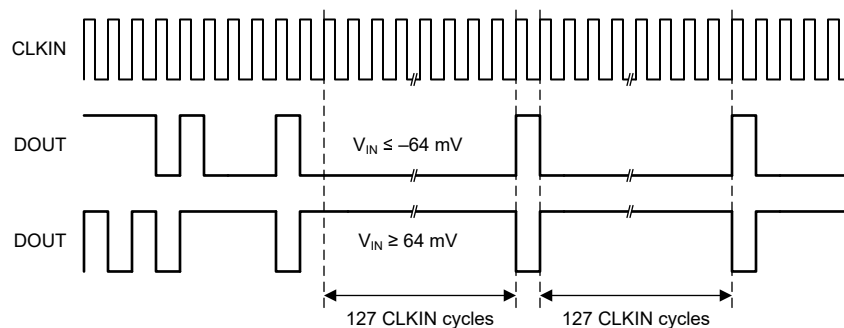
**Figure 7-4. AMC1306M05-Q1 Modulator Output vs Analog Input**

The density of ones in the output bitstream can be calculated using [Equation 1](#) for any input voltage ( $V_{IN} = V_{INP} - V_{INN}$ ) value with the exception of a full-scale input signal, as described in [Equation 1](#):

$$\rho = \frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

#### 7.3.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1306M05-Q1 (that is,  $|V_{IN}| \geq |V_{Clipping}|$ ), the device generates a single one or zero every 128 bits at DOUT, as shown in [Figure 7-5](#), depending on the actual polarity of the signal being sensed. In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level.



**Figure 7-5. Output of the AMC1306M05-Q1 in Case of an Input Overrange**

### 7.3.4.2 Output Behavior in Case of Input Common-Mode Overrange

If INN or INP is disconnected from the shunt resistor, the input bias current of the AMC1306M05-Q1 drives the disconnected terminal towards the positive supply rail, and the common-mode input voltage increases. A similar effect happens when there is no DC current path between INN, INP, and HGND. If the input common-mode voltage exceeds the common-mode overvoltage detection threshold  $V_{CMov}$ , the device provides a constant bitstream of logic 1's at the output, as shown in Figure 7-6; that is, DOUT is permanently high. A zero is not generated every 128 clock pulses, which differentiates this condition from a valid positive full-scale input. This feature is useful to identify interconnect problems on the board.

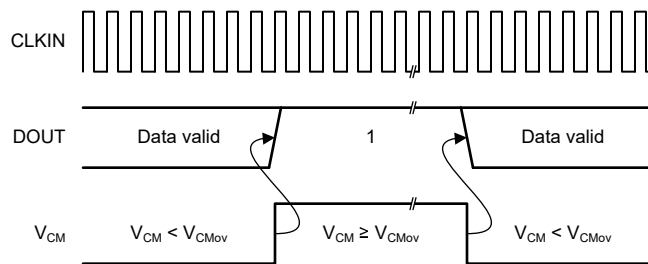


Figure 7-6. Output of the AMC1306M05-Q1 in Case of a Common-Mode Overvoltage

There is no common-mode overvoltage detection in the negative direction; thus, if the common-mode input voltage is below the minimum  $V_{CM}$  value specified in the [Recommended Operating Conditions](#) table, the bitstream at the DOUT output is not determined.

### 7.3.4.3 Output Behavior in Case of a Missing High-Side Supply

If the high-side supply is missing, the device provides a constant bitstream of logic 0's at the output, as shown in Figure 7-7; that is, DOUT is permanently low. A one is not generated every 128 clock pulses, which differentiates this condition from a valid negative full-scale input. This feature is useful to identify high-side power-supply problems on the board.

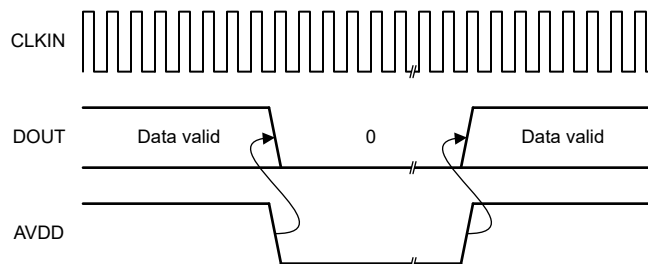


Figure 7-7. Output of the AMC1306M05-Q1 in Case of a Missing High-Side Supply

## 7.4 Device Functional Modes

The AMC1306M05-Q1 is operational when the power supplies AVDD and DVDD are applied as specified in the [Recommended Operating Conditions](#) table.



## 8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

**Table 8-1. Design Requirements**

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across RSHUNT for a linear response	±50 mV (maximum)

## 8.2.2 Detailed Design Procedure

In Figure 8-1, the high-side power supply (AVDD) for the AMC1306M05-Q1 is derived from the floating power supply of the upper gate driver, using a resistor (R4) and a Zener diode (D1).

The floating ground reference (AGND) is derived from the end of the shunt resistor that is connected to the negative input of the AMC1306M05-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC1306M05-Q1 are connected to the inner leads and AGND is connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting AGND to INN directly at the input to the device. See the [Layout](#) section for more details.

### 8.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor ( $V_{SHUNT}$ ) for the desired measured current:  $V_{SHUNT} = I \times RSHUNT$ .

Consider the following two restrictions when selecting the value of the shunt resistor, RSHUNT:

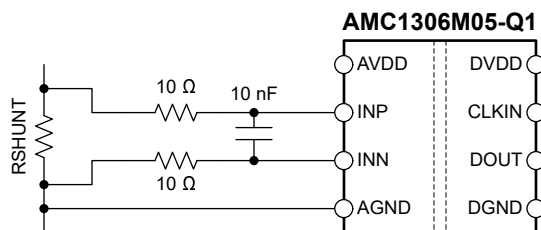
- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range for a linear response:  $|V_{SHUNT}| \leq |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output:  $|V_{SHUNT}| \leq |V_{Clipping}|$

### 8.2.2.2 Input Filter Design

Place an RC filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency ( $f_{CLKIN}$ ) of the  $\Delta\Sigma$  modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications, the structure shown in Figure 8-2 achieves excellent performance.



**Figure 8-2. Differential Input Filter**

### 8.2.2.3 Bitstream Filtering

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). As described by Equation 2, a very simple filter built with minimal effort and hardware, is a sinc<sup>3</sup>-type filter:

$$H(z) = \left( \frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All characterization in this document is also done with a sinc<sup>3</sup> filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits, unless specified otherwise. The measured effective number of bits (ENOB) as a function of the OSR is illustrated in Figure 8-3 of the *Typical Application* section.

A *Delta Sigma Modulator Filter Calculator* is available for download at [www.ti.com](http://www.ti.com) that aids in the filter design and selecting the right OSR and filter order to achieve the desired output resolution and filter response time.

An example code for implementing a sinc<sup>3</sup> filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at [www.ti.com](http://www.ti.com).

For modulator output bitstream filtering, a device from TI's C2000™ or Sitara™ microcontroller families is recommended. These families support up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high-accuracy results for the control loop and one fast-response path for overcurrent detection.

A *delta sigma modulator filter calculator* is available for download at [www.ti.com](http://www.ti.com) that aids in the filter design and selecting the right OSR and filter order to achieve the desired output resolution and filter response time.

### 8.2.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 8-3 shows the ENOB of the AMC1306M05-Q1 with different oversampling ratios. By using Equation 3, this number can also be calculated from the SINAD:

$$SINAD = 1.76 \text{ dB} + 6.02 \text{ dB} \times ENOB \quad (3)$$

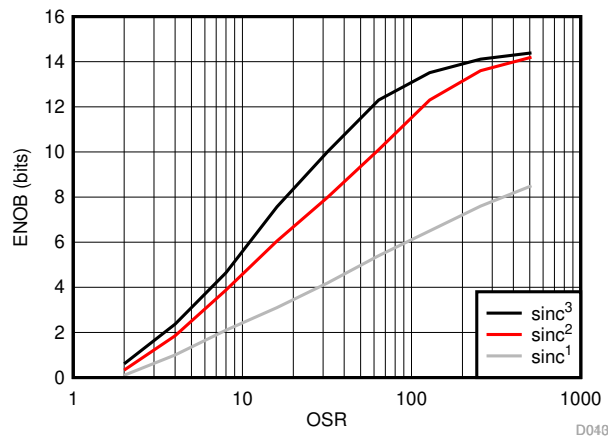


Figure 8-3. Measured Effective Number of Bits vs Oversampling Ratio

### 8.3 What to Do and What Not to Do

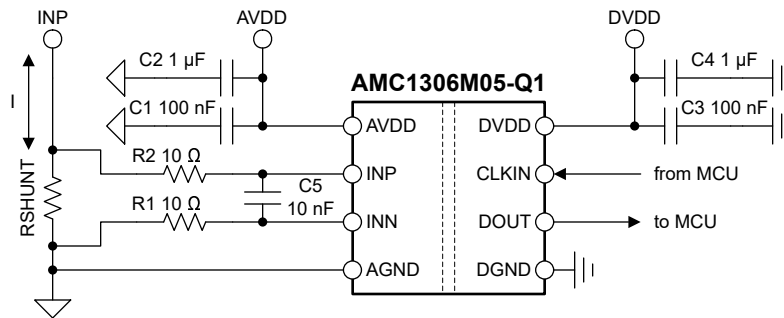
Do not leave the inputs of the AMC1306M05-Q1 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and DOUT is permanently high as described in the [Output Behavior in Case of Input Common-Mode Overrange](#) section.

Connect the high-side ground (AGND) to INN, either by a hard short or through a resistive path. A DC current path between INN and AGND is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the [Recommended Operating Conditions](#) table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting AGND to INN directly at the input to the device. See the [Layout](#) section for more details.

## 9 Power Supply Recommendations

The AMC1306M05-Q1 does not require any specific power-up sequencing. The high-side power supply (AVDD) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1- $\mu$ F capacitor (C2). The low-side power supply (DVDD) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1- $\mu$ F capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

The ground reference for the high-side (AGND) is derived from the end of the shunt resistor that is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace to make this connection instead of shorting AGND to INN directly at the device input. If a four-terminal shunt is used, the device inputs are connected to the inner leads and AGND is connected to the outer lead on the INN-side of the shunt. [Figure 9-1](#) shows a decoupling diagram of the AMC1306M05-Q1.



**Figure 9-1. Decoupling of the AMC1306M05-Q1**

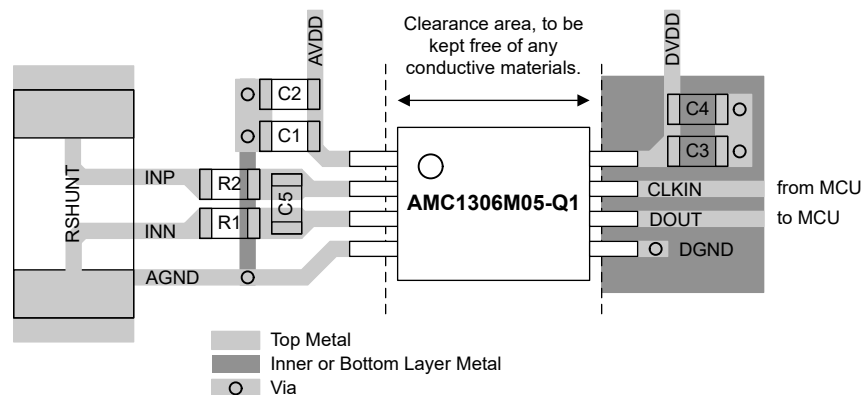
Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

## 10 Layout

### 10.1 Layout Guidelines

[Figure 10-1](#) shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1306M05-Q1 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1306M05-Q1 and keep the layout of both connections symmetrical.

### 10.2 Layout Example



**Figure 10-1. Recommended Layout of the AMC1306M05-Q1**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Isolation Glossary application report](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application report](#)
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity application report](#)
- Texas Instruments, [Delta Sigma Modulator Filter Calculator design tool](#)

#### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 11.4 Trademarks

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#### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1306M05QDWVRQ1	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF AMC1306M05-Q1 :**

- Catalog : [AMC1306M05](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

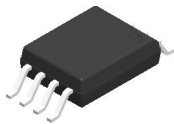

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1306M05QDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

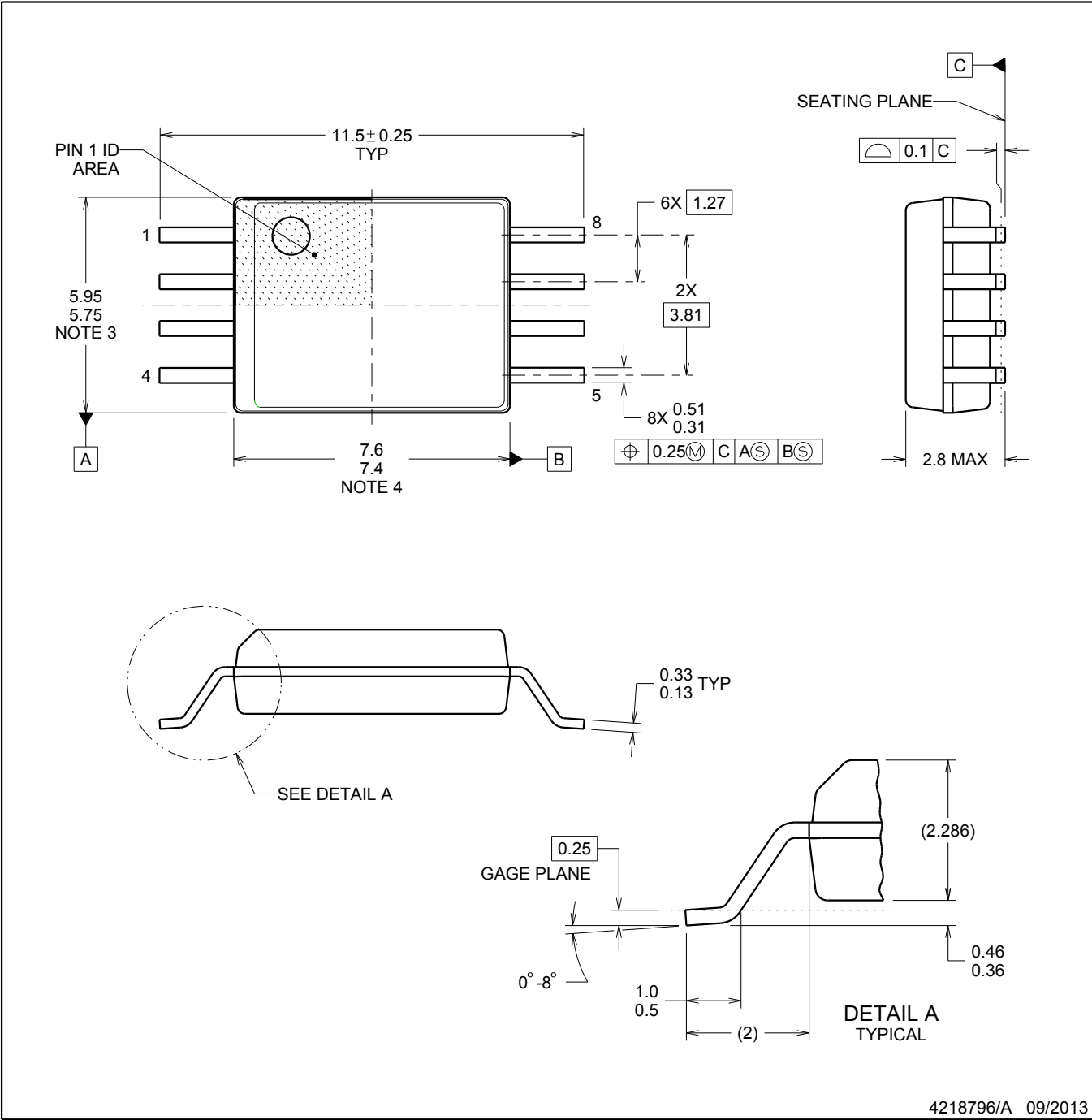
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1306M05QDWVRQ1	SOIC	DWV	8	1000	356.0	356.0	35.0



DWV0008A

SOIC - 2.8 mm max height

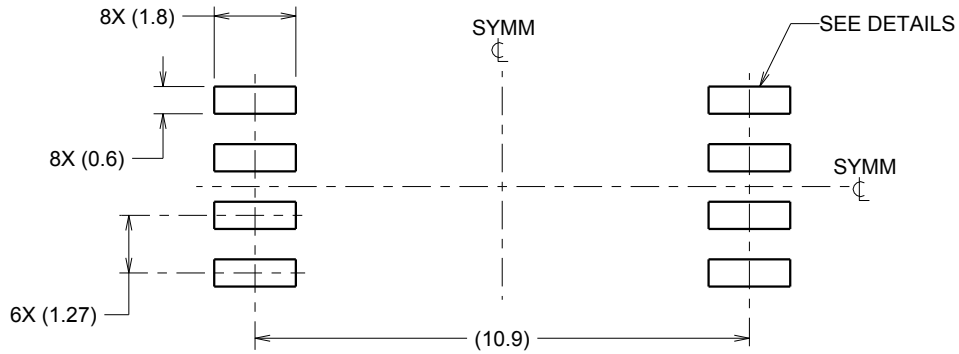
SOIC



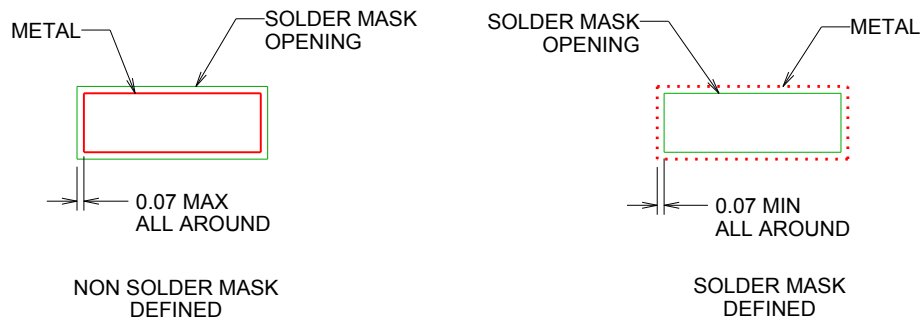
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NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE  
9.1 mm NOMINAL CLEARANCE/CREEPAGE  
SCALE:6X

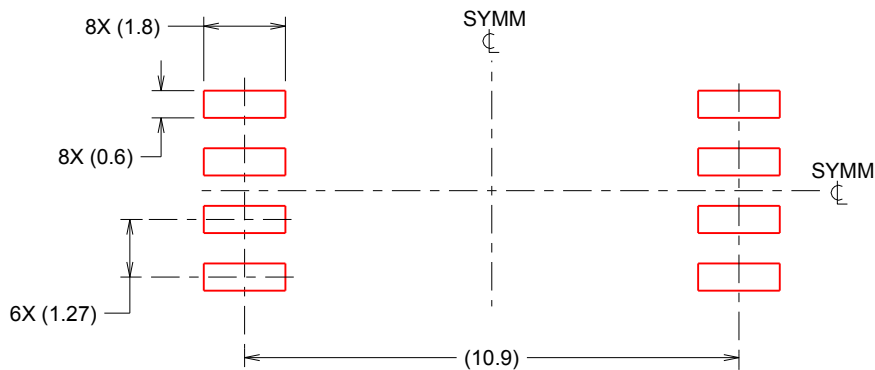


SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:6X

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NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.

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