



**THE DATASHEET OF
MR256A08BCYS35**



FEATURES

- 3.3 Volt power supply
- Fast 35 ns read/write cycle
- SRAM compatible timing
- Native non-volatility
- Unlimited read & write endurance
- Data always non-volatile for >20 years at temperature
- Commercial and industrial temperatures
- All products meet MSL-3 moisture sensitivity level
- RoHS-Compliant TSOP2 and BGA packages

BENEFITS

- One memory replaces FLASH, SRAM, EEPROM and MRAM in system for simpler, more efficient design
- Improves reliability by replacing battery-backed SRAM

INTRODUCTION

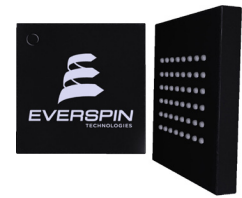
The **MR256A08B** is a 262,144-bit magnetoresistive random access memory (MRAM) device organized as 32,768 words of 8 bits. The MR256A08B offers SRAM compatible 35ns read/write timing with unlimited endurance.

Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The MR256A08B is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

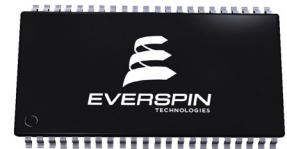
The **MR256A08B** is available in a small footprint 400-mil, 44-lead plastic small-outline TSOP type-2 package, or an 8 mm x 8 mm, 48-pin ball grid array (BGA) package. (The 32-SOIC package options is obsolete and no longer available for new orders.) All package footprints are compatible with similar low-power SRAM products and other non-volatile RAM products.

The **MR256A08B** provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70 °C) and industrial temperature (-40 to +85 °C) range options.

32K x 8 MRAM



48-ball FBGA



44-pin TSOP2



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BLOCK DIAGRAM AND PIN ASSIGNMENTS

Figure 1 – MR256A08B Block Diagram

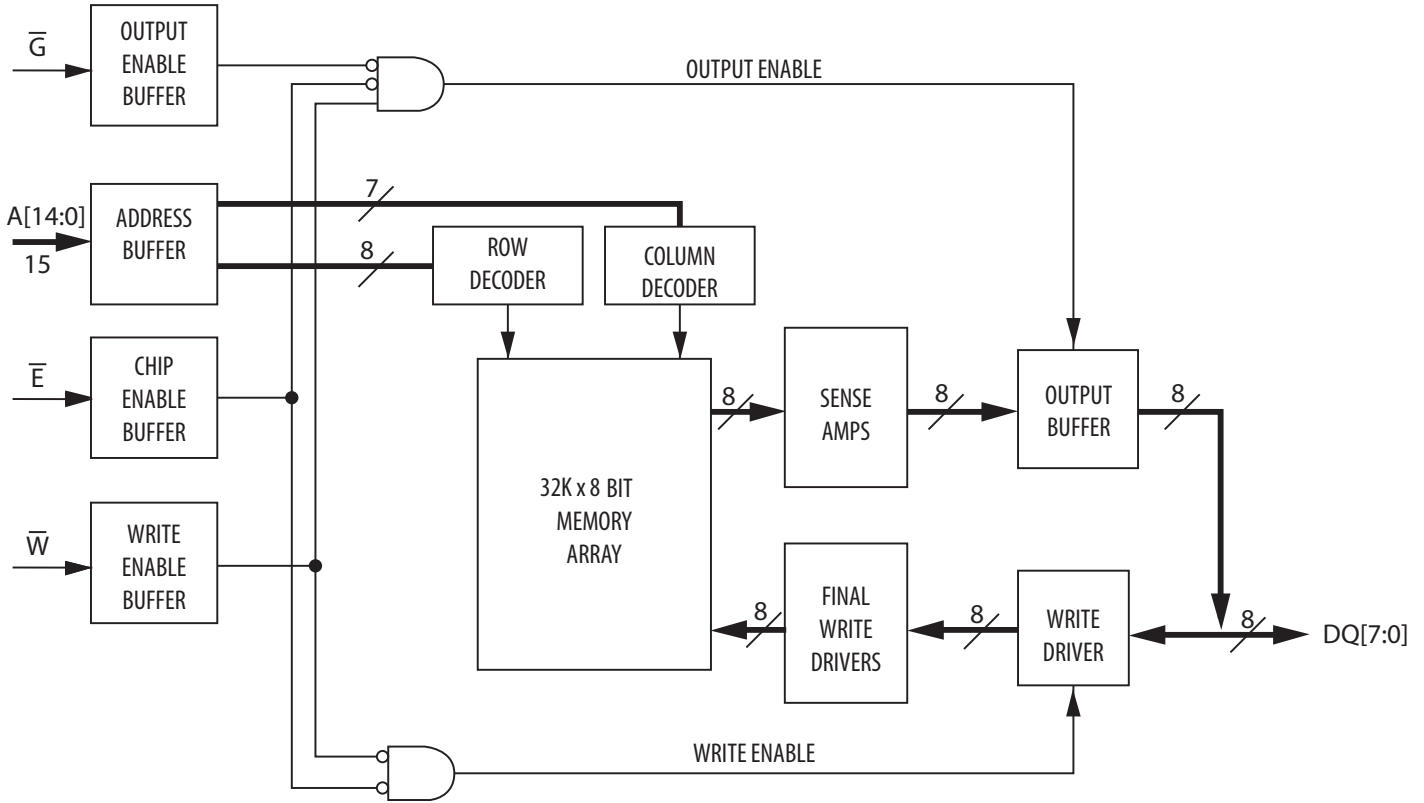
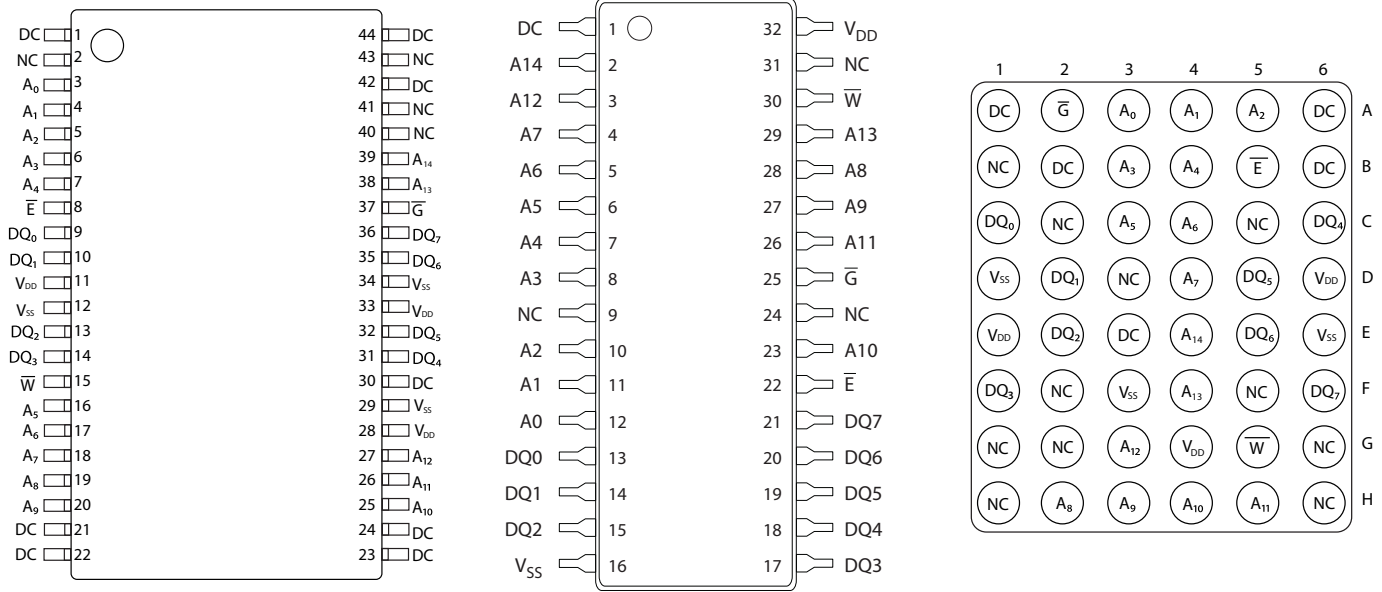


Table 1 – MR256A08B Pin Functions

| Signal Name | Function |
|-------------|--|
| A | Address Input |
| \bar{E} | Chip Enable |
| \bar{W} | Write Enable |
| \bar{G} | Output Enable |
| DQ | Data I/O |
| V_{DD} | Power Supply |
| V_{SS} | Ground |
| DC | Do Not Connect |
| NC | No Connection - Pin 2, 40, 41,43 (TSOP2); Ball C2, C5, D3, F2, F5, G1, G2, G6, H1, H6 (BGA); Pin 9, 24, 31(SOIC) Reserved For Future Expansion |

Figure 2 – Pin Diagrams for Available Packages (Top View) ¹



44 Pin TSOP2

32 Pin SOIC ¹

48 Pin FBGA

Note:

1. The 32-SOIC package is obsolete and shown for legacy reference only. This package option is no longer available for new orders.

Table 2 – Operating Modes

| \bar{E} ¹ | \bar{G} ¹ | \bar{W} ¹ | Mode | V_{DD} Current | DQ[7:0] ² |
|------------------------|------------------------|------------------------|-----------------|--------------------|----------------------|
| H | X | X | Not selected | I_{SB1}, I_{SB2} | Hi-Z |
| L | H | H | Output disabled | I_{DDR} | Hi-Z |
| L | L | H | Byte Read | I_{DDR} | D_{Out} |
| L | X | L | Byte Write | I_{DDW} | D_{in} |

Notes:

1. H = high, L = low, X = don't care
2. Hi-Z = high impedance

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings. ¹

Table 3 – Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|------------------|------------------------|-----------|
| Supply voltage ² | V_{DD} | -0.5 to 4.0 | V |
| Voltage on an pin ² | V_{IN} | -0.5 to $V_{DD} + 0.5$ | V |
| Output current per pin | I_{OUT} | ± 20 | mA |
| Package power dissipation ³ | P_D | 0.600 | W |
| Temperature under bias | T_{BIAS} | MR256A08B (Commercial) | -10 to 85 |
| MR256A08BC (Industrial) | | -45 to 95 | |
| Storage Temperature | T_{stg} | -55 to 150 | °C |
| Lead temperature during solder (3 minute max) | T_{Lead} | 260 | °C |
| Maximum magnetic field during write | H_{max_write} | 2000 | A/m |
| Maximum magnetic field during read or standby | H_{max_read} | 8000 | A/m |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V_{SS} .
3. Power dissipation capability depends on package characteristics and use environment.

OPERATING CONDITIONS

Table 4 – Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Unit |
|-------------------------|----------|-------------------|---------|-----------------------------|------|
| Power supply voltage | V_{DD} | 3.0 ¹ | 3.3 | 3.6 | V |
| Write inhibit voltage | V_{WI} | 2.5 | 2.7 | 3.0 ¹ | V |
| Input high voltage | V_{IH} | 2.2 | - | $V_{DD} + 0.3$ ² | V |
| Input low voltage | V_{IL} | -0.5 ³ | - | 0.8 | V |
| Temperature under bias | | | | | |
| MR256A08B (Commercial) | T_A | 0 | | 70 | °C |
| MR256A08BC (Industrial) | | -40 | | 85 | |

Notes:

1. There is a 2 ms startup time once V_{DD} exceeds $V_{DD}(\min)$. See "Power Up and Power Down Sequencing Timing Diagram".
2. $V_{IH}(\max) = V_{DD} + 0.3 V_{DC}$; $V_{IH}(\max) = V_{DD} + 2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.
3. $V_{IL}(\min) = -0.5 V_{DC}$; $V_{IL}(\min) = -2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.

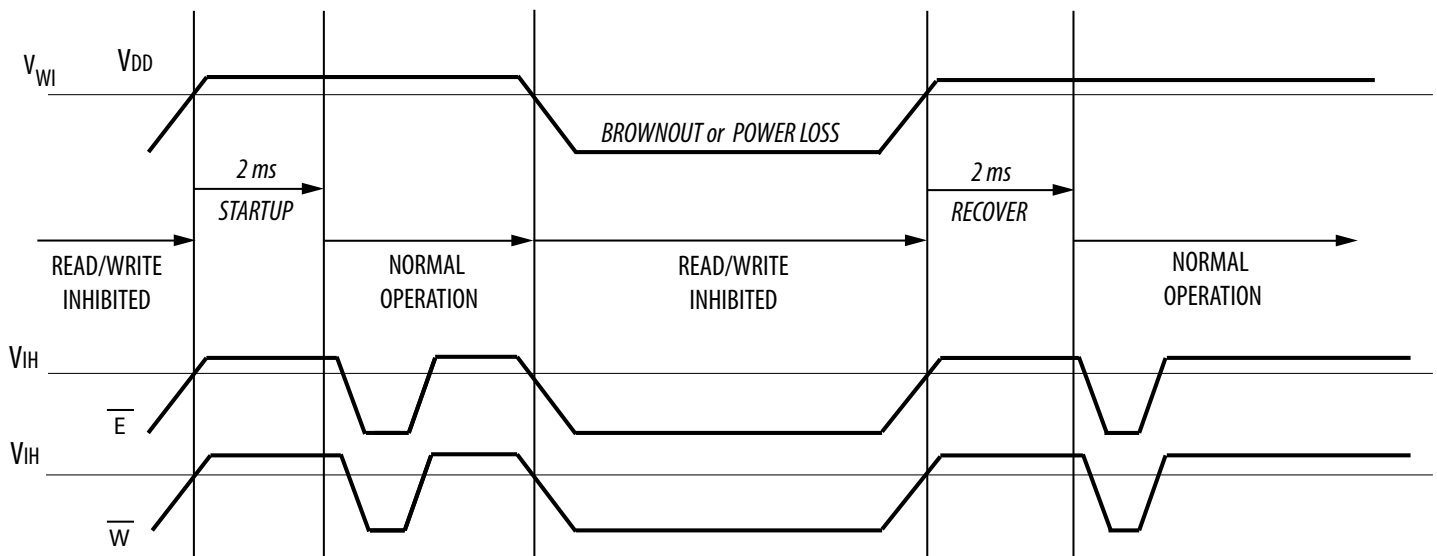
Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI} . As soon as V_{DD} exceeds $V_{DD}(\min)$, there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The \bar{E} and \bar{W} control signals should track V_{DD} on power up to $V_{DD} - 0.2V$ or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives \bar{E} and \bar{W} should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI} , writes are protected and a startup time must be observed when power returns above $V_{DD}(\min)$.

Figure 3 – Power Up and Power Down Sequencing Timing Diagram



DC CHARACTERISTICS

Table 5 – DC Characteristics

| Parameter | Symbol | Min | Typical | Max | Unit |
|--|--------------|-----------------------|---------|-----------------------|---------|
| Input leakage current | $I_{lkg(I)}$ | - | - | ± 1 | μA |
| Output leakage current | $I_{lkg(O)}$ | - | - | ± 1 | μA |
| Output low voltage ($I_{OL} = + 4 \text{ mA}$) ($I_{OL} = + 100 \mu A$) | V_{OL} | - | - | 0.4 $V_{SS} + 0.2$ | V |
| Output high voltage ($I_{OL} = - 4 \text{ mA}$) ($I_{OL} = - 100 \mu A$) | V_{OH} | 2.4 $V_{DD} - 0.2$ | - | - | V |

Table 6 – Power Supply Characteristics

| Parameter | Symbol | Typical | Max | Unit |
|---|-----------|------------------------------|-----|------|
| AC active supply current - read modes ¹ ($I_{OUT} = 0 \text{ mA}, V_{DD} = \text{max}$) | I_{DDR} | 25 | 30 | mA |
| AC active supply current - write modes ¹ ($V_{DD} = \text{max}$) | I_{DDW} | MR256A08B (Commercial) 55 | 65 | mA |
| MR256A08BC (Industrial) | | 55 | 75 | |
| AC standby current ($V_{DD} = \text{max}, \bar{E} = V_{IH}$) <i>no other restrictions on other inputs</i> | I_{SB1} | MR256A08B (Commercial) 6 | 7 | mA |
| MR256A08BC (Industrial) | | 6 | 8 | |
| CMOS standby current ($E \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$) ($V_{DD} = \text{max}, f = 0 \text{ MHz}$) | I_{SB2} | MR256A08B (Commercial) 5 | 6 | mA |
| MR256A08BC (Industrial) | | 5 | 7 | |

Notes:

1. All active current measurements are measured with one address transition per cycle and at minimum cycle time.

TIMING SPECIFICATIONS

Table 7 – Capacitance

| Parameter ¹ | Symbol | Typical | Max | Unit |
|---------------------------|-----------|---------|-----|------|
| Address input capacitance | C_{In} | - | 6 | pF |
| Control input capacitance | C_{In} | - | 6 | pF |
| Input/Output capacitance | $C_{I/O}$ | - | 8 | pF |

Notes:

- $f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25 \text{ }^\circ\text{C}$, periodically sampled rather than 100% tested.

Table 8 – AC Measurement Conditions

| Parameter | Value | Unit |
|---|--------------|------|
| Logic input timing measurement reference level | 1.5 | V |
| Logic output timing measurement reference level | 1.5 | V |
| Logic input pulse levels | 0 or 3.0 | V |
| Input rise/fall time | 2 | ns |
| Output load for low and high impedance parameters | See Figure 4 | |
| Output load for all other timing parameters | See Figure 5 | |

Figure 4 – Output Load Test Low and High

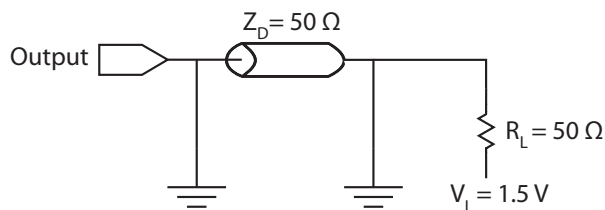
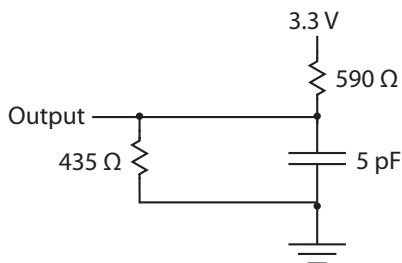


Figure 5 – Output Load Test All Others



Read Mode

Table 9 – Read Cycle Timing

| Parameter ¹ | Symbol | Min | Max | Unit |
|---|------------|-----|-----|------|
| Read cycle time | t_{AVAV} | 35 | - | ns |
| Address access time | t_{AVQV} | - | 35 | ns |
| Enable access time ² | t_{ELQV} | - | 35 | ns |
| Output enable access time | t_{GLQV} | - | 15 | ns |
| Output hold from address change | t_{AXQX} | 3 | - | ns |
| Enable low to output active ³ | t_{ELQX} | 3 | - | ns |
| Output enable low to output active ³ | t_{GLQX} | 0 | - | ns |
| Enable high to output Hi-Z ³ | t_{EHQZ} | 0 | 15 | ns |
| Output enable high to output Hi-Z ³ | t_{GHQZ} | 0 | 10 | ns |

Notes:

- \bar{W} is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
- Addresses valid before or at the same time \bar{E} goes low.
- This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage.

Figure 6 – Read Cycle 1

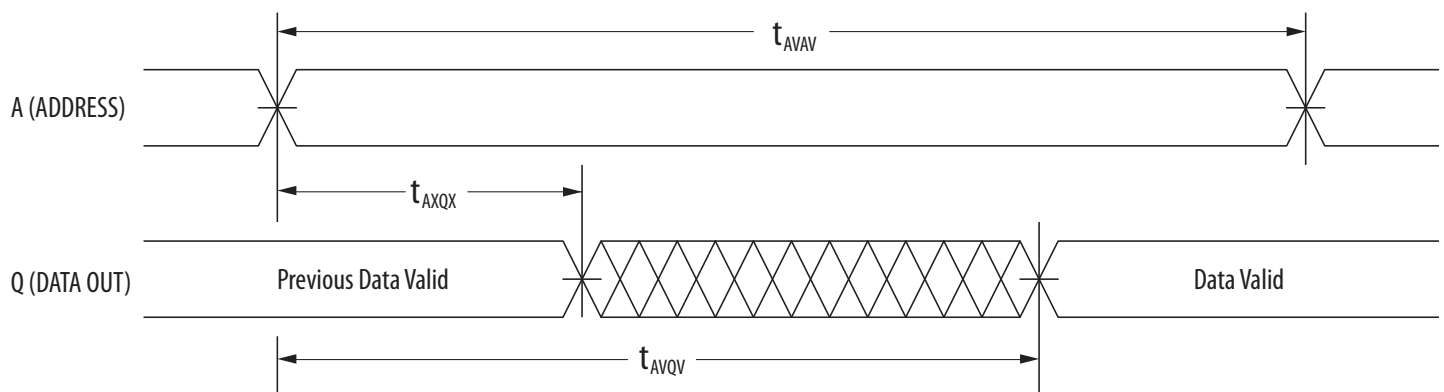
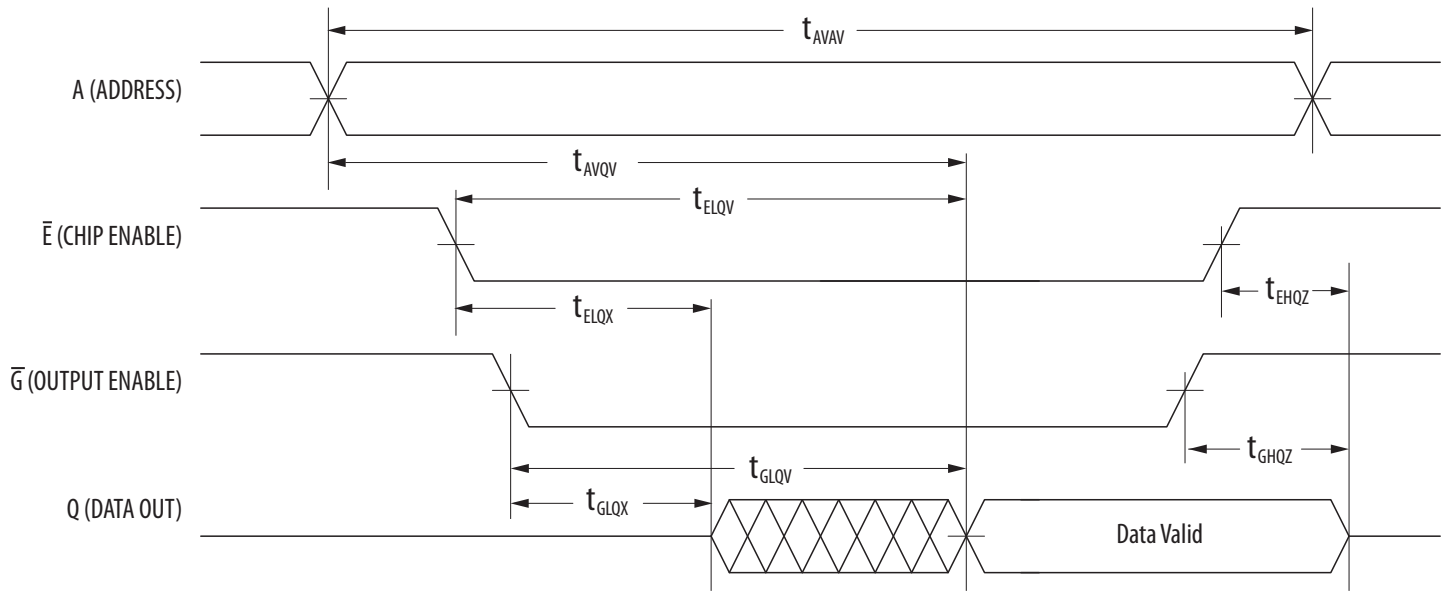


Figure 7 – Read Cycle 2



Write Mode
Table 10 – Write Cycle Timing 1 (\overline{W} Controlled)

| Parameter ¹ | Symbol | Min | Max | Unit |
|--|--------------------------|-----|-----|------|
| Write cycle time ² | t_{AVAV} | 35 | - | ns |
| Address set-up time | t_{AVWL} | 0 | - | ns |
| Address valid to end of write (\overline{G} high) | t_{AVWH} | 18 | - | ns |
| Address valid to end of write (\overline{G} low) | t_{AVWH} | 20 | - | ns |
| Write pulse width (\overline{G} high) | t_{WLWH} t_{WLEH} | 15 | - | ns |
| Write pulse width (\overline{G} low) | t_{WLWH} t_{WLEH} | 15 | - | ns |
| Data valid to end of write | t_{DVWH} | 10 | - | ns |
| Data hold time | t_{WHDX} | 0 | - | ns |
| Write low to data Hi-Z ³ | t_{WLQZ} | 0 | 12 | ns |
| Write high to output active ³ | t_{WHQX} | 3 | - | ns |
| Write recovery time | t_{WHAX} | 12 | - | ns |

Notes:

1. All writes occur during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} or \overline{E} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage. At any given voltage or temperature, $t_{WLQZ}(\text{max}) < t_{WHQX}(\text{min})$

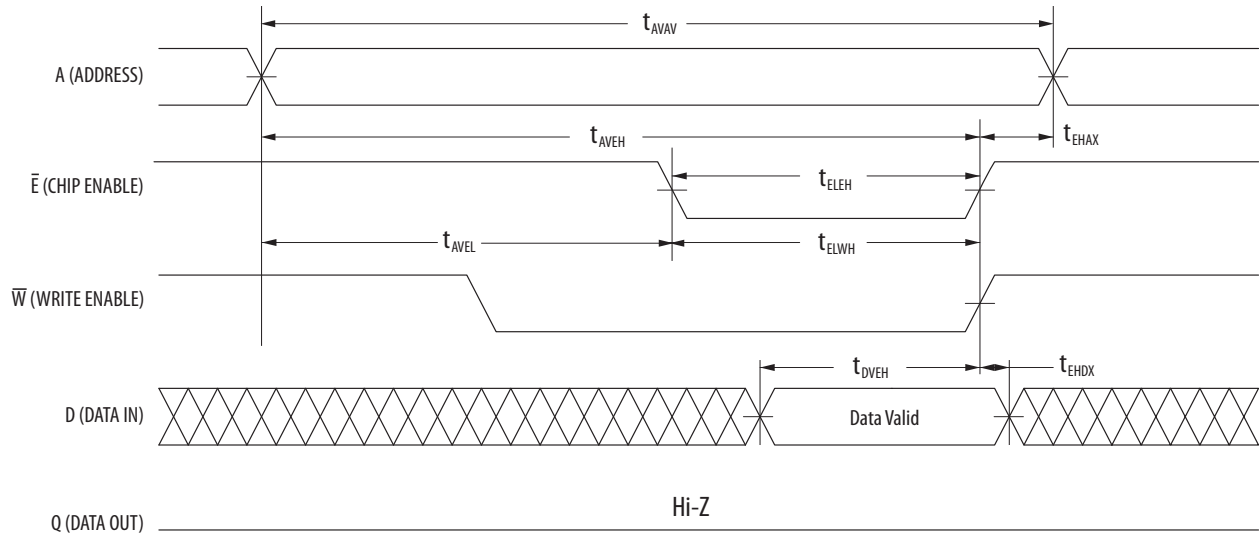
Table 11 – Write Cycle Timing 2 (\bar{E} Controlled)

| Parameter ¹ | Symbol | Min | Max | Unit |
|--|--------------------------|-----|-----|------|
| Write cycle time ² | t_{AVAV} | 35 | - | ns |
| Address set-up time | t_{AVEL} | 0 | - | ns |
| Address valid to end of write (\bar{G} high) | t_{AVEH} | 18 | - | ns |
| Address valid to end of write (\bar{G} low) | t_{AVEH} | 20 | - | ns |
| Enable to end of write (\bar{G} high) | t_{ELEH} t_{ELWH} | 15 | - | ns |
| Enable to end of write (\bar{G} low) ³ | t_{ELEH} t_{ELWH} | 15 | - | ns |
| Data valid to end of write | t_{DVEH} | 10 | - | ns |
| Data hold time | t_{EHDX} | 0 | - | ns |
| Write recovery time | t_{EHAX} | 12 | - | ns |

Notes:

1. All writes occur during the overlap of \bar{E} low and \bar{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \bar{G} goes low at the same time or after \bar{W} goes low, the output will remain in a high impedance state. After \bar{W} or \bar{E} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \bar{E} being asserted low in one cycle to \bar{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If \bar{E} goes low at the same time or after \bar{W} goes low, the output will remain in a high-impedance state. If \bar{E} goes high at the same time or before \bar{W} goes high, the output will remain in a high-impedance state.

Figure 9 – Write Cycle Timing 2 (\bar{E} Controlled)



ORDERING INFORMATION

Table 12 – Ordering Part Number System for Parallel I/O MRAM

| | Memory | Density | Type | I/O Width | Rev. | Temp | Package | Speed | Packing | Grade |
|---|--------------|---------|------|-----------|------|------|---------|-------|---------|-------|
| Example Ordering Part Number | MR | 256 | A | 08 | B | C | MA | 35 | R | |
| MRAM | MR | | | | | | | | | |
| 256 Kb | 256 | | | | | | | | | |
| 1 Mb | 0 | | | | | | | | | |
| 4 Mb | 2 | | | | | | | | | |
| 16 Mb | 4 | | | | | | | | | |
| Async 3.3v | A | | | | | | | | | |
| Async 3.3v Vdd and 1.8v Vddq | D | | | | | | | | | |
| Async 3.3v Vdd and 1.8v Vddq with 2.7v min. Vdd | DL | | | | | | | | | |
| 8-bit | 08 | | | | | | | | | |
| 16-bit | 16 | | | | | | | | | |
| Rev A | A | | | | | | | | | |
| Rev B | B | | | | | | | | | |
| Commercial | 0 to 70°C | Blank | | | | | | | | |
| Industrial | -40 to 85°C | C | | | | | | | | |
| Extended | -40 to 105°C | V | | | | | | | | |
| AEC Q-100 Grade 1 | -40 to 125°C | M | | | | | | | | |
| 44-TSOP-2 | YS | | | | | | | | | |
| 48-FBGA | MA | | | | | | | | | |
| 16-SOIC | SC | | | | | | | | | |
| 32-SOIC | SO | | | | | | | | | |
| 35 ns | 35 | | | | | | | | | |
| 45 ns | 45 | | | | | | | | | |
| Tray | Blank | | | | | | | | | |
| Tape and Reel | R | | | | | | | | | |
| Engineering Samples | ES | | | | | | | | | |
| Customer Samples | Blank | | | | | | | | | |
| Mass Production | Blank | | | | | | | | | |

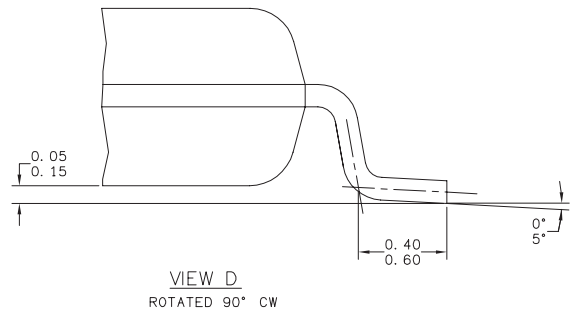
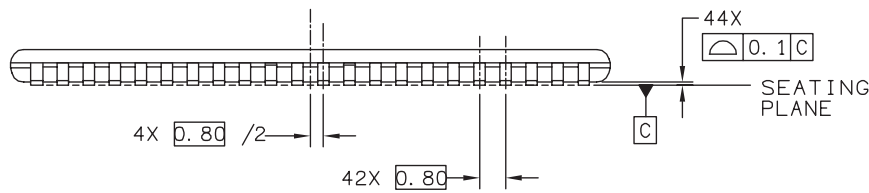
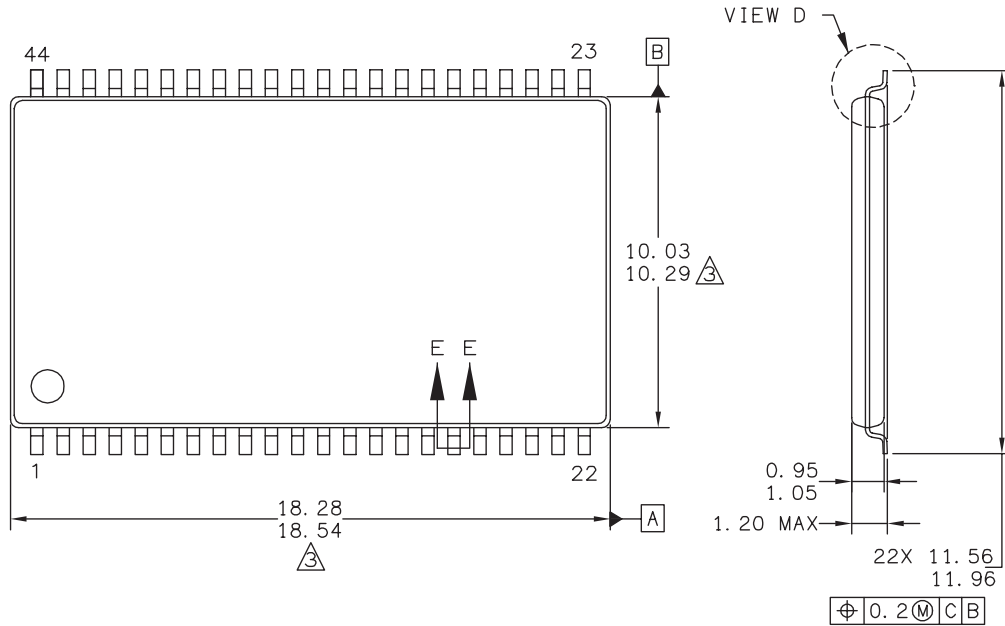
Table 13 – MR256A08B Ordering Part Numbers ¹

| Temp Grade | Temp | Package | Shipping | Ordering Part Number |
|------------|---------------|----------------------|---------------|--------------------------|
| Commercial | 0 to +70 °C | 44-TSOP2 | Tray | MR256A08BYS35 |
| | | | Tape and Reel | MR256A08BYS35R |
| | | 48-BGA | Tray | MR256A08BMA35 |
| | | | Tape and Reel | MR256A08BMA35R |
| | | 32-SOIC ¹ | Tray | MR256A08BSO35 Obsolete |
| | | | Tape and Reel | MR256A08BSO35R Obsolete |
| Industrial | -40 to +85 °C | 44-TSOP2 | Tray | MR256A08BCYS35 |
| | | | Tape and Reel | MR256A08BCYS35R |
| | | 48-BGA | Tray | MR256A08BCMA35 |
| | | | Tape and Reel | MR256A08BCMA35R |
| | | 32-SOIC ¹ | Tray | MR256A08BCSO35 Obsolete |
| | | | Tape and Reel | MR256A08BCSO35R Obsolete |

¹ The 32-SOIC package option is obsolete and no longer available. See PCN02895 here.

PACKAGE OUTLINE DRAWINGS

Figure 10 – 44-TSOP2 Package Outline



Not To Scale

1. Dimensions and tolerances per ASME Y14.5M - 1994.
2. Dimensions in Millimeters.
3. Dimensions do not include mold protrusion.
4. Dimension does not include DAM bar protrusions.
5. DAM Bar protrusion shall not cause the lead width to exceed 0.58.

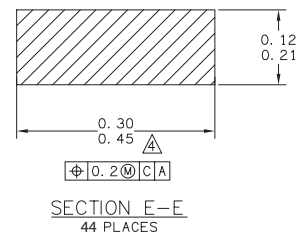
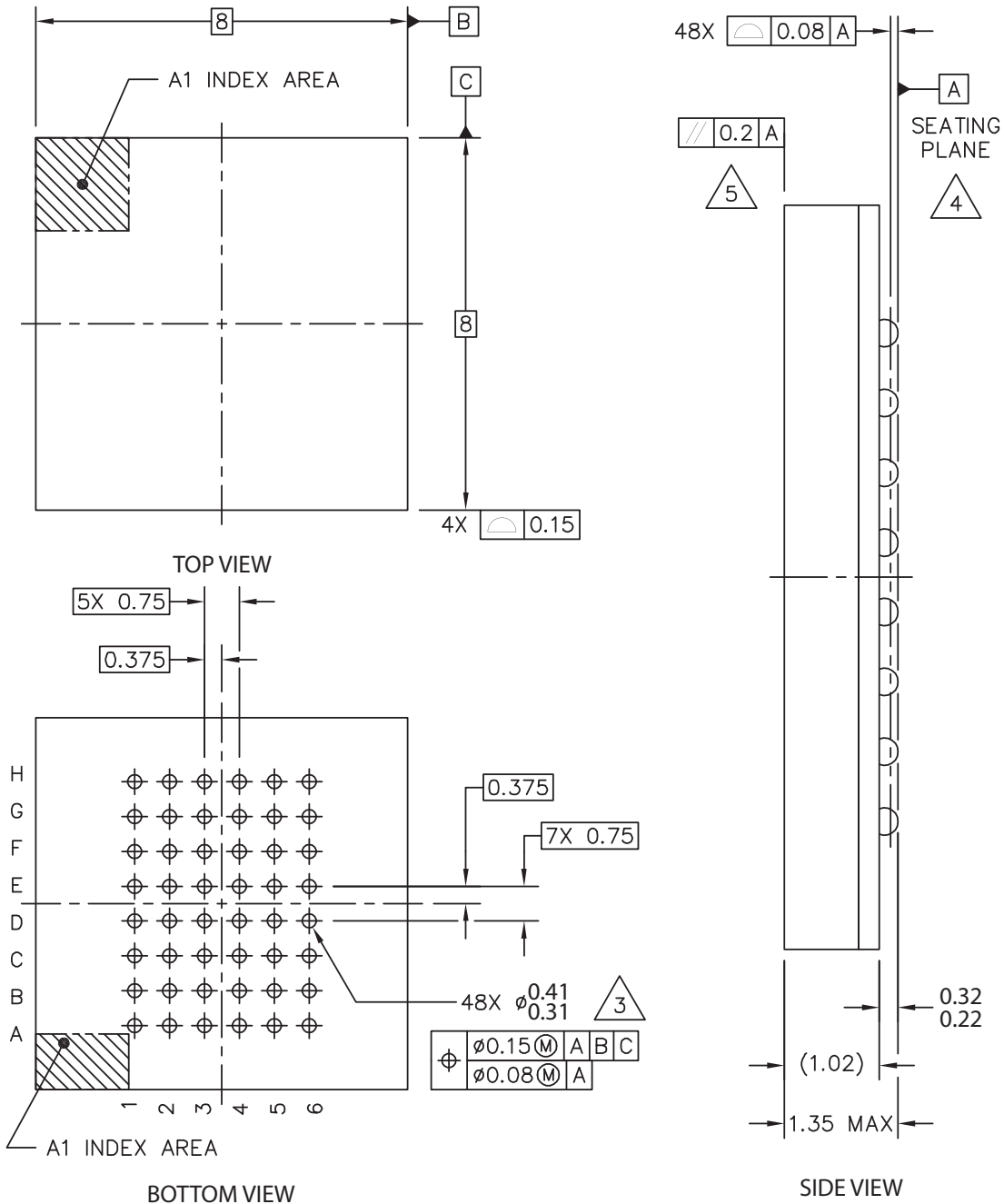


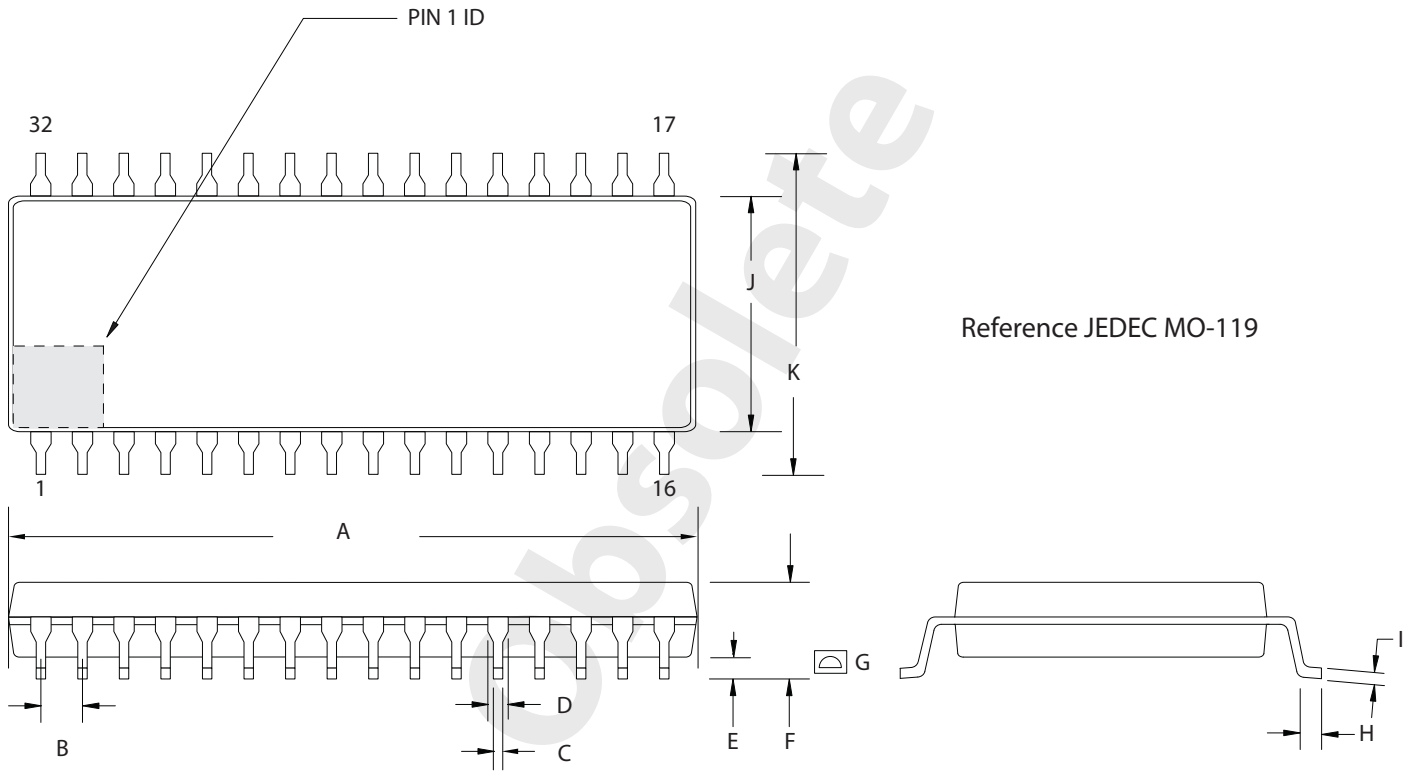
Figure 11 – 48-BGA Package Outline



Not To Scale

1. Dimensions in Millimeters.
2. Dimensions and tolerances per ASME Y14.5M - 1994.
3. Maximum solder ball diameter measured parallel to DATUM A
4. DATUM A, the seating plane is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

Figure 12 – 32-SOIC Package Outline ¹



| Unit | A | B | C | D | E | F | G | H | I | J | K |
|------------|--------|------|-------|-------|-------|-------|--------|-------|-------|-------|--------|
| mm - Min | 20.574 | 1.00 | 0.355 | 0.66 | 0.101 | 2.286 | Radius | 0.533 | 0.152 | 7.416 | 10.287 |
| - Max | 20.878 | 1.50 | 0.508 | 0.81 | 0.254 | 2.540 | 0.101 | 1.041 | 0.304 | 7.594 | 10.642 |
| inch - Min | 0.810 | 0.04 | 0.14 | 0.026 | 0.004 | 0.09 | Radius | 0.021 | 0.006 | 0.292 | 0.405 |
| - Max | 0.822 | 0.06 | 0.02 | 0.032 | 0.010 | 0.10 | 0.0040 | 0.041 | 0.012 | 0.299 | 0.419 |

Note:

1. The 32-SOIC package is obsolete and shown for legacy reference only. This package option is no longer available for new orders.

REVISION HISTORY

| Revision | Date | Description of Change |
|----------|------------------|---|
| 0 | Sept 12, 2008 | Initial Advance Information Release |
| 1 | Mar 25, 2009 | Add Industrial and Automotive Temperature Options |
| 2 | August 16, 2011 | Removed Automotive temperature options. Included SOIC package. Revised formatting |
| 3 | October 28, 2011 | Changed TSOP-II to TSOP2. Changed logo to new EST Logo. Revisions to Available Parts, Table 4.1: Added Industrial Temp Grade option in SOIC package. Deleted Tape & Reel pack option for all SOIC packaged parts. |
| 4 | Dec 9, 2011 | Figure 2.1 cosmetic update. Figure 5.2 BGA package outline drawing revised for package ball size. Revisions to ISB1, ISB2 and IDDW for Industrial Grade options in Table 2.4. |
| 5 | July 9, 2013 | MR256A08BCSO35 removed Preliminary status. Now MP. |
| 6 | October 11, 2013 | Added Tape and Reel shipping option for SOIC packaged products. Reformatted to current standards. |
| 6.1 | May 19, 2015 | Revised Everspin contact information. |
| 6.2 | June 11, 2015 | Corrected Japan Sales Office telephone number. |
| 6.3 | July 20, 2015 | 32-SOIC package options Not Recommended for New Designs. |
| 6.4 | October 17, 2015 | 32-SOIC package options are obsolete and no longer available. |
| 6.5 | March 23, 2018 | Updated the Contact Us table |

HOW TO CONTACT US

How to Reach Us:

Home Page:

www.everspin.com

World Wide Information Request

WW Headquarters - Chandler, AZ

5670 W. Chandler Blvd., Suite 100

Chandler, Arizona 85226

Tel: +1-877-480-MRAM (6726)

Local Tel: +1-480-347-1111

Fax: +1-480-347-1175

support@everspin.com

orders@everspin.com

sales@everspin.com

Europe, Middle East and Africa

Everspin Europe Support

support.europe@everspin.com

Japan

Everspin Japan Support

support.japan@everspin.com

Asia Pacific

Everspin Asia Support

support.asia@everspin.com

Everspin Technologies, Inc.

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