THE DATASHEET OF

DP83TC812SRHARQ1

www.win-source.net 0086-755-83957316

DP83TC812x-Q1 TC-10 Compliant 100BASE-T1 Automotive Ethernet PHY

1 Features

- Open Alliance and IEEE 802.3bw 100BASE-T1 compliant
  - Passes Level IV emissions with Integrated LPF
  - TC-10 compliant with < 20µA sleep current
- SAE J2962-3 EMC compliant
- Configurable I/O voltages: 3.3 V, 2.5 V, and 1.8 V
- MAC interfaces: MII, RMII, RGMII and SGMII
- Optional separate voltage rail for MAC interface pins (3.3 V, 2.5 V, 1.8 V)
- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125 °C ambient operating temperature
  - ±8-kV HBM ESD for pins 12 and 13
  - IEC61000-4-2 ESD classification level 4 for pins 12 and 13: ±8-kV contact discharge
- IEEE 1588 SFD support
- TSN compliant with 802.3br frame pre-emption support
- Low active power operation: < 230 mW
- Diagnostic tool kit
  - Signal quality indication (SQI)
  - Time domain reflectometry (TDR)
  - Electrostatic discharge sensor
  - Voltage sensor
  - PRBS Built-in Self-Test
  - Loopbacks
- VQFN, wettable flank packaging
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design

2 Applications

- ADAS
- Gateway and Body Control
- Telematics

3 Description

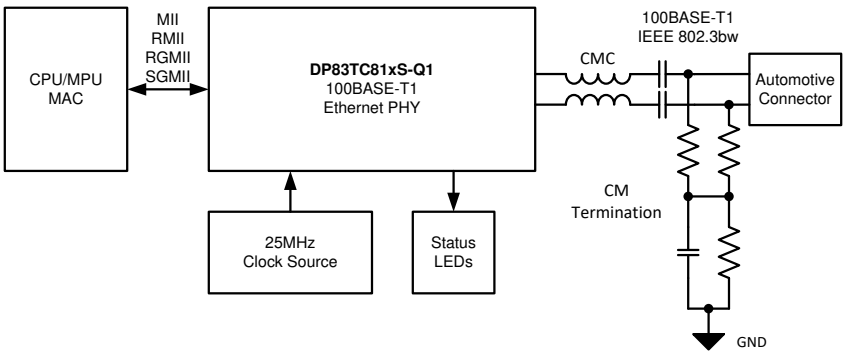
The DP83TC812-Q1 device is an IEEE 802.3bw-compliant automotive PHYTER™ Ethernet physical layer transceiver which can work with Unshielded Twisted Pair cable. The PHY supports TC10 sleep and wake features. It provides all physical layer functions needed to transmit and receive data over unshielded single twisted-pair cables. The device provides xMII flexibility with support for standard MII, RMII, RGMII, and SGMII MAC interfaces.The PHY also integrates a low pass filter on the MDI side to reduce emissions.

This device includes the Diagnostic Tool Kit, providing an extensive list of real-time monitoring tools, debug tools and test modes. Within the tool kit is the first integrated electrostatic discharge (ESD) monitoring tool. It is capable of counting ESD events on MDI as well as providing real-time monitoring through the use of a programmable interrupt. Additionally, the DP83TC812-Q1 includes a pseudo random binary sequence (PRBS) frame generation tool, which is fully compatible with internal loopbacks, to transmit and receive data without the use of a MAC. The device is housed in a 6.00-mm × 6.00-mm, 36-pin VQFN wettable flank package. This device is pin-2-pin compatible with DP83TG720 (1000BASE-T1). It is also form factor compatible with DP83TC811. This would allow for a single PCB layout to be used for DP83TC811, DP83TC812, DP83TC814, and DP83TG720.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
DP83TC812S-Q1	VQFN (36)	6.00 mm × 6.00 mm
DP83TC812R-Q1	VQFN (36)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Device Comparison Table....3
6 Pin Configuration and Functions....4
7 Specifications....16
7.1 Absolute Maximum Ratings....16
7.2 ESD Ratings....16
7.3 Recommended Operating Conditions....16
7.4 Thermal Information....17
7.5 Electrical Characteristics....17
7.6 Timing Requirements....22
7.7 Timing Diagrams....25
7.8 Typical Characteristics....31
8 Detailed Description....33
8.1 Overview....33
8.2 Functional Block Diagram....34
8.3 Feature Description....35
8.4 Device Functional Modes....44
8.5 Programming....58
8.6 Register Maps....62
9 Application and Implementation....175
9.1 Application Information Disclaimer....175
9.2 Application Information....175
9.3 Typical Applications....175
10 Power Supply Recommendations....182
11 Layout....184
11.1 Layout Guidelines....184
11.2 Layout Example....186
12 Device and Documentation Support....187
12.1 Receiving Notification of Documentation Updates....187
12.2 Support Resources....187
12.3 Community Resources....187
12.4 Trademarks....187
12.5 Electrostatic Discharge Caution....187
12.6 Glossary....187
13 Mechanical, Packaging, and Orderable Information....187

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2021) to Revision B (January 2023)	Page
• Added 'Functional Safety-Capable' to Feature List	1
• Table 6-1 Pin Functions: Changed TX_CLK description to include (50 ohm Driver) for MII transmit clock	4
• Table 6-4 Pin States -TC10 SLEEP: Changed the PULL TYPE of Pin 16 CLKOUT from PD->none	4
• Added line to CLKOUT/GPIO2's description about which registers to program to disable switching	4
• Added line to INT pin description. Reg 12-13 is recommended to be read only when INT_N is LOW	4
• MDC clock rate changed from 25MHz->20MHz in Serial Management Interface Section of Pin Function Table	4
• Updated Iozh to clarify mapping of Rx_Ctrl and Rx_ER pins	17
• Removed Supply ramp delay offset: For all supplies	22
• Power-Up Timing figure corrected	25
• PHY Operation State Diagram figure updated	44
• Added Auto-clear note to register 0x18B[6]	45
• Added XI clock PPM Table	50
• Added Auto-clear note to register 0x18B[6]	58
• Register 0x63E, clarified Bit Description	62
• Register 0x63D, clarified Bit Description	62
• Register 0x63C, clarified Bit Description	62
• Register 0x63B, clarified Bit Description	62
• Register 0x63A, clarified Bit Description	62
• Register 0x639, clarified Bit Description	62
• Register 0x451, clarified Bit Descriptions	62
• Register 0x18B has been added	62
• Register 0x12, Bit 15 has been removed	62

Changes from Revision * (April 2021) to Revision A (December 2021)	Page
• Advance Information to Production Data Release	1

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5 Device Comparison Table

PART NUMBER	SGMII SUPPORT	OPERATING TEMPERATURE
DP83TC812R-Q1	No	–40°C to 125°C
DP83TC812S-Q1	Yes	–40°C to 125°C

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6 Pin Configuration and Functions

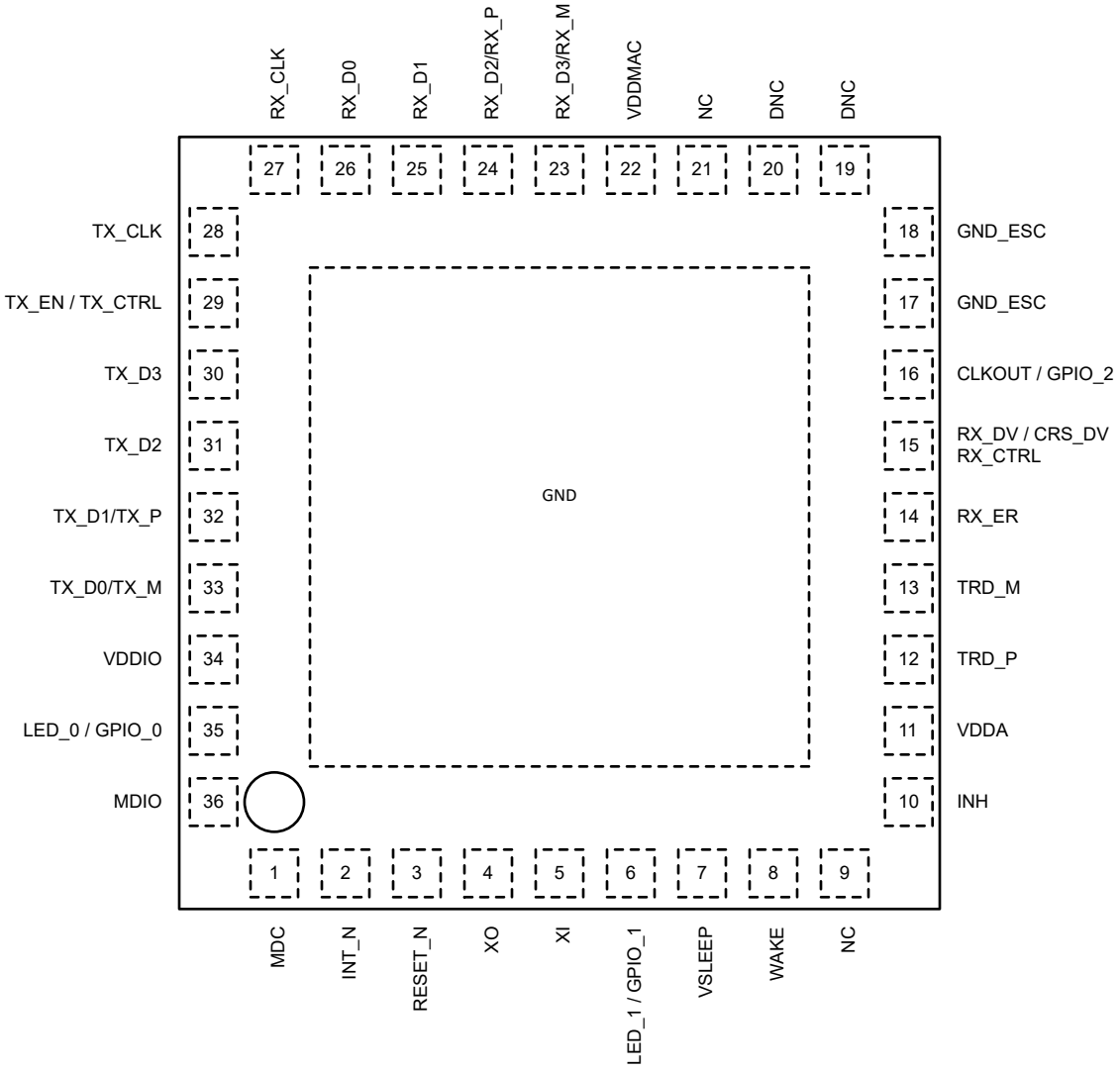

Figure 6-1. DP83TC812S-Q1 RHA Package
36-Pin VQFN
Top View

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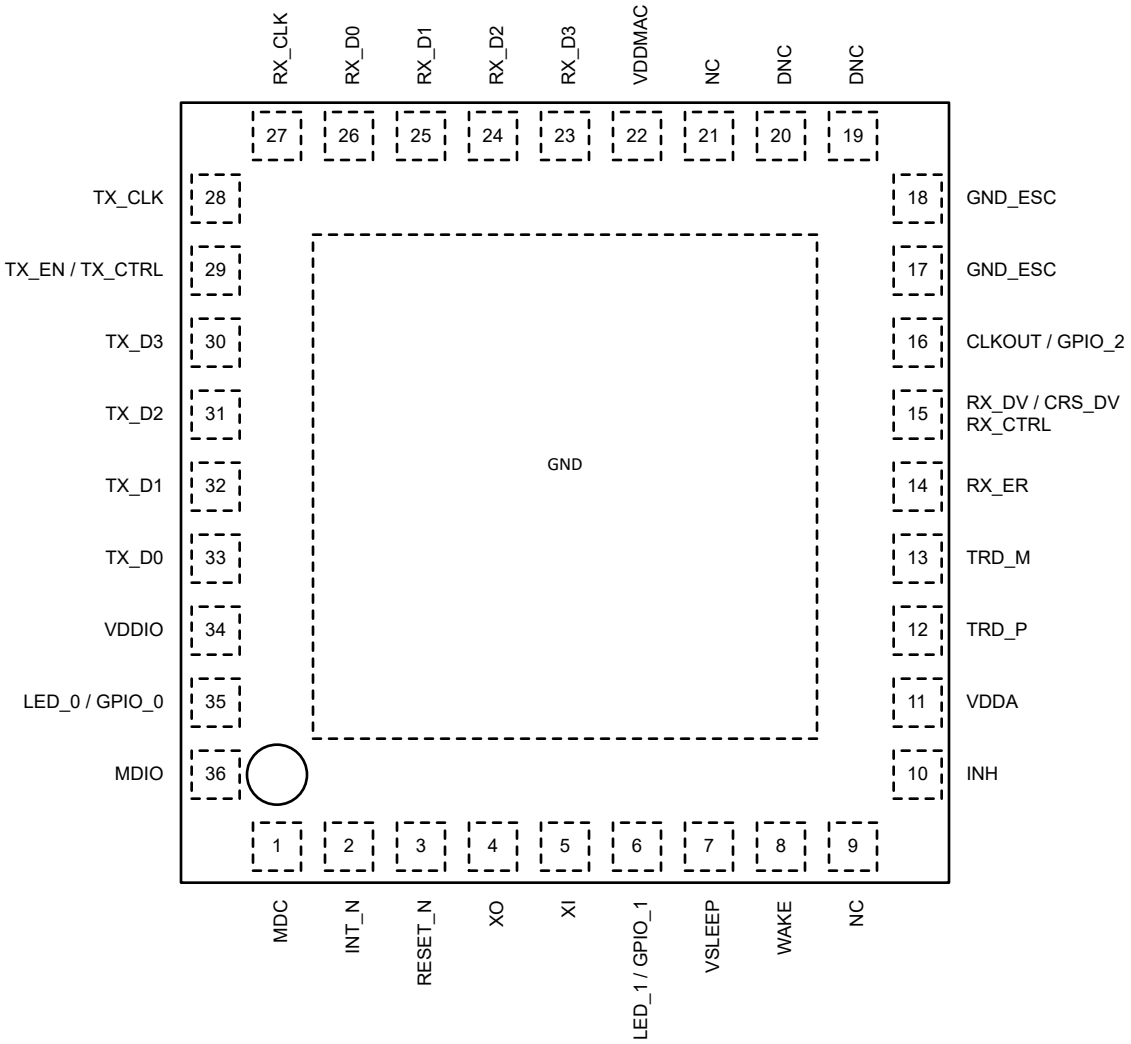

Figure 6-2. DP83TC812R-Q1 RHA Package
36-Pin VQFN
Top View

Table 6-1. Pin Functions

PIN		STATE[1]	DESCRIPTION
NAME[2]	NO.		
MAC INTERFACE			
RX_D3 RX_M	23	S, PD, O	**Receive Data:** Symbols received on the cable are decoded and transmitted out of these pins synchronous to the rising edge of RX_CLK. They contain valid data when RX_DV is asserted. A data nibble, RX_D[3:0], is transmitted in MII and RGMII modes. 2 bits; RX_D[1:0], are transmitted in RMII mode. RX_D[3:2] are not used when in RMII mode. If the PHY is bootstrapped to RMII Master mode, a 50-MHz clock reference is automatically outputted on RX_D3. This clock must be fed to the MAC. **RX_M / RX_P:** Differential SGMII Data Output. These pins transmit data from the PHY to the MAC.
RX_D2 RX_P	24		
RX_D1	25		
RX_D0	26		
RX_CLK	27	PD, O	**Receive Clock:** In MII and RGMII modes, the receive clock provides a 25-MHz reference clock. **Unused in RMII and SGMII modes**
RX_ER	14	S, PD, O	**Receive Error:** In MII and RMII modes, this pin indicates a receive error symbol has been detected within a received packet. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. This pin is not required to be used by the MAC in MII or RMII because the PHY will automatically corrupt data on a receive error. **Unused in RGMII and SGMII modes**
RX_DV CRS_DV RX_CTRL	15	S, PD, O	**Receive Data Valid:** This pin indicates when valid data is presented on RX_D[3:0] for MII mode. **Carrier Sense Data Valid:** This pin combines carrier sense and data valid into an asynchronous signal. When CRS_DV is asserted, data is presented on RX_D[1:0] in RMII mode. **RGMII Receive Control:** Receive control combines receive data valid indication and receive error indication into a single signal. RX_DV is presented on the rising edge of RX_CLK and RX_ER is presented on the falling edge of RX_CLK. **Unused in SGMII mode**
TX_CLK	28	PD, I, O	**Transmit Clock:** In MII mode, the transmit clock is a 25-MHz output (50 ohm Driver) and has constant phase referenced to the reference clock. In RGMII mode, this clock is sourced from the MAC layer to the PHY. A 25-MHz clock must be provided (not required to have constant phase to the reference clock unless synchronous RGMII is enabled) **Unused in RMII and SGMII modes**
TX_EN TX_CTRL	29	PD, I	**Transmit Enable:** In MII mode, transmit enable is presented prior to the rising edge of the transmit clock. TX_EN indicates the presence of valid data inputs on TX_D[3:0]. In RMII mode, transmit enable is presented prior to the rising edge of the reference clock. TX_EN indicates the presence of valid data inputs on TX_D[1:0]. **RGMII Transmit Control:** Transmit control combines transmit enable and transmit error indication into a single signal. TX_EN is presented prior to the rising edge of TX_CLK; TX_ER is presented prior to the falling edge of TX_CLK. **Unused in SGMII mode**
TX_D3	30	PD, I	**Transmit Data:** In MII and RGMII modes, the transmit data nibble, TX_D[3:0], is received from the MAC prior to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] is received from the MAC prior to the rising edge of the reference clock. TX_D[3:2] are not used in RMII mode. **TX_M / TX_P:** Differential SGMII Data Input. These pins receive data that is transmitted from the MAC to the PHY.
TX_D2	31		
TX_D1 TX_P	32		
TX_D0 TX_M	33		
SERIAL MANAGEMENT INTERFACE			
MDC	1	I	**Management Data Clock:** Synchronous clock to the MDIO serial management input and output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 20 MHz. There is no minimum clock rate.
MDIO	36	OD, IO	**Management Data Input/Output:** Bidirectional management data signal that may be sourced by the management station or the PHY. This pin requires a pullup resistor. In systems with multiple PHYs using same MDIO-MDC bus, a single pull-up resistor must be used on MDIO line. Recommended to use a resistor between 2.2 kΩ and 9 kΩ.

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Table 6-1. Pin Functions (continued)

PIN		STATE[1]	DESCRIPTION
NAME[2]	NO.		
CONTROL INTERFACE			
$\overline{\text{INT}}$	2	PU, OD, IO	**Interrupt:** Active-LOW output, which will be asserted LOW when an interrupt condition occurs. This pin has a weak internal pullup. Register access is necessary to enable various interrupt triggers. Once an interrupt event flag is set, register access is required to clear the interrupt event. This pin can be configured as an Active-HIGH output using register *0x0011*. Interrupt status from Reg 12-13 is recommended to be read only when INT_N is LOW. This pin can also operate as Power-Down control where asserting this pin low would put the PHY in power down mode and asserting high would put the PHY in normal mode. This feature can also be enabled via register *0x0011*.
$\overline{\text{RESET}}$	3	PU, I	**Reset:** Active-LOW input, which initializes or reinitializes the PHY. Asserting this pin LOW for at least 1 µs will force a reset process to occur. All internal registers will reinitialize to their default states as specified for each bit in the Register Maps section. All bootstrap pins are resampled upon deassertion of reset.
WAKE	8	PD, I/O	**WAKE:** Input/Outputpin which is Active-HIGH input by default. As input this pin wakes the PHY from TC-10 SLEEP. Asserting this pin HIGH at power-up will bring the PHY out of SLEEP. External 10kΩ pull down resistor can be used when implementing TC-10 circuit to prevent accidental wake-up. This pin can be directly tied to VSLEEP or it can be pulled to VSLEEP via a resistor to wake the device. This pin also supports wake forwarding feature where a WAKE pulse will be generated by the PHY which can be used for waking up other PHYs on the same system.
INH	10	O, OD	**INH:** Active-HIGH output. This pin will be Hi-Z when the PHY is in TC-10 SLEEP. This pin is HIGH for all other PHY states. External pull down resistor in th range of 2kΩ - 10kΩ must be used when implementing TC-10 circuit. If multiple devices are sharing INH pin, then a single pull down resistor must be used.
CLOCK INTERFACE			
XI	5	I	**Reference Clock Input (RMII):** Reference clock 50-MHz CMOS-level oscillator in RMII Slave mode. Reference clock 25-MHz crystal or oscillator in RMII Master mode. **Reference Clock Input (Other MAC Interfaces):** Reference clock 25-MHz crystal or oscillator input. The device supports either an external crystal resonator connected across pins XI and XO, or an external CMOS-level oscillator connected to pin XI only and XO left floating. This pin can also accept clock input from other devices like Ethernet MAC or another Ethernet PHY in daisy-chain operations.
XO	4	O	**Reference Clock Output:** XO pin is used for crystal only. This pin must be left floating when a CMOS-level oscillator is connected to XI.
LED/GPIO INTERFACE			
LED_0 / GPIO_0	35	S, PD, IO	**LED_0:** Link Status LED. This pin can also be used as LED or clock output via Register selection.
LED_1 / GPIO_1	6	S, PD, IO	**LED_1:** Link Status and BLINK for TX/RX Activity. This pin can also be used as LED or clock output via Strap/ Register selection.
CLKOUT / GPIO_2	16	IO	**Clock Output:** 25-MHz reference clock. This pin can also be used as LED or GPIO via Strap/Register selection. Program register<0x045F>=0x000F and register<0x0453>=0x0003 to disable switching on clkout pin
MEDIUM DEPENDENT INTERFACE			
TRD_M	13	IO	**Differential Transmit and Receive:** Bidirectional differential signaling configured for 100BASE-T1 operation, IEEE 802.3bw compliant.
TRD_P	12		
GROUND ESCAPE			
GND_ESC	17		**Ground Escape:** Optional ground escape pins. These pins can be connected to ground to optimize PCB layout. These pins are not substitute for power ground connection to DAP. DAP must always be connected to power ground. This pin can be left unconnected if not used.
GND_ESC	18		**Ground Escape:** Optional ground escape pins. These pins can be connected to ground to optimize PCB layout. These pins are not substitute for power ground connection to DAP. DAP must always be connected to power ground. This pin can be left unconnected if not used.

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Table 6-1. Pin Functions (continued)

PIN		STATE[1]	DESCRIPTION
NAME[2]	NO.		
POWER CONNECTIONS			
VDDA	11	SUPPLY	**Core Supply:** 3.3 V Recommend using 0.47-µF and 0.01-µF ceramic decoupling capacitors; optional ferrite bead can be used.
VDDIO	34	SUPPLY	**IO Supply:** 1.8 V, 2.5 V, or 3.3 V Recommend using ferrite bead, 0.47-µF and 0.01-µF ceramic decoupling capacitors.
VDDMAC	22	SUPPLY	**Optional MAC Interface Supply:** 1.8 V, 2.5 V, or 3.3 V Optional separate supply for MAC interface pins. This pin supplies power to the MAC interface pins and can be kept at a different voltage level as compared to other IO pins. Recommend using 0.47-µF, and 0.01-µF ceramic decoupling capacitors and ferrite bead. When separate VDDMAC is not required in the system then it must be connected to VDDIO. When connecting to VDDIO, 0.47-µF on the VDDIO can be removed. 0.47-µF must still be connected close to VDDMAC. In this case, one common ferrite bead can be used between VDDIO and VDDMAC.
VSLEEP	7	SUPPLY	**VSLEEP Supply:** 3.3 V Recommend using 0.1-µF ceramic decoupling capacitors.
GROUND	DAP	GROUND	**Ground:** This must always be connected to power ground.
DO NOT CONNECT			
DNC	19		**DNC:** Do not connect (leave floating)
DNC	20		**DNC:** Do not connect (leave floating)
NO CONNECT			
NC	9		**NC:** No connection. Can be left floating. Connecting to any signal will have no effect on PHY performance.
NC	21		**NC:** No connection. Can be left floating. Connecting to any signal will have no effect on PHY performance.

1. Pin Type:
   I = Input
   O = Output
   IO = Input/Output
   OD = Open Drain
   PD = Internal pulldown
   PU = Internal pullup
   S = Bootstrap configuration pin (all configuration pins have weak internal pullups or pulldowns)
2. When pins are unused, follow the recommended connection requirements provided in the table above. If pins do not have required termination, they may be left floating.

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Table 6-2. Pin Domain

PIN NO	PIN NAME	VOLTAGE DOMAIN
1	MDC	VDDIO
2	INT_N	VDDIO
3	RESET_N	VDDIO
4	XO	VDDIO
5	XI	VDDIO
6	LED_1/GPIO_1	VDDIO
8	WAKE	VSLEEP
10	INH	VSLEEP
12	TRD_P	VDDA
13	TRD_M	VDDA
14	RX_ER	VDDMAC
15	RX_DV/CRS_DV/RX_CTRL	VDDMAC
16	CLKOUT/GPIO_2	VDDMAC
23	RX_D3/RX_M	VDDMAC
24	RX_D2/RX_P	VDDMAC
25	RX_D1	VDDMAC
26	RX_D0	VDDMAC
27	RX_CLK	VDDMAC
28	TX_CLK	VDDMAC
29	TX_EN/TX_CTRL	VDDMAC
30	TX_D3	VDDMAC
31	TX_D2	VDDMAC
32	TX_D1/TX_P	VDDMAC
33	TX_D0/TX_M	VDDMAC
35	LED_0/GPIO_0	VDDIO
36	MDIO	VDDIO

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Table 6-3. Pin States - POWER-UP / RESET

PIN NO	PIN NAME	POWER-UP / RESET		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none
2	$\overline{\text{INT}}$	I	PU	9
3	$\overline{\text{RESET}}$	I	PU	9
4	XO	O	none	none
5	XI	I	none	none
6	LED_1	I	PD	9
7	VSLEEP	SUPPLY	none	none
8	WAKE	I/O	PD	455
9	NC	FLOAT	none	none
10	INH	OD, O	none	none
11	VDDA	SUPPLY	none	none
12	TRD_P	IO	none	none
13	TRD_M	IO	none	none
14	RX_ER	I	PD	6
15	RX_DV	I	PD	6
16	CLKOUT	O	none	none
17	GND_ESC	FLOAT	none	none
18	GND_ESC	I	PD	50
19	DNC	FLOAT	none	none
20	DNC	FLOAT	none	none
21	NC	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none
23	RX_D3	I	PD	9
24	RX_D2	I	PD	9
25	RX_D1	I	PD	9
26	RX_D0	I	PD	9
27	RX_CLK	I	PD	9
28	TX_CLK	I	none	none
29	TX_EN	I	none	none
30	TX_D3	I	none	none
31	TX_D2	I	none	none
32	TX_D1	I	none	none
33	TX_D0	I	none	none
34	VDDIO	SUPPLY	none	none
35	LED_0	I	PD	9
36	MDIO	OD, IO	none	none

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Table 6-4. Pin States - TC10 SLEEP

PIN NO	PIN NAME	TC10 SLEEP (All Supplies On)		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none
2	$\overline{\text{INT}}$	I	PU	9
3	$\overline{\text{RESET}}$	I	PU	9
4	XO	O	none	none
5	XI	I	none	none
6	LED_1[1]	I	PD	9
7	VSLEEP	SUPPLY	none	none
8	WAKE	I/O	PD	455
9	DNC	FLOAT	none	none
10	INH	OD, O	none	none
11	VDDA	SUPPLY	none	none
12	TRD_P	IO	none	none
13	TRD_M	IO	none	none
14	RX_ER	I	PD	6
15	RX_DV	I	PD	6
16	CLKOUT[2]	O	none	none
17	GND_ESC	FLOAT	none	none
18	GND_ESC	I	PD	50
19	DNC	FLOAT	none	none
20	DNC	FLOAT	none	none
21	DNC	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none
23	RX_D3	I	PD	9
24	RX_D2	I	PD	9
25	RX_D1	I	PD	9
26	RX_D0	I	PD	9
27	RX_CLK	I	PD	9
28	TX_CLK	I	none	none
29	TX_EN	I	none	none
30	TX_D3	I	none	none
31	TX_D2	I	none	none
32	TX_D1	I	none	none
33	TX_D0	I	none	none
34	VDDIO	SUPPLY	none	none
35	LED_0	I	PD	9
36	MDIO	OD, IO	none	none

1. If LED_1 is configured as CLKOUT, the TC10 Sleep IO state becomes: Output with no pull resistors
2. If CLKOUT is configured as LED_1, the TC10 Sleep IO state becomes: Input, 9 kΩ pull down

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Table 6-5. Pin States - MAC ISOLATE and IEEE PWDN

PIN NO	PIN NAME	MAC ISOLATE			IEEE PWDN		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9	I	PU	9
4	XO	O	none	none	O	none	none
5	XI	I	none	none	I	none	none
6	LED_1	O	none	none	O	none	none
7	VSLEEP	SUPPLY	none	none	SUPPLY	none	none
8	WAKE	IO	PD	455	IO	PD	455
9	NC	FLOAT	none	none	FLOAT	none	none
10	INH	OD, O	none	none	OD, O	none	none
11	VDDA	SUPPLY	none	none	SUPPLY	none	none
12	TRD_P	IO	none	none	IO	none	none
13	TRD_M	IO	none	none	IO	none	none
14	RX_ER	I	PD	6	I	PD	6
15	RX_DV	I	PD	6	O	none	none
16	CLKOUT	O	none	none	O	none	none
17	GND_ESC	FLOAT	none	none	FLOAT	none	none
18	GND_ESC	FLOAT	none	none	FLOAT	none	none
19	DNC	FLOAT	none	none	FLOAT	none	none
20	DNC	FLOAT	none	none	FLOAT	none	none
21	DNC	FLOAT	none	none	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none	SUPPLY	none	none
23	RX_D3	I	PD	9	O	none	none
24	RX_D2	I	PD	9	O	none	none
25	RX_D1	I	PD	9	O	none	none
26	RX_D0	I	PD	9	O	none	none
27	RX_CLK	I	PD	9	O	none	none
28	TX_CLK	I	PD	9	I	none	none
29	TX_EN	I	PD	9	I	none	none
30	TX_D3	I	PD	9	I	none	none
31	TX_D2	I	PD	9	I	none	none
32	TX_D1	I	PD	9	I	none	none
33	TX_D0	I	PD	9	I	none	none
34	VDDIO	SUPPLY	none	none	SUPPLY	none	none
35	LED_0	O	none	none	O	none	none
36	MDIO	OD, IO	none	none	OD, IO	none	none

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Table 6-6. Pin States - MII and RGMII

PIN NO	PIN NAME	MII			RGMII		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9	I	PU	9
4	XO	O	none	none	O	none	none
5	XI	I	none	none	I	none	none
6	LED_1	O	none	none	O	none	none
7	VSLEEP	SUPPLY	none	none	SUPPLY	none	none
8	WAKE	IO	PD	455	IO	PD	455
9	NC	FLOAT	none	none	FLOAT	none	none
10	INH	OD, O	none	none	OD, O	none	none
11	VDDA	SUPPLY	none	none	SUPPLY	none	none
12	TRD_P	IO	none	none	IO	none	none
13	TRD_M	IO	none	none	IO	none	none
14	RX_ER	O	none	none	I	PD	6
15	RX_DV	O	none	none	O	none	none
16	CLKOUT	O	none	none	O	none	none
17	GND_ESC	FLOAT	none	none	FLOAT	none	none
18	GND_ESC	FLOAT	none	none	FLOAT	none	none
19	DNC	FLOAT	none	none	FLOAT	none	none
20	DNC	FLOAT	none	none	FLOAT	none	none
21	DNC	FLOAT	none	none	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none	SUPPLY	none	none
23	RX_D3	O	none	none	O	none	none
24	RX_D2	O	none	none	O	none	none
25	RX_D1	O	none	none	O	none	none
26	RX_D0	O	none	none	O	none	none
27	RX_CLK	O	none	none	O	none	none
28	TX_CLK	O	none	none	I	none	none
29	TX_EN	I	none	none	I	none	none
30	TX_D3	I	none	none	I	none	none
31	TX_D2	I	none	none	I	none	none
32	TX_D1	I	none	none	I	none	none
33	TX_D0	I	none	none	I	none	none
34	VDDIO	SUPPLY	none	none	SUPPLY	none	none
35	LED_0	O	none	none	O	none	none
36	MDIO	OD, IO	none	none	OD, IO	none	none

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Table 6-7. Pin States - RMII MASTER and RMII SLAVE

PIN NO	PIN NAME	RMII MASTER			RMII SLAVE		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9	I	PU	9
4	XO	O	none	none	O	none	none
5	XI	I	none	none	I	none	none
6	LED_1	O	none	none	O	none	none
7	VSLEEP	SUPPLY	none	none	SUPPLY	none	none
8	WAKE	IO	PD	455	IO	PD	455
9	NC	FLOAT	none	none	FLOAT	none	none
10	INH	OD, O	none	none	OD, O	none	none
11	VDDA	SUPPLY	none	none	SUPPLY	none	none
12	TRD_P	IO	none	none	IO	none	none
13	TRD_M	IO	none	none	IO	none	none
14	RX_ER	O	none	none	O	none	none
15	RX_DV	O	none	none	O	none	none
16	CLKOUT	O	none	none	O	none	none
17	GND_ESC	FLOAT	none	none	FLOAT	none	none
18	GND_ESC	FLOAT	none	none	FLOAT	none	none
19	DNC	FLOAT	none	none	FLOAT	none	none
20	DNC	FLOAT	none	none	FLOAT	none	none
21	DNC	FLOAT	none	none	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none	SUPPLY	none	none
23	RX_D3	O, 50MHz	none	none	I	PD	9
24	RX_D2	I	PD	9	I	PD	9
25	RX_D1	O	none	none	O	none	none
26	RX_D0	O	none	none	O	none	none
27	RX_CLK	I	PD	9	I	PD	9
28	TX_CLK	I	none	none	I	none	none
29	TX_EN	I	none	none	I	none	none
30	TX_D3	I	none	none	I	none	none
31	TX_D2	I	none	none	I	none	none
32	TX_D1	I	none	none	I	none	none
33	TX_D0	I	none	none	I	none	none
34	VDDIO	SUPPLY	none	none	SUPPLY	none	none
35	LED_0	O	none	none	O	none	none
36	MDIO	OD, IO	none	none	OD, IO	none	none

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Table 6-8. Pin States - SGMII

PIN NO	PIN NAME	SGMII		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9
4	XO	O	none	none
5	XI	I	none	none
6	LED_1	O	none	none
7	VSLEEP	SUPPLY	none	none
8	WAKE	IO	PD	455
9	NC	FLOAT	none	none
10	INH	OD, O	none	none
11	VDDA	SUPPLY	none	none
12	TRD_P	IO	none	none
13	TRD_M	IO	none	none
14	RX_ER	I	PD	6
15	RX_DV	I	PD	6
16	CLKOUT	O	none	none
17	GND_ESC	FLOAT	none	none
18	GND_ESC	FLOAT	none	none
19	DNC	FLOAT	none	none
20	DNC	FLOAT	none	none
21	DNC	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none
23	RX_D3	O	none	none
24	RX_D2	O	none	none
25	RX_D1	I	PD	9
26	RX_D0	I	PD	9
27	RX_CLK	I	PD	9
28	TX_CLK	I	none	none
29	TX_EN	I	none	none
30	TX_D3	I	none	none
31	TX_D2	I	none	none
32	TX_D1	I	none	none
33	TX_D0	I	none	none
34	VDDIO	SUPPLY	none	none
35	LED_0	O	none	none
36	MDIO	OD, IO	none	none

(1) Type: I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	TYP	MAX	UNIT
Input Voltage	VDDA	–0.3		4	V
Input Voltage	VDDIO/VDDMAC (3.3V)	–0.3		4	V
Input Voltage	VDDIO/VDDMAC (2.5V)	–0.3		4	V
Input Voltage	VDDIO/VDDMAC (1.8V)	–0.3		4	V
Input Voltage	VSLEEP	-0.3		4	V
Pins	MDI	–0.3		4	V
Pins	MAC interface	–0.3		VDDMAC + 0.3	V
Pins	MDIO, MDC, GPIO, XI, XO, INT, RESET, CLKOUT	–0.3		VDDIO + 0.3	V
Pins	WAKE, INH	–0.3		VSLEEP + 0.3	V
DC Output Voltage	All Pins	–0.3		4	V
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature	–65		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
			TRD_N, TRD_P pins	±8000	
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750	
			Other pins	±750	
		IEC 61000-4-2 contact discharge	TRD_N, TRD_P pins	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIO / VDDMAC	IO Supply Voltage, 1.8V operation	1.62	1.8	1.98	V
	IO Supply Voltage, 2.5V operation	2.25	2.5	2.75	
	IO Supply Voltage, 3.3V operation	2.97	3.3	3.63	
VDDA	Core Supply Voltage, 3.3V	2.97	3.3	3.63	V
VSLEEP	Sleep Supply Voltage, 3.3V	2.97	3.3	3.63	V
T_A	Ambient temperature	–40		125	°C

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7.4 Thermal Information

THERMAL METRIC(1)		DP83TC812 RHA (VQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
100BASE-T1 PMA CONFORMANCE						
V_{OD-MDI}	Output Differential Voltage	$R_{L(diff)}$ = 100Ω			2.2	V
$R_{MDI-Diff}$	Integrated Differential Output Termination	TRD_P and TRD_M		100		Ω
BOOTSTRAP DC CHARACTERISTICS (2 Level)						
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 3.3V ±10%, 2-level strap	0		0.8	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 3.3V ±10%, 2-level strap	2		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 2.5V ±10%, 2-level strap	0		0.7	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 2.5V ±10%, 2-level strap	1.5		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 1.8V ±10%, 2-level strap	0		0.35 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 1.8V ±10%, 2-level strap	0.65 x VDDIO		VDDIO	V
BOOTSTRAP DC CHARACTERISTICS (3 Level)						
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 3.3V ±10%, 3-level strap	0		0.18 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 3.3V ±10%, 3-level strap	0.22 x VDDIO		0.42 x VDDIO	V
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 3.3V ±10%, 3-level strap	0.46 x VDDIO		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 2.5V ±10%, 3-level strap	0		0.19 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 2.5V ±10%, 3-level strap	0.27 x VDDIO		0.41 x VDDIO	V
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 2.5V ±10%, 3-level strap	0.58 x VDDIO		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 1.8V ±10%, 3-level strap	0		0.35 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 1.8V ±10%, 3-level strap	0.40 x VDDIO		0.75 x VDDIO	V

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7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 1.8V ±10%, 3-level strap	0.84 x VDDIO		VDDIO	V
IO CHARACTERISTICS						
V_{IH}	High Level Input Voltage	VDDIO = 3.3V ±10%	2			V
V_{IL}	Low Level Input Voltage	VDDIO = 3.3V ±10%			0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 3.3V ±10%	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 3.3V ±10%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 2.5V ±10%	1.7			V
V_{IL}	Low Level Input Voltage	VDDIO = 2.5V ±10%			0.7	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 2.5V ±10%	2			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 2.5V ±10%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 1.8V ±10%	0.65*VDDIO			V
V_{IL}	Low Level Input Voltage	VDDIO = 1.8V ±10%			0.35*VDDIO	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 1.8V ±10%	VDDIO-0.45			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 1.8V ±10%			0.45	V
I_{IH}	Input High Current(1)	T_A = -40°C to 125°C, VIN=VDDIO, All pins except XI and WAKE	-10		10	µA
I_{IH-XI}	Input High Current(1)	T_A = -40°C to 125°C, VIN=VDDIO, XI pin	-15		15	µA
I_{IL-XI}	Input Low Current(1)	T_A = -40°C to 125°C, VIN=GND, XI pin	-15		15	µA
I_{IL}	Input Low Current(1)	T_A = -40°C to 125°C, VIN=GND, All pins except XI pin	-10		10	µA
Iozh	Tri-state Output High Current	T_A = -40°C to 125°C, VIN=VDDIO, For pins RX_D[3:0], RX_CLK, MDIO, INT_N and XO	-10		10	µA
Iozh	Tri-state Output High Current	T_A = -40°C to 125°C, VIN=VDDIO, For pins RX_CTRL and RX_ER	-52		52	µA
Iozl	Tri-state Output Low Current(2)	T_A = -40°C to 125°C, VOUT=GND	-10		10	µA
R_{pulldn}	Internal Pull Down Resistor	RX_D[3:0], RX_CLK, LED_0, LED_1	6.2	8.4	10.7	kΩ
R_{pulldn}	Internal Pull Down Resistor	RX_CTRL, RX_ER	4.725	5.8	7.2	kΩ
R_{pulldn}	Internal Pull Down Resistor	WAKE		455		kΩ
R_{pullup}	Internal Pull Up Resistor	INT, RESET	6.3	9	11.2	kΩ
XI V_{IH}	High Level Input Voltage		1.3		VDDIO	V
XI V_{IL}	Low Level Input Voltage				0.5	V
C_{IN}	Input Capacitance XI			1		pF

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7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance INPUT PINS			5		pF
C_{OUT}	Output Capacitance XO			1		pF
C_{OUT}	Output Capacitance OUTPUT PINS			5		pF
R_{series}	Integrated MAC Series Termination Resistor	RX_D[3:0], RX_ER, RX_DV, RX_CLK	35	50	65	Ω
POWER CONSUMPTION						
I(3V3)	MII	-40°C to 125°C		57	63	mA
I(3V3)	RMII	-40°C to 125°C		57	63	mA
I(3V3)	RGMII	-40°C to 125°C		57	63	mA
I(3V3)	SGMII	-40°C to 125°C		81	95	mA
I(VDDIO=3.3V)	MII	-40°C to 125°C, VDDIO = VDDMAC		19	24	mA
I(VDDIO=3.3V)	RMII	-40°C to 125°C, VDDIO = VDDMAC		18	23	mA
I(VDDIO=3.3V)	RGMII	-40°C to 125°C, VDDIO = VDDMAC		13	21	mA
I(VDDIO=3.3V)	SGMII	-40°C to 125°C, VDDIO = VDDMAC		7	12	mA
I(VDDIO=2.5V)	MII	-40°C to 125°C, VDDIO = VDDMAC		12	18	mA
I(VDDIO=2.5V)	RMII	-40°C to 125°C, VDDIO = VDDMAC		12	17	mA
I(VDDIO=2.5V)	RGMII	-40°C to 125°C, VDDIO = VDDMAC		12	16	mA
I(VDDIO=2.5V)	SGMII	-40°C to 125°C, VDDIO = VDDMAC		6	9	mA
I(VDDIO=1.8V)	MII	-40°C to 125°C, VDDIO = VDDMAC		9	13	mA
I(VDDIO=1.8V)	RMII	-40°C to 125°C, VDDIO = VDDMAC		9	13	mA
I(VDDIO=1.8V)	RGMII	-40°C to 125°C, VDDIO = VDDMAC		9	12	mA
I(VDDIO=1.8V)	SGMII	-40°C to 125°C, VDDIO = VDDMAC		4	6	mA
POWER CONSUMPTION (LOW POWER MODE)						
I(VDDA3V3)	IEEE Power Down	-40°C to 125°C, All interfaces		8	22	mA
I(VDDA3V3)	TC-10 Sleep	-40°C to 125°C, All interfaces		30	50	mA
I(VDDA3V3)	RESET	-40°C to 125°C, All interfaces		9	23	mA
I(VDDA3V3)	Standby	-40°C to 125°C, MII		15	33	mA
I(VDDA3V3)	Standby	-40°C to 125°C, RMII		15	30	mA
I(VDDA3V3)	Standby	-40°C to 125°C, RGMII		15	30	mA
I(VDDA3V3)	Standby	-40°C to 125°C, SGMII		15	30	mA
I(VDDIO=3.3V)	IEEE Power Down	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		15	23	mA
I(VDDIO=3.3V)	TC-10 Sleep	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		15	23	mA
I(VDDIO=3.3V)	RESET	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		15	23	mA
I(VDDIO=3.3V)	Standby	-40°C to 125°C, MII, VDDIO=VDDMAC		19	25	mA
I(VDDIO=3.3V)	Standby	-40°C to 125°C, RMII, VDDIO=VDDMAC		16	20	mA
I(VDDIO=3.3V)	Standby	-40°C to 125°C, RGMII, VDDIO=VDDMAC		14	20	mA
I(VDDIO=3.3V)	Standby	-40°C to 125°C, SGMII, VDDIO=VDDMAC		14	16	mA
I(VDDIO=2.5V)	IEEE Power Down	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		10	16	mA
I(VDDIO=2.5V)	TC-10 Sleep	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		10	16	mA

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7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I(VDDIO=2.5V)	RESET	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		10	16	mA
I(VDDIO=2.5V)	Standby	-40°C to 125°C, MII, VDDIO=VDDMAC		14	18	mA
I(VDDIO=2.5V)	Standby	-40°C to 125°C, RMII, VDDIO=VDDMAC		11	14	mA
I(VDDIO=2.5V)	Standby	-40°C to 125°C, RGMII, VDDIO=VDDMAC		9	14	mA
I(VDDIO=2.5V)	Standby	-40°C to 125°C, SGMII, VDDIO=VDDMAC		9	14	mA
I(VDDIO=1.8V)	IEEE Power Down	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		7	11	mA
I(VDDIO=1.8V)	TC-10 Sleep	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		7	11	mA
I(VDDIO=1.8V)	RESET	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		7	11	mA
I(VDDIO=1.8V)	Standby	-40°C to 125°C, MII, VDDIO=VDDMAC		10	12	mA
I(VDDIO=1.8V)	Standby	-40°C to 125°C, RMII, VDDIO=VDDMAC		7	11	mA
I(VDDIO=1.8V)	Standby	-40°C to 125°C, RGMII, VDDIO=VDDMAC		6	11	mA
I(VDDIO=1.8V)	Standby	-40°C to 125°C, SGMII, VDDIO=VDDMAC		6	11	mA
I(VSLEEP)	TC-10 Sleep	-40°C to 125°C, All interfaces, All other supplies are off		7	18	µA
SGMII Input						
V_{IDTH}	Input differential voltage tolerance	SI_P and SI_N, AC coupled	0.1			V
$R_{IN-DIFF}$	Receiver differential input impedance (DC)		80		120	ohm
SGMII Output						
	Clock signal duty cycle	SO_P and SO_N, AC coupled, 0101010101 pattern	48		52	%
	Output Differential Voltage	SO_P and SO_N, AC coupled	150		400	mV
Voltage Sensor						
VDDA	VDDA Sensor Range	-40°C to +125°C	2.7	3.3	4	V
	VDDA Sensor Resolution (LSB)	-40°C to +125°C		8.8		mV
	VDDA Sensor Accuracy (voltage and temperature variation on single part)	-40°C to +125°C	-120		120	mV
	VDDA Sensor Accuracy (part-part variation)	-40°C to +125°C	-50		50	mV

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7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDIO / VDDMAC	VDDIO / VDDMAC Sensor Range	-40℃ to +125℃	1.44		3.9	V
	VDDIO / VDDMAC Sensor Resolution (LSB)	-40℃ to +125℃		16		mV
	VDDIO / VDDMAC Sensor Accuracy (voltage and temperature variation on single part)	-40℃ to +125℃	-144		144	mV
	VDDIO / VDDMAC Sensor Accuracy (part-part variation)	-40℃ to +125℃	-85		85	mV
VSLEEP	VSLEEP Sensor Range	-40℃ to +125℃	2.7	3.3	4	V
	VSLEEP Sensor Resolution (LSB)	-40℃ to +125℃		8.8		mV
	VSLEEP Sensor Accuracy (voltage and temperature variation on single part)	-40℃ to +125℃	-120		120	mV
	VSLEEP Sensor Accuracy (part-part variation)	-40℃ to +125℃	-50		50	mV

(1) For pins: MDC, TX_CLK, TX_CTRL, TX_D[3:0], and RESET_N
(2) For pins: RX_D[3:0], RX_CLK, RX_CTRL, MDIO, INT_N, and XO.

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7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
MII TIMING						
T1.1	TX_CLK High / Low Time		16	20	24	ns
T1.2	TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK		10			ns
T1.3	TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK		0			ns
T2.1	RX_CLK High / Low Time		16	20	24	ns
T2.2	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising		10		30	ns
RMII MASTER TIMING						
T3.1	RMII Master Clock Period			20		ns
	RMII Master Clock Duty Cycle		35		65	%
T3.2	TX_D[1:0], TX_ER, TX_EN Setup to RMII Master Clock		4			ns
T3.3	TX_D[1:0], TX_ER, TX_EN Hold from RMII Master Clock		2			ns
T3.4	RX_D[1:0], RX_ER, CRS_DV Delay from RMII Master Clock rising edge		4	10	14	ns
RMII SLAVE TIMING						
T3.1	Input Reference Clock Period			20		ns
	Reference Clock Duty Cycle		35		65	%
T3.2	TX_D[1:0], TX_ER, TX_EN Setup to XI Clock rising		4			ns
T3.3	TX_D[1:0], TX_ER, TX_EN Hold from XI Clock rising		2			ns
T3.4	RX_D[1:0], RX_ER, CRS_DV Delay from XI Clock rising		4		14	ns
RGMII INPUT TIMING						
T_{cyc}	Clock Cycle Duration	TX_CLK	36	40	44	ns
$T_{setup(align)}$	TX_D[3:0], TX_CTRL Setup to TX_CLK (Align Mode)		1	2		ns
$T_{hold(align)}$	TX_D[3:0], TX_CTRL Hold from TX_CLK (Align Mode)		1	2		ns
RGMII OUTPUT TIMING						
$T_{skew(align)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Align Mode Enabled)	On PHY Pins	-750		750	ps
$T_{setup(shift)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Shift Mode Enabled, default)	On PHY Pins	2			ns
T_{cyc}	Clock Cycle Duration	RX_CLK	36	40	44	ns
Duty_G	Duty Cycle	RX_CLK	45	50	55	%
Tr/Tf	Rise / Fall Time (20% to 80%)	C_{LOAD} = 5pF			1.2	ns
SMI TIMING						
T4.1	MDC to MDIO (Output) Delay Time	25pF load capacitance	0		40	ns
T4.2	MDIO (Input) to MDC Setup Time		10			ns
T4.3	MDIO (Input) to MDC Hold Time		10			ns
	MDC Frequency			2.5	20	MHz
POWER-UP TIMING						
T5.1	Supply ramp time: For all supplies (1)		0.2		8	ms
T5.3	XTAL Startup / Settling: Powerup to XI good/stabilized			0.35		ms
T5.4	Oscillator stabilization time from power up				10	ms
	Last Supply power up To Reset Release				10	ms
T5.5	Post power-up to SMI ready: Post Power-up wait time required before MDC preamble can be sent for register access		10			ms
T5.6	Power-up to Strap latch-in				10	ms

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7.6 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T5.7	CLKOUT Startup/Settling: Powerup to CLKOUT good/stabilized				10	ms
T5.8	Power-up to idle stream				10	ms
RESET TIMING (RESET_N)						
T6.1	Reset Pulse Width: Miminum Reset pulse width to be able to reset		720			ns
T6.2	Reset to SMI ready: Post reset wait time required before MDC preamble can be sent for register access		1			ms
T6.3	Reset to Strap latch-in: Hardware configuration pins transition to output drivers			40		µs
T6.4	Reset to idle stream				1800	µs
WAKE REQUEST AND WAKE PULSE TIMING						
T7.1	Local Wake-Up Pulse Duration		40			µs
T7.2	Local Wake-Up to INH Transition				40	µs
T7.3	Energy-detect-based Wake-Up Pulse Duration				0.7	ms
T7.4	Energy-detect-based Wake-Up to INH Transition				0.7	ms
T7.5	Energy-detect-based Wake-Up to WAKE forwarding pulse				1.4	ms
TRANSMIT LATENCY TIMING						
	MII Rising edge TX_CLK with assertion TX_EN to SSD symbol on MD		205		233	ns
	Slave RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI		374		409	ns
	Master RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI		382		408	ns
	RGMII Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI		370		390	ns
	First symbol of SGMII to SSD symbol on MDI		420		456	ns
RECEIVE LATENCY TIMING						
	SSD symbol on MDI to MII Rising edge of RX_CLK with assertion of RX_DV		467		491	ns
	SSD symbol on MDI to Slave RMII Rising edge of XI clock with assertion of CRS_DV		527		574	ns
	SSD symbol on MDI to Master RMII Rising edge of Master clock with assertion of CRS_DV		521		557	ns
	SSD symbol on MDI to Rising edge of RGMII RX_CLK with assertion of RX_CTRL		484		511	ns
	SSD symbol on MDI to first symbol of SGMII		708		788	ns
25 MHz OSCILLATOR REQUIREMENTS						
	Frequency Tolerance		-100		+100	ppm
	Rise / Fall Time (10%-90%)				8	ns
	Jitter Tolerance (RMS)				25	ps
	XI Duty Cycle in external clock mode		40		60	%
50 MHz OSCILLATOR REQUIREMENTS						
	Frequency			50		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Rise / Fall Time (10% - 90%)				4	ns
	Duty Cycle		35		65	%
25 MHz CRYSTAL REQUIREMENTS						
	Frequency			25		MHz

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7.6 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Equivalent Series Resistance				100	Ω
OUTPUT CLOCK TIMING (25 MHz)						
	Frequency (PPM)		-100		100	-
	Duty Cycle		40		60	%
	Rise Time				5000	ps
	Fall Time				5000	ps
	Jitter (Short Term)				1000	ps
	Frequency			25		MHz

(1) For supplies with ramp rate longer than 8ms, a RESET pulse will be required after the last supply becomes stable.

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7.7 Timing Diagrams

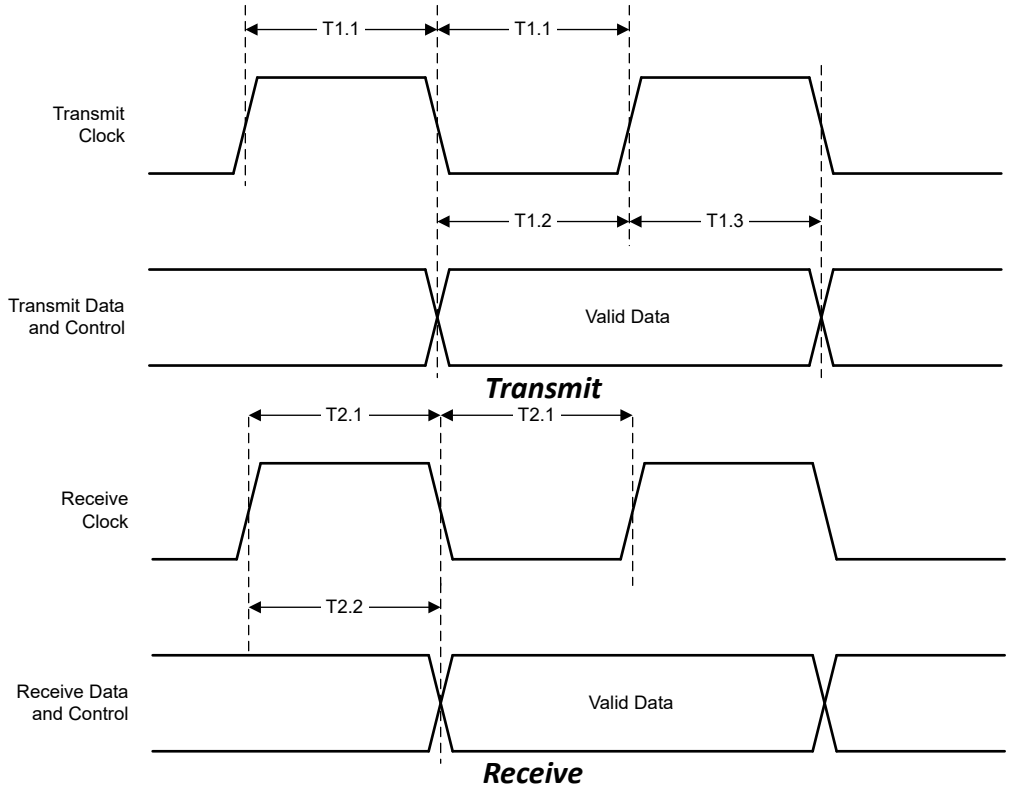

Figure 7-1. MII Timing

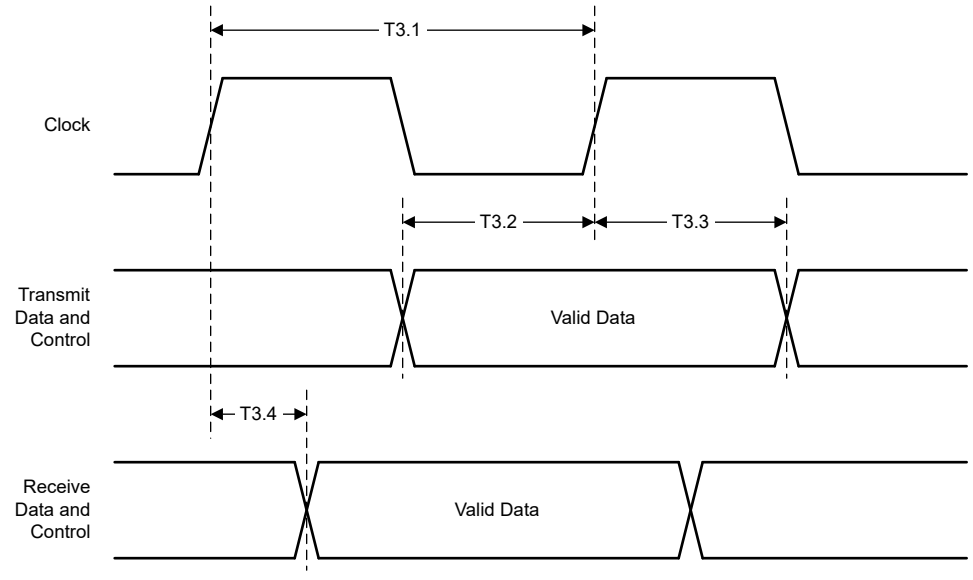

Figure 7-2. RMII Transmit and Receive Timing

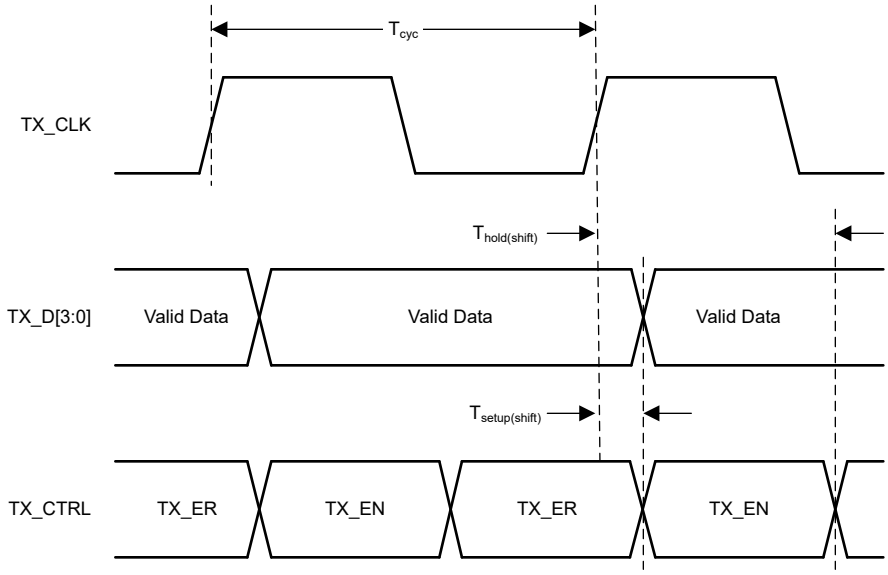

Figure 7-3. RGMII Transmit Timing (Internal Delay Enabled)

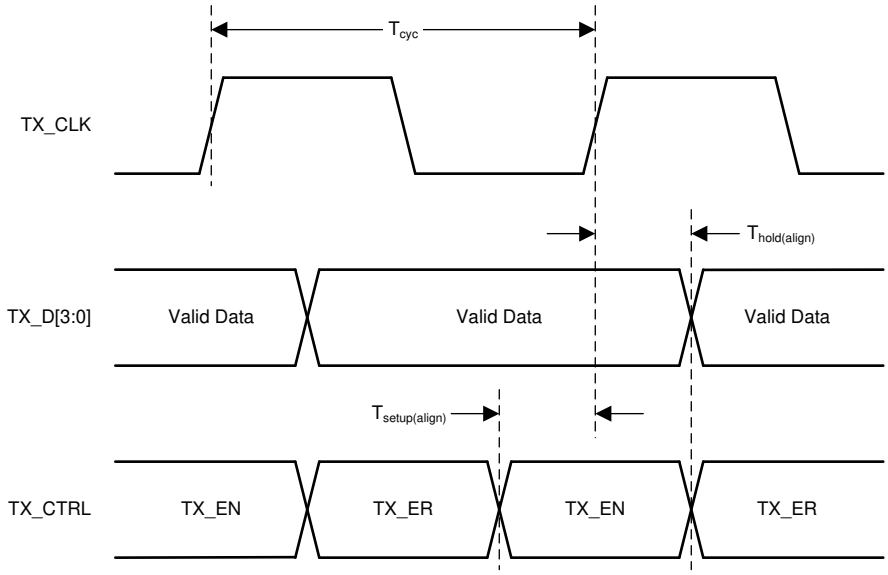

Figure 7-4. RGMII Transmit Timing (Internal Delay Disabled)

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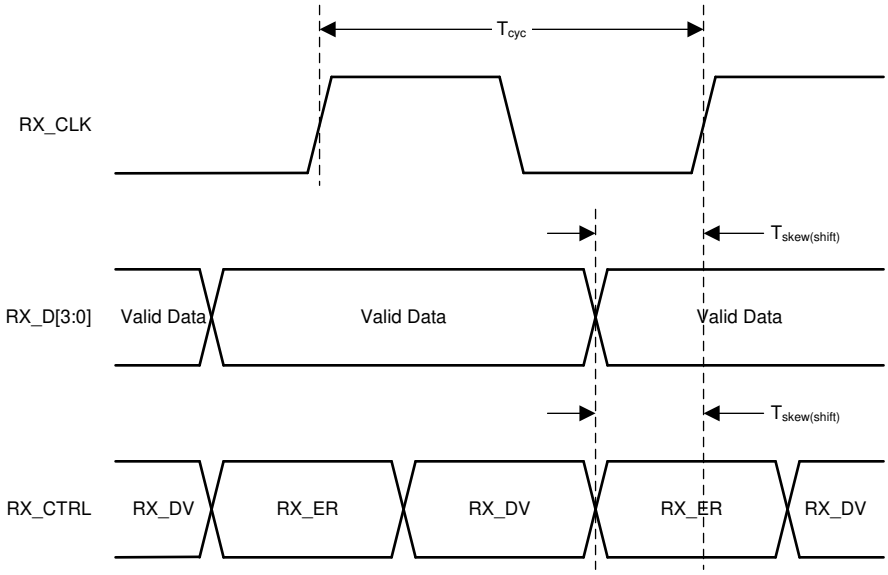

Figure 7-5. RGMII Receive Timing (Internal Delay Enabled)

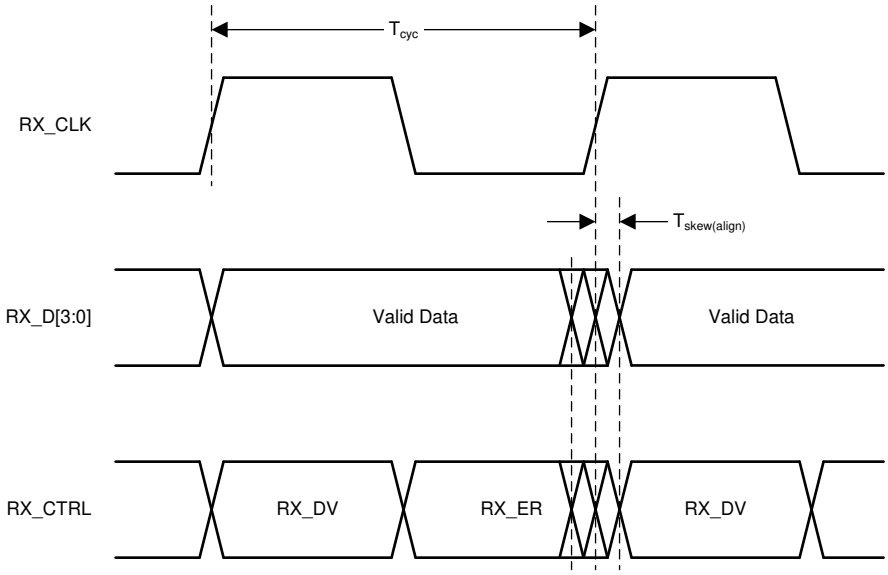

Figure 7-6. RGMII Receive Timing (Internal Delay Disabled)

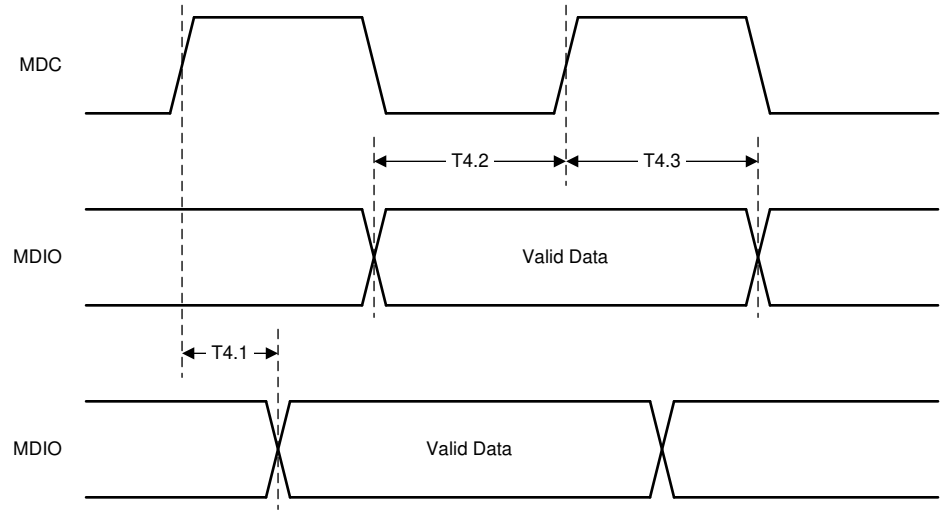

Figure 7-7. Serial Management Timing

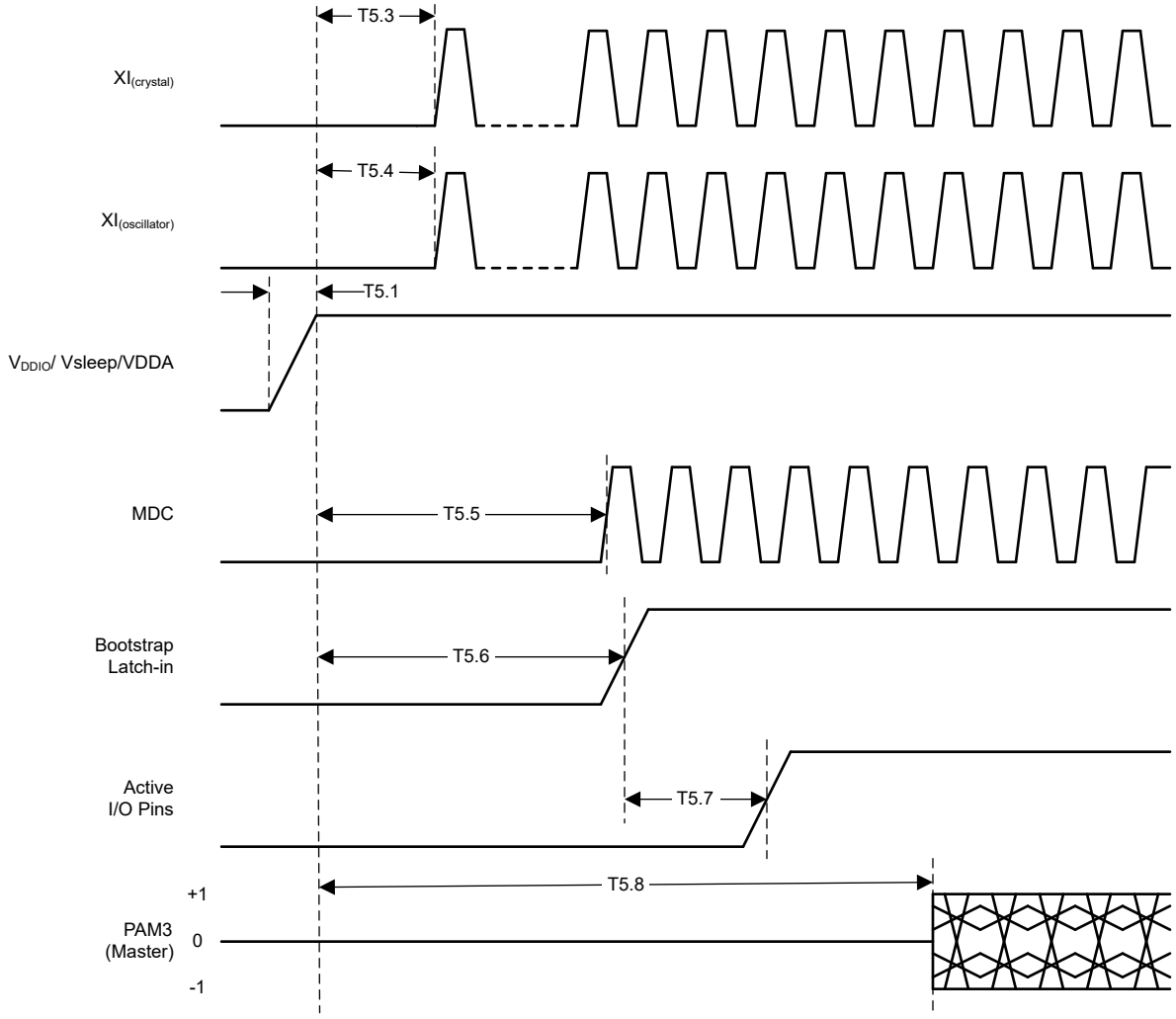

Figure 7-8. Power-Up Timing

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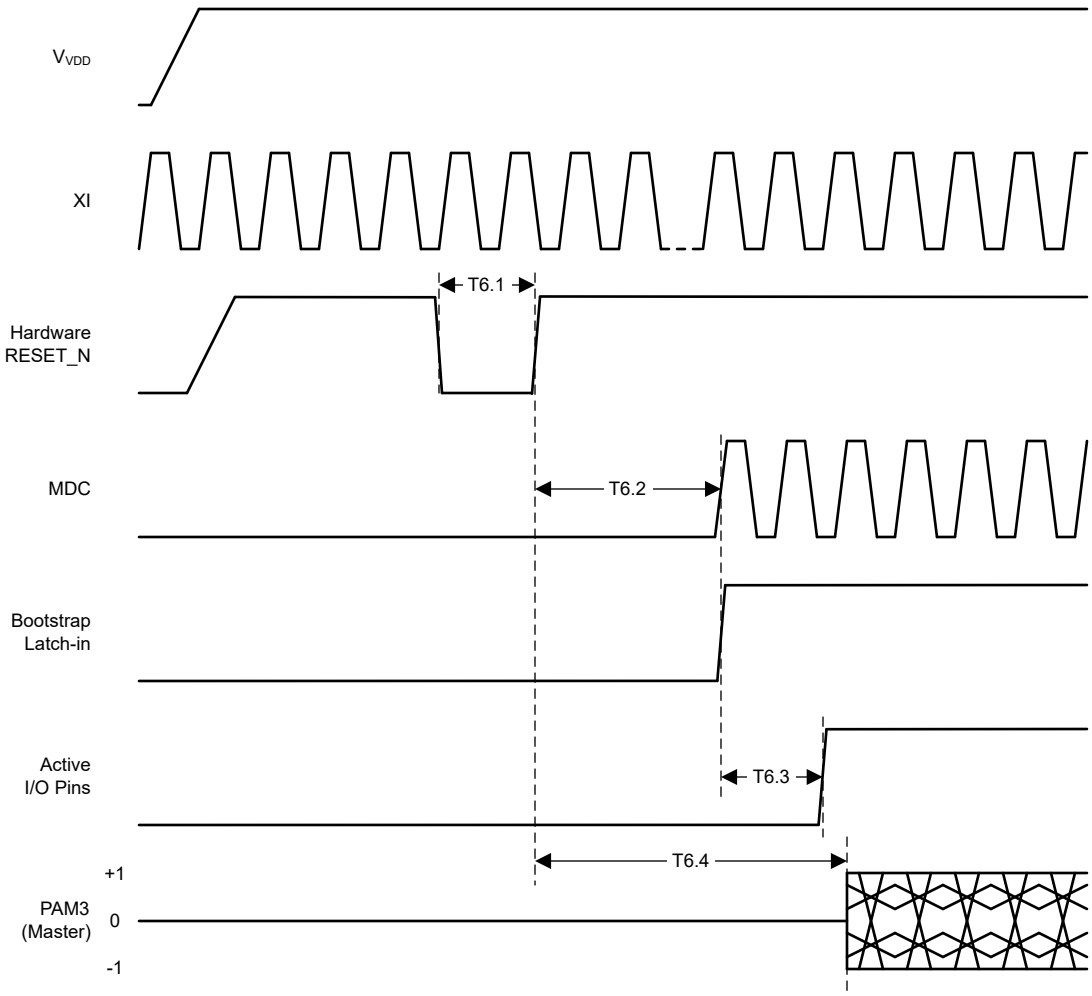

Figure 7-9. Reset Timing

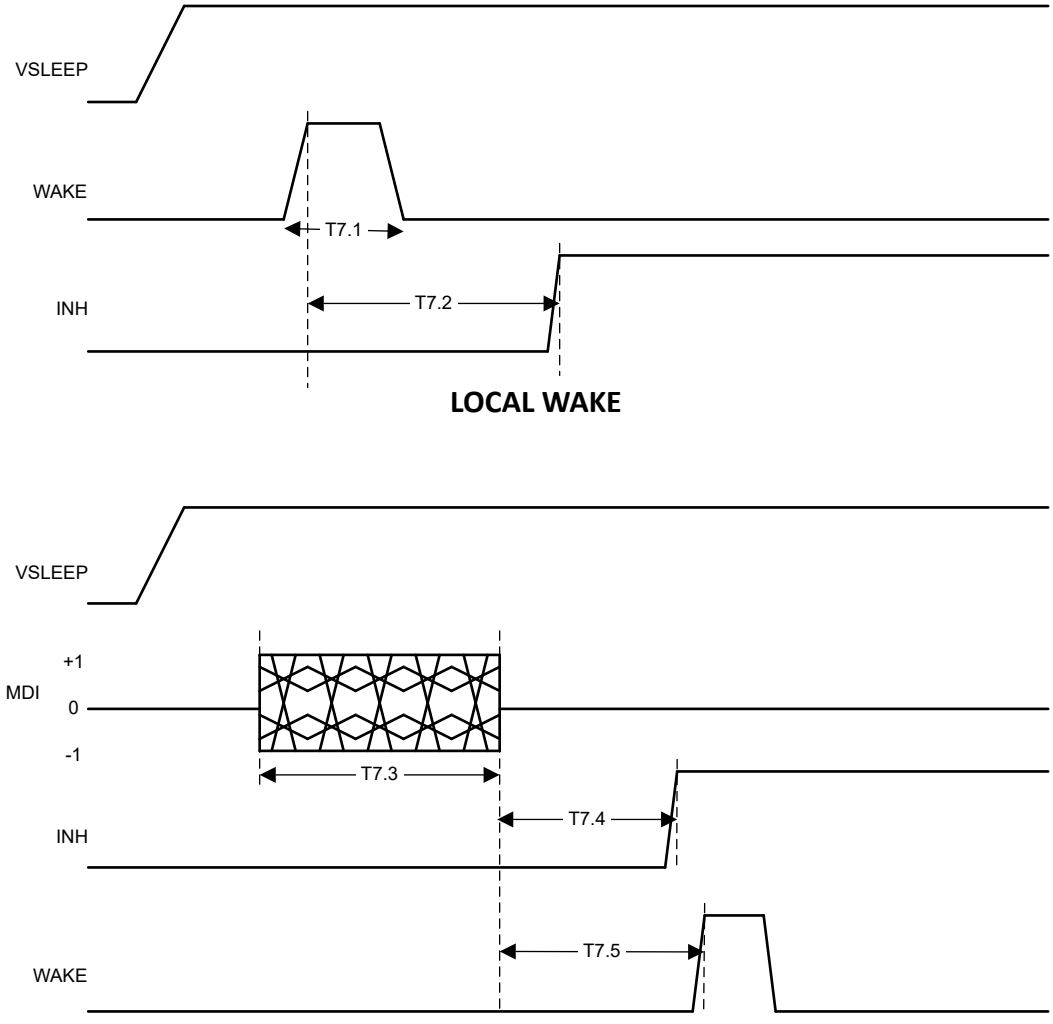

Figure 7-10. WAKE Timing

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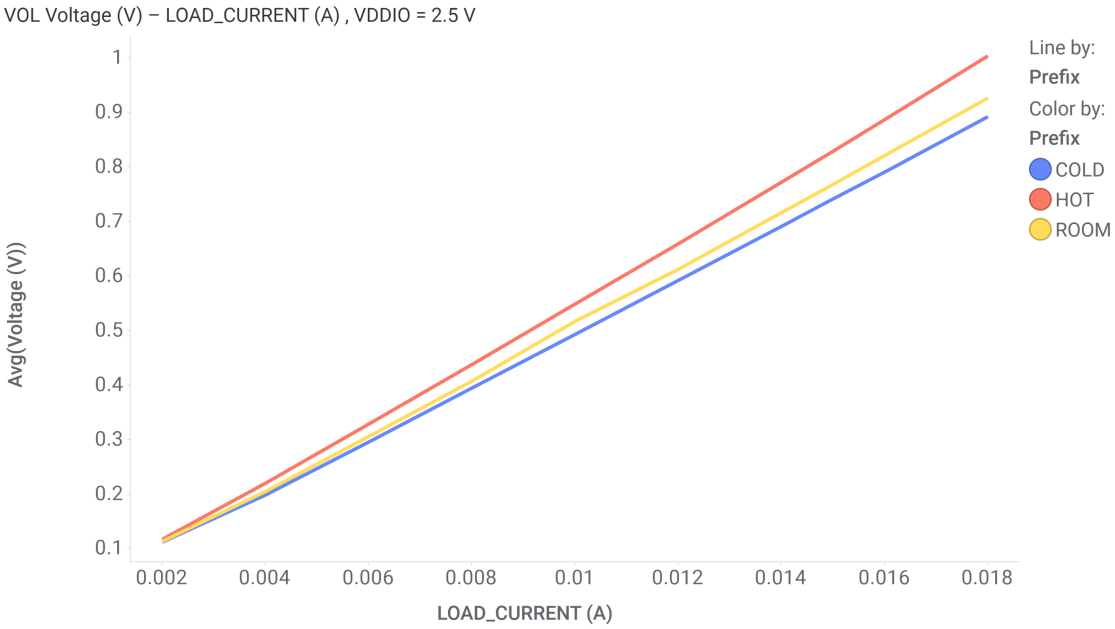
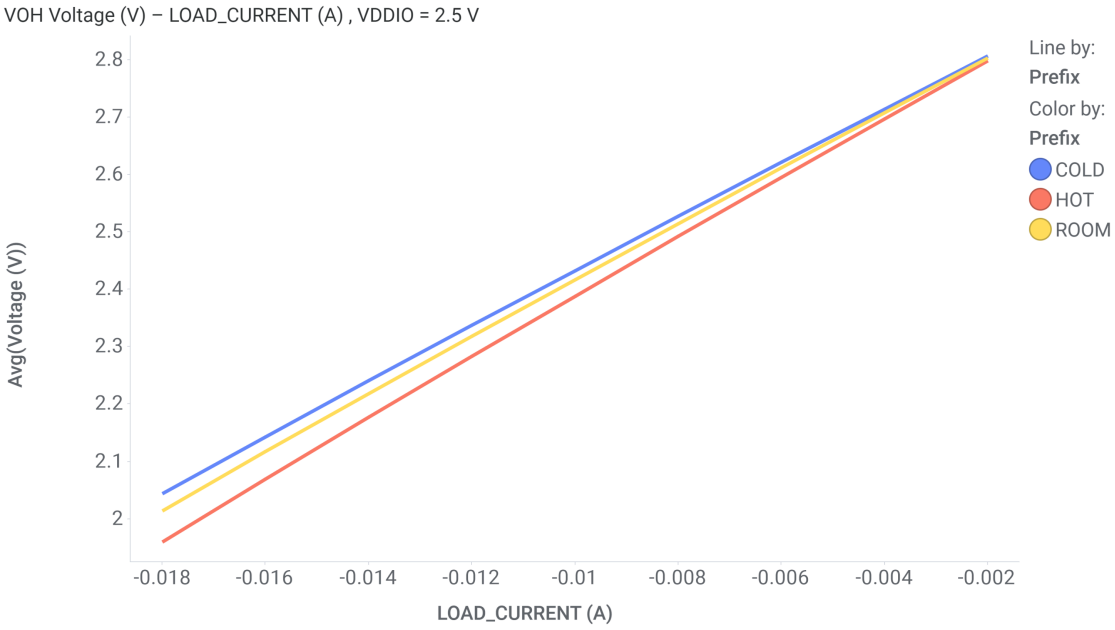
7.8 Typical Characteristics



VDDIO = 2.5 V

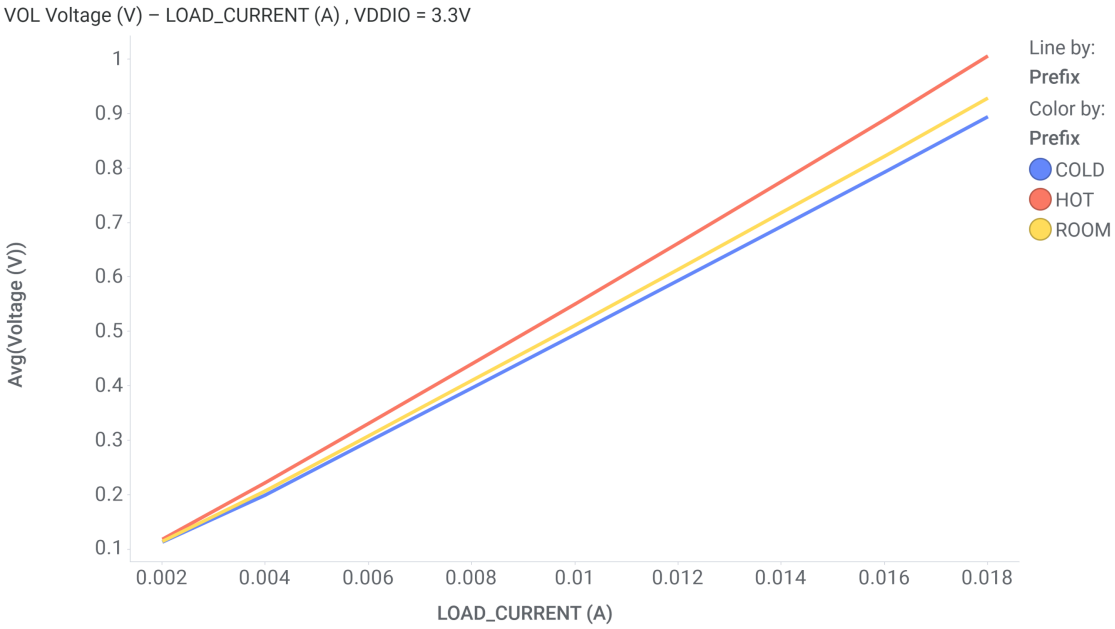
Figure 7-11. LED pins VOL (2.5 V)



VDDIO = 2.5 V

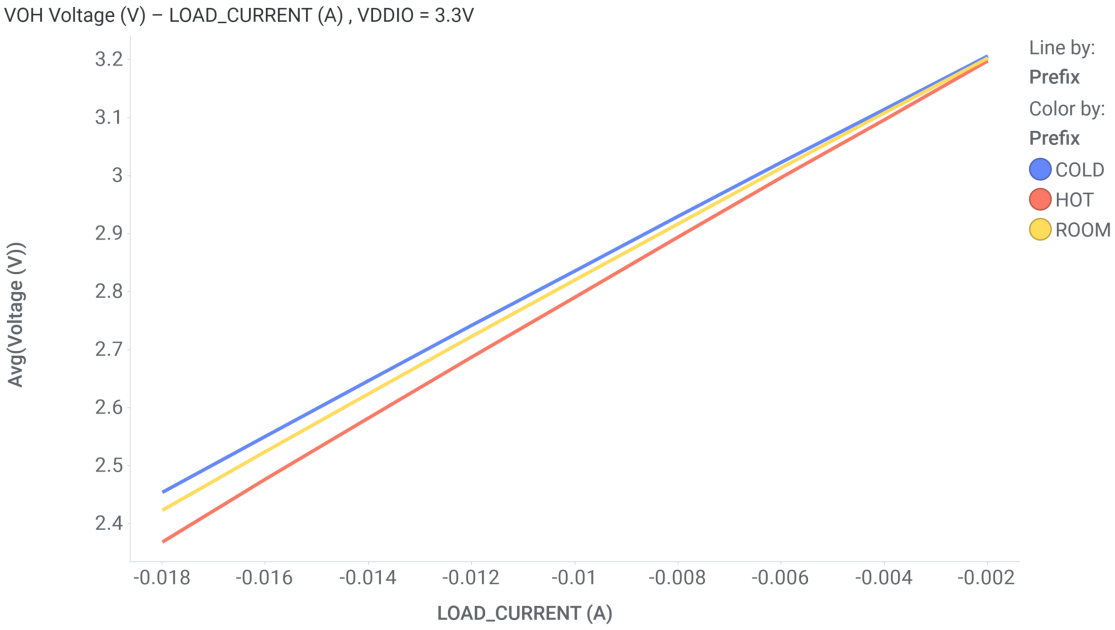
Figure 7-12. LED pins VOH (2.5 V)

7.8 Typical Characteristics



VDDIO = 3.3 V

Figure 7-13. LED pins VOL (3.3 V)



VDDIO = 3.3 V

Figure 7-14. LED pins VOH (3.3 V)

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8 Detailed Description

8.1 Overview

The DP83TC812S-Q1 is a 100BASE-T1 automotive Ethernet Physical Layer transceiver. It is IEEE 802.3bw compliant and AEC-Q100 qualified for automotive applications. The DP83TC812S-Q1 is interoperable with both BroadR-Reach PHYs and 100BASE-T1 PHYs.

The DP83TC812S-Q1 also supports Open Alliance TC-10 low power mode for additional power savings. The PHY supports WAKE and INH pins for implementing TC-10 functionality in the system.

This device is specifically designed to operate at 100-Mbps speed while meeting stringent automotive EMC limits. The DP83TC812S-Q1 transmits PAM3 ternary symbols at 66.667 MHz over unshielded single twisted-pair cable. It is application flexible; supporting MII, RMII, RGMII, and SGMII in a single 36-pin VQFN wettable flank package.

There is an extensive Diagnostic Tool Kit within the DP83TC812S-Q1 for both in-system use as well as debug, compliance and system prototyping for bring-up. The DP83TC812S-Q1 can meet IEC61000-4-2 Level 4 electrostatic discharge limits and it also includes an on-chip ESD sensor for detecting ESD events in real-time.

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8.2 Functional Block Diagram

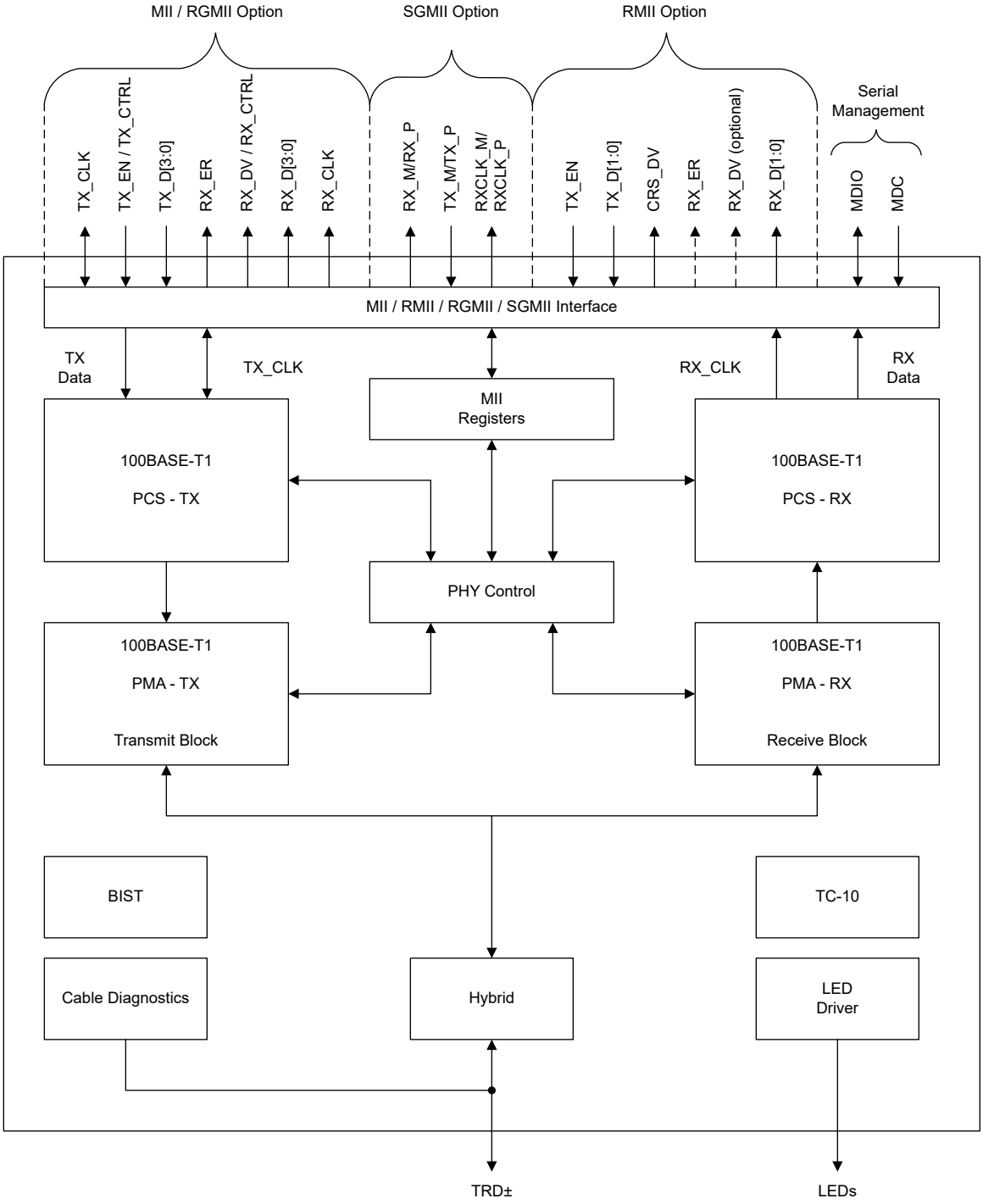

Figure 8-1. DP83TC812S-Q1

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8.3 Feature Description

Note

Refer to SNLA389 Application Note for more information about the register settings used for compliance testing. It is necessary to use these register settings to achieve the same performance as observed during compliance testing.

8.3.1 Diagnostic Tool Kit

The DP83TC812 diagnostic tool kit provides mechanisms for monitoring normal operation, device-level debugging, system-level debugging, fault detection, and compliance testing. This tool kit includes a built-in self-test with PRBS data, various loopback modes, Signal Quality Indicator (SQI), Time Domain Reflectometry (TDR), undervoltage monitor, electrostatic discharge monitor, and IEEE 802.3bw test modes.

8.3.1.1 Signal Quality Indicator

When the DP83TC812-Q1 is active, the Signal Quality Indicator may be used to determine the quality of link based on SNR readings made by the device. SQI is presented as a 8-level indication. Signal quality indication is accessible through register 0x871. SQI is continuously monitored by the PHY to allow for real-time link signal quality status.

Bits[3:1] in register 0x871 provide SQI value while bits [7:5] provide the worst SQI value since the last read. The SQI value reported in register 0x871[3:1] map directly to the SQI levels required by Open Alliance.

To get the most accurate SQI reporting, use the initialization routine explained in SNLA389 application note.

Table 8-1. Signal Quality Indicator

REG 0x871[3:1]	OPEN ALLIANCE SQI LEVEL	LINK QUALITY
0x0	0 (Worst)	Poor/ No Link
0x1	1	
0x2	2	
0x3	3	
0x4	4	Good / Excellent Link
0x5	5	
0x6	6	
0x7	7 (Best)	

8.3.1.2 Electrostatic Discharge Sensing

Electrostatic discharge is a serious issue for electronic circuits and if not properly mitigated can create short-term issues (signal integrity, link drops, packet loss) as well as long-term reliability faults. The DP83TC812 has robust integrated ESD circuitry and offers an ESD sensing architecture. ESD events can be detected on MDI pins independently for further analysis and debug.

Additionally, the DP83TC812 provides an interrupt status flag; *Register 0x12[11]* is set when an ESD event is logged. This interrupt can be routed to the INT_N pin using bit[3] of the same register. *Register 0x442[14:9]* store the number of ESD events that have occurred since power-up. Hardware and software resets are ignored by the ESDS register to prevent unwarranted clearing.

8.3.1.3 Time Domain Reflectometry

Time domain reflectometry helps determine the quality of the cable, connectors and terminations in addition to estimating OPEN and SHORT faults along a cable. The DP83TC812-Q1 transmits a test pulse down the attached twisted-pair cable. Transmitted pulses continue down the cable and reflect from each imperfection and fault, allowing the device to measure the time to return and strength (amplitude) of all reflections. This technique enables the DP83TC812-Q1 to identify cable OPENs and SHORTs.

TDR is activated by setting bit[15] in register 0x1E. The procedure is as follows.

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- Configure the DP83TC812-Q1 as per the initilization settings from SNLA389 Application Note
- Ensure that the Link Partner connected to the PHY is slient. Link will be down during TDR execution.
- Run the Pre-TDR configuration settings as listed in SNLA389.
- Start TDR by setting register 0x1E[15] to '1'.
- Wait 100ms, read register 0x1E[1:0]
  - If it reads 0b10 then TDR has executed successfully.
- If TDR executed successfully then read register 0x310 to get TDR results.
  - 0x310[8]: 0 = Half Wire Open not detected or 1 = Half Wire Open detected
  - 0x310[7]: 0 = Cable fault not detected or 1 = Cable fault detected
  - 0x310[6]: 0 = Cable fault is OPEN or 1 = Cable fault is SHORT
  - If valid cable fault is detected then 0x310[5:0] will store the location value in meters.

8.3.1.4 Voltage Sensing

The DP83TC812 offers sensors for monitoringvoltage at the supply pins. Undervoltage monitoring are always active in the DP83TC812 by default. If an undervoltage condition is detected, interrupt status flag is set in register 0x0013. These interrupts can also be optionally routed to the INT pin using the same register.

The following method must be used to read each sensor.

- Step 1: Program register 0x0467 = 0x6004 ; Initial configuration of monitors
- Step 2: Program register 0x046A = 0x00A3; Enable Monitors
- Step 3: Configure register 0x0468 with the corresponding setting to select the required sensor.
  - VDDA Sensor: Use 0x0468 = 0x0920
  - VSLEEP Sensor: Use 0x0468 = 0x1920
  - VDDMAC Sensor: Use 0x0468 = 0x2920
  - VDDIO Sensor: Use 0x0468 = 0x3920
- Step 4: Read register 0x047B[14:7] and convert this output code to decimal.
- Step 5: Use the output code in the following equations to get the sensor's absolute value. Refer to Table 8-2 table for constant values for corresponding sensors.
  - vdda_value = 3.3 + (vdda_output_code - vdda_output_mean_code)*slope_vdda_sensor
  - vsleep_value = 3.3 + (vsleep_output_code - vsleep_output_mean_code)*slope_vsleep_sensor
  - vddmac_value = 3.3 + (vddmac_output_code - vddmac_output_mean_code)*slope_vddmac_sensor
  - vddio_value = 3.3 + (vddio_output_code - vddio_output_mean_code)*slope_vddio_sensor

Table 8-2. Sensors Constant Values

Sensor	Constant	Value
VDDA	vdda_output_mean_code	126
	slope_vdda_sensor	0.0088
VSLEEP	vsleep_output_mean_code	134
	slope_vsleep_sensor	0.0088
VDDMAC	vddmac_output_mean_code	205
	slope_vddmac_sensor	0.016
VDDIO	vddio_output_mean_code	205
	slope_vddio_sensor	0.016

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8.3.1.5 BIST and Loopback Modes

DP83TC812 incorporates a data-path's Built-In-Self-Test (BIST) to check the PHY level and system level data-paths. BIST has following integrated features which make the system level data transfer tests (through-put etc) and diagnostics possible without relying on MAC or external data generator hardware/software.

The following features are available in the DP83TC812 which can be used for easy evaluation.

1. Loopback modes
2. Data Generator
   a. Customizable MAC packets generator
   b. Transmitted packet counter
   c. PRBS stream generator
3. Data Checker
   a. Received MAC packets error checker
   b. Received packet counter: Counts total packets received and packets received with errors
   c. PRBS lock and PRBS error checker

8.3.1.5.1 Data Generator and Checker

DP83TC812 supports inbuilt Pseudo-random data generator and checker which can be used in conjuction with Loopback modes to check the data path. Data generator can be programmed to generate either user defined MAC packets or PRBS stream.

Following parameters of generated MAC packets can be configured (refer to registers<0x061B>,register<0x061A> and register<0x0624> for required configuration):

- Packet Length
- Inter-packet gap
- Defined number of packets to be sent or continuous transmission
- Packet data-type: Incremental/Fixed/PRBS
- Number of valid bytes per packet

8.3.1.5.2 xMII Loopback

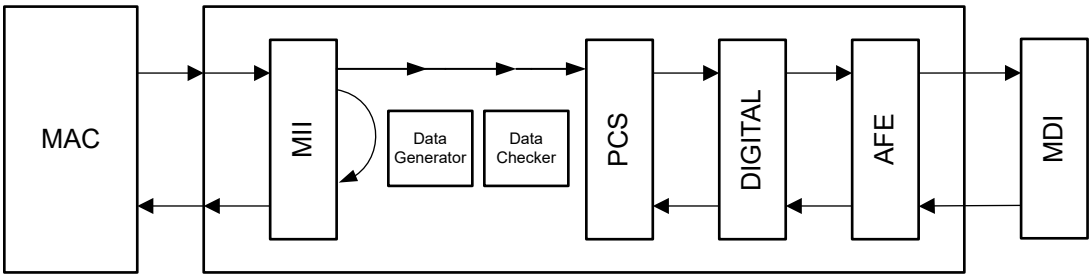

Figure 8-2. xMII Loopback Without Data Generator

xMII Loopback is the shallowest loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. When in xMII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83TC812 to the RX pins where it can be checked by the MAC. There is no link indication when in xMII loopback.

Enable Loopback

Write register 0x0000 = 0x6100

Enable data generator/checker for MAC side

Data will be generated externally on the MAC TX pins.

Use the following register settings to enable checker depending on the MAC interface mode.

- For RGMII, write register 0x0619 = 0x1004
- For SGMII, write register 0x0619 = 0x1114
- For RMII, write register 0x0619 = 0x1224
- For MII, write register 0x0619 = 0x1334

Check incoming data from MAC side

Data can be verified at MAC interface RX pins.

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E

Enable data generator/checker for Cable side

Not applicable as data will be generated externally on the MAC interface TX pins.

Check data for Cable side

Not applicable as PRBS stream checker works with only internal PRBS generator.

Other system requirements

Generated data will be going to cable side.

8.3.1.5.3 PCS Loopback

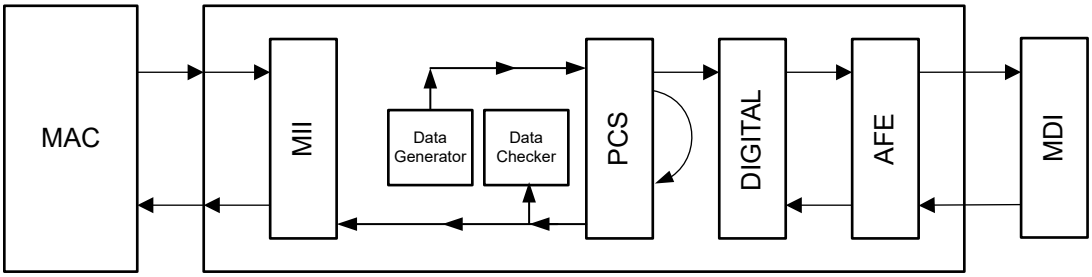

Figure 8-3. PCS Loopback with data generator

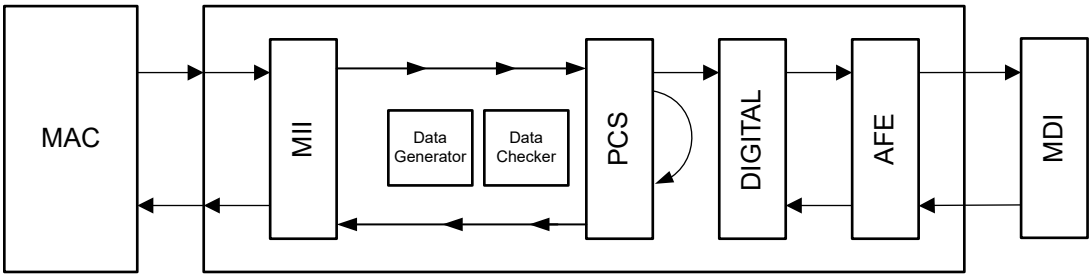

Figure 8-4. PCS Loopback without data generator

PCS Loopback will loop back data prior to it exiting the PCS and entering the PMA. Data received from the MAC on the transmit path is brought through the digital block within the PHY where it is then routed back to the MAC through the receive path. The DP83TC812 receive PMA circuitry is configured for isolation to prevent contention.

Enable Loopback

Write register 0x0016 = 0x0102

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Enable data generator/checker for MAC side

Write register 0x0619 = 0x1555

Write register 0x0624 = 0x55BF

Check incoming data from MAC side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E

Enable data generator/checker for Cable side

Write register 0x0619 = 0x0557

Write register 0x0624 = 0x55BF

Check data for Cable side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continously check error status of incoming data stream.

Other system requirements

Data generate by the internal PRBS will be transmitted over the MDI and the MAC interface.

8.3.1.5.4 Digital Loopback

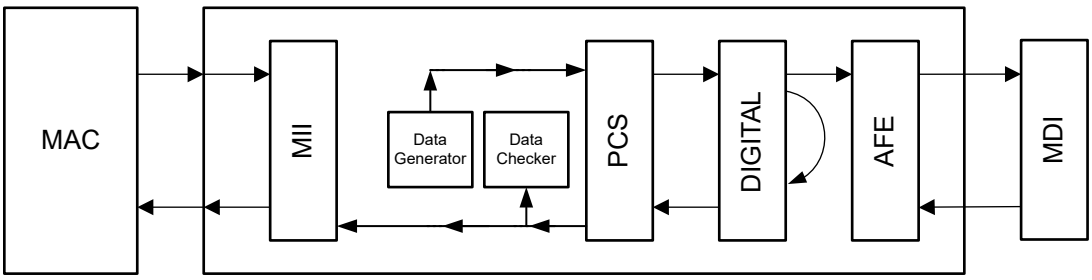

Figure 8-5. Digital loopback with data generator

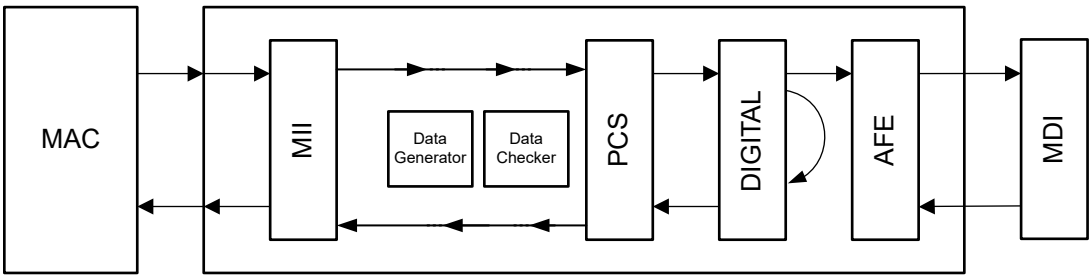

Figure 8-6. Digital loopback without data generator

Digital Loopback will loop back data prior to it exiting the Digital and entering the AFE. Data received from the MAC on the transmit path is brought through the digital block within the PHY where it is then routed back to the MAC through the receive path. The DP83TC812 receive Analog circuitry is configured for isolation to prevent contention.

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Enable Loopback

Write register 0x0016 = 0x0104

Enable data generator/checker for MAC side

Write register 0x0619 = 0x1555

Write register 0x0624 = 0x55BF

Check incoming data from MAC side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E

Enable data generator/checker for Cable side

Write register 0x0619 = 0x0557

Write register 0x0624 = 0x55BF

Check data for Cable side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continously check error status of incoming data stream.

Other system requirements

Data generate by the internal PRBS will be transmitted over the MDI and the MAC interface.

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8.3.1.5.5 Analog Loopback

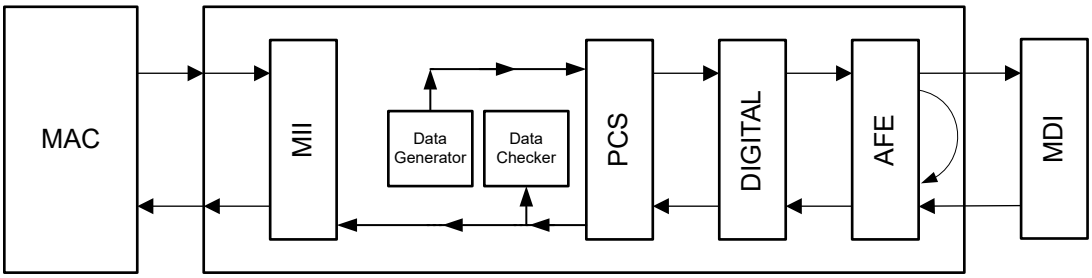

Figure 8-7. Analog loopback with data generator

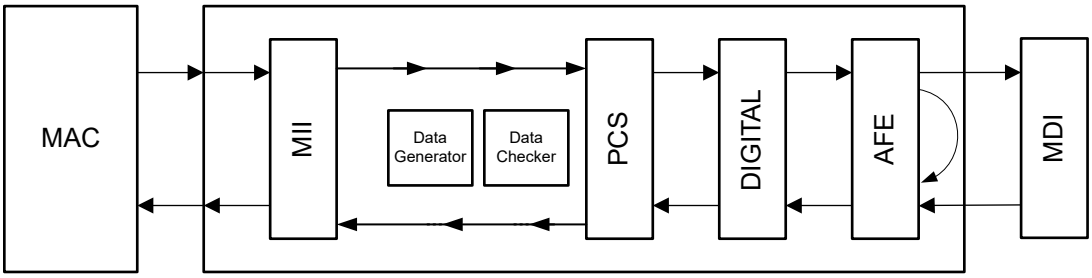

Figure 8-8. Analog loopback without data generator

Analog Loopback uses the echoed signals from the unterminated MDI and decodes these signals in the Hybrid to return the data to the MAC.

Enable Loopback

Write register 0x0016 = 0x0108

Enable data generator/checker for MAC side

Write register 0x0619 = 0x1555

Write register 0x0624 = 0x55BF

Check incoming data from MAC side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E

Enable data generator/checker for Cable side

Write register 0x0619 = 0x0557

Write register 0x0624 = 0x55BF

Check data for Cable side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continously check error status of incoming data stream.

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Other system requirements

Data generate by the internal PRBS will be transmitted over the MDI and the MAC interface.

8.3.1.5.6 Reverse Loopback

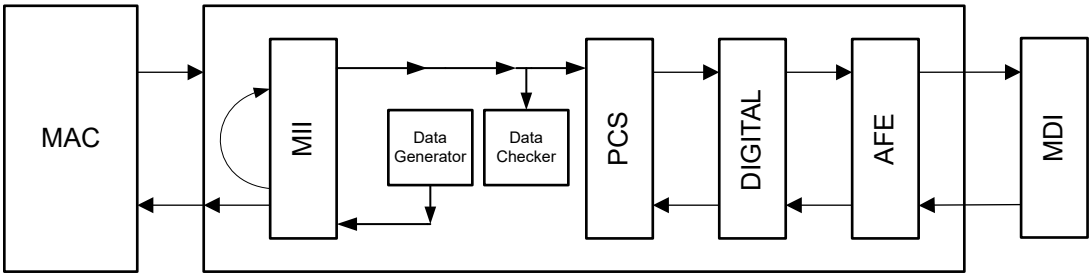

Figure 8-9. Reverse Loopback With Data Generator

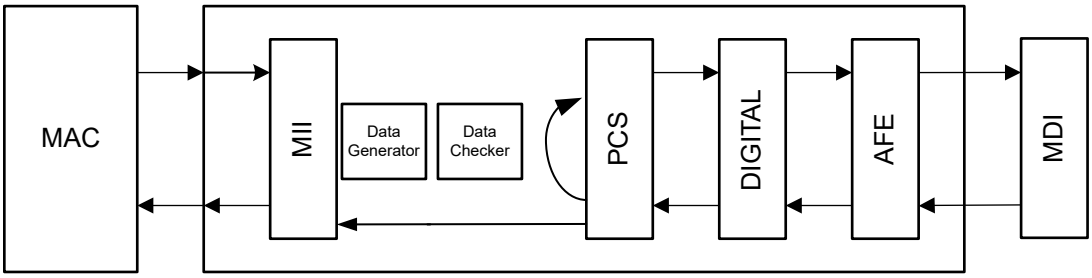

Figure 8-10. Reverse Loopback Without Data Generator

Reverse Loopback receives data on the MDI and passes it through the entire receive block where it is then looped back within the PCS layer to the transmit block. The data is transmitted back out on the MDI to the attached Link Partner. To avoid contention, MAC transmit path is isolated.

Enable Loopback

Write register 0x0016 = 0x0110

Enable data generator/checker for MAC side

Use the following register settings to enable checker depending on the MAC interface mode.

- For RGMII, write register 0x0619 = 0x1004
- For SGMII, write register 0x0619 = 0x1114
- For RMII, write register 0x0619 = 0x1224
- For MII, write register 0x0619 = 0x1334

Write register 0x0624 = 0x55BF

Check incoming data from MAC side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E

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Enable data generator/checker for Cable side

Write register 0x0619 = 0x0557

Write register 0x0624 = 0x55BF

Check data for Cable side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continously check error status of incoming data stream.

Other system requirements

Data generate by the internal PRBS will be transmitted over the MDI and the MAC interface.

8.3.2 Compliance Test Modes

Note

Refer to SNLA389 Application Note for more information about the register settings used for compliance testing. It is necessary to use these register settings to achieve the same performance as observed during compliance testing.

There are four PMA compliance test modes required in IEEE 802.3bw, sub-clause 96.5.2, which are all supported by the DP83TC812-Q1 . These compliance test modes include: transmitter waveform Power Spectral Density (PSD) mask, amplitude, distortion, 100BASE-T1 Master jitter, 100BASE-T1 Slave jitter, droop, transmitter frequency, frequency tolerance, return loss, and mode conversion.

Any of the three GPIOs can be used to output TX_TCLK for the 100BASE-T1 Slave jitter measurement. For routing TX_TCLK to CLKOUT pin for 100BASE-T1 Slave Jitter measurement, write to register 0x045F = 0x000D. The device must be configured in Slave mode.

8.3.2.1 Test Mode 1

Test mode 1 evaluates transmitter droop. In test mode 1, the DP83TC812-Q1 transmits '+1' symbols for a minimum of 600 ns followed by '–1' symbols for a minimum of 600 ns. This pattern is repeated continuously until the test mode is disabled.

Test mode 1 is enabled by setting bits[15:13] = 0b001 in the MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

8.3.2.2 Test Mode 2

Test mode 2 evaluates the transmitter 100BASE-T1 Master mode jitter. In test mode 2, the DP83TC812-Q1 transmits a {+1,-1} data symbol sequence. The transmitter synchronizes the transmitted symbols from the local reference clock.

Test mode 2 is enabled by setting bits[15:13] = 0b010 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

8.3.2.3 Test Mode 4

Test mode 4 evaluates the transmitter distortion. In test mode 4, the DP83TC812-Q1 transmits the sequence of symbols generated by Equation 1:

$$g(x) = 1 + x^9 + x^{11} \quad (1)$$

The bit sequences, x0n and x1n, are generated from combinations of the scrambler in accordance to Equation 2 and Equation 3:

$'x0_n = Scr_n[0]$ (2)

$x1_n = Scr_n[1] \wedge Scr_n[4]$ (3)

Example streams of the 3-bit nibbles are shown in Table 8-3.

Table 8-3. Transmitter Test Mode 4 Symbol Mapping

x1n	x0n	PAM3 SYMBOL
0	0	0
0	1	+1
1	0	0
1	1	–1

Test mode 4 is enabled by setting bits[15:13] = 0b100 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

8.3.2.4 Test Mode 5

Test mode 5 evaluates the transmitter PSD mask. In test mode 5, the DP83TC812-Q1 transmits a pseudo-random sequence of PAM3 symbols.

Test mode 5 is enabled by setting bits[15:13] = 0b101 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

8.4 Device Functional Modes

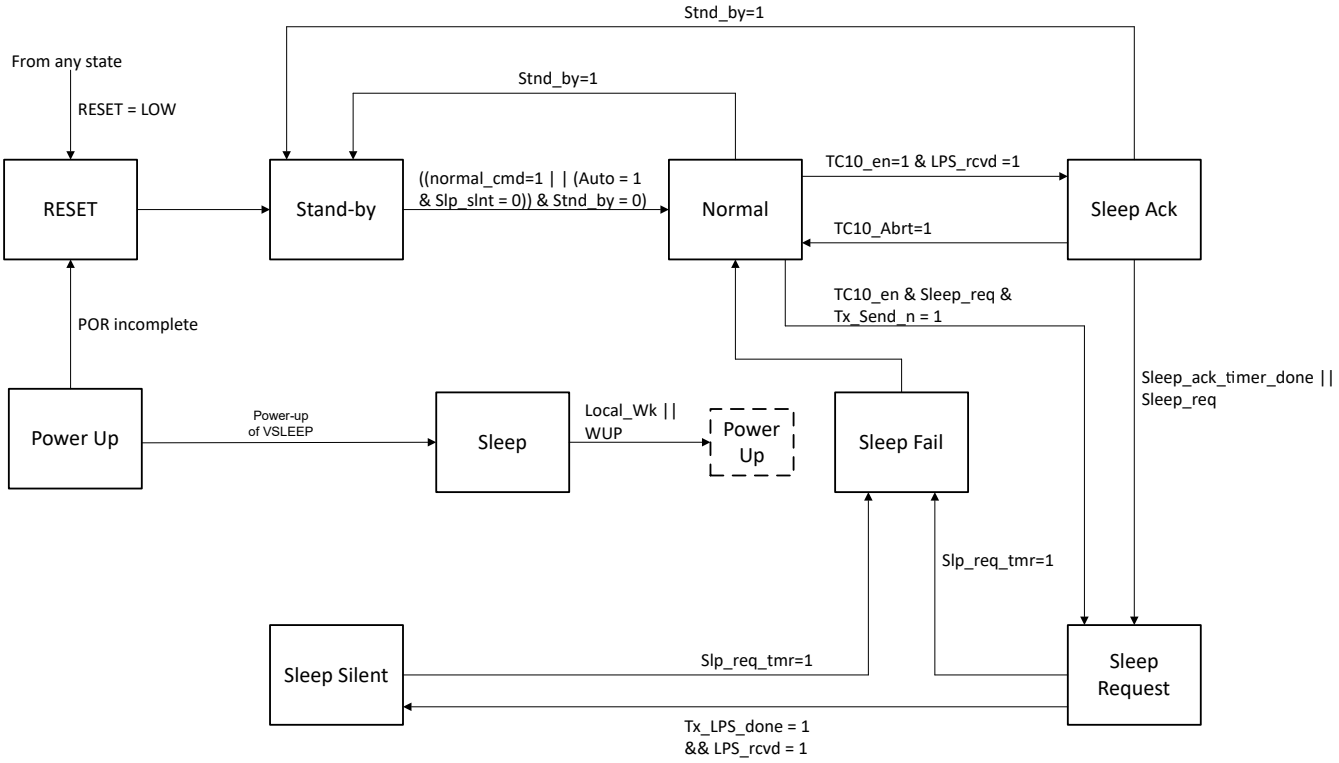

Figure 8-11. PHY Operation State Diagram

8.4.1 Power Down

When any of the supply rails are below the POR threshold (~0.6V), the PHY is in a power-down state. All digital IOs will remain in high impedance states and analog blocks are disabled. PMA termination is not present when powered down.

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8.4.2 Reset

Reset is activated upon power-up, when $\overline{\text{RESET}}$ is pulled LOW (for the minimum reset pulse time) or if hardware reset is initiated by setting bit[15] in register 0x1F. All digital circuitry is cleared along with register settings during reset. Once reset completes, device bootstraps are re-sampled and associated bootstrap registers are set accordingly. PMA termination is not present in reset.

8.4.3 Standby

The device (100BASE-T1 Master mode only) automatically enters into standby post power-up and reset so long that all supplies including VSLEEP are available and the device is bootstrapped for managed operation.

In standby, all PHY functions are operational except for PCS and PMA blocks. The PMA termination is also not present. Link establishment is not possible in standby and data cannot be transmitted or received. SMI functions are operational and register configurations are maintained.

If the device is configured for autonomous operation through bootstrap setting, the PHY automatically switches to normal operation once POR is complete.

8.4.4 Normal

Normal mode can be entered from either autonomous or managed operation. When in autonomous operation, the PHY will automatically try to establish a link with a valid Link Partner once POR is complete.

In managed operation, SMI access is required to allow the device to exit standby (100BASE-T1 Master mode only); commands issued through the SMI allow the device to exit standby and enables both the PCS and PMA blocks. All device features are operational in normal mode.

Autonomous operation can be enabled through SMI access by setting register 0x18B[6] = '1'. Note that this bit is auto-cleared after link up.

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8.4.5 Sleep Ack

When the PHY receives low power sleep requests from the link partner, it enter Sleep Ack mode. In this mode, the PHY allows 8ms for the MAC to decide if TC-10 sleep mode must be enabled or not. If the MAC decides to allow TC-10, the PHY proceeds to the next step in TC-10 state machine. However, the MAC can decide to abort TC-10 and the PHY returns to Normal mode. TC10 can be aborted via register setting by disabling TC10 or via GPIO. If TC10 is aborted by disabling TC10 feature, then it is recommended to re-enable TC10 feature once the sleep request has been aborted.

8.4.6 Sleep Request

Sleep request is entered when switching from normal mode to sleep mode. This is an intermediate state and is used to for a smooth transition into sleep mode. In sleep request mode, the PHY transmits LPS code-groups, informing the Link Partner that sleep is requested.

PHY sleep_rqst_timer (default = 16ms) begins once the PHY enters into sleep request mode. LPS decoding at the Link Partner will trigger the LPS RECEIVED interrupt. In sleep request state device waits for Link Partner to send LPS symbols. Once LPS symbols are received by the device, it transitions to SLEEP_SILENT state. If the sleep_rqst_timer expires before device receives LPS codes, the device enters SLEEP FAIL state. .

8.4.7 Sleep Fail

The PHY enters sleep fail mode if the Sleep_rqst_timer expires when in sleep_request state or sleep_silent state.. This indicates that the link partner has not entered sleep mode. After entering sleep fail mode, the PHY transitions to Normal mode.

8.4.8 Sleep

If sleep enable is set, the PHY transitions to sleep mode after the MDI line goes silent when in sleep_silent state; however, if sleep enable is not set, the device transitions to standby after the MDI line goes silent. By default, sleep enable is set. Once in sleep mode, all PHY blocks are disabled except for energy detection on the MDI. All register configurations are lost in sleep mode. No link can be established, data cannot be transmitted or received and SMI access is not available when in sleep mode.

Note

When the PHY is in Sleep mode, the MAC interface must not be driven by the Ethernet MAC.

8.4.9 Wake-Up

The user can wake up the DP83TC812S-Q1 remotely through energy detection on the MDI or locally using the WAKE pin. For local wake, the WAKE pin must be pulled HIGH. If the WAKE pin is tied LOW, the PHY will only exit sleep if energy is detected on the MDI.

8.4.10 TC10 System Example

The following block diagrams explains how TC10 sleep and wake function works in a system.

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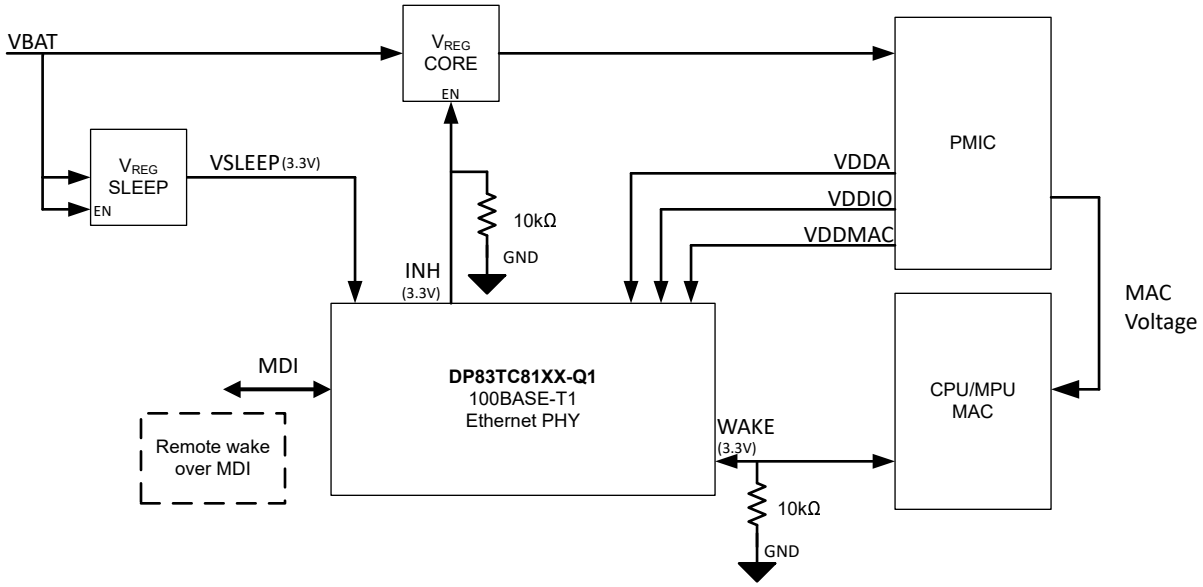

Figure 8-12. TC10 System Example - Remote Wake

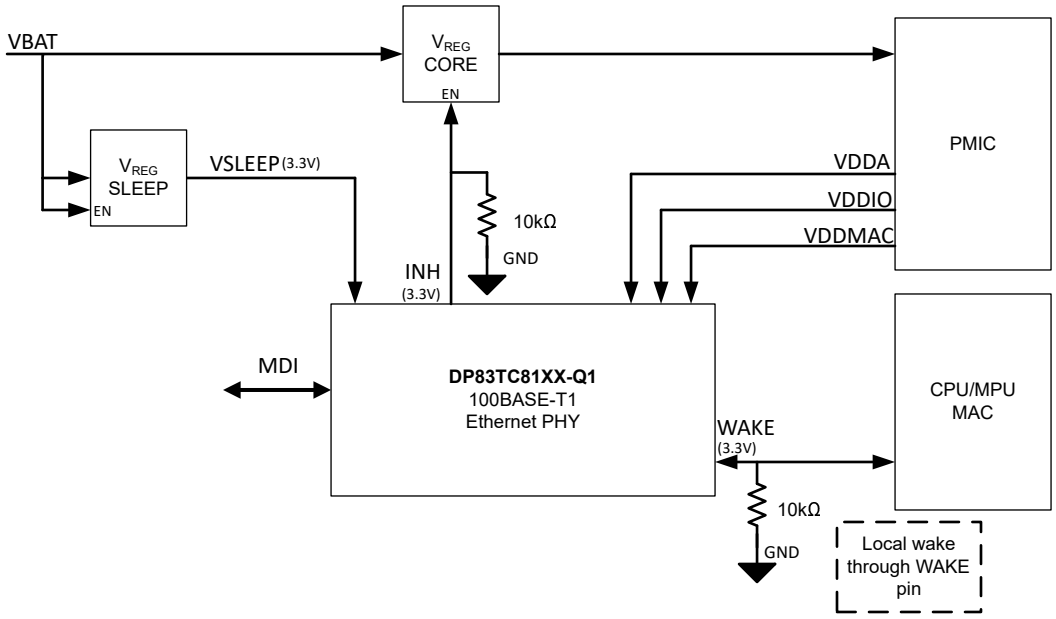

Figure 8-13. TC10 System Example - Local Wake

Remote Wake Up

For remote wake up, the initial state of the system is TC10 sleep. Core voltages to the PHY and MAC are turned off but the VSLEEP of the PHY is present. At some time, wake-up pulses (WUP) are received on the MDI lines. The PHY recevies the message and if its a valid sequence then the PHY wakes up and drives INH pin HIGH. INH pin is used as enable input to voltage regulator (e.g. LDO). Voltage regulators turns on and supplies power to a power management device. The power management device then supplies power to the PHY, MAC, and any other devices on the system. The whole system powers up and becomes operational.

Wake Forwarding

DP83TC812-Q1

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support wake forwarding feature. When the device received Wake-Up Requests (WUR) or Wake-Up Pulses (MDI) on the MDI then the PHY will transmit an 40µs high pulse on the WAKE pin. This can be used to wake-up any other PHYs on the system that are in TC-10 sleep.

Local Wake Up

For local wake, it is assumed that some portion of the system is already active and the PHY is in TC10 sleep. As a example, the system might have micro-controller in active mode to control the WAKE pin of the PHY. When the MCU wants to wake up the PHY from TC10 sleep, it raises the WAKE pin to 3.3V to send a wake pulse (min. 40µs). The PHY wakes up and drives INH pin HIGH. INH pin is used as enable input to voltage regulator (e.g. LDO). Voltage regulators turns on and supplies power to a power management device. The power management device then supplies power to the PHY. Any other device on the system that depends on the PHY wake up can now be powered up and the system becomes operational.

Local Sleep

When the PHY is in normal operational mode and the MAC needs to put it in TC10 sleep, it initiates the TC10 sleep process via SMI on the PHY. DP83TC812-Q1 then sends LPS signals on MDI to the link partner. If the link partner also agrees to enter TC10 sleep, the host PHY enters TC10 sleep. It then releases the INH pin and it gets pulled low through the external pull down resistor. Voltage regulator that uses INH pin as enable input will be turned off. PHY, MAC, and any other devices that are dependent on the voltage regulator will be turned off. The PHY will still have VSLEEP voltage present and continue to stay in TC10 sleep.

8.4.11 Media Dependent Interface

8.4.11.1 100BASE-T1 Master and 100BASE-T1 Slave Configuration

100BASE-T1 Master and 100BASE-T1 Slave are configured using either hardware bootstraps or through register access.

LED_0 controls the 100BASE-T1 Master and 100BASE-T1 Slave bootstrap configuration. By default, 100BASE-T1 Slave mode is configured because there is an internal pulldown resistor on LED_0 pin. If 100BASE-T1 Master mode configuration through hardware bootstrap is preferred, an external pullup resistor is required.

Additionally, bit[14] in the **MMD1_PMA_CTRL_2 Register (Address 0x1834)** controls the 100BASE-T1 Master and 100BASE-T1 Slave configuration. When this bit is set, 100BASE-T1 Master mode is enabled.

8.4.11.2 Auto-Polarity Detection and Correction

During the link training process, the DP83TC812-Q1 100BASE-T1 Slave device is able to detect polarity reversal and automatically corrects the error. If polarity reversal is detected, the 100BASE-T1 Slave will invert its own transmitted signals to account for the error and ensure compatibility with the 100BASE-T1 Master. Polarity at the 100BASE-T1 Master is always observed as correct because polarity detection and correction is handled entirely by the 100BASE-T1 Slave.

Auto-polarity correction may be disabled in cases where it is not required. Disabling of auto-polarity correction is achieved via register 0x0553.

8.4.11.3 Jabber Detection

The jabber function prevents the PCS Receive state machine from locking up into a DATA state if the End-of-Stream Delimiters, ESD1 and ESD2, are never detected or received within the rcv_max_timer. When the maximum receive DATA state timer expires, the PCS Receive state machine is reset and transitions into IDLE state. IEEE 802.3bw specifies that jabber timeout be set to 1.08 ms ± 54 µs. By default, jabber timeout in the DP83TC812 is set to 1.1 ms. This timer is configurable in *Register 0x496[10:0]*.

8.4.11.4 Interleave Detection

The interleave function allows for the DP83TC812-Q1 to detect and de-interleave the serial stream from a connected link partner. The two possible interleave sequences of ternary symbols include: (TA_n, TB_n) or (TB_n, TA_n).

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8.4.12 MAC Interfaces

8.4.12.1 Media Independent Interface

The Media Independent Interface (MII) is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC. The MII is fully compliant with IEEE 802.3-2015 clause 22. The PHY has internal series termination resistors on MII output pins including TX_CLK output when the PHY is operating in MII mode. In this mode, it is recommended to not leave the MII-TX pins floating or High-Z.

The MII signals are summarized in Table 8-4:

Table 8-4. MII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Control Signals	TX_EN, TX_ER
	RX_DV, RX_ER
Clock Signals	TX_CLK
	RX_CLK

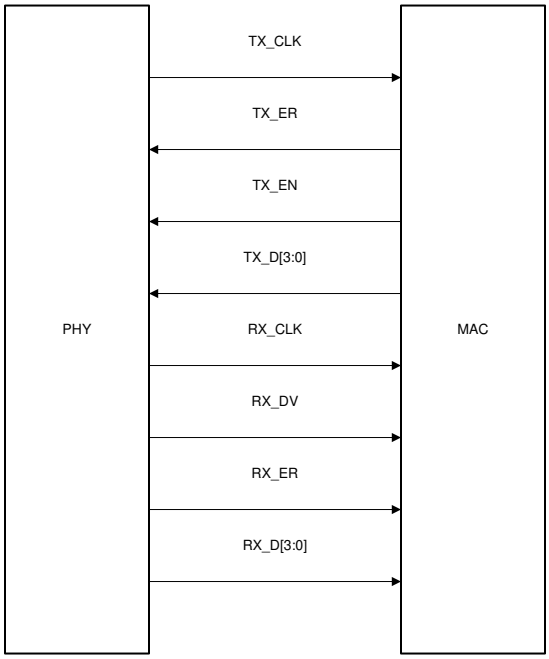

Figure 8-14. MII Signaling

Table 8-5. MII Transmit Encoding

TX_EN	TX_ER	TX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission
1	1	0000 through 1111	Transmit Error Propagation

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Table 8-6. MII Receive Encoding

RX_DV	RX_ER	RX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000	Normal Inter-Frame
0	1	0001 through 1101	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

8.4.12.2 Reduced Media Independent Interface

The DP83TC812-Q1 incorporates the Reduced Media Independent Interface (RMII) as defined in the RMII Revision 1.2 and 1.0 from the RMII consortium. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3u MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII.

The DP83TC812-Q1 offers two types of RMII operations: RMII Slave and RMII Master. In RMII Slave Mode, the DP83TC812-Q1 operates off a 50-MHz CMOS-level oscillator, which is either provided by the MAC or synchronous to the MAC's reference clock. In RMII Master operation, the DP83TC812-Q1 operates off of either a 25-MHz CMOS-level oscillator connected to XI pin or a 25-MHz crystal connected across XI and XO pins. When bootstrapping to RMII Master Mode, a 50-MHz output clock will automatically be enabled on RX_D3. This 50-MHz output clock must be routed to the MAC.

The RMII specification has the following characteristics:

- Single clock reference shared between MAC and PHY
- Provides independent 2-bit wide transmit and receive data paths

In this mode, data transfers are two bits for every clock cycle using the 50-MHz reference clock for both transmit and receive paths.

The RMII signals are summarized in Table 8-7:

Table 8-7. RMII Signals

FUNCTION	PINS
Data Signals	TX_D[1:0]
	RX_D[1:0]
Control Signals	TX_EN
	CRS_DV

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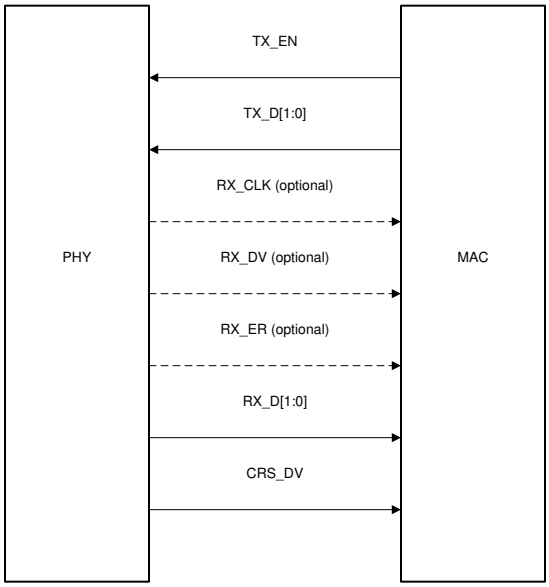

Figure 8-15. RMII Signaling

Table 8-8. RMII Transmit Encoding

TX_EN	TX_D[1:0]	DESCRIPTION
0	00 through 11	Normal Inter-Frame
1	00 through 11	Normal Data Transmission

Table 8-9. RMII Receive Encoding

CRS_DV	RX_ER	RX_D[1:0]	DESCRIPTION
0	0	00 through 11	Normal Inter-Frame
0	1	00	Normal Inter-Frame
0	1	01 through 11	Reserved
1	0	00 through 11	Normal Data Reception
1	1	00 through 11	Data Reception with Errors

RMII Slave: Data on TX_D[1:0] are latched at the PHY with reference to the rising edge of the reference clock at the XI pin. Data is presented on RX_D[1:0] with reference to the same rising clock edges at the XI pin.

RMII Master: Data on TX_D[1:0] are latched at the PHY with reference to the rising edge of the reference clock at the RX_D3 pin. Data is presented on RX_D[1:0] with reference to the same rising clock edges at the RX_D3 pin.

The DP83TC812-Q1 RMII supplies an RX_DV signal, which provides a simpler method to recover receive data without the need to separate RX_DV from the CRS_DV indication. RX_ER is also supported even though it is not required by the RMII specification.

RMII includes a programmable FIFO to adjust for the frequency differences between the reference clock and the recovered clock. The programmable FIFO, located in the register 0x0011[9:8] and register 0x0648[9:7], minimizes internal propagation delay based on expected maximum packet size and clock accuracy.

Table 8-10. XI clock's PPM = +/- 100ppm

Reg 0x0011 <9:8>	Reg 0x0648 <9:7>	Increment PHY latency	Max packet length without errors
01	010	Default	2250
10	100	80 ns	7250

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8.4.12.3 Reduced Gigabit Media Independent Interface

The DP83TC812-Q1 also supports Reduced Gigabit Media Independent Interface (RGMII) as specified by RGMII version 2.0 with LVCMOS. RGMII is designed to reduce the number of pins required to connect MAC and PHY. To accomplish this goal, the control signals are multiplexed. Both rising and falling edges of the clock are used to sample the control signal pin on transmit and receive paths. Data is samples on just the rising edge of the clock. For 100-Mbps operation, RX_CLK and TX_CLK operate at 25 MHz.

The RGMII signals are summarized in Table 8-11:

Table 8-11. RGMII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Control Signals	TX_CTRL
	RX_CTRL
Clock Signals	TX_CLK
	RX_CLK

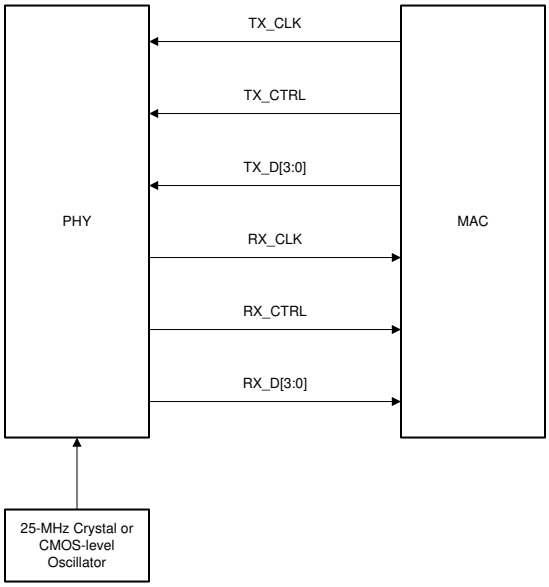

Figure 8-16. RGMII Connections

Table 8-12. RGMII Transmit Encoding

TX_CTRL (POSITIVE EDGE)	TX_CTRL (NEGATIVE EDGE)	TX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission
1	1	0000 through 1111	Transmit Error Propagation

Table 8-13. RGMII Receive Encoding

RX_CTRL (POSITIVE EDGE)	RX_CTRL (NEGATIVE EDGE)	RX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1101	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved

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Table 8-13. RGMII Receive Encoding (continued)

RX_CTRL (POSITIVE EDGE)	RX_CTRL (NEGATIVE EDGE)	RX_D[3:0]	DESCRIPTION
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

During packet reception, RX_CLK may be stretched on either the positive or negative pulse to accommodate the transition from the internal free running clock to a recovered clock (data synchronous). Data may be duplicated on the falling edge of the clock because double data rate (DDR) is only required for 1-Gbps operation, which is not supported by the DP83TC812-Q1.

The DP83TC812-Q1 supports in-band status indication to help simplify link status detection. Inter-frame signals on RX_D[3:0] pins as specified in Table 8-14.

Table 8-14. RGMII In-Band Status

RX_CTRL	RX_D3	RX_D[2:1]	RX_D0
00 **Note:** In-band status is only valid when RX_CTRL is low	**Duplex Status:** 0 = Half-Duplex 1 = Full-Duplex	**RX_CLK Clock Speed:** 00 = 2.5 MHz 01 = 25 MHz 10 = 125 MHz 11 = Reserved	**Link Status:** 0 = Link not established 1 = Valid link established

8.4.12.4 Serial Gigabit Media Independent Interface

The Serial Gigabit Media Independent Interface (SGMII) provides a means for data transfer between MAC and PHY with significantly less signal pins (4 pins) compared to MII (14 pins), RMII (7 pins) or RGMII (12 pins). SGMII uses low-voltage differential signaling (LVDS) to reduce emissions and improve signal quality.

The DP83TC812 SGMII is capable of operating in 4-wire. SGMII is configurable through hardware bootstraps. In 4-wire operation, two differential pairs are used to transmit and receive data. Clock and data recovery are performed in the MAC and in the PHY.

Because the DP83TC812 operates at 100-Mbps, the 1.25-Gbps rate of the SGMII is excessive. The SGMII specification allows for 100-Mbps operation by replicating each byte within a frame 10 times. Frame elongation takes place above the IEEE 802.3 PCS layer, which prevents the start-of-frame delimiter from appearing more than once.

Because the DP83TC812 only supports 100-Mbps speed, SGMII Auto-Negotitation can be disabled by setting bit[0] = 0b0 in the *Register 0x608*.

The SGMII signals are summarized in Table 8-15.

Table 8-15. SGMII Signals

FUNCTION	PINS
Data Signals	TX_M, TX_P
	RX_M, RX_P

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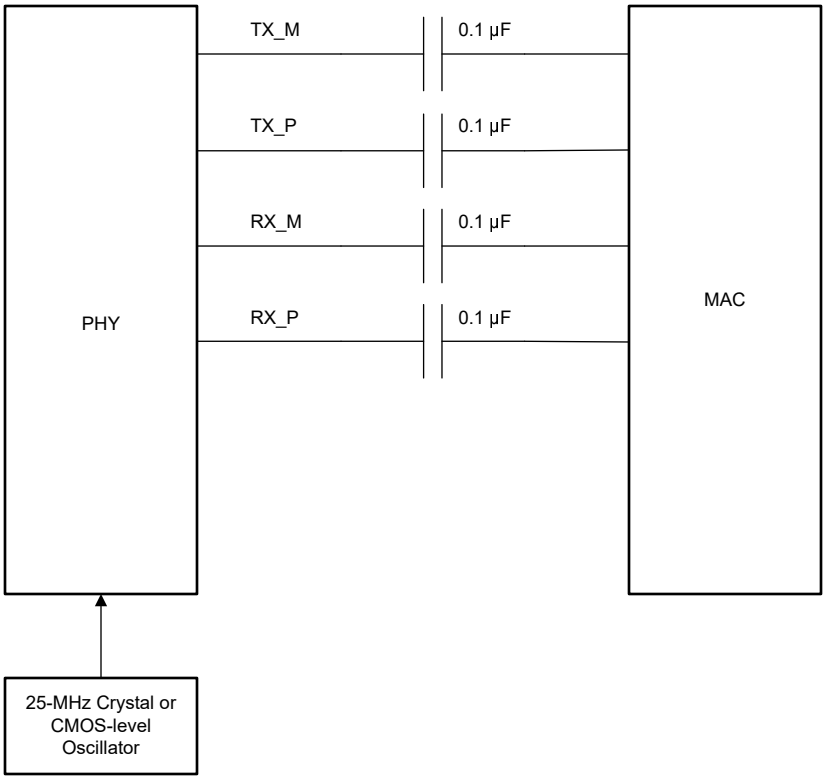

Figure 8-17. SGMII Connections

8.4.13 Serial Management Interface

The Serial Management Interface (SMI) provides access to the DP83TC812S-Q1 internal register space for status information and configuration. The SMI frames and base registers are compatible with IEEE 802.3 clause 22. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83TC812S-Q1 . Additionally, the DP83TC812S-Q1 includes control and status registers added to clause 45 as defined by IEEE 802.3bw. Access to clause 45 register field is achieved using clause 22 access.

The SMI includes the management clock (MDC) and the management input and output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 24 MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2 KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 9 DP83TC812S-Q1 PHYs can share a common SMI bus. To distinguish between the PHYs, a 4-bit address is used. During power-up-reset, the DP83TC812S-Q1 latches the PHYAD[3:0] configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power-up-reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed

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DP83TC812S-Q1 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83TC812S-Q1 , thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

Table 8-16. SMI Protocol Structure

SMI PROTOCOL	<idle> <start> <op code> <device address> <reg address> <turnaround> <data> <idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

8.4.14 Direct Register Access

Direct register access can be used for the first 31 registers (0x0 through 0x1F).

8.4.15 Extended Register Space Access

The DP83TC812S-Q1 SMI function supports read and write access to the extended register set using registers REGCR (0xD) and ADDAR (0xE) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for Clause 22 for accessing the Clause 45 extended register set.

REGCR (0xD) is the MDIO Manageable MMD access control. In general, register REGCR[4:0] is the device address DEVAD that directs any accesses of ADDAR (0xE) register to the appropriate MMD.

The DP83TC812S-Q1 supports 3 MMD device addresses:

1. DEVAD[4:0] = 11111 is used for general MMD register accesses for IEEE defined registers as well as vendor defined registers.
2. DEVAD[4:0] = 00001 is used for 100BASE-T1 PMA MMD register accesses. Register names for registers accessible at this device address are preceded by MMD1.
3. DEVAD[4:0] = 00011 is used for vendor specific registers. This registers space is called MMD3.

All accesses through register REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVADs are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address and data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is (00), then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to (00), accesses to register ADDAR modify the extended register set address register. This address register must always be initialized to access any of the registers within the extended register set.
- When REGCR[15:14] is set to (01), accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to (10), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to (11), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write access only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR.

8.4.16 Write Address Operation

To set the address register:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the register address to register ADDAR.

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Subsequent writes to register ADDAR (step 2) continue to write the address register.

8.4.16.1 MMD1 - Write Address Operation

For writing register addresses within MMD1 field:
1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the register address to register ADDAR.

8.4.17 Read Address Operation

To read the address register:
1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

8.4.17.1 MMD1 - Read Address Operation

For reading register addresses within MMD1 field:
1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Read the register address from register ADDAR.

8.4.18 Write Operation (No Post Increment)

To write a register in the extended register set:
1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = '11111') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

8.4.18.1 MMD1 - Write Operation (No Post Increment)

To write a register in the MMD1 extended register set:
1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x4001 (data, no post increment function field = 01, DEVAD = '00001') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

8.4.19 Read Operation (No Post Increment)

To read a register in the extended register set:
1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = '11111') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) continue to reading the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

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8.4.19.1 MMD1 - Read Operation (No Post Increment)

To read a register in the MMD1 extended register set:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x4001 (data, no post increment function field = 01, DEVAD = '00001') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

8.4.20 Write Operation (Post Increment)

To write a register in the extended register set with post increment:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = '11111') or the value 0xC01F (data, post increment on writes function field = 11, DEVAD = '11111') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

8.4.20.1 MMD1 - Write Operation (Post Increment)

To write a register in the MMD1 extended register set with post increment:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x8001 (data, post increment function field = 10, DEVAD = '00001') or the value 0xC001 (data, post increment on writes function field = 11, DEVAD = '00001') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

8.4.21 Read Operation (Post Increment)

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = '11111') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

8.4.21.1 MMD1 - Read Operation (Post Increment)

To read a register in the MMD1 extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x8001 (data, post increment function field = 10, DEVAD = '00001') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

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8.5 Programming

8.5.1 Strap Configuration

The DP83TC812S-Q1 uses functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up and hardware reset (through either the $\overline{\text{RESET}}$ pin or register access). Some strap pins support 3 levels and some strap pins support 2 levels, which are described in greater detail below. PHY address straps, RX_DV/RX_CTRL and RX_ER, are 3-level straps while all other straps are two levels. Configuration of the device may be done through strapping or through serial management interface.

Note

Because strap pins are functional pins after reset is deasserted, they must not be connected directly to VDDIO or VDDMAC or GND. Either pullup resistors, pulldown resistors, or both are required for proper operation.

Note

When using VDDMAC and VDDIO separately, it is important to connect strap resistors to the correct voltage rail. Each pin's voltage domain is listed in the Table 8-19 table below.

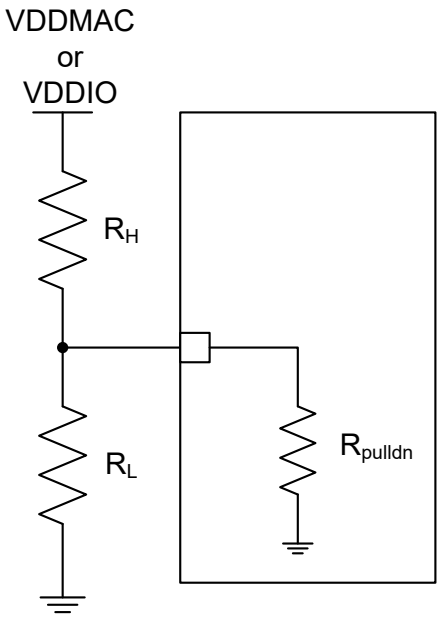

Figure 8-18. Strap Circuit

R_{pulldn} value is included in the Electrical Characteristics table of the data sheet.

Table 8-17. Recommended 3-Level Strap Resistor Ratios for PHY Address

MODE[3]	IDEAL RH (kΩ) (VDDIO = 3.3V)[1]	IDEAL RH (kΩ) (VDDIO = 2.5V)[2]	IDEAL RH (kΩ) (VDDIO = 1.8V)[1]
1	OPEN	OPEN	OPEN
2	13	12	4
3	4.5	2	0.8

1. Strap resistors with 10% tolerance.
2. Strap resistors with 1% tolerance.
3. RL is optional and can be added if voltage on bootstrap pins needs to be adjusted.

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Table 8-18. Recommended 2-Level Strap Resistors

MODE	IDEAL RH (kΩ) [1, 2]
1	OPEN
2	2.49

1. Strap resistors with up to 10% tolerance can be used.
2. To gain more margin in customer application for 1.8V VDDIO, either 2.1 kΩ +/-10% pull-up can be used or resistor accuracy of 2.49 kΩ resistor can be limited to 1%.

The following table describes the PHY configuration bootstraps:

Table 8-19. Bootstraps

PIN NAME	PIN NO.	DOMAIN	DEFAULT MODE	STRAP FUNCTION			DESCRIPTION
RX_DV/ RX_CTRL	15	VDDMAC	1	**MODE**	**PHY_AD[0]**	**PHY_AD[2]**	PHY_AD: PHY Address ID
				1	0	0	
				2	0	1	
				3	1	1	
RX_ER	14	VDDMAC	1	**MODE**	**PHY_AD[1]**	**PHY_AD[3]**	PHY_AD: PHY Address ID
				1	0	0	
				2	0	1	
				3	1	1	
CLKOUT	16	VDDMAC	1	**MODE**	**$\overline{\text{AUTO}}$**		$\overline{\text{AUTO}}$: Autonomous Disable. This is a duplicate strap for LED_1. If CLKOUT pin is configured as LED_1 pin then the $\overline{\text{AUTO}}$strap functionality also moves to the CLKOUT pin.
				1	0		
				2	1		
RX_D0	26	VDDMAC	1	**MODE**	**MAC[0]**		MAC: MAC Interface Selection
				1	0		
				2	1		
RX_D1	25	VDDMAC	1	**MODE**	**MAC[1]**		MAC: MAC Interface Selection
				1	0		
				2	1		
RX_D2	24	VDDMAC	1	**MODE**	**MAC[2]**		MAC: MAC Interface Selection
				1	0		
				2	1		
RX_D3	23	VDDMAC	1	**MODE**	**CLKOUT_PIN**		CLKOUT_PIN: This strap determines which pin will be used for output clock.
				1	0		
				2	1		
LED_0	35	VDDIO	1	**MODE**	**MS**		MS: 100BASE-T1 Master & 100BASE-T1 Slave Selection
				1	0		
				2	1		
LED_1	6	VDDIO	1	**MODE**	**$\overline{\text{AUTO}}$**		$\overline{\text{AUTO}}$: Autonomous Disable This is the default strap pin for controlling $\overline{\text{AUTO}}$ feature. If this pin is configured as CLKOUT, the $\overline{\text{AUTO}}$ feature will move to pin 16.
				1	0		
				2	1		

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Note

Refer to SNLA389 Application Note for more information about the register settings used for compliance testing. It is necessary to use these register settings to achieve the same performance as observed during compliance testing. Managed mode strap option is recommended to prevent the link up process from initiating while the software configuration from SNLA389 is being executed. Once the software configuration is completed, the PHY can be removed from Managed mode by setting bit 0x018B[6] to '1'. This bit is auto-cleared after link up

RX_D3 strap pin has a special functionality of controlling the output status of CLKOUT (pin 16) and LED_1 (pin 6). The Table 8-20 table below shows how pin 16 and pin 6 will be affected by RX_D3 strap status. Note that RX_D3 option only changes the pin functionality but not their voltage domains. Pin 16 will always be in VDDMAC domain and Pin 6 will always be in VDDIO domain. If VDDIO and VDDMAC are at separate voltage levels, it must be ensured that pin 16 and pin 6 are strapped to their respective voltage domains.

In clock output daisy chain applications, if VDDMAC and VDDIO are at different voltages then clock output must be routed to pin 6. Internal oscillator of the DP83TC812 operates in the VDDIO domain, so clock ouput must also be used on the pin in VDDIO domain i.e. pin 6. In clock output daisy chain applications where VDDMAC and VDDIO are same, this requirement can be ignored. This requirement can also be ignored in applications where clock output is not being used.

Table 8-20. Clock Output Pin Selection

CLKOUT_PIN	DESCRIPTION
0	Pin 16 is Clock output, Pin 6 is LED_1 pin. $\overline{\text{AUTO}}$ will be controlled by straps on pin 6.
1	Pin 6 is Clock output, Pin 16 is LED_1 pin. $\overline{\text{AUTO}}$ will be controlled by straps on pin 16.

Table 8-21. 100BASE-T1 Master and 100BASE-T1 Slave Selection Bootstrap

MS	DESCRIPTION
0	100BASE-T1 Slave Configuration
1	100BASE-T1 Master Configuration

Table 8-22. Autonomous Mode Bootstrap

$\overline{\text{AUTO}}$	DESCRIPTION
0	Autonomous Mode, PHY able to establish link after power-up
1	Managed Mode, PHY must be allowed to establish link after power-up based on register write

Table 8-23. MAC Interface Selection Bootstraps

MAC[2]	MAC[1]	MAC[0]	DESCRIPTION
0	0	0	SGMII (4-wire)(1)
0	0	1	MII
0	1	0	RMII Slave
0	1	1	RMII Master
1	0	0	RGMII (Align Mode)
1	0	1	RGMII (TX Internal Delay Mode)
1	1	0	RGMII (TX and RX Internal Delay Mode)
1	1	1	RGMII (RX Internal Delay Mode)

(1) SGMII strap mode is only available on 'S' type device variant. For 'R' type device variant, this strap mode is RESERVED

Table 8-24. PHY Address Bootstraps

PHY_AD[3:0]	RX_CTRL STRAP MODE	RX_ER STRAP MODE	DESCRIPTION Section 8.5.1
0000	1	1	PHY Address: 0b00000 (0x0)
0001	-	-	NA
0010	-	-	NA

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Table 8-24. PHY Address Bootstraps (continued)

PHY_AD[3:0]	RX_CTRL STRAP MODE	RX_ER STRAP MODE	DESCRIPTION Section 8.5.1
0011	-	-	NA
0100	2	1	PHY Address: 0b00100 (0x4)
0101	3	1	PHY Address: 0b00101 (0x5)
0110	-	-	NA
0111	-	-	NA
1000	1	2	PHY Address: 0b01000 (0x8)
1001	-	-	NA
1010	1	3	PHY Address: 0b01010 (0xA)
1011	-	-	NA
1100	2	2	PHY Address: 0b01010 (0xC)
1101	3	2	PHY Address: 0b01011 (0xD)
1110	2	3	PHY Address: 0b01110 (0xE)
1111	3	3	PHY Address: 0b01111 (0xF)

8.5.2 LED Configuration

The DP83TC812S-Q1 supports up to three configurable Light Emitting Diode (LED) pins: LED_0, LED_1, and LED_2 (CLKOUT). Several functions can be multiplexed onto the LEDs for different modes of operation. LED operations are selected using registers 0x0450.

Because the LED output pins are also used as strap pins, external components required for strapping and the user must consider the LED usage to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding input upon power up or hardware reset.

Figure 8-19 shows the two proper ways of connecting LEDs directly to the DP83TC812S-Q1 .

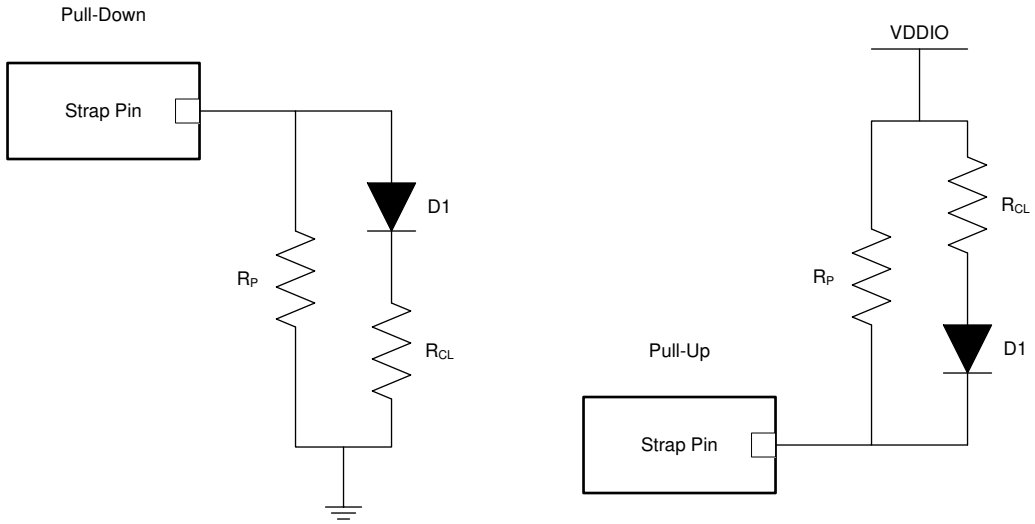

Figure 8-19. Example Strap Connections

8.5.3 PHY Address Configuration

The DP83TC812S-Q1 can be set to respond to any of 9 possible PHY addresses through bootstrap pins. The PHY address is latched into the device upon power-up or hardware reset. Each PHY on the serial management bus in the system must have a unique PHY address.

By default, DP83TC812S-Q1 will latch to a PHY address of 0 (<0b00000>). This address can be changed by adding pullup resistors to bootstrap pins found in Section 8.5.3.

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8.6 Register Maps

8.6.1 Register Access Summary

There are two different methods for accessing registers within the field. Direct register access method is only allowed for the first 31 registers (0x0 through 0x1F). Registers beyond 0x1F must be accessed by use of the Indirect Method (Extended Register Space) described in *Section 8.4.15*.

Table 8-25. MMD Register Space Division

MMD REGISTER SPACE	REGISTER ADDRESS RANGE
MMD1F	0x0000 - 0x0EFD
MMD1	0x1000 - 0x1836
MMD3	0x3000 - 0x3001

Note

For MMD1 and MMD3, the most significant nibble of the register address is used to denote the respective MMD space. This nibble must be ignored during actual register access operation. For example, to access register 0x1836, use 0x1 as the MMD indicator and 0x0836 as the register address.

Table 8-26. Register Access Summary

REGISTER FIELD	REGISTER ACCESS METHODS
0x0 through 0x1F	Direct Access
	Indirect Access, MMD1F = '11111' **Example:** to read register 0x17 in MMD1F field with no post increment Step 1) write 0x1F to register 0xD Step 2) write 0x17 to register 0xE Step 3) write 0x401F to register 0xD Step 4) read register 0xE
MMD1F Field 0x20 - 0xFFF	Indirect Access, MMD1F = '11111' **Example:** to read register 0x462 in MMD1F field with no post increment Step 1) write 0x1F to register 0xD Step 2) write 0x462 to register 0xE Step 3) write 0x401F to register 0xD Step 4) read register 0xE
MMD1 Field 0x0 - 0xFFF	Indirect Access, MMD1 = '00001' **Example:** to read register 0x7 in MMD1 field (register 0x1007) with no post increment Step 1) write 0x1 to register 0xD Step 2) write 0x7 to register 0xE Step 3) write 0x4001 to register 0xD Step 4) read register 0xE

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8.6.2 DP83TC812 Registers

Table 8-27 lists the memory-mapped registers for the DP83TC812 registers. All register offset addresses not listed in Table 8-27 should be considered as reserved locations and the register contents should not be modified.

Table 8-27. DP83TC812 Registers

Address	Acronym	Register Name	Section
0h	BMCR		Section 8.6.2.1
1h	BMSR		Section 8.6.2.2
2h	PHYIDR1		Section 8.6.2.3
3h	PHYIDR2		Section 8.6.2.4
10h	PHYSTS		Section 8.6.2.5
11h	PHYSCR		Section 8.6.2.6
12h	MISR1		Section 8.6.2.7
13h	MISR2		Section 8.6.2.8
15h	RECR		Section 8.6.2.9
16h	BISCR		Section 8.6.2.10
18h	MISR3		Section 8.6.2.11
19h	REG_19		Section 8.6.2.12
1Bh	TC10_ABORT_REG		Section 8.6.2.13
1Eh	CDCR		Section 8.6.2.14
1Fh	PHYRCR		Section 8.6.2.15
41h	Register_41		Section 8.6.2.16
133h	Register_133		Section 8.6.2.17
17Fh	Register_17F		Section 8.6.2.18
180h	Register_180		Section 8.6.2.19
181h	Register_181		Section 8.6.2.20
182h	Register_182		Section 8.6.2.21
183h	LPS_CFG4		Section 8.6.2.22
184h	LPS_CFG		Section 8.6.2.23
185h	LPS_CFG5		Section 8.6.2.24
187h	LPS_CFG7		Section 8.6.2.25
188h	LPS_CFG8		Section 8.6.2.26
189h	LPS_CFG9		Section 8.6.2.27
18Ah	LPS_CFG10		Section 8.6.2.28
18Bh	LPS_CFG2		Section 8.6.2.29
18Ch	LPS_CFG3		Section 8.6.2.30
18Eh	LPS_STATUS		Section 8.6.2.31
300h	TDR_TX_CFG		Section 8.6.2.32
301h	TAP_PROCESS_CFG		Section 8.6.2.33
302h	TDR_CFG1		Section 8.6.2.34
303h	TDR_CFG2		Section 8.6.2.35
304h	TDR_CFG3		Section 8.6.2.36
305h	TDR_CFG4		Section 8.6.2.37
306h	TDR_CFG5		Section 8.6.2.38
310h	TDR_TC1		Section 8.6.2.39
430h	A2D_REG_48		Section 8.6.2.40
444h	A2D_REG_68		Section 8.6.2.41
450h	LEDS_CFG_1		Section 8.6.2.42

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Table 8-27. DP83TC812 Registers (continued)

Address	Acronym	Register Name	Section
451h	LEDS_CFG_2		Section 8.6.2.43
452h	IO_MUX_CFG_1		Section 8.6.2.44
453h	IO_MUX_CFG_2		Section 8.6.2.45
456h	IO_MUX_CFG		Section 8.6.2.46
457h	IO_STATUS_1		Section 8.6.2.47
458h	IO_STATUS_2		Section 8.6.2.48
45Dh	CHIP_SOR_1		Section 8.6.2.49
45Fh	LED1_CLKOUT_ANA_CTRL		Section 8.6.2.50
485h	PCS_CTRL_1		Section 8.6.2.51
486h	PCS_CTRL_2		Section 8.6.2.52
489h	TX_INTER_CFG		Section 8.6.2.53
496h	JABBER_CFG		Section 8.6.2.54
497h	TEST_MODE_CTRL		Section 8.6.2.55
4A0h	RXF_CFG		Section 8.6.2.56
553h	PG_REG_4		Section 8.6.2.57
560h	TC1_CFG_RW		Section 8.6.2.58
561h	TC1_LINK_FAIL_LOSS		Section 8.6.2.59
562h	TC1_LINK_TRAINING_TIME		Section 8.6.2.60
600h	RGMII_CTRL		Section 8.6.2.61
601h	RGMII_FIFO_STATUS		Section 8.6.2.62
602h	RGMII_CLK_SHIFT_CTRL		Section 8.6.2.63
603h	RGMII_EEE_CTRL		Section 8.6.2.64
608h	SGMII_CTRL_1		Section 8.6.2.65
609h	SGMII_EEE_CTRL_1		Section 8.6.2.66
60Ah	SGMII_STATUS		Section 8.6.2.67
60Bh	SGMII_EEE_CTRL_2		Section 8.6.2.68
60Ch	SGMII_CTRL_2		Section 8.6.2.69
60Dh	SGMII_FIFO_STATUS		Section 8.6.2.70
618h	PRBS_STATUS_1		Section 8.6.2.71
619h	PRBS_CTRL_1		Section 8.6.2.72
61Ah	PRBS_CTRL_2		Section 8.6.2.73
61Bh	PRBS_CTRL_3		Section 8.6.2.74
61Ch	PRBS_STATUS_2		Section 8.6.2.75
61Dh	PRBS_STATUS_3		Section 8.6.2.76
61Eh	PRBS_STATUS_4		Section 8.6.2.77
620h	PRBS_STATUS_5		Section 8.6.2.78
622h	PRBS_STATUS_6		Section 8.6.2.79
623h	PRBS_STATUS_7		Section 8.6.2.80
624h	PRBS_CTRL_4		Section 8.6.2.81
625h	PATTERN_CTRL_1		Section 8.6.2.82
626h	PATTERN_CTRL_2		Section 8.6.2.83
627h	PATTERN_CTRL_3		Section 8.6.2.84
628h	PMATCH_CTRL_1		Section 8.6.2.85
629h	PMATCH_CTRL_2		Section 8.6.2.86
62Ah	PMATCH_CTRL_3		Section 8.6.2.87

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Table 8-27. DP83TC812 Registers (continued)

Address	Acronym	Register Name	Section
639h	TX_PKT_CNT_1		Section 8.6.2.88
63Ah	TX_PKT_CNT_2		Section 8.6.2.89
63Bh	TX_PKT_CNT_3		Section 8.6.2.90
63Ch	RX_PKT_CNT_1		Section 8.6.2.91
63Dh	RX_PKT_CNT_2		Section 8.6.2.92
63Eh	RX_PKT_CNT_3		Section 8.6.2.93
648h	RMII_CTRL_1		Section 8.6.2.94
649h	RMII_STATUS_1		Section 8.6.2.95
64Ah	RMII_OVERRIDE_CTRL		Section 8.6.2.96
871h	dsp_reg_71		Section 8.6.2.97
1000h	MMD1_PMA_CTRL_1		Section 8.6.2.98
1001h	MMD1_PMA_STATUS_1		Section 8.6.2.99
1007h	MMD1_PMA_STAUS_2		Section 8.6.2.100
100Bh	MMD1_PMA_EXT_ABILITY_1		Section 8.6.2.101
1012h	MMD1_PMA_EXT_ABILITY_2		Section 8.6.2.102
1834h	MMD1_PMA_CTRL_2		Section 8.6.2.103
1836h	MMD1_PMA_TEST_MODE_CTRL		Section 8.6.2.104
3000h	MMD3_PCS_CTRL_1		Section 8.6.2.105
3001h	MMD3_PCS_Status_1		Section 8.6.2.106

Complex bit access types are encoded to fit into small table cells. Table 8-28 shows the codes that are used for access types in this section.

Table 8-28. DP83TC812 Access Type Codes

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W0S	W 0S	Write 0 to set
W1S	W 1S	Write 1 to set
WSC	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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8.6.2.1 BMCR Register (Address = 0h) [Reset = 2100h]

BMCR is shown in Figure 8-20 and described in Table 8-29.

Return to the Table 8-27.

Figure 8-20. BMCR Register

15	14	13	12	11	10	9	8
MII_reset	xMII Loopback	Manual_speed_MII	Auto-Negotiation Enable	Power Down	Isolate	RESERVED	Duplex Mode
RH/W1S-0b	R/W-0b	R-1b	R-0b	R/W-0b	R/W-0b	R-0b	R-1b
7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R/W-0b	R-0b						

Table 8-29. BMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	MII_reset	RH/W1S	0b	MII Reset. This bit will reset the Digital blocks of the PHY and return registers 0x0-0x0F back to default values. Other register will not be affected. 0b = No reset 1b = Digital in reset and all MII regs (0x0 - 0xF) reset to default
14	xMII Loopback	R/W	0b	xMII Loopback: 1 = xMII Loopback enabled 0 = Normal Operation When xMII loopback mode is activated, the transmitted data presented on xMII TXD is looped back to xMII RXD internally. There is no LINK indication generated when xMII loopback is enabled. 1b = Enable Loopback from G/MII input to G/MII output
13	Manual_speed_MII	R	1b	Speed Selection: Always 100-Mbps Speed
12	Auto-Negotiation Enable	R	0b	Auto-Negotiation: Not supported on this device 0b = Disable Auto-Negotiation
11	Power Down	R/W	0b	Power Down: The PHY is powered down after this bit is set. Only register access is enabled during this power down condition. The power down mode can be controlled via this bit or via INT_N pin. INT_N pin needs to be configured to operate as power down control. This bit is OR-ed with the input from the INT_N pin. When the active low INT_N is asserted, this bit is set. 0b = Normal Mode 1b = IEEE Power Down
10	Isolate	R/W	0b	Isolate:Isolates the port from the xMII with the exception of the serial management interface 0b = Normal Mode 1b = Enable Isolate Mode
9	RESERVED	R	0b	Reserved
8	Duplex Mode	R	1b	1 = Full Duplex 0 = Half duplex 0b = Half duplex 1b = Full Duplex
7	RESERVED	R/W	0b	Reserved
6-0	RESERVED	R	0b	Reserved

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8.6.2.2 BMSR Register (Address = 1h) [Reset = 0061h]

BMSR is shown in Figure 8-21 and described in Table 8-30.

Return to the Table 8-27.

Figure 8-21. BMSR Register

15	14	13	12	11	10	9	8
100Base-T4	100Base-X Full Duplex	100Base-X Half Duplex	10 Mbps Full Duplex	10 Mbps Half Duplex	RESERVED		
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b		
7	6	5	4	3	2	1	0
RESERVED	MF Preamble Suppression	Auto-Negotiation Complete	Remote fault	Auto-Negotiation Ability	Link status	jabber detect	Extended Capability
R-0b	R-1b	R-1b	H-0b	R-0b	0b	H-0b	R-1b

Table 8-30. BMSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	100Base-T4	R	0b	Always 0 - PHY not able to perform 100Base-T4
14	100Base-X Full Duplex	R	0b	1 = PHY able to perform full duplex 100Base-X 0 = PHY not able to perform full duplex 100Base-X 0b = PHY not able to perform full duplex 100Base-X 1b = PHY able to perform full duplex 100Base-X
13	100Base-X Half Duplex	R	0b	1 = PHY able to perform half duplex 100Base-X 0 = PHY not able to perform half duplex 100Base-X 0b = PHY not able to perform half duplex 100Base-X 1b = PHY able to perform half duplex 100Base-X
12	10 Mbps Full Duplex	R	0b	1 = PHY able to operate at 10Mbps in full duplex 0 = PHY not able to operate at 10Mbps in full duplex 0b = PHY not able to operate at 10Mbps in full duplex 1b = PHY able to operate at 10Mbps in full duplex
11	10 Mbps Half Duplex	R	0b	1 = PHY able to operate at 10Mbps in half duplex 0 = PHY not able to operate at 10Mbps in half duplex 0b = PHY not able to operate at 10Mbps in half duplex 1b = PHY able to operate at 10Mbps in half duplex
10-7	RESERVED	R	0b	Reserved
6	MF Preamble Suppression	R	1b	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed 0b = PHY will not accept management frames with preamble suppressed 1b = PHY will accept management frames with preamble suppressed
5	Auto-Negotiation Complete	R	1b	1 = Auto-Negotiation process completed 0 = Auto Negotiation process not completed (either still in process, disabled or reset) 0b = Auto Negotiation process not completed (either still in process, disabled or reset) 1b = Auto-Negotiation process completed
4	Remote fault	H	0b	1 = Remote fault condition detected 0 = No remote fault condition detected 0b = No remote fault condition detected 1b = Remote fault condition detected
3	Auto-Negotiation Ability	R	0b	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation 0b = PHY is not able to perform Auto-Negotiation 1b = PHY is able to perform Auto-Negotiation
2	Link status		0b	Link Status bit 0b = Link is down 1b = Link is up

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Table 8-30. BMSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	jabber detect	H	0b	1= jabber condition detected 0 = No jabber condition detected 0b = No jabber condition detected 1b = jabber condition detected
0	Extended Capability	R	1b	1 = Extended register capabilities 0 = Basic register set capabilities only 0b = Basic register set capabilities only 1b = Extended register capabilities

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8.6.2.3 PHYIDR1 Register (Address = 2h) [Reset = 2000h]

PHYIDR1 is shown in Figure 8-22 and described in Table 8-31.

Return to the Table 8-27.

Figure 8-22. PHYIDR1 Register

15	14	13	12	11	10	9	8
Organizationally Unique Identifier Bits 21:6							
R-100000000000000b							
7	6	5	4	3	2	1	0
Organizationally Unique Identifier Bits 21:6							
R-100000000000000b							

Table 8-31. PHYIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Organizationally Unique Identifier Bits 21:6	R	1000000000 0000b	Organizationally Unique Identification Number

8.6.2.4 PHYIDR2 Register (Address = 3h) [Reset = A271h]

PHYIDR2 is shown in Figure 8-23 and described in Table 8-32.

Return to the Table 8-27.

Figure 8-23. PHYIDR2 Register

15	14	13	12	11	10	9	8
Organizationally Unique Identifier Bits 5:0						Model Number	
R-101000b						R-100111b	
7	6	5	4	3	2	1	0
Model Number				Revision Number			
R-100111b				R-1b			

Table 8-32. PHYIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Organizationally Unique Identifier Bits 5:0	R	101000b	Organizationally Unique Identification Number
9-4	Model Number	R	100111b	Vendor Model Number: The six bits of vendor model number are mapped from bits 9 to 4
3-0	Revision Number	R	1b	Device Revision Number 0b = Silicon Rev 1.0 1b = Silicon Rev 2.0

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8.6.2.5 PHYSTS Register (Address = 10h) [Reset = 0004h]

PHYSTS is shown in Figure 8-24 and described in Table 8-33.

Return to the Table 8-27.

Figure 8-24. PHYSTS Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	receive_error_latch	RESERVED	RESERVED	signal_detect	descrambler_lock	RESERVED
R-0b	R-0b	H-0b	H-0b	H-0b	R/W0S-0b	R/W0S-0b	R-0b
7	6	5	4	3	2	1	0
mii_interrupt	RESERVED	jabber_dtct	RESERVED	loopback_status	duplex_status	RESERVED	link_status
H-0b	R-0b	R-0b	H-0b	R-0b	R-1b	R-0b	R-0b

Table 8-33. PHYSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved
14	RESERVED	R	0b	Reserved
13	receive_error_latch	H	0b	RxerrCnt0 since last read.clear on read
12	RESERVED	H	0b	Reserved
11	RESERVED	H	0b	Reserved
10	signal_detect	R/W0S	0b	Channel ok latch low 0b = Channel ok had been reset 1b = Channel ok is set
9	descrambler_lock	R/W0S	0b	Descrambler lock latch low 0b = Descrmabler had been locked 1b = Descrambler is locked
8	RESERVED	R	0b	Reserved
7	mii_interrupt	H	0b	Interrupts pin status, cleared on reading 0x12 1b0 = Interrupts pin not set 1b1 = Interrupt pin had been set
6	RESERVED	R	0b	Reserved
5	jabber_dtct	R	0b	duplicate from reg.0x1.1
4	RESERVED	H	0b	Reserved
3	loopback_status	R	0b	MII loopback status 0b = No MII loopback 1b = MII loopback
2	duplex_status	R	1b	Duplex mode status 0b = Half duplex 1b = Full duplex
1	RESERVED	R	0b	Reserved
0	link_status	R	0b	duplication of reg.0x1.2 - link_status_bit 0b = Link is down 1b = Link is up

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8.6.2.6 PHYSCR Register (Address = 11h) [Reset = 010Bh]

PHYSCR is shown in Figure 8-25 and described in Table 8-34.

Return to the Table 8-27.

Figure 8-25. PHYSCR Register

15	14	13	12	11	10	9	8
dis_clk_125	pwr_save_mode_en	pwr_save_mode		sgmii_soft_reset	use_PHYAD0_as_Isolate	tx_fifo_depth	
R/W-0b	R/W-0b	R/W-0b		R/WSC-0b	R/W-0b	R/W-1b	
7	6	5	4	3	2	1	0
RESERVED	RESERVED			int_pol	force_interrupt	INTEN	INT_OE
R/W-0b	R-0b			R/W-1b	R/W-0b	R/W-1b	R/W-1b

Table 8-34. PHYSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	dis_clk_125	R/W	0b	1 = Disable CLK125 (Sourced by the CLK125 port) 1b = Disable CLK125 (Sourced by the CLK125 port)
14	pwr_save_mode_en	R/W	0b	Enable power save mode config from reg
13-12	pwr_save_mode	R/W	0b	Power Save Mode 0b = Normal mode 1b = IEEE mode: power down all digital and analog blocks, if bit [11] set to zero, PLL is also powered down 10 = Reserved 11 = Reserved
11	sgmii_soft_reset	R/WSC	0b	Reset SGMII
10	use_PHYAD0_as_Isolate	R/W	0b	1- when phy_addr == 0, isolate MAC Interface 0- do not Isolate for PHYAD == 0. 0b = do not Isolate for PHYAD is 0. 1b = when phy_addr is 0, isolate MAC Interface
9-8	tx_fifo_depth	R/W	1b	RMII TX fifo depth 0b = 4 nibbles 1b = 5 nibbles 1010b = 6 nibbles 1011b = 8 nibbles
7	RESERVED	R/W	0b	Reserved
6-4	RESERVED	R	0b	Reserved
3	int_pol	R/W	1b	Interrupt Polarity 0b = Steady state (normal operation) without an interrupt is logical 0; during interrupt, pin is logical 1 1b = Steady state (normal operation) without an interrupt is logical 1; during interrupt, pin is logical 0
2	force_interrupt	R/W	0b	Force interrupt pin 0b = Do not force interrupt pin 1b = Force interrupt pin
1	INTEN	R/W	1b	Enable interrupts 0b = Disable interrupts 1b = Enable interrupts
0	INT_OE	R/W	1b	Interrupt/Power down pin configuration 0b = PIN is a power down PIN (input) 1b = PIN is an interrupt pin (output)

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8.6.2.7 MISR1 Register (Address = 12h) [Reset = 0000h]

MISR1 is shown in Figure 8-26 and described in Table 8-35.

Return to the Table 8-27.

Figure 8-26. MISR1 Register

15	14	13	12	11	10	9	8
RESERVED	energy_det_int	link_int	wol_int	esd_int	ms_train_done_int	fhf_int	rhf_int
H-0b	H-0b	H-0b	H-0b	H-0b	H-0b	H-0b	H-0b
7	6	5	4	3	2	1	0
link_qual_int_en	energy_det_int_en	link_int_en	wol_int_en	esd_int_en	ms_train_done_int_en	fhf_int_en	rhf_int_en
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-35. MISR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	H	0b	Reserved
14	energy_det_int	H	0b	This INT can be asserted upon Rising edge only of energy_det signal using reg0x101 bit [0] : cfg_energy_det_int_le_only. status output of energy_det_hist signal on reg0x19 bit[10]. 0b = No Change of energy detected 1b = Change of energy_detected (both rising and falling edges)
13	link_int	H	0b	Link status change interrupt 0b = No change of link status interrupt pending. 1b = Change of link status interrupt is pending and is cleared by the current read.
12	wol_int	H	0b	Interrupt bit indicating that WOL packet is received 0b = No WoL interrupt pending. 1b = WoL packet received interrupt is pending and is cleared by the current read.
11	esd_int	H	0b	1 = ESD detected interrupt is pending and is cleared by the current read. 0 = No ESD interrupt pending.
10	ms_train_done_int	H	0b	1 = M/S Link Training Completed interrupt is pending and is cleared by the current read. 0 = No M/S Link Training Completed interrupt pending.
9	fhf_int	H	0b	1 = False carrier counter half-full interrupt is pending and is cleared by the current read. 0 = No false carrier counter half-full interrupt pending.
8	rhf_int	H	0b	1 = Receive error counter half-full interrupt is pending and is cleared by the current read. 0 = No receive error carrier counter half-full interrupt pending.
7	link_qual_int_en	R/W	0b	Enable Interrupt on Link Quality status.
6	energy_det_int_en	R/W	0b	Enable Interrupt on change of Energy Detect histr. Status
5	link_int_en	R/W	0b	Enable Interrupt on change of link status
4	wol_int_en	R/W	0b	Enable Interrupt on WoL detection
3	esd_int_en	R/W	0b	Enable Interrupt on ESD detect event
2	ms_train_done_int_en	R/W	0b	Enable Interrupt on M/S Link Training Completed event
1	fhf_int_en	R/W	0b	Enable Interrupt on False Carrier Counter Register half-full event
0	rhf_int_en	R/W	0b	Enable Interrupt on Receive Error Counter Register half-full event

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8.6.2.8 MISR2 Register (Address = 13h) [Reset = 0000h]

MISR2 is shown in Figure 8-27 and described in Table 8-36.

Return to the Table 8-27.

Figure 8-27. MISR2 Register

15	14	13	12	11	10	9	8
under_volt_int	over_volt_int	RESERVED	RESERVED	RESERVED	sleep_int	pol_int	jabber_int
H-0b	H-0b	H-0b	H-0b	H-0b	H-0b	H-0b	H-0b
7	6	5	4	3	2	1	0
under_volt_int_en	over_volt_int_en	page_rcvd_int_en	Fifo_int_en	RESERVED	sleep_int_en	pol_int_en	jabber_int_en
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-36. MISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	under_volt_int	H	0b	1 = Under Voltage has been detected 0 =Under Voltage has not been detected 0b = Under Voltage has not been detected 1b = Under Voltage has been detected
14	over_volt_int	H	0b	1 = Over Voltage has been detected 0 = Over Voltage has not been detected 0b = Over Voltage has not been detected 1b = Over Voltage has been detected
13	RESERVED	H	0b	Reserved
12	RESERVED	H	0b	Reserved
11	RESERVED	H	0b	Reserved
10	sleep_int	H	0b	1 = Sleep mode has changed 0 = Sleep mode has not changed 0b = Sleep mode has not changed 1b = Sleep mode has changed
9	pol_int	H	0b	The device has auto-polarity correction when operating in slave mode. This bit will reflect if polarity was automatically swapped or not. 0b = Data polarity has not changed 1b = Data polarity has changed
8	jabber_int	H	0b	1 = Jabber detected 0 = Jabber not detected 0b = Jabber not detected 1b = Jabber detected
7	under_volt_int_en	R/W	0b	0 = Disable interrupt 0b = Disable interrupt
6	over_volt_int_en	R/W	0b	0 = Disable interrupt 0b = Disable interrupt
5	page_rcvd_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt
4	Fifo_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt
3	RESERVED	R/W	0b	Reserved
2	sleep_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt
1	pol_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt
0	jabber_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt

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8.6.2.9 RECR Register (Address = 15h) [Reset = 0000h]

RECR is shown in Figure 8-28 and described in Table 8-37.

Return to the Table 8-27.

Figure 8-28. RECR Register

15	14	13	12	11	10	9	8
rx_err_cnt							
0b							
7	6	5	4	3	2	1	0
rx_err_cnt							
0b							

Table 8-37. RECR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_err_cnt		0b	RX_ER Counter: When a valid carrier is presented (only while RX_DV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in xMII loopback mode. The counter stops when it reaches its maximum count (0xFFFF). When the counter exceeds half-full (0x7FFF), an interrupt is generated. This register is cleared on read.

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8.6.2.10 BISCR Register (Address = 16h) [Reset = 0100h]

BISCR is shown in Figure 8-29 and described in Table 8-38.

Return to the Table 8-27.

Figure 8-29. BISCR Register

15	14	13	12	11	10	9	8
RESERVED					prbs_sync_loss	RESERVED	core_pwr_mode
R-0b					H-0b	R-0b	R-1b
7	6	5	4	3	2	1	0
RESERVED	tx_mii_lpbk	loopback_mode				pcs_lpbck	RESERVED
R-0b	R/W-0b	R/W-0b				R/W-0b	R/W-0b

Table 8-38. BISCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0b	Reserved
10	prbs_sync_loss	H	0b	Prbs lock lost latch status 0b = Prbs lock never lost 1b = Prbs lock had been lost
9	RESERVED	R	0b	Reserved
8	core_pwr_mode	R	1b	1b0 = Core is in power down or sleep mode 1b1 = Core is is normal power mode 0b = Core is in power down or sleep mode 1b = Core is is normal power mode
7	RESERVED	R	0b	Reserved
6	tx_mii_lpbk	R/W	0b	Transmit data control during xMII Loopback 0b = Suppress data during xMII loopback 1b = Transmit data on MDI during xMII loopback
5-2	loopback_mode	R/W	0b	Loopback Modes (Bit [1:0] should be 0) 1b = Digital Loopback 10b = Analog Loopback 100b = Reverse Loopback 1000b = External Loopback
1	pcs_lpbck	R/W	0b	PCS loopback after PAM3 0b = Disable PCS Loopback 1b = Enable PCS Loopback
0	RESERVED	R/W	0b	Reserved

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8.6.2.11 MISR3 Register (Address = 18h) [Reset = X]

MISR3 is shown in Figure 8-30 and described in Table 8-39.

Return to the Table 8-27.

Figure 8-30. MISR3 Register

15	14	13	12	11	10	9	8
wup_psv_int	no_link_int	sleep_fail_int	POR_done_int	no_frame_int	wake_req_int	WUP_sleep_int	LPS_int
H-0b	H-0b	H-0b	H-0b	H-0b	H-0b	H-0b	H-0b
7	6	5	4	3	2	1	0
wup_psv_int_en	no_link_int_en	sleep_fail_int_en	POR_done_int_en	no_frame_int_en	wake_req_int_en	WUP_sleep_int_en	LPS_int_en
R/W-X	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-1b

Table 8-39. MISR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	wup_psv_int	H	0b	0b = WUP are not received 1b = WUP received from remote PHY when in passive link
14	no_link_int	H	0b	1= Link has not been observed within time programmed in 0x562 once training has started. 0= Link up is still in progress or Link has already formed 0b = Link up is still in progress or Link has already formed 1b = Link has not been observed within time programmed in 0x562 once training has started.
13	sleep_fail_int	H	0b	0b = Sleep negotiation not failed yet 1b = Sleep negotiation failed
12	POR_done_int	H	0b	0b = POR not completed yet 1b = POR completed (required for re-initialization of registers when we come out of sleep)
11	no_frame_int	H	0b	0b = Frame was detected 1b = No Frame detected for transmission or reception in given time
10	wake_req_int	H	0b	0b = Wake-up request not received 1b = Wake-up request command was received from remote PHY
9	WUP_sleep_int	H	0b	0b = WUP not received 1b = WUP received from remote PHY when in sleep
8	LPS_int	H	0b	0b = LPS symbols not detected 1b = LPS symbols detetced
7	wup_psv_int_en	R/W	X	0b = Disable interrupt 1b = Enable interrupt
6	no_link_int_en	R/W	0b	0b = Disable interrupt 1b = Enable interrupt
5	sleep_fail_int_en	R/W	1b	0b = Disable interrupt 1b = Enable interrupt
4	POR_done_int_en	R/W	0b	0b = Disable interrupt 1b = Enable interrupt
3	no_frame_int_en	R/W	0b	0b = Disable interrupt 1b = Enable interrupt
2	wake_req_int_en	R/W	1b	0b = Disable interrupt 1b = Enable interrupt
1	WUP_sleep_int_en	R/W	0b	0b = Disable interrupt 1b = Enable interrupt
0	LPS_int_en	R/W	1b	0b = Disable interrupt 1b = Enable interrupt

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8.6.2.12 REG_19 Register (Address = 19h) [Reset = 0800h]

REG_19 is shown in Figure 8-31 and described in Table 8-40.

Return to the Table 8-27.

Figure 8-31. REG_19 Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED	RESERVED	RESERVED	dsp_energy_detect	RESERVED	
R-0b		R-0b	R-0b	R-1b	R-0b	R-0b	
7	6	5	4	3	2	1	0
RESERVED			PHY_ADDR				
R-0b			R-0b				

Table 8-40. REG_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13	RESERVED	R	0b	Reserved
12	RESERVED	R	0b	Reserved
11	RESERVED	R	1b	Reserved
10	dsp_energy_detect	R	0b	DSP energy detected status
9-5	RESERVED	R	0b	Reserved
4-0	PHY_ADDR	R	0b	PHY address decode from straps

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8.6.2.13 TC10_ABORT_REG Register (Address = 1Bh) [Reset = 0000h]

TC10_ABORT_REG is shown in Figure 8-32 and described in Table 8-41.

Return to the Table 8-27.

Figure 8-32. TC10_ABORT_REG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED						cfg_tc10_abort_gpio_en	cfg_sleep_abort
R-0b						R/W-0b	R/W-0b

Table 8-41. TC10_ABORT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0b	Reserved
1	cfg_tc10_abort_gpio_en	R/W	0b	enables aborting TC10 via GPIO. one of CLKOUT/LED_1 pins which is being used as an LED can be used to abort 0b = disable TC10 abort via GPIO 1b = enable TC10 abort via GPIO
0	cfg_sleep_abort	R/W	0b	loc_sleep_abprt as defined by TC10 standard. Aborts sleep negotiation while in SLEEP_ACK state 0b = allow TC10 sleep negotiation 1b = abort TC10 sleep negotiation

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8.6.2.14 CDCR Register (Address = 1Eh) [Reset = 0000h]

CDCR is shown in Figure 8-33 and described in Table 8-42.

Return to the Table 8-27.

Figure 8-33. CDCR Register

15	14	13	12	11	10	9	8
tdr_start	cfg_tdr_auto_run	RESERVED					
RH/W1S-0b	R/W-0b	R-0b					
7	6	5	4	3	2	1	0
RESERVED						tdr_done	tdr_fail
R-0b						R-0b	R-0b

Table 8-42. CDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	tdr_start	RH/W1S	0b	clr by tdr done Start TDR manually 0b = No TDR 1b = TDR start
14	cfg_tdr_auto_run	R/W	0b	Enable TDR auto run on link down 0b = TDR start manually 1b = TDR start automatically on link down
13-2	RESERVED	R	0b	Reserved
1	tdr_done	R	0b	TDR done status 0b = TDR still not done 1b = TDR done
0	tdr_fail	R	0b	TDR fail status

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8.6.2.15 PHYRCR Register (Address = 1Fh) [Reset = 0000h]

PHYRCR is shown in Figure 8-34 and described in Table 8-43.

Return to the Table 8-27.

Figure 8-34. PHYRCR Register

15	14	13	12	11	10	9	8
Software Global Reset	Digital reset	RESERVED	RESERVED				
RH/W1S-0b	RH/W1S-0b	R/W-0b	R/W-0b				
7	6	5	4	3	2	1	0
Standby_mode	RESERVED	RESERVED	RESERVED				
R/W-0b	R/W-0b	R-0b	R/W-0b				

Table 8-43. PHYRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Software Global Reset	RH/W1S	0b	Hardware Reset(Reset digital + register file) 0b = Normal Operation 1b = Reset PHY. This bit is self cleared and has the same effect as the RESET pin.
14	Digital reset	RH/W1S	0b	Software Restart 0b = Normal Operation 1b = Restart PHY. This bit is self cleared and resets all PHY circuitry except registers.
13	RESERVED	R/W	0b	Reserved
12-8	RESERVED	R/W	0b	Reserved
7	Standby_mode	R/W	0b	Standby Mode 0b = Normal operation 1b = Standby mode enabled
6	RESERVED	R/W	0b	Reserved
5	RESERVED	R	0b	Reserved
4-0	RESERVED	R/W	0b	Reserved

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8.6.2.16 Register_41 (Address = 41h) [Reset = 88F7h]

Register_41 is shown in Figure 8-35 and described in Table 8-44.

Return to the Table 8-27.

Figure 8-35. Register_41

15	14	13	12	11	10	9	8
cfg_ether_type_pattern							
R/W-1000100011110111b							
7	6	5	4	3	2	1	0
cfg_ether_type_pattern							
R/W-1000100011110111b							

Table 8-44. Register_41 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_ether_type_pattern	R/W	1000100011110111b	Ethertype pattern to be detected when 0x40[0] is enabled

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8.6.2.17 Register_133 (Address = 133h) [Reset = 0000h]

Register_133 is shown in Figure 8-36 and described in Table 8-45.

Return to the Table 8-27.

Figure 8-36. Register_133

15	14	13	12	11	10	9	8
RESERVED	link_up_c_and_s	link_status_pc	link_status	RESERVED			
R-0b	R-0b	R-0b	R-0b	R-0b			
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	descr_sync	loc_rcvr_status	rem_rcvr_status
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-45. Register_133 Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved
14	link_up_c_and_s	R	0b	link up for C & S
13	link_status_pc	R	0b	PHY control in SEND_DATA state
12	link_status	R	0b	link status set by link monitor
11-8	RESERVED	R	0b	Reserved
7	RESERVED	R	0b	Reserved
6	RESERVED	R	0b	Reserved
5	RESERVED	R	0b	Reserved
4	RESERVED	R	0b	Reserved
3	RESERVED	R	0b	Reserved
2	descr_sync	R	0b	Status of descrambler 0b = Scrambler Not Locked 1b = Scrambler Locked
1	loc_rcvr_status	R	0b	Local receiver status 0b = Local PHY received link invalid 1b = Local PHY received link valid
0	rem_rcvr_status	R	0b	Remote receiver status 0b = Remote PHY received link invalid 1b = Remote PHY received link valid

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8.6.2.18 Register_17F (Address = 17Fh) [Reset = 4028h]

Register_17F is shown in Figure 8-37 and described in Table 8-46.

Return to the Table 8-27.

Figure 8-37. Register_17F

15	14	13	12	11	10	9	8
cfg_en_wur_via_wake	cfg_en_wup_via_wake	RESERVED					
R/W-0b	R/W-1b	R-0b					
7	6	5	4	3	2	1	0
cfg_wake_pin_len_fr_wur_th							
R/W-101000b							

Table 8-46. Register_17F Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_en_wur_via_wake	R/W	0b	enable sending WUR when wake pin is asserted during active link. Duration of pulse on WAKE pin can be configured in 0x17F[7:0] 0b = disable sending WUR when pulse on wake pin 1b = enable sending WUR when pulse on wake pin
14	cfg_en_wup_via_wake	R/W	1b	enable sending WUP when device is woken by WAKE pin 0b = disables WUP 1b = enables WUP
13-8	RESERVED	R	0b	Reserved
7-0	cfg_wake_pin_len_fr_wur_th	R/W	101000b	Width of pulse in microseconds required to initiate WUR during an active link

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8.6.2.19 Register_180 (Address = 180h) [Reset = 0000h]

Register_180 is shown in Figure 8-38 and described in Table 8-47.

Return to the Table 8-27.

Figure 8-38. Register_180

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED			cfg_sleep_req_timer_sel		RESERVED	cfg_sleep_ack_timer_sel	
R-0b			R/W-0b		R-0b	R/W-0b	

Table 8-47. Register_180 Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0b	Reserved
4-3	cfg_sleep_req_timer_sel	R/W	0b	Configure sleep request timer 0b = 16ms 1b = 4ms 10b = 32ms 11b = 40ms
2	RESERVED	R	0b	Reserved
1-0	cfg_sleep_ack_timer_sel	R/W	0b	Configure sleep acknowledge timer 0b = 8ms 1b = 6ms 10b = 24ms 11b = 32ms

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8.6.2.20 Register_181 (Address = 181h) [Reset = 0000h]

Register_181 is shown in Figure 8-39 and described in Table 8-48.

Return to the Table 8-27.

Figure 8-39. Register_181

15	14	13	12	11	10	9	8
RESERVED						rx_lps_cnt	
R-0b						R-0b	
7	6	5	4	3	2	1	0
rx_lps_cnt							
R-0b							

Table 8-48. Register_181 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0b	Reserved
9-0	rx_lps_cnt	R	0b	indicates number of LPS codes received

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8.6.2.21 Register_182 (Address = 182h) [Reset = 0000h]

Register_182 is shown in Figure 8-40 and described in Table 8-49.

Return to the Table 8-27.

Figure 8-40. Register_182

15	14	13	12	11	10	9	8
RESERVED						tx_lps_cnt	
R-0b						R-0b	
7	6	5	4	3	2	1	0
tx_lps_cnt							
R-0b							

Table 8-49. Register_182 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0b	Reserved
9-0	tx_lps_cnt	R	0b	indicates number of WUR codes received

8.6.2.22 LPS_CFG4 Register (Address = 183h) [Reset = 0000h]

LPS_CFG4 is shown in Figure 8-41 and described in Table 8-50.

Return to the Table 8-27.

Figure 8-41. LPS_CFG4 Register

15	14	13	12	11	10	9	8
cfg_send_wup_dis_tx	cfg_force_lps_sleep_en	cfg_force_lps_sleep	cfg_force_tx_lps_en	cfg_force_tx_lps	cfg_force_lps_link_control_en	cfg_force_lps_link_control	cfg_force_lps_st_en
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
RESERVED	cfg_force_lps_st						
R-0b	R/W-0b						

Table 8-50. LPS_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_send_wup_dis_tx	R/W	0b	Write 1 to this bit to send WUP when PHY control is in DISABLE_TRANSMIT state
14	cfg_force_lps_sleep_en	R/W	0b	force control enable for sleep from LPS SM to PHY control SM
13	cfg_force_lps_sleep	R/W	0b	force value for sleep from LPS SM to PHY control SM
12	cfg_force_tx_lps_en	R/W	0b	force enable for TX_LPS
11	cfg_force_tx_lps	R/W	0b	force value for TX_LPS
10	cfg_force_lps_link_control_en	R/W	0b	force link control enable to LPS state machine
9	cfg_force_lps_link_control	R/W	0b	force link control value from LPS state machine
8	cfg_force_lps_st_en	R/W	0b	force enable for LPS state machine
7	RESERVED	R	0b	Reserved
6-0	cfg_force_lps_st	R/W	0b	force value of LPS state machine

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8.6.2.23 LPS_CFG Register (Address = 184h) [Reset = 0223h]

LPS_CFG is shown in Figure 8-42 and described in Table 8-51.

Return to the Table 8-27.

Figure 8-42. LPS_CFG Register

15	14	13	12	11	10	9	8
cfg_reset_wur_cnt_rx_data	RESERVED		cfg_reset_lps_cnt_rx_data	RESERVED		cfg_reset_wur_cnt_tx_data	RESERVED
R/W-0b	R-0b		R/W-0b	R-0b		R/W-1b	R-0b
7	6	5	4	3	2	1	0
RESERVED	cfg_reset_lps_cnt_tx_data	cfg_wake_fwd_en_wup_psv_link	cfg_wake_fwd_man_trig	cfg_wake_fwd_dig_timer		cfg_wake_fwd_en_wur	cfg_wake_fwd_en_wup
R-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b		R/W-1b	R/W-1b

Table 8-51. LPS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_reset_wur_cnt_rx_data	R/W	0b	When set, resets the WUR received symbol counter upon receiving data
14-13	RESERVED	R	0b	Reserved
12	cfg_reset_lps_cnt_rx_data	R/W	0b	When set, resets the LPS received symbol counter upon receiving data
11-10	RESERVED	R	0b	Reserved
9	cfg_reset_wur_cnt_tx_data	R/W	1b	When set, resets the transmitted WUR symbols count when sending data
8-7	RESERVED	R	0b	Reserved
6	cfg_reset_lps_cnt_tx_data	R/W	0b	When set, resets the transmitted LPS symbols count when sending data
5	cfg_wake_fwd_en_wup_psv_link	R/W	1b	control to enable/disable Wake forwarding on WAKE pin when WUP is received when in PASSIVE_LINK mode 0b = disables wake forwarding 1b = enables wake forwarding
4	cfg_wake_fwd_man_trig	R/W	0b	Write 1 to manually generate Wake forwarding signal on WAKE pin. This bit is self-cleared
3-2	cfg_wake_fwd_dig_timer	R/W	0b	when wake up request is received on an active link, the width of wake forwarding pulses are configurable to : 00: 50us 01: 500us 10: 2ms 11: 20ms
1	cfg_wake_fwd_en_wur	R/W	1b	If set, enables doing wake forwarding when WUR symbols are received 0b = Don 't do wake forwarding on WAKE pin 1b = do wake forwarding on WAKE pin
0	cfg_wake_fwd_en_wup	R/W	1b	If set, enables doing wake forwarding when WUP symbols are received 0b = Don 't do wake forwarding on WAKE pin 1b = do wake forwarding on WAKE pin

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8.6.2.24 LPS_CFG5 Register (Address = 185h) [Reset = 0000h]

LPS_CFG5 is shown in Figure 8-43 and described in Table 8-52.

Return to the Table 8-27.

Figure 8-43. LPS_CFG5 Register

15	14	13	12	11	10	9	8
cfg_wup_timer			RESERVED				
R/W-0b			R-0b				
7	6	5	4	3	2	1	0
RESERVED				cfg_rx_wur_sym_gap		cfg_rx_lps_sym_gap	
R-0b				R/W-0b		R/W-0b	

Table 8-52. LPS_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	cfg_wup_timer	R/W	0b	Time for which PHY control SM stays in WAKE_TRANSMIT b000: 1ms b001: 0.7ms b010: 1.3ms b011: 0.85ms b100: 1.5ms b101: 2ms b110: 2.5ms b111: 3ms
12-4	RESERVED	R	0b	Reserved
3-2	cfg_rx_wur_sym_gap	R/W	0b	max gap allowed b/w two WUR symbols for ack of WUR
1-0	cfg_rx_lps_sym_gap	R/W	0b	max gap allowed b/w two LPS symbols for ack of LPS

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8.6.2.25 LPS_CFG7 Register (Address = 187h) [Reset = 0000h]

LPS_CFG7 is shown in Figure 8-44 and described in Table 8-53.

Return to the Table 8-27.

Figure 8-44. LPS_CFG7 Register

15	14	13	12	11	10	9	8
cfg_tx_lps_stop_on_done	RESERVED						
R/W-0b	R-0b						
7	6	5	4	3	2	1	0
cfg_tx_lps_sel							
R/W-0b							

Table 8-53. LPS_CFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_tx_lps_stop_on_done	R/W	0b	configures the device to stop sending LPS codes once it is done sending the number of codes configures in 0x1879:0 0b = continues even after reaching limit 1b = stops after reaching limit
14-8	RESERVED	R	0b	Reserved
9-0	cfg_tx_lps_sel	R/W	0b	Indicates number of LPS symbols to be transmitted before tx_lps_done becomes true

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8.6.2.26 LPS_CFG8 Register (Address = 188h) [Reset = 0080h]

LPS_CFG8 is shown in Figure 8-45 and described in Table 8-54.

Return to the Table 8-27.

Figure 8-45. LPS_CFG8 Register

15	14	13	12	11	10	9	8
RESERVED						cfg_tx_wur_sel	
R-0b						R/W-10000000b	
7	6	5	4	3	2	1	0
cfg_tx_wur_sel							
R/W-10000000b							

Table 8-54. LPS_CFG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0b	Reserved
9-0	cfg_tx_wur_sel	R/W	10000000b	Indicates number of WUR symbols to be transmitted

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8.6.2.27 LPS_CFG9 Register (Address = 189h) [Reset = 0040h]

LPS_CFG9 is shown in Figure 8-46 and described in Table 8-55.

Return to the Table 8-27.

Figure 8-46. LPS_CFG9 Register

15	14	13	12	11	10	9	8
RESERVED						cfg_rx_lps_sel	
R-0b						R/W-1000000b	
7	6	5	4	3	2	1	0
cfg_rx_lps_sel							
R/W-1000000b							

Table 8-55. LPS_CFG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0b	Reserved
9-0	cfg_rx_lps_sel	R/W	1000000b	Indicates number of LPS symbols to be received to set lps_recv

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8.6.2.28 LPS_CFG10 Register (Address = 18Ah) [Reset = 0040h]

LPS_CFG10 is shown in Figure 8-47 and described in Table 8-56.

Return to the Table 8-27.

Figure 8-47. LPS_CFG10 Register

15	14	13	12	11	10	9	8
RESERVED						cfg_rx_wur_sel	
R-0b						R/W-1000000b	
7	6	5	4	3	2	1	0
cfg_rx_wur_sel							
R/W-1000000b							

Table 8-56. LPS_CFG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0b	Reserved
9-0	cfg_rx_wur_sel	R/W	1000000b	Indicates number of WUR symbols to be received to acknowlege WUR and do wake forwarding

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8.6.2.29 LPS_CFG2 Register (Address = 18Bh) [Reset = 1C4Bh]

LPS_CFG2 is shown in Figure 8-48 and described in Table 8-57.

Return to the Table 8-27.

Figure 8-48. LPS_CFG2 Register

15	14	13	12	11	10	9	8
RESERVED			cfg_stop_sleep_neg_on_no_send_n	cfg_stop_sleep_neg_on_activity	RESERVED	RESERVED	RESERVED
R-0b			R/W-1b	R/W-1b	R/W-1b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
RESERVED	cfg_auto_mode_en	cfg_lps_mon_en	RESERVED	RESERVED	RESERVED	cfg_lps_sleep_en	RESERVED
R-0b	R/W-1b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-1b

Table 8-57. LPS_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12	cfg_stop_sleep_neg_on_no_send_n	R/W	1b	If this bit is set, TC10 statemachine reverts back to NORMAL state from SLEEP_ACK or SLEEP_REQ states when Link is dropped
11	cfg_stop_sleep_neg_on_activity	R/W	1b	When packets are either transmitted or received by the PHY, setting this bit Stops sleep negotiation and TC10 state machine reverts back to NORMAL state when it is in SLEEP_ACK or SLEEP_REQ state(when sleep negotiation is ongoing)
10	RESERVED	R/W	1b	Reserved
9	RESERVED	R/W	0b	Reserved
8	RESERVED	R/W	0b	Reserved
7	RESERVED	R	0b	Ignore on read
6	cfg_auto_mode_en	R/W	1b	LPS autonomous mode enable if(RX_D3_strap ==1) reset_val = ~CLKOUT_strap else reset_val = ~LED_1_strap This bit is Auto-cleared after Link-Up 0b = AUTO mode disabled 1b = AUTO mode enable
5	cfg_lps_mon_en	R/W	0b	Normal to Standby Transition Enable 0b = Disable normal to standby transition on over temp/under volt 1b = Enable normal to standby transition on over temp/under volt
4	RESERVED	R/W	0b	Reserved
3	RESERVED	R/W	1b	Reserved
2	RESERVED	R/W	0b	Reserved
1	cfg_lps_sleep_en	R/W	1b	Enable transition to Standby mode instead of Sleep mode after successful sleep negotiation (refered to as TC10_SBY) 0b = Enter standby after negotiated LPS 1b = Enter sleep after negotiated LPS
0	RESERVED	R/W	1b	Reserved

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8.6.2.30 LPS_CFG3 Register (Address = 18Ch) [Reset = 0000h]

LPS_CFG3 is shown in Figure 8-49 and described in Table 8-58.

Return to the Table 8-27.

Figure 8-49. LPS_CFG3 Register

15	14	13	12	11	10	9	8
RESERVED							cfg_lps_pwr_mode
R-0b							RH/W1S-0b
7	6	5	4	3	2	1	0
cfg_lps_pwr_mode							
RH/W1S-0b							

Table 8-58. LPS_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0b	Reserved
8-0	cfg_lps_pwr_mode	RH/W1S	0b	1b = Normal command 10b = Sleep request 10000b = Standby command 10000000b = WUR command

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8.6.2.31 LPS_STATUS Register (Address = 18Eh) [Reset = 0000h]

LPS_STATUS is shown in Figure 8-50 and described in Table 8-59.

Return to the Table 8-27.

Figure 8-50. LPS_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED	status_lps_st						
R-0b	R-0b						

Table 8-59. LPS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0b	Reserved
6-0	status_lps_st	R	0b	LPS SM state 1b = SLEEP 10b = STANDBY 100b = NORMAL 1000b = SLEEP_ACK 10000b = SLEEP_REQ 100000b = SLEEP_FAIL 1000000b = SLEEP_SILENT 1000001b = PASSIVE_LINK

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8.6.2.32 TDR_TX_CFG Register (Address = 300h) [Reset = 2710h]

TDR_TX_CFG is shown in Figure 8-51 and described in Table 8-60.

Return to the Table 8-27.

Figure 8-51. TDR_TX_CFG Register

15	14	13	12	11	10	9	8
cfg_tdr_tx_duration							
R/W-10011100010000b							
7	6	5	4	3	2	1	0
cfg_tdr_tx_duration							
R/W-10011100010000b							

Table 8-60. TDR_TX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_tdr_tx_duration	R/W	1001110001 0000b	TDR transmit duration in usec, Default : 10000usec

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8.6.2.33 TAP_PROCESS_CFG Register (Address = 301h) [Reset = 1703h]

TAP_PROCESS_CFG is shown in Figure 8-52 and described in Table 8-61.

Return to the Table 8-27.

Figure 8-52. TAP_PROCESS_CFG Register

15	14	13	12	11	10	9	8
RESERVED			cfg_end_tap_index				
R-0b			R/W-10111b				
7	6	5	4	3	2	1	0
RESERVED			cfg_start_tap_index				
R-0b			R/W-11b				

Table 8-61. TAP_PROCESS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12-8	cfg_end_tap_index	R/W	10111b	End echo coefficient index for peak detect sweep during TDR
7-5	RESERVED	R	0b	Reserved
4-0	cfg_start_tap_index	R/W	11b	Starting echo coefficient index for peak detect sweep during TDR

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8.6.2.34 TDR_CFG1 Register (Address = 302h) [Reset = 0045h]

TDR_CFG1 is shown in Figure 8-53 and described in Table 8-62.

Return to the Table 8-27.

Figure 8-53. TDR_CFG1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
cfg_forward_shadow				cfg_post_silence_time		cfg_pre_silence_time	
R/W-100b				R/W-1b		R/W-1b	

Table 8-62. TDR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-4	cfg_forward_shadow	R/W	100b	Num of neighboring echo coeff taps to be considered for calculating local maximum
3-2	cfg_post_silence_time	R/W	1b	Post-Silence state timer in ms 0x00 : 0ms 0x01 : 10ms 0x10 : 100ms 0x11 : 1000ms
1-0	cfg_pre_silence_time	R/W	1b	Pre-Silence state timer in ms 0x00 : 0ms 0x01 : 10ms 0x10 : 100ms 0x11 : 1000ms

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8.6.2.35 TDR_CFG2 Register (Address = 303h) [Reset = 0419h]

TDR_CFG2 is shown in Figure 8-54 and described in Table 8-63.

Return to the Table 8-27.

Figure 8-54. TDR_CFG2 Register

15	14	13	12	11	10	9	8
RESERVED			cfg_tdr_filt_loc_offset				
R-0b			R/W-100b				
7	6	5	4	3	2	1	0
cfg_tdr_filt_init							
R/W-11001b							

Table 8-63. TDR_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12-8	cfg_tdr_filt_loc_offset	R/W	100b	tap index offset of dyamic peak equation, cfg_start_tap_index + 1'b1
7-0	cfg_tdr_filt_init	R/W	11001b	Value of peak_th at x=start_tap_index of dynamic peak threshold equation

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8.6.2.36 TDR_CFG3 Register (Address = 304h) [Reset = 0030h]

TDR_CFG3 is shown in Figure 8-55 and described in Table 8-64.

Return to the Table 8-27.

Figure 8-55. TDR_CFG3 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
cfg_tdr_filt_slope							
R/W-110000b							

Table 8-64. TDR_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-0	cfg_tdr_filt_slope	R/W	110000b	Slope of dynamic peak threshold equation (0.4)

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8.6.2.37 TDR_CFG4 Register (Address = 305h) [Reset = 0004h]

TDR_CFG4 is shown in Figure 8-56 and described in Table 8-65.

Return to the Table 8-27.

Figure 8-56. TDR_CFG4 Register

15	14	13	12	11	10	9	8
RESERVED						RESERVED	RESERVED
R-0b						R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
RESERVED	RESERVED	hpf_gain_tdr		pga_gain_tdr			
R/W-0b	R/W-0b	R/W-0b		R/W-100b			

Table 8-65. TDR_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0b	Reserved
9	RESERVED	R/W	0b	Reserved
8-7	RESERVED	R/W	0b	Reserved
6	RESERVED	R/W	0b	Reserved
5-4	hpf_gain_tdr	R/W	0b	HPF gain code during TDR
3-0	pga_gain_tdr	R/W	100b	PGA gain code during TDR

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8.6.2.38 TDR_CFG5 Register (Address = 306h) [Reset = 000Ah]

TDR_CFG5 is shown in Figure 8-57 and described in Table 8-66.

Return to the Table 8-27.

Figure 8-57. TDR_CFG5 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED			cfg_half_open_det_en	cfg_cable_delay_num			
R-0b			R/W-0b	R/W-1010b			

Table 8-66. TDR_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0b	Reserved
4	cfg_half_open_det_en	R/W	0b	enables detection of half cable 0b = Disables half open detection 1b = Enbales half open detection
3-0	cfg_cable_delay_num	R/W	1010b	Configure the propagation delay per meter of the cable in nanoseconds. This is used for the fault location estimation Valid values : 4 'd0 to 4 'd11 - [4.5:0.1:5.6]ns Default : 4 'd10 (5.5 ns)

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8.6.2.39 TDR_TC1 Register (Address = 310h) [Reset = 0000h]

TDR_TC1 is shown in Figure 8-58 and described in Table 8-67.

Return to the Table 8-27.

Figure 8-58. TDR_TC1 Register

15	14	13	12	11	10	9	8
RESERVED							half_open_detect
R-0b							R-0b
7	6	5	4	3	2	1	0
peak_detect	peak_sign	peak_loc_in_meters					
R-0b	R-0b	R-0b					

Table 8-67. TDR_TC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0b	Reserved
8	half_open_detect	R	0b	Half wire open detect value 0b = Half wire open not detected 1b = Half wire open detected
7	peak_detect	R	0b	Set if fault is detected in cable 0b = Fault not detected in cable 1b = Fault detected in cable
6	peak_sign	R	0b	Nature of discontinuity. Valid only if peak_detect is set 0b = Short to GND, supply, or between MDI pins 1b = Open. Applicable to both 1-wire and 2-wire open faults
5-0	peak_loc_in_meters	R	0b	Fault location in meters (Valid only if peak_detect is set)

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8.6.2.40 A2D_REG_48 Register (Address = 430h) [Reset = 0770h]

A2D_REG_48 is shown in Figure 8-59 and described in Table 8-68.

Return to the Table 8-27.

Figure 8-59. A2D_REG_48 Register

15	14	13	12	11	10	9	8
RESERVED			RESERVED	dll_tx_delay_ctrl_rgmii_sl			
R-0b			R/W-0b	R/W-111b			
7	6	5	4	3	2	1	0
dll_rx_delay_ctrl_rgmii_sl				RESERVED			
R/W-111b				R/W-0b			

Table 8-68. A2D_REG_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12	RESERVED	R/W	0b	Reserved
11-8	dll_tx_delay_ctrl_rgmii_sl	R/W	111b	controls TX DLL in RGMII mode inSteps of 312.5ps, affects the CLK_90 output. Delay = ((Bit[11:8] in decimal) + 1)*312.5 ps
7-4	dll_rx_delay_ctrl_rgmii_sl	R/W	111b	Controls RX DLL in RGMII mode in Steps of 312.5ps, affects the CLK_90 output. Delay = ((Bit[7:4] in decimal) + 1)*312.5 ps
3-0	RESERVED	R/W	0b	Reserved

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8.6.2.41 A2D_REG_68 Register (Address = 444h) [Reset = 0000h]

A2D_REG_68 is shown in Figure 8-60 and described in Table 8-69.

Return to the Table 8-27.

Figure 8-60. A2D_REG_68 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED				goto_sleep_force_val	goto_sleep_force_control	wake_fwd_force_val	wake_fwd_force_control
R-0b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-69. A2D_REG_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0b	Reserved
3	goto_sleep_force_val	R/W	0b	Sleep Mode Force Value:
2	goto_sleep_force_control	R/W	0b	Sleep Mode Force Control:
1	wake_fwd_force_val	R/W	0b	WAKE Output Force Value:
0	wake_fwd_force_control	R/W	0b	WAKE Output Value Force Control: 1b = Force Control Enable. Output value is set by 0x0444[1]

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8.6.2.42 LEDS_CFG_1 Register (Address = 450h) [Reset = 2610h]

LEDS_CFG_1 is shown in Figure 8-61 and described in Table 8-70.

Return to the Table 8-27.

Figure 8-61. LEDS_CFG_1 Register

15	14	13	12	11	10	9	8
RESERVED	leds_bypass_stretching	leds_blink_rate		led_2_option			
R-0b	R/W-0b	R/W-10b		R/W-110b			
7	6	5	4	3	2	1	0
led_1_option				led_0_option			
R/W-1b				R/W-0b			

Table 8-70. LEDS_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved
14	leds_bypass_stretching	R/W	0b	0b = Normal Operation 1b = Bypass LEDs stretching
13-12	leds_blink_rate	R/W	10b	0b = 20Hz (50mSec) 1b = 10Hz (100mSec) 1010b = 5Hz (200mSec) 1011b = 2Hz (500mSec)
11-8	led_2_option	R/W	110b	Controlls LED_2 sources (same as bits 3:0)
7-4	led_1_option	R/W	1b	Controlls LED_1 sources (same as bits 3:0)
3-0	led_0_option	R/W	0b	Controlls LED_0 source: 0b = link OK 1b = link OK + blink on TX/RX activity 10b = link OK + blink on TX activity 11b = link OK + blink on RX activity 100b = link OK + 100Base-T1 Master 101b = link OK + 100Base-T1 Slave 110b = TX/RX activity with stretch option 111b = Reserved 1000b = Reserved 1001b = Link lost (remains on until register 0x1 is read) 1010b = PRBS error (toggles on error) 1011b = XMII TX/RX Error with stretch option

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8.6.2.43 LEDS_CFG_2 Register (Address = 451h) [Reset = 0049h]

LEDS_CFG_2 is shown in Figure 8-62 and described in Table 8-71.

Return to the Table 8-27.

Figure 8-62. LEDS_CFG_2 Register

15	14	13	12	11	10	9	8
clk_o_gpio_ctrl_3	led_1_gpio_ctrl_3	led_0_gpio_ctrl_3	RESERVED				led_2_drv_en
R/W-0b	R/W-0b	R/W-0b	R-0b				R/W-0b
7	6	5	4	3	2	1	0
led_2_drv_val	led_2_polarity	led_1_drv_en	led_1_drv_val	led_1_polarity	led_0_drv_en	led_0_drv_val	led_0_polarity
R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-1b

Table 8-71. LEDS_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	clk_o_gpio_ctrl_3	R/W	0b	MSB of CLKOUT gpio control. This bit provides additional options for configuring CLKOUT If set to 1, it changes the effect ofclk_o_gpio_ctrl bits of 0x453 Reg 0x453[2:0] will control CLKOUT as follows 0b = pwr_seq_done 1b = loc_wake_req from analog 10b = loc_wake_req to PHY control 11b = tx_lps_done 100b = tx_lps_done_64 101b = tx_lps 110b = pcs rx sm - receiving 111b = pcs tx sm - tx_enable
14	led_1_gpio_ctrl_3	R/W	0b	MSB of LED_1 gpio control. This bit provides additional options for configuring LED_0 If set to 1, it changes the effect of led_1_gpio_ctrl bits of 0x452 Reg 0x452[10:8] will control LED_1 as follows 0b = pwr_seq_done 1b = loc_wake_req from analog 10b = loc_wake_req to PHY control 11b = tx_lps_done 100b = tx_lps_done_64 101b = tx_lps 110b = pcs rx sm - receiving 111b = pcs tx sm - tx_enable
13	led_0_gpio_ctrl_3	R/W	0b	MSB of LED_0 gpio control. This bit provides additional options for configuring LED_0 If set to 1, it changes the effect of led_0_gpio_ctrl bits of 0x452 Reg 0x452[2:0] will control LED_0 as follows 0b = pwr_seq_done 1b = loc_wake_req from analog 10b = loc_wake_req to PHY control 11b = tx_lps_done 100b = tx_lps_done_64 101b = tx_lps 110b = pcs rx sm - receiving 111b = pcs tx sm - tx_enable
12-9	RESERVED	R	0b	Reserved
8	led_2_drv_en	R/W	0b	0b = LED_2 is in normal operation mode 1b = Drive the value of LED_2 (driven value is bit 7)
7	led_2_drv_val	R/W	0b	If bit #8 is set, this is the value of LED_2 Note: There is no LED_2, only if CLK_OUT is configured as LED_2
6	led_2_polarity	R/W	1b	LED_2 polarity. Note: There is no LED_2, only if CLK_OUT is configured as LED_2 0b = Active low 1b = Active high

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Table 8-71. LEDS_CFG_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	led_1_drv_en	R/W	0b	Note: There is no LED_2, only if CLK_OUT is configured as LED_2 0b = LED_1 is in normal operation mode 1b = Drive the value of LED_1 (driven value is bit #4)
4	led_1_drv_val	R/W	0b	If bit #5 is set, this is the value of LED_1
3	led_1_polarity	R/W	1b	LED_1 polarity: if(RX_D3_strap == 1) reset_val = ~CLKOUT_strap else reset_val = ~LED_1_strap 0b = Active low 1b = Active high
2	led_0_drv_en	R/W	0b	0 - LED_0 is in normal operation mode 1 - Drive the value of LED_0 (driven value is bit #1)
1	led_0_drv_val	R/W	0b	If bit #2 is set, this is the value of LED_1
0	led_0_polarity	R/W	1b	LED_0 polarity: reset_val = ~LED_0_strap 0b = Active low 1b = Active high

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8.6.2.44 IO_MUX_CFG_1 Register (Address = 452h) [Reset = 0000h]

IO_MUX_CFG_1 is shown in Figure 8-63 and described in Table 8-72.

Return to the Table 8-27.

Figure 8-63. IO_MUX_CFG_1 Register

15	14	13	12	11	10	9	8
led_1_clk_div_2_en	led_1_clk_source			led_1_clk_inv_en	led_1_gpio_ctrl		
R/W-0b	R/W-0b			R/W-0b	R/W-0b		
7	6	5	4	3	2	1	0
led_0_clk_div_2_en	led_0_clk_source			led_0_clk_inv_en	led_0_gpio_ctrl		
R/W-0b	R/W-0b			R/W-0b	R/W-0b		

Table 8-72. IO_MUX_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	led_1_clk_div_2_en	R/W	0b	If led_1_gpio is configured to led_1_clk_source, Selects divide by 2 of clock at led_1_clk_source
14-12	led_1_clk_source	R/W	0b	In case clk_out is MUXed to LED_1 IO, this field controls clk_out source: 000b - XI clock 001b - 200M pll clock 010b - 67 MHz ADC clock (recovered) 011b - Free 200MHz clock 100b - 25M MII clock derived from 200M LD clock 101b - 25MHz clock to PLL (XI or XI/2) or POR clock 110b - Core 100 MHz clock 111b - 67 MHz DSP clock (recovered, 1/3 duty cycle)
11	led_1_clk_inv_en	R/W	0b	If led_1_gpio is configured to led_1_clk_source, Selects inversion of clock at led_1_clk_source

10-8	led_1_gpio_ctrl	R/W	0b	controls the output of LED_1 IO:
				000b - LED_1 (default: LINK + ACT)
				001b - LED_1 Clock mux out
				010b - WoL
				011b - Under-Voltage indication
				100b - 1588 TX
				101b - 1588 RX
				110b - ESD
				111b - interrupt
				if(RX_D3_strap ==1)
				reset_val = 3'b001
				else
				reset_val = 3'b000

7	led_0_clk_div_2_en	R/W	0b	If led_0_gpio is configured to led_0_clk_source, Selects divide by 2 of clock at led_0_clk_source
6-4	led_0_clk_source	R/W	0b	In case clk_out is MUXed to LED_0 IO, this field controls clk_out source: 0b = XI clock 1b = 200M pll clock 10b = 67 MHz ADC clock (recovered) 11b = Free 200MHz clock 100b = 25M MII clock derived from 200M LD clock 101b = 25MHz clock to PLL (XI or XI/2) or POR clock 110b = Core 100 MHz clock 111b = 67 MHz DSP clock (recovered, 1/3 duty cycle)
3	led_0_clk_inv_en	R/W	0b	If led_0_gpio is configured to led_0_clk_source, Selects inversion of clock at led_0_clk_source

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Table 8-72. IO_MUX_CFG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	led_0_gpio_ctrl	R/W	0b	controls the output of LED_0 IO: 0b = LED_0 (default: LINK) 001b =LED_0 Clock mux out 010b = WoL 011b = Under-Voltage indication 100b = 1588 TX 101b = 1588 RX 110b = ESD 111b = interrupt

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8.6.2.45 IO_MUX_CFG_2 Register (Address = 453h) [Reset = 0001h]

IO_MUX_CFG_2 is shown in Figure 8-64 and described in Table 8-73.

Return to the Table 8-27.

Figure 8-64. IO_MUX_CFG_2 Register

15	14	13	12	11	10	9	8
cfg_tx_er_on_led1	RESERVED						clk_o_clk_div_2_en
R/W-0b	R-0b						R/W-0b
7	6	5	4	3	2	1	0
clk_o_clk_source				clk_o_clk_inv_en	clk_o_gpio_ctrl		
R/W-0b				R/W-0b	R/W-1b		

Table 8-73. IO_MUX_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_tx_er_on_led1	R/W	0b	configures led_1 pin to tx_er pin and LED_1 pin is made input
14-9	RESERVED	R	0b	Reserved
8	clk_o_clk_div_2_en	R/W	0b	If clk_out is configured to output clk_o_clk_source, Selects divide by 2 of clock at clk_o_clk_source
7-4	clk_o_clk_source	R/W	0b	In case clk_out is MUXed to CLK_O IO, this field controls clk_out source: 0000b - XI clock 0001b - 200M pll clock 0010b - 67 MHz ADC clock (recovered) 0011b - Free 200MHz clock 0100b - 25M MII clock derived from 200M LD clock 0101b - 25MHz clock to PLL (XI or XI/2) or POR clock 0110b - Core 100 MHz clock 0111b - 67 MHz DSP clock (recovered, 1/3 duty cycle) 1000b - CLK25_50 (50 MHz in RMII, 25 MHz in others) 1001b - 50M RMII RX clk 1010b - SGMII serlz clk 1011b - SGMII deserlz clk 1100b - 30ns tick 1101b - 40ns tick 1110b - DLL TX CLK 1111b - DLL RX CLK
3	clk_o_clk_inv_en	R/W	0b	If clk_out is configured to output clk_o_clk_source, Selects inversion of clock at clk_o_clk_source

2-0	clk_o_gpio_ctrl	R/W	1b	controls the output of CLK_O IO:
				000b - LED_1
				001b - CLKOUT Clock mux out
				010b - WoL
				011b - Under-Voltage indication
				100b - 1588 TX
				101b - 1588 RX
				110b - ESD
				111b - interrupt
				Automatically gets configured
				to 3 'h0 if pin6(LED_1) is strapped
				As daisy chain CLKOUT
				if(RX_D3_strap ==1)
				reset_val = 3'b000
				else
				reset_val = 3'b001

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8.6.2.46 IO_MUX_CFG Register (Address = 456h) [Reset = 0000h]

IO_MUX_CFG is shown in Figure 8-65 and described in Table 8-74.

Return to the Table 8-27.

Figure 8-65. IO_MUX_CFG Register

15	14	13	12	11	10	9	8
rx_pins_pupd_value		rx_pins_pupd_force_control	tx_pins_pupd_value		tx_pins_pupd_force_control	mac_rx_impedance_ctrl	
R/W-0b		R/W-0b	R/W-0b		R/W-0b	R/W-0b	
7	6	5	4	3	2	1	0
mac_rx_impedance_ctrl			mac_tx_impedance_ctrl				
R/W-0b			R/W-0b				

Table 8-74. IO_MUX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	rx_pins_pupd_value	R/W	0b	when RX pins PUPD force control is enabled, PUPD is contolled by this register 0b = No pull 1b = Pull up 10b = Pull down 11b = Reserved
13	rx_pins_pupd_force_control	R/W	0b	enables PUPD force control on RX MAC pins 0b = No force control 1b = enables force control
12-11	tx_pins_pupd_value	R/W	0b	when TX pins PUPD force control is enabled, PUPD is contolled by this register 0b = No pull 1b = Pull up 10b = Pull down 11b = Reserved
10	tx_pins_pupd_force_control	R/W	0b	enables PUPD force control on TX MAC pins 0b = No force control 1b = enables force control
9-5	mac_rx_impedance_ctrl	R/W	0b	RX MAC interface PAD impedance control
4-0	mac_tx_impedance_ctrl	R/W	0b	TX MAC interface PAD impedance control

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8.6.2.47 IO_STATUS_1 Register (Address = 457h) [Reset = 0000h]

IO_STATUS_1 is shown in Figure 8-66 and described in Table 8-75.

Return to the Table 8-27.

Figure 8-66. IO_STATUS_1 Register

15	14	13	12	11	10	9	8
io_status_1							
R-0b							
7	6	5	4	3	2	1	0
io_status_1							
R-0b							

Table 8-75. IO_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	io_status_1	R	0b	If IO direction is controlled via register IO_MUX_CFG & IO_INPUT_MODE_1, and direction is INPUT (i.e. io_oe_n_force_ctrl=1, io_input_mode[*]=1) - shows the current value of the following IOs: bit 0 - RX_D3 bit 1 - TX_CLK bit 2 - TX_EN bit 3 - TX_D0 bit 4 - TX_D1 bit 5 - TX_D2 bit 6 - TX_D3 bit 7 - INT_N bit 8 - CLKOUT bit 9 - LED_0 bit 10 - RX_CLK bit 11 - RX_DV bit 12 - 0 bit 13 - RX_ERR bit 14 - LED_1 bit 15 - RX_D0

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8.6.2.48 IO_STATUS_2 Register (Address = 458h) [Reset = 0000h]

IO_STATUS_2 is shown in Figure 8-67 and described in Table 8-76.

Return to the Table 8-27.

Figure 8-67. IO_STATUS_2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED						io_status_2	
R-0b						R-0b	

Table 8-76. IO_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0b	Reserved
1-0	io_status_2	R	0b	"If IO direction is controlled via register IO_MUX_CFG & IO_INPUT_MODE_2, and direction is INPUT (i.e. io_oe_n_force_ctrl=1, io_input_mode[*]=1) - shows the current value of the following IOs: bit 0 - RX_D1 bit 1 - RX_D2 "

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8.6.2.49 CHIP_SOR_1 Register (Address = 45Dh) [Reset = 0000h]

CHIP_SOR_1 is shown in Figure 8-68 and described in Table 8-77.

Return to the Table 8-27.

Figure 8-68. CHIP_SOR_1 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	LED1_POR	RX_D3_POR	RESERVED	RESERVED	LED0_STRAP	RXD3_STRAP
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b
7	6	5	4	3	2	1	0
RXD2_STRAP	RXD1_STRAP	RXD0_STRAP	RXCLK_STRAP	RXER_STRAP		RXDV_STRAP	
R-0b	R-0b	R-0b	R-0b	R-0b		R-0b	

Table 8-77. CHIP_SOR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	
14	RESERVED	R	0b	Reserved
13	LED1_POR	R	0b	LED_1 strap sampled at power up
12	RX_D3_POR	R	0b	RX_D3 strap sampled at power up
11	RESERVED	R	0b	Reserved
10	RESERVED	R	0b	Reserved
9	LED0_STRAP	R	0b	LED_0 strap sampled at power up or reset
8	RXD3_STRAP	R	0b	RX_D3 strap sampled at reset
7	RXD2_STRAP	R	0b	RX_D2 strap sampled at power up or reset
6	RXD1_STRAP	R	0b	RX_D1 strap sampled at power up or reset
5	RXD0_STRAP	R	0b	RX_D0 strap sampled at power up or reset
4	RXCLK_STRAP	R	0b	RX_CLK strap sampled at power up or reset
3-2	RXER_STRAP	R	0b	RX_ER strap sampled at power up or reset
1-0	RXDV_STRAP	R	0b	RX_DV strap sampled at power up or reset

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8.6.2.50 LED1_CLKOUT_ANA_CTRL Register (Address = 45Fh) [Reset = 000Ch]

LED1_CLKOUT_ANA_CTRL is shown in Figure 8-69 and described in Table 8-78.

Return to the Table 8-27.

Figure 8-69. LED1_CLKOUT_ANA_CTRL Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED					
R/W-0b	R/W-0b	R-0b					
7	6	5	4	3	2	1	0
RESERVED			clkout_ana_sel_1p0v_sl	led_1_ana_mux_ctrl		clkout_ana_mux_ctrl	
R-0b			R/W-0b	R/W-11b		R/W-0b	

Table 8-78. LED1_CLKOUT_ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0b	Reserved
14	RESERVED	R/W	0b	Reserved
13-5	RESERVED	R	0b	Reserved
4	clkout_ana_sel_1p0v_sl	R/W	0b	For selecting test line b/w analog test clocks
3-2	led_1_ana_mux_ctrl	R/W	11b	Selects the signal to be sent out on LED_1 pin Automatically selects output from digital if Pin6(LED_1) is strapped As daisy chain CLKOUT if(RX_D3_strap == 1) reset_val = 2'b00 else reset_val = 2'b11 0b = Daisy chain clock 1b = TX_TCLK for test modes 10b = ANA Test clock 11b = clkout_out_1p0v_sl from digital
1-0	clkout_ana_mux_ctrl	R/W	0b	Selects the signal to be sent out on CLKOUT pin Automatically selects output from digital if Pin6(LED_1) is strapped As daisy chain CLKOUT if(RX_D3_strap == 1) reset_val = 2'b11 else reset_val = 2'b00 0b = Daisy chain clock 1b = TX_TCLK for test modes 10b = ANA Test clock 11b = clkout_out_1p0v_sl from digital

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8.6.2.51 PCS_CTRL_1 Register (Address = 485h) [Reset = 1078h]

PCS_CTRL_1 is shown in Figure 8-70 and described in Table 8-79.

Return to the Table 8-27.

Figure 8-70. PCS_CTRL_1 Register

15	14	13	12	11	10	9	8
RESERVED	cfg_force_slave_phase1_done	cfg_dis_ipg_scr_lock_check	cfg_link_control	RESERVED			cfg_desc_first_lock_count
R-0b	R/W-0b	R/W-0b	R/W-1b	R-0b			R/W-1111000b
7	6	5	4	3	2	1	0
cfg_desc_first_lock_count							
R/W-1111000b							

Table 8-79. PCS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved
14	cfg_force_slave_phase1_done	R/W	0b	Force to say phase1 of DSP slave training done
13	cfg_dis_ipg_scr_lock_check	R/W	0b	Disable scrambler lock check during IPG
12	cfg_link_control	R/W	1b	Enable for the entire training/linkup to start
11-9	RESERVED	R	0b	Reserved
8-0	cfg_desc_first_lock_count	R/W	1111000b	Number of idle symbols to decide on scrambler lock

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8.6.2.52 PCS_CTRL_2 Register (Address = 486h) [Reset = 0A05h]

PCS_CTRL_2 is shown in Figure 8-71 and described in Table 8-80.

Return to the Table 8-27.

Figure 8-71. PCS_CTRL_2 Register

15	14	13	12	11	10	9	8
cfg_desc_error_count							
R/W-1010b							
7	6	5	4	3	2	1	0
RESERVED			cfg_rem_rcvr_sts_error_cnt				
R-0b			R/W-101b				

Table 8-80. PCS_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_desc_error_count	R/W	1010b	Number of non-idle ymbols to look for to say scrambler unlocked
7-5	RESERVED	R	0b	Reserved
4-0	cfg_rem_rcvr_sts_error_cnt	R/W	101b	No of error symbols to rem rcvr status to go low

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8.6.2.53 TX_INTER_CFG Register (Address = 489h) [Reset = 0001h]

TX_INTER_CFG is shown in Figure 8-72 and described in Table 8-81.

Return to the Table 8-27.

Figure 8-72. TX_INTER_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED					cfg_force_tx_interleave	cfg_tx_interleave_en	cfg_interleave_det_en
R-0b					R/W-0b	R/W-0b	R/W-1b

Table 8-81. TX_INTER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0b	Reserved
2	cfg_force_tx_interleave	R/W	0b	Force interleave on Tx
1	cfg_tx_interleave_en	R/W	0b	Enable interleave on tx, if interleave detected on the Rx 0b = Interleave on Tx disabled 1b = Interleave on Tx enabled if interleave detected on Rx
0	cfg_interleave_det_en	R/W	1b	Enable interleave detection 0b = Disable Interleave Detection 1b = Enable Interleave Detection

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8.6.2.54 JABBER_CFG Register (Address = 496h) [Reset = 044Ch]

JABBER_CFG is shown in Figure 8-73 and described in Table 8-82.

Return to the Table 8-27.

Figure 8-73. JABBER_CFG Register

15	14	13	12	11	10	9	8
RESERVED					cfg_rcv_jab_timer_val		
R-0b					R/W-10001001100b		
7	6	5	4	3	2	1	0
cfg_rcv_jab_timer_val							
R/W-10001001100b							

Table 8-82. JABBER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0b	Reserved
10-0	cfg_rcv_jab_timer_val	R/W	10001001100b	Jabber timeout count in usec

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8.6.2.55 TEST_MODE_CTRL Register (Address = 497h) [Reset = 01C0h]

TEST_MODE_CTRL is shown in Figure 8-74 and described in Table 8-83.

Return to the Table 8-27.

Figure 8-74. TEST_MODE_CTRL Register

15	14	13	12	11	10	9	8
RESERVED						cfg_test_mode1_symbol_cnt	
R-0b						R/W-11100b	
7	6	5	4	3	2	1	0
cfg_test_mode1_symbol_cnt				RESERVED			
R/W-11100b				R-0b			

Table 8-83. TEST_MODE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0b	Reserved
9-4	cfg_test_mode1_symbol_cnt	R/W	11100b	number of +1/-1 symbols to send in test_mode_1 N= 2 + 2* CFG_TEST_MODE1_SYMBOL_CNT
3-0	RESERVED	R	0b	Reserved

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8.6.2.56 RXF_CFG Register (Address = 4A0h) [Reset = 1000h]

RXF_CFG is shown in Figure 8-75 and described in Table 8-84.

Return to the Table 8-27.

Figure 8-75. RXF_CFG Register

15	14	13	12	11	10	9	8
bits_nibbles_swap		sfd_byte	RESERVED	RESERVED	RESERVED		RESERVED
R/W-0b		R/W-0b	R/W-1b	R/W-0b	R/W-0b		R/W-0b
7	6	5	4	3	2	1	0
enhanced_mac_support	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b

Table 8-84. RXF_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	bits_nibbles_swap	R/W	0b	Option to swap bits / nibbles inside every RX data byte 0b = regular order, no swaps - RXD[3-0] 1b = swap bits order - RXD[0-3] 1010b = swap nibbles order - { RXD[3-0] , RXD[7-4] } 1011b = swap bits order in each nibble - { RXD[4-7] , RXD[0-3] }
13	sfd_byte	R/W	0b	0 - SFD is 0xD5 (i.e. RXF module searchs 0xD5) 1 - SFD is 0x5D (i.e. RXF module searchs 0x5D) 0b = SFD is 0xD5 (i.e. RXF module searchs 0xD5) 1b = SFD is 0x5D (i.e. RXF module searchs 0x5D)
12	RESERVED	R/W	1b	Reserved
11	RESERVED	R/W	0b	Reserved
10-9	RESERVED	R/W	0b	Reserved
8	RESERVED	R/W	0b	Reserved
7	enhanced_mac_support	R/W	0b	Enables enhanced RX features. This bit shall be set when using wakeup abilities, CRC check or RX 1588 indication
6	RESERVED	R/W	0b	Reserved
5	RESERVED	R/W	0b	Reserved
4	RESERVED	R/W	0b	Reserved
3	RESERVED	R/W	0b	Reserved
2	RESERVED	R/W	0b	Reserved
1	RESERVED	R	0b	Reserved
0	RESERVED	R/W	0b	Reserved

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8.6.2.57 PG_REG_4 Register (Address = 553h) [Reset = 0000h]

PG_REG_4 is shown in Figure 8-76 and described in Table 8-85.

Return to the Table 8-27.

Figure 8-76. PG_REG_4 Register

15	14	13	12	11	10	9	8
RESERVED		force_pol_en	force_pol_val	RESERVED			
R/W-0b		R/W-0b	R/W-0b	R/W-0b			
7	6	5	4	3	2	1	0
RESERVED							
R/W-0b							

Table 8-85. PG_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0b	Reserved
13	force_pol_en	R/W	0b	Enable force on polarity 0b = Auto-polarity on MDI 1b = Force polarity on MDI
12	force_pol_val	R/W	0b	Polarity force value. Only valid if bit [13] is 1. 0b = Forced Normal polarity 1b = Forced Inverted polarity
11-0	RESERVED	R/W	0b	Reserved

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8.6.2.58 TC1_CFG_RW Register (Address = 560h) [Reset = 07E4h]

TC1_CFG_RW is shown in Figure 8-77 and described in Table 8-86.

Return to the Table 8-27.

Figure 8-77. TC1_CFG_RW Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED	cfg_link_status_metric		cfg_link_failure_multihot		
R-0b		R/W-0b	R/W-0b		R/W-111111b		
7	6	5	4	3	2	1	0
cfg_link_failure_multihot			cfg_comm_timer_thrs		cfg_bad_sqi_thrs		
R/W-111111b			R/W-0b		R/W-100b		

Table 8-86. TC1_CFG_RW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13	RESERVED	R/W	0b	Reserved
12-11	cfg_link_status_metric	R/W	0b	selects following link up signals as defined by C&S 0b = link_up_c_and_s 1b = link_montor_status 10b = (phy_control = SEND_DATA) 11b = comm_ready from TC1 spec
10-5	cfg_link_failure_multihot	R/W	111111b	each bit enables logging of link failure in the given scenario: bit[5] - SQI greater than configured thershold in register cfg_bad_sqi_thrs bit[6] - RCV_JABBER_DET5 - BAD_SSD bit[7] - LINK_FAILED bit[8] - RX_ERROR bit[9] - BAD_END bit[10] - RESERVED
4-3	cfg_comm_timer_thrs	R/W	0b	selects the hysteresis timer value for TC1 comm ready 0b = 2ms 1b = 500us 10b = 1ms 11b = 4ms
2-0	cfg_bad_sqi_thrs	R/W	100b	SQI threshold used to increment Link Failure Count defined by TC1. Whenever SQI becomes worse than the threshold, link failure count (Register 0x0561 bit[9:0]) as defined by TC1 is incremented

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8.6.2.59 TC1_LINK_FAIL_LOSS Register (Address = 561h) [Reset = 0000h]

TC1_LINK_FAIL_LOSS is shown in Figure 8-78 and described in Table 8-87.

Return to the Table 8-27.

Figure 8-78. TC1_LINK_FAIL_LOSS Register

15	14	13	12	11	10	9	8
link_losses						link_failures	
R-0b						R-0b	
7	6	5	4	3	2	1	0
link_failures							
R-0b							

Table 8-87. TC1_LINK_FAIL_LOSS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	link_losses	R	0b	Number of Link Losses occurred since last power cycle (as per TC1 specification)
9-0	link_failures	R	0b	Number of Link Failures causing NOT a link loss since last power cycle (as per TC1 specification)

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8.6.2.60 TC1_LINK_TRAINING_TIME Register (Address = 562h) [Reset = 0000h]

TC1_LINK_TRAINING_TIME is shown in Figure 8-79 and described in Table 8-88.

Return to the Table 8-27.

Figure 8-79. TC1_LINK_TRAINING_TIME Register

15	14	13	12	11	10	9	8
comm_ready	RESERVED						
R-0b	R-0b						
7	6	5	4	3	2	1	0
lq_ltt							
R-0b							

Table 8-88. TC1_LINK_TRAINING_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
15	comm_ready	R	0b	TC1 comm ready signal (Optimized link status indication for higher Layers to indicate if communication is possible via link) 0b = Communication Not Possible 1b = Communication Possible
14-8	RESERVED	R	0b	Reserved
7-0	lq_ltt	R	0b	Link training time of the last link training (as per TC1 specification)

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8.6.2.61 RGMII_CTRL Register (Address = 600h) [Reset = 0030h]

RGMII_CTRL is shown in Figure 8-80 and described in Table 8-89.

Return to the Table 8-27.

Figure 8-80. RGMII_CTRL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED	rgmii_tx_half_full_th			cfg_rgmii_en	inv_rgmii_txd	inv_rgmii_rxd	sup_tx_err_fd_rgmii
R-0b	R/W-11b			R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-89. RGMII_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0b	Reserved
6-4	rgmii_tx_half_full_th	R/W	11b	RGMII TX sync FIFO half full threshold in number if nibbles
3	cfg_rgmii_en	R/W	0b	RGMII enable bit Default from strap if(RX_D2_strap == 1) reset_val = 1 else reset_val = 0 0b = RGMII disable 1b = RGMII enable
2	inv_rgmii_txd	R/W	0b	Invert RGMII Tx wire order - full swap [3:0] -- [0:3]
1	inv_rgmii_rxd	R/W	0b	Invert RGMII Rx wire order - full swap [3:0] -- [0:3]
0	sup_tx_err_fd_rgmii	R/W	0b	this bit can disable the TX_ERR indication input

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8.6.2.62 RGMII_FIFO_STATUS Register (Address = 601h) [Reset = 0000h]

RGMII_FIFO_STATUS is shown in Figure 8-81 and described in Table 8-90.

Return to the Table 8-27.

Figure 8-81. RGMII_FIFO_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED						rgmii_tx_af_full_err	rgmii_tx_af_empty_err
R-0b						R-0b	R-0b

Table 8-90. RGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0b	Reserved
1	rgmii_tx_af_full_err	R	0b	RGMII Tx fifo full error
0	rgmii_tx_af_empty_err	R	0b	RGMII Tx fifo empty error

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8.6.2.63 RGMII_CLK_SHIFT_CTRL Register (Address = 602h) [Reset = 0000h]

RGMII_CLK_SHIFT_CTRL is shown in Figure 8-82 and described in Table 8-91.

Return to the Table 8-27.

Figure 8-82. RGMII_CLK_SHIFT_CTRL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED						cfg_rgmii_rx_clk_shift_sel	cfg_rgmii_tx_clk_shift_sel
R-0b						R/W-0b	R/W-0b

Table 8-91. RGMII_CLK_SHIFT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0b	Reserved
1	cfg_rgmii_rx_clk_shift_sel	R/W	0b	0: clock and data are aligned 1: clock on PIN is delayed by 90 degrees relative to RGMII_RX data if({RX_D2_strap, RX_D1_strap} == 2'b11) reset_val = 1 else resett_val = 0 0b = clock and data are aligned 1b = clock on PIN is delayed by 90 degrees relative to RGMII_RX data
0	cfg_rgmii_tx_clk_shift_sel	R/W	0b	use this mode when RGMII_TX_CLK & RGMII_TXD are aligned if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3'b101) reset_val = 1 else if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3'b110) reset_val = 1 else reset_val = 0

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8.6.2.64 RGMII_EEE_CTRL Register (Address = 603h) [Reset = 0000h]

RGMII_EEE_CTRL is shown in Figure 8-83 and described in Table 8-92.

Return to the Table 8-27.

Figure 8-83. RGMII_EEE_CTRL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED							cfg_rgmii_wake_signaling_en
R-0b							R/W-0b

Table 8-92. RGMII_EEE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0b	Reserved
1-0	cfg_rgmii_wake_signaling_en	R/W	0b	RGMII signaling behavior during exit LPI period. Bit[1] - exhibit rx_err on rx_ctrl for lpi_exit, else rx_ctrl is zero for both lpi and exit_lpi periods. Bit[0] - exhibit zeros on rxd for lpi_exit, else rxd=IB_code Note: option 00b is not supported, non-valid coding.

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8.6.2.65 SGMII_CTRL_1 Register (Address = 608h) [Reset = 007Bh]

SGMII_CTRL_1 is shown in Figure 8-84 and described in Table 8-93.

Return to the Table 8-27.

Figure 8-84. SGMII_CTRL_1 Register

15	14	13	12	11	10	9	8
sgmii_tx_err_dis	cfg_align_idx_force_en	cfg_align_idx_value				cfg_sgmii_en	cfg_sgmii_rx_pol_invert
R/W-0b	R/W-0b	R/W-0b				R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
cfg_sgmii_tx_pol_invert	serdes_tx_bits_order		serdes_rx_bits_order	cfg_sgmii_align_pkt_en	sgmii_autoneg_timer		sgmii_autoneg_en
R/W-0b	R/W-11b		R/W-1b	R/W-1b	R/W-1b		R/W-1b

Table 8-93. SGMII_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	sgmii_tx_err_dis	R/W	0b	SGMII TX err disable bit
14	cfg_align_idx_force_en	R/W	0b	Force word boundray index selection
13-10	cfg_align_idx_value	R/W	0b	when cfg_align_idx_force is set,This value set the iword boundray index
9	cfg_sgmii_en	R/W	0b	SGMII enable bit Default from strap if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3'b000) reset_val = 1 else reset_val = 0 0b = SGMII MAC i/f disabled 1b = SGMII MAC i/f enabled
8	cfg_sgmii_rx_pol_invert	R/W	0b	SGMII RX bus invert polarity
7	cfg_sgmii_tx_pol_invert	R/W	0b	SGMII TX bus invert polarity
6-5	serdes_tx_bits_order	R/W	11b	SERDES TX bits order (input to digital core)
4	serdes_rx_bits_order	R/W	1b	SERDES RX bits order (output of digital core) : 0 - MSB-first (default) 1 - LSB-first (reversed order)
3	cfg_sgmii_align_pkt_en	R/W	1b	For aligning the start of read out TX packet (towards serializer) w/ tx_even pulse. To sync with the Code_Group/OSET FSM code slots. Default is '1', when using '0' we go back to Gemini code
2-1	sgmii_autoneg_timer	R/W	1b	Selects duration of SGMII Auto-Negotiation timer 0b = 1.6ms 1b = 2us 10b = 800us 11b = 11ms
0	sgmii_autoneg_en	R/W	1b	sgmii auto negotiation enable 0b = SGMII autoneg disabled 1b = SGMII autoneg enabled

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8.6.2.66 SGMII_EEE_CTRL_1 Register (Address = 609h) [Reset = 0000h]

SGMII_EEE_CTRL_1 is shown in Figure 8-85 and described in Table 8-94.

Return to the Table 8-27.

Figure 8-85. SGMII_EEE_CTRL_1 Register

15	14	13	12	11	10	9	8
cfg_sgmii_tx_tr_timer_val					cfg_sgmii_tx_tq_timer_val		
R/W-0b					R/W-0b		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
cfg_sgmii_tx_tq_timer_val		cfg_sgmii_tx_ts_timer_val					cfg_support_non_eee_mac_sgmii_en
R/W-0b		R/W-0b					R/W-0b

Table 8-94. SGMII_EEE_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	cfg_sgmii_tx_tr_timer_val	R/W	0b	
10-6	cfg_sgmii_tx_tq_timer_val	R/W	0b	
5-1	cfg_sgmii_tx_ts_timer_val	R/W	0b	
0	cfg_support_non_eee_mac_sgmii_en	R/W	0b	special mode to support non sgmii eee mac in eee mode in the phy

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8.6.2.67 SGMII_STATUS Register (Address = 60Ah) [Reset = 0000h]

SGMII_STATUS is shown in Figure 8-86 and described in Table 8-95.

Return to the Table 8-27.

Figure 8-86. SGMII_STATUS Register

15	14	13	12	11	10	9	8
RESERVED			sgmii_page_received	link_status_1000bx	sgmii_autoneg_complete	cfg_align_en	cfg_sync_status
R-0b			R-0b	R-0b	R-0b	R-0b	R-0b
7	6	5	4	3	2	1	0
cfg_align_idx				RESERVED			
R-0b				R-0b			

Table 8-95. SGMII_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12	sgmii_page_received	R	0b	Clear on read bit. Indicates that a new auto neg page was received
11	link_status_1000bx	R	0b	sgmii link status 0b = SGMII link is down 1b = SGMII link is up
10	sgmii_autoneg_complete	R	0b	sgmii autoneg complete indication 0b = SGMII autoneg incomplete 1b = SGMII autoneg completed
9	cfg_align_en	R	0b	word boundary FSM - align indication
8	cfg_sync_status	R	0b	word boundary FSM - sync status indication
7-4	cfg_align_idx	R	0b	word boundary index selection
3-0	RESERVED	R	0b	Reserved

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8.6.2.68 SGMII_EEE_CTRL_2 Register (Address = 60Bh) [Reset = 0005h]

SGMII_EEE_CTRL_2 is shown in Figure 8-87 and described in Table 8-96.

Return to the Table 8-27.

Figure 8-87. SGMII_EEE_CTRL_2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED				cfg_sgmii_rx_quiet_timer_val			
R-0b				R/W-101b			

Table 8-96. SGMII_EEE_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0b	Reserved
3-0	cfg_sgmii_rx_quiet_timer_val	R/W	101b	Configures the RX Quiet Timer Value. Timer Value = (3100 + code*100)us

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8.6.2.69 SGMII_CTRL_2 Register (Address = 60Ch) [Reset = 0024h]

SGMII_CTRL_2 is shown in Figure 8-88 and described in Table 8-97.

Return to the Table 8-27.

Figure 8-88. SGMII_CTRL_2 Register

15	14	13	12	11	10	9	8
RESERVED							sgmii_cdr_lock_force_val
R-0b							R/W-0b
7	6	5	4	3	2	1	0
sgmii_cdr_lock_force_ctrl	sgmii_mr_restart_an	tx_half_full_th			rx_half_full_th		
R/W-0b	RH/W1S-0b	R/W-100b			R/W-100b		

Table 8-97. SGMII_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0b	Reserved
8	sgmii_cdr_lock_force_val	R/W	0b	SGMII cdr lock force value
7	sgmii_cdr_lock_force_ctrl	R/W	0b	SGMII cdr lock force enable
6	sgmii_mr_restart_an	RH/W1S	0b	Restart sgmii autonegotiation
5-3	tx_half_full_th	R/W	100b	SGMII TX sync FIFO half full threshold
2-0	rx_half_full_th	R/W	100b	SGMII RX sync FIFO half full threshold

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8.6.2.70 SGMII_FIFO_STATUS Register (Address = 60Dh) [Reset = 0000h]

SGMII_FIFO_STATUS is shown in Figure 8-89 and described in Table 8-98.

Return to the Table 8-27.

Figure 8-89. SGMII_FIFO_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED				sgmii_rx_af_full_err	sgmii_rx_af_empty_err	sgmii_tx_af_full_err	sgmii_tx_af_empty_err
R-0b				H-0b	H-0b	H-0b	H-0b

Table 8-98. SGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0b	Reserved
3	sgmii_rx_af_full_err	H	0b	SGMII RX fifo full error 0b = No error indication 1b = SGMII RX fifo full error has been indicated
2	sgmii_rx_af_empty_err	H	0b	SGMII RX fifo empty error 0b = No error indication 1b = SGMII RX fifo empty error has been indicated
1	sgmii_tx_af_full_err	H	0b	SGMII TX fifo full error 0b = No error indication 1b = SGMII TX fifo full error has been indicated
0	sgmii_tx_af_empty_err	H	0b	SGMII TX fiff empty error 0b = No error indication 1b = SGMII TX fifo empty error has been indicated

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8.6.2.71 PRBS_STATUS_1 Register (Address = 618h) [Reset = 0000h]

PRBS_STATUS_1 is shown in Figure 8-90 and described in Table 8-99.

Return to the Table 8-27.

Figure 8-90. PRBS_STATUS_1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
prbs_err_ov_cnt							
R-0b							

Table 8-99. PRBS_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-0	prbs_err_ov_cnt	R	0b	Holds number of error counter overflow that received by the PRBS checker. Value in this register is locked when write is done to register 0x001B bit[0] or bit[1]. Counter stops on 0xFF. Note: when PRBS counters work in single mode, overflow counter is not active

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8.6.2.72 PRBS_CTRL_1 Register (Address = 619h) [Reset = 0574h]

PRBS_CTRL_1 is shown in Figure 8-91 and described in Table 8-100.

Return to the Table 8-27.

Figure 8-91. PRBS_CTRL_1 Register

15	14	13	12	11	10	9	8
RESERVED		cfg_pkt_gen_64	send_pkt	RESERVED	cfg_prbs_chk_sel		
R-0b		R/W-0b	RH/W1S-0b	R-0b	R/W-101b		
7	6	5	4	3	2	1	0
RESERVED	cfg_prbs_gen_sel			cfg_prbs_cnt_mode	cfg_prbs_chk_enable	cfg_pkt_gen_prbs	pkt_gen_en
R-0b	R/W-111b			R/W-0b	R/W-1b	R/W-0b	R/W-0b

Table 8-100. PRBS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13	cfg_pkt_gen_64	R/W	0b	0b = Transmit 1518 byte packets in packet generation mode 1b = Transmit 64 byte packets in packet generation mode
12	send_pkt	RH/W1S	0b	Enables generating MAC packet with fix/incremental data w CRC (pkt_gen_en has to be set and cfg_pkt_gen_prbs has to be clear) Cleared automatically when pkt_done is set
11	RESERVED	R	0b	Reserved
10-8	cfg_prbs_chk_sel	R/W	101b	000 : Checker receives from RGMII TX 001 : Checker receives from SGMII TX 010 : Checker receives from RMII RX 011 : Checker receives from MII 101 : Checker receives from Cu RX 110 : Reserved 111 : Reserved
7	RESERVED	R	0b	Reserved
6-4	cfg_prbs_gen_sel	R/W	111b	000 : PRBS transmits to RGMII RX 001 : PRBS transmits to SGMII RX 010 : PRBS transmits to RMII RX 011 : PRBS transmits to MII RX 101 : PRBS transmits to Cu TX 110 : Reserved 111 : Reserved
3	cfg_prbs_cnt_mode	R/W	0b	0b = Single mode, When one of the PRBS counters reaches max value, PRBS checker stops counting. 1b = Continuous mode, when one of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again
2	cfg_prbs_chk_enable	R/W	1b	Enable PRBS checker
1	cfg_pkt_gen_prbs	R/W	0b	If set: (1) When pkt_gen_en is set, PRBS packets are generated continuously (3) When pkt_gen_en is cleared, PRBS RX checker is still enabled If cleared: (1) When pkt_gen_en is set, non - PRBS packet is generated (3) When pkt_gen_en is cleared, PRBS RX checker is disabled as well
0	pkt_gen_en	R/W	0b	Enable/disable for prbs/packet generator 0b = Disable for prbs/packet generator 1b = Enable for prbs/packet generator

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8.6.2.73 PRBS_CTRL_2 Register (Address = 61Ah) [Reset = 05DCh]

PRBS_CTRL_2 is shown in Figure 8-92 and described in Table 8-101.

Return to the Table 8-27.

Figure 8-92. PRBS_CTRL_2 Register

15	14	13	12	11	10	9	8
cfg_pkt_len_prbs							
R/W-10111011100b							
7	6	5	4	3	2	1	0
cfg_pkt_len_prbs							
R/W-10111011100b							

Table 8-101. PRBS_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_pkt_len_prbs	R/W	1011101110 0b	Length (in bytes) of PRBS packets and MAC packets w CRC

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8.6.2.74 PRBS_CTRL_3 Register (Address = 61Bh) [Reset = 007Dh]

PRBS_CTRL_3 is shown in Figure 8-93 and described in Table 8-102.

Return to the Table 8-27.

Figure 8-93. PRBS_CTRL_3 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
cfg_ipg_len							
R/W-1111101b							

Table 8-102. PRBS_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-0	cfg_ipg_len	R/W	1111101b	Inter-packet gap (in bytes) between packets

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8.6.2.75 PRBS_STATUS_2 Register (Address = 61Ch) [Reset = 0000h]

PRBS_STATUS_2 is shown in Figure 8-94 and described in Table 8-103.

Return to the Table 8-27.

Figure 8-94. PRBS_STATUS_2 Register

15	14	13	12	11	10	9	8
prbs_byte_cnt							
R-0b							
7	6	5	4	3	2	1	0
prbs_byte_cnt							
R-0b							

Table 8-103. PRBS_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_byte_cnt	R	0b	Holds number of total bytes that received by the PRBS checker. Value in this register is locked when write is done to register 0x001B bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFF

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8.6.2.76 PRBS_STATUS_3 Register (Address = 61Dh) [Reset = 0000h]

PRBS_STATUS_3 is shown in Figure 8-95 and described in Table 8-104.

Return to the Table 8-27.

Figure 8-95. PRBS_STATUS_3 Register

15	14	13	12	11	10	9	8
prbs_pkt_cnt_15_0							
R-0b							
7	6	5	4	3	2	1	0
prbs_pkt_cnt_15_0							
R-0b							

Table 8-104. PRBS_STATUS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_pkt_cnt_15_0	R	0b	Bits [15:0] of number of total packets received by the PRBS checker Value in this register is locked when write is done to register 0x001B bit[15] or bit[14]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

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8.6.2.77 PRBS_STATUS_4 Register (Address = 61Eh) [Reset = 0000h]

PRBS_STATUS_4 is shown in Figure 8-96 and described in Table 8-105.

Return to the Table 8-27.

Figure 8-96. PRBS_STATUS_4 Register

15	14	13	12	11	10	9	8
prbs_pkt_cnt_31_16							
R-0b							
7	6	5	4	3	2	1	0
prbs_pkt_cnt_31_16							
R-0b							

Table 8-105. PRBS_STATUS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_pkt_cnt_31_16	R	0b	Bits [31:16] of number of total packets received by the PRBS checker Value in this register is locked when write is done to register 0x001B bit[15] or bit[14]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

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8.6.2.78 PRBS_STATUS_5 Register (Address = 620h) [Reset = 0000h]

PRBS_STATUS_5 is shown in Figure 8-97 and described in Table 8-106.

Return to the Table 8-27.

Figure 8-97. PRBS_STATUS_5 Register

15	14	13	12	11	10	9	8
RESERVED			pkt_done	pkt_gen_busy	prbs_pkt_ov	prbs_byte_ov	prbs_lock
R-0b			R-0b	R-0b	R-0b	R-0b	R-0b
7	6	5	4	3	2	1	0
prbs_err_cnt							
R-0b							

Table 8-106. PRBS_STATUS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12	pkt_done	R	0b	Set when all MAC packets w CRC are transmitted
11	pkt_gen_busy	R	0b	status of packet generator
10	prbs_pkt_ov	R	0b	If set, packet counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit[15] of 0x001B
9	prbs_byte_ov	R	0b	If set, bytes counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit[15] of 0x001B
8	prbs_lock	R	0b	prbs lock status
7-0	prbs_err_cnt	R	0b	Holds number of errored bytes that received by the PRBS checker Value in this register is locked when write is done to bit[0] or bit[1] When PRBS Count Mode set to zero, count stops on 0xFF Notes: Writing bit 0 generates a lock signal for the PRBS counters. Writing bit 1 generates a lock and clear signal for the PRBS counters

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8.6.2.79 PRBS_STATUS_6 Register (Address = 622h) [Reset = 0000h]

PRBS_STATUS_6 is shown in Figure 8-98 and described in Table 8-107.

Return to the Table 8-27.

Figure 8-98. PRBS_STATUS_6 Register

15	14	13	12	11	10	9	8
pkt_err_cnt_15_0							
R-0b							
7	6	5	4	3	2	1	0
pkt_err_cnt_15_0							
R-0b							

Table 8-107. PRBS_STATUS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pkt_err_cnt_15_0	R	0b	bits [15:0] of counter which records number or PRBS erroneous bytes received. This field gets cleared when bit[15] or bit[14] is written as 1 to register 0x001B

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8.6.2.80 PRBS_STATUS_7 Register (Address = 623h) [Reset = 0000h]

PRBS_STATUS_7 is shown in Figure 8-99 and described in Table 8-108.

Return to the Table 8-27.

Figure 8-99. PRBS_STATUS_7 Register

15	14	13	12	11	10	9	8
pkt_err_cnt_31_16							
R-0b							
7	6	5	4	3	2	1	0
pkt_err_cnt_31_16							
R-0b							

Table 8-108. PRBS_STATUS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pkt_err_cnt_31_16	R	0b	bits [31:16] of counter which records number or PRBS erroneous bytes received. This field gets cleared when bit[15] or bit[14] is written as 1 to register 0x001B

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8.6.2.81 PRBS_CTRL_4 Register (Address = 624h) [Reset = 5511h]

PRBS_CTRL_4 is shown in Figure 8-100 and described in Table 8-109.

Return to the Table 8-27.

Figure 8-100. PRBS_CTRL_4 Register

15	14	13	12	11	10	9	8
cfg_pkt_data							
R/W-1010101b							
7	6	5	4	3	2	1	0
cfg_pkt_mode		cfg_pattern_vld_bytes			cfg_pkt_cnt		
R/W-0b		R/W-10b			R/W-1b		

Table 8-109. PRBS_CTRL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_pkt_data	R/W	1010101b	Fixed data to be sent in Fix data mode
7-6	cfg_pkt_mode	R/W	0b	Selects the type of data sent 0b = Incremental Data 1b = Fixed Data 10b = PRBS Data (Random Data) 11b = PRBS Data (Random Data)
5-3	cfg_pattern_vld_bytes	R/W	10b	Number of bytes of valid pattern in packet (Max - 6)
2-0	cfg_pkt_cnt	R/W	1b	Configures the number of MAC packets to be transmitted by packet generator 0b = 1 packet 1b = 10 packets 10b = 100 packets 11b = 1000 packets 100b = 10000 packets 101b = 100000 packets 110b = 1000000 packets 111b = Continuous packets

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8.6.2.82 PATTERN_CTRL_1 Register (Address = 625h) [Reset = 0000h]

PATTERN_CTRL_1 is shown in Figure 8-101 and described in Table 8-110.

Return to the Table 8-27.

Figure 8-101. PATTERN_CTRL_1 Register

15	14	13	12	11	10	9	8
pattern_15_0							
R/W-0b							
7	6	5	4	3	2	1	0
pattern_15_0							
R/W-0b							

Table 8-110. PATTERN_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_15_0	R/W	0b	Bits 15:0 of pattern

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8.6.2.83 PATTERN_CTRL_2 Register (Address = 626h) [Reset = 0000h]

PATTERN_CTRL_2 is shown in Figure 8-102 and described in Table 8-111.

Return to the Table 8-27.

Figure 8-102. PATTERN_CTRL_2 Register

15	14	13	12	11	10	9	8
pattern_31_16							
R/W-0b							
7	6	5	4	3	2	1	0
pattern_31_16							
R/W-0b							

Table 8-111. PATTERN_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_31_16	R/W	0b	Bits 31:16 of pattern

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8.6.2.84 PATTERN_CTRL_3 Register (Address = 627h) [Reset = 0000h]

PATTERN_CTRL_3 is shown in Figure 8-103 and described in Table 8-112.

Return to the Table 8-27.

Figure 8-103. PATTERN_CTRL_3 Register

15	14	13	12	11	10	9	8
pattern_47_32							
R/W-0b							
7	6	5	4	3	2	1	0
pattern_47_32							
R/W-0b							

Table 8-112. PATTERN_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_47_32	R/W	0b	Bits 47:32 of pattern

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8.6.2.85 PMATCH_CTRL_1 Register (Address = 628h) [Reset = 0000h]

PMATCH_CTRL_1 is shown in Figure 8-104 and described in Table 8-113.

Return to the Table 8-27.

Figure 8-104. PMATCH_CTRL_1 Register

15	14	13	12	11	10	9	8
pmatch_data_15_0							
R/W-0b							
7	6	5	4	3	2	1	0
pmatch_data_15_0							
R/W-0b							

Table 8-113. PMATCH_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_15_0	R/W	0b	Bits 15:0 of Perfect Match Data - used for DA (destination address) match

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8.6.2.86 PMATCH_CTRL_2 Register (Address = 629h) [Reset = 0000h]

PMATCH_CTRL_2 is shown in Figure 8-105 and described in Table 8-114.

Return to the Table 8-27.

Figure 8-105. PMATCH_CTRL_2 Register

15	14	13	12	11	10	9	8
pmatch_data_31_16							
R/W-0b							
7	6	5	4	3	2	1	0
pmatch_data_31_16							
R/W-0b							

Table 8-114. PMATCH_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_31_16	R/W	0b	Bits 31:16 of Perfect Match Data - used for DA (destination address) match

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8.6.2.87 PMATCH_CTRL_3 Register (Address = 62Ah) [Reset = 0000h]

PMATCH_CTRL_3 is shown in Figure 8-106 and described in Table 8-115.

Return to the Table 8-27.

Figure 8-106. PMATCH_CTRL_3 Register

15	14	13	12	11	10	9	8
pmatch_data_47_32							
R/W-0b							
7	6	5	4	3	2	1	0
pmatch_data_47_32							
R/W-0b							

Table 8-115. PMATCH_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_47_32	R/W	0b	Bits 47:32 of Perfect Match Data - used for DA (destination address) match

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8.6.2.88 TX_PKT_CNT_1 Register (Address = 639h) [Reset = 0000h]

TX_PKT_CNT_1 is shown in Figure 8-107 and described in Table 8-116.

Return to the Table 8-27.

Figure 8-107. TX_PKT_CNT_1 Register

15	14	13	12	11	10	9	8
tx_pkt_cnt_15_0							
0b							
7	6	5	4	3	2	1	0
tx_pkt_cnt_15_0							
0b							

Table 8-116. TX_PKT_CNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_pkt_cnt_15_0		0b	Lower 16 bits of Tx packet counter Note : Register is cleared when 0x639, 0x63A, 0x63B are read in sequence

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8.6.2.89 TX_PKT_CNT_2 Register (Address = 63Ah) [Reset = 0000h]

TX_PKT_CNT_2 is shown in Figure 8-108 and described in Table 8-117.

Return to the Table 8-27.

Figure 8-108. TX_PKT_CNT_2 Register

15	14	13	12	11	10	9	8
tx_pkt_cnt_31_16							
0b							
7	6	5	4	3	2	1	0
tx_pkt_cnt_31_16							
0b							

Table 8-117. TX_PKT_CNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_pkt_cnt_31_16		0b	Upper 16 bits of Tx packet counter Note : Register is cleared when 0x639, 0x63A, 0x63B are read in sequence

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8.6.2.90 TX_PKT_CNT_3 Register (Address = 63Bh) [Reset = 0000h]

TX_PKT_CNT_3 is shown in Figure 8-109 and described in Table 8-118.

Return to the Table 8-27.

Figure 8-109. TX_PKT_CNT_3 Register

15	14	13	12	11	10	9	8
tx_err_pkt_cnt							
0b							
7	6	5	4	3	2	1	0
tx_err_pkt_cnt							
0b							

Table 8-118. TX_PKT_CNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_err_pkt_cnt		0b	Tx packet w error (CRC error) counter Note : Register is cleared when 0x639, 0x63A, 0x63B are read in sequence

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8.6.2.91 RX_PKT_CNT_1 Register (Address = 63Ch) [Reset = 0000h]

RX_PKT_CNT_1 is shown in Figure 8-110 and described in Table 8-119.

Return to the Table 8-27.

Figure 8-110. RX_PKT_CNT_1 Register

15	14	13	12	11	10	9	8
rx_pkt_cnt_15_0							
0b							
7	6	5	4	3	2	1	0
rx_pkt_cnt_15_0							
0b							

Table 8-119. RX_PKT_CNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_pkt_cnt_15_0		0b	Lower 16 bits of Rx packet counter Note : Register is cleared when 0x63C, 0x63D, 0x63E are read in sequence

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8.6.2.92 RX_PKT_CNT_2 Register (Address = 63Dh) [Reset = 0000h]

RX_PKT_CNT_2 is shown in Figure 8-111 and described in Table 8-120.

Return to the Table 8-27.

Figure 8-111. RX_PKT_CNT_2 Register

15	14	13	12	11	10	9	8
rx_pkt_cnt_31_16							
0b							
7	6	5	4	3	2	1	0
rx_pkt_cnt_31_16							
0b							

Table 8-120. RX_PKT_CNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_pkt_cnt_31_16		0b	Upper 16 bits of Rx packet counter Note : Register is cleared when 0x63C, 0x63D, 0x63E are read in sequence

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8.6.2.93 RX_PKT_CNT_3 Register (Address = 63Eh) [Reset = 0000h]

RX_PKT_CNT_3 is shown in Figure 8-112 and described in Table 8-121.

Return to the Table 8-27.

Figure 8-112. RX_PKT_CNT_3 Register

15	14	13	12	11	10	9	8
rx_err_pkt_cnt							
0b							
7	6	5	4	3	2	1	0
rx_err_pkt_cnt							
0b							

Table 8-121. RX_PKT_CNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_err_pkt_cnt		0b	Rx packet w error (CRC error) counter Note : Register is cleared when 0x63C, 0x63D, 0x63E are read in sequence

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8.6.2.94 RMII_CTRL_1 Register (Address = 648h) [Reset = 0120h]

RMII_CTRL_1 is shown in Figure 8-113 and described in Table 8-122.

Return to the Table 8-27.

Figure 8-113. RMII_CTRL_1 Register

15	14	13	12	11	10	9	8
RESERVED					cfg_rmii_dis_delayed_txd_en	cfg_rmii_half_full_th	
R-0b					R/W-0b	R/W-10b	
7	6	5	4	3	2	1	0
cfg_rmii_half_full_th	cfg_rmii_mode	cfg_rmii_bypass_afifo_en	cfg_xi_50	RESERVED	RESERVED	cfg_rmii_rev1_0	cfg_rmii_enh
R/W-10b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-122. RMII_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0b	Reserved
10	cfg_rmii_dis_delayed_txd_en	R/W	0b	If set, disables delay of TXD in RMII mode
9-7	cfg_rmii_half_full_th	R/W	10b	FIFO Half Full Threshold in nibbles for the RMII Rx FIFO
6	cfg_rmii_mode	R/W	0b	1 = RMII enabled 0 = RMII disabled if({RX_D2_strap, RX_D1_strap} == 2'b01) reset_val = 1 else reset_val = 0 0b = RMII disabled 1b = RMII enabled
5	cfg_rmii_bypass_afifo_en	R/W	1b	1= RMII async fifo bypass enable 0= RMII async fifo not bypassed 0b = RMII async fifo not bypassed 1b = RMII async fifo bypass enable
4	cfg_xi_50	R/W	0b	XI sel for RMII mode if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3'b010) reset_val = 1 else reset_val = 0
3	RESERVED	R/W	0b	Reserved
2	RESERVED	R/W	0b	Reserved
1	cfg_rmii_rev1_0	R/W	0b	RMII Rev1.0 enable bit
0	cfg_rmii_enh	R/W	0b	RMII enahnced mode enable bit

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8.6.2.95 RMII_STATUS_1 Register (Address = 649h) [Reset = 0000h]

RMII_STATUS_1 is shown in Figure 8-114 and described in Table 8-123.

Return to the Table 8-27.

Figure 8-114. RMII_STATUS_1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED						rmii_af_unf_err	rmii_af_ovf_err
R-0b						R-0b	R-0b

Table 8-123. RMII_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0b	Reserved
1	rmii_af_unf_err	R	0b	Clear on read bit RMII fifo undeflow error status
0	rmii_af_ovf_err	R	0b	Clear on Read bit RMII fifo overflow status

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8.6.2.96 RMII_OVERRIDE_CTRL Register (Address = 64Ah) [Reset = 0010h]

RMII_OVERRIDE_CTRL is shown in Figure 8-115 and described in Table 8-124.

Return to the Table 8-27.

Figure 8-115. RMII_OVERRIDE_CTRL Register

15	14	13	12	11	10	9	8
RESERVED					cfg_clk50_tx_dll	cfg_clk50_dll	RESERVED
R-0b					R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-124. RMII_OVERRIDE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0b	Reserved
10	cfg_clk50_tx_dll	R/W	0b	1 = use 50M DLL clock in RMII master for TX 0 = legacy mode if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3'b011) reset_val = 1 else reset_val = 0 0b = legacy mode 1b = use 50M DLL clock in RMII master for TX
9	cfg_clk50_dll	R/W	0b	1 = use 50M DLL clock in RMII slave for RX 0 = use legacy mode if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3'b010) reset_val = 1 else reset_val = 0 0b = use legacy mode 1b = use 50M DLL clock in RMII slave for RX
8	RESERVED	R/W	0b	Reserved
7	RESERVED	R/W	0b	Reserved
6	RESERVED	R/W	0b	Reserved
5	RESERVED	R/W	0b	Reserved
4	RESERVED	R/W	1b	Reserved
3	RESERVED	R/W	0b	Reserved
2	RESERVED	R/W	0b	Reserved
1	RESERVED	R/W	0b	Reserved
0	RESERVED	R/W	0b	Reserved

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8.6.2.97 dsp_reg_71 Register (Address = 871h) [Reset = 0000h]

dsp_reg_71 is shown in Figure 8-116 and described in Table 8-125.

Return to the Table 8-27.

Figure 8-116. dsp_reg_71 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
worst_sqi_out			RESERVED	sqi_out			RESERVED
0b			R-0b	R-0b			R-0b

Table 8-125. dsp_reg_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-5	worst_sqi_out		0b	Worst SQI value since last read
4	RESERVED	R	0b	Reserved
3-1	sqi_out	R	0b	SQI value
0	RESERVED	R	0b	Reserved

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8.6.2.98 MMD1_PMA_CTRL_1 Register (Address = 1000h) [Reset = 0000h]

MMD1_PMA_CTRL_1 is shown in Figure 8-117 and described in Table 8-126.

Return to the Table 8-27.

Figure 8-117. MMD1_PMA_CTRL_1 Register

15	14	13	12	11	10	9	8
PMA_reset	RESERVED						
R/W-0b	R-0b						
7	6	5	4	3	2	1	0
RESERVED							PMA_loopback
R-0b							R/W-0b

Table 8-126. MMD1_PMA_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PMA_reset	R/W	0b	0 = PMA not reset 1= PMA reset 0b = PMA not reset 1b = PMA reset
14-1	RESERVED	R	0b	Reserved
0	PMA_loopback	R/W	0b	0 = PMA loopback not set 1= PMA loopback set 0b = PMA loopback not set 1b = PMA loopback set

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8.6.2.99 MMD1_PMA_STATUS_1 Register (Address = 1001h) [Reset = 0000h]

MMD1_PMA_STATUS_1 is shown in Figure 8-118 and described in Table 8-127.

Return to the Table 8-27.

Figure 8-118. MMD1_PMA_STATUS_1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED					link_status	RESERVED	
R-0b					R-0b	R-0b	

Table 8-127. MMD1_PMA_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0b	Reserved
2	link_status	R	0b	link status from link monitor state machine 0b = link status is down 1b = link status is up
1-0	RESERVED	R	0b	Reserved

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8.6.2.100 MMD1_PMA_STAUS_2 Register (Address = 1007h) [Reset = 003Dh]

MMD1_PMA_STAUS_2 is shown in Figure 8-119 and described in Table 8-128.

Return to the Table 8-27.

Figure 8-119. MMD1_PMA_STAUS_2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED		PMA/PMD type selection					
R-0b		R-111101b					

Table 8-128. MMD1_PMA_STAUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0b	Reserved
5-0	PMA/PMD type selection	R	111101b	PMA or PMD type selection field 11111xb = reserved for future use 111100b = reserved for future use 1110xxb = reserved for future use 110xxxb = reserved for future use 111101b = 100BASE-T1 PMA or PMD

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8.6.2.101 MMD1_PMA_EXT_ABILITY_1 Register (Address = 100Bh) [Reset = 0800h]

MMD1_PMA_EXT_ABILITY_1 is shown in Figure 8-120 and described in Table 8-129.

Return to the Table 8-27.

Figure 8-120. MMD1_PMA_EXT_ABILITY_1 Register

15	14	13	12	11	10	9	8
RESERVED				BASE-T1 extended abilities	RESERVED		
R-0b				R-1b	R-0b		
7	6	5	4	3	2	1	0
RESERVED							
R-0b							

Table 8-129. MMD1_PMA_EXT_ABILITY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0b	Reserved
11	BASE-T1 extended abilities	R	1b	1 = PMA/PMD has BASE-T1 extended abilities listed in register 18 in MMD1 0 = PMA/PMD does not have BASE-T1 extended abilities 0b = PMA/PMD does not have BASE-T1 extended abilities 1b = PMA/PMD has BASE-T1 extended abilities listed in register 18 in MMD1
10-0	RESERVED	R	0b	Reserved

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8.6.2.102 MMD1_PMA_EXT_ABILITY_2 Register (Address = 1012h) [Reset = 0001h]

MMD1_PMA_EXT_ABILITY_2 is shown in Figure 8-121 and described in Table 8-130.

Return to the Table 8-27.

Figure 8-121. MMD1_PMA_EXT_ABILITY_2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
RESERVED							100BASE-T1 ability
R-0b							R-1b

Table 8-130. MMD1_PMA_EXT_ABILITY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0b	Reserved
0	100BASE-T1 ability	R	1b	1 = PMA/PMD is able to perform 100BASE-T1 0 = PMA/PMD is not able to perform 100BASE-T1 0b = PMA/PMD is not able to perform 100BASE-T1 1b = PMA/PMD is able to perform 100BASE-T1

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8.6.2.103 MMD1_PMA_CTRL_2 Register (Address = 1834h) [Reset = 8000h]

MMD1_PMA_CTRL_2 is shown in Figure 8-122 and described in Table 8-131.

Return to the Table 8-27.

Figure 8-122. MMD1_PMA_CTRL_2 Register

15	14	13	12	11	10	9	8
master_slave_man_cfg_en	brk_ms_cfg	RESERVED					
R-1b	R/W-0b	R-0b					
7	6	5	4	3	2	1	0
RESERVED				type selection			
R-0b				R-0b			

Table 8-131. MMD1_PMA_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	master_slave_man_cfg_en	R	1b	Value always 1
14	brk_ms_cfg	R/W	0b	1 = Configure PHY as MASTER 0 = Configure PHY as SLAVE pkg_36: reset_val = LED_0_strap pkg_28: reset_val = RX_D3_strap 0b = Configure PHY as SLAVE 1b = Configure PHY as MASTER
13-4	RESERVED	R	0b	Reserved
3-0	type selection	R	0b	type selection field 1xxxb = Reserved for future use 01xxb = Reserved for future use 001xb = Reserved for future use 0001b = Reserved for future use 0b = 100BASE-T1

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8.6.2.104 MMD1_PMA_TEST_MODE_CTRL Register (Address = 1836h) [Reset = 0000h]

MMD1_PMA_TEST_MODE_CTRL is shown in Figure 8-123 and described in Table 8-132.

Return to the Table 8-27.

Figure 8-123. MMD1_PMA_TEST_MODE_CTRL Register

15	14	13	12	11	10	9	8
brk_test_mode			RESERVED				
R/W-0b			R/W-0b				
7	6	5	4	3	2	1	0
RESERVED							
R/W-0b							

Table 8-132. MMD1_PMA_TEST_MODE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	brk_test_mode	R/W	0b	100BASE-T1 test mode control 000b = Normal mode operation 001b = Test mode 1 010b = Test mode 2 011b = Reserved 100b = Test mode 4 101b = Test mode 5 110b = Reserved 111b = Reserved
12-0	RESERVED	R/W	0b	Reserved

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8.6.2.105 MMD3_PCS_CTRL_1 Register (Address = 3000h) [Reset = 0000h]

MMD3_PCS_CTRL_1 is shown in Figure 8-124 and described in Table 8-133.

Return to the Table 8-27.

Figure 8-124. MMD3_PCS_CTRL_1 Register

15	14	13	12	11	10	9	8
PCS_Reset	PCS_loopback	RESERVED			rx_clock_stoppable	RESERVED	
R/W-0b	R/W-0b	R-0b			R/W-0b	R-0b	
7	6	5	4	3	2	1	0
RESERVED							
R-0b							

Table 8-133. MMD3_PCS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCS_Reset	R/W	0b	Reset bit, Self Clear. When write to this bit 1: 1. reset the registers (not vendor specific) at MMD3/MMD7. 2. Reset brk_top Please notice: This register is WSC (write-self-clear) and not read-only!
14	PCS_loopback	R/W	0b	This bit is cleared by PCS_Reset
13-11	RESERVED	R	0b	Reserved
10	rx_clock_stoppable	R/W	0b	RW, reset value = 1. 1= PHY may stop receive clock during LPI 0= Clock not stoppable Note: this flop implemented at glue logic
9-0	RESERVED	R	0b	Reserved

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8.6.2.106 MMD3_PCS_Status_1 Register (Address = 3001h) [Reset = 0000h]

MMD3_PCS_Status_1 is shown in Figure 8-125 and described in Table 8-134.

Return to the Table 8-27.

Figure 8-125. MMD3_PCS_Status_1 Register

15	14	13	12	11	10	9	8
RESERVED				TX_LPI_received	RX_LPI_received	Tx_LPI_indication	Rx_LPI_indication
R-0b				R-0b	R-0b	R-0b	R-0b
7	6	5	4	3	2	1	0
RESERVED	tx_clock_stoppable	RESERVED					
R-0b	R-0b	R-0b					

Table 8-134. MMD3_PCS_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0b	Reserved
11	TX_LPI_received	R	0b	RO/LH 0b = LPI not received 1b = Tx PCS hs received LPI
10	RX_LPI_received	R	0b	RO/LH 0b = LPI not received 1b = Rx PCS hs received LPI
9	Tx_LPI_indication	R	0b	1= TX PCS is currently receiving LPI 0= PCS is not currently receiving LPI 0b = PCS is not currently receiving LPI 1b = TX PCS is currently receiving LPI
8	Rx_LPI_indication	R	0b	1= RX PCS is currently receiving LPI 0= PCS is not currently receiving LPI 0b = PCS is not currently receiving LPI 1b = RX PCS is currently receiving LPI
7	RESERVED	R	0b	Reserved
6	tx_clock_stoppable	R	0b	1= the MAC may stop the clock during LPI 0= Clock not stoppable 0b = Clock not stoppable 1b = the MAC may stop the clock during LPI
5-0	RESERVED	R	0b	Reserved

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.2 Application Information

The DP83TC812 is a single-port 100-Mbps Automotive Ethernet PHY. It supports IEEE 802.3bw and allows for connections to an Ethernet MAC through MII, RMII, RGMII, or SGMII. When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required connections.

Note

Refer to SNLA389 Application Note for more information about the register settings used for compliance testing. It is necessary to use these register settings to achieve the same performance as observed during compliance testing.

9.3 Typical Applications

Figure 9-1 through Figure 9-5 show some the typical applications for the DP83TC812x-Q1.

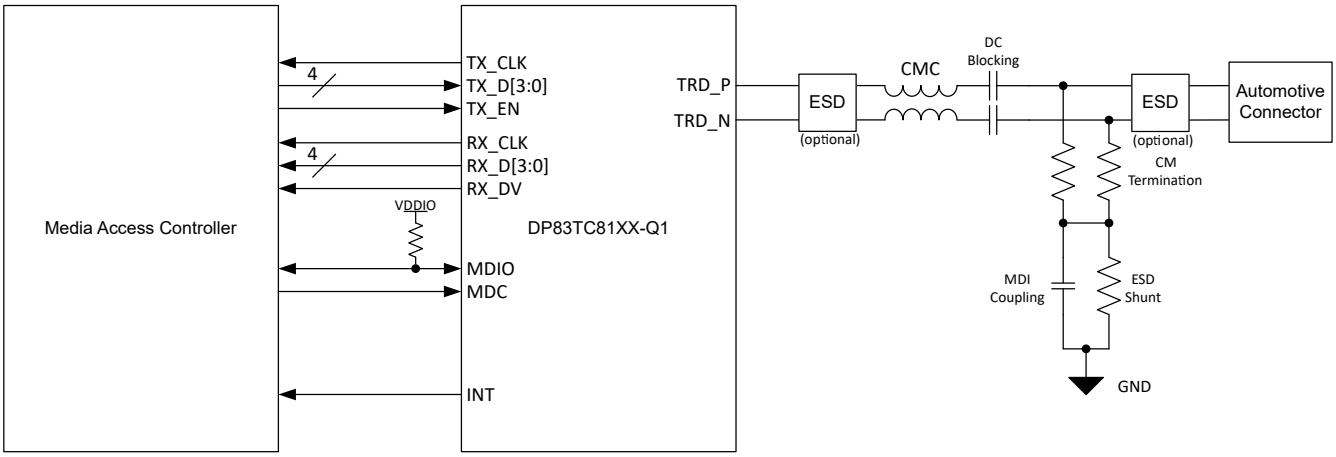

Figure 9-1. Typical Application (MII)

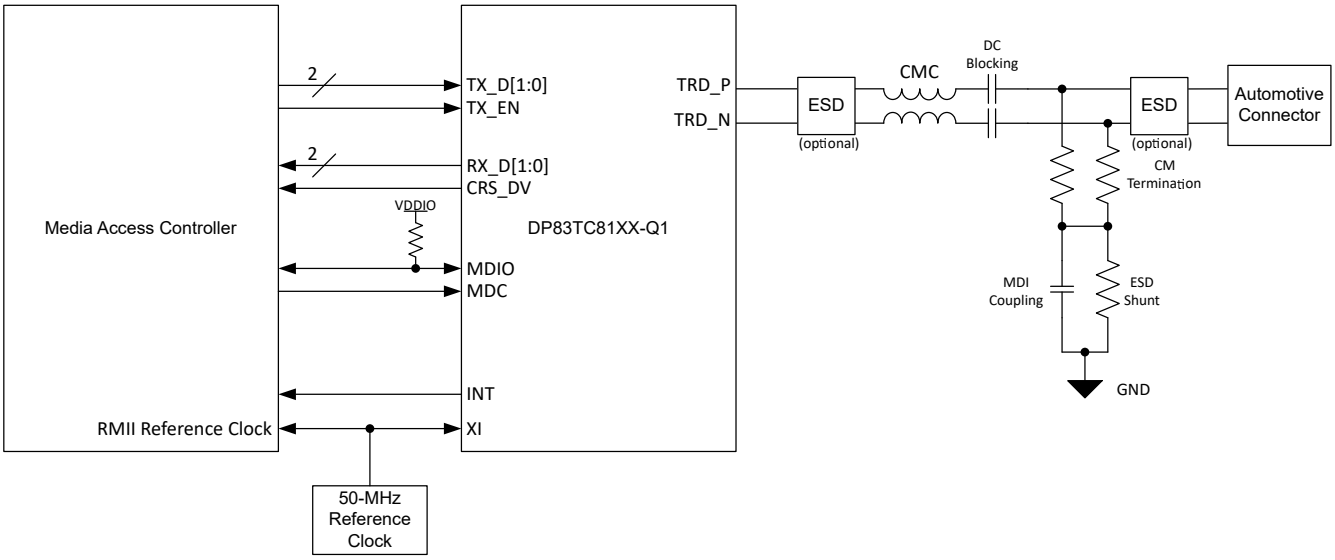

Figure 9-2. Typical Application (RMII Slave)

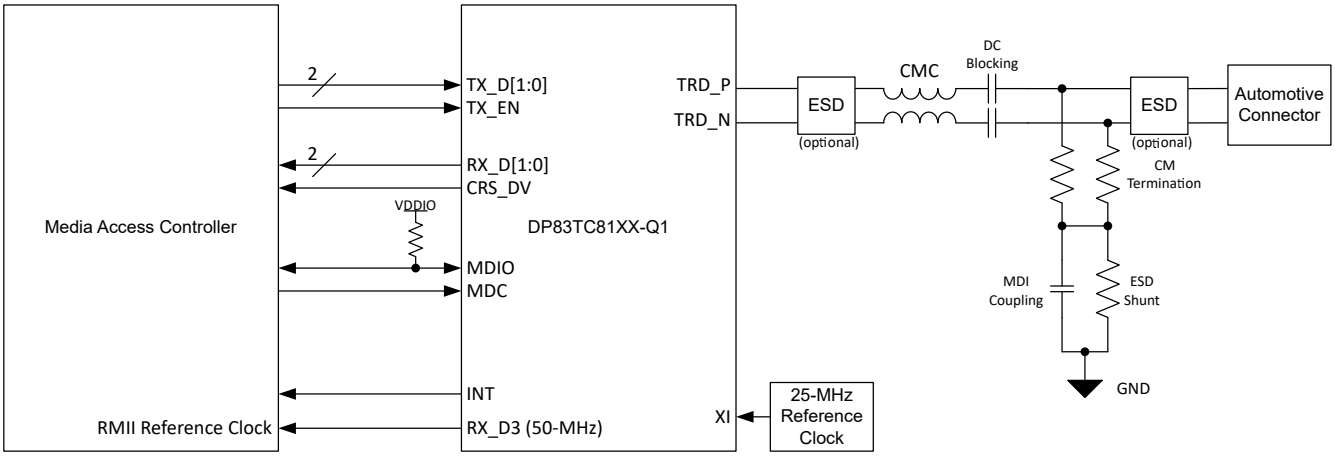

Figure 9-3. Typical Application (RMII Master)

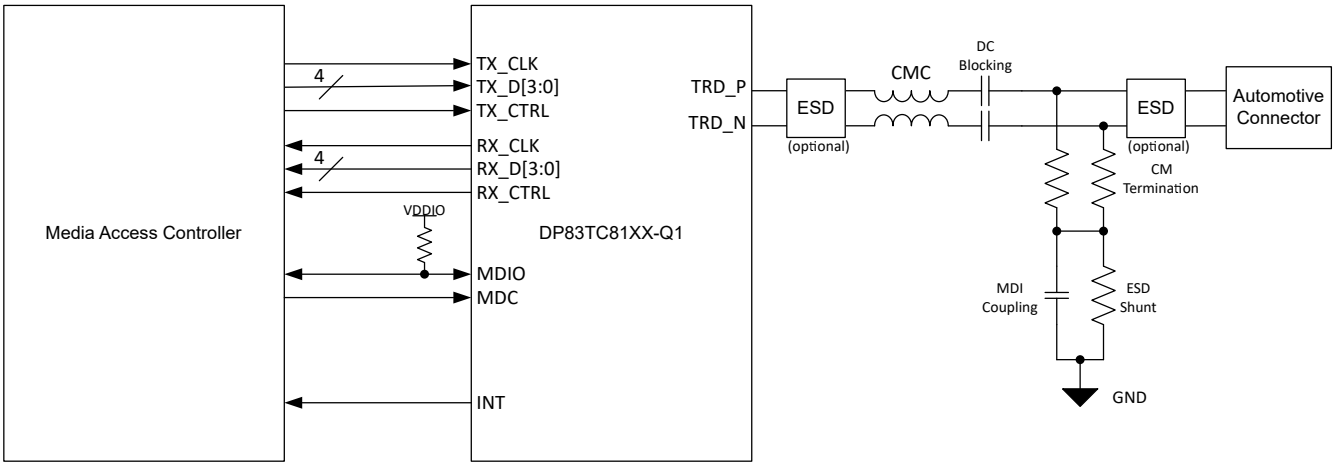

Figure 9-4. Typical Application (RGMII)

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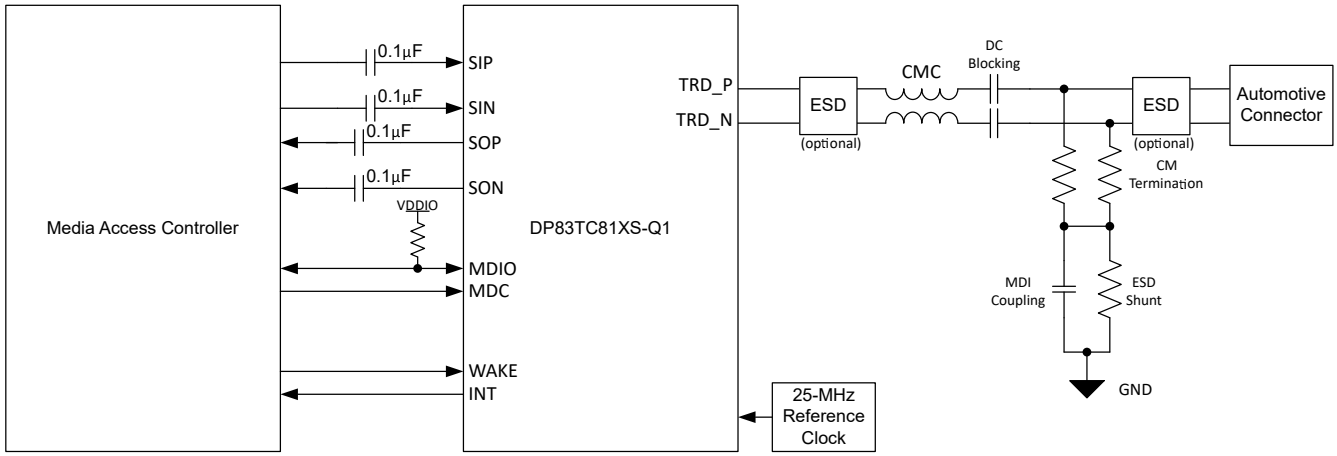

Figure 9-5. Typical Application (SGMII)

9.3.1 Design Requirements

For these typical applications, use the following as design parameters from the table below. Refer to *Power Supply Recommendations* section for detailed connection diagram.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DDIO}	1.8 V, 2.5 V, or 3.3 V
V_{DDMAC}	1.8 V, 2.5 V, or 3.3 V
V_{DDA}	3.3 V
V_{SLEEP}	3.3 V
Decoupling capacitors V_{DDIO} (2) (3)	0.01 µF
(Optional) ferrite bead for V_{DDIO} (3)	1 kΩ at 100 MHz (BLM18KG601SH1D)
Decoupling capacitors V_{DDMAC} (2)	0.01 µF, 0.47 µF
Ferrite bead for V_{DDMAC}	1 kΩ at 100 MHz (BLM18KG601SH1D)
Decoupling capacitors V_{DDA} (2)	0.01 µF, 0.47 µF
(Optional) ferrite bead for V_{DDA}	1 kΩ at 100 MHz (BLM18KG601SH1D)
Decoupling capacitors V_{SLEEP}	0.1 µF
DC Blocking Capacitors (2)	0.1 µF
Common-Mode Choke	200 µH
Common Mode Termination Resistors(1)	1 kΩ
MDI Coupling Capacitor (2)	4.7 nF
ESD Shunt(2)	100 kΩ
Reference Clock	25 MHz

(1) 1% tolerance components are recommended.
(2) 10% tolerance components are recommended.
(3) If VDDIO is separate from VDDMAC then additional ferrite bead and 0.47µF capacitor will be required on VDDIO.

9.3.1.1 Physical Medium Attachment

There must be no metal running beneath the common-mode choke. CMCs can inject noise into metal beneath them, which can affect the emissions and immunity performance of the system. Because the DP83TC812S-Q1 is a voltage mode line driver, no external termination resistors are required. The ESD shunt and MDI coupling capacitor must be connected to ground. Ensure that the common mode termination resistors are 1% tolerance or better to improve differential coupling.

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9.3.1.1.1 Common-Mode Choke Recommendations

The following CMCs are recommended for use with the DP83TC812S-Q1 :

Table 9-2. Recommended CMCs

MANUFACTURER	PART NUMBER
Pulse Electronics	AE2002
Murata	DLW43MH201XK2L
Murata	DLW32MH201XK2
TDK	ACT1210L-201

Table 9-3. CMC Electrical Specifications

PARAMETER	TYP	UNITS	CONDITIONS
Insertion Loss	–0.5	dB	1 – 30 MHz
	–1.0	dB	30 – 60 MHz
Return Loss	–26	dB	1 – 30 MHz
	–20	dB	30 – 60 MHz
Common-Mode Rejection	–24	dB	1 MHz
	–42	dB	10 – 100 MHz
	–25	dB	400 MHz
Differential Common-Mode Rejection	–70	dB	1 – 10 MHz
	–50	dB	100 MHz
	–24	dB	1000 MHz

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9.3.2 Detailed Design Procedure

When creating a new system design with an Ethernet PHY, follow this schematic capture procedure:

1. Select desired PHY hardware configurations in table Table 8-19.
2. Use the Electrical Characteristics table, the Table 8-17 table and the Table 8-18 table to select the correct external bootstrap resistors.
3. If using LEDs, ensure the correct external circuit is applied as shown in Figure 8-19.
4. Select an appropriate clock source that adheres to either the CMOS-level oscillator or crystal resonator requirements within the Electrical Characteristics table.
5. Select a CMC, a list of recommended CMCs are located in Table 9-2.
6. Add common-mode termination, DC-blocking capacitors, an MDI-coupling capacitor, and an ESD shunt found in Table 9-1.
7. Ensure that there is sufficient supply decoupling on VDDIO and VDDA supply pins.
8. Add an external pullup resistor (tie to VDDIO) on MDIO line.
9. If operating with SGMII, place 0.1-µF, DC-blocking capacitors between the MAC and PHY SGMII pins.
10. If sleep modes are not desired, WAKE and EN pins must be tied to VSLEEP directly or through an external pullup resistor.

The following layout procedure must be followed:

1. Locate the PHY near the edge of the board so that short MDI traces can be routed to the desired connector.
2. Place the MDI external components: CMC, DC-blocking capacitors, CM termination, MDI-coupling capacitor, and ESD shunt.
3. Create a top-layer metal pour keepout under the CMC.
4. Ensure that the MDI TRD_M and TRD_P traces are routed such that they are 100-Ω differential.
5. Place the clock source near the XI and XO pins.
6. Ensure that when configured for MII, RMII, or RGMII operation, the xMII pins are routed 50-Ω and are single-ended with reference to ground.
7. Ensure that transmit path xMII pins are routed such that setup and hold timing does not violate the PHY requirements.
8. Ensure that receive path xMII pins are routed such that setup and hold timing does not violate the MAC requirements.
9. Ensure that when configured for SGMII operation, the xMII RX_P, RX_M, TX_P, and TX_M pins are routed 100-Ω differential.
10. Place the MDIO pullup close to the PHY.

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9.3.3 Application Curves

The following curves were obtained using the PHY evaluation module under nominal conditions.

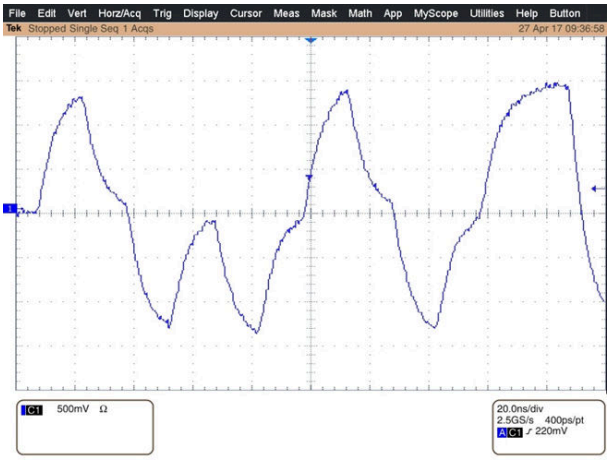

Figure 9-6. MDI IDLE Stream

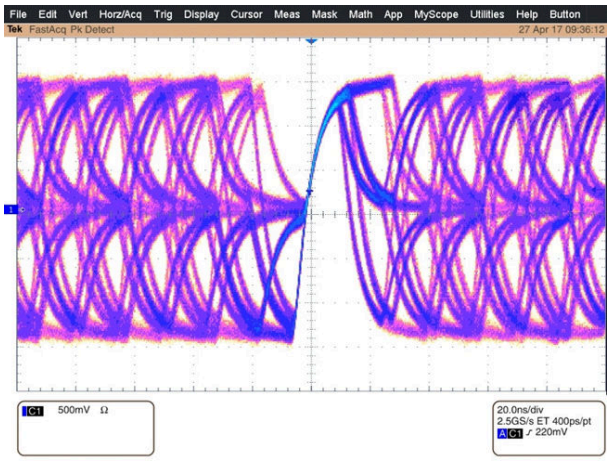

Figure 9-7. MDI IDLE Stream (Variable Persistence)

10 Power Supply Recommendations

The DP83TC812S-Q1 is capable of operating with a wide range of IO supply voltages (3.3 V, 2.5 V, or 1.8 V). No power supply sequencing is required. The recommended power supply de-coupling network is shown in the figure below. For improved conducted emissions, an optional ferrite bead may be placed between the supply and the PHY de-coupling network.

Typical TC-10 application block diagram along with supply and peripherals is shown below. TPS7B81-Q1 is the recommended part number to be used as 3.3V LDO for the VSLEEP rail. The low quiescent current of this LDO makes it ideal for TC-10 applications.

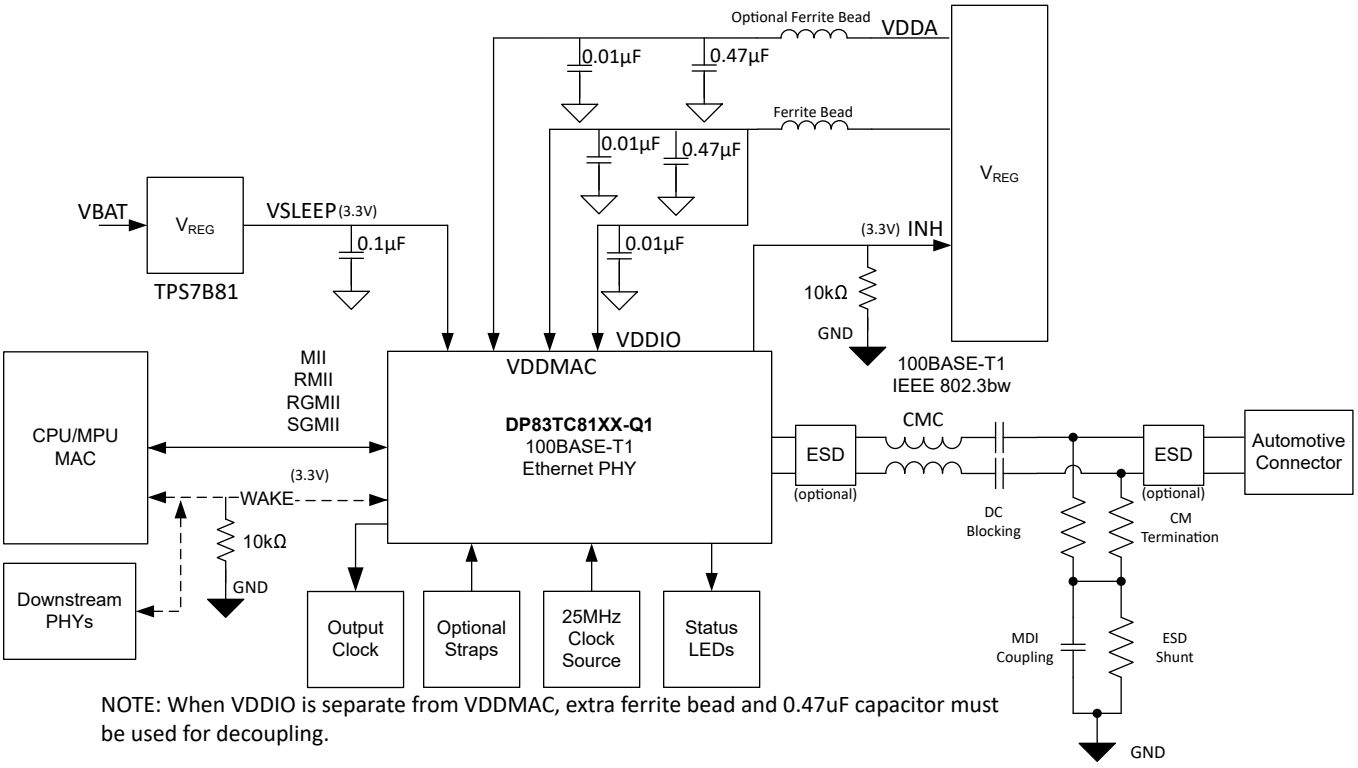

Figure 10-1. Typical TC-10 Application With Peripherals

When VDDIO and VDDMAC are separate, both voltage rails must have a dedicated network of ferrite bead, 0.47uF, and 0.01uF capacitors. VSLEEP can also be connected to VDDA, 0.1uF capacitor must be retained in this configuration.

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Current Consumption Break-Down

The following table highlights the break down of power consumption in active mode for each supply rail, specifically highlighting the split between VDDMAC and VDDIO.

Table 10-1. Active Mode Current Consumption

VOLTAGE RAIL	VOLTAGE (V)	MAX CURRENT (mA)[1]
MII		
VDDA	3.3	63
VDDIO	3.3	4
	2.5	3
	1.8	2
VDDMAC	3.3	20
	2.5	15
	1.8	11
VSLEEP	3.3	2
RMII		
VDDA	3.3	63
VDDIO	3.3	6
	2.5	4
	1.8	3
VDDMAC	3.3	17
	2.5	13
	1.8	10
VSLEEP	3.3	2
RGMII		
VDDA	3.3	63
VDDIO	3.3	4
	2.5	3
	1.8	2
VDDMAC	3.3	17
	2.5	13
	1.8	10
VSLEEP	3.3	2
SGMII		
VDDA	3.3	95
VDDIO	3.3	4
	2.5	3
	1.8	2
VDDMAC	3.3	8
	2.5	6
	1.8	4
VSLEEP	3.3	2

1. Current consumption measured across voltage, temperature, and process with active data communication.

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11 Layout

11.1 Layout Guidelines

11.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Traces must be kept short as possible. Unless mentioned otherwise, all signal traces must be 50-Ω, single-ended impedance. Differential traces must be 50-Ω single-ended and 100-Ω differential. Take care to ensure impedance is controlled throughout. Impedance discontinuities will cause reflections leading to emissions and signal integrity issues. Stubs must be avoided on all signal traces, especially differential signal pairs.

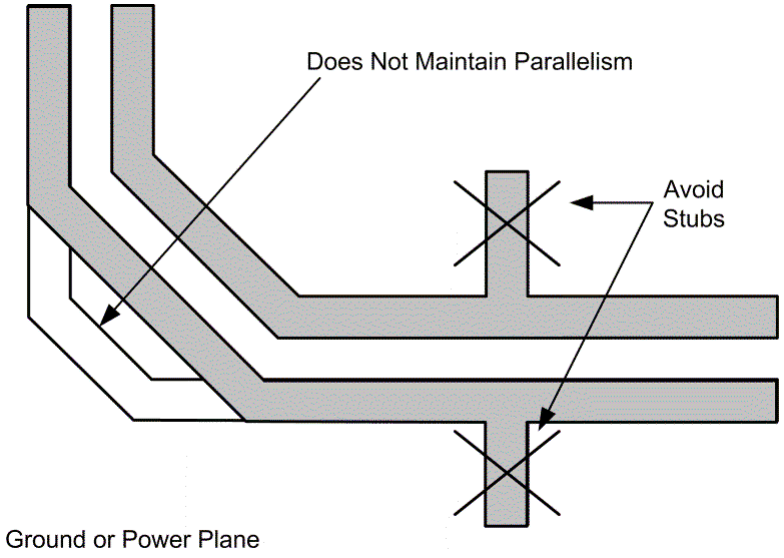

Figure 11-1. Differential Signal Trace Routing

Within the differential pairs, trace lengths must be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All transmit signal traces must be length matched to each other and all receive signal traces must be length matched to each other. For SGMII differential traces, it is recommended to keep the skew mismatch below 20ps.

Ideally, there must be no crossover on signal path traces. High speed signal traces must be routed on internal layers to improved EMC performance. However, vias present impedance discontinuities and must be minimized when possible. Route trace pairs on the same layer. Signals on different layers must not cross each other without at least one return path plane between them. Differential pairs must always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

11.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces must be avoided at all cost. A signal crossing a split plane may cause unpredictable return path currents and could impact signal quality and result in emissions issues.

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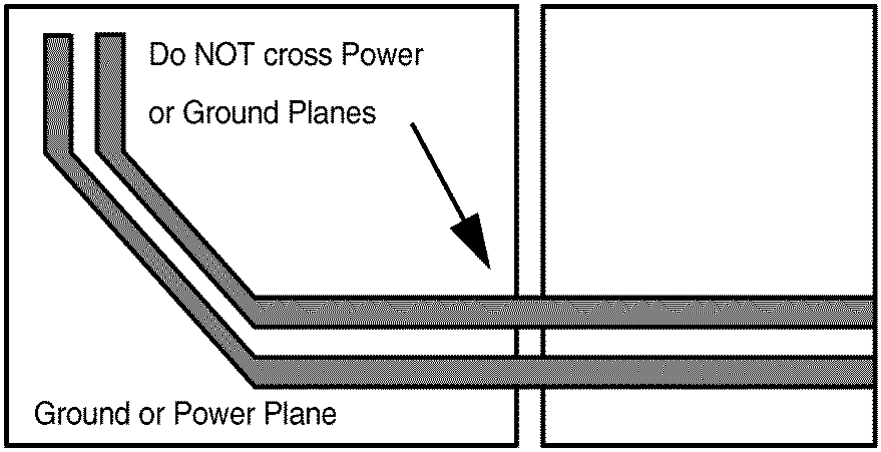

Figure 11-2. Power and Ground Plane Breaks

11.1.3 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

11.1.4 PCB Layer Stacking

To meet signal integrity and performance requirements, minimum four-layer PCB is recommended. However, a six-layer PCB and above must be used when possible.

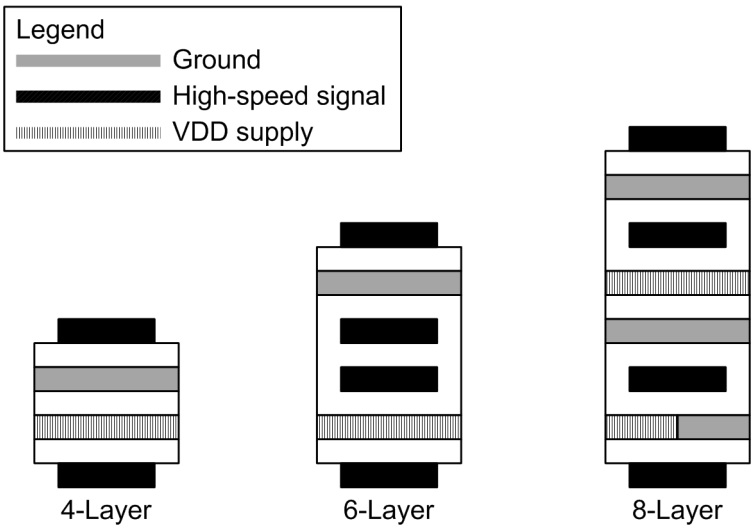

Figure 11-3. Recommended PCB Layer Stack-Up

11.2 Layout Example

There is an evaluation board references for the DP83TC812-Q1 . The DP83TC812EVM-MC is a media converter board which can be used for interoperability and bit error rate testing.

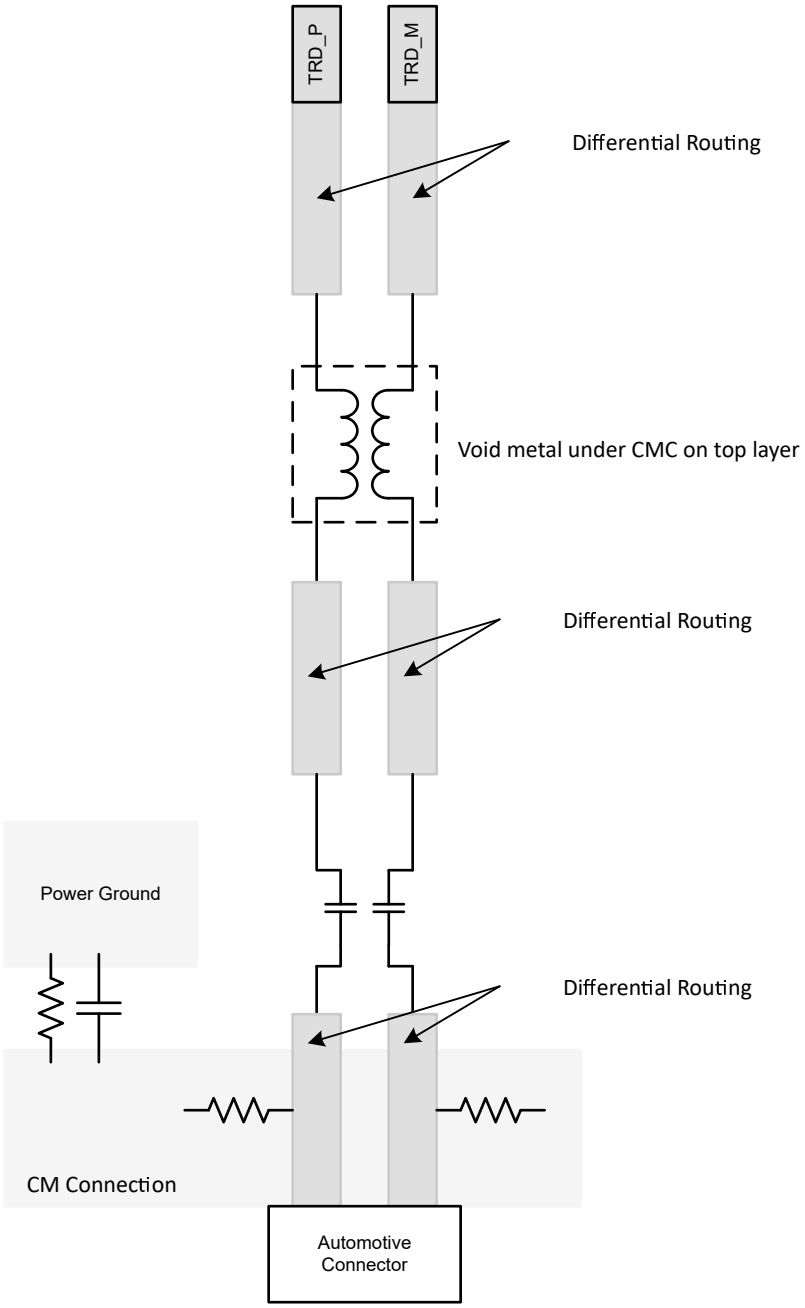

Figure 11-4. MDI Low-Pass Filter Layout Recommendation

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Community Resources

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DP83TC812RRHARQ1	ACTIVE	VQFN	RHA	36	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	812R	Samples
DP83TC812RRHATQ1	ACTIVE	VQFN	RHA	36	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	812R	Samples
DP83TC812SRHARQ1	ACTIVE	VQFN	RHA	36	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	812S	Samples
DP83TC812SRHATQ1	ACTIVE	VQFN	RHA	36	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	812S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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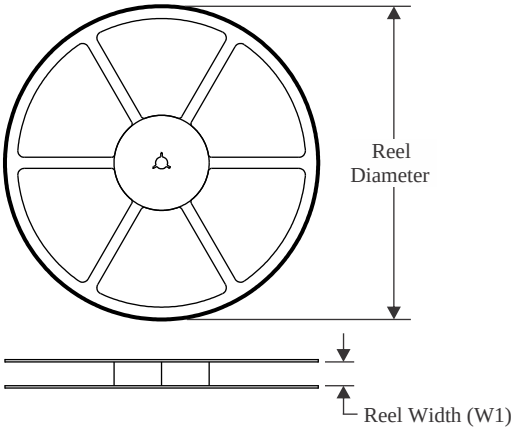
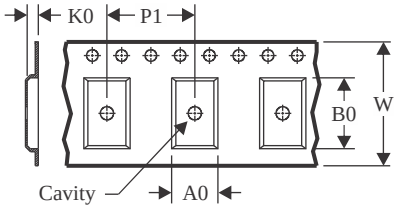
TAPE AND REEL INFORMATION

REEL DIMENSIONS

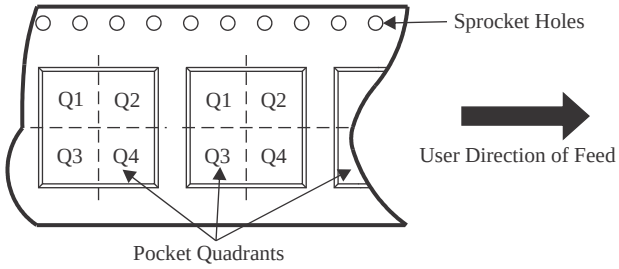


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

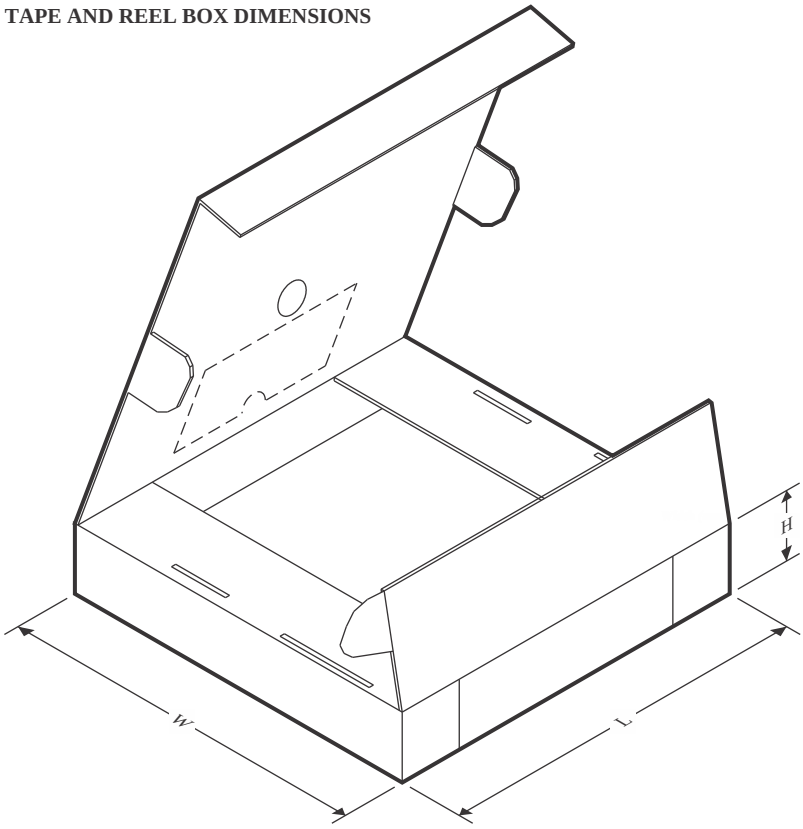
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83TC812RRHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC812RRHATQ1	VQFN	RHA	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC812SRHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC812SRHATQ1	VQFN	RHA	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83TC812RRHARQ1	VQFN	RHA	36	2500	367.0	367.0	35.0
DP83TC812RRHATQ1	VQFN	RHA	36	250	210.0	185.0	35.0
DP83TC812SRHARQ1	VQFN	RHA	36	2500	367.0	367.0	35.0
DP83TC812SRHATQ1	VQFN	RHA	36	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

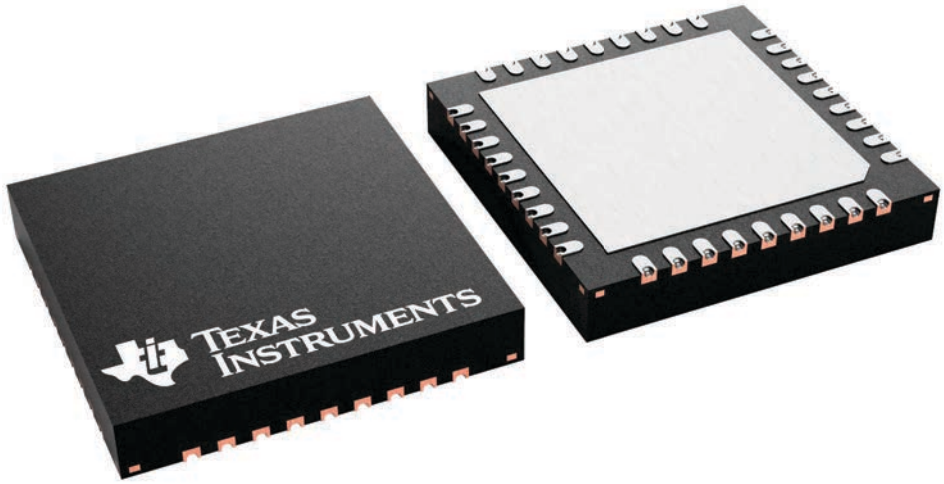
RHA 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



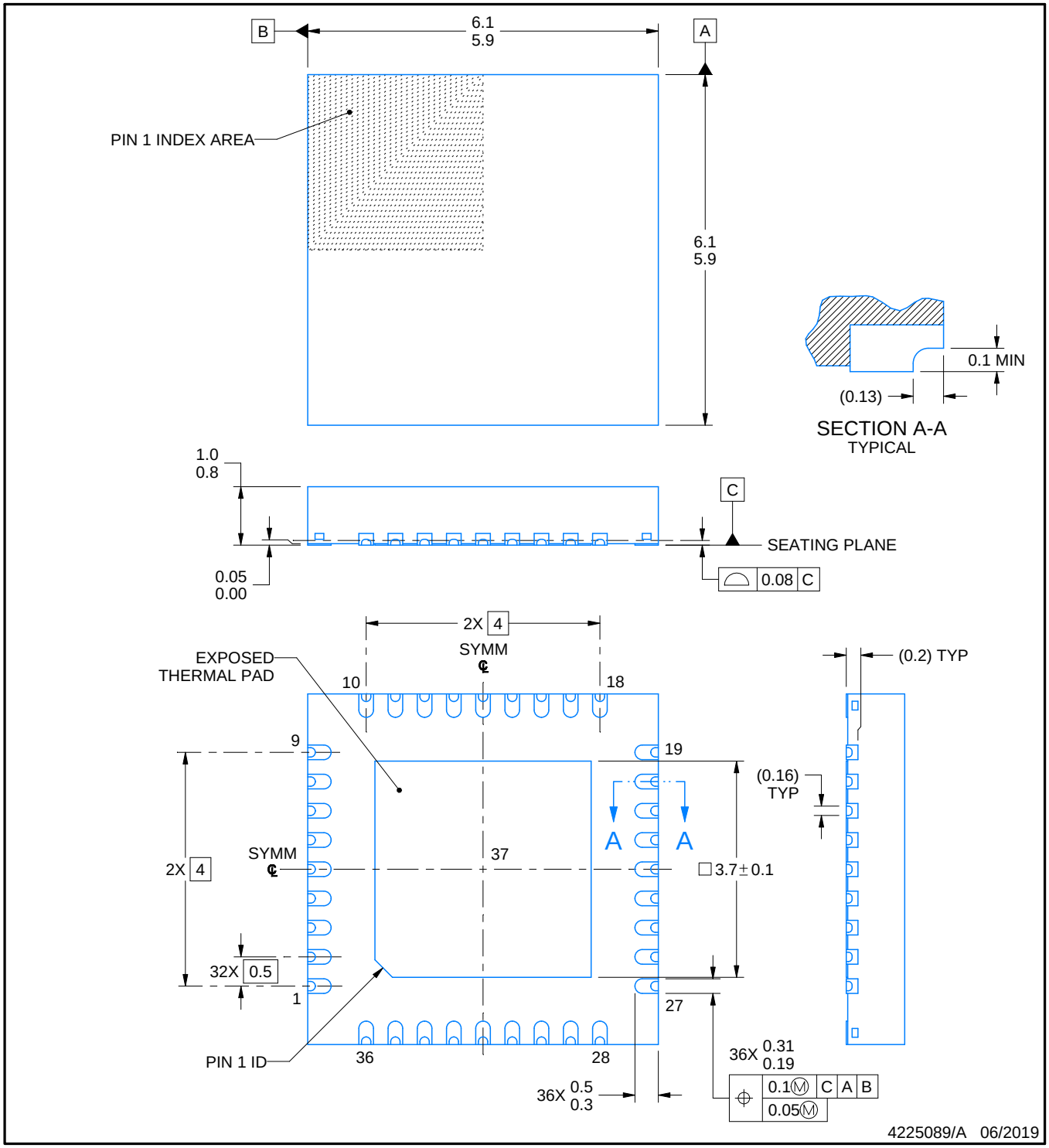
4228438/A

PACKAGE OUTLINE

RHA0036A

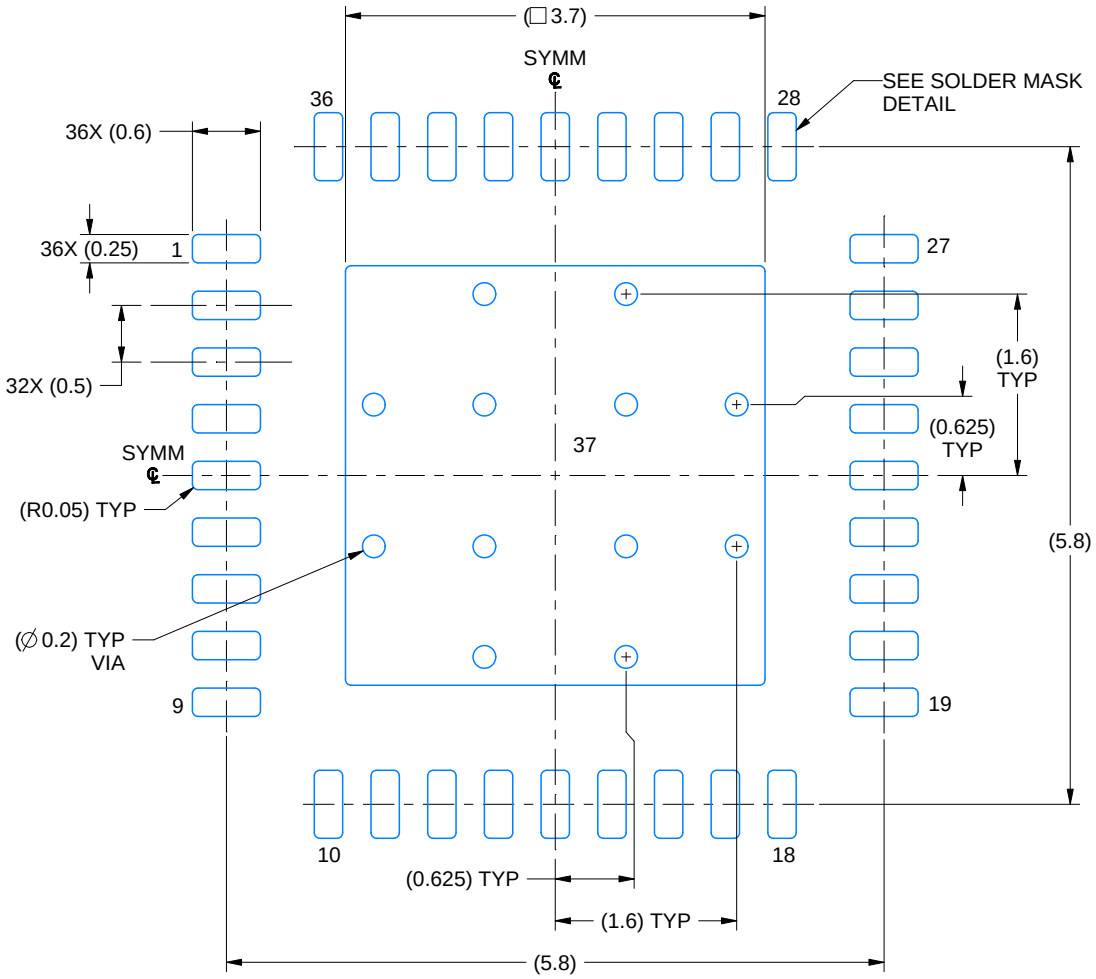
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

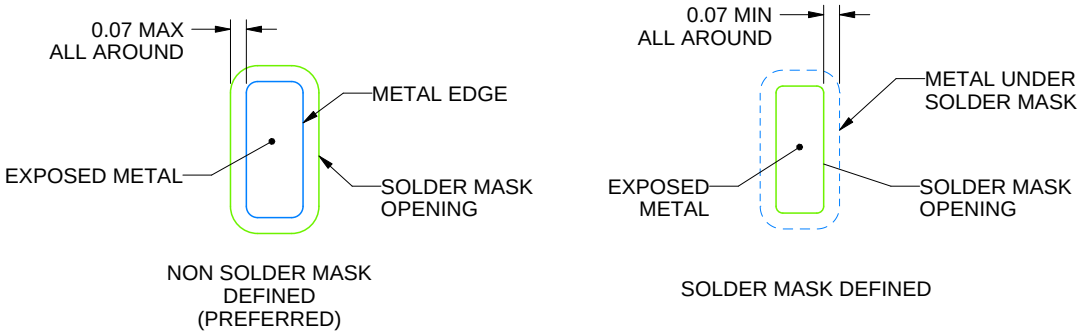


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4225089/A 06/2019

NOTES: (continued)

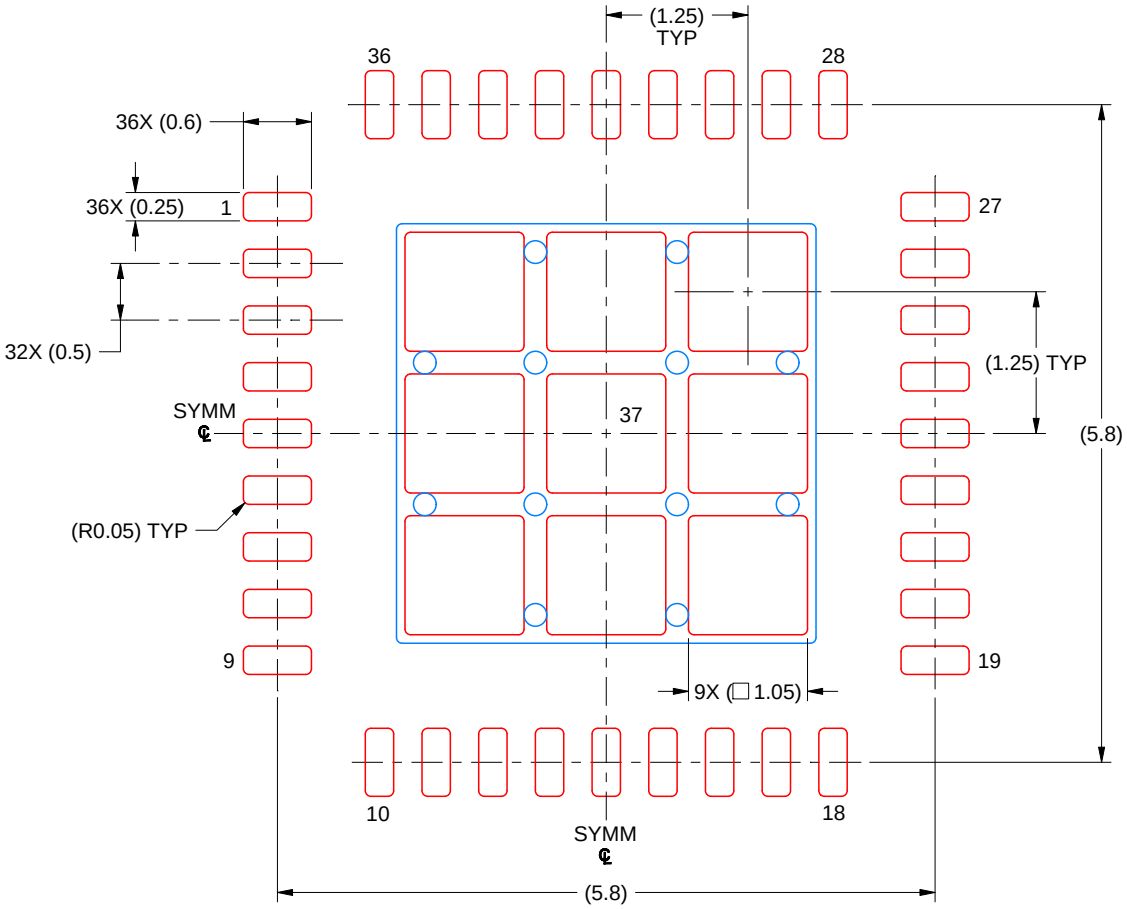
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0036A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225089/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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- Shortage Management
- Alternative Solution
- Excess Inventory Management