THE DATASHEET OF

LTC6373HDFM#TRPBF

36 V Fully-Differential Programmable-Gain Instrumentation Amplifier with 25 pA Input Bias Current

FEATURES

- Pin-Programmable Gains:
  - G = 0.25, 0.5, 1, 2, 4, 8, 16 V/V + Shutdown
- Fully Differential Outputs
- Gain Error: 0.015% (Max)
- Gain Error Drift: 1 ppm/°C (Max)
- CMRR: 103 dB (Min), G = 16
- Input Bias Current: 25 pA (Max)
- Input Offset Voltage: 92 µV (Max), G = 16
- Input Offset Voltage Drift: 1.7 µV/°C (Max), G = 16
- –3 dB Bandwidth: 4 MHz, G = 16
- Input Noise Density: 8 nV/√Hz, G = 16
- Slew Rate: 12 V/µs, G = 16
- Adjustable Output Common Mode Voltage
- Quiescent Supply Current: 4.4 mA
- Supply Voltage Range: ±4.5 V to ±18 V
- –40°C to +105°C Specified Temperature Range
- Small 12-Lead 4 mm × 4 mm DFN (LFCSP) Package

APPLICATIONS

- Data Acquisition Systems
- Biomedical Instrumentation
- Test and Measurement Equipment
- Differential ADC Drivers
- Single-Ended-to-Differential Conversion
- Multiplexed Applications

GENERAL DESCRIPTION

The LTC6373 is a precision instrumentation amplifier with fully differential outputs which includes a closely-matched internal resistor network to achieve excellent CMRR, offset voltage, gain error, gain drift, and gain nonlinearity. The user can easily program the gain to one of seven available settings through a 3-bit parallel interface (A2 to A0). The 8th state puts the part in shutdown which reduces the current consumption to 220 µA. Unlike a conventional voltage feedback amplifier, the LTC6373 maintains nearly the same bandwidth across all its gain settings.

The LTC6373 features fully differential outputs to drive high performance, differential-input ADCs. The output common mode voltage is independently adjustable via the V_{OCM} pin. The combination of high impedance inputs, DC precision, low noise, low distortion, and high-speed differential ADC drive makes the LTC6373 an ideal candidate for optimizing data acquisition systems.

The LTC6373 is available in a 12-lead 4 mm × 4 mm DFN (LFCSP) package and is fully specified over the −40°C to +105°C temperature range.

TYPICAL APPLICATION

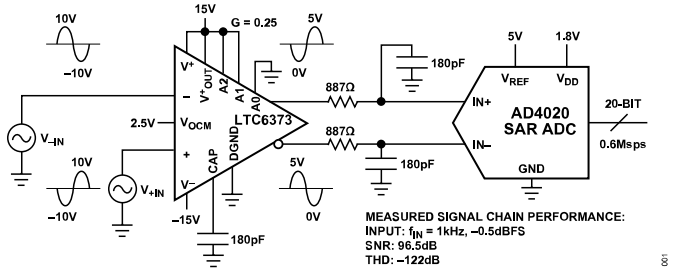

Figure 1. Interfacing a 40 V_{P-P} Ground-Referenced Differential Input Signal to a 5 V ADC

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8/2020—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V^+ = V^+_{OUT}$ = 15 V, V^- = −15 V, $V_{ICM} = V_{OCM}$ = DGND = 0 V, G = 1 (A2 = 5 V, A1 = A0 = 0 V). V_S is defined as ($V^+ – V^-$). V_{ICM} is defined as ($V_{+IN} + V_{-IN}$)/2. V_{OUTCM} is defined as ($V_{+OUT} + V_{-OUT}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{-OUT}$), T_A = 25°C unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIFFERENTIAL GAIN						
Differential Gain Range	G_{DIFF}	G = 16, 8, 4, 2, 1, 0.5, 0.25	0.25		16	V/V
Differential Gain Error[1]	ΔG_{DIFF}	G = 16, 8, 4, 2, 1, 0.5, 0.25		0.003	0.015	%
		T_A = −40°C to +105°C			0.023	%
Differential Gain Drift[2, 3]	$\Delta G_{DIFF}/\Delta T$			0.25	1	ppm/°C
Differential Gain Nonlinearity[1]	GNL	$V_{OUTDIFF}$ = 40 V_{P-P}		1	3	ppm
		T_A = −40°C to +105°C			10	ppm
DIFFERENTIAL OFFSET VOLTAGE (INPUT REFERRED)[4]	V_{OSDIFF}	G = 16, 8, 4, 2, 1, 0.5, 0.25		10 + 40/G	80 + 192/G	µV
		T_A = −40°C to +85°C			250 + 400/G	µV
		T_A = −40°C to +105°C			1120 + 1120/G	µV
Differential Offset Voltage Drift (Input Referred)[3]	$\Delta V_{OSDIFF}/\Delta T$	G = 16, 8, 4, 2, 1, 0.5, 0.25				
		T_A = −40°C to +85°C		0.3 + 0.5/G	1.5 + 2.5/G	µV/°C
		T_A = −40°C to +105°C		2 + 1.5/G	5 + 5.5/G	µV/°C
Differential Offset Voltage Hysteresis (Input Referred)[2, 5]		G = 16, 8, 4, 2, 1, 0.5, 0.25		10 + 15/G		µV
INPUT CHARACTERICS						
Input Bias Current[4, 6]	I_B	Active		2	25	pA
		T_A = −40°C to +85°C			100	pA
		T_A = −40°C to +105°C			600	pA
		Shutdown (A2 = A1 = A0 = 5 V)		20		pA
Input Offset Current[4, 6]	I_{OS}	Active		2	25	pA
		T_A = −40°C to +85°C			60	pA
		T_A = −40°C to +105°C			150	pA
		Shutdown (A2 = A1 = A0 = 5 V)		5		pA
Input Resistance	R_{IN}	Differential mode		5×10^{12}		Ω
		Common mode		5×10^{12}		Ω
Input Capacitance	C_{IN}			15		pF
Input Voltage Range	V_{INR}		V^- + 3		V^+ – 3	V
		T_A = −40°C to +105°C	V^- + 3.25		V^+ – 3	V
NOISE						
Differential Input Voltage Noise Density	e_n	f = 10 kHz				
		G = 16		8		nV/√Hz
		G = 8		8.4		nV/√Hz
		G = 4		9.5		nV/√Hz
		G = 2		12.2		nV/√Hz
		G = 1		18.7		nV/√Hz
		G = 0.5		26.4		nV/√Hz
		G = 0.25		41		nV/√Hz
Differential Input Voltage Noise		0.1 Hz to 10 Hz				
		G = 16		1.1		μV_{P-P}
		G = 8		1.2		μV_{P-P}
		G = 4		1.3		μV_{P-P}
		G = 2		1.5		μV_{P-P}
		G = 1		1.8		μV_{P-P}

SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		G = 0.5		2.4		μV_{P-P}
		G = 0.25		4.2		μV_{P-P}
Input Current Noise Density	i_n	f = 10 kHz		1		$fA/\sqrt{Hz}$
Input Current Noise		0.1 Hz to 10 Hz		100		fA_{P-P}
Common Mode Voltage Noise Density	e_{nVOCM}	f = 10 kHz		24		$nV/\sqrt{Hz}$
COMMON MODE REJECTION RATIO (INPUT REFERRED)						
Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$[7]	CMRR	DC to 60 Hz, 1 kΩ source Imbalance, V_{ICM} = ±10 V				
		G = 16	103	119		dB
		G = 16, T_A = –40°C to +105°C	98			dB
		G = 8	100	113		dB
		G = 8, T_A = –40°C to +105°C	98			dB
		G = 4	94	107		dB
		G = 4, T_A = –40°C to +105°C	92			dB
		G = 2	88	101		dB
		G = 2, T_A = –40°C to +105°C	86			dB
		G = 1	82	95		dB
		G = 1, T_A = –40°C to +105°C	80			dB
		G = 0.5	83	95		dB
		G = 0.5, T_A = –40°C to +105°C	80			dB
		G = 0.25	80	95		dB
		G = 0.25, T_A = –40°C to +105°C	75			dB
Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$[2, 7]	CMRRIO	V_{OCM} = ±13 V	75	95		dB
POWER SUPPLY REJECTION RATIO						
Differential Power Supply Rejection Ratio ($\Delta V_S/\Delta V_{OSDIFF}$)[2, 8]	PSRR	V_S = ±4.5 V to ±18 V				
		G = 16	105	142		dB
		G = 8	102	139		dB
		G = 4	102	136		dB
		G = 2	100	133		dB
		G = 1	98	130		dB
		G = 0.5	95	125		dB
		G = 0.25	92	120		dB
Output Common Mode Power Supply Rejection Ratio ($\Delta V_S/\Delta V_{OSCM}$)[2, 8]	PSRRCM	V_S = ±4.5 V to ±18 V	110	135		dB
OUTPUT[2]						
Output Voltage, High, Either Output Pin	V_{OUT}	I_L = 0 mA, V_S = ±4.5 V	V^+_{OUT} – 0.6	V^+_{OUT} – 0.3		V
		I_L = –5 mA, V_S = ±4.5 V	V^+_{OUT} –1.1	V^+_{OUT} – 0.7		V
		I_L = 0 mA, V_S = ±15 V	V^+_{OUT} – 1.8	V^+_{OUT} – 1.1		V
		I_L = –5 mA, V_S = ±15 V	V^+_{OUT} – 1.9	V^+_{OUT} – 1.3		V
Output Voltage, Low, Either Output Pin	V_{OUT}	I_L = 0 mA, V_S = ±4.5 V		V^- + 0.3	V^- + 0.6	V
		I_L = 5 mA, V_S = ±4.5 V		V^- + 0.6	V^- + 1	V
		I_L = 0 mA, V_S = ±15 V		V^- + 1.1	V^- + 1.8	V
		I_L = 5 mA, V_S = ±15 V		V^- + 1.2	V^- + 1.9	V
Output Short-Circuit Current, Either Output Pin, Sinking	I_{SC}	V_S = ±4.5 V	27	39		mA
		V_S = ±15 V	35	47		mA
Output Short-Circuit Current, Either Output Pin, Sourcing	I_{SC}	V_S = ±4.5 V	23	33		mA
		V_S = ±15 V	29	38		mA

SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	BAL	$V_{OUTDIFF}$ = ±10 V				
		Single-ended input		–80	–70	dB
		Differential input		–90	–75	dB
COMMON MODE GAIN ($\Delta V_{OUTCM}/\Delta V_{OCM}$)[2]	G_{CM}	V_S = ±4.5 V, V_{OCM} = ±3 V		1		V/V
		V_S = ±15 V, V_{OCM} = ±13 V		1		V/V
Common Mode Gain Error 100 × (G_{CM} – 1)	ΔG_{CM}	V_S = ±4.5 V, V_{OCM} = ±3 V		0.05	0.1	%
		V_S = ±15 V, V_{OCM} = ±13 V		0.05	0.1	%
COMMON MODE OFFSET VOLTAGE (V_{OUTCM} – V_{OCM})	V_{OSCM}			1	40	mV
		T_A = –40°C to +105°C			50	mV
V_{OCM} PIN[2]						
Voltage Range for the V_{OCM} Pin (Guaranteed by ΔG_{CM})	V_{OUTCMR}	V_S = ±4.5 V	V^- + 1.5		V^+_{OUT} – 1.5	V
		V_S = ±15 V	V^- + 2		V^+_{OUT} – 2	V
Self-Biased Voltage at the V_{OCM} Pin	V_{OCM}	V_{OCM} not connected	(V^+_{OUT} + V^-)/2 – 0.1	(V^+_{OUT} + V^-)/2	(V^+_{OUT} + V^-)/2 + 0.1	V
Input Resistance, V_{OCM} Pin	R_{INVOCM}		1.9	2.3	2.7	MΩ
DGND PIN[2]						
Voltage Range for the DGND Pin	V_{DGND}		V^-	0	V^+ – 2.5	V
DGND Pin Current	I_{DGND}	DGND = 5 V, A2 = A1 = A0 = 15 V	–7	–4	–1	µA
DIGITAL INPUT[2]						
Digital Input (A2/A1/A0) Logic Low	V_{IL}	Referred to DGND	DGND		DGND + 0.6	V
Digital Input (A2/A1/A0) Logic High	V_{IH}	Referred to DGND	DGND + 1.5		V^+	V
Digital Input (A2/A1/A0) Pin Current	$I_{A2/A1/A0}$	A2/A1/A0 = 5 V		8	12	µA
DYNAMIC RESPONSE						
–3 dB Bandwidth	f_{-3dB}	G = 16		4		MHz
		G = 8		5.5		MHz
		G = 4		6		MHz
		G = 2		6.5		MHz
		G = 1		6.5		MHz
		G = 0.5		7		MHz
		G = 0.25		7.5		MHz
Slew Rate[2]	SR	G = 16, $V_{OUTDIFF}$ = 40 V_{P-P} Step, R_L = 2 kΩ	7.5	12		V/µs
Settling Time	t_s	G = 16, $V_{OUTDIFF}$ = 8 V_{P-P} Step, R_L = 1 kΩ				
		0.1%		2.1		µs
		0.01%		2.25		µs
		0.0015% (16-bit)		2.4		µs
		4 ppm (18-bit)		2.7		µs
Total Harmonic Distortion	THD	G = 1, $V_{OUTDIFF}$ = 10 V_{P-P}, R_L = 2 kΩ				
		f = 1 kHz		–115		dB
		f = 10 kHz		–110		dB
TIMING CHARACTERISTICS						
Turn-On Time	t_{ON}			10		µs
Turn-Off Time	t_{OFF}			5		µs
Gain Switching Time				5		µs
SUPPLY						
Supply Voltage Range[2]	V_S	Guaranteed by PSRR	9		36	V
Supply Current	I_S	Active		4.4	4.75	mA
		T_A = –40°C to +105°C			5.25	mA
		Shutdown (A2 = A1 = A0 = 5 V)[2]		220	600	µA

SPECIFICATIONS

[1] This parameter is measured in a high speed automatic tester that does not measure the thermal effects with longer time constants. The magnitude of these thermal effects is dependent on the package used, PCB layout, heat sinking, and air flow conditions.

[2] This specification is applied over the full operating temperature range.

[3] Guaranteed by design.

[4] ESD (Electrostatic Discharge) sensitive device. ESD protection devices are used extensively internal to the LTC6373; however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

[5] Hysteresis in output voltage is created by mechanical stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. For instruments that are stored in well controlled temperatures (within 20 or 30 degrees of operational temperature), hysteresis is usually not a significant error source. Typical Hysteresis is the worst case of differential offset measured between 25°C to -40°C to 25°C thermal cycle and 25°C to 105°C to 25°C thermal cycle.

[6] Input bias current is defined as the maximum of the input currents flowing into either of the input pins (–IN and +IN). Input Offset current is defined as the difference between the input currents ($I_{OS} = I_B^+ – I_B^–$).

[7] Input CMRR (CMRR) is defined as the ratio of the change in the input common mode voltage at the pins +IN or –IN to the change in differential input referred offset voltage. Output CMRR (CMRRIO) is defined as the ratio of the change in the voltage at the VOCM pin to the change in differential input referred offset voltage.

[8] Differential power supply rejection ratio (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred offset voltage. Common mode power supply rejection ratio (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the common mode offset voltage.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages	
V^+	V^- to (V^- + 40 V)
V^+_{OUT}	V^- to (V^+ + 0.3 V)
V_{OCM}	(V^- – 0.3 V) to (V^+_{OUT} + 0.3 V)
A0, A1, A2, DGND	(V^- – 0.3 V) to (V^+ + 0.3 V)
+IN, –IN	
Common Mode	(V^- – 0.3 V) to (V^+ + 0.3 V)
Differential	±20 V
Output Current (+OUT, –OUT)[1]	40 mA_{RMS}
Output Short-Circuit Duration (+OUT, –OUT)[2]	Thermally Limited
Operating and Specified Temperature Range[3, 4]	
LTC6373I	–40°C to +85°C
LTC6373S	–40°C to +105°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	–65°C to +150°C

[1] The LTC6373 is capable of producing peak output currents in excess of 40 mA. Current density limitations within the IC require the continuous RMS current supplied by the output (sourcing or sinking) over the operating lifetime of the part be limited to under 40 mA (Absolute Maximum).

[2] A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

[3] The LTC6373I is guaranteed functional over the operating temperature range of –40°C to +85°C. The LTC6373S is guaranteed functional over the operating temperature range of –40°C to +105°C.

[4] The LTC6373I is guaranteed to meet specified performance from –40°C to +85°C. The LTC6373S is guaranteed to meet specified performance from –40°C to +105°C.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment. Careful attention to the printed circuit board (PCB) thermal design is required. θ_{JC} is the channel to case thermal resistance, channel to bottom of die using die attach epoxy.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
05-08-1791	43	3.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

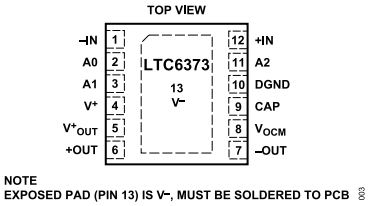

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN	Inverting Input of Instrumentation Amplifier. Input voltage range is between V^- + 3 V and V^+ – 3 V.
2	A0	Digital Gain Programming Pin 0. In combination with A2 and A1, the user can choose the desired gain setting for the LTC6373 (refer to Gain Selection section of this data sheet). The logic threshold for the A0 pin is specified with respect to the voltage on the DGND pin (logic low = any voltage between DGND and DGND + 0.6 V; logic high = any voltage between DGND + 1.5 V and V^+). If the A0 pin is left floating, an internal resistor pulls its voltage close to the DGND pin, resulting in a default logic low state for this programming pin.
3	A1	Digital Gain Programming Pin 1. In combination with A2 and A0, the user can choose the desired gain setting for the LTC6373 (refer to Gain Selection section of this data sheet). The logic threshold for the A1 pin is specified with respect to the voltage on the DGND pin (logic low = any voltage between DGND and DGND + 0.6 V; logic high = any voltage between DGND + 1.5 V and V^+). If the A1 pin is left floating, an internal resistor pulls its voltage close to the DGND pin, resulting in a default logic low state for this programming pin.
4	V^+	Positive Power Supply. The operating voltage range for V^+ is (V^- + 9 V) ≤ V^+ ≤ (V^- + 36 V).
5	V^+_{OUT}	Positive Power Supply for the Output Differential Amplifier inside the LTC6373 (the amplifier marked as A3 in Figure 76 of this data sheet). V^+_{OUT} pin is normally tied to V^+ pin, however the user may also choose a lower voltage for V^+_{OUT} to save power dissipation or to help protect ADC inputs. The voltage on V^+_{OUT} pin should never be higher than V^+ pin. The operating voltage range for V^+_{OUT} is (V^- + 9 V) ≤ V^+_{OUT} ≤ V^+.
6	+OUT	Positive Output Pin of Instrumentation Amplifier.
7	–OUT	Negative Output Pin of Instrumentation Amplifier.
8	V_{OCM}	Output Common Mode Reference Voltage. Voltage applied to this pin sets the output common mode voltage level. If the V_{OCM} pin is left floating, an internal resistor divider creates a default voltage approximately halfway between V^+_{OUT} and V^-. The V_{OCM} pin should be decoupled to ground with a minimum of 0.1 µF bypass capacitor.
9	CAP	Bypass Capacitor Pin. The CAP pin should be decoupled to ground with a 180 pF bypass capacitor.
10	DGND	Reference for Digital Gain Programming Pins (A2/A1/A0). DGND is normally tied to ground, however any voltage between V^- and V^+ – 2.5 V may also be chosen. If the DGND pin is left floating, an internal resistor divider creates a default voltage approximately halfway between V^+ and V^-. The logic threshold for A2/A1/A0 pins is specified with respect to the DGND pin.
11	A2	Digital Gain Programming Pin 2. In combination with A1 and A0, the user can choose the desired gain setting for the LTC6373 (refer to Gain Selection section of this data sheet). The logic threshold for the A2 pin is specified with respect to the voltage on the DGND pin (logic low = any voltage between DGND and DGND + 0.6 V; logic high = any voltage between DGND + 1.5 V and V^+). If the A2 pin is left floating, an internal resistor pulls its voltage close to the DGND pin, resulting in a default logic low state for this programming pin.
12	+IN	Noninverting Input of Instrumentation Amplifier. Input voltage range is between V^- + 3 V and V^+ – 3 V.
13	EPAD (V^-)	Exposed Pad (Negative Power Supply). The exposed pad must be soldered to PCB and connected to V^-.

TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V^+_{OUT}$ = 15 V, V^- = –15 V, $V_{ICM} = V_{OCM}$ = 0 V, T_A = 25°C, G = 1, unless otherwise noted.

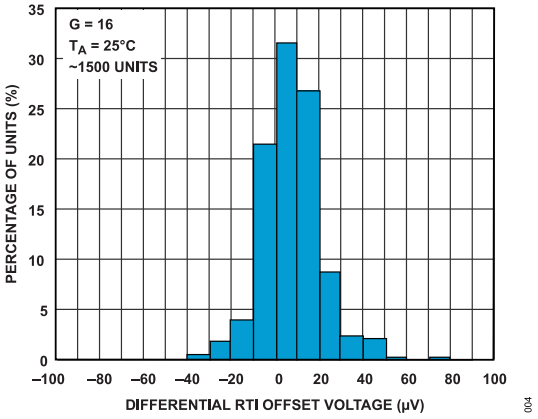

Figure 3. Typical Distribution of Differential RTI Offset Voltage

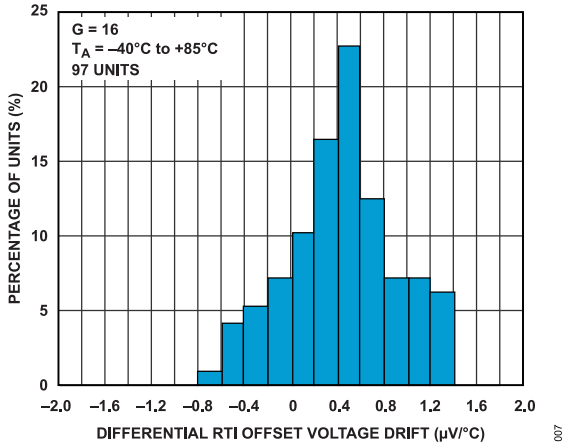

Figure 6. Typical Distribution of Differential RTI Offset Voltage Drift

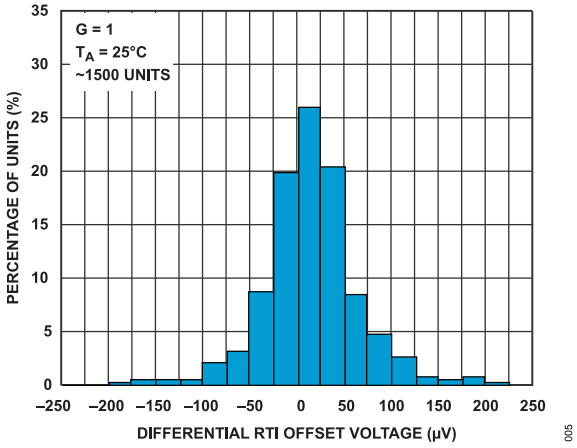

Figure 4. Typical Distribution of Differential RTI Offset Voltage

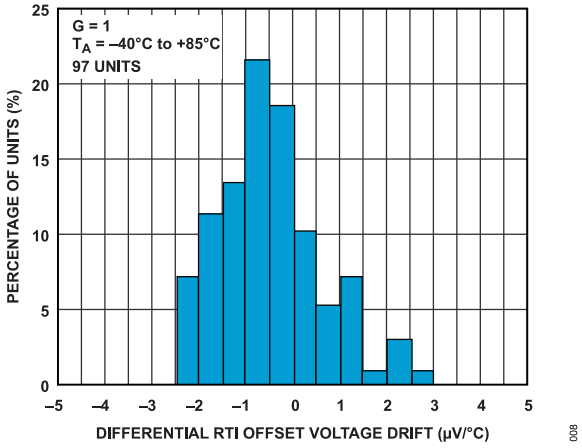

Figure 7. Typical Distribution of Differential RTI Offset Voltage Drift

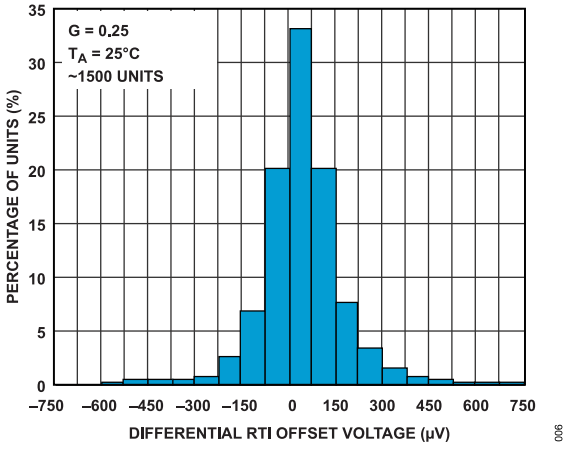

Figure 5. Typical Distribution of Differential RTI Offset Voltage

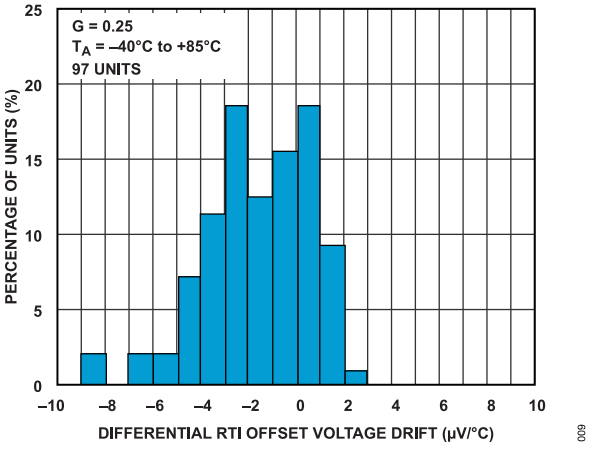

Figure 8. Typical Distribution of Differential RTI Offset Voltage Drift

TYPICAL PERFORMANCE CHARACTERISTICS

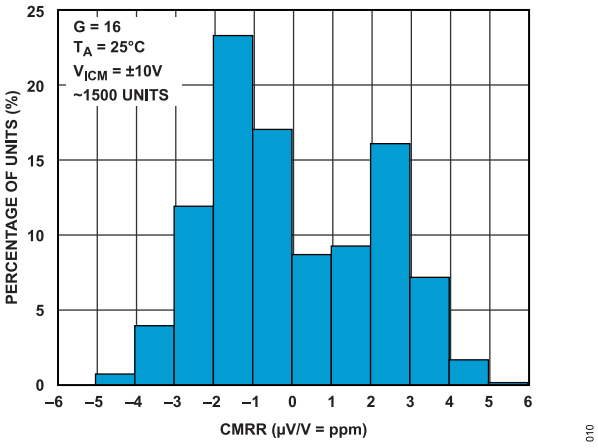

Figure 9. Typical Distribution of CMRR

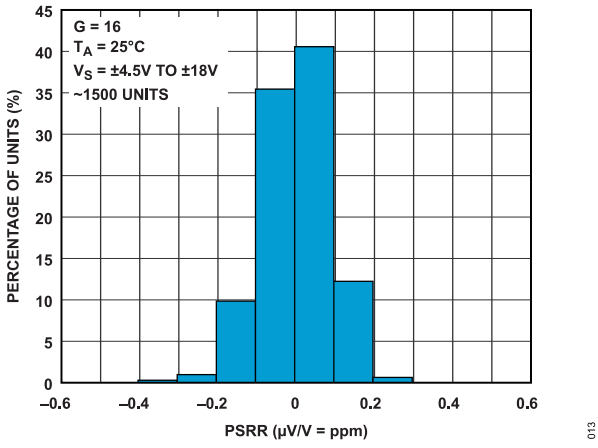

Figure 12. Typical Distribution of Differential PSRR

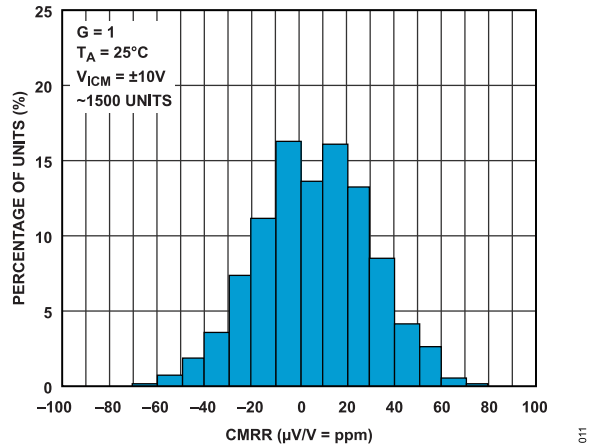

Figure 10. Typical Distribution of CMRR

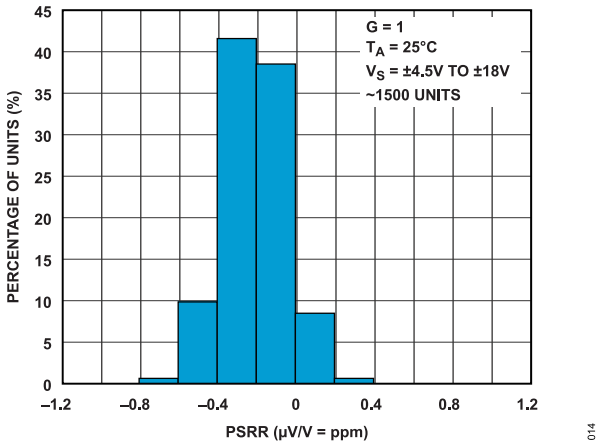

Figure 13. Typical Distribution of Differential PSRR

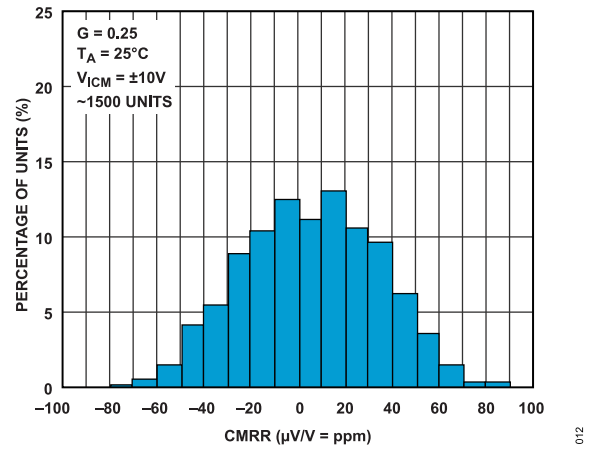

Figure 11. Typical Distribution of CMRR

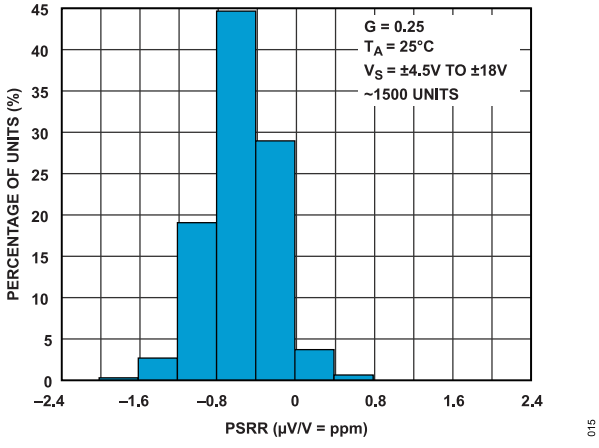

Figure 14. Typical Distribution of Differential PSRR

TYPICAL PERFORMANCE CHARACTERISTICS

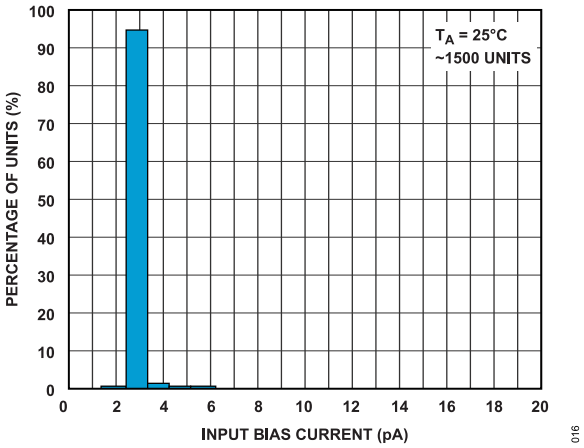

Figure 15. Typical Distribution of Input Bias Current

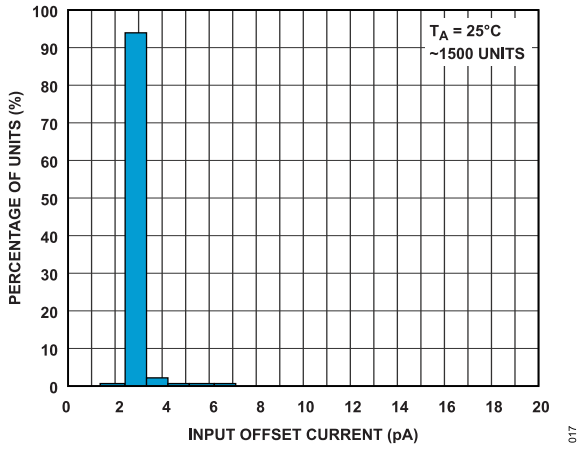

Figure 16. Typical Distribution of Input Offset Current

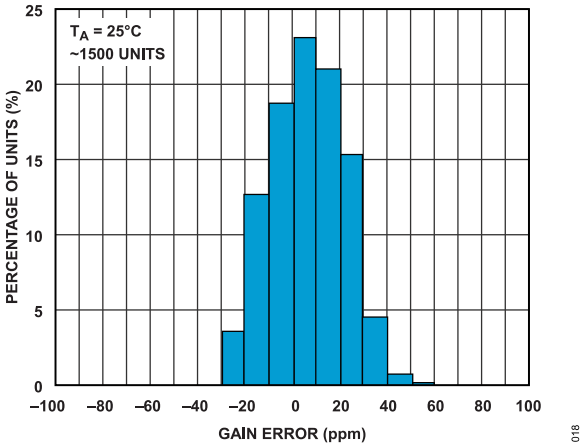

Figure 17. Typical Distribution of Differential Gain Error

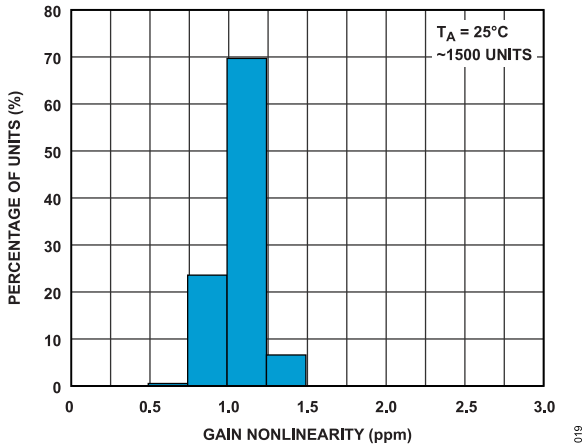

Figure 18. Typical Distribution of Differential Gain Nonlinearity

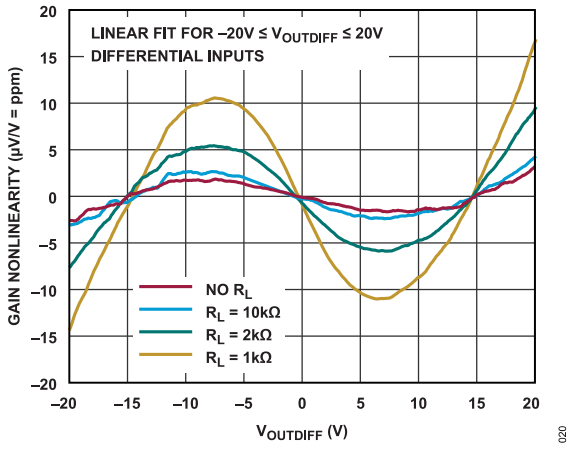

Figure 19. Differential Gain Nonlinearity vs. Output Voltage

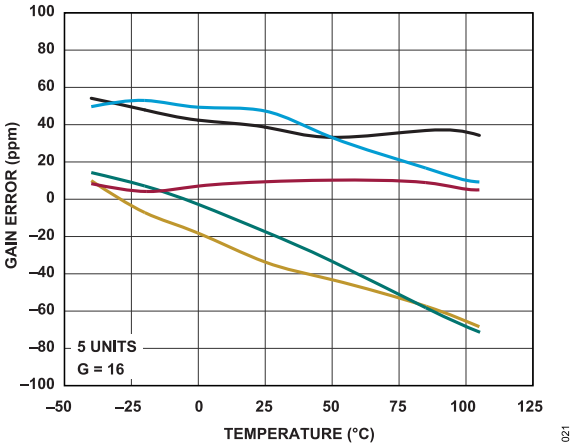

Figure 20. Differential Gain Error vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

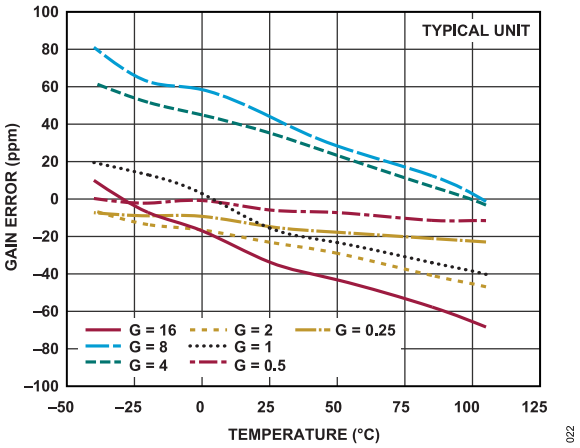

Figure 21. Differential Gain Error vs. Temperature

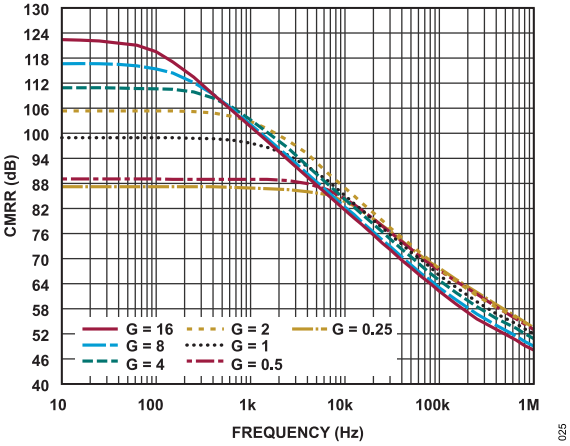

Figure 24. CMRR vs. Frequency

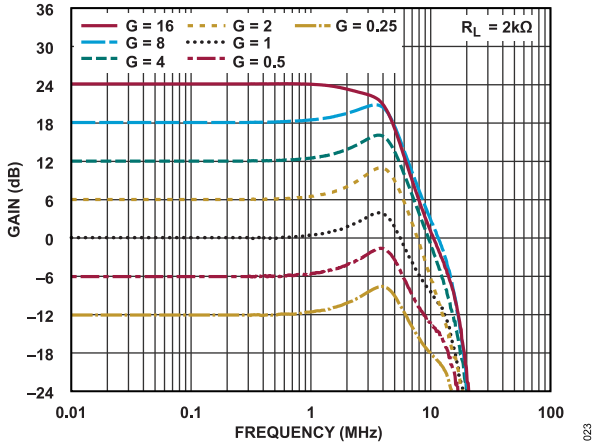

Figure 22. Gain vs. Frequency

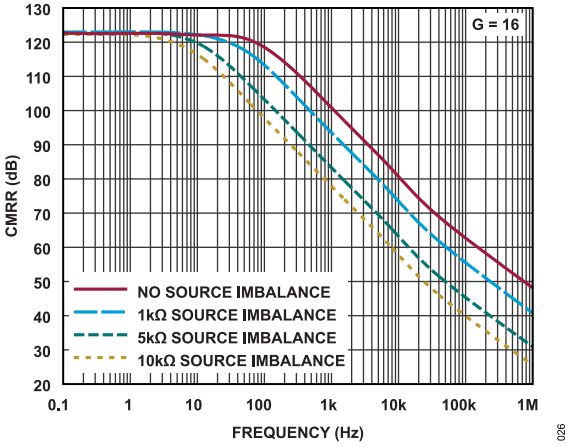

Figure 25. CMRR vs. Frequency With Source Imbalance

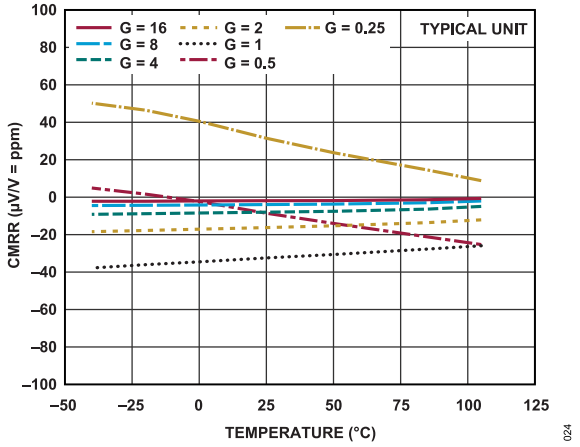

Figure 23. CMRR vs. Temperature

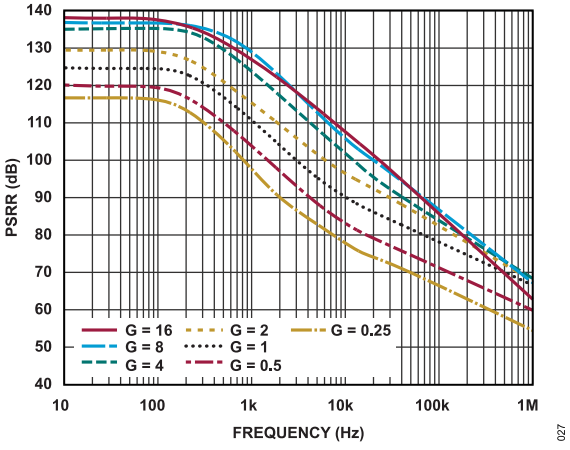

Figure 26. Positive PSRR vs. Frequency, RTI

TYPICAL PERFORMANCE CHARACTERISTICS

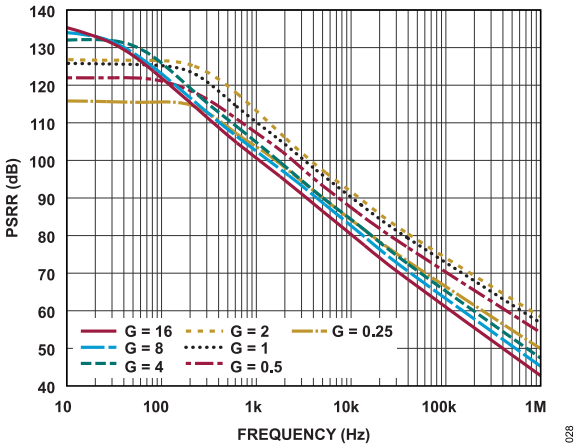

Figure 27. Negative PSRR vs. Frequency, RTI

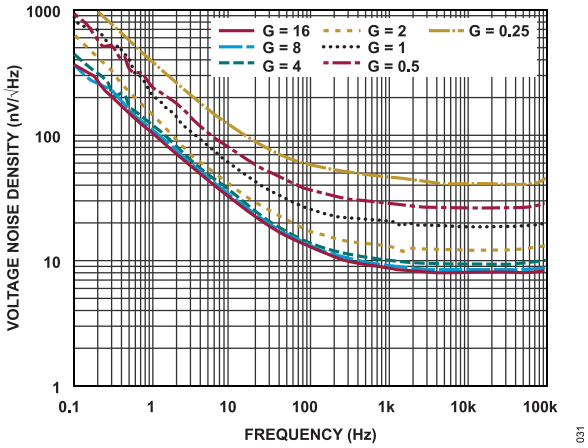

Figure 30. Input Referred Voltage Noise Density vs. Frequency

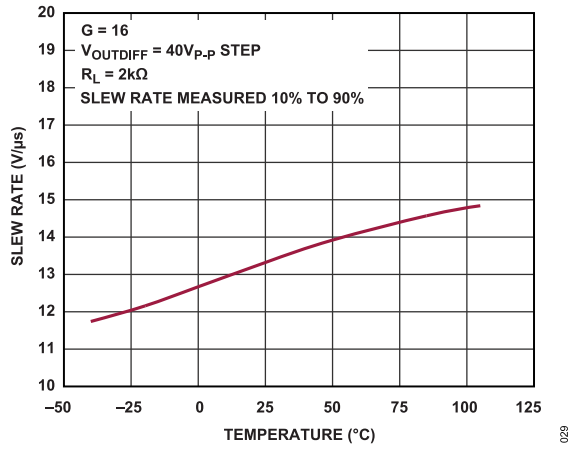

Figure 28. Slew Rate vs. Temperature

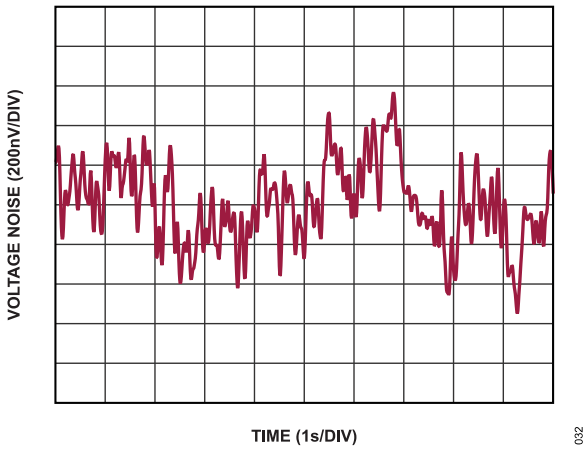

Figure 31. Input Referred 0.1 Hz to 10 Hz Voltage Noise (G = 16)

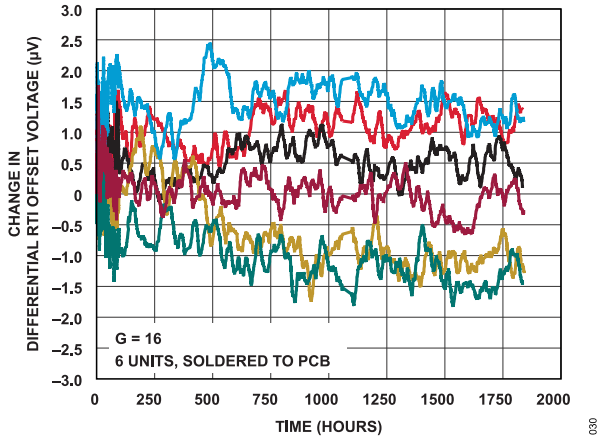

Figure 29. Long Term Differential RTI Offset Voltage Drift

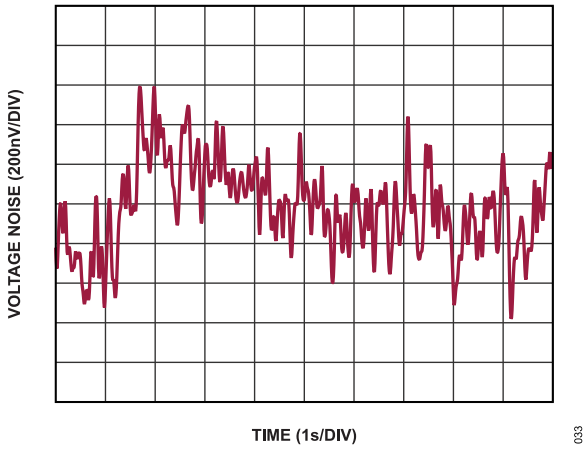

Figure 32. Input Referred 0.1 Hz to 10 Hz Voltage Noise (G = 8)

TYPICAL PERFORMANCE CHARACTERISTICS

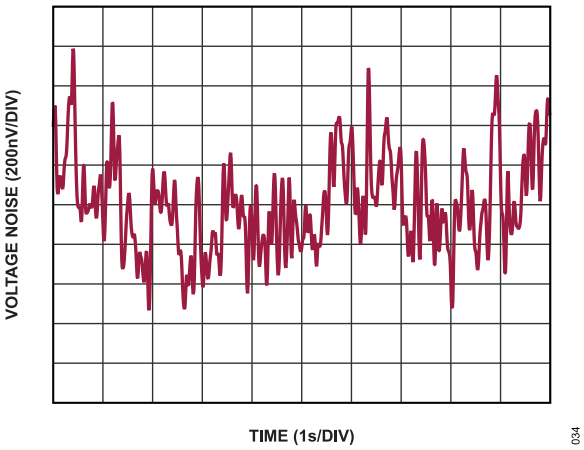

Figure 33. Input Referred 0.1 Hz to 10 Hz Voltage Noise (G = 4)

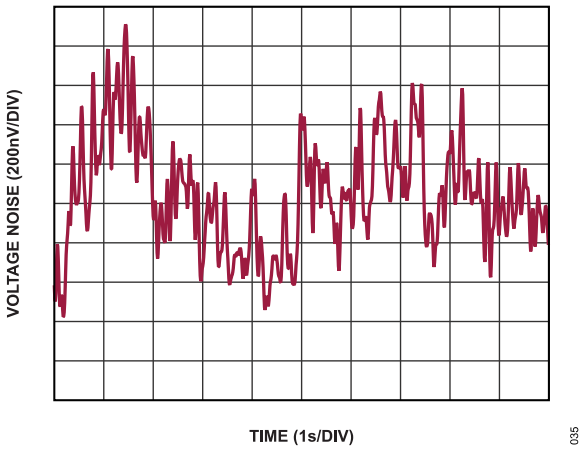

Figure 34. Input Referred 0.1 Hz to 10 Hz Voltage Noise (G = 2)

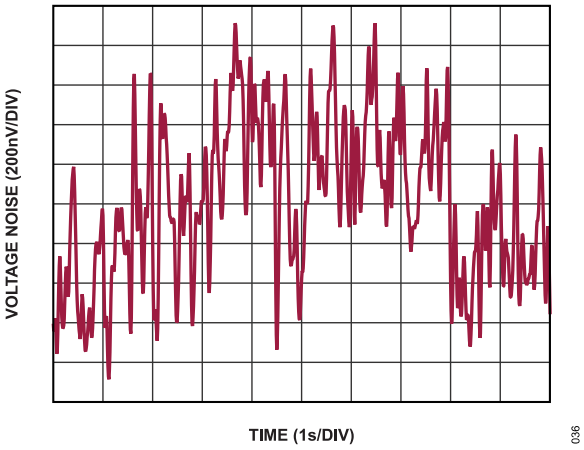

Figure 35. Input Referred 0.1 Hz to 10 Hz Voltage Noise (G = 1)

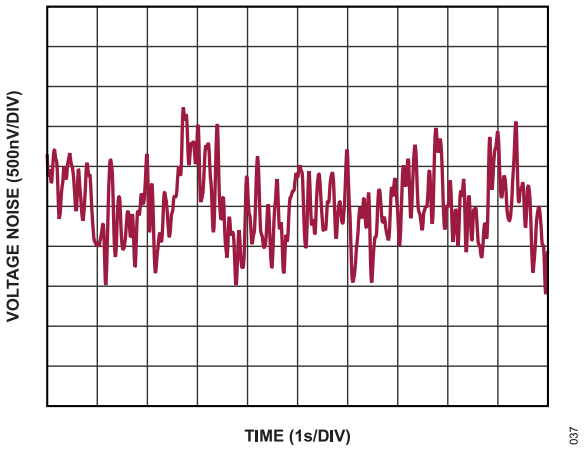

Figure 36. Input Referred 0.1 Hz to 10 Hz Voltage Noise (G = 0.5)

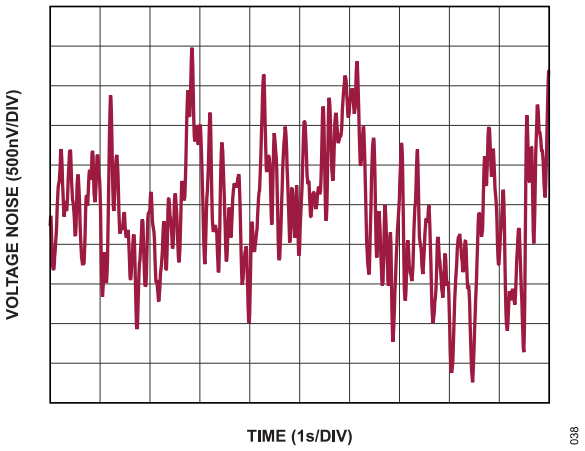

Figure 37. Input Referred 0.1 Hz to 10 Hz Voltage Noise (G = 0.25)

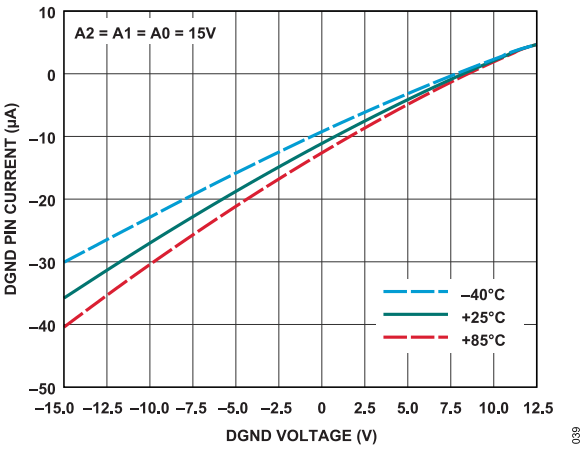

Figure 38. DGND Pin Current vs. DGND Pin Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

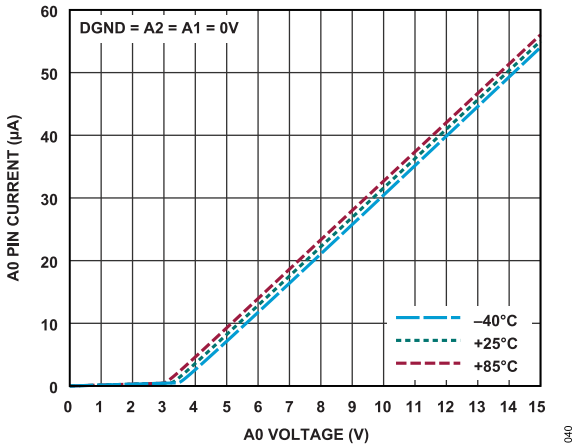

Figure 39. A0 Digital Input Pin Current vs. A0 Digital Input Pin Voltage

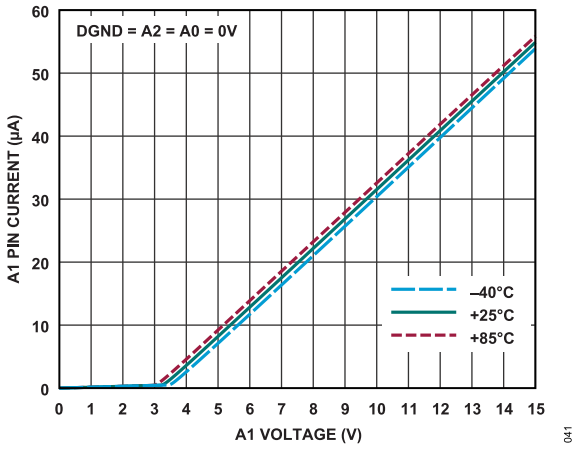

Figure 40. A1 Digital Input Pin Current vs. A1 Digital Input Pin Voltage

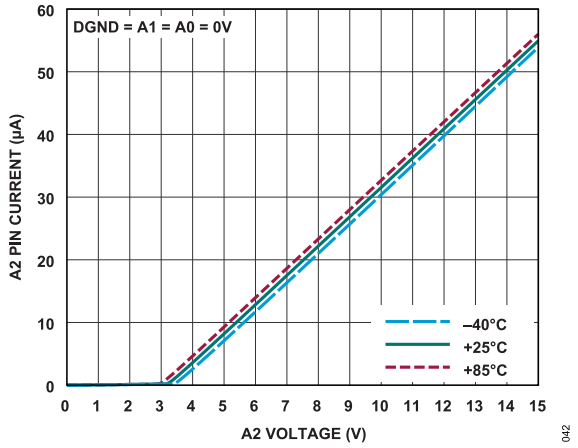

Figure 41. A2 Digital Input Pin Current vs. A2 Digital Input Pin Voltage

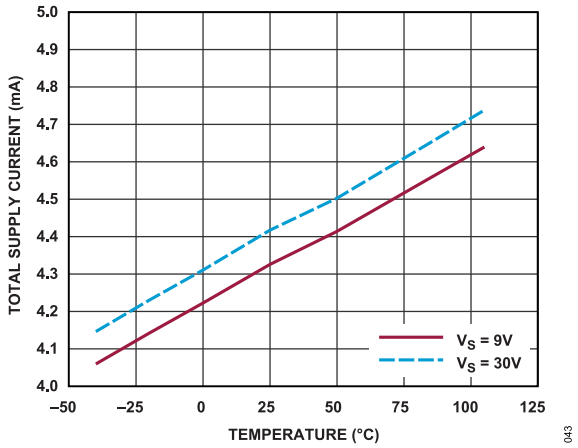

Figure 42. Supply Current vs. Temperature

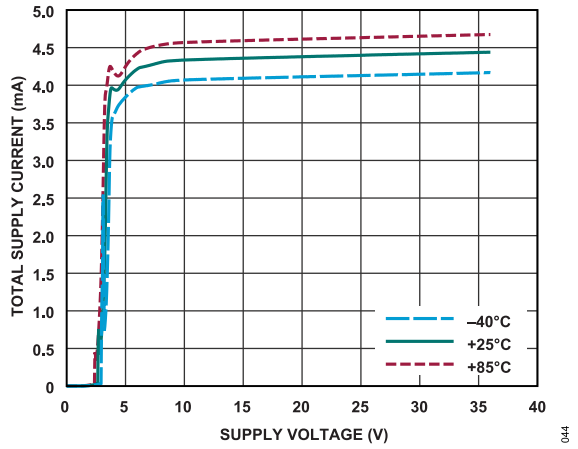

Figure 43. Supply Current vs. Supply Voltage

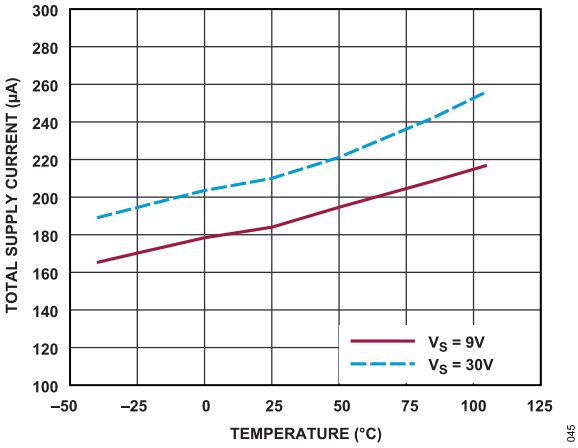

Figure 44. Shutdown Supply Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

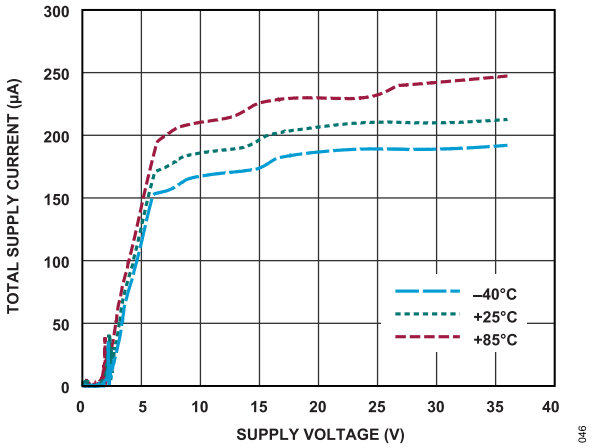

Figure 45. Shutdown Supply Current vs. Supply Voltage

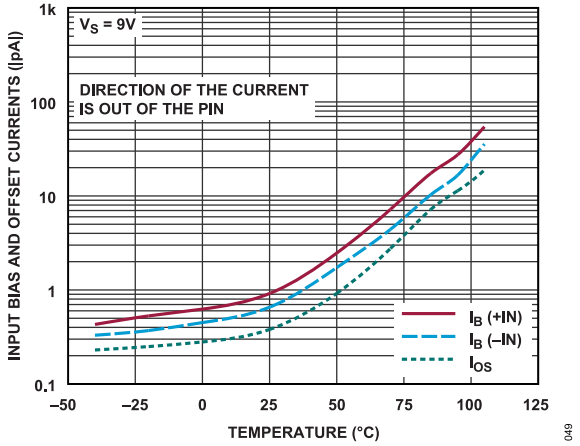

Figure 48. Input Bias Current and Offset Current vs. Temperature

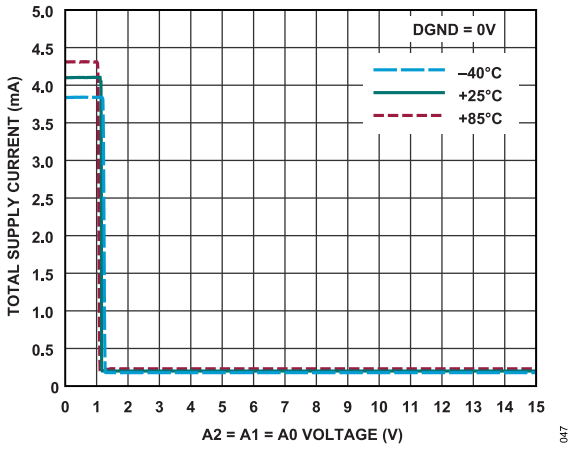

Figure 46. Supply Current vs Digital Input (A2/A1/A0) Pin Voltage

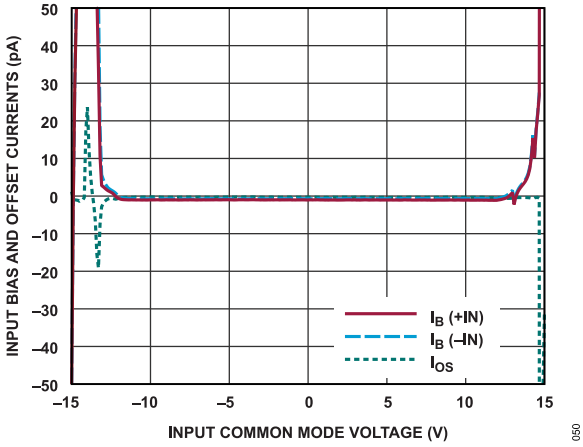

Figure 49. Input Bias Current and Offset Current vs. Input Common Mode Voltage

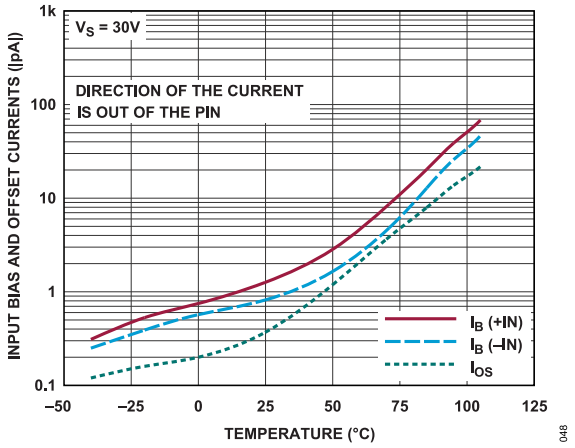

Figure 47. Input Bias Current and Offset Current vs. Temperature

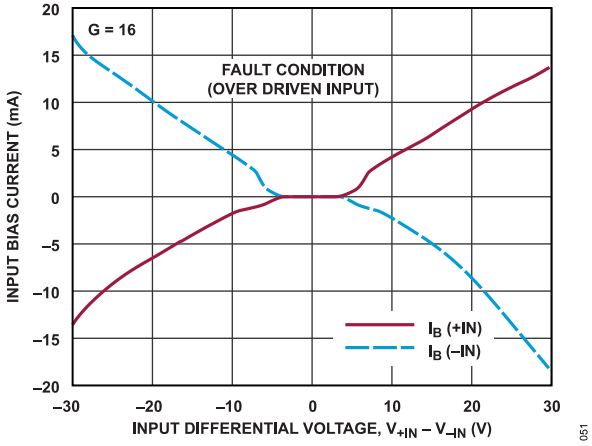

Figure 50. Input Bias Current vs. Input Differential Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

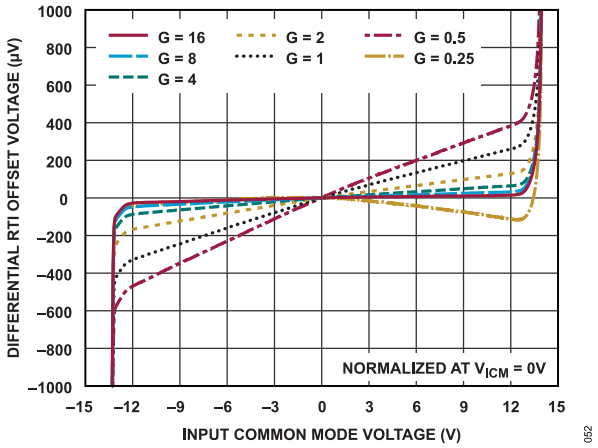

Figure 51. Differential RTI Offset Voltage vs. Input Common Mode Voltage

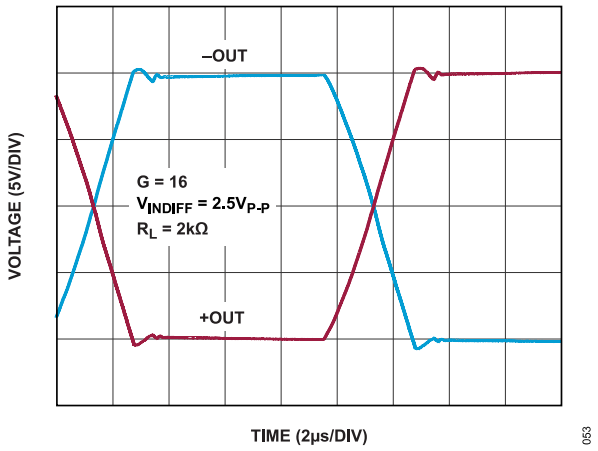

Figure 52. Large Signal Step Response

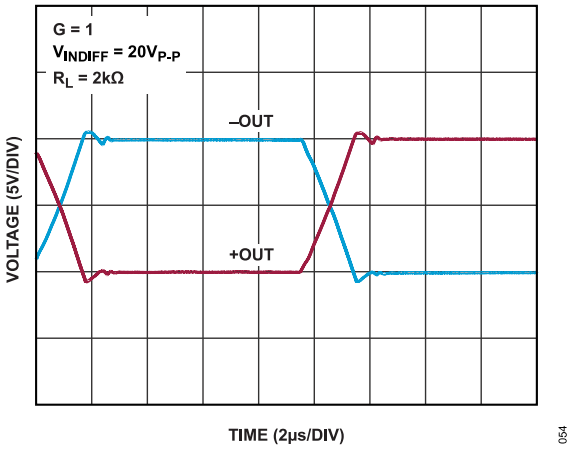

Figure 53. Large Signal Step Response

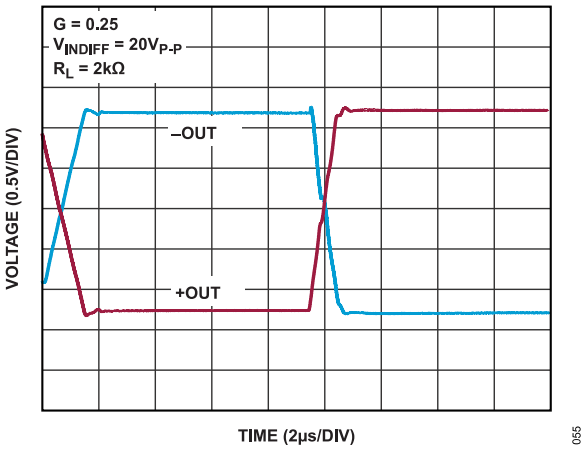

Figure 54. Large Signal Step Response

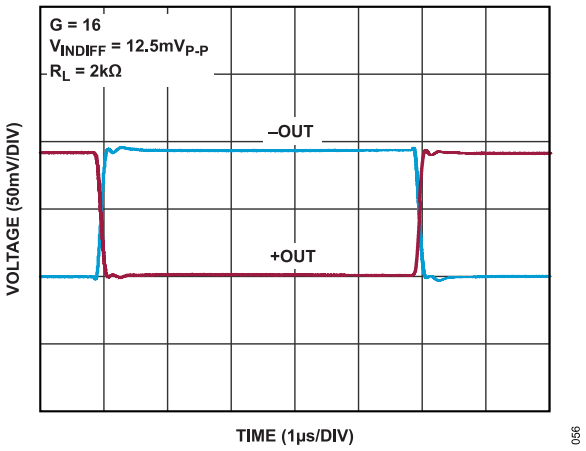

Figure 55. Small Signal Step Response

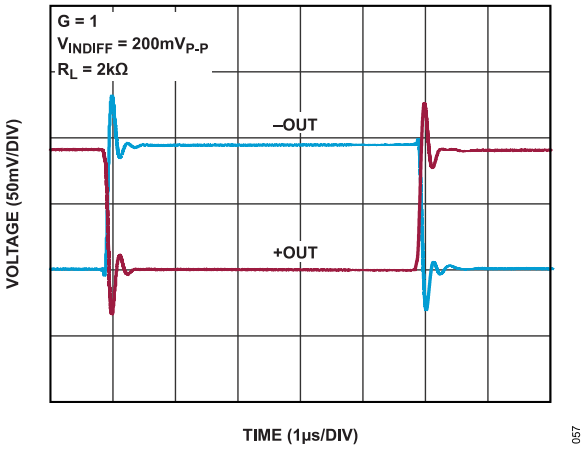

Figure 56. Small Signal Step Response

TYPICAL PERFORMANCE CHARACTERISTICS

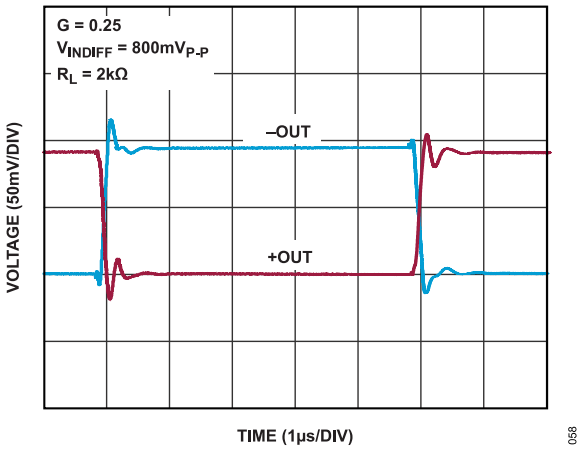

Figure 57. Small Signal Step Response

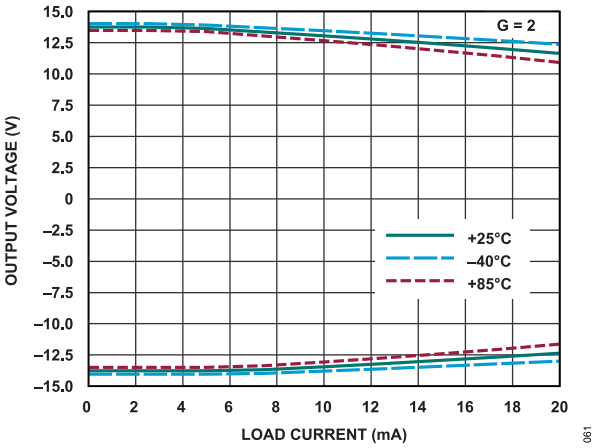

Figure 60. Output Voltage Swing vs. Load Current

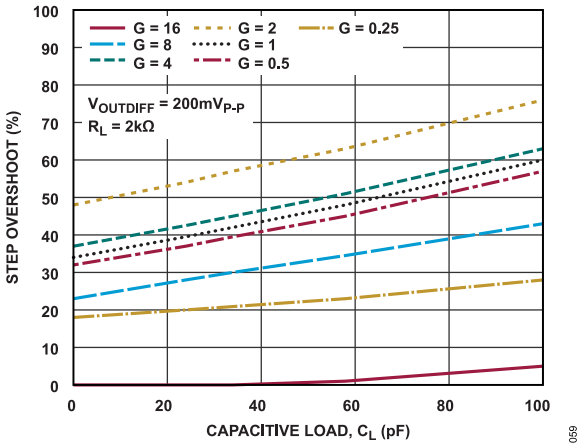

Figure 58. Small Signal Step Overshoot vs. Load Capacitance

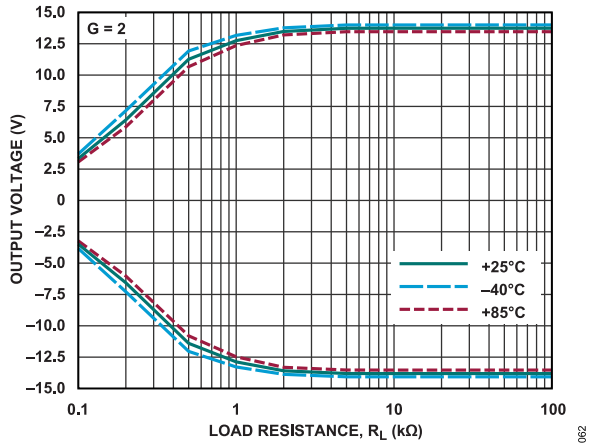

Figure 61. Output Voltage Swing vs. Load Resistance

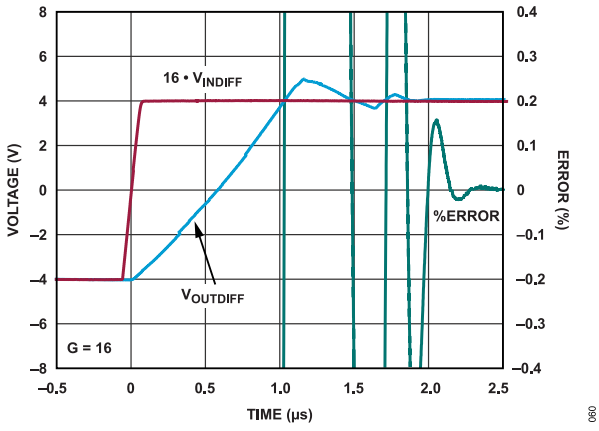

Figure 59. Settling Time to 8 V_{P-P} Output Step

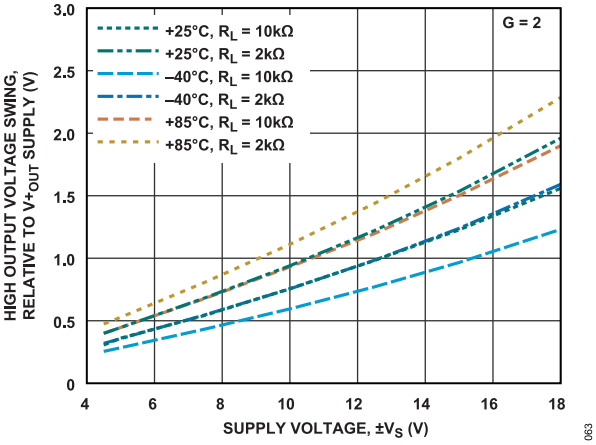

Figure 62. High Output Voltage Swing vs. Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

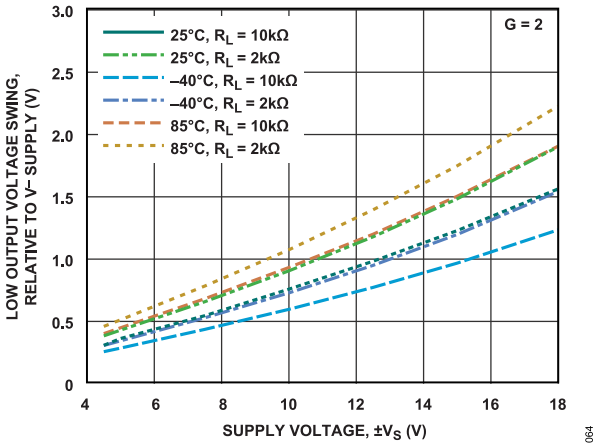

Figure 63. Low Output Voltage Swing vs. Supply Voltage

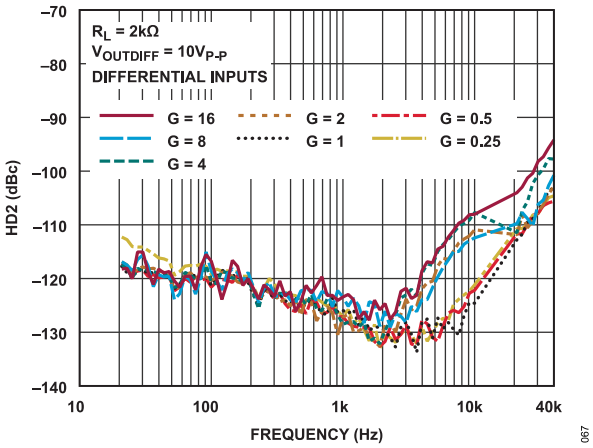

Figure 66. 2nd Harmonic Distortion vs. Frequency

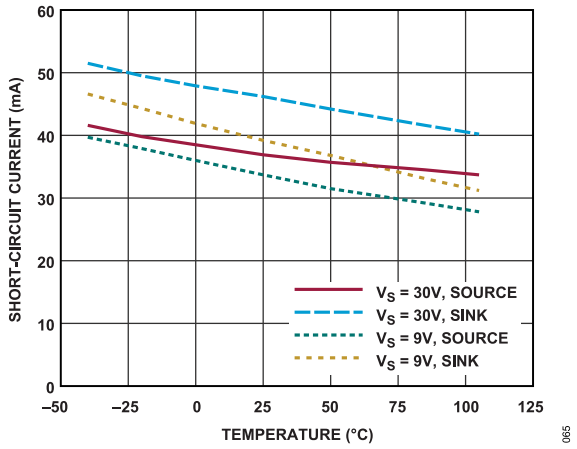

Figure 64. Output Short-Circuit Current vs. Temperature

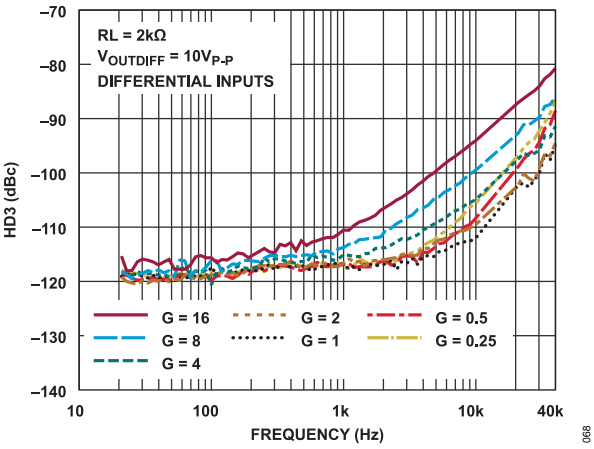

Figure 67. 3rd Harmonic Distortion vs. Frequency

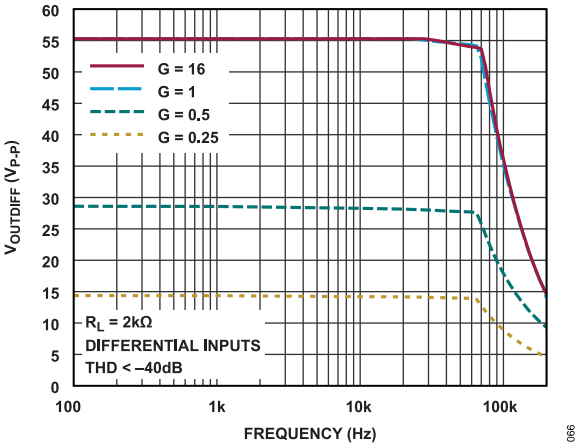

Figure 65. Maximum Undistorted Output Swing vs. Frequency

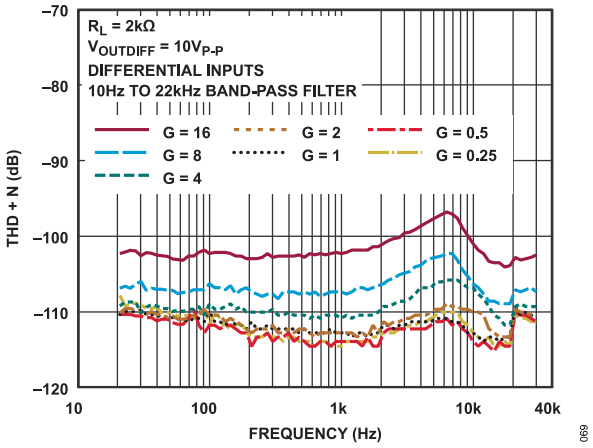

Figure 68. Total Harmonic Distortion + Noise vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

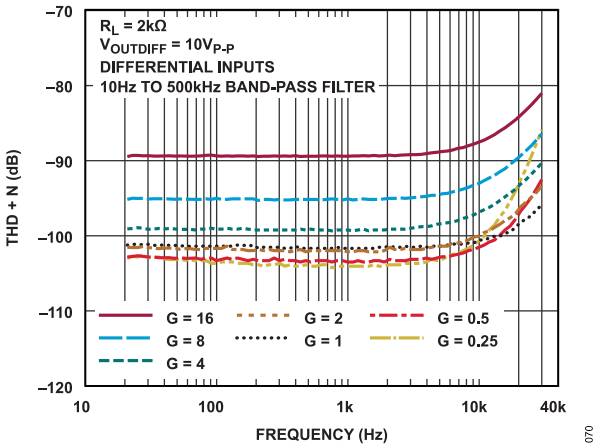

Figure 69. Total Harmonic Distortion + Noise vs. Frequency

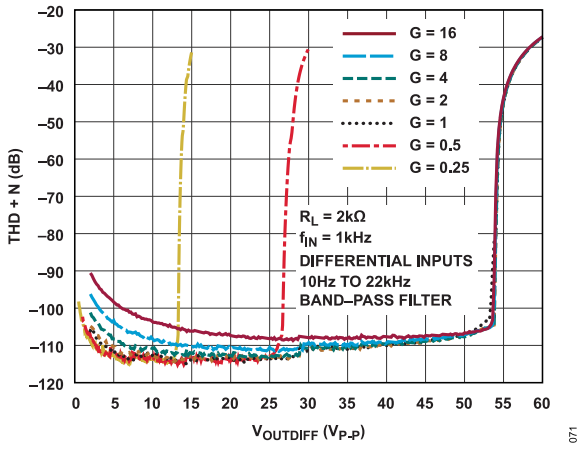

Figure 70. Total Harmonic Distortion + Noise vs. Output Amplitude

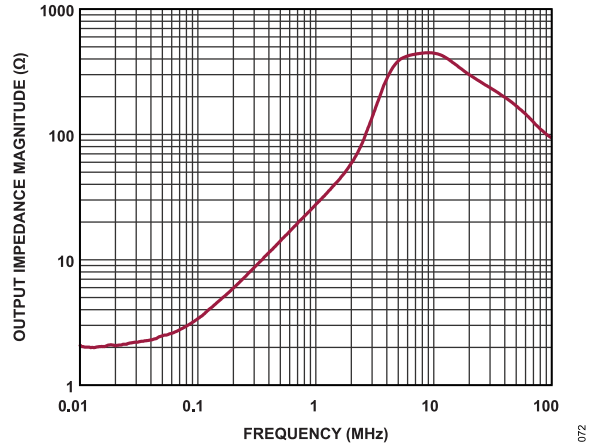

Figure 71. Differential Output Impedance vs. Frequency

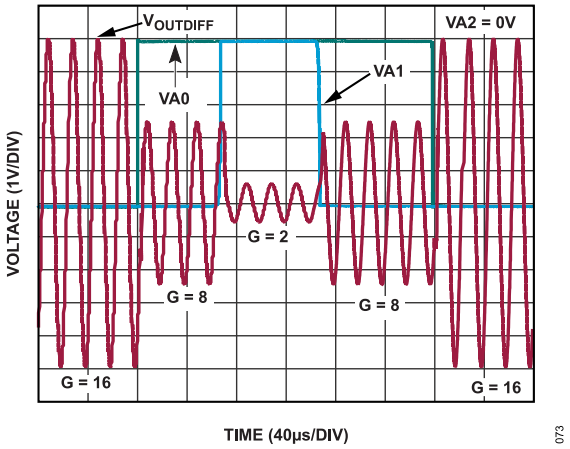

Figure 72. Gain Switching Transient Response

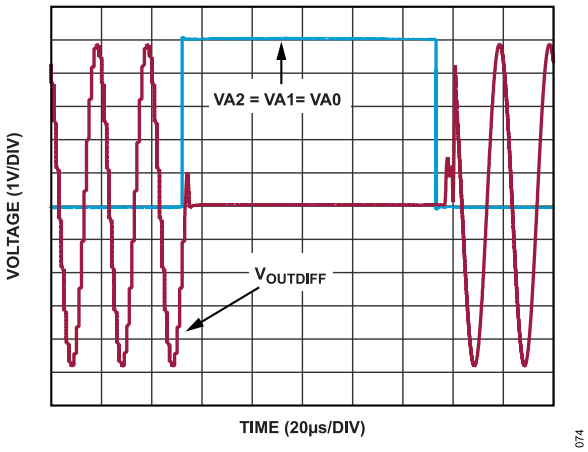

Figure 73. Turn-On and Turn-Off Transient Response

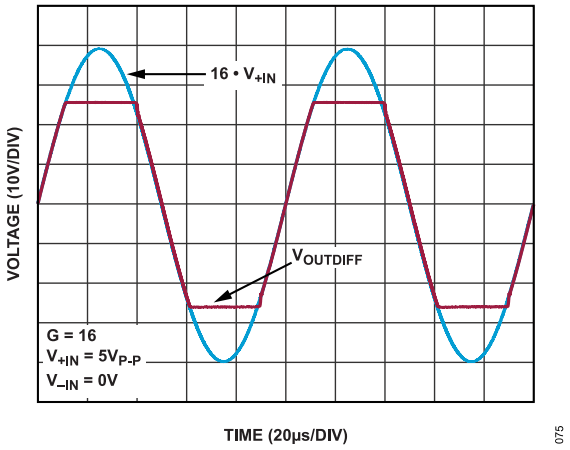

Figure 74. Output Overdrive Recovery

TYPICAL PERFORMANCE CHARACTERISTICS

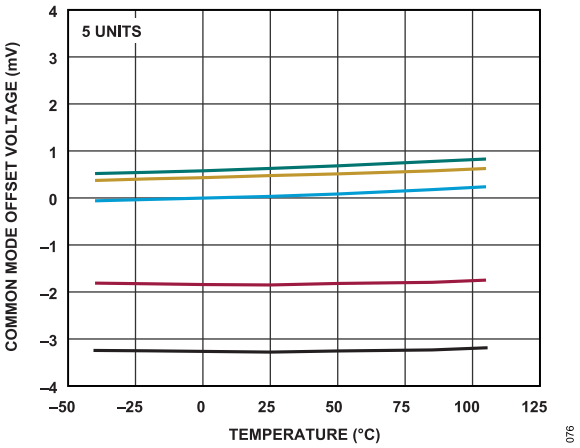

Figure 75. Common Mode Offset Voltage vs. Temperature

THEORY OF OPERATION

FUNCTIONAL DESCRIPTION

The LTC6373 is a monolithic instrumentation amplifier based on the classic 3-op-amp topology, as shown in the Block Diagram of Figure 76. A parallel interface allows users to digitally program gains to one of the seven available settings (G = 0.25, 0.5, 1, 2, 4, 8, and 16 V/V) while the 8th state puts the part in shutdown mode (which reduces the current drawn from the supplies to 220 µA). Gain control is achieved by switching resistors in an internal, precision resistor array (as shown in Figure 76). Although the LTC6373 has a voltage feedback topology, the gain-bandwidth product increases at higher gain settings because each gain has its own frequency compensation, resulting in increased bandwidth at higher gains and minimum phase variation across all gains.

The LTC6373 is optimized to convert a fully differential or single-ended input signal to a low impedance, balanced differential output suitable for driving high performance, analog-to-digital converters (ADCs). The balanced differential nature of the amplifier provides even-order harmonic distortion cancellation, and low susceptibility to common mode noise (like power supply noise). Load capacitances above 50 pF to ground or 25 pF differentially should be decoupled with 10 Ω to 50 Ω of series resistance from each output to prevent oscillation or ringing.

Overall, the LTC6373 simplifies signal chain design by offering:

- High impedance buffering (due to using CMOS technology and the resulting pA input bias current)
- Signal amplification (G > 1) and attenuation (G < 1) together in one socket at nearly the same bandwidth
- Digital gain programming (which enables changing gain settings easily and rapidly)
- Superior matching specs (due to trimmed, precision internal resistors)
- The ability to drive ADCs directly (due to attributes such as fully differential outputs, good DC precision, low noise, low distortion, and high bandwidth)
- Level shifting (achieved by using V_{OCM} pin to independently adjust the output common mode voltage to match it to the desired input level of the next stage of the signal chain).

The LTC6373 accommodates all the above features in a small 12-lead 4 mm × 4 mm DFN (LFCSP) package, making it an excellent solution for applications where size and packing density are important considerations.

THEORY OF OPERATION

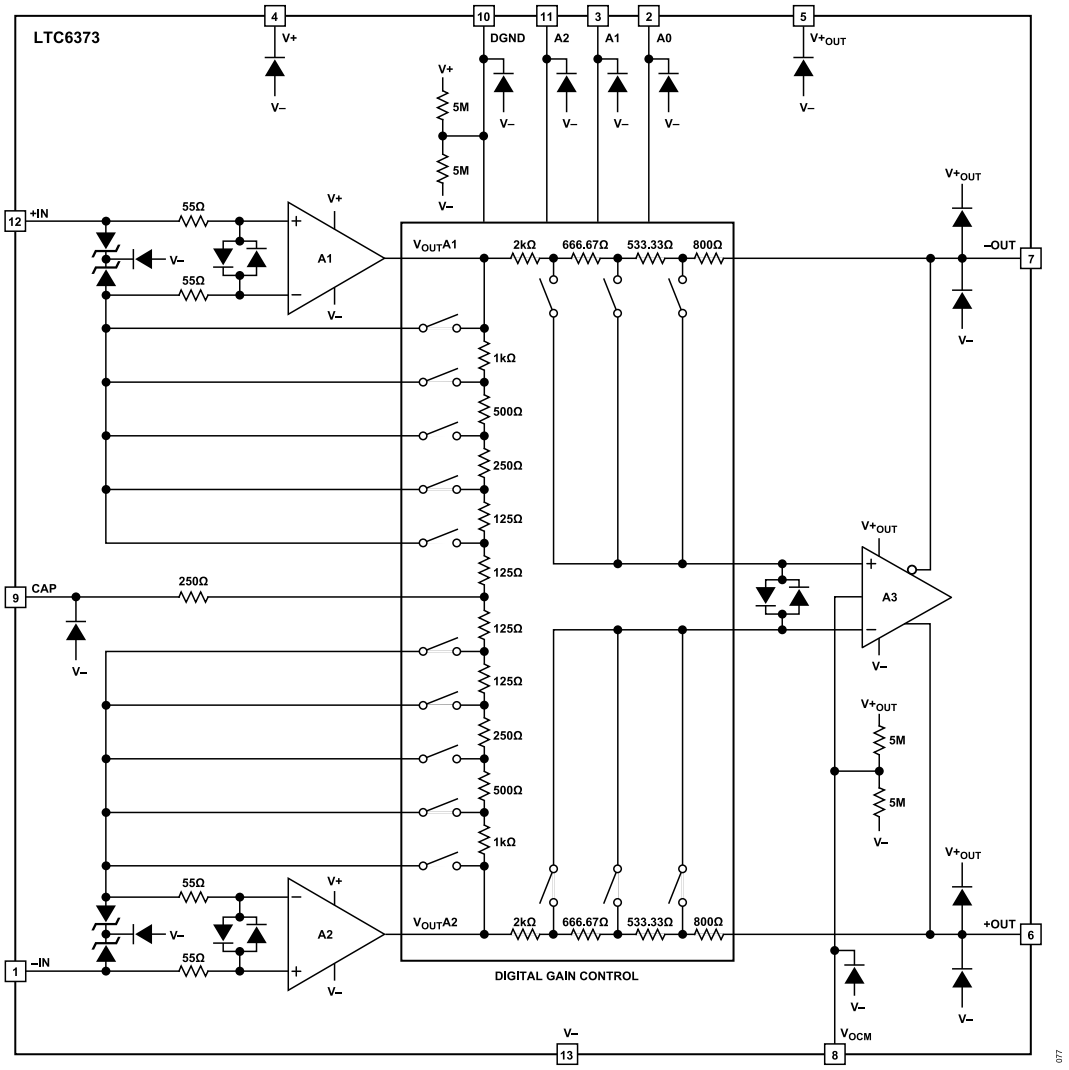

Figure 76. Simplified Block Diagram

APPLICATIONS INFORMATION

GAIN SELECTION

The gain of the LTC6373 can be programmed to its desired setting using a digital interface consisting of a digital reference pin DGND and three parallel gain programming pins A2, A1, and A0. The logic threshold for A2/A1/A0 pins is specified with respect to the voltage on the DGND pin. Any voltage between DGND and DGND + 0.6 V on A2 or A1 or A0 pins will generate a logic low (L) state for that pin; any voltage between DGND + 1.5 V and V^+ on A2 or A1 or A0 pins will generate a logic high (H) state for that pin. The gain for the LTC6373 is programmed according to the truth table below:

Table 5. Gain Selection Table for LTC6373

A2	A1	A0	G = Gain Setting (V/V)
L	L	L	16
L	L	H	8
L	H	L	4
L	H	H	2
H	L	L	1
H	L	H	0.5
H	H	L	0.25
H	H	H	Shutdown

The permissible voltage range for DGND is between V^- and V^+ – 2.5 V. However, typically DGND is tied to ground (0 V) and A2/A1/A0 pins can be connected to 0 V or 5 V to generate logic low (L) and logic high (H) states, respectively.

If the DGND pin is left floating, an internal resistor divider creates a default voltage approximately halfway between V^+ and V^-. Additionally, if A2 or A1 or A0 pins are left floating, internal resistors pull the voltage on each of these pins close to the DGND pin, resulting in a default logic low (L) state for that programming pin. As a result, if A2 and A1 and A0 pins are left floating all at the same time, the LTC6373 will have a gain setting of G = 16. When these pins are left open, care should be taken to control leakage currents at these pins to prevent inadvertently putting the LTC6373 into an undesired gain setting.

Keep in mind that any change in voltages applied to A2 or A1 or A0 pins from logic low to logic high (or vice versa) immediately results in a gain setting change for LTC6373 (transparent mode).

VALID INPUT AND OUTPUT RANGE

Instrumentation amplifiers traditionally specify a valid input common mode range and an output swing range. This however often fails to identify swing limitations associated with internal nodes, as they experience a combination of gained differential signal and common mode signal. Referring to the Simplified Block Diagram of Figure 76, the output swing of amplifiers A1, A2, and A3 as well as the common mode input range of the output differential amplifier A3 impose limitations on the valid operating range. The graphs in Figure 78 to Figure 84 show the maximum input common mode voltage limits where a valid output is produced for each gain setting of LTC6373.

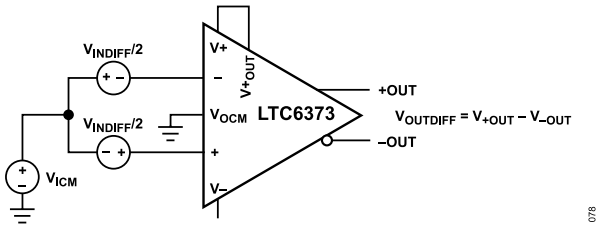

Figure 77. LTC6373 Input Configuration and Differential Output Calculation

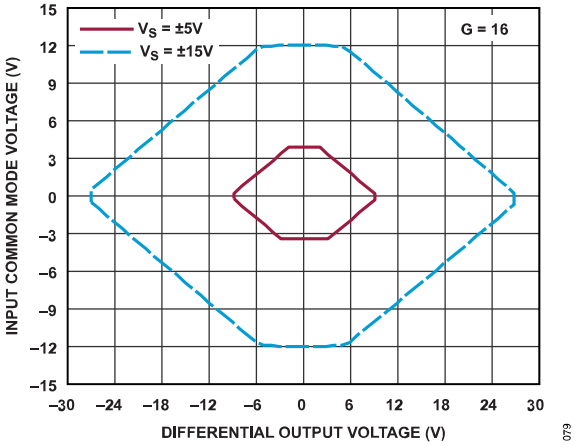

Figure 78. Input Common Mode Range vs. Differential Output Voltage at G = 16 with No Load

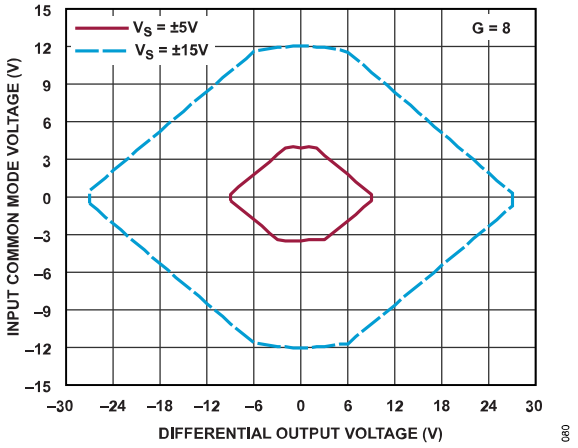

Figure 79. Input Common Mode Range vs. Differential Output Voltage at G = 8 with No Load

APPLICATIONS INFORMATION

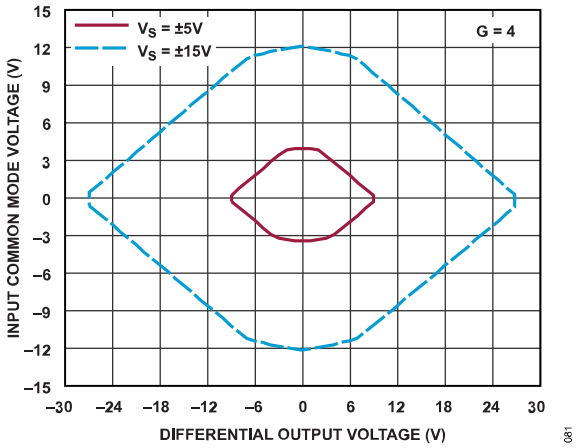

Figure 80. Input Common Mode Range vs. Differential Output Voltage at G = 4 with No Load

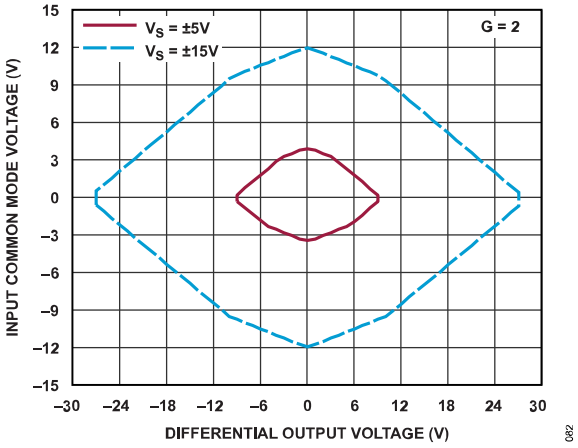

Figure 81. Input Common Mode Range vs. Differential Output Voltage at G = 2 with No Load

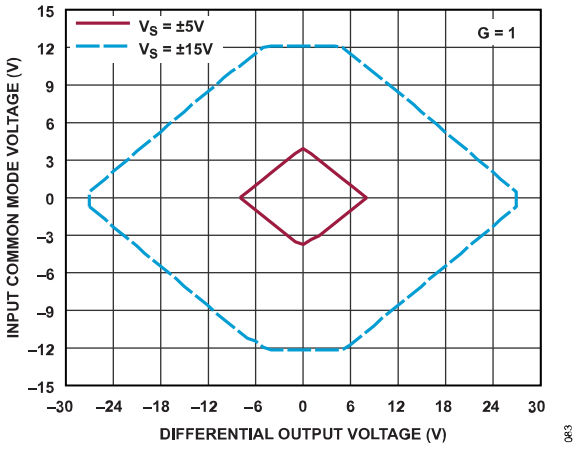

Figure 82. Input Common Mode Range vs. Differential Output Voltage at G = 1 with No Load

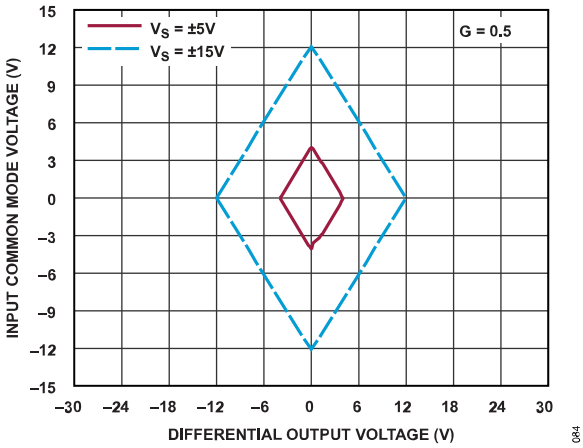

Figure 83. Input Common Mode Range vs. Differential Output Voltage at G = 0.5 with No Load

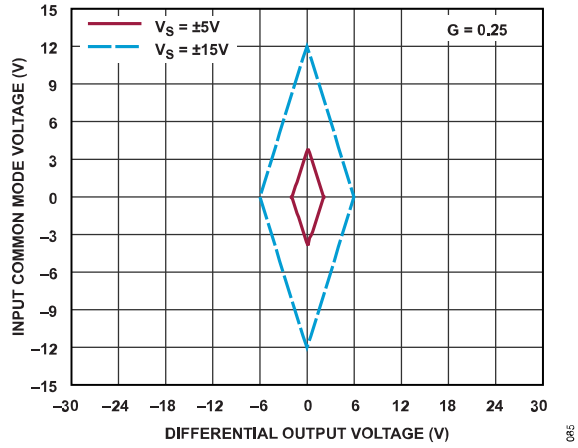

Figure 84. Input Common Mode Range vs. Differential Output Voltage at G = 0.25 with No Load

APPLICATIONS INFORMATION

DIAMOND PLOT INTERPRETATION

Diamond plots can be used to determine the valid input common mode voltage (V_{ICM}) operating range for instrumentation amplifiers such as LTC6373. The valid region of operation is where all signals, input or output, are not clipped.

Plots in Figure 78 to Figure 84 show the input common mode voltage (V_{ICM}) range allowed for a given differential output voltage ($V_{OUTDIFF}$), under various combinations of gain (G) and supply (V_S) settings. In each plot, the output stage positive supply pin V^+_{OUT} is tied to the main positive supply pin V^+, V_{OCM} = 0 V (mid-rail) and there is no load.

To identify the valid V_{ICM} range for a specific application: First, identify the gain and supply conditions that the LTC6373 will be operated under. Then, identify the range of valid differential output voltages ($V_{OUTDIFF}$) desired. For example, this could be the full-scale signal that is optimal for the subsequent ADC's SNR.

This combination of settings and output range implies a specific differential input signal (V_{INDIFF}) range, since $V_{INDIFF} = V_{OUTDIFF}/G$.

While the input signal's V_{INDIFF} is fixed when specific $V_{OUTDIFF}$ and G are chosen, the input signal's common mode voltage V_{ICM} is not, because the same V_{INDIFF} can be superimposed on many different V_{ICM} values.

The valid V_{ICM} range can be set by the swing limits on +IN and/or –IN, since V_{ICM} is the average of +IN and –IN. It can also be set by internal node swing limits, since the internal nodes are also operating with common mode voltage V_{ICM}, and these nodes must also be able to swing enough away from V_{ICM} to produce the gained-up output.

On a diamond plot, this valid region of operation for V_{ICM} for a specific output $V_{OUTDIFF}$ is indicated by the portion of the vertical line going straight up from $V_{OUTDIFF}$ that falls inside the diamond borders, as shown in Figure 85.

If the part's input common mode voltage is within the V_{ICM} borders of the diamond, there should be no problems with clipping. If the differential input signal is shifted by a V_{ICM} value that is outside of the diamond, either +IN or –IN (or internal nodes) will be clipped, or the output itself will hit the rails, and thus result in a clipped output.

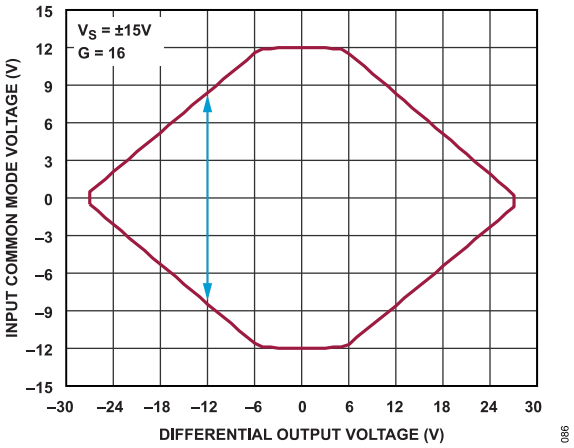

Figure 85. The Blue Arrow Indicates the Range of Valid V_{ICM} Values for $V_{OUTDIFF}$ = −12 V, Where No Signals are Clipped, for the V_S = ±15 V, G = 16 Case

The following example shows how a diamond plot point is determined. For the specific case of $V_{OUTDIFF}$ = −12 V as shown in Figure 85, the upper limit of V_{ICM} is 8 V, and the lower limit is −8 V.

For V_{ICM} = 8 V, if the gained-up input (aka output) is −12 V, the maximum negative internal node swing is 6 V above V_{ICM}. Referenced to ground, this internal node reaches 8 V + 6 V = 14 V, which is roughly the output high limit of LTC6373 with ±15 V supplies. If V_{ICM} were any higher than 8 V, the internal node would run into the output high limit, and the output would clip.

For V_{ICM} = −8 V, with −12 V output, the minimum positive internal node swing is −6 V below V_{ICM}. Referenced to ground, this internal node can hit a minimum of −6 V + (−8 V) = –14V, which is roughly the output low limit of LTC6373 with ±15 V supplies. If V_{ICM} were any lower than −8 V, this internal node would run into the output low limit, and the output would clip.

OUTPUT COMMON MODE AND V_{OCM} PIN

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = (V_{+OUT} + V_{–OUT})/2 = V_{OCM}$$

As the equation shows, the output common mode voltage is independent of the input common mode voltage, and is instead determined by the voltage on the V_{OCM} pin, by means of an internal common mode feedback loop. If the V_{OCM} pin is left floating, an internal resistor divider creates a default voltage approximately halfway between V^+_{OUT} and $V^–$. The V_{OCM} pin can be overdriven to another voltage if desired for greater accuracy or flexibility. For example, when driving an ADC, if the ADC makes a reference available for setting the common mode voltage, it can be directly tied to the V_{OCM} pin, as long as the ADC is capable of driving the 2.3 MΩ input resistance presented by the V_{OCM} pin. The Electrical Characteristics table specifies the valid range that can be applied to the V_{OCM} pin (V_{OUTCMR}).

APPLICATIONS INFORMATION

INPUT PIN PROTECTION

To prevent damage, the LTC6373 has a comprehensive protection scheme, especially on the input pins, as illustrated in the Simplified Block Diagram of Figure 76. The input current applied to the LTC6373's input pins should be kept under ±10 mA. To achieve additional input protection, external series resistors and/or low leakage clamp diodes should be used.

REDUCING BOARD-RELATED LEAKAGE EFFECTS

Leakage currents can have a significant impact on system accuracy, particularly in high temperature and high voltage applications. Quality insulation materials should be used, and insulating surfaces should be cleaned to remove fluxes and other residues. For humid environments, surface coating may be necessary to provide a moisture barrier.

Leakage into the input pins reacts with the source resistance, creating an error directly at the input. As shown in Figure 86, this leakage can be minimized by enclosing the input connections with guard rings operated at a potential very close to that of the input pins. For the lowest leakage, amplifiers can be used to drive the guard rings. These buffers must have very low input bias current since that current will now be a leakage current.

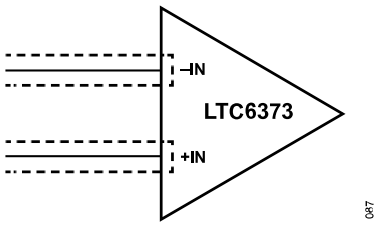

Figure 86. Guard Rings Can Be Used to Minimize Leakage into the Input Pins

INPUT BIAS CURRENT RETURN PATH

The low input bias current (25 pA max) and high input impedance (5000 GΩ) of the LTC6373 allow the use of high impedance sources without introducing additional offset voltage errors, even when the full common mode range is required. However, a DC path must be provided for the input bias currents of both inputs when a purely differential signal is being amplified. Without this path, the inputs will float to either rail and exceed the input voltage range of the LTC6373, resulting in a saturated input amplifier. Figure 87 shows three examples of an input bias current path. The first example is of a purely differential signal source with a 10 kΩ input current path to ground. Since the impedance of the signal source is low, only one resistor is needed. Two matching resistors are needed for higher impedance signal sources as shown in the second example. Balancing the input impedance improves both DC and AC common mode rejection as well as DC offset. The need for input resistors is eliminated if a center tap is present as shown in the third example.

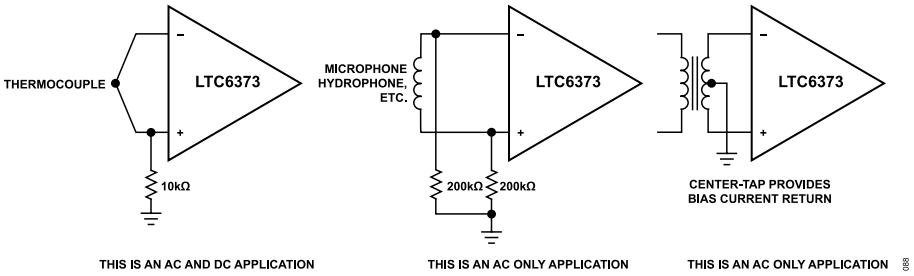

Figure 87. Providing an Input Common Mode Current Path

APPLICATIONS INFORMATION

RF INTERFERENCE

In many industrial and data acquisition applications, the LTC6373 will be used to process small signals accurately in the presence of large common mode voltages or high levels of noise. Typically, the sources of these very small signals (on the order of microvolts or millivolts) are sensors that can be a significant distance from the signal conditioning circuit. Although these sensors may be connected to signal conditioning circuitry using shielded or unshielded twisted-pair cabling, the cabling may act as an antenna, conveying very high frequency interference directly into the input stage of the LTC6373.

The amplitude and frequency of the interference can have an adverse effect on an instrumentation amplifier's input stage by causing an unwanted DC shift in the amplifier's input offset voltage. This well known effect is called RFI rectification and is produced when out-of-band interference is coupled (inductively, capacitively, or via radiation) and rectified by the instrumentation amplifier's input transistors. These transistors act as high frequency signal detectors, in the same way diodes were used as RF envelope detectors in early radio designs. Regardless of the type of interference or the method by which it is coupled into the circuit, an out-of-band error signal appears in series with the instrumentation amplifier's inputs.

To help minimize this effect, high frequency signals can be filtered with a low pass RC network placed at the input of the LTC6373, as illustrated in Figure 88.

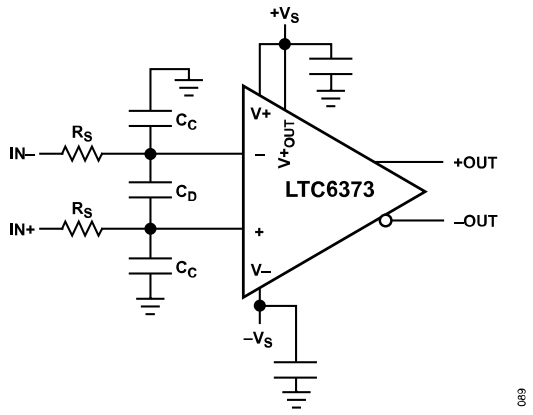

Figure 88. Adding a Simple External RC Filter at the Inputs of the LTC6373 Is Effective in Suppressing RF Interference.

The filter limits the input signal bandwidth according to the following formulas:

$FilterFreq_{DIFF} = 1/[2 \times \pi \times R_S \times (C_C + 2C_D)]$

$FilterFreq_{CM} = 1/[2 \times \pi \times R_S \times C_C]$

Setting the filter frequencies requires knowledge of the frequency (or frequencies) of the RF interference. Once the interference frequency is known, the common mode filter frequency can be set (low enough to filter out the interference frequency) followed by the differential mode filter frequency. To avoid any possibility of inadvertently affecting the differential signal of interest, set the common mode filter frequency an order of magnitude (or more) higher than the differential mode filter frequency. Set the common mode filter frequency such that it does not degrade the LTC6373's inherent AC CMRR. To avoid any possibility of common mode to differential mode signal conversion, match the common mode filter frequencies (on positive and negative inputs of LTC6373) to 1% or better. Then the differential mode filter frequency can be set for the bandwidth of the signal to be processed in the application. Setting the differential mode filter frequency close to the sensor's bandwidth also minimizes any noise pickup along the leads. If the sensor is an RTD or a resistive strain gauge in close proximity to the LTC6373, then the series resistors R_S can be omitted. As an example, if the bandwidth of the signal of interest is 100 kHz whereas the interference frequency is 10 MHz and above, an appropriate choice for differential mode filter ($FilterFreq_{DIFF}$) and common mode filter ($FilterFreq_{CM}$) frequencies could be 200 kHz/4 MHz. Assuming R_S is chosen to be 1 kΩ, using the formula provided earlier in this section results in C_C = 39 pF and C_D = 390 pF.

ERROR BUDGET ANALYSIS

Figure 89 shows the LTC6373 in a typical application to buffer and amplify the differential output of a bridge transducer. The LTC6373 is programmed to a gain of 8 V/V in this example and amplifies a differential, full-scale (FS) voltage of 100 mV = 0.1 V at transducer's output (or LTC6373's input). Table 6 shows the error budget in this application, listing various error sources in parts per million (ppm) normalized to full-scale voltage (0.1 V) and across the temperature range of 25°C to 85°C. The LTC6373 achieves superior performance compared to all other monolithic programmable-gain instrumentation amplifiers (PGIA) in the market, enabling more accurate measurements.

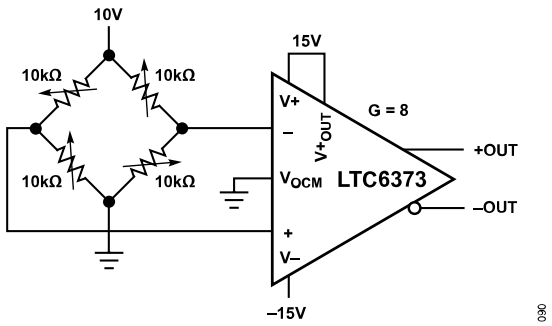

Figure 89. Precision Bridge Amplifier

APPLICATIONS INFORMATION

Table 6. Error Budget Analysis

	Calculation		Error, ppm of Input Full Scale (FS)	
Error Source	**LTC6373 (G = 8)**	**Closest Competitor PGIA (G = 8)**	**LTC6373 (G = 8)**	**Closest Competitor PGIA (G = 8)**
Absolute Accuracy at T_A = 25°C				
Gain Error	0.015% FS	0.05% FS	150	500
Offset Voltage (RTI)	(104 µV)/0.1 V	(1500 µV)/0.1 V	1040	15000
Input Offset Current	[(25 pA)(10 kΩ)/2]/0.1 V	[(100 pA)(10 kΩ)/2]/0.1 V	1	5
CMRR	[(5 V)/(100 dB)]/0.1 V	[(5 V)/(95 dB)]/0.1 V	500	889
		Total Accuracy Error	1691	16394
Temperature Drift to 85°C				
Gain Drift	(1 ppm/°C)(60°C)	(10 ppm/°C)(60°C)	60	600
Offset Voltage Drift (RTI)	[(1.8 µV/°C)(60°C)]/0.1 V	[(6 µV/°C)(60°C)]/0.1 V	1080	3600
		Total Drift Error	1140	4200
Resolution				
Gain Nonlinearity	3 ppm	20 ppm	3	20
Typ 0.1 Hz to 10 Hz Input Voltage Noise	(1.2 μV_{P-P})/ 0.1V	(1 μV_{P-P})/0.1 V	12	10
		Total Resolution Error	15	30
		Grand Total Error	2846	20624

DYNAMIC POWER CONSUMPTION CALCULATION

As shown in the Simplified Block Diagram of Figure 76, the LTC6373 has three internal chains of gain setting resistors. To achieve a low wideband noise for the LTC6373, a relatively small value, 4 kΩ, has been chosen for the total resistance of each chain. The voltages across the three chains are:

1. $V_{OUT}A1$ to –OUT
2. $V_{OUT}A2$ to +OUT
3. $V_{OUT}A1$ to $V_{OUT}A2$

Each of these voltages is imposed across what is effectively one 4 kΩ resistor, establishing currents in them. These three currents are independent of each other and the part's quiescent supply current (I_S), and all of them are drawn from the supplies.

For example, assume LTC6373 is being used with ±15 V supplies (i.e., $V^+ = V^+_{OUT}$ = 15 V, V^- = –15 V), V_{OCM} = 0 V, G = 2, and has input voltages of +IN = 3 V and –IN = –3 V (i.e., V_{ICM} = 0 V, V_{INDIFF} = 6 V). The resulting output voltage is $V_{OUTDIFF} = 2 \times V_{INDIFF}$ = 12 V. Since $V_{OUTCM} = V_{OCM}$ = 0 V, this implies that the value of LTC6373's output voltages are +OUT = 6 V, –OUT = –6 V.

Since the gain is applied in the A1 and A2 amplifiers, the output voltages of these internal amplifiers are $V_{OUT}A1$ = +6 V and $V_{OUT}A2$ = –6 V, respectively.

Thus, the voltages and currents in each 4 kΩ resistor chain are:

$I_1 = [(V_{OUT}A1) – (–OUT)]/4\ k\Omega = [6\ V – (–6\ V)]/4\ k\Omega = 3\ mA$

$I_2 = [(+OUT) – (V_{OUT}A2)]/4\ k\Omega = [6\ V – (–6\ V)]/4\ k\Omega = 3\ mA$

$I_3 = [(V_{OUT}A1) – (V_{OUT}A2)]/4\ k\Omega = [6\ V – (–6\ V)]/4\ k\Omega = 3\ mA$

Therefore, the total supply current is:

$I_{TOTAL} = I_S + I_1 + I_2 + I_3 = 4.4\ mA + 3 \times 3\ mA = 13.4\ mA$

In case the output pins (+OUT, −OUT) of the LTC6373 connect to resistive loads, the currents provided by the LTC6373 to these loads should also be added to the calculations above.

BOARD LAYOUT AND BYPASS CAPACITORS

It is recommended that high quality 0.1 µF ceramic bypass capacitors be placed directly between the V^+ pin and the V^- pin (exposed pad), between V^+ and ground plane, and between V^- and ground plane with minimal routing. In applications where V^+_{OUT} pin is not directly connected to V^+, it is recommended that additional high quality 0.1 µF ceramic capacitors be used to bypass V^+_{OUT} to ground and V^+_{OUT} to V^-, again with minimal routing. Small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self-resonant frequency than leaded capacitors, and perform best with the LTC6373.

Always keep in mind the differential nature of the LTC6373. At the inputs, keep any (intended or parasitic) resistance and capacitance as balanced and symmetric as possible to preserve AC CMRR performance of the amplifier. Apply the same practice at the output, because it is equally critical that the load impedances seen by both outputs (intended or parasitic) be as balanced and symmetric as possible. This will help preserve the balanced operation of the LTC6373 that minimizes the generation of even-order harmonics and maximizes the rejection of common mode noise and signals.

To minimize thermocouple induced errors, further attention must be given to board layout and component selection. It is good practice to minimize the number of junctions in the LTC6373's input signal paths and avoid connectors, sockets, switches, and relays whenever possible. If such components are required, they should be selected for low thermal EMF characteristics. Furthermore, the number, type, and layout of junctions should be matched for both

APPLICATIONS INFORMATION

inputs with respect to thermal gradients on the circuit board. Doing so may involve deliberately introducing dummy junctions to offset unavoidable junctions.

The V_{OCM} pin should be bypassed to the ground plane with a high quality 0.1 µF ceramic capacitor. This will prevent common mode signals and noise on this pin from being inadvertently converted to differential signals and noise by impedance mismatches internally to the IC. Additionally, the CAP pin should be bypassed to the ground plane with a high quality 180 pF ceramic capacitor to ensure proper operation of LTC6373 across its different gain settings.

To prevent coupling noise onto LTC6373, shield fast switching digital signals where they are in proximity of analog signals on the board.

DRIVING HIGH PRECISION ADCS

The LTC6373 makes an excellent PGIA for use in data acquisition systems. Attributes such as fully differential outputs, good DC precision, low noise, low distortion, and high bandwidth enable LTC6373 to drive ADCs directly in many signal conditioning applications. The recommended list of precision SAR ADCs for use with the LTC6373 is shown in Table 7. The circuit in Figure 90 shows an example of the LTC6373 driving a precision ADC such as the AD4020 (a 20-bit, 1.8 Msps, SAR ADC) or AD7134 (a 24-bit, 1.5 Msps, Continuous-Time, ∑-Δ ADC). The LTC6373 is DC-coupled on the input and the output, which eliminates the need for a transformer to drive the ADC. The LTC6373 gain is programmed to its desired setting using A2/A1/A0 pins, as previously described in the Gain Selection section of this data sheet. In the example of Figure 90, the LTC6373 is being used in a differential input to differential output configuration with dual supplies of ±15 V. It can also be used in a single-ended input to differential output configuration.

The V_{OCM} pin is biased to $V_{REF}/2$ (which is provided directly by the ADC in some products). This achieves level shifting of the outputs of the LTC6373 to match the desired input common mode of the ADC. In Figure 90, each of the LTC6373 outputs swings between 0 V and V_{REF} (opposite in phase), thus providing 2 × V_{REF} peak-to-peak differential signal to the ADC inputs. In some cases, an RC network between the LTC6373 outputs and the ADC inputs is required providing a single-pole, low-pass filter to help reduce nonlinear charge kickback due to ADC input switching as well as limiting the broadband noise.

Table 7. Recommended SAR ADCs

Resolution (Bits)	Product	Max Throughput (Msps)	Power @ Max Throughput (mW)	Typical SNR (dB)
20	AD4020	1.8	15	100.5
	LTC2378-20	1	21	104
18	AD4003	2	16	100.5
	LTC2379-18	1.6	18	101.2
16	AD4001	2	16	96.2
	LTC2380-16	2	19	96.2

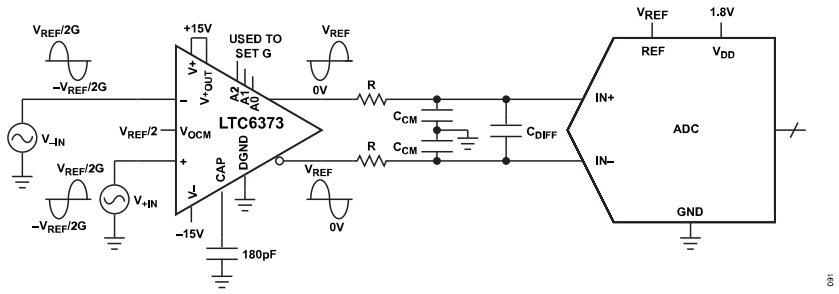

Figure 90. LTC6373 Driving Precision ADC (SAR ADC: Refer to Table 7; Σ-Δ ADC: AD7134)

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As a more specific example, Figure 91 and Figure 92 show typical Signal-to-Noise Ratio (SNR) and Total Harmonic Distortion (THD) of the LTC6373 driving the AD4020 SAR ADC (with high-Z mode enabled) at a near full-scale signal for various ADC throughputs. The recommended RC filter values used in Figure 90 for optimum performance at each throughput are listed in Table 8, as well as the selected reference voltage (V_{REF}).

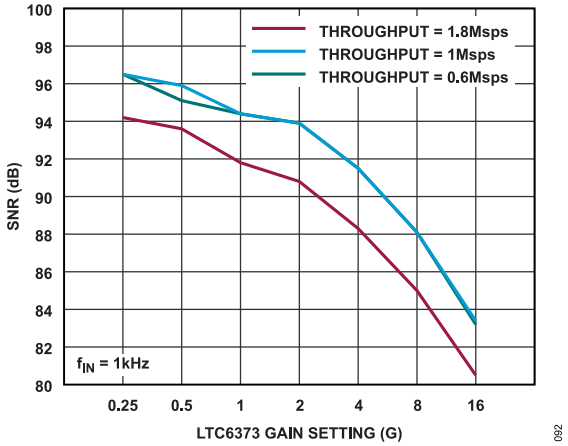

Figure 91. SNR for LTC6373 Driving AD4020

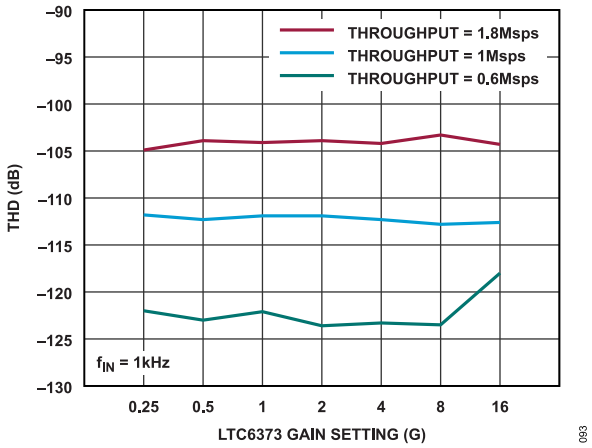

Figure 92. THD for LTC6373 Driving AD4020

Table 8. RC Filter Selection for LTC6373 Driving AD4020 (at Various Throughputs)

ADC	Throughput (Msps)	V_{REF} (V)	Signal Level at LTC6373 Outputs = ADC Inputs (V_{P-P})	R (Ω)	C_{CM} (pF)	C_{DIFF} (pF)	Typical SNR (dB)	Typical THD (dB)
AD4020	1.8	5	10	442	180	Open	See Figure 91	See Figure 92
	1	5	10	887	180	Open	See Figure 91	See Figure 92
	0.6	5	10	887	180	Open	See Figure 91	See Figure 92

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Table 9 lists the typical SNR and THD achieved when the ADC used in Figure 90 is AD7134 ∑-Δ ADC being driven directly (with no RC filter in between) by the LTC6373 at a near full-scale signal.

In some applications, it might be beneficial to use a separate amplifier/ADC driver between the LTC6373 and the precision ADC to ease the settling requirements on the LTC6373 and improve the linearity and THD performance of the signal chain. An implementation of such signal chain can be achieved by using the ADAQ4003, a precision data acquisition µModule which integrates multiple signal conditioning and processing blocks inside a single package. These blocks include a fully differential ADC driver, a stable reference buffer, an 18-bit, 2 Msps, SAR ADC, as well as critical passive components necessary for optimum performance. This µModule achieves 4X footprint reduction by itself (compared to discrete solution) without sacrificing any performance.

The ADAQ4003 offers pin-selectable gain or attenuation options, giving the user the flexibility to match to their input signal range. This is showcased in Figure 93–Figure 101 as LTC6373 is directly driving the ADAQ4003 at its 3 different gain options, in each case providing the signal amplitude necessary to utilize the maximum 2 × V_{REF} peak-to-peak differential signal range of the ADC inside the ADAQ4003 µModule.

Table 9. SNR and THD Results for LTC6373 Directly Driving AD7134 (at 250 ksps)

ADC	LTC6373 Gain Setting (G)	V_{REF} (V)	Signal Level at LTC6373 Outputs = ADC Inputs (V_{P-P})	R (Ω)	C_{CM} (pF)	C_{DIFF} (pF)	f_{IN} (kHz)	Typical SNR (dB)	Typical THD (dB)
AD7134	0.25	4.096	8.192	0	Open	Open	1	108.4	–124
							20	107.7	–97
	1	4.096	8.192	0	Open	Open	1	107.2	–121
							20	106.9	–100
	16	4.096	8.192	0	Open	Open	1	94.3	–112
							20	94.3	–93

Table 10. Details for LTC6373 Driving ADAQ4003 at 3 Different Gain Options and Signal Amplitudes

ADAQ4003 Gain	V_{REF} (V)	Signal Level at LTC6373 Outputs = ADAQ4003 Inputs (V_{P-P})	Circuit Configuration	Typical SNR (dB)	Typical THD (dB)
0.454	5	22	See Figure 93	See Figure 94	See Figure 95
0.9	5	11	See Figure 96	See Figure 97	See Figure 98
1.9	5	5.2	See Figure 99	See Figure 100	See Figure 101

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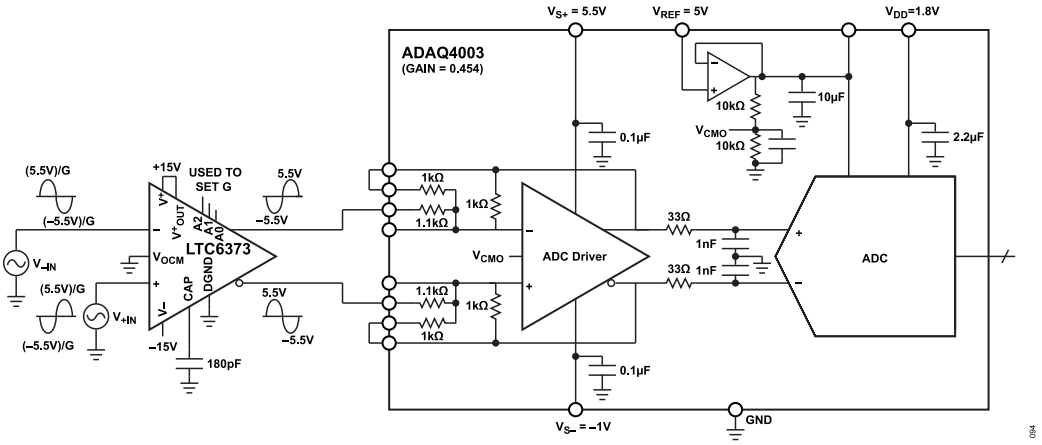

Figure 93. LTC6373 Driving ADAQ4003 (Gain = 0.454)

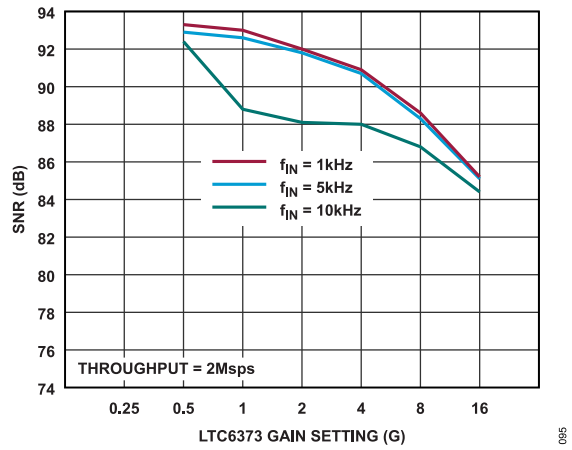

Figure 94. SNR for LTC6373 Driving ADAQ4003 (Gain = 0.454)

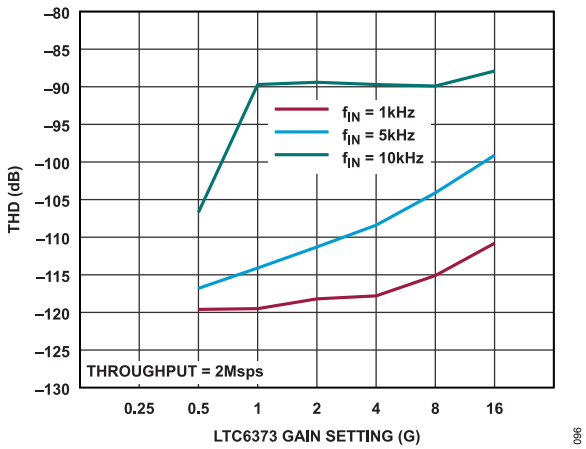

Figure 95. THD for LTC6373 Driving ADAQ4003 (Gain = 0.454)

APPLICATIONS INFORMATION

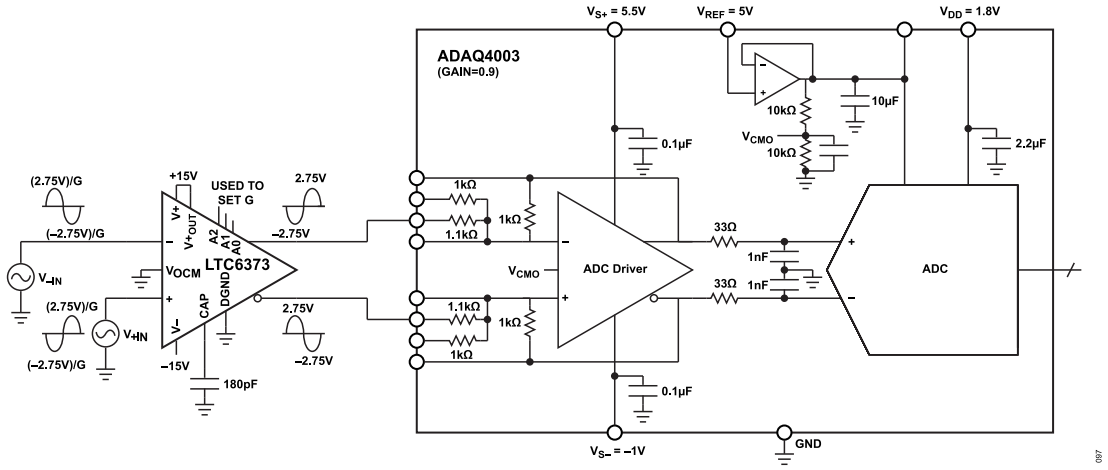

Figure 96. LTC6373 Driving ADAQ4003 (Gain = 0.9)

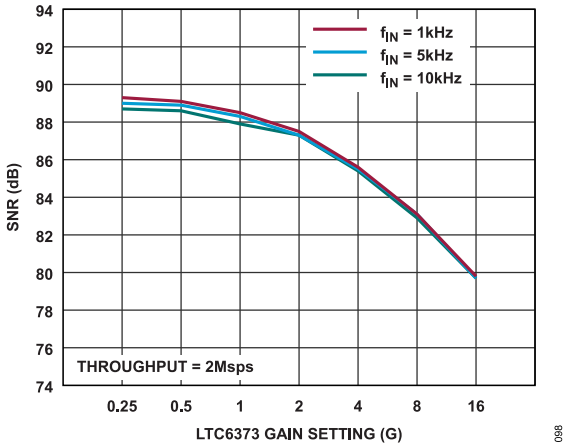

Figure 97. SNR for LTC6373 Driving ADAQ4003 (Gain = 0.9)

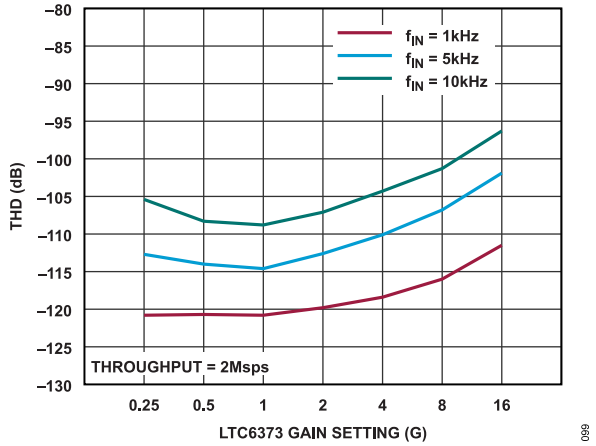

Figure 98. THD for LTC6373 Driving ADAQ4003 (Gain = 0.9)

APPLICATIONS INFORMATION

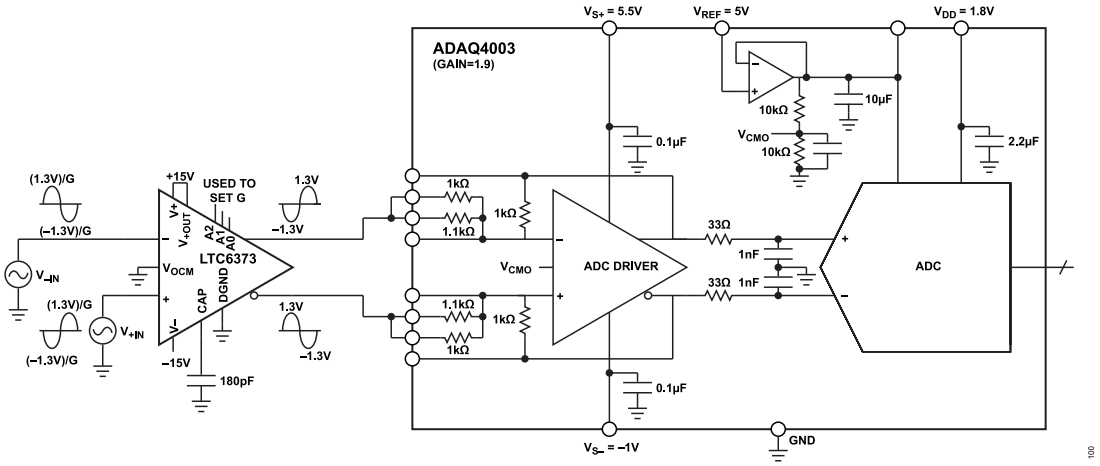

Figure 99. LTC6373 Driving ADAQ4003 (Gain = 1.9)

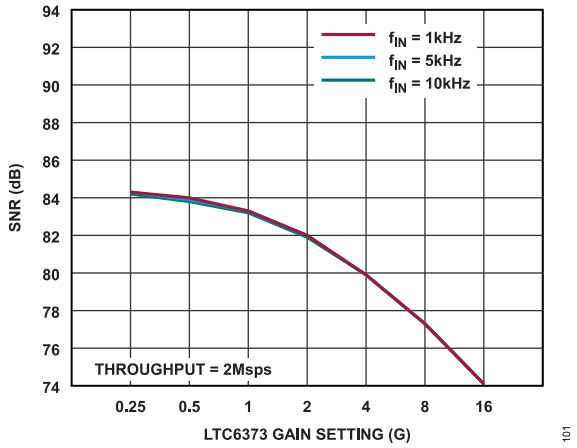

Figure 100. SNR for LTC6373 Driving ADAQ4003 (Gain = 1.9)

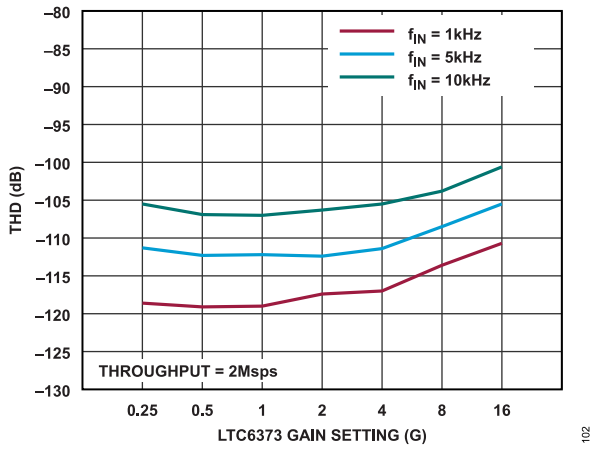

Figure 101. THD for LTC6373 Driving ADAQ4003 (Gain = 1.9)

As another data acquisition system example, the circuit of Figure 102 shows the LTC6373 driving the AD7768-1 (a 24-bit, 256 ksps, ∑-Δ ADC) through the ADA4945-1 (a high speed, fully differential ADC driver). The ADC driver in this circuit has been configured with a closed-loop gain of 1.3 V/V (by using matched discrete resistors) and once again the LTC6373 in conjunction with the ADA4945-1 provide the maximum 2 × V_{REF} peak-to-peak differential signal range needed at the AD7768-1 inputs. More details about this circuit can be found in Table 11 and the typical SNR and THD achieved by this signal chain are illustrated in Figure 103 and Figure 104.

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Table 11. Details for LTC6373 Driving AD7768-1 Through ADA4945-1

ADC	V_{REF} (V)	Signal Level at LTC6373 Outputs = ADC Driver Inputs (V_{P-P})	Signal Level at ADC Driver Outputs = ADC Inputs (V_{P-P})	Typical SNR (dB)	Typical THD (dB)
AD7768-1	4.096	6.3	8.192	See Figure 103	See Figure 104

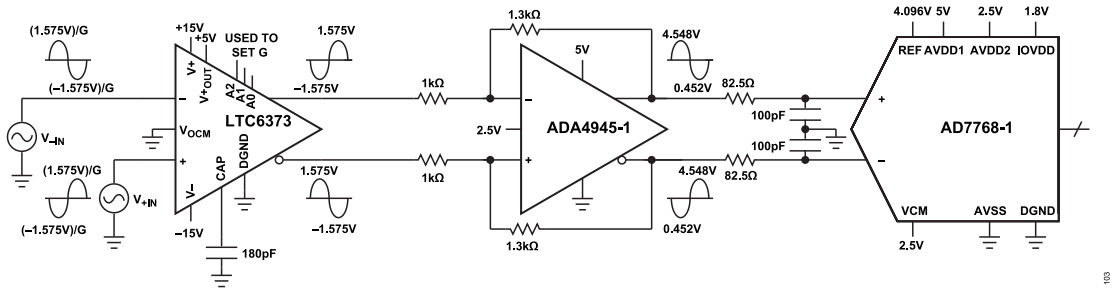

Figure 102. LTC6373 (PGIA) + ADA4945-1 (ADC Driver) + AD7768-1 (ADC) Signal Chain

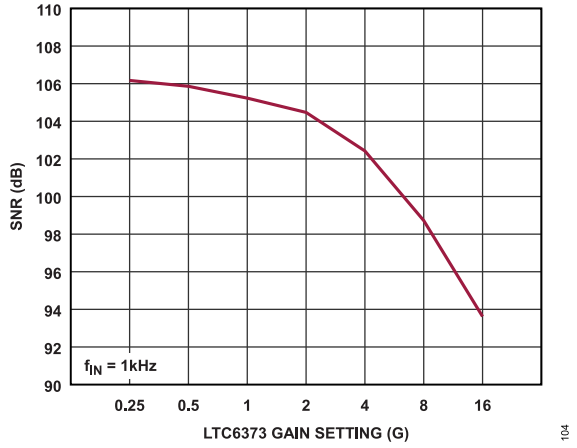

Figure 103. SNR for LTC6373 + ADA4945-1 + AD7768-1 Signal Chain

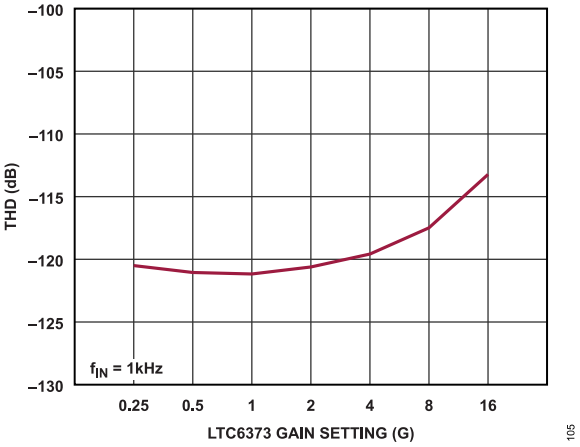

Figure 104. THD for LTC6373 + ADA4945-1 + AD7768-1 Signal Chain

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TYPICAL APPLICATION

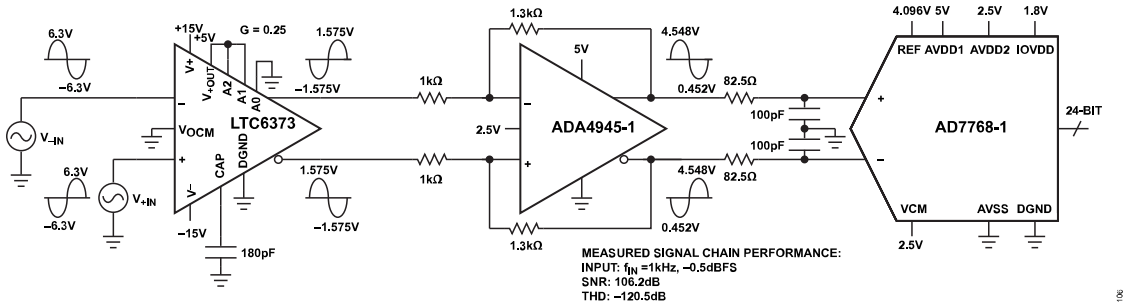


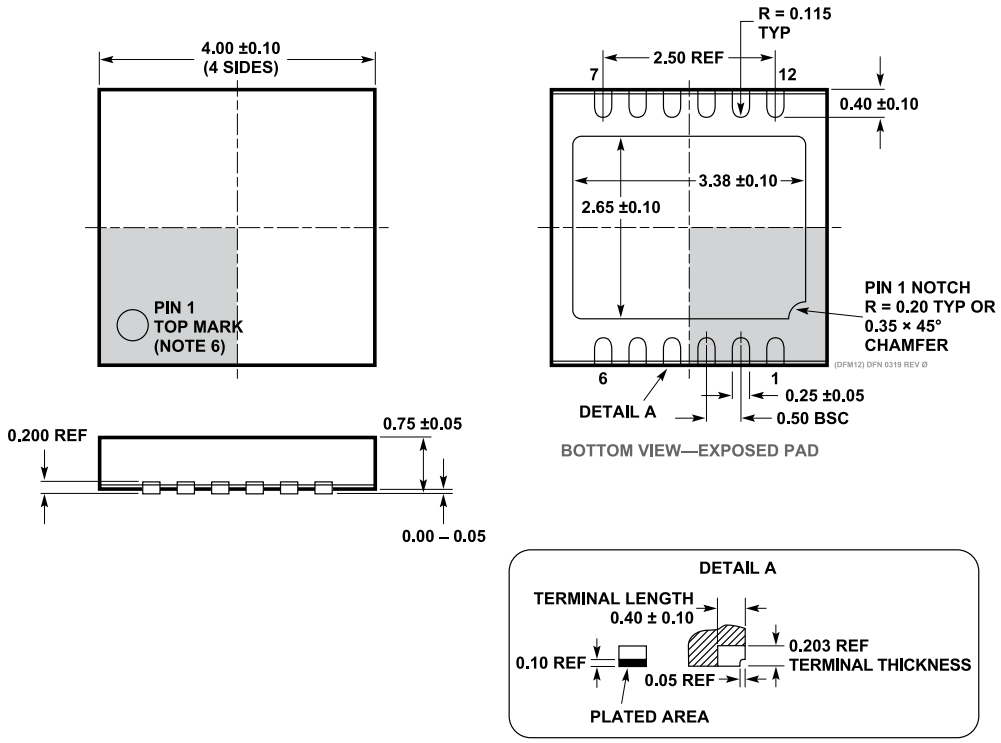
Figure 105. LTC6373 Driving the AD7768-1 Σ-Δ ADC Through a Fully Differential ADC Driver (ADA4945-1)

Related Parts

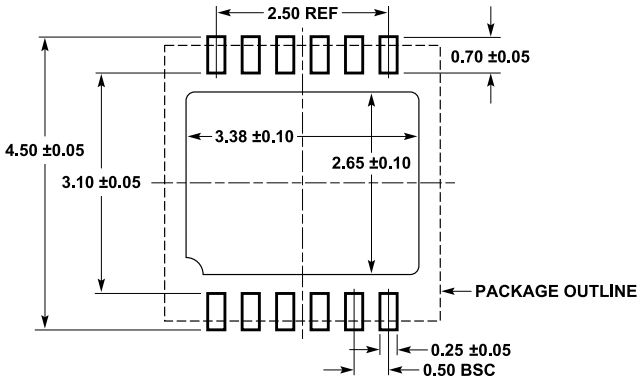
Table 12.

Part Number	Description	Comments
Programmable-Gain Instrumentation Amplifiers (PGIAs)		
AD8250	G = 1, 2, 5, 10	V_S = 30 V, I_S = 4.1 mA, V_{OS} = 200 µV, BW = 10 MHz
AD8251	G = 1, 2, 4, 8	V_S = 30 V, I_S = 4.1 mA, V_{OS} = 200 µV, BW = 10 MHz
AD8253	G = 1, 10, 100, 1000	V_S = 30 V, I_S = 4.6 mA, V_{OS} = 150 µV, BW = 10 MHz
AD8231	Zero-Drift, G = 1, 2, 4, 8, 16, 32, 64, 128 + Shutdown	V_S = 5 V, I_S = 4 mA, V_{OS} = 15 µV, BW = 2.7 MHz
Instrumentation Amplifiers (Resistor-Programmable)		
AD8421	3 nV/√Hz Instrumentation Amplifier	V_S = 36 V, I_S = 2 mA, V_{OS} = 25 µV, BW = 10 MHz
AD8422	Low Power Instrumentation Amplifier	V_S = 36 V, I_S = 300 µA, V_{OS} = 25 µV, BW = 2.2 MHz
LT1167	Precision Instrumentation Amplifier	V_S = 36 V, I_S = 900 µA, V_{OS} = 40 µV, BW = 1 MHz
AD8221	Precision Instrumentation Amplifier	V_S = 36 V, I_S = 900 µA, V_{OS} = 25 µV, BW = 825 kHz
Fully Differential Amplifiers		
ADA4945-1	High Speed, Fully Differential ADC Driver	3 V-10 V Supply Range, 4 mA/1.4 mA Supply Current in Full and Low Power Modes, −133 dBc Distortion at 1 kHz
Analog to Digital Converters (ADCs)		
AD4020	20-Bit, 1.8 Msps, High Precision SAR ADC	1.8 V Supply, Differential Input, 100.5 dB SNR, ±5 V Input Range
LTC2378-20	20-Bit, 1 Msps, High Precision SAR ADC	2.5 V Supply, Differential Input, 104 dB SNR, ±5 V Input Range
AD4003	18-Bit, 2 Msps, High Precision SAR ADC	1.8 V Supply, Differential Input, 100.5 dB SNR, ±5 V Input Range
LTC2379-18	18-Bit, 1.6 Msps, High Precision SAR ADC	2.5 V Supply, Differential Input, 101.2 dB SNR, ±5 V Input Range
AD7768/ AD7768-4/ AD7768-1	8-/4-/1-Channel, 24-Bit, Simultaneous-Sampling, 256 ksps ∑-Δ ADC	5 V Supply, Differential or Unipolar/Bipolar Input, 108 dB DR, 110.8 kHz BW
AD7134	4-Channel, 24-Bit, Continuous Time, 1.5 Msps ∑-Δ ADC	Easy to Drive Resistive ADC input, 108 dB DR, 392 kHz BW
ADAQ4003	18-Bit, 2 Msps, Data Acquisition µModule	Integrates ADC Driver, Reference Buffer, and SAR ADC in a 7 × 7 mm BGA Package

OUTLINE DIMENSIONS



NOTE:
1. PACKAGE OUTLINE DOES NOT CONFORM TO JEDEC MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

Figure 106. 12-Lead 4 mm × 4 mm DFN
(05-08-1791)
Dimensions shown in millimeters

OUTLINE DIMENSIONS

Updated: February 27, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
LTC6373SDFM#PBF	-40°C to +105°C	12-Lead Plastic Side Solderable DFN (4mm × 4mm)		05-08-1791
LTC6373SDFM#TRPBF	-40°C to +105°C	12-Lead Plastic Side Solderable DFN (4mm × 4mm)	Reel, 2500	05-08-1791
LTC6373IDFM#PBF	-40°C to +85°C	12-Lead Plastic Side Solderable DFN (4mm × 4mm)		05-08-1791
LTC6373IDFM#TRPBF	-40°C to +85°C	12-Lead Plastic Side Solderable DFN (4mm × 4mm)	Reel, 2500	05-08-1791

[1] All models are RoHS compliant.

EVALUATION BOARDS

Model[1]	Description
DC2398A	Evaluation Board

[1] DC2398A is RoHS compliant.

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- Alternative Solution
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