



**THE DATASHEET OF
PI6CG188Q2ZLQEX**



8-Output PCIe Gen 4 Clock Generator for Automotive Applications

Features

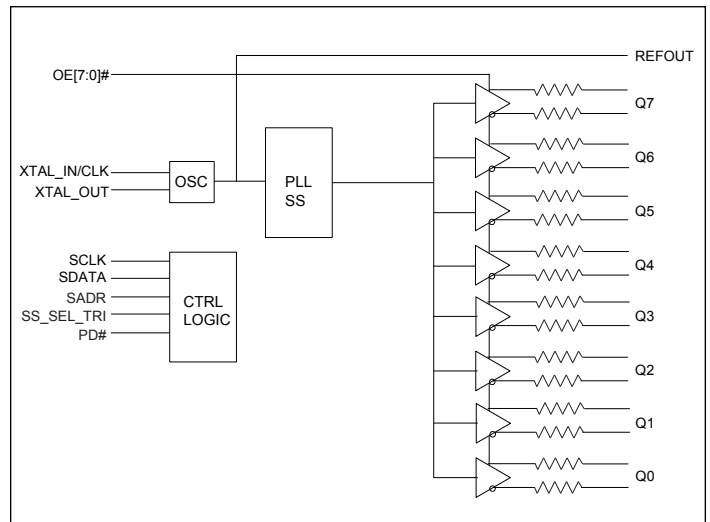
- 1.8V Supply Voltage
- Crystal/CMOS Input: 25MHz
- 8 Differential Low-Power HCSL Outputs with On-Chip Termination
- Individual Output Enable
- Reference CMOS Output
- Programmable Slew Rate and Output Amplitude for Each Output
- Differential Outputs Blocked until PLL is Locked
- Selectable 0%, -0.25%, or -0.5% Spread on Differential Outputs
- Strapping pins or SMBus for Configuration
- 3.3V Tolerant SMBus Interface Support
- Very-Low-Jitter Outputs
 - Differential Cycle-to-Cycle Jitter <50ps
 - Differential Output-to-Output Skew <60ps
 - PCIe Gen1/Gen2/Gen3/ Gen4 Compliant
 - CMOS REFOUT Phase Jitter is < 1.5ps RMS
- AEC-Q 100 Qualified, Automotive Grade 2 Support
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green): 48-lead 6mm × 6mm TQFN

Description

The PI6CG188Q is an 8-output very-low-power PCIe Gen1/Gen2/Gen3/Gen4 clock generator. It uses 25MHz crystal or CMOS reference as an input to generate the 100MHz low-power differential HCSL outputs with on-chip terminations. The on-chip termination can save 32 external resistors and make layout easier. An additional buffered reference output is provided to serve as a low-noise reference for other circuitry.

The device uses Diodes' proprietary PLL design to achieve very-low jitter that meets PCIe Gen1/Gen2/Gen3/Gen4 requirements. It also provides various options, such as different slew rate and amplitude, through strapping pins or SMBUS, so users can configure the device easily for optimized performance for their individual boards. The device also supports selectable spread-spectrum options to reduce EMI for Automotive applications.

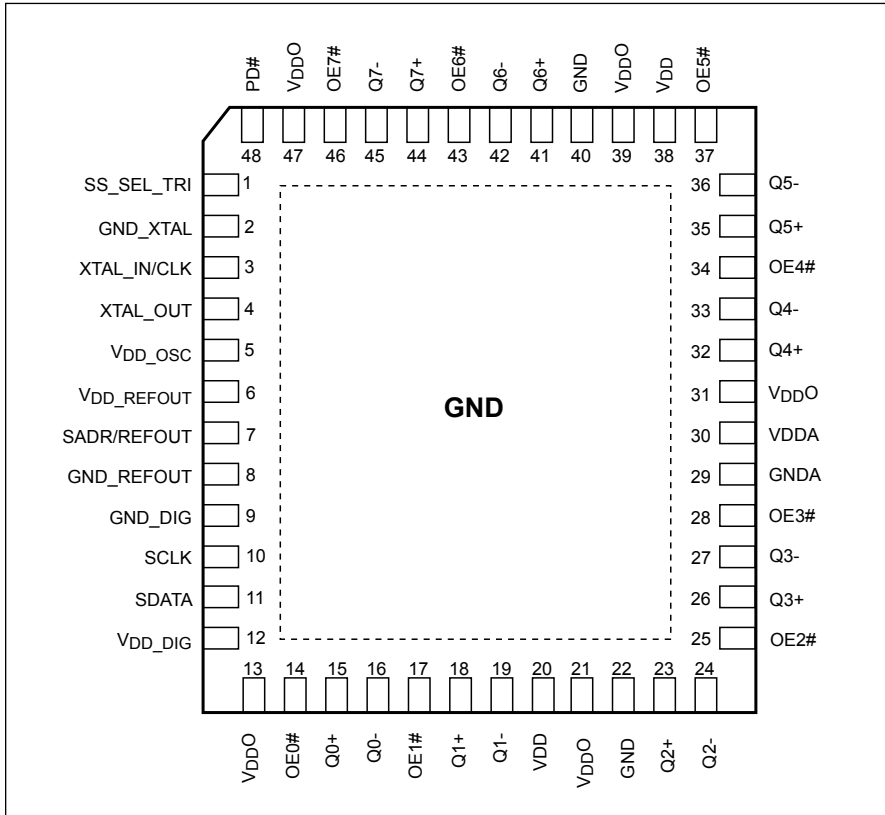
Block Diagram



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin #	Pin Name	Type		Description
1	SS_SEL_TRI	Input	Tri-level	Latched select input to select spread spectrum amount at initial power up 1 = -0.5% spread M = -0.25% 0 = Spread Off
2	GND_XTAL	Power	—	Ground for Oscillator Circuit
3	XTAL_IN/CLK	Input	—	Crystal Input or CMOS Reference Input
4	XTAL_OUT	Output	—	Crystal Output
5	V _{DD} _OSC	Power	—	Power Supply for Oscillator Circuitry, Nominal 1.8V
6	V _{DD} _REFOUT	Power	—	Power Supply for Buffered CMOS Output
7	SADR/REFOUT	Input/ Output	CMOS	Latch to select SMBus Address or 1.8V LVCMOS REFOUT. This pin has an internal pulldown.
8	GND_REFOUT	Power	—	Ground for REFOUT
9	GND_DIG	Power	—	Ground for Digital Circuitry
10	SCLK	Input	CMOS	SMBUS Clock Input, 3.3V Tolerant
11	SDATA	Input/ Output	CMOS	SMBUS Data Line, 3.3V Tolerant
12	V _{DD} _DIG	Power	—	Power Supply for Digital Circuitry, Nominal 1.8V

Pin Description Cont.

Pin #	Pin Name	Type		Description
13, 21, 31, 39, 47	V _{DDO}	Power	—	Power Supply for Differential Outputs
14	OE0#	Input	CMOS	Active-low input for enabling Q0 pair. This pin has an internal pulldown. 1 =disable outputs 0 = enable outputs
15	Q0+	Output	HCSL	Differential True Clock Output
16	Q0-	Output	HCSL	Differential Complementary Clock Output
17	OE1#	Input	CMOS	Active-low input for enabling Q1 pair. This pin has an internal pulldown. 1 =disable outputs 0 = enable outputs
18	Q1+	Output	HCSL	Differential True Clock Output
19	Q1-	Output	HCSL	Differential Complementary Clock Output
20, 38	V _{DD}	Power	—	Power Supply, Nominal 1.8V
22, 40	GND	Power	—	Ground
23	Q2+	Output	HCSL	Differential True Clock Output
24	Q2-	Output	HCSL	Differential Complementary Clock Output
25	OE2#	Input	CMOS	Active-low input for enabling Q2 pair. This pin has an internal pulldown. 1 =disable outputs 0 = enable outputs
26	Q3+	Output	HCSL	Differential True Clock Output
27	Q3-	Output	HCSL	Differential Complementary Clock Output
28	OE3#	Input	CMOS	Active-low input for enabling Q3 pair. This pin has an internal pulldown. 1 =disable outputs 0 = enable outputs
29	GNDA	Power	—	Ground for Analog Circuitry
30	V _{DDA}	Power	—	Power Supply for Analog Circuitry
32	Q4+	Output	HCSL	Differential True Clock Output
33	Q4-	Output	HCSL	Differential Complementary Clock Output
34	OE4#	Input	CMOS	Active-low input for enabling Q4 pair. This pin has an internal pulldown. 1 =disable outputs 0 = enable outputs
35	Q5+	Output	HCSL	Differential True Clock Output
36	Q5-	Output	HCSL	Differential Complementary Clock Output
37	OE5#	Input	CMOS	Active-low input for enabling Q5 pair. This pin has an internal pulldown. 1 =disable outputs 0 = enable outputs
41	Q6+	Output	HCSL	Differential True Clock Output
42	Q6-	Output	HCSL	Differential Complementary Clock Output

Pin Description Cont.

Pin #	Pin Name	Type		Description
43	OE6#	Input	CMOS	Active-low input for enabling Q6 pair. This pin has an internal pulldown. 1 =disable outputs 0 = enable outputs
44	Q7+	Output	HCSL	Differential True Clock Output
45	Q7-	Output	HCSL	Differential Complementary Clock Output
46	OE7#	Input	CMOS	Active-low input for enabling Q7 pair. This pin has an internal pulldown. 1 =disable outputs 0 = enable outputs
48	PD#	Input	CMOS	Input notifies device to sample latched inputs and startup on first high assertion. Low enters Power Down Mode; subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.

SMBus Address Selection Table

	SADR	Address	+Read/Write Bit
State of SADR on First Application of PD#	0	1101000	X
	1	1101010	X

Power Management Table

PD#	SMBus OE bit	OEn#	Qn+	Qn-	REFOUT
0	X	X	Low	Low	HiZ
1	1	0	Running	Running	Running
1	1	1	Low	Low	Low
1	0	X	Low	Low	Low

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-65°C to +150°C
Supply Voltage to Ground Potential, V _{DDXX}	-0.5V to +2.5V
Input Voltage	-0.5V to V _{DD} +0.5V, not exceed 2.5V
SMBus, Input High Voltage	3.6V
ESD Protection (HBM)	2000 V
ESD Protection (CDM) PD# pin #48 only	250 V
ESD Protection (CDM) all other pins.....	500 V
Max Junction Temperature	+125°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V _{DD} , V _{D_{DDA}} , V _{DD_} OSC, V _{DD_} REFOUT, V _{DD_} DIG	Power Supply Voltage	—	1.7	1.8	1.9	V
V _{DDO}	Output Power Supply Voltage	—	0.9975	1.05-1.8	1.9	V
I _{DDA}	Analog Power Supply Current	All Outputs Active @ 100MHz	—	6	9	mA
I _{DD}	Power Supply Current	All V _{DD} , Except V _{D_{DDA}} and V _{DDO} , All Outputs Active @ 100MHz	—	5	7.5	mA
I _{DDO}	Power Supply Current for Outputs	All Outputs Active @ 100MHz	—	32	40	mA
I _{DDA_WL}	Analog Power Supply Wake-on-LAN ⁽¹⁾ Current	Q Outputs Off, REF Output Running	—	0.4	1	mA
I _{DD_WL}	Power Supply Wake-on-LAN ⁽¹⁾ Current	All V _{DD} , except V _{D_{DDA}} and V _{DDO} , Q Outputs Off, REF Output Running	—	0.5	1.2	mA
I _{DDO_WL}	Power Supply Wake-on-LAN ⁽¹⁾ Current for Outputs	Q Outputs Off, REF Output Running	—	0.04	0.1	mA
I _{DDA_PD}	Analog Power Supply Power Down ⁽²⁾ Current	All Outputs Off	—	0.4	1	mA
I _{DD_PD}	Power Supply Power Down ⁽²⁾ Current	All Outputs Off	—	0.6	1	mA
I _{DDO_PD}	Power Supply Current Power Down ⁽²⁾ for Outputs	All Outputs Off	—	0.0005	0.1	mA
T _A	Ambient Temperature	Industrial Grade	-40	—	105	°C

Note: 1. Wake-on-LAN mode: PD# = '0' Byte 3, bit 5 = '1'
2. Power down mode: PD# = '0' Byte 3, bit 5 = '0'

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R _{pu}	Internal Pullup Resistance	—	—	120	—	KΩ
R _{dn}	Internal Pulldown Resistance	—	—	120	—	KΩ
C _{XTAL}	Internal Capacitance on X_IN and X_OUT pins	—	—	5	—	pF
L _{PIN}	Pin Inductance	—	—	—	7	nH

Crystal Characteristic

Parameters	Description	Min.	Typ	Max.	Units
OSCmode	Mode of Oscillation	Fundamental			
FREQ	Frequency	—	25	—	MHz
ESR ⁽¹⁾	Equivalent Series Resistance	—	—	50	Ω
Cload	Load Capacitance	—	8	—	pF
Cshunt	Shunt Capacitance	—	—	7	pF
—	Drive Level	—	—	300	uW

Note: 1. ESR value is dependent upon frequency of oscillation

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V _{DDSMB}	Nominal Bus Voltage	—	1.7	—	3.6	V
V _{IHSMB}	SMBus Input High Voltage	SMBus, V _{DDSMB} = 3.3V	2.1	—	3.6	V
		SMBus, V _{DDSMB} < 3.3V	0.65 V _{DDSMB}	—	—	
V _{ILSMB}	SMBus Input Low Voltage	SMBus, V _{DDSMB} = 3.3V	—	—	0.6	V
		SMBus, V _{DDSMB} < 3.3V	—	—	0.6	
I _{SMBSINK}	SMBus Sink Current	SMBus, at V _{OLSMB}	4	—	—	mA
V _{OLSMB}	SMBus Output Low Voltage	SMBus, at I _{SMBSINK}	—	—	0.4	V
f _{MAXSMB}	SMBus Operating Frequency	Maximum Frequency	—	—	400	kHz
t _{RMSB}	SMBus Rise Time	(Max V _{IL} - 0.15) to (Min V _{IH} + 0.15)	—	—	1000	ns
t _{FMSB}	SMBus Fall Time	(Min V _{IH} + 0.15) to (Max V _{IL} - 0.15)	—	—	300	ns

Spread Spectrum Characteristic

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f _{MOD}	SS Modulation Frequency	Triangular Modulation	30	31.6	33	kHz

LVCMOS DC Electrical Characteristics

 Temperature = T_A ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-Ended Inputs, Except SMBus	0.75 V_{DD}	—	V_{DD} +0.3	V
V_{IM}	Input Mid Voltage	SS_SEL_TRI	0.4 V_{DD}	0.5 V_{DD}	0.6 V_{DD}	V
V_{IL}	Input Low Voltage	Single-Ended Inputs, Except SMBus	-0.3	—	0.25 V_{DD}	V
I_{IH}	Input High Current	Single-Ended Inputs, $V_{IN} = V_{DD}$	—	—	20	mA
I_{IL}	Input Low Current	Single-Ended Inputs, $V_{IN} = 0V$	-20	—	—	μA
I_{IH}	Input High Current	Single-Ended Inputs with Pullup/Pulldown Resistor, $V_{IN} = V_{DD}$	—	—	220	mA
I_{IL}	Input Low Current	Single-Ended Inputs with Pullup/Pulldown Resistor, $V_{IN} = 0V$	-220	—	—	μA
V_{OH}	Output High Voltage	REFOUT, except SMBus; $I_{OH} = -2mA$	V_{DD} -0.45	—	—	V
V_{OL}	Output Low Voltage	REFOUT, except SMBus; $I_{OH} = 2mA$	—	—	0.45	V
R_{OUT}	CMOS Output impedance	—	—	20	—	Ω
C_{IN}	Input Capacitance	—	1.5	—	5	pF

LVCMOS AC Characteristics

 Temperature = T_A ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{INPUT}	Input Frequency	XTAL_IN/CLK	23	25	27	MHz
t_{RIN}	Input Rise Time	Single-Ended Inputs	—	—	5	ns
t_{FIN}	Input Fall Time	Single-Ended Inputs	—	—	5	ns
t_{STAB}	Clock Stabilization	From Powerup and After Input Clock Stabilization or Deassertion of PD# to 1st Clock	—	0.6	1.8	ms
t_{OELAT}	Output Enable Latency	Q Start After OE# Assertion Q Stop After OE# Deassertion	1	—	3	clocks
t_{PDLAT}	PD# Deassertion	Differential Outputs Enable after PD# Deassertion	—	20	300	μs
t_{PERIOD}	REFOUT Clock Period	REFOUT, Assume Input is at 25MHz	—	40	—	ns
f_{ACC}	REFOUT Frequency Accuracy ⁽¹⁾	REFOUT, Long Term Accuracy to Input	—	0	—	ppm
t_{SLEW}	REFOUT Slew Rate ⁽¹⁾	Byte 3 = 1F, 20% to 80% of V_{DDREF}	0.6	1	1.6	V/ns
		Byte 3 = 5F, 20% to 80% of V_{DDREF}	0.75	1.4	2.2	V/ns
		Byte 3 = 9F, 20% to 80% of V_{DDREF}	0.85	1.7	2.7	V/ns
		Byte 3 = DF, 20% to 80% of V_{DDREF}	1.0	1.8	2.9	V/ns

LVC MOS AC Characteristics Cont.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
t _{DC}	REFOUT Duty Cycle ⁽¹⁾	V _T = V _{DD} / 2 V, driven by a Xtal	45	50	55	%
t _{DCDIS}	REFOUT Duty Cycle Distortion	V _T = V _{DD} / 2 V, Driven by an External Source	0	2	4	%
t _{JITCC}	REFOUT Cycle-Cycle Jitter	V _T = V _{DD} / 2 V, Driven by a Xtal	—	19.1	250	ps
t _{JITPH}	REFOUT Phase Jitter	12kHz to 5MHz, RMS, Driven by a Xtal	—	0.63	1.5	ps
t _{JITN}	Noise Floor	1kHz Offset, Driven by a Xtal	—	-129.8	-105	dBc
		10kHz Offset to Nyquist, Driven by a Xtal	—	-143.6	-115	dBc

Note: 1. Guaranteed by design and characterization—not 100% tested in production.

HCSL Output Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V _{OH}	Output Voltage High ⁽¹⁾	Statistical Measurement on Single-Ended Signal Using Oscilloscope Math Function	660	784	900	mV
V _{OL}	Output Voltage Low ⁽¹⁾		-150	—	150	mV
V _{OMAX}	Output Voltage Maximum ⁽¹⁾	Measurement on Single-Ended Signal Using Absolute Value	—	816	1150	mV
V _{OMIN}	Output Voltage Minimum ⁽¹⁾		-300	-42	—	mV
V _{OSWING}	Output Swing Voltage ^(1,2,3)	Scope Averaging Off	300	1634	—	mV
V _{OC}	Output Cross Voltage ^(1,2,4)	—	250	430	550	mV
DV _{OC}	V _{OC} Magnitude Change ^(1,2,5)	—	—	12	140	mV

- Note:
- At default SMBUS amplitude settings.
 - Guaranteed by design and characterization—not 100% tested in production.
 - Measured from differential waveform.
 - This one is defined as voltage where Q+ = Q- measured on a component test board and only applied to the differential rising edge.
 - The total variation of all V_{cross} measurements in any particular system. This is a subset of V_{cross_min/max} allowed.

HCSL Output AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
f _{OUT}	Output Frequency	—	—	100	—	MHz
t _{RF}	Slew Rate ^(1,2,3)	Scope Averaging on Fast Setting	1.9	2.3	4	V/ns
		Scope Averaging on Slow Setting	1.1	1.9	2.9	V/ns
Dt _{RF}	Slew Rate Matching ^(1,2,4)	Scope Averaging on	—	3	—	%
t _{DC}	Duty Cycle ^(1,2)	Measured Differentially, PLL Mode	45	50	55	%
t _{SKEW}	Output Skew ^(1,2)	Averaging on, V _T = 50%	—	43	60	ps
t _{Jc-c}	Cycle-to-Cycle Jitter ^(1,2)	—	—	42	50	ps
t _{STARTUP}	Startup Time	—	—	—	10	ms
t _{LOCK}	PLL Lock Time	—	—	—	20	ms

PI6CG188Q

HC SL Output AC Characteristics Cont.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
t _{JPHASE}	Integrated Phase Jitter (RMS) (1,5,6)	PCIe Gen 1	25	35	86	ps
		PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz	0.9	1.2	3.0	ps
		PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz)	1.6	2.1	3.1	ps
		PCIe Gen 3 Common Clock Architecture (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	0.4	0.5	1.0	ps
		PCIe Gen 3 Separate Reference No Spread (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	0.4	0.5	0.7	ps
		PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	0.3	0.37	0.5	ps

- Note:
1. Guaranteed by design and characterization—not 100% tested in production.
 2. Measured from differential waveform.
 3. Slew rate is measured through the V_{swing} voltage range centered around differential 0V, within ±150mV window.
 4. It is measured using a ±75mV window centered on the average cross point.
 5. See <http://www.pcisig.com> for complete specifications.
 6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10⁻¹².

Differential Output Clock Periods - Spread Spectrum Disabled ^{1, 2}

Center Freq. MHz	Measurement Window							Units
	1 clock	1 μs	0.1 s	0.1 s	0.1 s	1 μs	1 clock	
	-c2c jitter AbsPer Min	- SSC Short-Term Avg. Min	-ppm Long-Term Avg. Min	0 ppm Period Nominal	+ppm Long-Term Avg. Max	+ SSC Short-Term Avg. Max	-c2c jitter AbsPer Max	
100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns

Differential Output Clock Periods - Spread Spectrum Enabled ^{1, 2}

Center Freq. MHz	Measurement Window							Units
	1 clock	1 us	0.1 s	0.1 s	0.1 s	1 us	1 clock	
	-c2c jitter AbsPer Min	- SSC Short-Term Avg. Min	-ppm Long-Term Avg. Min	0 ppm Period Nominal	+ppm Long-Term Avg. Max	+ SSC Short-Term Avg. Max	-c2c jitter AbsPer Max	
99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns

- Note:
1. Guaranteed by design and characterization—not 100% tested in production.
 2. All long term accuracy and clock period specifications are guaranteed assuming REF is trimmed to 25.00MHz.

SMBus Serial Data Interface

PI6CG188Q is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	SADR	0	1/0

Note: 1. SMBus address is latched on SADR pin.

How to Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte Location = N	Ack	Data Byte Count = X	Ack	Beginning Data Byte (N)	Ack	Data Byte (N+X-1)	Ack	Stop bit

How to Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte Location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte Count = X	Ack	Beginning Data Byte (N)	Ack
										8 bits	1 bit	1 bit	
.....										Data Byte (N+X-1)	NAck	Stop bit	

Byte 0: Output Enable Register⁽¹⁾

Bit	Control Function	Description	Type	Powerup Condition	0	1
7	Q7_OE	Q7 Output Enable	RW	1	Low/Low	Enabled
6	Q6_OE	Q6 Output Enable	RW	1	Low/Low	Enabled
5	Q5_OE	Q5 Output Enable	RW	1	Low/Low	Enabled
4	Q4_OE	Q4 Output Enable	RW	1	Low/Low	Enabled
3	Q3_OE	Q3 Output Enable	RW	1	Low/Low	Enabled
2	Q2_OE	Q2 Output Enable	RW	1	Low/Low	Enabled
1	Q1_OE	Q1 Output Enable	RW	1	Low/Low	Enabled
0	Q0_OE	Q0 Output Enable	RW	1	Low/Low	Enabled

Note: 1. A low on these bits will override the OE# pins and force the differential outputs to Low/Low states.

Byte 1: SS Readback and Control Register

Bit	Control Function	Description	Type	Powerup Condition	0	1
7	SSENRB1	SS Enable Readback Bit1	R	Latch	'00' for SS_SEL_TRI = '0', '01' for SS_SEL_TRI = 'M', '11' for SS_SEL_TRI = '1'	
6	SSENRB0	SS Enable Readback Bit0	R	Latch		
5	SSEN_SWCTR	Enable SW Control of SS	RW	0	Values in B1[7:6] Control SS Amount	Values in B1[4:3] Control SS Amount
4	SSENSW1	SS Enable SW Control Bit1	RW ⁽¹⁾	0	'00' = SS off, '01' = -0.25% SS, '10' = Reserved, '11' = -0.5% SS	
3	SSENSW0	SS Enable SW Control Bit0	RW ⁽¹⁾	0		
2	Reserved	—	—	1	—	—
1	Amplitude1	Control Output Amplitude	RW	1	'00' = 0.6V, '01' = 0.7V, '10' = 0.8V, '11' = 0.9V	
0	Amplitude0		RW	0		

Note: 1. B1[5] must be set to a 1 for these bits to have any effect on the part.

Byte 2: Differential Output Slew Rate Control Register

Bit	Control Function	Description	Type	Powerup Condition	0	1
7	SLEWRATECTR_Q7	Control Slew Rate of Q7	RW	1	Slow Setting	Fast Setting
6	SLEWRATECTR_Q6	Control Slew Rate of Q6	RW	1	Slow Setting	Fast Setting
5	SLEWRATECTR_Q5	Control Slew Rate of Q5	RW	1	Slow Setting	Fast Setting
4	SLEWRATECTR_Q4	Control Slew Rate of Q4	RW	1	Slow Setting	Fast Setting
3	SLEWRATECTR_Q3	Control Slew Rate of Q3	RW	1	Slow Setting	Fast Setting
2	SLEWRATECTR_Q2	Control Slew Rate of Q2	RW	1	Slow Setting	Fast Setting
1	SLEWRATECTR_Q1	Control Slew Rate of Q1	RW	1	Slow Setting	Fast Setting
0	SLEWRATECTR_Q0	Control Slew Rate of Q0	RW	1	Slow Setting	Fast Setting

Byte 3: REF Control Register

Bit	Control Function	Description	Type	Powerup Condition	0	1
7	REFSLEWRATE	Slew Rate Control for REF	RW	0	'00' = 0.9V/ns '01' = 1.3V/ns, '10' = 1.6V/ns, '11' = 1.8V/ns	
6			RW	1		
5	REF_PDSTATE	Wake-on-Lan Enable for REF	RW	0	REF = 'Low'	REF = running
4	REF_OE	Output Enable for REF	RW	1	REF = "Low"	REF = running
3	Reserved	—	—	1	—	—
2	Reserved	—	—	1	—	—
1	Reserved	—	—	1	—	—
0	Reserved	—	—	1	—	—

Byte 4: Reserved

Bit	Control Function	Description	Type	Powerup Condition	0	1
7:0	Reserved	—	—	—	—	—

Byte 5: Revision and Vendor ID Register

Bit	Control Function	Description	Type	Powerup Condition	0	1
7	RID3	Revision ID	R	0	rev = 0000	
6	RID2		R	0		
5	RID1		R	0		
4	RID0		R	0		
3	PVID3	Vendor ID	R	0	Diodes = 0011	
2	PVID3		R	0		
1	PVID3		R	1		
0	PVID3		R	1		

Byte 6: Device Type/Device ID Register

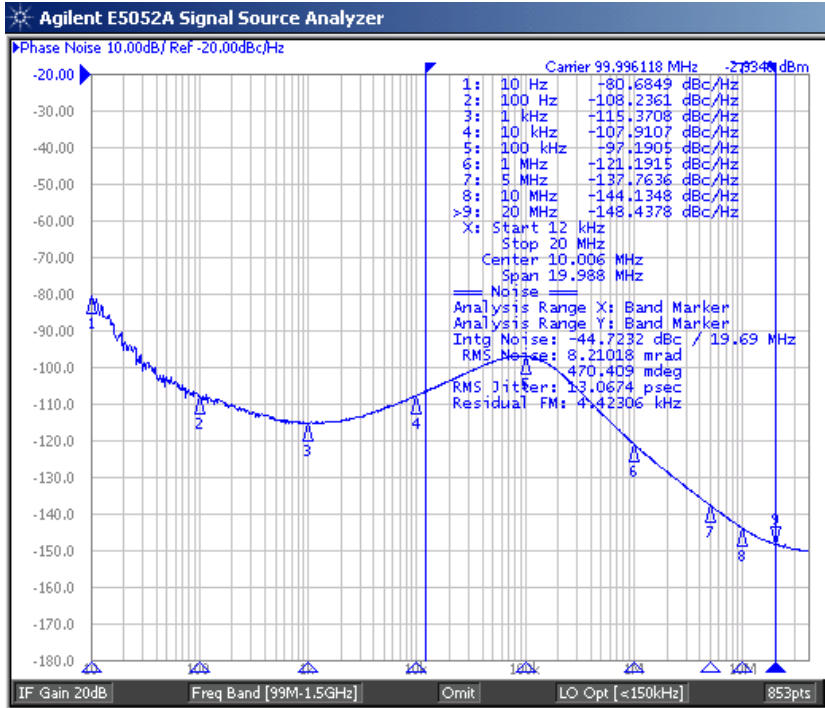
Bit	Control Function	Description	Type	Powerup Condition	0	1
7	DTYPE1	Device Type	R	0	'00' = CG, '01' = ZDB, '10' = Reserve, '11' = ZDB	
6	DTYPE0		R	0		
5	DID5	Device ID	R	0	001000 binary, 08Hex	
4	DID4		R	0		
3	DID3		R	1		
2	DID2		R	0		
1	DID1		R	0		
0	DID0		R	0		

Byte 7: Byte Count Register

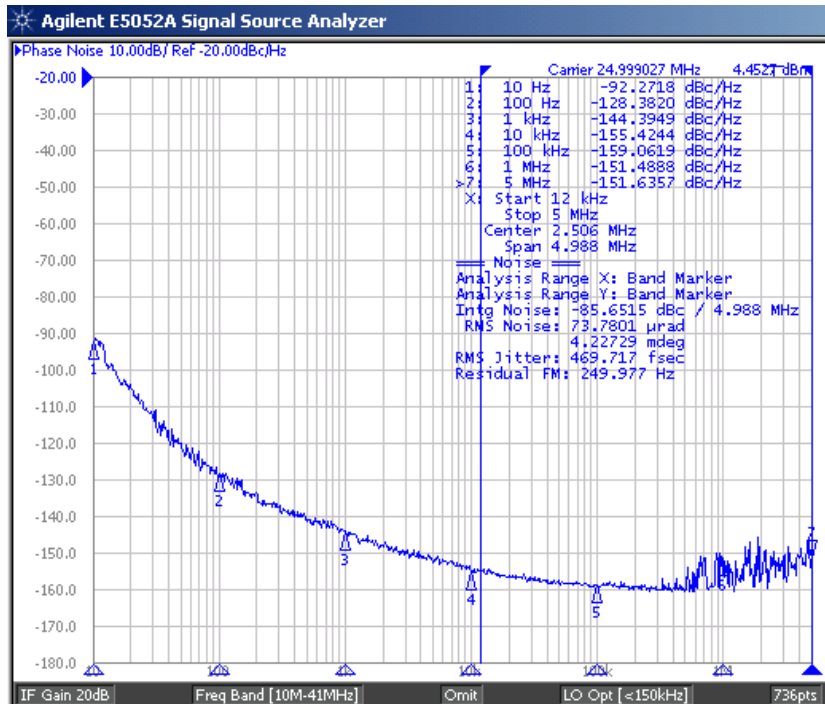
Bit	Control Function	Description	Type	Powerup Condition	0	1
7	Reserved	—	—	0	—	—
6	Reserved	—	—	0	—	—
5	Reserved	—	—	0	—	—
4	BC4	Byte Count Programming	RW	0	Writing to this register will configure how many bytes will be read back, default is 8 bytes	
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		

Plots

100MHz HCSL Clock (12k to 20MHz)



25MHz CMOS Clock



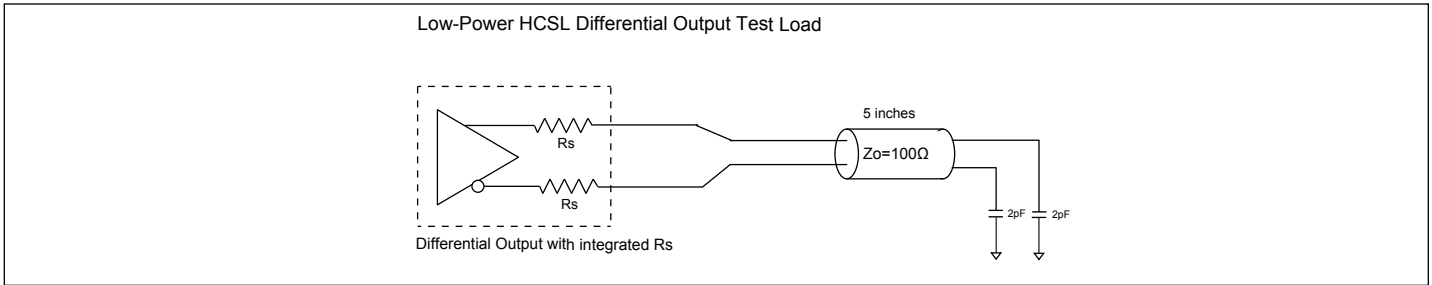


Figure 1. Low-Power HCSL Test Circuit

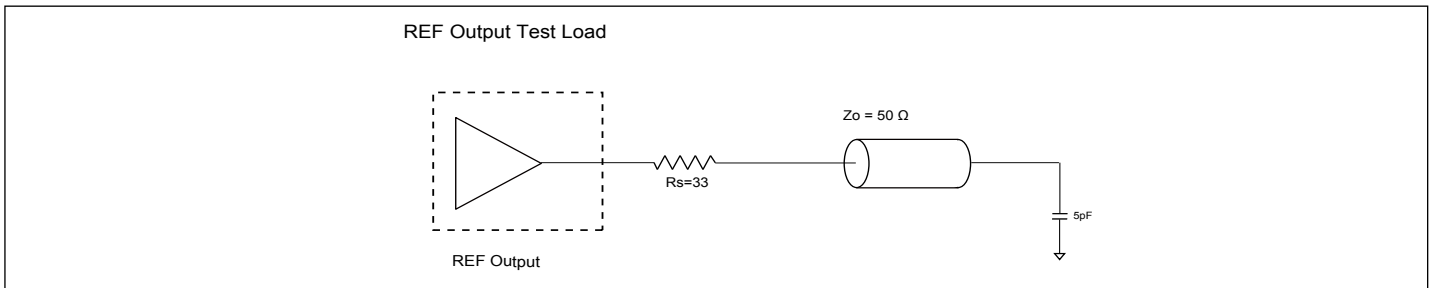


Figure 2. CMOS REF Test Circuit

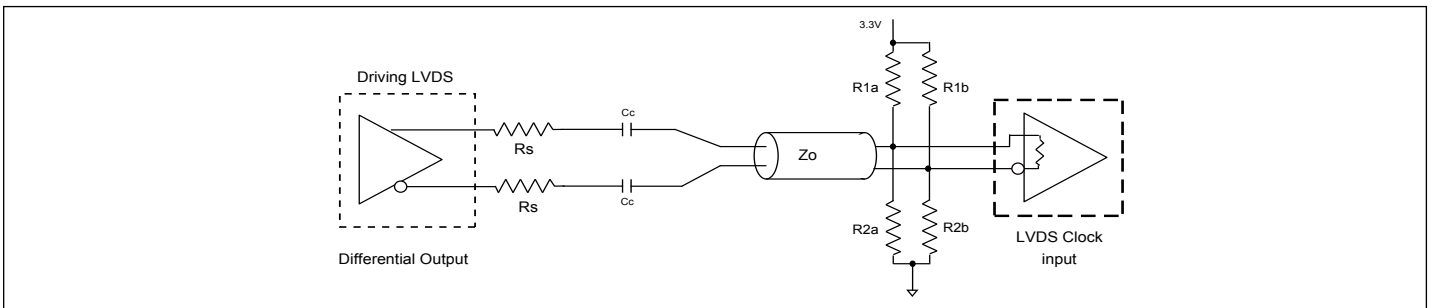


Figure 3. Differential Output Driving LVDS

Alternate Differential Output Terminations

Component	Receiver with Termination	Receiver without Termination	Unit
R_{1a}, R_{1b}	10,000	140	Ω
R_{2a}, R_{2b}	5600	75	Ω
C_c	0.1	0.1	μF
V_{CM}	1.2	1.2	V

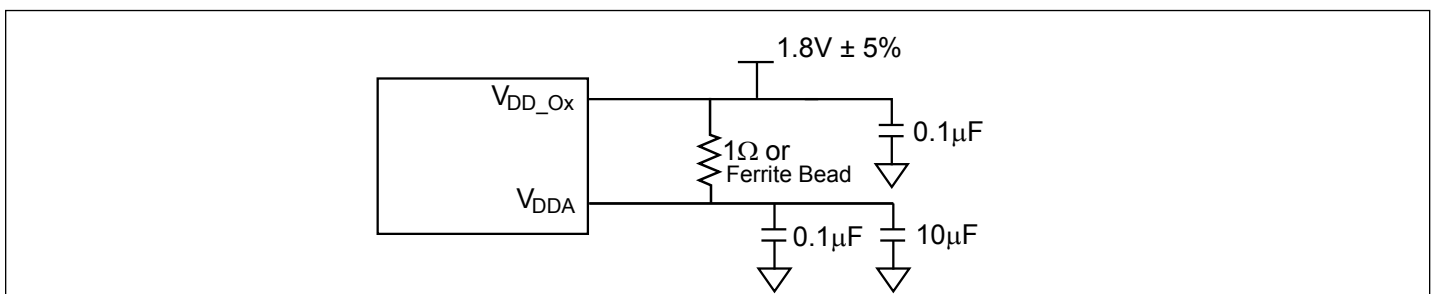
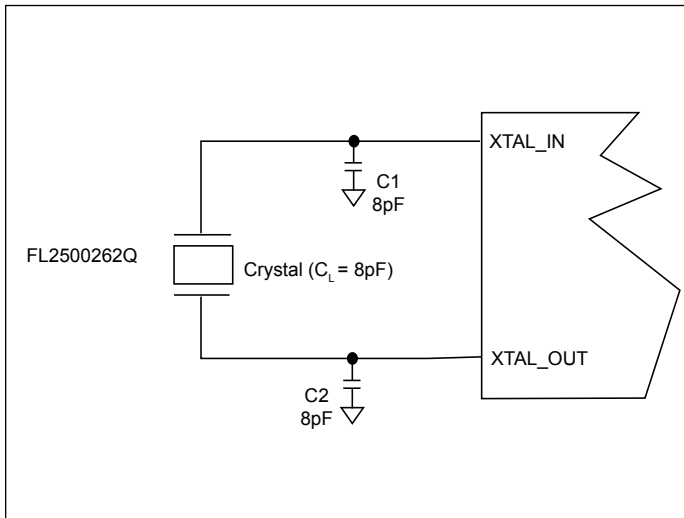


Figure 4. Power Supply Filter

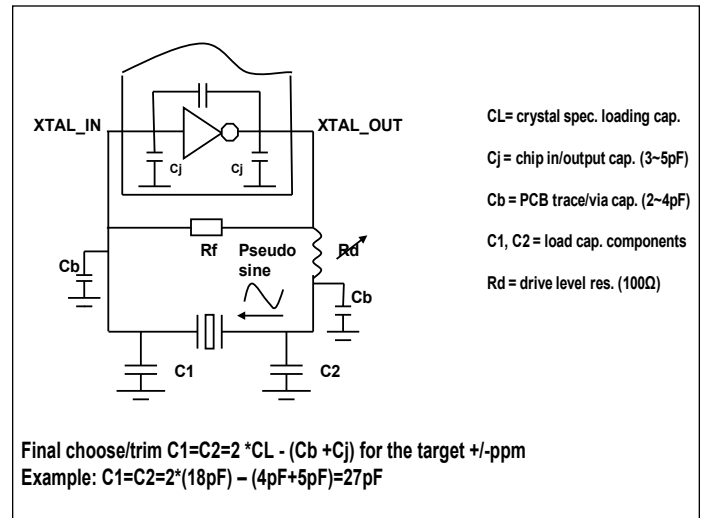
Crystal Circuit Connection

The following diagram shows PI6CG188Q crystal circuit connection with a parallel crystal. For the $CL = 8\text{pF}$ crystal, it is suggested to use $C1 = 8\text{pF}$, $C2 = 8\text{pF}$. $C1$ and $C2$ can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts based on the following formular in the Crystal Capacitor Calculation diagram.

Crystal Oscillator Circuit



Crystal Capacitor Calculation



Recommended Crystal Specification

Diodes Recommends:

- FL2500262Q, SMD 3.2x2.5(4P), 25MHz, $CL=8\text{pF}$, $\pm 50\text{ppm}$, <https://www.diodes.com/assets/Datasheets/FL.pdf>.
- FW2500054Q, SMD 2.0x1.6(4P), 25MHz, $CL=8\text{pF}$, $\pm 50\text{ppm}$, <https://www.diodes.com/assets/Datasheets/FW.pdf>.

Part Marking

ZLQ Package



1st Y: Die Rev
 2nd & 3rd Y: Year
 WW: Workweek
 1st X: Assembly Code
 2nd X: Fab Code

Packaging Mechanical: 48-TQFN (ZLQ)

SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
e	0.40 BSC		
K	0.35 REF.		
D2	4.45	4.50	4.55
E2	4.45	4.50	4.55
L	0.35	0.40	0.45

NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

DATE: 11/23/17

DESCRIPTION: 48-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZLQ (ZLQ48)

DOCUMENT CONTROL #: PD-2235

REVISION: -

17-0143

For latest package information:

See <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>.

Ordering Information

Ordering Code	Package Code	Package Description	Operating Temperature
PI6CG188Q2ZLQEX	ZLQ	48-Contact, Very Thin Quad Flat No-Lead (TQFN)	-40°C to 105°C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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