THE DATASHEET OF

NTTFS012N10MDTAG

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MOSFET – Power, Single N-Channel

100 V, 14.4 mΩ, 45 A

NTTFS012N10MD

Features

- Shielded Gate MOSFET Technology
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Low Q_{RR}, Soft Recovery Body Diode
- Low Q_{OSS} to Improve Light Load Efficiency
- These Devices are Pb−Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

Typical Applications

- Primary Switch in Isolated DC−DC Converter
- Synchronous Rectification (SR) in DC−DC and AC−DC
- AC−DC Adapters (USB PD) SR
- Load Switch, Hotswap, and ORing Switch
- BLDC Motor and Solar Inverter

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Breakdown Voltage			$V_{(BR)DSS}$	100	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	45	A
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	P_D	62	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	9.2	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	P_D	2.7	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	217	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	51.8	A
Single Pulse Drain−to−Source Avalanche Energy (I_{AV} = 9 A, L = 3 mH)			E_{AS}	121	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	2.0	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	46.5	

1. Surface−mounted on FR4 board using a 1 in^2 pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

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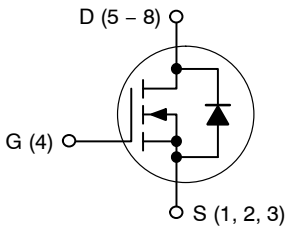
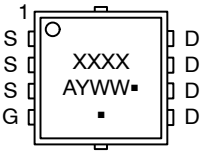
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
100 V	14.4 mΩ @ 10 V	45 A
	21.0 mΩ @ 6 V	

N−Channel



WDFN8
(μ8FL)
CASE 511DY

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS012N10MD	WDFN8 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			60		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25°C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 78 μA		2		4	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 78 μA, ref to 25°C			−8.1		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 15 A		12.2	14.4	mΩ
		V_{GS} = 6 V	I_D = 7.5 A		16.7	21.0	
Forward Transconductance	g_{FS}	V_{DS} = 8 V, I_D = 15 A			36		S
Gate−Resistance	R_G	T_A = 25°C			0.5	1.6	Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 50 V			965		pF
Output Capacitance	C_{OSS}				270		
Reverse Transfer Capacitance	C_{RSS}				8.4		
Output Charge	Q_{OSS}	V_{GS} = 0 V, V_{DS} = 50 V			22		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 6 V, V_{DS} = 50 V, I_D = 15 A			8		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 15 A			13		
Gate−to−Source Charge	Q_{GS}				4.6		
Gate−to−Drain Charge	Q_{GD}				1.8		
Plateau Voltage	V_{GP}				4.5		V
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 15 A, R_G = 6 Ω			12		ns
Rise Time	t_r				2.7		
Turn−Off Delay Time	$t_{d(OFF)}$				17		
Fall Time	t_f				2.6		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 15 A	T_J = 25°C		0.85		V
			T_J = 125°C		0.72		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 1000 A/μs, I_S = 7.5 A			20		ns
Reverse Recovery Charge	Q_{RR}				116		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 15 A			36		ns
Reverse Recovery Charge	Q_{RR}				34		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.
4. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
5. Pulse Test: Pulse Width < 300 μs. Duty cycle < 2%.
6. E_{AS} of 121 mJ is based on started T_J = 25°C, L = 3 mH, I_{AV} = 9 A, V_{DD} = 100 V, V_{GS} = 15 V. 100% test at L = 0.1 mH, I_{AV} = 24 A.
7. As an N−ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

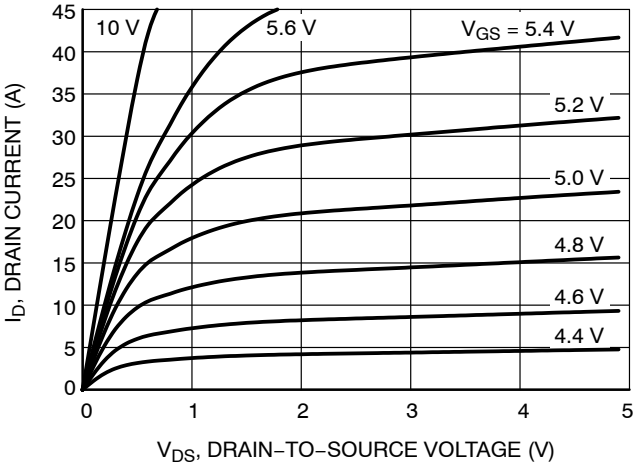


Figure 1. On−Region Characteristics

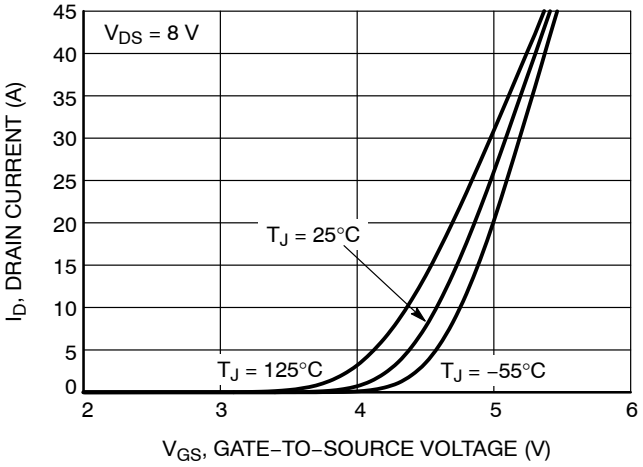


Figure 2. Transfer Characteristics

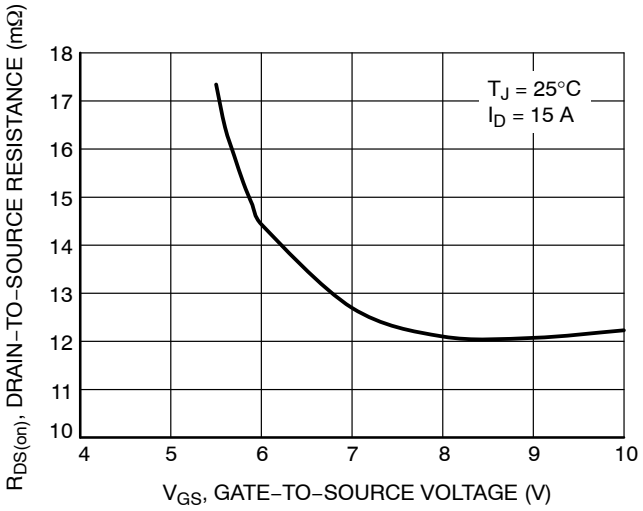


Figure 3. On−Resistance vs. Gate−to−Source Voltage

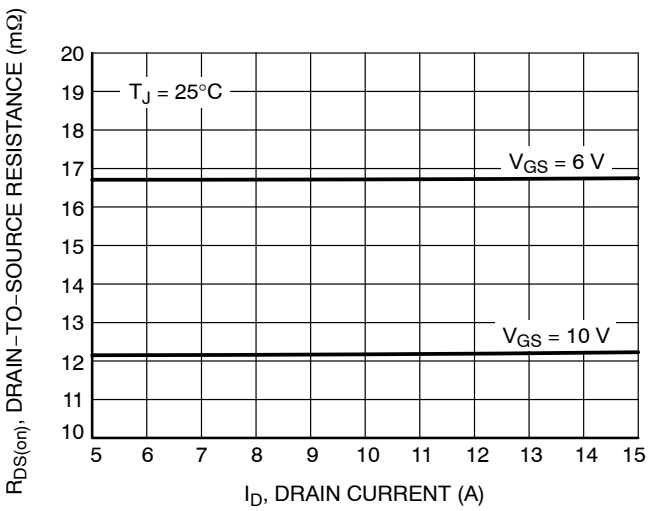


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

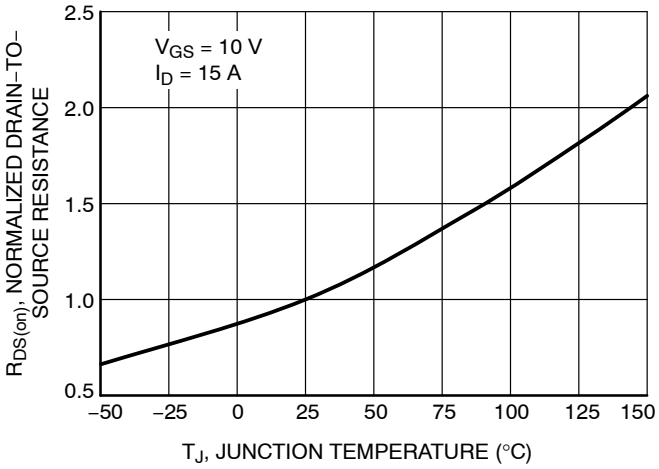


Figure 5. On−Resistance Variation with Temperature

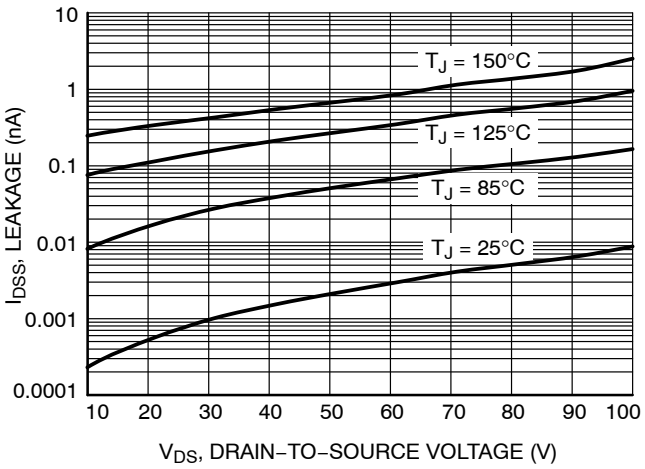


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

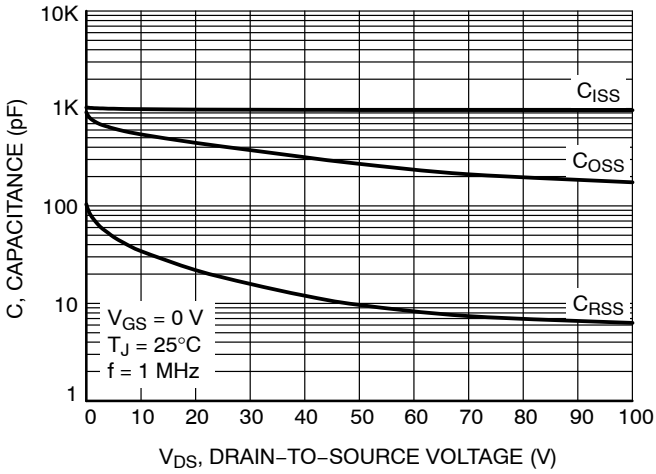


Figure 7. Capacitance Variation

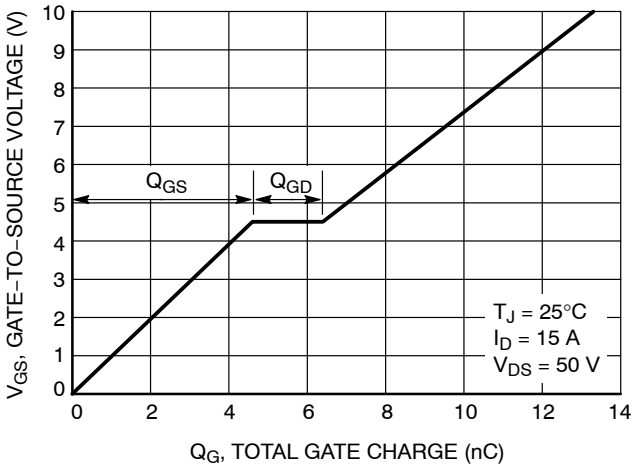


Figure 8. Gate−to−Source Voltage vs. Total Charge

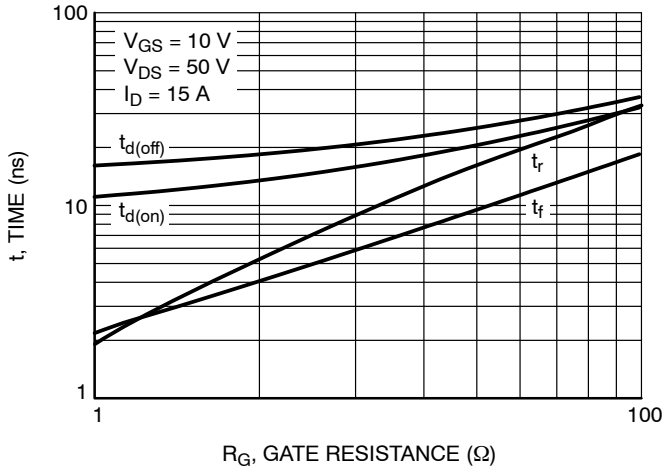


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

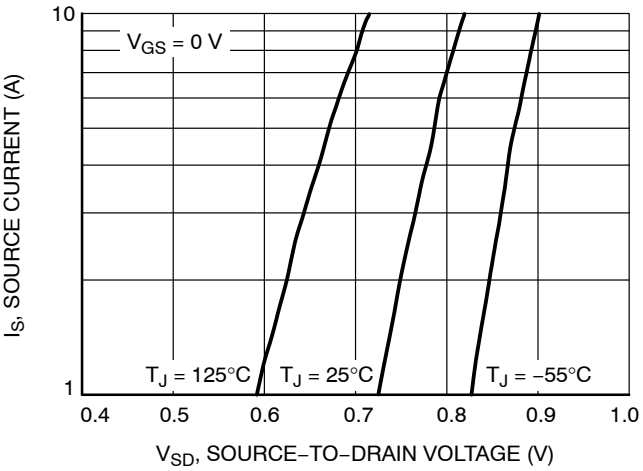


Figure 10. Diode Forward Voltage vs. Current

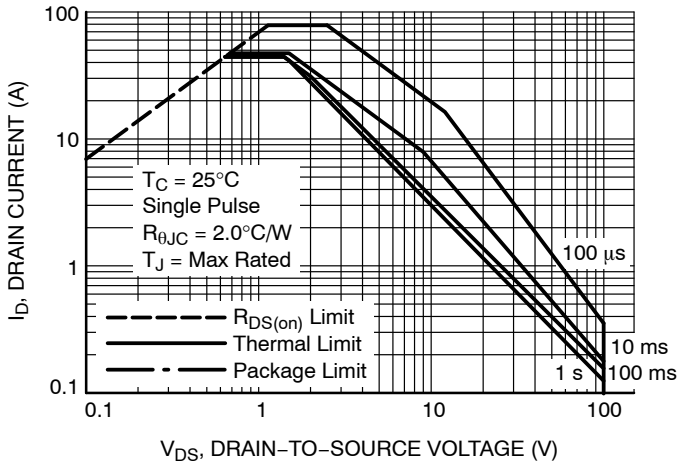


Figure 11. Maximum Rated Forward Biased Safe Operating Area

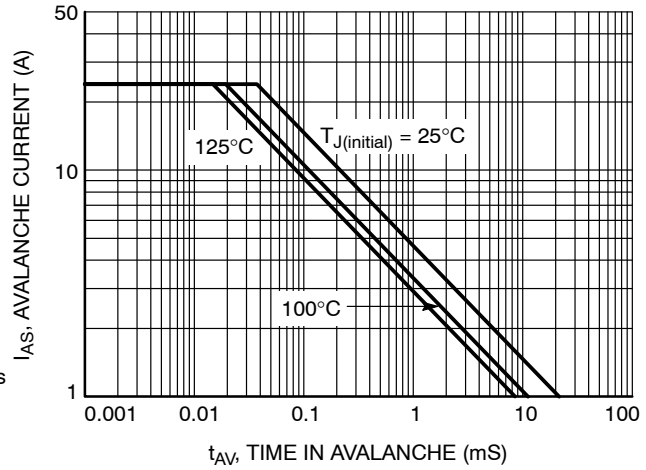


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

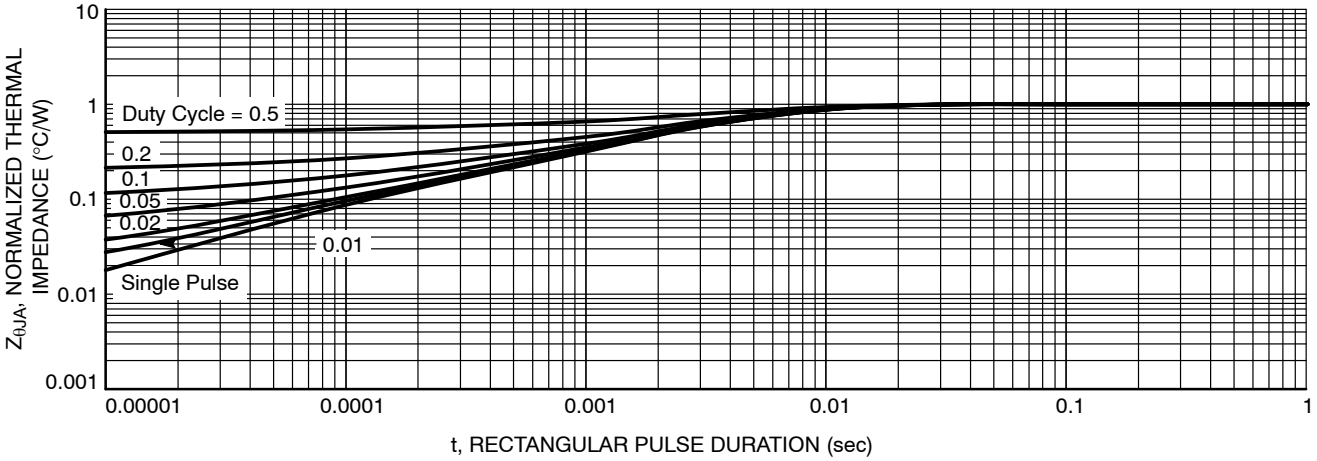
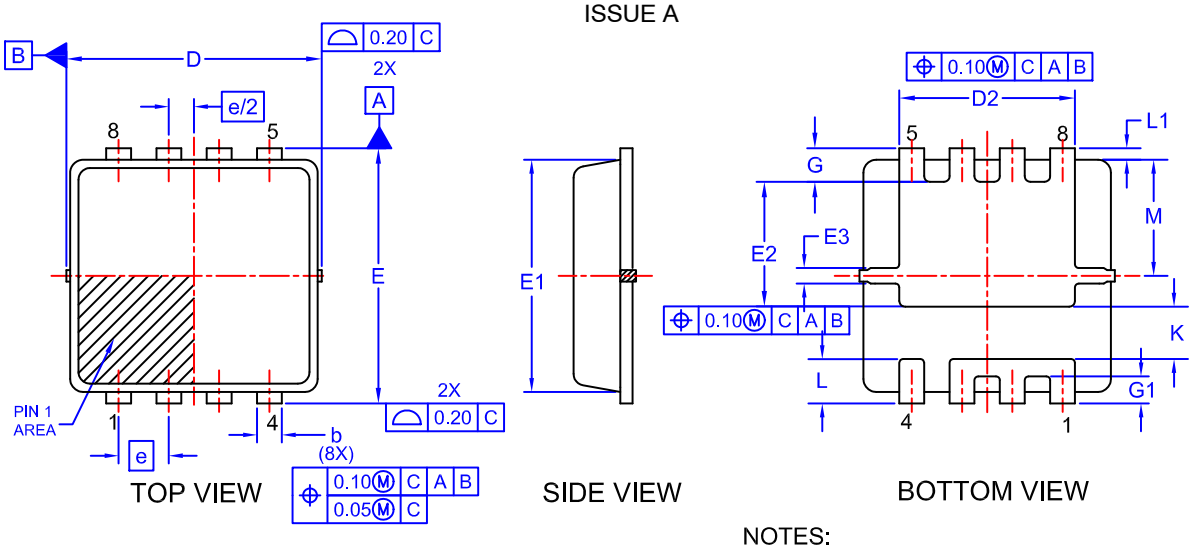


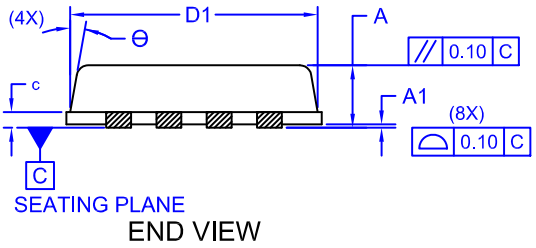
Figure 13. Transient Thermal Impedance

PACKAGE DIMENSIONS

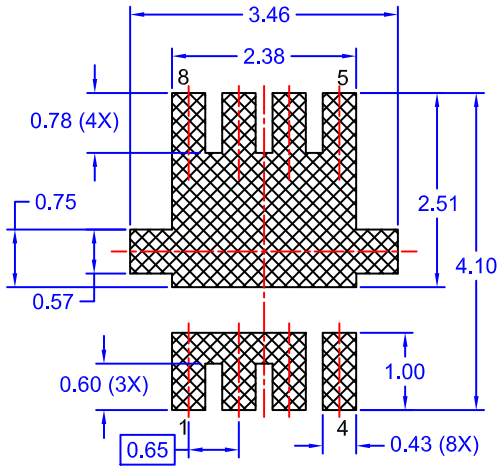
WDFN8 3.3x3.3, 0.65P
CASE 511DY
ISSUE A



NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS D1 & E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60
θ	0	-	12



RECOMMENDED LAND PATTERN

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