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# MOSFET – Power, Single N-Channel

## 100 V, 14.4 mΩ, 45 A



ON Semiconductor®

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## NTTFS012N10MD

### Features

- Shielded Gate MOSFET Technology
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- Low  $Q_{RR}$ , Soft Recovery Body Diode
- Low  $Q_{OSS}$  to Improve Light Load Efficiency
- These Devices are Pb-Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

### Typical Applications

- Primary Switch in Isolated DC-DC Converter
- Synchronous Rectification (SR) in DC-DC and AC-DC
- AC-DC Adapters (USB PD) SR
- Load Switch, Hotswap, and ORing Switch
- BLDC Motor and Solar Inverter

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Breakdown Voltage		$V_{(BR)DSS}$	100	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	45	A
		$T_C = 25^\circ\text{C}$	$P_D$	62	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	9.2	A
		$T_A = 25^\circ\text{C}$	$P_D$	2.7	W
Power Dissipation $R_{\theta JC}$ (Note 2)					
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)					
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	217	A	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	51.8	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{AV} = 9 \text{ A}, L = 3 \text{ mH}$ )		$E_{AS}$	121	mJ	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		$T_L$	300	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

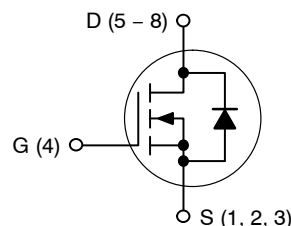
### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	2.0	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	46.5	

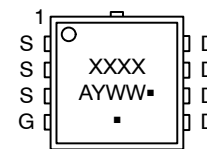
1. Surface-mounted on FR4 board using a 1 in<sup>2</sup> pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
100 V	14.4 mΩ @ 10 V	45 A
	21.0 mΩ @ 6 V	

### N-Channel



### MARKING DIAGRAM



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTTFS012N10MD	WDFN8 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTTFS012N10MD

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		60		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 78\ \mu\text{A}$	2		4	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 78\ \mu\text{A}$ , ref to $25^\circ\text{C}$		-8.1		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}$	12.2	14.4	m $\Omega$
		$V_{GS} = 6\text{ V}$	$I_D = 7.5\text{ A}$	16.7	21.0	
Forward Transconductance	$g_{FS}$	$V_{DS} = 8\text{ V}, I_D = 15\text{ A}$		36		S
Gate-Resistance	$R_G$	$T_A = 25^\circ\text{C}$		0.5	1.6	$\Omega$

## CHARGES & CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		965		pF
Output Capacitance	$C_{OSS}$			270		
Reverse Transfer Capacitance	$C_{RSS}$			8.4		
Output Charge	$Q_{OSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		22		nC
Total Gate Charge	$Q_G(TOT)$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 15\text{ A}$		8		nC
Total Gate Charge	$Q_G(TOT)$			13		
Gate-to-Source Charge	$Q_{GS}$			4.6		
Gate-to-Drain Charge	$Q_{GD}$			1.8		
Plateau Voltage	$V_{GP}$			4.5		

## SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 15\text{ A}, R_G = 6\ \Omega$		12		ns
Rise Time	$t_r$			2.7		
Turn-Off Delay Time	$t_{d(OFF)}$			17		
Fall Time	$t_f$			2.6		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 15\text{ A}$	$T_J = 25^\circ\text{C}$		0.85		V
			$T_J = 125^\circ\text{C}$		0.72		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 7.5\text{ A}$		20		ns	
Reverse Recovery Charge	$Q_{RR}$			116		nC	
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 15\text{ A}$		36		ns	
Reverse Recovery Charge	$Q_{RR}$			34		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

4.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

5. Pulse Test: Pulse Width < 300  $\mu\text{s}$ . Duty cycle < 2%.

6.  $E_{AS}$  of 121 mJ is based on started  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AV} = 9\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 15\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AV} = 24\text{ A}$ .

7. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

# NTTFS012N10MD

## TYPICAL CHARACTERISTICS

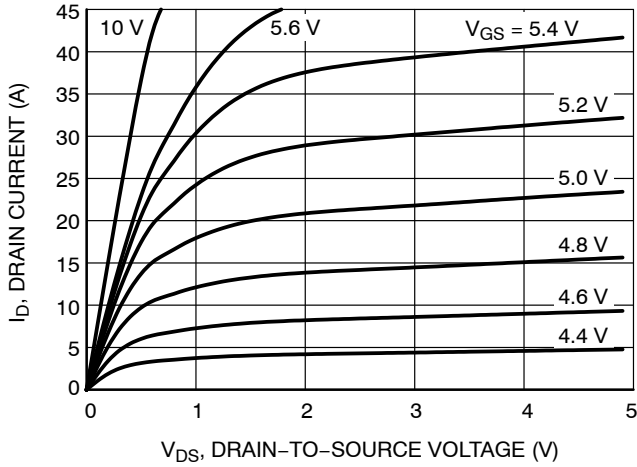


Figure 1. On-Region Characteristics

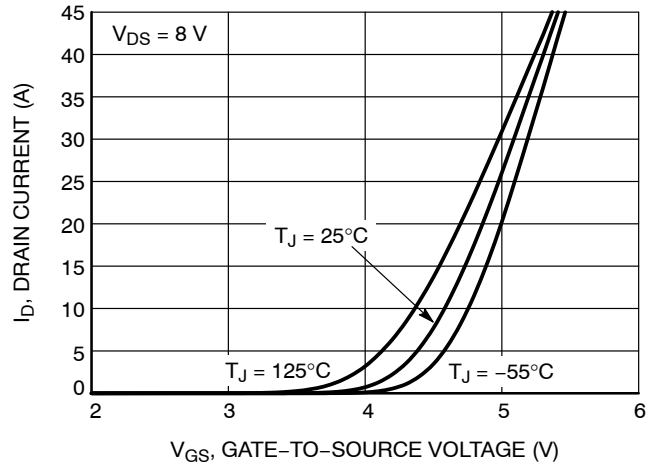


Figure 2. Transfer Characteristics

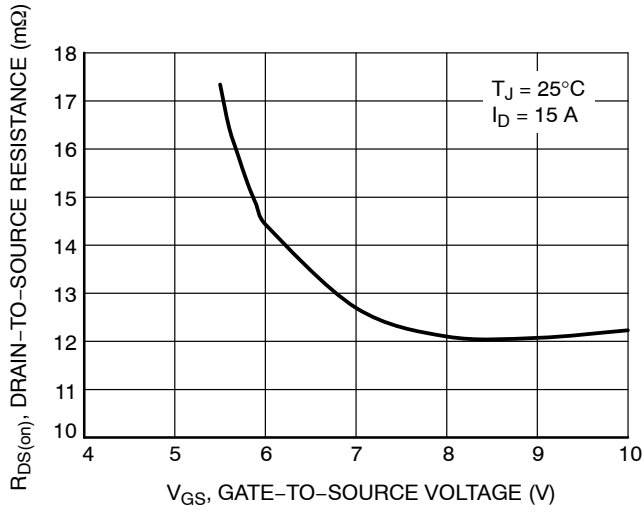


Figure 3. On-Resistance vs. Gate-to-Source Voltage

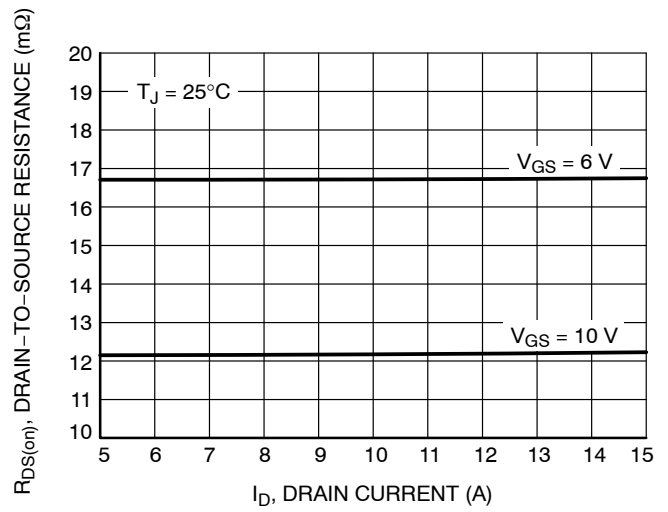


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

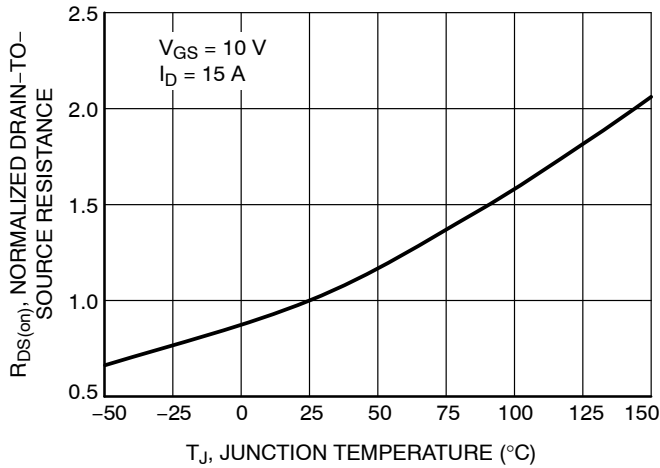


Figure 5. On-Resistance Variation with Temperature

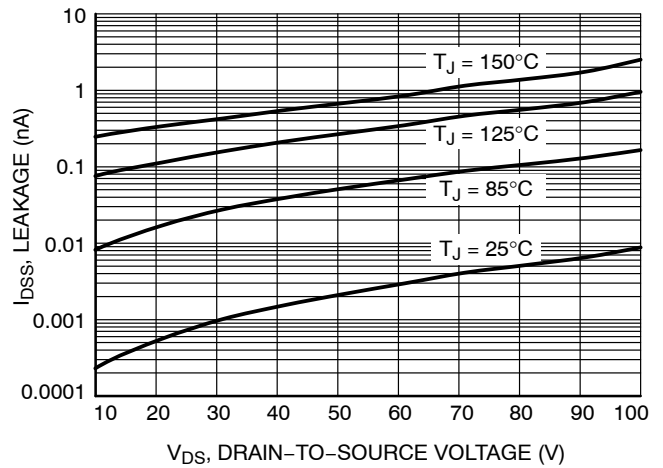


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

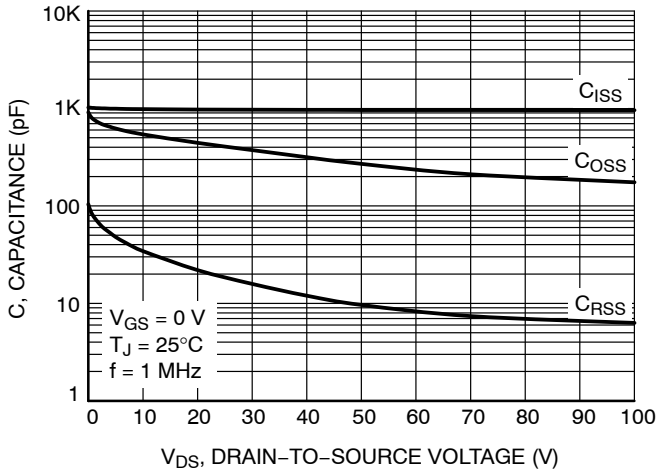


Figure 7. Capacitance Variation

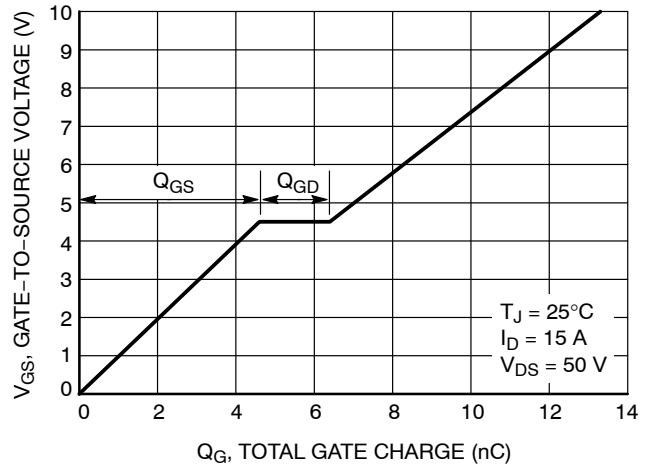


Figure 8. Gate-to-Source Voltage vs. Total Charge

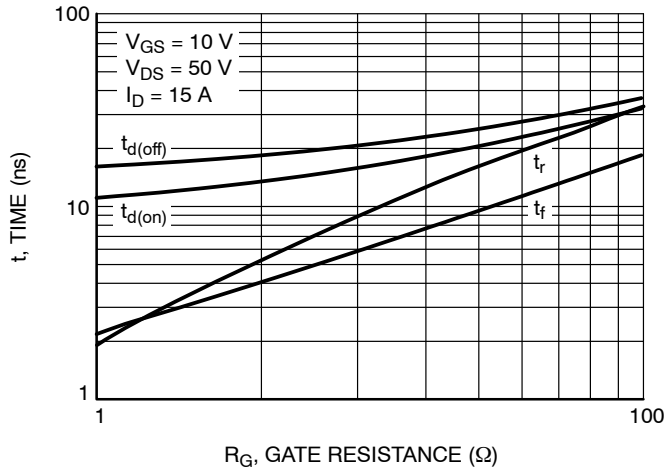


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

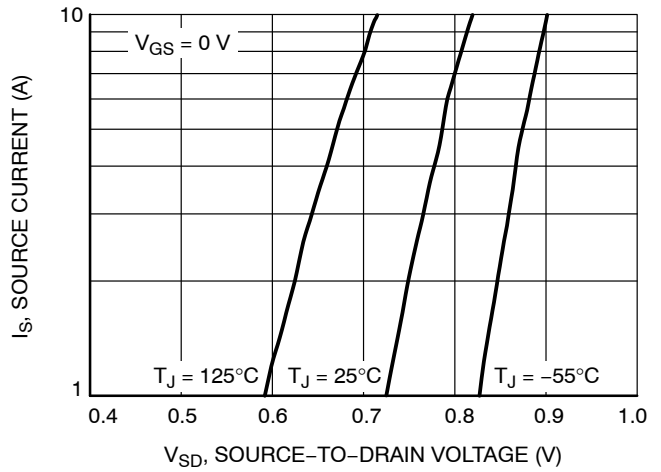


Figure 10. Diode Forward Voltage vs. Current

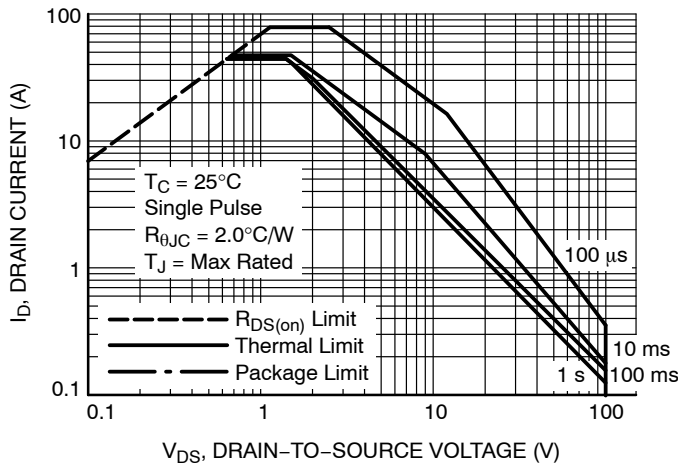


Figure 11. Maximum Rated Forward Biased Safe Operating Area

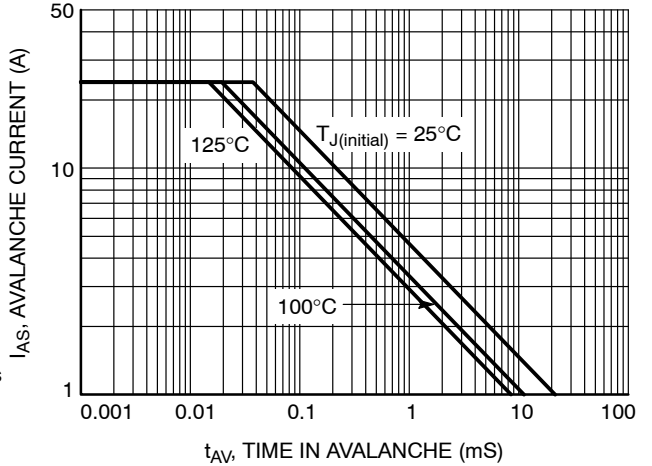


Figure 12. Maximum Drain Current vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

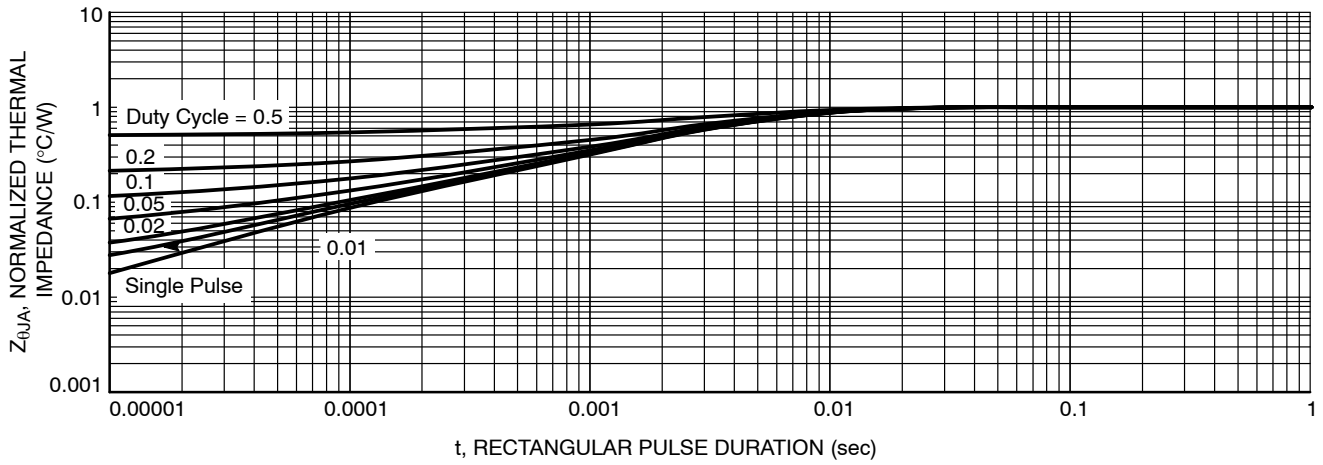
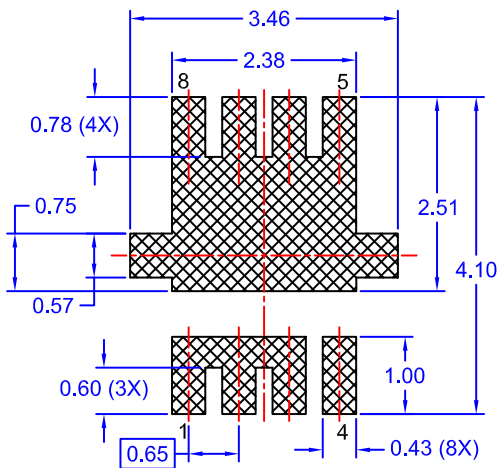
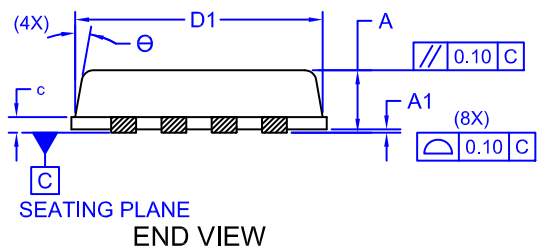
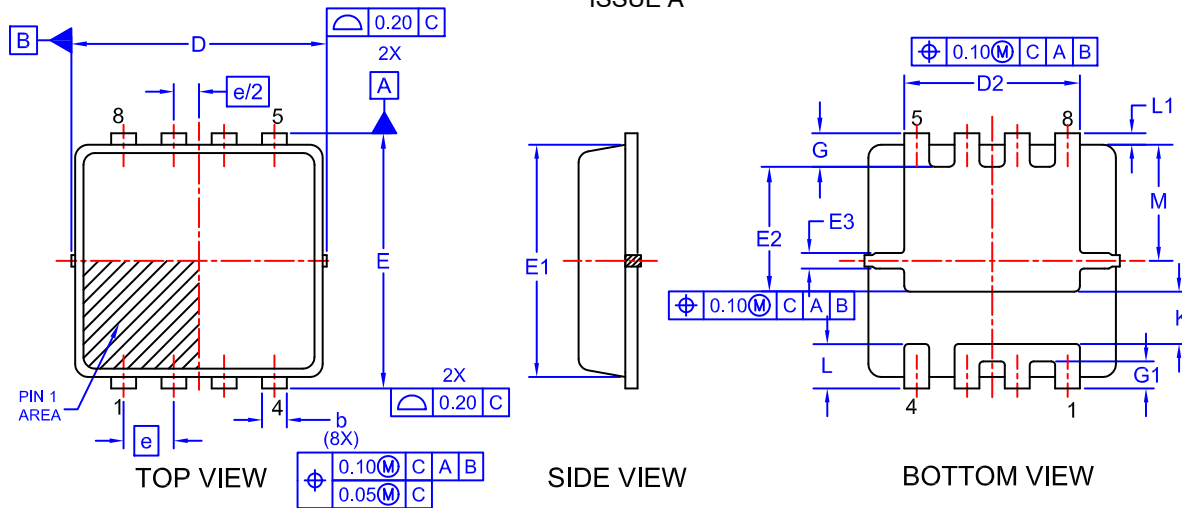


Figure 13. Transient Thermal Impedance

# NTTFS012N10MD

## PACKAGE DIMENSIONS


WDFN8 3.3x3.3, 0.65P  
CASE 511DY  
ISSUE A



**NOTES:**

1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS D1 & E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60
Θ	0	-	12

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