



**THE DATASHEET OF  
ISL8843AAUZ**



## ISL8840A, ISL8841A, ISL8842A, ISL8843A, ISL8844A, ISL8845A

### High Performance Industry Standard Single-Ended Current Mode PWM Controller

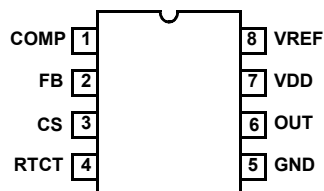
The ISL884xA are high performance drop-in replacements for the popular 28C4x and 18C4x PWM controllers suitable for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Their fast signal propagation and output switching characteristics make them an ideal product for existing and new designs.

Features include 30V operation, low operating current, 90 $\mu$ A start-up current, adjustable operating frequency to 2MHz, and high peak current drive capability with 20ns rise and fall times.

PART NUMBER	RISING UVLO	MAX. DUTY CYCLE
ISL8840A	7.0	100%
ISL8841A	7.0	50%
ISL8842A	14.4V	100%
ISL8843A	8.4V	100%
ISL8844A	14.4V	50%
ISL8845A	8.4V	50%

### Pinout

ISL8840A, ISL8841A, ISL8842A, ISL8843A, ISL8844A, ISL8845A  
(8 LD SOIC, MSOP)  
TOP VIEW



### Features

- 1A MOSFET gate driver
- 90 $\mu$ A start-up current, 125 $\mu$ A maximum
- 35ns propagation delay current sense to output
- Fast transient response with peak current mode control
- 30V operation
- Adjustable switching frequency to 2MHz
- 20ns rise and fall times with 1nF output load
- Trimmed timing capacitor discharge current for accurate deadtime/maximum duty cycle control
- 1.5MHz bandwidth error amplifier
- Tight tolerance voltage reference over line, load and temperature
- $\pm$ 3% current limit threshold
- Pb-free plus anneal available and ELV, WEEE, RoHS Compliant

### Applications

- Telecom and datacom power
- Wireless base station power
- File server power
- Industrial power systems
- PC power supplies
- Isolated buck and flyback regulators
- Boost regulators

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**Ordering Information**

PART NUMBER (Notes 1, 2)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 3)	TEMP. RANGE
ISL8840AABZ	8840 AABZ	8 Ld SOIC	M8.15	Tube	-40 to +105°C
ISL8840AABZ-T				Reel, 2.5k	
ISL8840AAUZ	40AAZ	8 Ld MSOP	M8.118	Tube	-40 to +105°C
ISL8840AAUZ-T				Reel, 2.5k	
ISL8840AMUZ-T	40AMZ	8 Ld MSOP	M8.118	Reel, 2.5k	-55 to +125°C
ISL8841AMBZ	8841 AMBZ	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL8841AMBZ-T				Reel, 2.5k	
ISL8841AMUZ	41AMZ	8 Ld MSOP	M8.118	Tube	-55 to +125°C
ISL8841AMUZ-T				Reel, 2.5k	
ISL8842AABZ	8842 AABZ	8 Ld SOIC	M8.15	Tube	-40 to +105°C
ISL8842AABZ-T				Reel, 2.5k	
ISL8842AAUZ	42AAZ	8 Ld MSOP	M8.118	Tube	-40 to +105°C
ISL8842AAUZ-T				Reel, 2.5k	
ISL8842AMBZ	8842 AMBZ	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL8842AMBZ-T				Reel, 2.5k	
ISL8842AMUZ	42AMZ	8 Ld MSOP	M8.118	Tube	-55 to +125°C
ISL8842AMUZ-T				Reel, 2.5k	
ISL8843AABZ	8843 AABZ	8 Ld SOIC	M8.15	Tube	-40 to +105°C
ISL8843AABZ-T				Reel, 2.5k	
ISL8843AAUZ	43AAZ	8 Ld MSOP	M8.118	Tube	-40 to +105°C
ISL8843AAUZ-T				Reel, 2.5k	
ISL8843AMBZ	8843 AMBZ	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL8843AMBZ-T				Reel, 2.5k	
ISL8843AMUZ	43AMZ	8 Ld MSOP	M8.118	Tube	-55 to +125°C
ISL8843AMUZ-T				Reel, 2.5k	
ISL8844AABZ	8844 AABZ	8 Ld SOIC	M8.15	Tube	-40 to +105°C
ISL8844AABZ-T				Reel, 2.5k	
ISL8844AAUZ	44AAZ	8 Ld MSOP	M8.118	Tube	-40 to +105°C
ISL8844AAUZ-T				Reel, 2.5k	
ISL8844AMBZ	8844 AMBZ	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL8844AMBZ-T				Reel, 2.5k	
ISL8844AMUZ	44AMZ	8 Ld MSOP	M8.118	Tube	-55 to +125°C
ISL8844AMUZ-T				Reel, 2.5k	

PART NUMBER (Notes 1, 2)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 3)	TEMP. RANGE
ISL8845AABZ	8845 AABZ	8 Ld SOIC	M8.15	Tube	-40 to +105°C
ISL8845AABZ-T				Reel, 2.5k	
ISL8845AAUZ	45AAZ	8 Ld MSOP	M8.118	Tube	-40 to +105°C
ISL8845AAUZ-T				Reel, 2.5k	
ISL8845AMBZ	8845 AMBZ	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL8845AMBZ-T				Reel, 2.5k	
ISL8845AMUZ	45AMZ	8 Ld MSOP	M8.118	Tube	-55 to +125°C
ISL8845AMUZ-T				Reel, 2.5k	

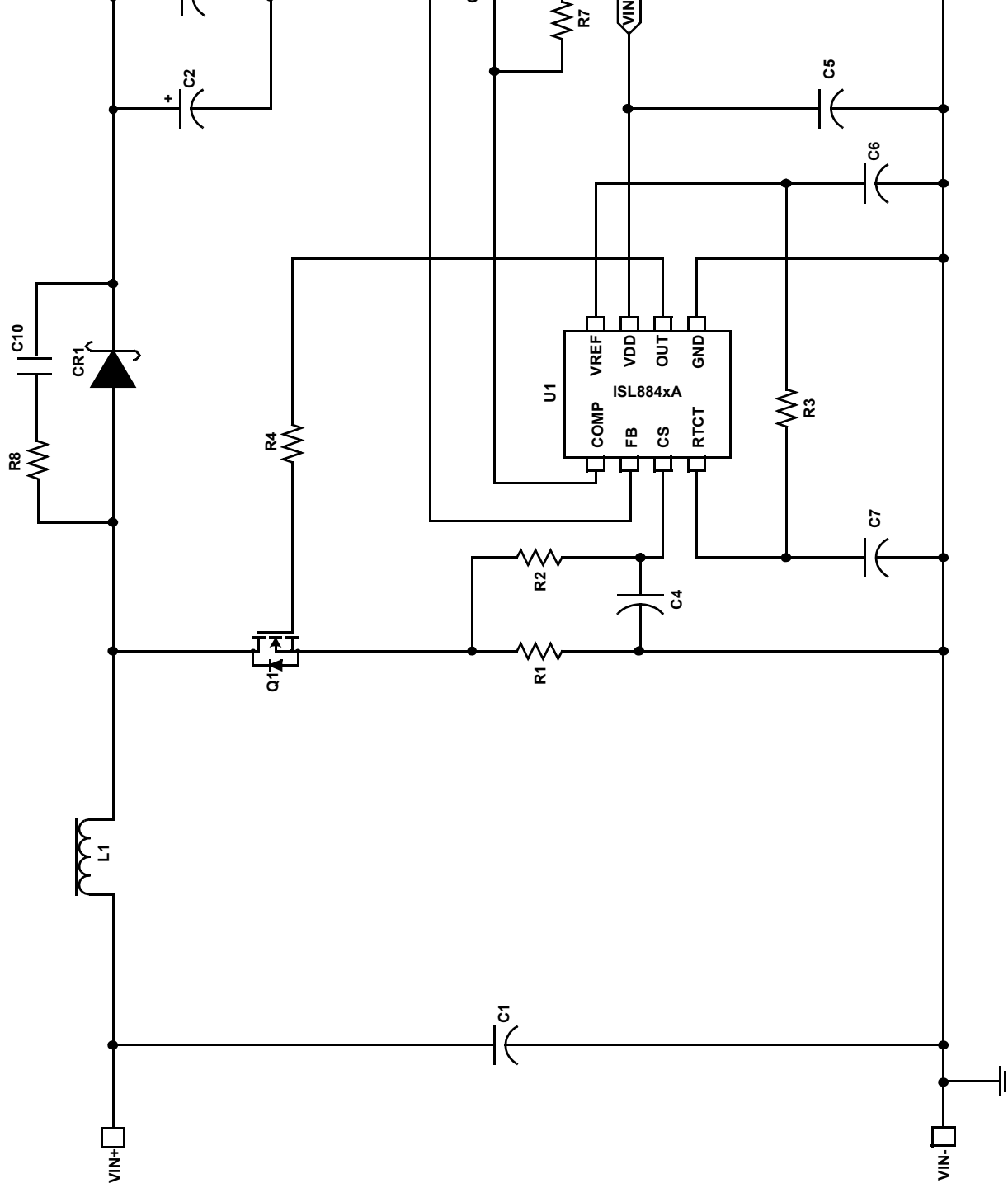
## NOTES:

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the [ISL8840A](#), [ISL8841A](#), [ISL8842A](#), [ISL8843A](#), [ISL8844A](#), [ISL8845A](#), product pages. For more information about MSL, see [TB363](#).
3. Refer to [TB347](#) for details about reel specifications.





# Typical Application - Boost Converter



### Absolute Maximum Ratings

Supply Voltage, $V_{DD}$	GND -0.3V to +30V
OUT	GND -0.3V to $V_{DD} + 0.3V$
Signal Pins	GND -0.3V to 6.0V
Peak GATE Current	1A
ESD Classification	
Human Body Model (Per JESD22-A114C.01)	2000V
Machine Model (Per EIA/JESD22-A115-A)	200V
Charged Device Model (Per JESD22-C191-A)	1000V

### Thermal Information

Thermal Resistance (Typical, Note 4)	$\theta_{JA}$ (°C/W)
SOIC Package	100
MSOP Package	130
Maximum Junction Temperature	-55°C to +150°C
Maximum Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering 10s)	+300°C (SOIC, MSOP - Lead Tips Only)

### Operating Conditions

Temperature Range	
ISL884xAAxZ	-40°C to +105°C
ISL884xAMxZ	-55°C to +125°C
Supply Voltage Range (Typical, Note 5)	
ISL884xA	9V to 30V

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

+150°C max junction temperature is intended for short periods of time to prevent shortening the lifetime. Constantly operated at +150°C may shorten the life of the part.

NOTES:

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Technical Brief TB379 for details.
- All voltages are with respect to GND.

## Electrical Specifications

### ISL884xAA

Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic on page 5 and page 6.  $V_{DD} = 15V$ ,  $R_T = 10k\Omega$ ,  $C_T = 3.3nF$ ,  $T_A = -40$  to  $+105^\circ C$  (Note 6). Typical values are at  $T_A = +25^\circ C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>UNDERVOLTAGE LOCKOUT</b>					
START Threshold (ISL8840A, ISL8841A)		6.5	7.0	7.5	V
START Threshold (ISL8843A, ISL8845A)		8.0	8.4	9.0	V
START Threshold (ISL8842A, ISL8844A)	(Note 9)	13.3	14.3	15.3	V
STOP Threshold (ISL8840A, ISL8841A)		6.1	6.6	6.9	V
STOP Threshold (ISL8843A, ISL8845A)		7.3	7.6	8.0	V
STOP Threshold (ISL8842A, ISL8844A)		8.0	8.8	9.6	V
Hysteresis (ISL8840A, ISL8841A)		-	0.4	-	V
Hysteresis (ISL8843A, ISL8845A)		-	0.8	-	V
Hysteresis (ISL8842A, ISL8844A)		-	5.4	-	V
Startup Current, $I_{DD}$	$V_{DD} < \text{START Threshold}$	-	90	125	$\mu A$
Operating Current, $I_{DD}$	(Note 7)	-	2.9	4.0	mA
Operating Supply Current, $I_D$	Includes 1nF GATE loading	-	4.75	5.5	mA
<b>REFERENCE VOLTAGE</b>					
Overall Accuracy	Over line ( $V_{DD} = 12V$ to $30V$ ), load, temperature	4.925	5.000	5.050	V
Long Term Stability	$T_A = +125^\circ C$ , 1000 hours (Note 8)	-	5	-	mV
Current Limit, Sourcing		-20	-	-	mA
Current Limit, Sinking		5	-	-	mA
<b>CURRENT SENSE</b>					
Input Bias Current	$V_{CS} = 1V$	-1.0	-	1.0	$\mu A$

Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic on page 5 and page 6.  $V_{DD} = 15V$ ,  $R_T = 10k\Omega$ ,  $C_T = 3.3nF$ ,  $T_A = -40$  to  $+105^\circ C$  (Note 6). Typical values are at  $T_A = +25^\circ C$  (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CS Offset Voltage	$V_{CS} = 0V$ (Note 8)	95	100	105	mV
COMP to PWM Comparator Offset Voltage	$V_{CS} = 0V$ (Note 8)	0.80	1.15	1.30	V
Input Signal, Maximum		0.97	1.00	1.03	V
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	$0 < V_{CS} < 910mV$ , $V_{FB} = 0V$	2.5	3.0	3.5	V/V
CS to OUT Delay		-	35	55	ns
<b>ERROR AMPLIFIER</b>					
Open Loop Voltage Gain	(Note 8)	60	90	-	dB
Unity Gain Bandwidth	(Note 8)	1.0	1.5	-	MHz
Reference Voltage	$V_{FB} = V_{COMP}$	2.475	2.500	2.530	V
FB Input Bias Current	$V_{FB} = 0V$	-1.0	-0.2	1.0	$\mu A$
COMP Sink Current	$V_{COMP} = 1.5V$ , $V_{FB} = 2.7V$	1.0	4.86	-	mA
COMP Source Current	$V_{COMP} = 1.5V$ , $V_{FB} = 2.3V$	-0.4	-0.58	-	mA
COMP VOH	$V_{FB} = 2.3V$	4.80	-	VREF	V
COMP VOL	$V_{FB} = 2.7V$	0.4	-	1.0	V
PSRR	Frequency = 120Hz, $V_{DD} = 12V$ to 30V (Note 8)	60	80	-	dB
<b>OSCILLATOR</b>					
Frequency Accuracy	Initial, $T_A = +25^\circ C$	48	51	53	kHz
Frequency Variation with $V_{DD}$	$T_A = +25^\circ C$ , $(f_{30V} - f_{10V})/f_{30V}$	-	0.2	1.0	%
Temperature Stability	(Note 8)	-	-	5	%
Amplitude, Peak to Peak	Static Test	-	1.75	-	V
RTCT Discharge Voltage (Valley Voltage)	Static Test	-	1.0	-	V
Discharge Current	RTCT = 2.0V	6.5	7.8	8.5	mA
<b>OUTPUT</b>					
Gate VOH	$V_{DD}$ to OUT, $I_{OUT} = -200mA$	-	1.0	2.0	V
Gate VOL	OUT to GND, $I_{OUT} = 200mA$	-	1.0	2.0	V
Peak Output Current	$C_{OUT} = 1nF$ (Note 8)	-	1.0	-	A
Rise Time	$C_{OUT} = 1nF$ (Note 8)	-	20	40	ns
Fall Time	$C_{OUT} = 1nF$ (Note 8)	-	20	40	ns
GATE VOL UVLO Clamp Voltage	$V_{DD} = 5V$ , $I_{LOAD} = 1mA$	-	-	1.2	V
<b>PWM</b>					
Maximum Duty Cycle (ISL8840A, ISL8842A, ISL8843A)	COMP = VREF	94.0	96.0	-	%
Maximum Duty Cycle (ISL8841A, ISL8844A, ISL8845A)	COMP = VREF	47.0	48.0	-	%
Minimum Duty Cycle	COMP = GND	-	-	0	%

## NOTES:

- Specifications at  $-40^\circ C$  and  $+105^\circ C$  are guaranteed by  $+25^\circ C$  test with margin limits.
- This is the  $V_{DD}$  current consumed when the device is active but not switching. Does not include gate drive current.
- These parameters, although guaranteed, are not 100% tested in production.
- Adjust  $V_{DD}$  above the start threshold and then lower to 15V.

**ISL884xAM**

Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic.  $V_{DD} = 15V$ ,  $R_T = 10k\Omega$ ,  $C_T = 3.3nF$ ,  $T_A = -55$  to  $+125^\circ C$  (Note 10), Typical values are at  $T_A = +25^\circ C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>UNDERVOLTAGE LOCKOUT</b>					
START Threshold (ISL8840A, ISL8841A)		6.5	7.0	7.5	V
START Threshold (ISL8843A, ISL8845A)		8.0	8.4	9.0	V
START Threshold (ISL8842A, ISL8844A)	(Note 13)	13.3	14.3	15.3	V
STOP Threshold (ISL8840A, ISL8841A)		6.1	6.6	6.9	V
STOP Threshold (ISL8843A, ISL8845A)		7.3	7.6	8.0	V
STOP Threshold (ISL8842A, ISL8844A)		8.0	8.8	9.6	V
Hysteresis (ISL8840A, ISL8841A)		-	0.4	-	V
Hysteresis (ISL8843A, ISL8845A)		-	0.8	-	V
Hysteresis (ISL8842A, ISL8844A)		-	5.4	-	V
Startup Current, $I_{DD}$	$V_{DD} < \text{START Threshold}$	-	90	125	$\mu A$
Operating Current, $I_{DD}$	(Note 11)	-	2.9	4.0	mA
Operating Supply Current, $I_D$	Includes 1nF GATE loading	-	4.75	5.5	mA
<b>REFERENCE VOLTAGE</b>					
Overall Accuracy	Over line ( $V_{DD} = 12V$ to $30V$ ), load, temperature	4.900	5.000	5.050	V
Long Term Stability	$T_A = +125^\circ C$ , 1000 hours (Note 12)	-	5	-	mV
Current Limit, Sourcing		-20	-	-	mA
Current Limit, Sinking		5	-	-	mA
<b>CURRENT SENSE</b>					
Input Bias Current	$V_{CS} = 1V$	-1.0	-	1.0	$\mu A$
CS Offset Voltage	$V_{CS} = 0V$ (Note 12)	95	100	105	mV
COMP to PWM Comparator Offset Voltage	$V_{CS} = 0V$ (Note 12)	0.80	1.15	1.30	V
Input Signal, Maximum		0.97	1.00	1.03	V
Gain, $A_{CS} = \Delta V_{COMP} / \Delta V_{CS}$	$0 < V_{CS} < 910mV$ , $V_{FB} = 0V$	2.5	3.0	3.5	V/V
CS to OUT Delay		-	35	60	ns
<b>ERROR AMPLIFIER</b>					
Open Loop Voltage Gain	(Note 12)	60	90	-	dB
Unity Gain Bandwidth	(Note 12)	1.0	1.5	-	MHz
Reference Voltage	$V_{FB} = V_{COMP}$	2.460	2.500	2.535	V
FB Input Bias Current	$V_{FB} = 0V$	-1.0	-0.2	1.0	$\mu A$
COMP Sink Current	$V_{COMP} = 1.5V$ , $V_{FB} = 2.7V$	1.0	4.86	-	mA
COMP Source Current	$V_{COMP} = 1.5V$ , $V_{FB} = 2.3V$	-0.4	-0.58	-	mA
COMP VOH	$V_{FB} = 2.3V$	4.80	-	$V_{REF}$	V
COMP VOL	$V_{FB} = 2.7V$	0.4	-	1.0	V
PSRR	Frequency = 120Hz, $V_{DD} = 12V$ to $30V$ (Note 12)	60	80	-	dB
<b>OSCILLATOR</b>					
Frequency Accuracy	Initial, $T_A = +25^\circ C$	48	51	53	kHz
Frequency Variation with $V_{DD}$	$T_A = +25^\circ C$ , $(f_{30V} - f_{10V}) / f_{30V}$	-	0.2	1.0	%
Temperature Stability	(Note 12)	-	-	5	%

Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic.  $V_{DD} = 15V$ ,  $R_T = 10k\Omega$ ,  $C_T = 3.3nF$ ,  $T_A = -55$  to  $+125^\circ C$  (Note 10), Typical values are at  $T_A = +25^\circ C$  (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Amplitude, Peak to Peak	Static Test	-	1.75	-	V
RTCT Discharge Voltage (Valley Voltage)	Static Test	-	1.0	-	V
Discharge Current	RTCT = 2.0V	6.2	8.0	8.5	mA
<b>OUTPUT</b>					
Gate VOH	$V_{DD} - OUT$ , $I_{OUT} = -200mA$	-	1.0	2.0	V
Gate VOL	$OUT - GND$ , $I_{OUT} = 200mA$	-	1.0	2.0	V
Peak Output Current	$C_{OUT} = 1nF$ (Note 12)	-	1.0	-	A
Rise Time	$C_{OUT} = 1nF$ (Note 12)	-	20	40	ns
Fall Time	$C_{OUT} = 1nF$ (Note 12)	-	20	40	ns
GATE VOL UVLO Clamp Voltage	$V_{DD} = 5V$ , $I_{LOAD} = 1mA$	-	-	1.2	V
<b>PWM</b>					
Maximum Duty Cycle (ISL8840A, ISL8842A, ISL8843A)	COMP = VREF	94.0	96.0	-	%
Maximum Duty Cycle (ISL8841A, ISL8844A, ISL8845A)	COMP = VREF	47.0	48.0	-	%
Minimum Duty Cycle	COMP = GND	-	-	0	%

## NOTES:

10. Specifications at  $-55^\circ C$  and  $+125^\circ C$  are guaranteed by  $+25^\circ C$  test with margin limits.
11. This is the  $V_{DD}$  current consumed when the device is active but not switching. Does not include gate drive current.
12. These parameters, although guaranteed, are not 100% tested in production.
13. Adjust  $V_{DD}$  above the start threshold and then lower to 15V.

## Typical Performance Curves

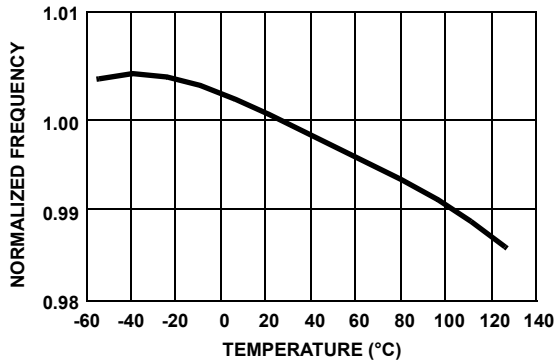


FIGURE 1. FREQUENCY vs TEMPERATURE

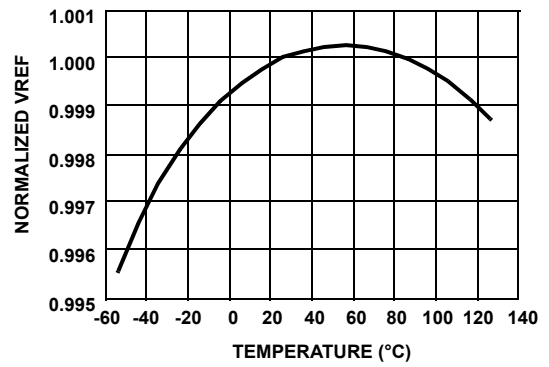


FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

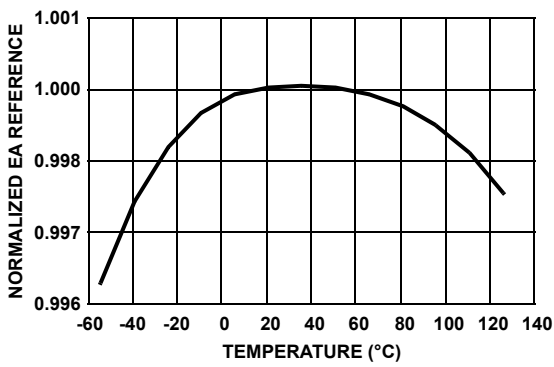


FIGURE 3. EA REFERENCE vs TEMPERATURE

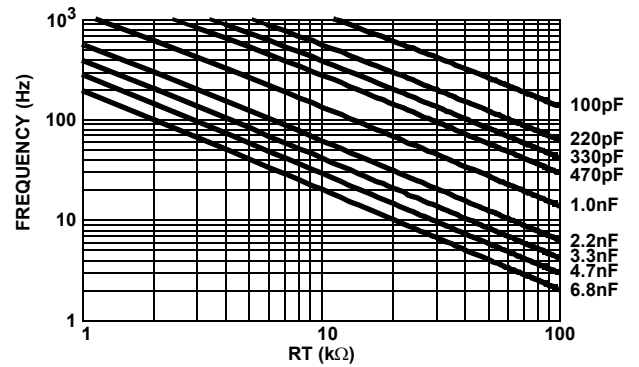


FIGURE 4. RESISTANCE FOR CT CAPACITOR VALUES GIVEN

## Pin Descriptions

**RTCT** - This is the oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, RT, between VREF and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time,  $t_C$ , the discharge time,  $t_D$ , the switching frequency,  $f$ , and the maximum duty cycle,  $D_{max}$ , can be approximated from the following equations:

$$t_C \approx 0.533 \cdot RT \cdot CT \quad (\text{EQ. 1})$$

$$t_D \approx -RT \cdot CT \cdot \ln\left(\frac{0.008 \cdot RT - 3.83}{0.008 \cdot RT - 1.71}\right) \quad (\text{EQ. 2})$$

$$f = 1/(t_C + t_D) \quad (\text{EQ. 3})$$

$$D = t_C \cdot f \quad (\text{EQ. 4})$$

The formulae have increased error at higher frequencies due to propagation delays. Figure 4 may be used as a guideline in selecting the capacitor and resistor values required for a given frequency.

**COMP** - COMP is the output of the error amplifier and the input of the PWM comparator. The control loop frequency compensation network is connected between the COMP and FB pins.

**FB** - The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The non-inverting input of the error amplifier is internally tied to a reference voltage.

**CS** - This is the current sense input to the PWM comparator. The range of the input signal is nominally 0V to 1.0V and has an internal offset of 100mV.

**GND** - GND is the power and small signal reference ground for all functions.

**OUT** - This is the drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A. This GATE output is actively held low when  $V_{DD}$  is below the UVLO threshold.

**VDD** -  $V_{DD}$  is the power connection for the device. The total supply current will depend on the load applied to OUT. Total  $I_{DD}$  current is the sum of the operating current and the average output current. Knowing the operating frequency,  $f$ , and the MOSFET gate charge,  $Q_g$ , the average output current can be calculated from:

$$I_{OUT} = Q_g \times f \quad (\text{EQ. 5})$$

To optimize noise immunity, bypass  $V_{DD}$  to GND with a ceramic capacitor as close to the  $V_{DD}$  and GND pins as possible.

**VREF** - The 5.00V reference voltage output. +1.0/-1.5% tolerance over line, load and operating temperature. Bypass to GND with a 0.1 $\mu$ F to 3.3 $\mu$ F capacitor to filter this output as needed.

## Functional Description

### Features

The ISL884xA current mode PWM makes an ideal choice for low-cost flyback and forward topology applications. With its greatly improved performance over industry standard parts, it is the obvious choice for new designs or existing designs which require updating.

### Oscillator

The ISL884xA has a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from VREF and a capacitor to GND on the RTCT pin. (Please refer to Figure 4 for the resistor and capacitance required for a given frequency.)

### Soft-Start Operation

Soft-start must be implemented externally. One method, illustrated below, clamps the voltage on COMP.

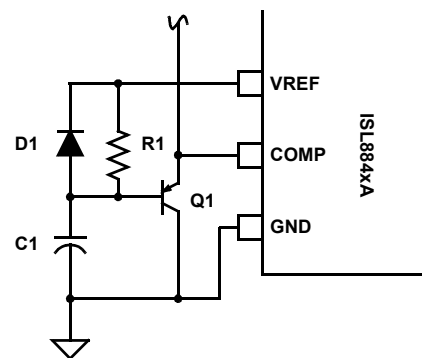


FIGURE 5. SOFT-START

The COMP pin is clamped to the voltage on capacitor C1 plus a base-emitter junction by transistor Q1. C1 is charged from VREF through resistor R1 and the base current of Q1. At power-up C1 is fully discharged, COMP is at ~0.7V, and the duty cycle is zero. As C1 charges, the voltage on COMP increases, and the duty cycle increases in proportion to the voltage on C1. When COMP reaches the steady state operating point, the control loop takes over and soft start is complete. C1 continues to charge up to VREF and no longer affects COMP. During power down, diode D1 quickly discharges C1 so that the soft start circuit is properly initialized prior to the next power on sequence.

### Gate Drive

The ISL884xA is capable of sourcing and sinking 1A peak current. To limit the peak current through the IC, an optional external resistor may be placed between the totem-pole output

of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

### Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation may be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability.

Slope compensation may be accomplished by summing an external ramp with the current feedback signal or by subtracting the external ramp from the voltage feedback error signal. Adding the external ramp to the current feedback signal is the more popular method.

From the small signal current-mode model [1] it can be shown that the naturally-sampled modulator gain,  $F_m$ , without slope compensation, is in Equation 6.

$$F_m = \frac{1}{S_n T_{sw}} \quad (\text{EQ. 6})$$

where  $S_n$  is the slope of the sawtooth signal and  $T_{sw}$  is the duration of the half-cycle. When an external ramp is added, the modulator gain becomes:

$$F_m = \frac{1}{(S_n + S_e) T_{sw}} = \frac{1}{m_c S_n T_{sw}} \quad (\text{EQ. 7})$$

where  $S_e$  is slope of the external ramp and

$$m_c = 1 + \frac{S_e}{S_n} \quad (\text{EQ. 8})$$

The criteria for determining the correct amount of external ramp can be determined by appropriately setting the damping factor of the double-pole located at the switching frequency. The double-pole will be critically damped if the Q-factor is set to 1, over-damped for  $Q < 1$ , and under-damped for  $Q > 1$ . An under-damped condition may result in current loop instability.

$$Q = \frac{1}{\pi(m_c(1-D) - 0.5)} \quad (\text{EQ. 9})$$

where  $D$  is the percent of on time during a switching cycle. Setting  $Q = 1$  and solving for  $S_e$  yields

$$S_e = S_n \left( \left( \frac{1}{\pi} + 0.5 \right) \frac{1}{1-D} - 1 \right) \quad (\text{EQ. 10})$$

Since  $S_n$  and  $S_e$  are the on time slopes of the current ramp and the external ramp, respectively, they can be multiplied by  $t_{ON}$  to obtain the voltage change that occurs during  $t_{ON}$ .

$$V_e = V_n \left( \left( \frac{1}{\pi} + 0.5 \right) \frac{1}{1-D} - 1 \right) \quad (\text{EQ. 11})$$

where  $V_n$  is the change in the current feedback signal ( $\Delta I$ ) during the on time and  $V_e$  is the voltage that must be added by the external ramp.

For a flyback converter,  $V_n$  can be solved for in terms of input voltage, current transducer components, and primary inductance, yielding

$$V_e = \frac{D \cdot T_{sw} \cdot V_{IN} \cdot R_{CS}}{L_p} \left( \left( \frac{1}{\pi} + 0.5 \right) \frac{1}{1-D} - 1 \right) \quad V \quad (\text{EQ. 12})$$

where  $R_{CS}$  is the current sense resistor,  $f_{sw}$  is the switching frequency,  $L_p$  is the primary inductance,  $V_{IN}$  is the minimum input voltage, and  $D$  is the maximum duty cycle.

The current sense signal at the end of the ON time for CCM operation is:

$$V_{CS} = \frac{N_s \cdot R_{CS}}{N_p} \left( I_O + \frac{(1-D) \cdot V_O \cdot f_{sw}}{2L_s} \right) \quad V \quad (\text{EQ. 13})$$

where  $V_{CS}$  is the voltage across the current sense resistor,  $L_s$  is the secondary winding inductance, and  $I_O$  is the output current at current limit. Equation 13 assumes the voltage drop across the output rectifier is negligible.

Since the peak current limit threshold is 1.00V, the total current feedback signal plus the external ramp voltage must sum to this value when the output load is at the current limit threshold.

$$V_e + V_{CS} = 1 \quad (\text{EQ. 14})$$

Substituting Equations 12 and 13 into Equation 14 and solving for  $R_{CS}$  yields

$$R_{CS} = \frac{1}{\frac{D \cdot f_{sw} \cdot V_{IN}}{L_p} \cdot \left( \frac{1}{\pi} + 0.5 \right) \frac{1}{1-D} - 1 + \frac{N_s}{N_p} \cdot \left( I_O + \frac{(1-D) \cdot V_O \cdot f_{sw}}{2L_s} \right)} \quad (\text{EQ. 15})$$

Adding slope compensation is accomplished in the ISL884xA using an external buffer transistor and the RTCT signal. A typical application sums the buffered RTCT signal with the current sense feedback and applies the result to the CS pin as shown in Figure 6.

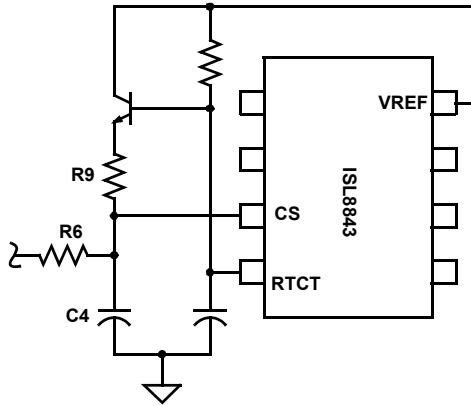


FIGURE 6. SLOPE COMPENSATION

Assuming the designer has selected values for the RC filter ( $R_6$  and  $C_4$ ) placed on the CS pin, the value of  $R_9$  required to add the appropriate external ramp can be found by superposition.

$$V_e = \frac{2.05D \cdot R_6}{R_6 + R_9} \quad \text{V} \quad (\text{EQ. 16})$$

The factor of 2.05 in Equation 16 arises from the peak amplitude of the sawtooth waveform on RTCT minus a base-emitter junction drop. That voltage multiplied by the maximum duty cycle is the voltage source for the slope compensation. Rearranging to solve for  $R_9$  yields:

$$R_9 = \frac{(2.05D - V_e) \cdot R_6}{V_e} \quad \Omega \quad (\text{EQ. 17})$$

The value of  $R_{CS}$  determined in Equation 15 must be rescaled so that the current sense signal presented at the CS pin is that predicted by Equation 13. The divider created by  $R_6$  and  $R_9$  makes this necessary.

$$R'_{CS} = \frac{R_6 + R_9}{R_9} \cdot R_{CS} \quad (\text{EQ. 18})$$

Example:

$$V_{IN} = 12\text{V}$$

$$V_O = 48\text{V}$$

$$L_s = 800\mu\text{H}$$

$$N_s/N_p = 10$$

$$L_p = 8.0\mu\text{H}$$

$$I_O = 200\text{mA}$$

$$\text{Switching Frequency, } f_{sw} = 200\text{kHz}$$

$$\text{Duty Cycle, } D = 28.6\%$$

$$R_6 = 499\Omega$$

Solve for the current sense resistor,  $R_{CS}$ , using Equation 15.

$$R_{CS} = 295\text{m}\Omega$$

Determine the amount of voltage,  $V_e$ , that must be added to the current feedback signal using Equation 12.

$$V_e = 92.4\text{mV}$$

Using Equation 17, solve for the summing resistor,  $R_9$ , from CT to CS.

$$R_9 = 2.67\text{k}\Omega$$

Determine the new value of  $R_{CS}$  ( $R'_{CS}$ ) using Equation 18.

$$R'_{CS} = 350\text{m}\Omega$$

Additional slope compensation may be considered for design margin. The above discussion determines the minimum external ramp that is required. The buffer transistor used to create the external ramp from RTCT should have a sufficiently high gain ( $>200$ ) so as to minimize the required base current. Whatever base current is required reduces the charging current into RTCT and will reduce the oscillator frequency.

### Fault Conditions

A Fault condition occurs if VREF falls below 4.65V. When a Fault is detected OUT is disabled. When VREF exceeds 4.80V, the Fault condition clears, and OUT is enabled.

### Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage.  $V_{DD}$  should be bypassed directly to GND with good high frequency capacitors.

### References

- [1] Ridley, R., "A New Continuous-Time Model for Current Mode Control", IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

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## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
May 23, 2024	4.00	Updated ordering information table. Added COMP Sink Current and COMP Source Current typical values in the EC tables. Updated POD M8.15 to the latest version. Updated POD M8.118 to the latest version. Added Revision History section.

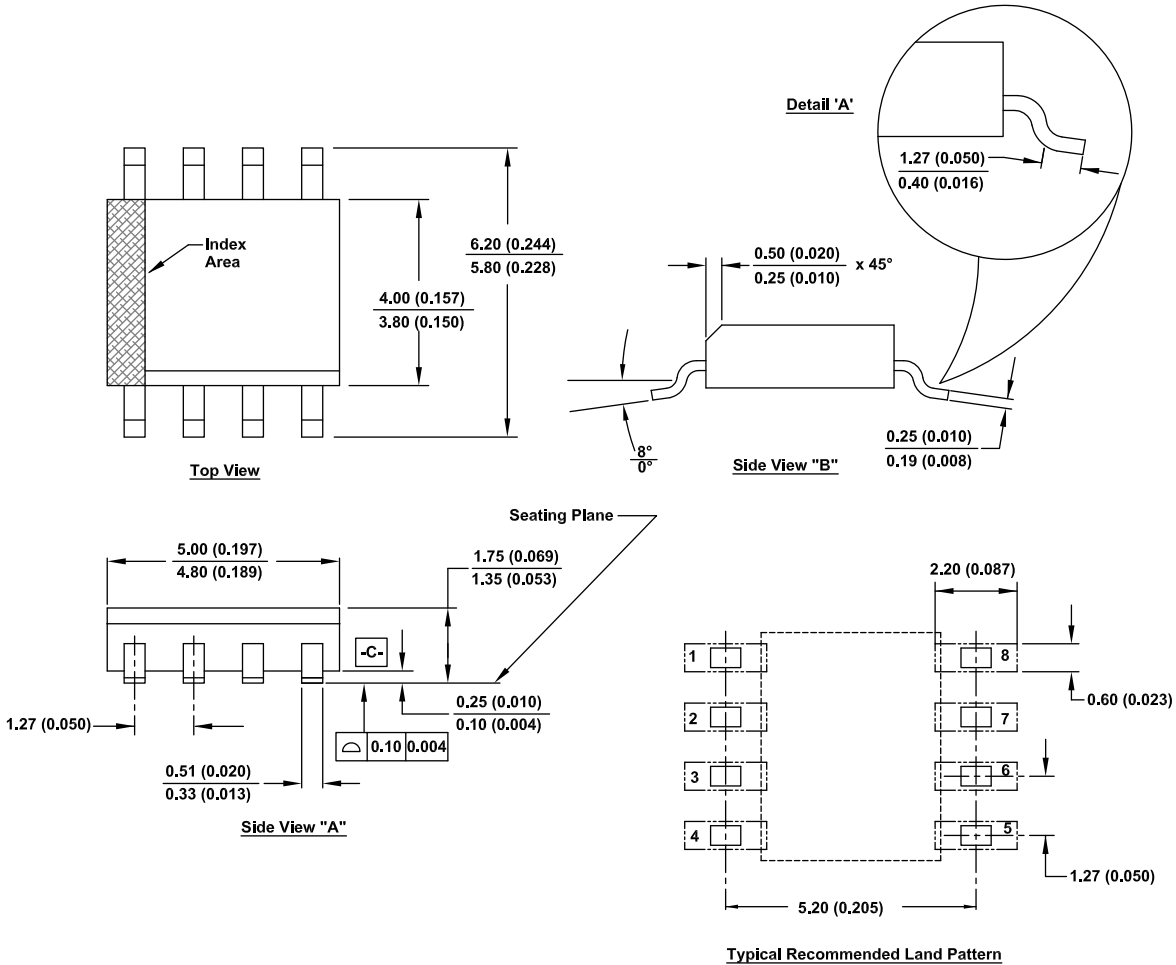
## Package Outline Drawings

For the most recent package outline drawing, see [M8.15](#).

M8.15

8 Lead Narrow Body Small Outline Plastic Package

Rev 7, 9/2023

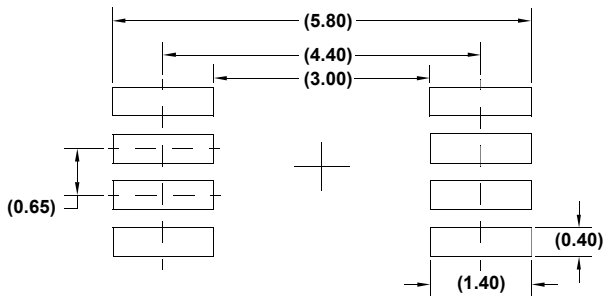
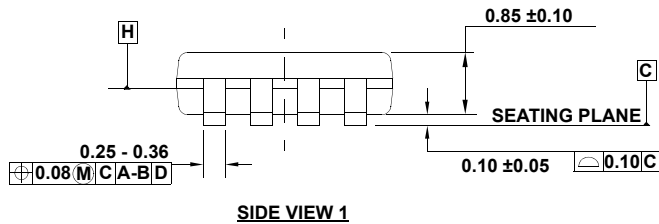
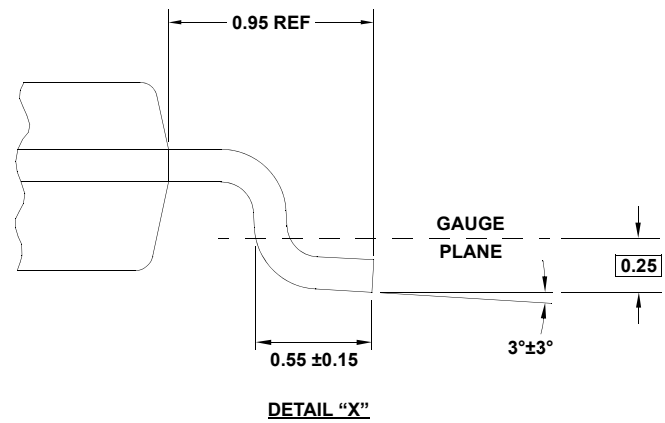
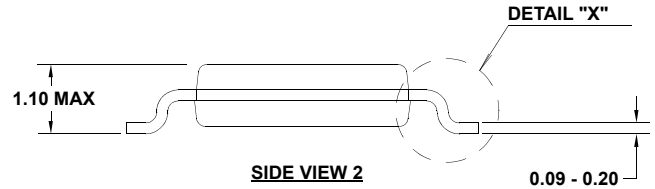
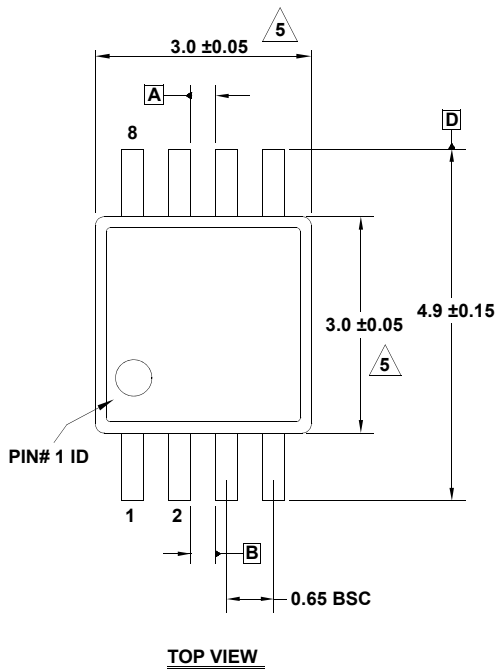


### Notes:

1. Dimension long and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

For the most recent package outline drawing, see [M8.118](#).

M8.118  
 8 Lead Mini Small Outline Plastic Package  
 Rev 5, 5/2021



**NOTES:**

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

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