THE DATASHEET OF

LTC3877IUK#TRPBF

Dual Phase Step-Down Synchronous Controller with VID Output Voltage Programming and Low Value DCR Sensing

FEATURES

- **6-Bit Parallel VID (Voltage Identification) Inputs Set Output Voltage from 0.6V to 1.23V in 10mV Steps**
- **Output Voltage Range: 0.6V to 5V (Without VID)**
- **Ultra Low Value DCR/R_{SENSE} Current Sensing**
- **±1% Maximum Total Regulation Voltage Accuracy Over Temperature**
- **Dual Differential Remote Sensing Amplifiers**
- **$t_{ON(MIN)}$ = 40ns, Capable of Very Low Duty Cycles at High Frequency**
- **Phase-Lockable Frequency from 250kHz to 1MHz**
- **Current Mismatch Between Channels: 5% Max**
- Adjustable Soft-Start Current Ramping or Tracking
- Multi-IC Operation Up To 12 Phases
- Wide V_{IN} Range: 4.5V to 38V
- Dual Power Good Output Voltage Monitors
- Output Overvoltage Protection
- Foldback Output Current Limiting and Soft Recovery

APPLICATIONS

- FPGAs and Processor Power
- Servers and Computing

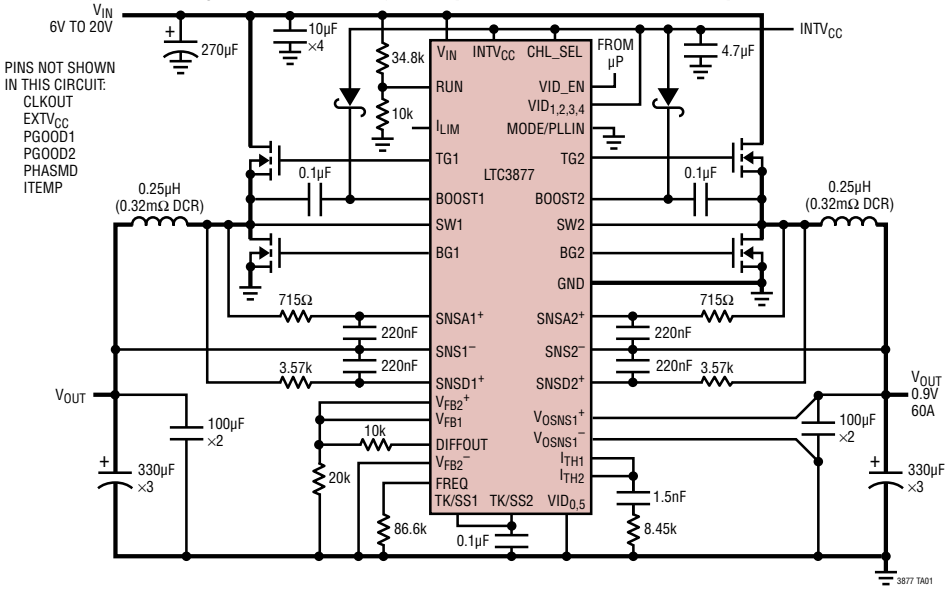
DESCRIPTION

The LTC®3877 is a VID-programmable, constant frequency current mode step-down controller using an advanced and proprietary architecture. This new architecture enhances the signal-to-noise ratio of the current sense signal, allowing the use of very low DC resistance power inductors to maximize efficiency in high current applications. This feature also dramatically reduces the current sensing error, so that current sharing is greatly improved in multi-phase low DCR applications. In addition, the controller achieves a minimum on-time of just 40ns, permitting the use of high switching frequency at high step-down ratios.

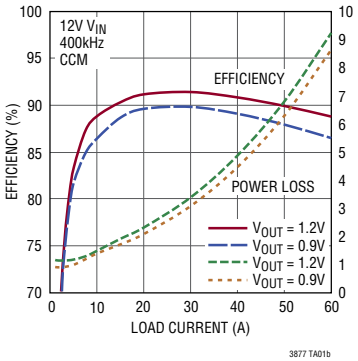
The LTC3877 features dual high speed remote sense differential amplifiers, programmable current sense limits and DCR temperature compensation to limit the maximum output current precisely over temperature. The LTC3877 also features a precise 0.6V reference with guaranteed accuracy of ±0.5%. The LTC3877 is available in a low profile 44-lead 7mm × 7mm QFN package.

TYPICAL APPLICATION

High Efficiency Dual Phase Single Output, 400kHz, 0.9V/60A Step-Down Converter



Efficiency and Power Loss vs Load Current

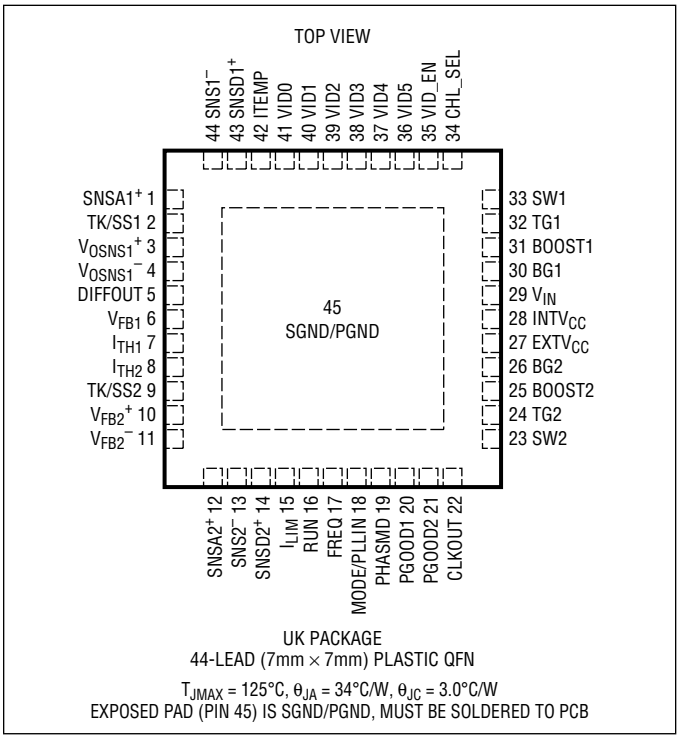


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 40V
Topside Driver Voltages
(BOOST1, BOOST2) ..... –0.3V to 46V
Switch Voltages (SW1, SW2) ..... –5V to 40V
$SNSA1^+$, $SNSD1^+$, $SNS1^-$, $SNSA2^+$, $SNSD2^+$,
$SNS2^-$ Voltages ..... –0.3V to $INTV_{CC}$
(BOOST1-SW1), (BOOST2-SW2) Voltages ... –0.3V to 6V
RUN Voltage ..... –0.3 to 9V
PGOOD1, PGOOD2,
$EXTV_{CC}$ Voltages ..... –0.3V to 6V
MODE/PLLIN, FREQ, PHASMD Voltages ... –0.3V to $INTV_{CC}$
CHL_SEL, VID(s), VID_EN Voltages ..... –0.3V to $INTV_{CC}$
TK/SS1, TK/SS2 Voltages ..... –0.3V to $INTV_{CC}$
I_{TH1}, I_{TH2}, ITEMP, I_{LIM} Voltages ..... –0.3V to $INTV_{CC}$
V_{FB1}, V_{OSNS1}^+, V_{OSNS1}^-, V_{FB2}^+,
V_{FB2}^- Voltages ..... –0.3V to $INTV_{CC}$
$INTV_{CC}$ Peak Output Current 100mA
Operating Junction Temperature Range
(Note2, Note 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UK PACKAGE
44-LEAD (7mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 3.0°C/W
EXPOSED PAD (PIN 45) IS SGND/PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3877EUK#PBF	LTC3877EUK#TRPBF	LTC3877UK	44-Lead (7mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3877IUK#PBF	LTC3877IUK#TRPBF	LTC3877UK	44-Lead (7mm × 7mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 15V, V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
V_{IN}	Input Voltage Range			4.5		38	V
V_{OUT}	Output Voltage Range When VID Control Disabled	V_{INTVCC} = 5.5V, With Low DCR Sensing (Note 10) Without Low DCR Sensing (Note 9)		 0.6 0.6		 3.5 5	 V V
V_{OUT_VID}	Output Voltage When VID Control Enabled (Diff Amp and Error Amp Included)	(Note 4) I_{TH1} Voltage = 1.2V VID0,1,2,3,4,5 = 0V VID0 = 1V, VID1,2,3,4,5 = 0V VID0,5 = 0V, VID1,2,3,4 = 1V VID1,2,3,4 = 0V, VID0,5 = 1V VID0,1,2,3,4,5 = 1V	 ● ● ● ● ●	 594 604 891 921 1.218	 600 610 900 930 1.23	 606 616 909 939 1.242	 mV mV mV mV V
I_Q	Input DC Supply Current Normal Operation Shutdown	(Note 5) V_{IN} = 15V, V_{RUN} = 5V, No Switching, $EXTV_{CC}$ Float V_{RUN} = 0V			 7.3 33	 10 50	 mA µA
UVLO	Undervoltage Lockout Threshold	V_{INTVCC} Ramping Down		3.6	3.8	4.1	V
$UVLO_{HYS}$	UVLO Hysteresis				0.5		V
V_{FB2}^+	Regulated V_{OUT} Feedback Voltage Including Diffamp Error (Channel 2)	(Note 4), I_{TH2} Voltage = 1.2V (–40°C to 85°C) (Note 4), I_{TH2} Voltage = 1.2V (–40°C to 125°C)	 ●	597 595.5	600 600	603 604.5	mV mV
I_{FB1}	Channel 1 Feedback Current	(Note 4)			2	20	nA
I_{FB2}^+	Channel 2 Feedback Current	(Note 4)			40	100	nA
DF_{MAX}	Maximum Duty Cycle	In Dropout, f_{OSC} = 625kHz	●	94	96		%
V_{OVL}	Feedback Overvoltage Lockout	Measured at V_{FB1}, V_{FB2}^+		650	670	690	mV
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 4.5V to 38V (Note 4)			0.002	0.01	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) In Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V In Servo Loop; ΔI_{TH} Voltage = 1.2V to 1.6V	 ● ●		 0.01 –0.01	 0.1 –0.1	 % %
$g_{m1,2}$	EA Transconductance	$I_{TH1,2}$ Voltage = 1.2V; Sink/Source 5µA (Note 4)			2.5		mmho
I_{TEMP}	DCR Temp. Compensation Current	V_{ITEMP} = 0.5V		29	30	31	µA
t_{SSINT}	Internal Soft Start Time	$V_{TK/SS}$ = 5V (Note 8)			600		µs
$I_{TK/SS1,2}$	Soft Start Charge Current	$V_{TK/SS}$ = 0V	●	1.0	1.25	1.5	µA
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising	●	1.1	1.22	1.35	V
V_{RUN} HYS	RUN Pin ON Hysteresis				80		mV
I_{RUN} HYS	RUN Pin Current Hysteresis				4.5		µA
Current Sensing							
I_{SNSA}^+	AC Sense Pin Bias Current	V_{SNSAn}^+ = 1V	●		55	120	nA
I_{SNSD}^+	DC Sense Pin Bias Current	V_{SNSDn}^+ = 1V	●		30	50	nA
A_{VT_SNS}	Total Sense Gain to Current Comp				5		V/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 15V, V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{SENSE(MAX)DC}$	Maximum Current Sense Threshold with Low DCR Sensing (Note 10)	$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 0V		9	10	11	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 1/4 $INTV_{CC}$		14	15	16	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 1/2 $INTV_{CC}$		19	20	21	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 3/4 $INTV_{CC}$		23.5	25	26.5	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = $INTV_{CC}$		28.5	30	31.5	mV
		–40°C to 125°C					
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 0V	●	8.5	10	11.5	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 1/4 $INTV_{CC}$	●	13.5	15	16.5	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 1/2 $INTV_{CC}$	●	17.5	20	22.5	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 3/4 $INTV_{CC}$	●	22	25	28	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = $INTV_{CC}$	●	26.5	30	33.5	mV
$V_{SENSE(MAX)NODC}$	Maximum Current Sense Threshold without Low DCR Sensing (Note 11)	$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 0V	●	45	50	55	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 1/4 $INTV_{CC}$	●	70	75	80	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 1/2 $INTV_{CC}$	●	95	100	105	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = 3/4 $INTV_{CC}$	●	117.5	125	132.5	mV
		$V_{SNS^-(s)}$ = 0.9V, I_{LIM} = $INTV_{CC}$	●	142.5	150	157.5	mV
$I_{MISMATCH}$	Channel-to-Channel Current Mismatch	I_{LIM} = Float				5	%
Differential Amplifier 1							
I_{CL}	Maximum Output Current			3	5		mA
$V_{OUT(MAX)}$	Maximum Output Voltage	$I_{DIFFOUT}$ = 300µA			$INTV_{CC}$ – 1.5V		V
GBW	Gain Bandwidth Product	(Note 8)		3	4.5		MHz
Slew Rate	Differential Amplifier Slew Rate	(Note 8)			2V		V/µs
VID Parameters							
R_{TOP}	VID Top Resistance	(Note 8)			3.33		kΩ
Digital Inputs $VID_{0,1,2,3,4,5}$, VID_EN, CHL_SEL							
V_{IH}	Input High Threshold Voltage			0.7			V
V_{IL}	Input Low Threshold Voltage					0.3	V
Rpd	Pin Pull-down Resistor				100		kΩ
Gate Drivers							
TG $R_{UP1,2}$	TG Pull-Up $R_{DS(ON)}$	TG High			2.6		Ω
TG $R_{DOWN1,2}$	TG Pull-Down $R_{DS(ON)}$	TG Low			1.5		Ω
BG $R_{UP1,2}$	BG Pull-Up $R_{DS(ON)}$	BG High			2.4		Ω
BG $R_{DOWN1,2}$	BG Pull-Down $R_{DS(ON)}$	BG Low			1.1		Ω
	TG Transition Time	(Notes 6, 8)					
$TG_{1,2}$ t_r	Rise Time	C_{LOAD} = 3300pF			25		ns
$TG_{1,2}$ t_f	Fall Time	C_{LOAD} = 3300pF			25		ns
	BG Transition Time	(Notes 6, 8)					
$BG_{1,2}$ t_r	Rise Time	C_{LOAD} = 3300pF			25		ns
$BG_{1,2}$ t_f	Fall Time	C_{LOAD} = 3300pF			25		ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay	C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay	C_{LOAD} = 3300pF Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			40		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 15V, V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal LDO Output Voltage	6V < V_{IN} < 38V		5.3	5.5	5.7	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0 to 20mA			0.5	2.0	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Rising	●	4.5	4.7		V
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5.5V			40	100	mV
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				300		mV
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.22V		575	625	675	kHz
f_{RANGE}	PLL SYNC Range		●	250		1000	kHz
V_{SYNC}	MODE/PLLIN Sync Input Threshold	V_{SYNC} Rising V_{SYNC} Falling			1.6 1		V V
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				250		kΩ
I_{FREQ}	Frequency Setting Current	V_{FREQ} = 1.2V		9	10	11	µA
V_{CLKOUT}	High Output Voltage Low Output Voltage	V_{INTVCC} = 5.5V		4	5.5 0	 0.2	V V
$\Phi_2 - \Phi_1$	Channel 2 to Channel 1 Phase Delay	V_{PHSMD} = 0V V_{PHSMD} = Float V_{PHSMD} = $INTV_{CC}$			180 180 240		Deg Deg Deg
$\Phi_{CLKOUT} - \Phi_1$	CLKOUT to Channel 1 Phase Delay	V_{PHSMD} = 0V V_{PHSMD} = Float V_{PHSMD} = $INTV_{CC}$			60 90 120		Deg Deg Deg
Power Good Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5.5V				2	µA
V_{PG}	PGOOD Trip Level	V_{FB1}, V_{FB2}^+ with Respect to Set Output Voltage V_{FB1}, V_{FB2}^+ Ramping Up V_{FB1}, V_{FB2}^+ Ramping Down			 10 –10		 % %
T_{DELAY}	V_{PGOOD} High to Low Delay Time				50		µs
T_{BLANK}	PGOOD Bad Blanking Time	Measure from VID Transition Edge			235		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation PD according to the following formula: $T_J = T_A + (P_D \bullet 34°C/W)$.

Note 3: The LTC3877 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3877E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3877I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 4: The LTC3877 is tested in a feedback loop that servos $V_{ITH1,2}$ to a specified voltage and measures the resultant V_{OSNS1}^+, V_{FB2}^+.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

Note 8: Guaranteed by design.

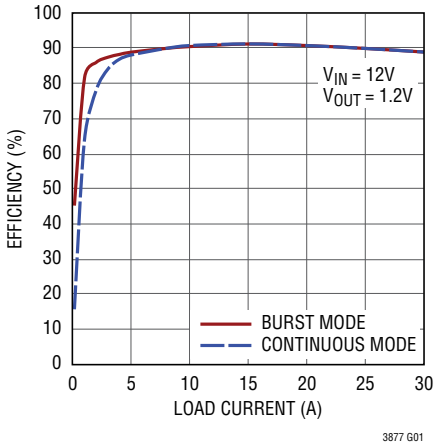
Note 9: Both VID_EN and $SNSD^+$ pins to GND. In order to obtain 5V at the output of Channel 1, the V_{OSNS1}^+ pin must be connected to the mid-point of an external resistor divider, and the V_{FB1} pin must be shorted to the DIFFOUT pin.

Note 10: $SNSD^+$ pin to V_{OUT}.

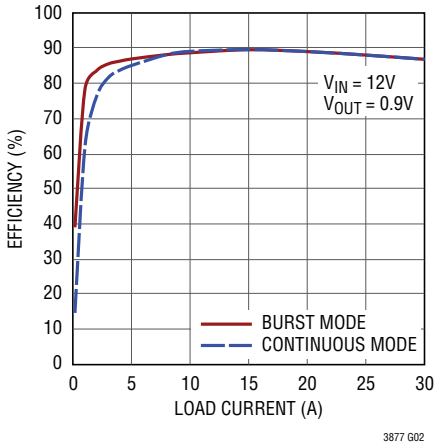
Note 11: $SNSD^+$ pin to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

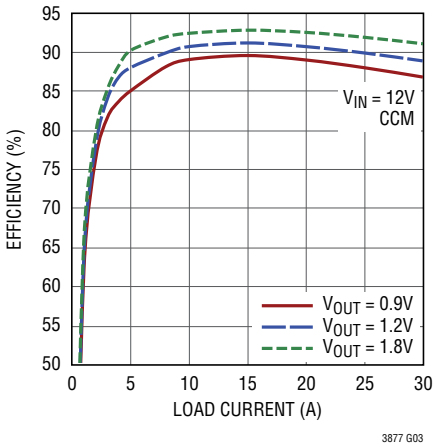
Efficiency vs Output Current and Mode (Circuit on Last Page)



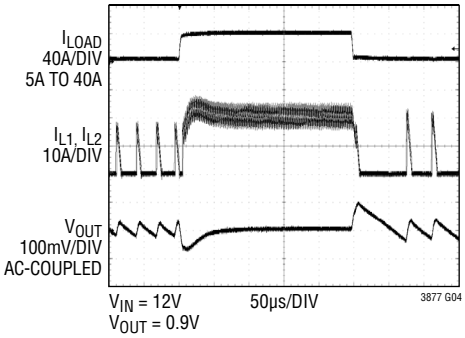
Efficiency vs Output Current and Mode (Circuit on Last Page)



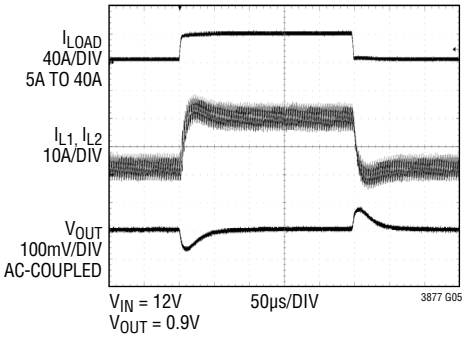
Efficiency vs Output Current and Voltage



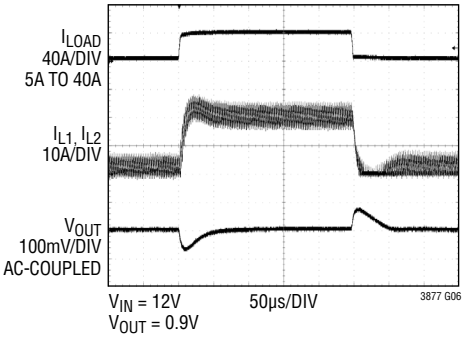
Load Step (Figure 16 Application Circuit) (Burst Mode Operation)



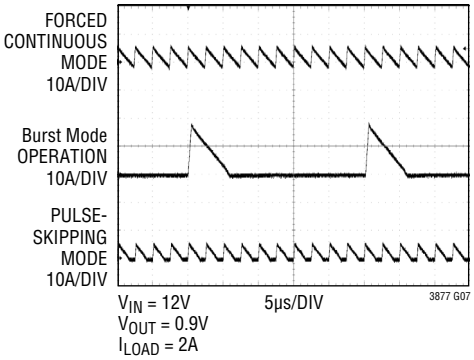
Load Step (Figure 16 Application Circuit) (Forced Continuous Mode)



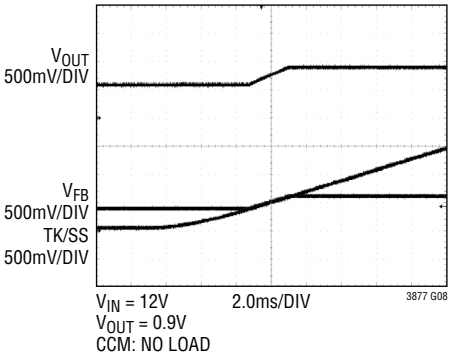
Load Step (Figure 16 Application Circuit) (Pulse-Skipping Mode)



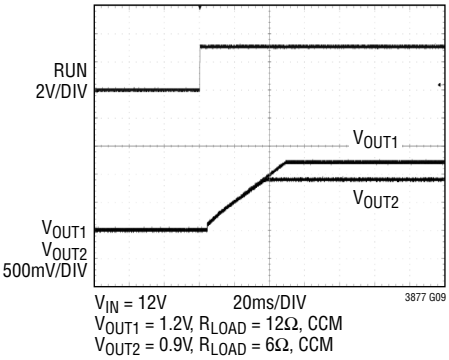
Inductor Current at Light Load



Prebiased Output at 0.6V

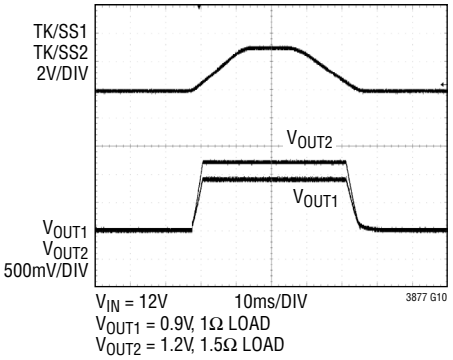


Coincident Tracking

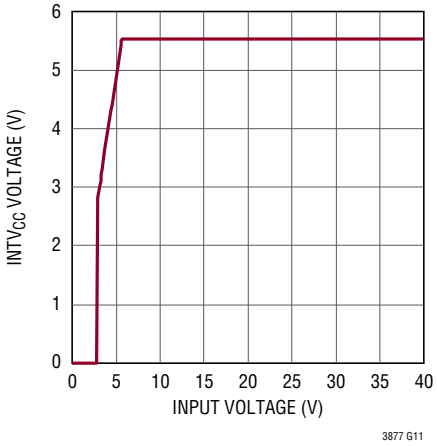


TYPICAL PERFORMANCE CHARACTERISTICS

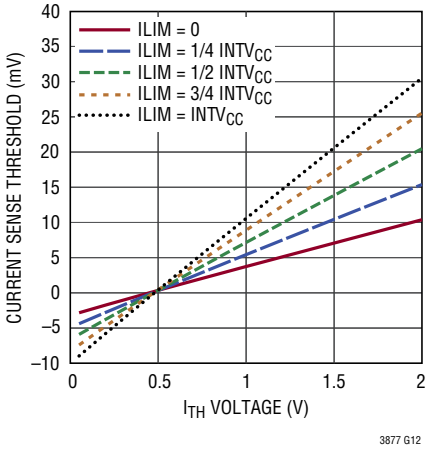
Tracking Up and Down with External Ramp



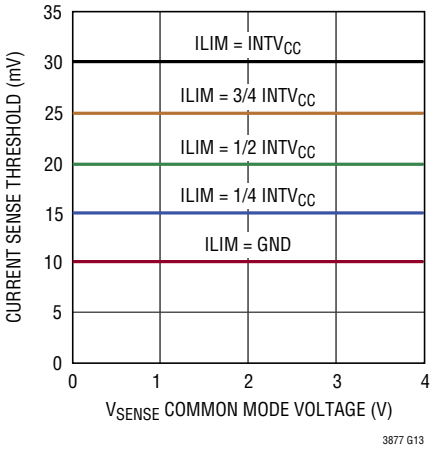
$INTV_{CC}$ Line Regulation



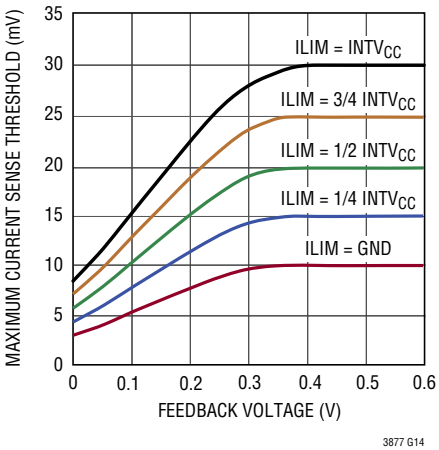
Current Sense Threshold vs I_{TH} Voltage



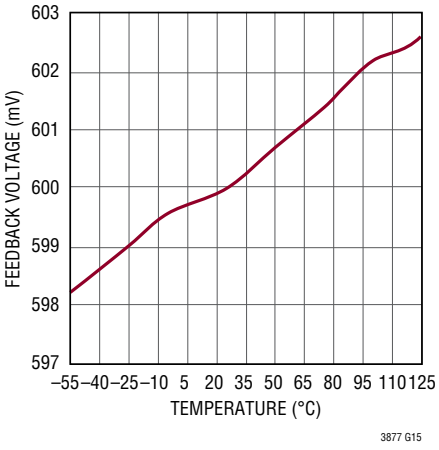
Maximum Current Sense Threshold vs Common Mode Voltage



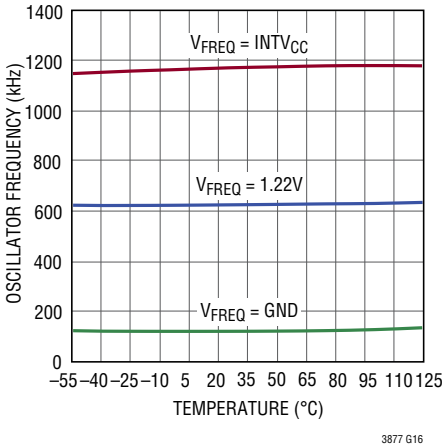
Maximum Current Sense Threshold vs Feedback Voltage (Current Foldback)



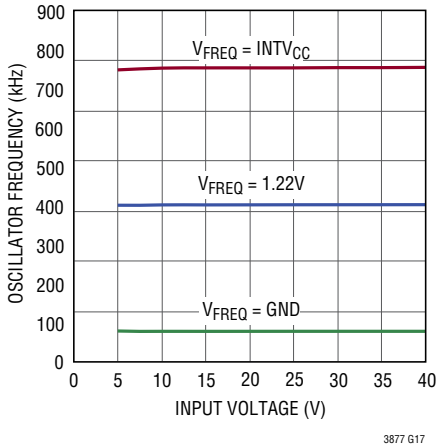
Regulated Feedback Voltage vs Temperature



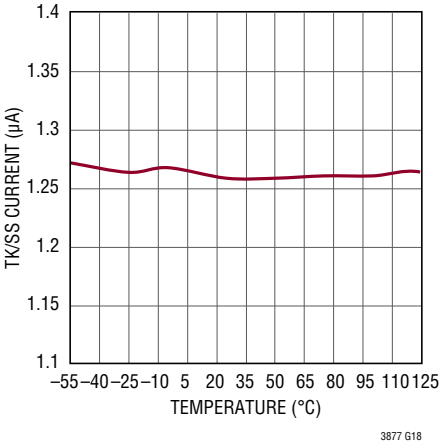
Oscillator Frequency vs Temperature



Oscillator Frequency vs Input Voltage

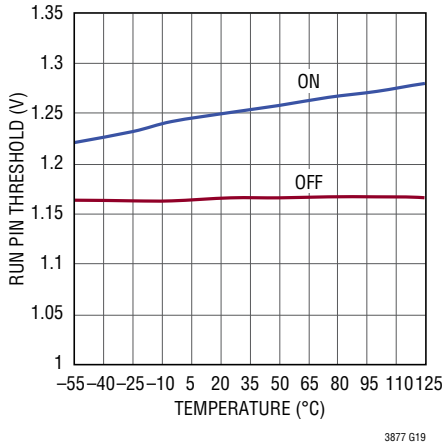


TK/SS Pull-Up Current vs Temperature

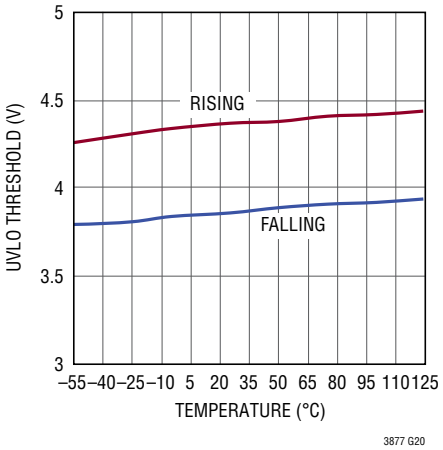


TYPICAL PERFORMANCE CHARACTERISTICS

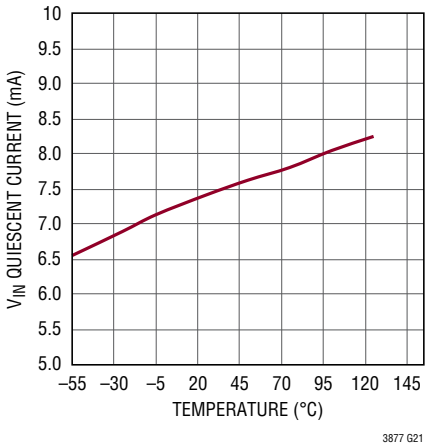
Shutdown (RUN) Threshold vs Temperature



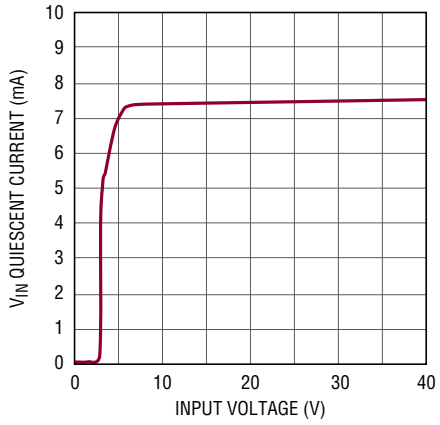
Undervoltage Lockout Threshold ($INTV_{CC}$) vs Temperature



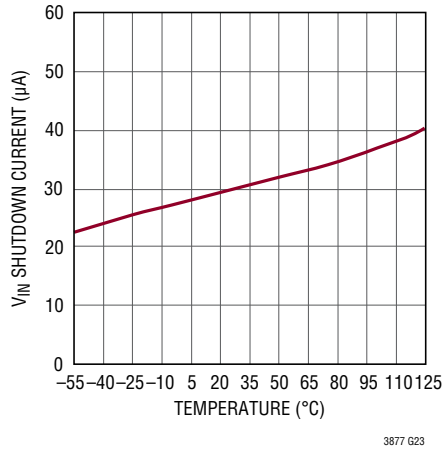
Quiescent Current vs Temperature without $EXTV_{CC}$



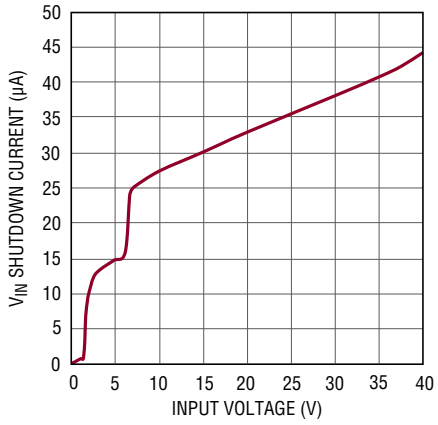
Quiescent Current vs Input Voltage without $EXTV_{CC}$



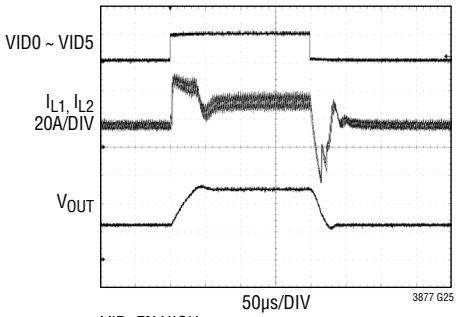
Shutdown Current vs Temperature



Shutdown Current vs Input Voltage

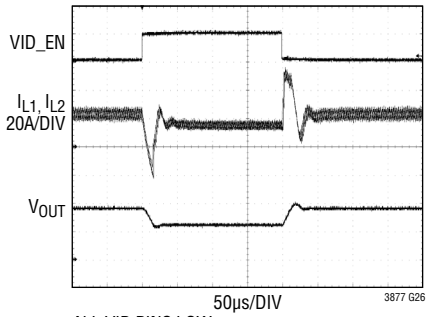


VID Transient (Figure 16 Application Circuit)



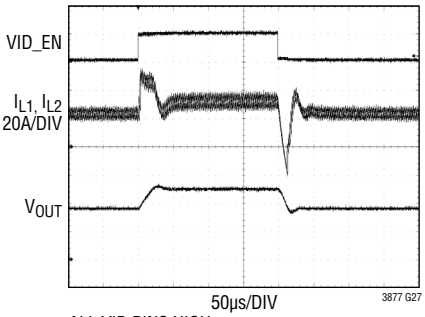
VID_EN HIGH
CCM, 40mΩ LOAD
V_{OUT} = 0.6V TO 1.23V TO 0.6V

VID_EN Transient with All VID Pins Low (Figure 16 Application Circuit)



ALL VID PINS LOW
CCM, 40mΩ LOAD
V_{OUT} = 0.9V TO 0.6V TO 0.9V

VID_EN Transient with All VID Pins High (Figure 16 Application Circuit)



ALL VID PINS HIGH
CCM, 40mΩ LOAD
V_{OUT} = 0.9V TO 1.23V TO 0.9V

PIN FUNCTIONS

RUN (Pin 16): Run Control Input. A voltage above 1.22V on this pin turns on the IC. However, forcing this pin below 1.14V causes the IC to shut down. There is a 1.0µA pull-up current for this pin. Once the Run pin rises above 1.22V, an additional 4.5µA pull-up current is added to the pin. It is highly recommended to have a resistor divider from V_{IN} to SGND, and connect the center tap to RUN pin in order not to turn on the IC until V_{IN} is high enough.

VID0, VID1, VID2, VID3, VID4, VID5 (Pin 41, Pin 40, Pin 39, Pin 38, Pin 37, Pin 36): Digital VID Inputs for Output Voltage Programming. There are internal 100kΩ pull-down resistors connected to these pins respectively.

VID_EN (Pin 35): VID Enable Pin. When this pin is asserted, channel 1's output will be programmed by the VID inputs after startup is complete. If the LTC3877 is configured as a dual-phase single-output controller with the CHL_SEL pin high, its output will be programmed through the VID pins after VID_EN is asserted. Before VID_EN is asserted, channel 1's output is set by an external resistor divider. There is an internal 100kΩ pull-down resistor connected to this pin.

CHL_SEL (Pin 34): Channel Configuration Pin. When this pin is asserted, the two channels are configured as a dual-phase single-output regulator, and the output voltage can be programmed by VID inputs if VID_EN is asserted. When this pin is grounded, the two channels operate independently. Channel 1's output can be programmed by VID inputs if VID_EN is high, but Channel 2's output must be set by an external resistor divider. There is an internal 100kΩ pull-down resistor connected to this pin.

V_{OSNS1}^+ (Pin 3): Positive Input of Channel 1 Remote Sensing Differential Amplifier. Connect this pin to the remote load voltage directly.

V_{OSNS1}^- (Pin 4): Negative Input of Channel 1 Remote Sensing Differential Amplifier. Connect this pin to the negative terminal of the output capacitors near the load.

DIFFOUT (Pin 5): Output of Channel 1 Remote Sensing Differential Amplifier. If remote sensing is used on channel 1, connect this pin to V_{FB1} through a resistor divider.

V_{FB1} (Pin 6): Channel 1 Error Amplifier Feedback input. This pin receives the remotely sensed feedback voltage from the external resistive divider across the output. The error amp of channel 1 is disconnected from this pin when VID_EN is asserted.

V_{FB2}^+ (Pin 10): Positive Input of Channel 2 Remote Sensing Differential Amplifier. This pin receives the remotely sensed feedback voltage from an external resistive divider across the output. The Differential Amplifier output is connected directly to the Error Amplifier's input inside the IC.

V_{FB2}^- (Pin 11): Negative Input of Channel 2 Remote Sensing Differential Amplifier. Connect this pin to the negative terminal of the output capacitors near the load when remote sensing is desired.

SNSA1+, SNSA2+ (Pin 1, Pin 12): Positive Terminals of the AC Current Sense Comparator Inputs. The (+) input to the AC current comparator is normally connected to a DCR sensing network. When the respective channel's $SNSD^+$ pin is connected to this network, the channel's AC ripple voltage seen by the IC is effectively increased by a factor of 5.

SNSD1+, SNSD2+ (Pin 43, Pin 14): Positive Terminals of the DC Current Sense Comparator Inputs. The (+) input to the DC current comparator is normally connected to a DC current sensing network. When this pin is grounded, the respective phase's current limit is increased by a factor of 5.

SNS1–, SNS2– (Pin 44, Pin 13): Negative Terminals of the AC and DC Current Sense Comparator Inputs. The (–) inputs to the current comparators are connected to the output at the inductor (or current sense resistor, if one is used).

I_{LIM} (Pin 15): Current Comparators' Sense Voltage Range Input. A DC voltage applied to this pin programs the maximum current sense threshold to one of five different levels for the current comparators.

ITH1, ITH2 (Pin 7, Pin 8): Current Control Threshold and Error Amplifier Compensation Points. The current comparators' tripping thresholds increase with these control voltages.

PIN FUNCTIONS

TK/SS1, TK/SS2 (Pin 2, Pin 9): Output Voltage Tracking and Soft Start Inputs. When one channel is configured to be the master, a capacitor to ground at this pin sets the ramp rate for the master channel's output voltage. When the channel is configured to be the slave, the feedback voltage of the master channel is reproduced by a resistor divider and applied to this pin. Internal soft start currents of 1.25µA charge these pins.

ITEMP (Pin 42): Input to the Temperature Sensing Comparator. This pin can be programmed to compensate the temperature coefficient of the inductor DCR. When CHL_SEL is asserted, the voltage on this pin can be used to compensate both channels temperature. When CHL_SEL is grounded, the voltage on this pin only compensates channel 1's current limit for temperature. Connect this pin to an external NTC resistor network placed near the appropriate inductors. Floating this pin disables the DCR temperature compensation function.

PGOOD1, PGOOD2 (Pin 20, Pin 21): Power Good Indicator Output for Each Channel. Open drain logic that is pulled to ground when the respective channel's output exceeds its ±10% regulation window, after the internal 50µs power bad mask timer expires. During a VID transition, PGOOD is blanked for 235µs.

MODE/PLLIN (Pin 18): Force Continuous Mode, Burst Mode or Pulse Skip Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force the IC into continuous mode of operation. Connect to $INTV_{CC}$ to enable pulse skip mode of operation. Leave the pin floating to enable Burst Mode operation. A clock on the pin will force the IC into continuous mode of operation and synchronize the internal oscillator with the clock on this pin. The PLL compensation network is integrated into the IC.

FREQ (Pin 17): Oscillator Frequency Control Input. There is a precision 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

PHASMD (Pin 19): Phase Program Pin. This pin can be tied to SGND, $INTV_{CC}$ or left floating. It determines the relative phases between the internal controllers as well as the phasing of the CLKOUT signal. See Table 1 in the Operation section for detail.

CLKOUT (Pin 22): Clock Output Pin. Clock output with phase changeable by PHASMD to enable usage of multiple LTC3877s in PolyPhase systems. Signal swing is from $INTV_{CC}$ to ground.

BOOST1, BOOST2 (Pin 31, Pin 25): Boosted Floating Driver Supplies. The (+) terminal of the bootstrap capacitors connect to these pins. These pins swing from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

TG1, TG2 (Pin 32, Pin 24): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage.

SW1, SW2 (Pin 33, Pin 23): Switch Node Connections to Inductors. Voltage swings at these pins are from a Schottky diode (external) voltage drop below ground to V_{IN}.

BG1, BG2 (Pin 30, Pin 26): Bottom Gate Driver Outputs. These pins drive the gates of the bottom N-Channel MOSFETs between PGND and $INTV_{CC}$.

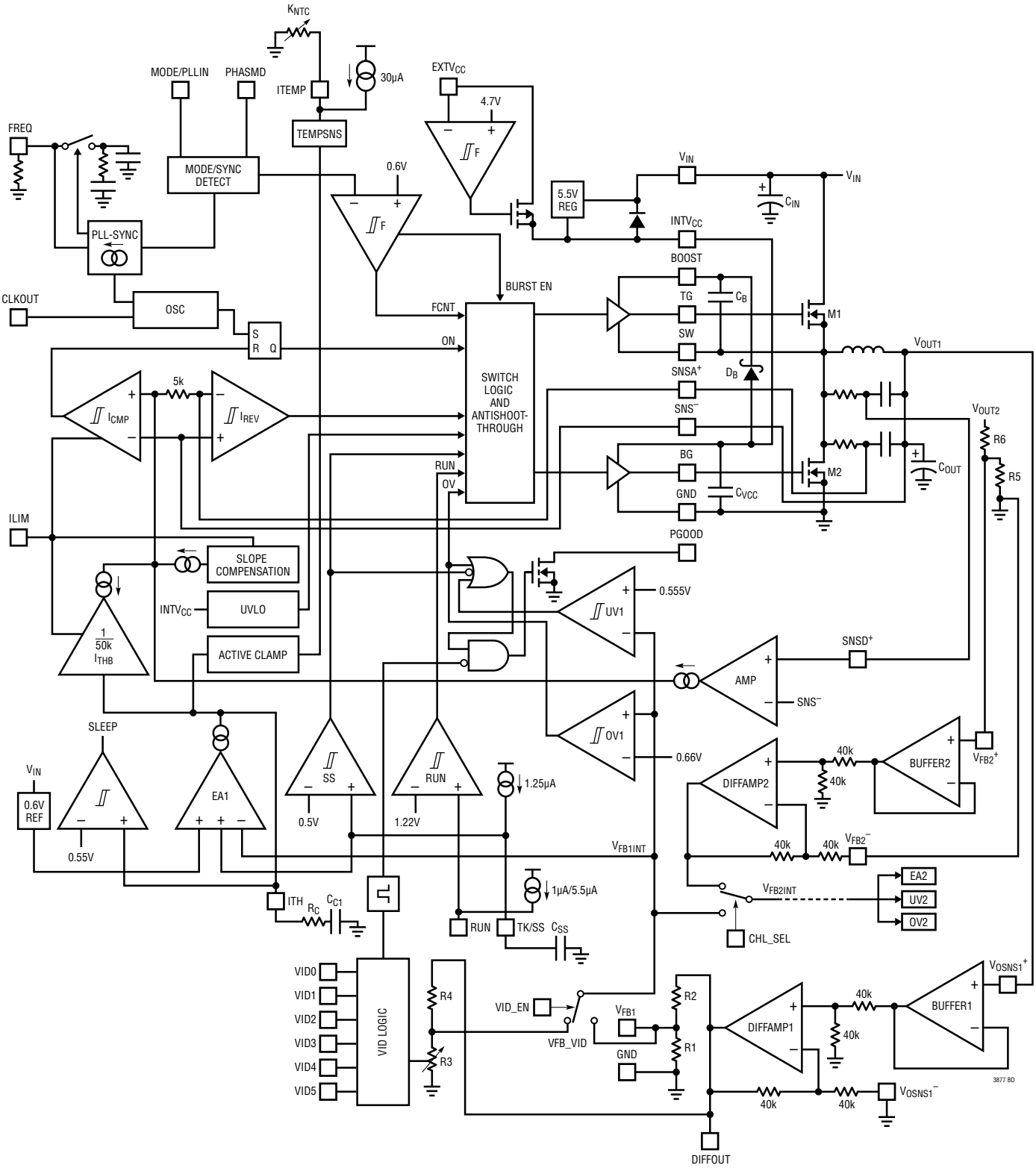
V_{IN} (Pin 29): Main Input Supply. Bypass this pin to PGND with a capacitor (0.1µF to 1µF).

$INTV_{CC}$ (Pin 28): Internal 5.5V Regulator Output. The control circuits are powered from this voltage. Bypass this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

$EXTV_{CC}$ (Pin 27): External Power Input to Internal Switch Connected to $INTV_{CC}$. The internal switch closes and supplies the IC power, bypassing the internal low dropout regulator, whenever $EXTV_{CC}$ is higher than 4.7V. Do not exceed 6V on this pin.

SGND/PGND (Exposed Pad Pin 45): Signal/Power Ground Pin. Connect this pin closely to the sources of the bottom N-channel MOSFETs and the negative terminals of the V_{IN} and $INTV_{CC}$ bypassing capacitors. All small-signal components and compensation components should also connect to this ground.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3877 is a constant frequency, current mode, step-down controller with both channels operating 180° or 240° out-of-phase. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the ITH pin, which is the output of each error amplifier EA. The remote sense amplifier (DIFFAMP) converts the sensed differential voltage across the output (or output feedback resistor divider, depending on the mode of operation) to an internal voltage referred to SGND. This feedback signal is then compared to the internal 0.6V reference voltage by the EA. When the load current increases, it causes a slight decrease in the feedback relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the reverse current comparator I_{REV}, or the beginning of the next cycle.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.5V, an internal 5.5V linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 4.7V, the 5.5V regulator is turned off and an internal switch is turned on, allowing $EXTV_{CC}$ to power the IC. When using $EXTV_{CC}$, the V_{IN} voltage has to be higher than $EXTV_{CC}$ voltage at all times and has to come before $EXTV_{CC}$ is applied. Otherwise, $EXTV_{CC}$ current will flow back to V_{IN} through the internal switch's body diode and potentially damage the device. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source.

Each top MOSFET driver is biased from its floating bootstrap capacitor C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 100ns every third cycle to allow C_B to recharge. However, it is recommended that a load be present or the IC operates at low frequency during the drop-out transition to ensure that C_B is recharged.

Channel Selection (CHL_SEL Pin)

The LTC3877 has two alternative configurations, which can be selected by the CHL_SEL pin. When CHL_SEL is asserted, the controller enters the dual phase single output configuration. Channel 1 becomes the master channel while Channel 2's Differential Amplifier (DIFFAMP2) and Error Amplifier (EA2) are disabled. The two channels share Channel 1's Error Amplifier (EA1) and the feedback voltages of the two channels are shorted internally. Also, an internal circuit allows the inductor's DCR temperature compensation to be shared between the two channels. If VID_EN is asserted also, the output can be programmed by 6-bit Voltage Identification (VID) inputs. Otherwise, the output is set by the external resistor divider connected to the V_{FB1} pin.

If CHL_SEL pin is grounded, the two channels operate independently. Channel 2's output is set by an external resistor divider between the V_{FB2}^+ and $V_{FB2}–$ pins. Channel 1's output is programmed by the VID inputs if VID_EN pin is HIGH, or set by an external resistor divider on the V_{FB1} pin if VID_EN is grounded.

There is an internal 100k pull-down resistor connected to the CHL_SEL pin. It is recommended to ground this pin instead of floating it if logic low state is desired. The logic low threshold of the CHL_SEL pin is 0.3V; the logic high threshold is 0.7V.

Output Voltage Programming (VID0~VID5 Pins) and VID Mode (VID_EN Pin)

The LTC3877 output voltage can be programmed by either an internal Voltage Identification (VID) resistor bank or an external resistor divider, depending on the state of the VID_EN pin. Before VID_EN is driven HIGH, the output voltage is set by an external resistor divider connected to

OPERATION

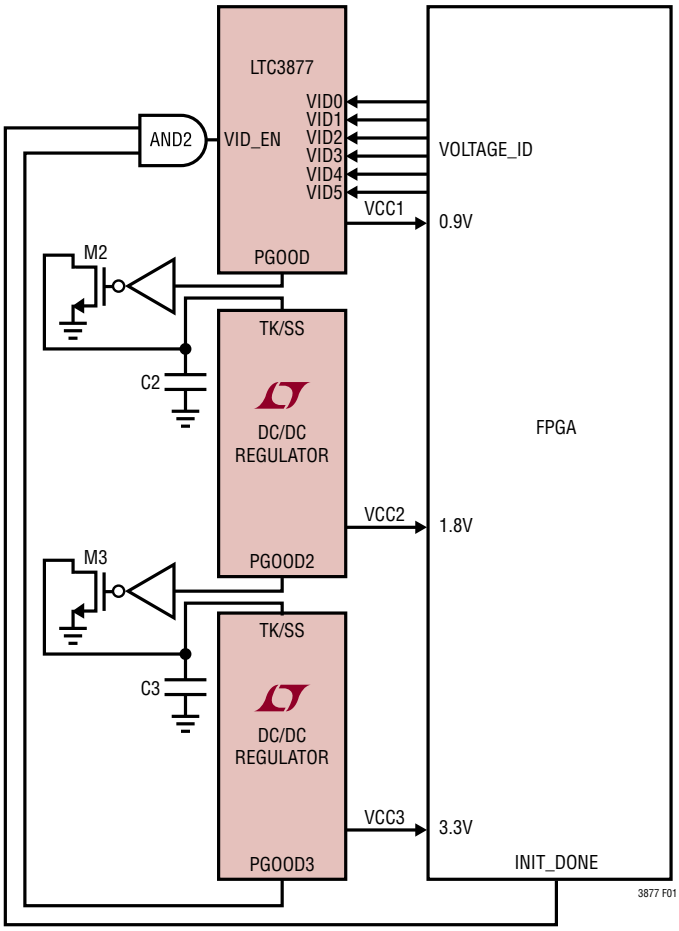


Figure 1. Suggested FPGA VID Regulator Diagram

the V_{FB1} pin. Once VID_EN goes to HIGH, the voltage on the V_{FB1} pin is ignored, and the output voltage is digitally programmed by 6-bit parallel VID inputs, which command output voltages from 0.6V to 1.23V in 10mV steps. When the CHL_SEL pin is grounded, the VID mode is only available for Channel 1. When CHL_SEL is asserted, the VID mode is available for both channels. There are internal 100k pull-down resistors connected to all VID input pins and the VID_EN pin. It is recommended to ground these pins instead of floating them if logic low state is desired. The logic low threshold of the VID and VID_EN pins is 0.3V; the logic high threshold is 0.7V.

Figure 1 is a conceptual example of the LTC3877 supplying power for an FPGA. First, LTC3877 starts up. Its output voltage is set by an external resistor divider to an initial voltage, such as 0.9V. When the LTC3877 startup is complete, its Power Good (PGOOD) pin will go HIGH and turn on the second DC/DC regulator in sequence. The second regulator may or may not be an LTC3877. When its output voltage is ready, its Power Good signal (PGOOD2) will trigger the third regulator, and so on, until all the regulators are powered up. The last one will send out a Ready signal, such as PGOOD3. Then, the FPGA will initialize and send out its own Ready signal (INIT_DONE). When these two Ready signals are asserted, the external AND gate drives the VID_EN pin of LTC3877 HIGH. At that time, the LTC3877 will regulate its output voltage according to the VID inputs coming from the FPGA. The VID signals can be sent to LTC3877 before or after VID_EN is asserted. Before VID_EN is High, the VID inputs are ignored.

Shutdown and Start-Up (RUN and TK/SS1, TK/SS2 Pins)

The LTC3877 can be shut down using the RUN pin. Pulling the RUN pin below 1.14V disables both channels and most internal circuits, including the $INTV_{CC}$ regulator. Releasing RUN allows an internal 1µA current to pull up the pin and enable the controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the Absolute Maximum Rating of 6V on this pin.

The start-up of each channel's output voltage V_{OUT} is controlled by the voltage on its TK/SS pin. When the voltage on the TK/SS pin is less than the 0.6V internal reference, the LTC3877 regulates the V_{FB} voltage to the TK/SS pin voltage instead of the 0.6V reference. This allows the TK/SS pin to be used to program the soft-start period by connecting an external capacitor from the TK/SS pin to SGND. An internal 1.25µA pull-up current charges this capacitor, creating a voltage ramp on the TK/SS pin. As the TK/SS voltage rises linearly from 0V to 0.6V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. Alternatively the TK/SS pin can be used to cause the start-up of V_{OUT} to "track" that of another supply. Typically, this requires connecting to the TK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section). When the RUN pin is pulled low to disable the controller, or when $INTV_{CC}$ drops below its undervoltage lockout threshold of 3.7V, the TK/SS pins are pulled low by internal MOSFETs. When in undervoltage lockout, both channels are disabled and the external MOSFETs are held off.

OPERATION

Internal Soft-Start

By default, the start-up of the output voltage is normally controlled by an internal soft-start ramp. The internal soft-start ramp represents one of the non-inverting inputs to the error amplifier. The V_{FB} signal is regulated to the lower of the error amplifier's three non-inverting inputs (the internal soft-start ramp, the TK/SS pin or the internal 600mV reference). As the ramp voltage rises from 0V to 0.6V over approximately 600µs, the output voltage rises smoothly from its pre-biased value to its final set value. Certain applications can result in the start-up of the converter into a non-zero load voltage, where residual charge is stored on the output capacitor at the onset of converter switching. In order to prevent the output from discharging under these conditions, the top and bottom MOSFETs are disabled until the soft-start voltage is greater than V_{FB}.

Light Load Current Operation (Burst Mode® Operation, Pulse-Skipping, or Continuous Conduction)

The LTC3877 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode, or forced continuous conduction mode. To select forced continuous operation, tie the MODE/PLLIN pin to a DC voltage below 0.6V (e.g., SGND). To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select Burst Mode operation, float the MODE/PLLIN pin. When a controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-third of the maximum sense voltage even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier EA will decrease the voltage on the ITH pin. When the I_{TH} voltage drops below 0.5V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator. When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (I_{REV}) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the MODE/PLLIN pin is connected to $INTV_{CC}$, the LTC3877 operates in PWM pulse-skipping mode at light loads. At very light loads, the current comparator I_{CMP} may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Differential Sensing of the Output Voltage (V_{OSNS1}^+ Pin, V_{OSNS1}^- Pin, DIFFOUT Pin, V_{FB2}^+ Pin, V_{FB2}^- Pin)

The LTC3877 includes two low offset, high input impedance, high bandwidth differential amplifiers (diffamp) for applications that require true remote sensing. Both of the LTC3877 differential amplifiers have a typical output slew rate of 2V/µs and both of their positive terminals are high impedance. Each amplifier is configured for unity gain, meaning that the difference between the inputs is translated to its output, relative to SGND. Differentially sensing the load greatly benefits regulation in high current, low voltage applications, where board interconnection losses can be a significant portion of the total error budget.

However, the differential amplifiers of the two channels are configured differently. Channel 1's diffamp (DIFFAMP1) has a traditional three terminal arrangement, as shown in Figure 2a. Its positive terminal V_{OSNS1}^+ and negative terminal V_{OSNS1}^- sense directly across the output

OPERATION

capacitor's two terminals. The processed differential signal appears between the DIFFOUT pin and SGND. This is the signal that the internal VID resistor bank uses to program the output voltage. An external resistor divider needs to be connected between DIFFOUT pin and SGND, and its center tap should connect to the V_{FB1} pin to set the output voltage at startup or before the VID_EN pin is asserted. If VID output voltage programming is not desired, Channel 1's diffamp can be configured like that of Channel 2. See Figure 2b. In this configuration, connect the V_{OSNS1}^+ pin to the center tap of the feedback divider across the output load, and short the DIFFOUT and V_{FB1} pins together. When VID_EN and SNSD+ pins are both grounded, the connections in Figure 2b can allow Channel 1's output up to 5V, while the connections in Figure 2a allows Channel 1's output up to 3.5V. Typically, V_{INTVCC} has to be at least 1.5V above the output voltage for the connections in Figure 2a.

The second channel differential amplifier's (DIFFAMP2) positive terminal V_{FB2}^+ senses the divided output through a resistor divider and its negative terminal V_{FB2}^- senses the remote ground of the load as shown in Figure 2c. This Differential Amplifier output is connected to the negative terminal of the internal Error Amplifier inside the controller.

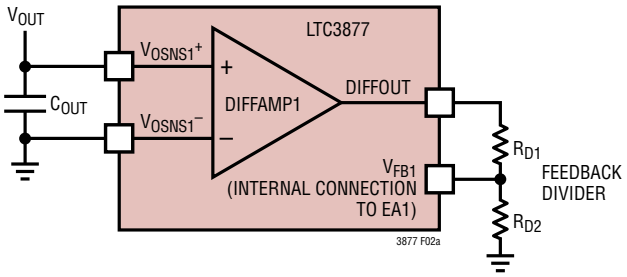


Figure 2a.

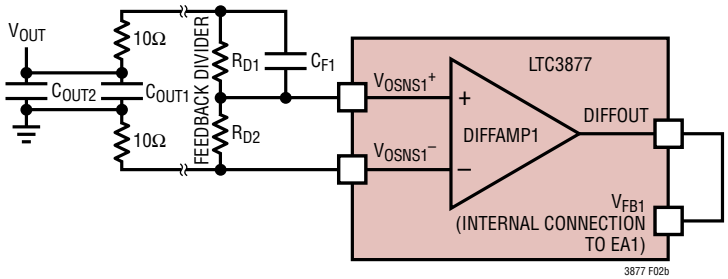


Figure 2b.

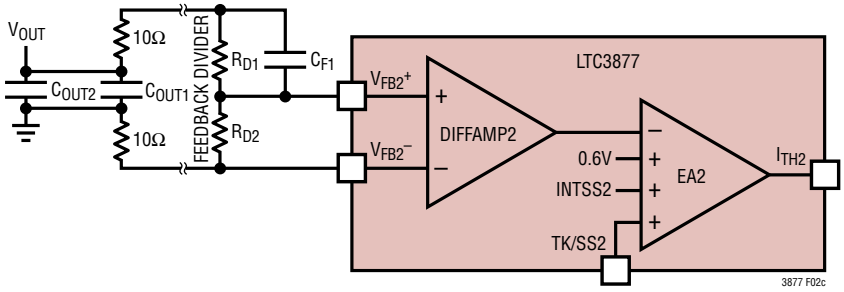


Figure 2c.

Figure 2. Differential Amplifier Connection

OPERATION

Therefore, its differential output signal is not accessible from outside the IC. In a typical application when differential sensing is desired, connect V_{FB2}^+ pin to the center tap of the feedback divider across the output load, and V_{FB2}^- pin to the load ground. When differential sensing is not desired, the V_{FB2}^- pin can be connected to local ground.

When sensing the output voltage remotely, care should be taken to route the V_{OSNS1}^+ and V_{OSNS1}^- PCB traces parallel to each other all the way from the IC to the remote sensing points on the board. Follow the same practice for the V_{FB2}^+ and V_{FB2}^- PCB traces. In addition, avoid routing these sensitive traces near any high speed switching nodes in the circuit. Ideally, these traces should be shielded by a low impedance ground plane to maintain signal integrity.

Current Sensing with Very Low Inductor DCR

For low output voltage, high current applications, it's common to use low winding resistance (DCR) inductors to minimize the winding conduction loss and maximize the supply efficiency. Inductor DCR current sensing is also used to eliminate the current sensing resistor and its conduction loss. Unfortunately, with a very low inductor DCR value, 1mΩ or less, the AC current sensing signal ripple can be less than $10mV_{P-P}$. This makes the current loop sensitive to PCB switching noise and causes switching jitter.

The LTC3877 employs a unique and proprietary current sensing architecture to enhance its signal-to-noise ratio in these situations. This enables it to operate with a small sense signal of a very low value inductor DCR, 1mΩ or less. The result is improved power efficiency, and reduced jitter due to switching noise which could corrupt the signal. The LTC3877 can sense a DCR value as low as 0.2mΩ with careful PCB layout. The LTC3877 uses two positive sense pins, $SNSD^+$ and $SNSA^+$, to acquire signals. It processes them internally to provide the response as with a DCR sense signal that has a 14dB (5×) signal-to-noise ratio improvement, without affecting the output voltage feedback loop, so that its sensing accuracy is also improved by five times. In the meantime, the current limit threshold is still a function of the inductor peak current times its DCR value; its accuracy is also improved five times and can be accurately set from 10mV to 30mV in 5mV steps using the I_{LIM} pin (see Figure 4b for inductor DCR sensing connections). The filter time constant, R1 • C1, of the $SNSD^+$ should match the L/DCR of the output inductor, while the filter at $SNSA^+$ should have a bandwidth of five times larger than that of $SNSD^+$, i.e, R2 • C2 equals one-fifth of R1 • C1.

Inductor DCR Sensing Temperature Compensation (ITEMP Pin)

Inductor DCR current sensing provides a lossless method of sensing the instantaneous current. Therefore, it can provide higher efficiency for applications with high output currents. However, the DCR of a copper inductor typically has a positive temperature coefficient. As the temperature of the inductor rises, its DCR value increases. The current limit of the controller is therefore reduced.

The LTC3877 offers a method to counter this inaccuracy by allowing the user to place an NTC temperature sensing resistor near the inductor. A constant and precise 30µA current flows out of the ITEMP pin. By connecting a linearized NTC resistor network from the ITEMP pin to SGND, the maximum current sense threshold can be varied over temperature according to the following equation:

$$V_{SENSEMAX(ADJ)} = V_{SENSE(MAX)} \bullet \frac{2.2 - V_{ITEMP}}{1.5}$$

Where:

$V_{SENSEMAX(ADJ)}$ is the maximum adjusted current sense threshold.

$V_{SENSE(MAX)}$ is the maximum current sense threshold specified in the Electrical Characteristics table. It is typically 10mV, 15mV, 20mV, 25mV or 30mV, depending on the I_{LIM} pin's voltage.

V_{ITEMP} is the voltage of the ITEMP pin.

The valid voltage range for DCR temperature compensation on the ITEMP pin is between 0.7V to SGND with 0.7V or above being no DCR temperature correction.

An NTC resistor has a negative temperature coefficient, meaning that its resistance decreases as its temperature rises. The V_{ITEMP} voltage, therefore, decreases as the inductor's temperature increases, and in turn the $V_{SENSEMAX(ADJ)}$ will increase to compensate for the inductor's DCR temperature coefficient. The NTC resistor, however, is

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non-linear and the user can linearize its value by building a resistor network with regular resistors. Consult the NTC manufacturers' data sheets for detailed information.

The LTC3877 has only one ITEMP pin. When the CHL_SEL pin is asserted, the V_{ITEMP} voltage can be used to compensate both channels' temperature coefficient by placing the NTC resistor between the inductors of two channels. When the CHL_SEL pin is grounded, the V_{ITEMP} voltage only compensates Channel 1's temperature coefficient.

Another use for the ITEMP pins, in addition to NTC compensated DCR sensing, is adjusting $V_{SENSE(MAX)}$ to values between the nominal values of 10mV, 15mV, 20mV, 25mV and 30mV for a more precise current limit. This is done by applying a voltage less than 0.7V to the ITEMP pin. $V_{SENSE(MAX)}$ will be varied per the above equation. The current limit can be adjusted using this method either with a sense resistor or DCR sensing.

For more information see the NTC Compensated DCR Sensing paragraph in the Applications Information section.

Frequency Selection and Phase-Locked Loop (FREQ and MODE/PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3877's controllers can be selected using the FREQ pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 250kHz to 1MHz. There is a precision 10µA current flowing out of the FREQ pin, so the user can program the controller's switching frequency with a single resistor to SGND. A curve is provided later in the application section showing the relationship between the voltage on the FREQ pin and switching frequency. A phase-locked loop (PLL) is integrated on the LTC3877 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The controller is operating in forced continuous mode when it is synchronized. The PLL loop filter network is also integrated inside the LTC3877. The phase-locked loop is capable of locking to any frequency within the range of 250kHz to 1MHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock. The lock-in time can be minimized this way.

Power Good (PGOOD1, PGOOD2 Pins)

When either feedback voltage is not within ±10% of the 0.6V reference voltage, its respective PGOOD pin is pulled low. A PGOOD pin will also pull low when its channel is in the soft-start, UVLO or tracking phase. Both PGOOD pins pull low when the RUN pin is below 1.14V. The PGOOD pins will flag power good immediately when their feedback voltages are within ±10% of the reference window. However, there is an internal 50µs power bad mask when feedback voltages go out of the ±10% window. When there is a logic change with VID pins, the output voltage can initially be out of the ±10% window of the newly set regulation point. To avoid nuisance indications from PGOOD, the PGOOD signal is blanked for 235µs. The PGOOD pins are allowed to be pulled up by external resistors to sources of up to 6V.

Multichip Operations (PHASMD and CLKOUT Pins)

The PHASMD pin determines the relative phases between the internal channels as well as the CLKOUT signal as shown in Table 1. The phases tabulated are relative to zero phase being defined as the rising edge of the clock of phase 1.

Table 1

PHASMD	GND	FLOAT	$INTV_{CC}$
Phase 1	0°	0°	0°
Phase 2	180°	180°	240°
CLKOUT	60°	90°	120°

The CLKOUT signal can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or separate outputs. Input capacitance ESR requirements and efficiency losses are substantially reduced because the peak current drawn from the input capacitor is effectively divided by the number of phases used, and power loss is proportional to the RMS current squared. A two stage, single output voltage implementation can reduce input path power loss by 75% and radically reduce the required RMS current rating of the input capacitor(s).

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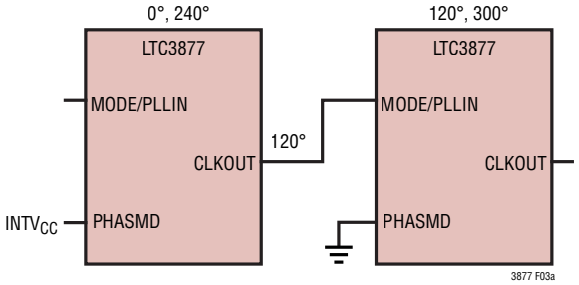

Figure 3a. 3-Phase Operation

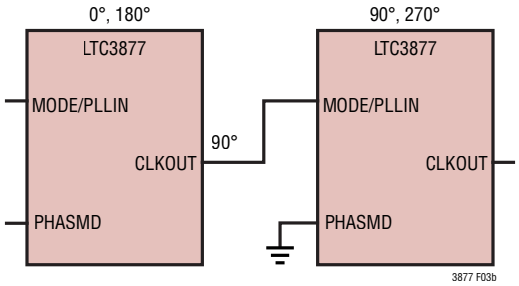

Figure 3b. 4-Phase Operation

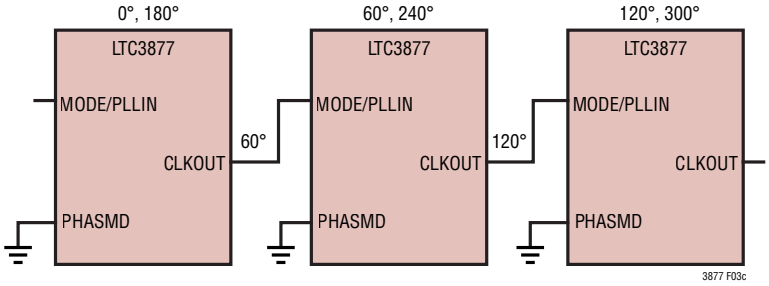

Figure 3c. 6-Phase Operation

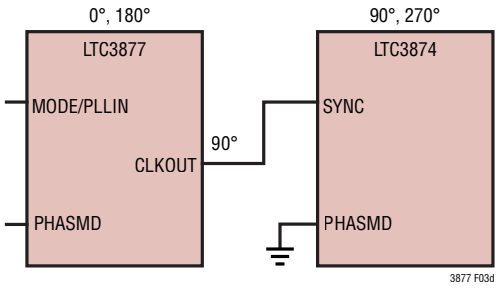

Figure 3d. 4-Phase Operation with LTC3874 as Slave IC

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Single Output Multiphase Multi-IC Operations with LTC3877 as Slave IC (V_{OSNS1}^+ Pin)

The LTC3877 can be used for single output multiphase applications. For single output operation with multiple LTC3877s, only the Master chip's DIFFAMP1 is needed and its V_{OSNS1}^+ and V_{OSNS1}^- should sense the output voltage directly across the output capacitors. The V_{OSNS1}^- pins of the slave LTC3877s are tied to local ground and their V_{OSNS1}^+ pins are tied to the master IC's DIFFOUT pin. The slave LTC3877s DIFFOUT pins are left floating. Besides these connections, the connections below are also needed:

- Tie all of the ITH pins together;
- Tie all of the V_{FB1} and V_{FB2}^+ pins together;
- Tie all of the V_{FB2}^- pins to local ground;
- Tie all of the TK/SS pins together;
- Tie all of the RUN pins together;
- Tie all of the I_{LIM} pins together or tie the I_{LIM} pins to the same voltage potential;
- Make all of the FREQ pins have the same voltage potential;
- Tie the CLKOUT pin of the Master IC to the MODE/PLLIN pins of the first Slave IC as shown in Figure 3a and 3b. If there is a second Slave IC, connect the first Slave's CLKOUT to the second Slave's MODE/PLLIN pin as shown in Figure 3c;
- Tie all of the ITEMP pins together if DCR tempco compensation is desired;
- If VID programming is desired, tie all of the VID_EN and VID0~VID5 pins together, respectively;
- If VID programming is not desired, all of the VID_EN pins and VID0~VID5 pins should be grounded;
- Add an external pull-up resistor only to the Master IC's PGOOD pin; the other PGOOD pins can be left floating.

Examples of single output multiphase multi-IC configurations are shown in Figures 16 and 17.

Single Output Multi-IC Operations with LTC3874 as Slave IC

The LTC3877 can be configured for single output multi-IC applications with LTC3874 as a Slave IC. The LTC3874 is a dedicated slave controller. Refer to the data sheet of LTC3874 for operation and typical applications. To build this type of multi-IC configuration, make the following connections:

- The LTC3874 has no internal Error Amplifier, so its ITH pins need to be tied to the LTC3877 ITH pins;
- The LTC3874's switching synchronizes to the falling edge of the external clock. Refer to Table 1 in the LTC3874 data sheet. Tie the LTC3874 SYNC pin to the CLKOUT pin of LTC3877 and bias the PHASMD pins as shown in Figure 3d;
- The rising threshold of the LTC3877 RUN pin is 1.22V, whereas the threshold of the LTC3874 RUN pin is around 1.7V;
- Connect the LTC3877 PGOOD pin to the LTC3874 FAULTB pins through an NMOS with its gate tied to the LTC3877 TK/SS pins and its drain tied to the $\overline{FAULT0}$ and $\overline{FAULT1}$ pins of the LTC3874. By this connection, the Master and Slave can startup at the same time. After the startup, the LTC3877 PGOOD signal will be the fault indicator for the LTC3874 controller;
- Tie the FAULT pins of the LTC3874 to its $INTV_{CC}$ through 120k pull-up resistors;
- Tie the MODE pins of the LTC3874 to the LTC3877 PGOOD pin for start-up control. During soft-start, the LTC3874 operates in DCM mode. After the soft-start interval is done, the LTC3874 operates in CCM mode;
- The LTC3874 and the LTC3877 have different relationships between the oscillator frequency and the voltage at their respective FREQ pins. Refer to Figure 5 in the LTC3874 data sheet. Bias the FREQ pins of LTC3874 and LTC3877 individually;

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- The LTC3874 and the LTC3877 have two current limit settings compatible for each other. Both settings require the LOWDCR pin of LTC3874 to be driven HIGH and the $SNSD^+$ pins of LTC3877 to be tied to V_{OUT}. When the LTC3874 I_{LIM} pin is grounded and the I_{LIM} pin of LTC3877 is biased to 1/4 of its $INTV_{CC}$, the Maximum Current Sense Threshold is 15mV. The other setting is to assert the I_{LIM} pin of LTC3874 and bias the I_{LIM} pin of LTC3877 to ¾ of its $INTV_{CC}$. In this case, the Maximum Current Sense Threshold is 25mV.

An example of a four phase single output multi-IC configuration with LTC3874 as a Slave IC is shown in Figure 18.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the reverse current limit for the OV condition is reached. The bottom MOSFET will be turned on again at the following edge of the next clock pulse and be turned off when the reverse current limit is reached again. This process repeats until the overvoltage condition is cleared. The reverse current limit is about two thirds of the maximum current sense threshold set by the ILM pin's voltage. This feature is especially suited for applications where VID codes are changed dynamically so that a smooth transition is ensured and the bottom MOSFET will not over-heat.

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The Typical Application on the first page of this data sheet is a basic LTC3877 application circuit configured as a dual phase single output power supply with output voltage programmed to 0.9V by VID inputs. The LTC3877 can be configured in two ways: either as a dual-phase single-output controller with output voltage programmable from 0.6V to 1.23V in 10mV steps by 6-bit parallel VID inputs, or as a two-output controller with one output voltage programmable by VID inputs and the other output voltage set by an external resistor divider.

By achieving 40ns minimum on-time, the LTC3877 can reach very low duty cycles, thus facilitating high input voltages and low output voltage applications even at high switching frequency. A wide 4.5V to 38V input supply range allows it to support a very wide variety of bus voltage. Current foldback limits the output current during a short-circuit condition. The MODE/PLLIN pin selects among Burst Mode, Pulse-Skipping Mode, or Forced Continuous Mode, and allows the IC to be synchronized to an external clock. The LTC3877 can be configured for up to 12-phase operation.

The LTC3877 is designed and optimized for use with very low DCR values by utilizing a novel approach to reduce the noise sensitivity of the sensing signal by a factor of 14dB. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, as the DCR value drops below 1mΩ, the signal-to-noise ratio is low and current sensing is difficult. The LTC3877 uses an LTC proprietary technique to solve this issue with minimum additional external components. In general, external component selection is driven by the load requirement, and begins with the DCR and inductor value. Next, power MOSFETs are selected. Finally, input and output capacitors are selected.

Current Limit Programming

The I_{LIM} pin is a 5-level logic input which sets the maximum current limit of the controller. When I_{LIM} is either grounded, floated, or tied to $INTV_{CC}$, the typical value for the maximum current sense threshold will be 10mV, 20mV, or 30mV, respectively. Setting I_{LIM} to one-fourth $INTV_{CC}$ and three-fourths $INTV_{CC}$ sets maximum current sense thresholds of 15mV and 25mV, respectively. Please note that the I_{LIM} pin has an internal 500k pull-down resistor to SGND and a 500k pull-up resistor to $INTV_{CC}$. The user should select the proper I_{LIM} level based on the inductor DCR value and targeted current limit level.

SNSD+, SNSA+ and SNS– Pins

The SNSA+ and SNS– pins are the direct inputs to the current comparators, while the SNSD+ pin is the input of an internal DC amplifier. The operating input voltage range of 0V to 3.5V is for SNSA+, SNSD+ and SNS– in a typical application. All the positive sense pins that are connected to the current comparator or the DC amplifier are high impedance with input bias currents of less than 1µA, but there is a resistance of about 300k from the SNS– pin to ground. The SNS– pin should be connected directly to V_{OUT}. The SNSD+ pin connects to the filter that has a R1 • C1 time constant equal to L/DCR of the inductor. The SNSA+ pin is connected to the second filter, R2 • C2, with the time constant equal to (R1 • C1)/5. Care must be taken not to float these pins. Filter components, especially capacitors, must be placed close to the LTC3877, and the sense lines should run close together to a Kelvin connection underneath the current sense element (Figure 4a). Because the LTC3877 is designed to be used with a very low DCR value to sense inductor current, without proper care, the parasitic resistance, capacitance and inductance will degrade the current sense signal integrity, making the programmed current limit unpredictable. As shown in Figure 4b, resistors R1 and R2 are placed close to the output inductor and capacitors C1 and C2 are close to the IC pins to prevent noise coupling to and from the sense signal.

For applications where the inductor DCR is large, the LTC3877 could also be used like any typical current mode controller with conventional DCR sensing by disabling the SNSD+ pin, shorting it to ground. An R_{SENSE} resistor or a DCR sensing RC filter can be used to sense the output inductor signal and connects to the SNSA+ pin. When the RC filter is used, its time constant, R • C, equals L/DCR of the output inductor. In these applications, the current limit, $V_{SENSE(MAX)}$, will be five times the value of $V_{SENSE(MAX)}$ with the DC loop enabled, and the operating voltage range of SNSA+ and SNS– is from 0V to 5V. An output voltage of 5V can be generated.

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Low Inductor DCR Sensing and Current Limit Estimation

The LTC3877 is specifically designed for high load current applications requiring the highest possible efficiency; it is capable of sensing the signal of an inductor DCR in the sub milliohm range (Figure 4b). The DCR is the inductor DC winding resistance, which is often less than 1mΩ for high current inductors. In high current and low output voltage applications, conduction loss of a high DCR inductor or a sense resistor will cause a significant reduction in power efficiency. For a specific output requirement and inductor, choose the current limit sensing level that provides proper margin for maximum load current, and uses the relationship of the sense pin filters to output inductor characteristics as depicted in the following equation.

$$DCR = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

$$L/DCR = R1 \bullet C1 = 5 \bullet R2 \bullet C2$$

where:

$V_{SENSE(MAX)}$ is the maximum sense voltage for a given I_{LIM} threshold;

I_{MAX} is the maximum load current per phase;

ΔI_L is the inductor ripple current;

L/DCR is the output inductor characteristics;

R1 • C1 is the filter time constant of the SNSD+ pin; and

R2 • C2 is the filter time constant of the SNSA+ pin.

For example, for a $12V_{IN}$, 1.2V/30A step-down buck converter running at 400kHz frequency, a 0.15µH, 0.4mΩ inductor is chosen. This inductor provides 15A peak-to-peak ripple current, which is 50% of the 30A full load current. At full load, the inductor peak current is 30A + 15A/2 = 37.5A.

$I_L(PK)$ • DCR = 37.5A • 0.4mΩ = 15mV.

In this case, choose the 20mV I_{LIM} setting which is the closest but higher than 15mV to provide margin for current limit.

Select the two R/C sensing networks:

Filter on SNSD+ pin: R1 • C1 = L/DCR,

Filter on SNSA+ pin: R2 • C2 = (L/DCR)/5.

In this case, the ripple sense signal across SNSA+ and SNS– pins is Δ_{ILP-P} • DCR • 5 = 15A • 0.4mΩ • 5 = 30mV.

This signal should be more than 15mV for good signal-to-noise ratio. In this case, it is certainly sufficient.

The peak inductor current at current limit is:

$I_{LIM(PK)}$ = 20mV/DCR = 20mV/0.4mΩ = 50A.

The average inductor current, which is also the output current, at current limit is:

$I_{LIM(AVG)} = I_{LIM(PK)} - \Delta_{ILP-P}/2$ = 50A – 15A/2 = 42.5A.

To ensure that the load current will be delivered over the full operating temperature range, the temperature coefficient of DCR resistance, approximately 0.4%/°C, should be taken into account. The LTC3877 features a DCR temperature compensation circuit that uses an NTC temperature sensing resistor for this purpose. See the Inductor DCR Sensing Temperature Compensation section for details.

Typically, C1 and C2 are selected in the range of 0.047µF to 0.47µF. If C1 and C2 are chosen to be 100nF, and an inductor of 150nH with 0.4mΩ DCR is selected, R1 and R2 will be 4.64k and 931Ω respectively. The bias current at SNSD+ and SNSA+ is about 30nA and 500nA respectively, and it causes some small error to the sense signal.

There will be some power loss in R1 and R2 that relates to the duty cycle, and will be the most in continuous mode at the maximum input voltage:

$$P_{LOSS}(R) = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R}$$

Ensure that R1 and R2 have a power rating higher than this value. However, DCR sensing eliminates the conduction loss of a sense resistor; it will provide better efficiency at heavy loads. To maintain a good signal-to-noise ratio for the current sense signal, use ΔV_{SENSE} of 15mV between

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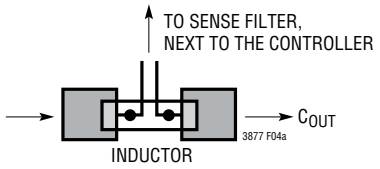

Figure 4a. Sense Lines Placement with Inductor DCR

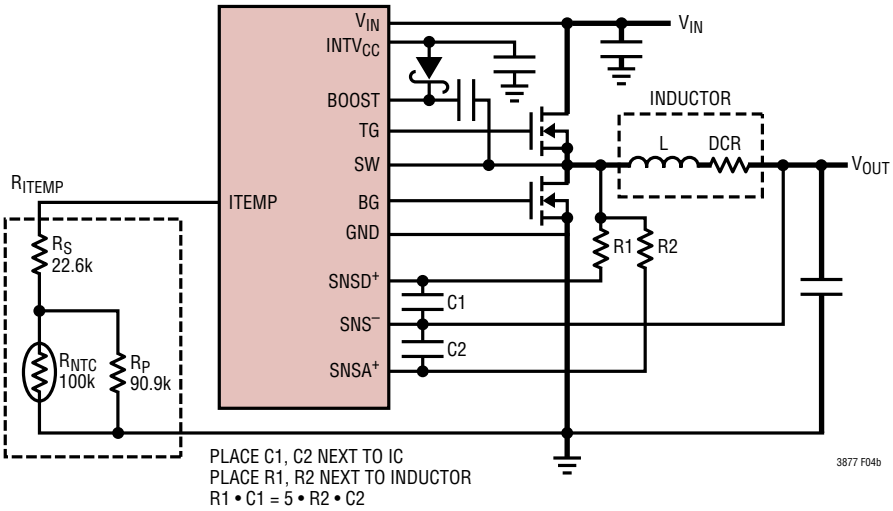

Figure 4b. Inductor DCR Current Sensing

the SNSA+ and SNS– pins or an equivalent 3mV ripple on the current sense signal. The actual ripple voltage across SNSA+ and SNS– pins will be determined by the following equation:

$$\Delta V_{SENSE} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{V_{IN} - V_{OUT}}{R2 \bullet C2 \bullet f_{OSC}}$$

Inductor DCR Sensing Temperature Compensation with NTC Thermistor

For DCR sensing applications, the temperature coefficient of the inductor winding resistance should be taken into account when the accuracy of the current limit is critical over a wide range of temperature. The main element used in inductors is copper, which has a positive tempco of approximately 4000ppm/°C. The LTC3877 provides a feature to correct for this variation through the use of the ITEMP pin. There is a 30µA precision current source flowing out of the ITEMP pin. A thermistor with a NTC (negative temperature coefficient) resistance can be used in a network, R_{ITEMP} (Figure 4b), connected to maintain the current limit threshold constant over a wide operating temperature. The ITEMP voltage range that activates the correction is from 0.7V or less. If this pin is floating, its voltage will be at $INTV_{CC}$ potential, about 5.5V. When the ITEMP voltage is higher than 0.7V, the temperature compensation is inactive. The following guidelines will help to choose components for temperature correction. The initial compensation is for 25°C ambient temperature:

1. Set the ITEMP pin resistance to 23.33k at 25°C. With 30µA flowing out of the ITEMP pin, the voltage on the ITEMP pin will be 0.7V at room temperature. Current limit correction will occur for inductor temperatures greater than 25°C.
2. Calculate the ITEMP pin resistance at the maximum inductor temperature, which is typically 100°C.

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Use the following equations:

$$V_{ITEMP100C} = 0.7 - 1.5\left(\frac{I_{MAX} \bullet DCR\,(Max) \bullet \frac{(100°C - 25°C) \bullet 0.4}{100}}{V_{SENSE(MAX)}}\right) = 0.25V$$

Since $V_{SENSE(MAX)} = I_{MAX} \bullet DCR\,(Max)$:

$$R_{ITEMP100C} = \frac{V_{ITEMP100C}}{30\mu A} = 8.33k$$

where:

$R_{ITEMP100C}$ = ITEMP pin resistance at 100°C;

$V_{ITEMP100C}$ = ITEMP pin voltage at 100°C;

$V_{SENSE(MAX)}$ = Maximum current sense threshold at room temperature;

I_{MAX} = Maximum load current per phase; and

DCR (Max) = Maximum DCR value.

Calculate the values for the NTC network's parallel and series resistors, R_P and R_S. A simple method is to graph the following R_S versus R_P equations with R_S on the y-axis and R_P on the x-axis.

$R_S = R_{ITEMP25C} - R_{NTC25C}||R_P$

$R_S = R_{ITEMP100C} - R_{NTC100C}||R_P$

Next, find the value of R_P that satisfies both equations, which will be the point where the curves intersect. Once R_P is known, solve for R_S. The resistance of the NTC thermistor can be obtained from the vendor's data sheet in the form of graphs, tabulated data, or formulas. The approximate value for the NTC thermistor for a given temperature can be calculated from the following equation:

$$R = R_0 \bullet \exp\left(B \bullet \left(\frac{1}{T + 273} - \frac{1}{T_0 + 273}\right)\right)$$

where:

R = Resistance at temperature T, which is in degrees C.

R_0 = Resistance at temperature T_0, typically 25°C.

B = B-constant of the thermistor.

Figure 5 shows a typical resistance curve for a 100k thermistor and the ITEMP pin network over temperature.

Starting values for the NTC compensation network are:

- NTC R_0 = 100k
- R_S = 7.32k
- R_P = 20k

But, the final values should be calculated using the above equations and checked at 25°C and 100°C. After determining the components for the temperature compensation network, check the results by plotting I_{MAX} versus inductor temperature using the following equations:

$$I_{DC(MAX)} = \frac{V_{SENSEMAX(ADJ)} - \frac{\Delta V_{SENSE}}{2}}{DCR(MAX)\ at\ 25°C \bullet \left(1 + \left(T_{L(MAX)} - 25°C\right) \bullet \frac{0.4}{100}\right)}$$

where:

$$V_{SENSEMAX(ADJ)} = V_{SENSE(MAX)} \bullet \frac{2.2 - V_{ITEMP}}{1.5};$$

$V_{ITEMP} = 30\mu A \bullet (R_S + R_P||R_{NTC})$;

$I_{DC(MAX)}$ = Maximum average inductor current; and

T_L is the inductor temperature.

The resulting current limit should be greater than or equal to I_{MAX} for inductor temperatures between 25°C and 100°C.

Typical values for the NTC compensation network are:

- NTC R_0 = 100k, B-constant = 3000 to 4000
- $R_S \approx$ 7.32k
- $R_P \approx$ 20k

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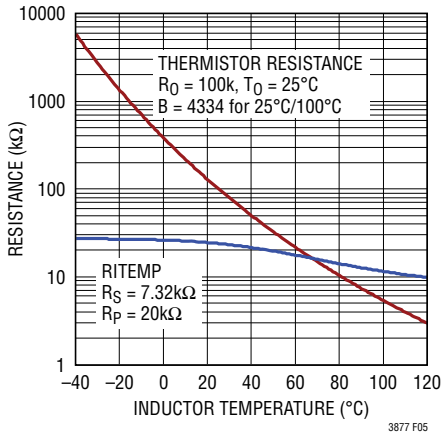


Figure 5. Resistance vs Temperature for I_{TEMP} Pin Network with 100k NTC

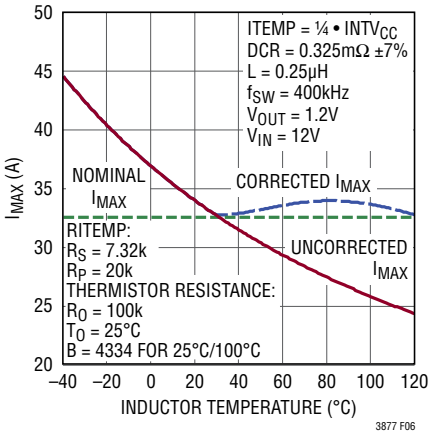
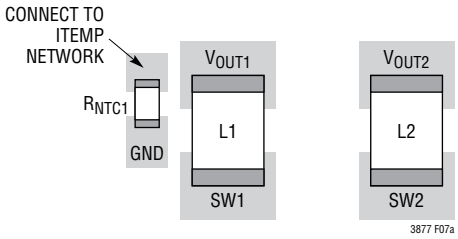
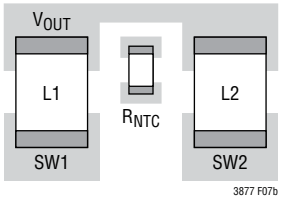


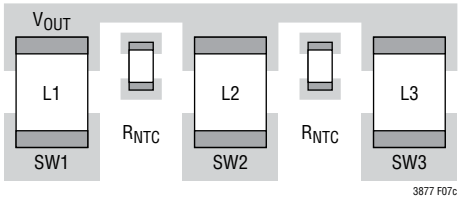
Figure 6. Worst-Case I_{MAX} vs Inductor Temperature Curve with and without NTC Temperature Compensation



(7a) Dual Output Dual Phase DCR Sensing Application



(7b) Single Output Dual Phase DCR Sensing Application



(7c) Single Output Three Phase DCR Sensing Application

Figure 7. Thermistor Locations. Place Thermistor Next to Inductor(s) for Accurate Sensing of the Inductor Temperature, but Keep the ITEMP Pin away from the Switch Nodes and Gate Traces

Generating the I_{MAX} versus inductor temperature curve plot first using the above values as a starting point, and then adjusting the R_S and R_P values as necessary, is another approach. Figure 6 shows a curve of I_{MAX} versus inductor temperature.

The LTC3877 has one ITEMP pin. For a Dual Output Dual Phase configuration, the DCR temperature compensation function is only available for channel 1. Place the NTC resistor next to the inductor of channel 1 as shown in Figure 7a. For a Single Output Dual Phase application, place the NTC resistor in between the inductors of the two channels, as shown in Figure 7b. For a Single Output Multi IC application, place NTC resistors of the same value in between of any two channels' inductors as shown in Figure 7c. Connect all these NTC resistors in parallel, and calculate the R_S and R_P value accordingly. In this case, tie the ITEMP pins together and calculate for an ITEMP pin current of 30µA • number of ITEMP pins.

For the most accurate temperature detection, place the thermistors next to the inductors. Take care to keep the ITEMP pins and their traces away from the switch nodes and gate traces.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current

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signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles > 40%. However, the LTC3877 uses a scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}}\left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

At least two external power MOSFETs need to be selected: one N-channel MOSFET for the top (main) switch and one or more N-channel MOSFET(s) for the bottom (synchronous) switch. The number, type and on-resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than one-third of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFET's on-resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the main switch application in switching regulators.

The peak-to-peak MOSFET gate drive levels are set by the internal regulator voltage, V_{INTVCC}, requiring the use of logic-level threshold MOSFETs in most applications. Pay close attention to the BVDSS specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less. Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, input capacitance, input voltage, and maximum output current. MOSFET input capacitance is a combination of several components but can be taken from the typical gate charge curve included on most data sheets (Figure 8). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given VDS drain voltage, but can be adjusted for different VDS voltages by multiplying the ratio of the application VDS to the curve specified VDS values. A way to estimate the C_{MILLER} term

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is to take the change in gate charge from points a and b on a manufacturer's data sheet and divide by the stated VDS voltage specified. C_{MILLER} is the most important selection criterion for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. CRSS and COS are specified sometimes but definitions of these parameters are not included. When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet \left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right]\bullet f$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

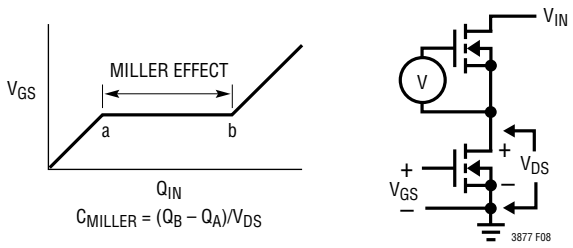

Figure 8. Gate Charge Characteristic

where δ is the temperature dependency of $R_{DS(ON)}$, RDR is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), V_{IN} is the drain potential and the change in drain potential in the particular application. $V_{TH(MIN)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above. Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For V_{IN} < 20V, the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

An optional Schottky diode across the synchronous MOSFET conducts during the dead time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse-recovery period which could cost as much as several percent in efficiency. A 2A to 8A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition loss due to their larger junction capacitance.

Soft-Start and Tracking and Sequencing

The LTC3877 has the ability to either soft-start by itself with a capacitor or track the output of another channel or external supply. When one particular channel is configured to soft-start by itself, a capacitor should be connected to its TK/SS pin. Both channels are in the shutdown state if the RUN pin voltage is below 1.14V. The TK/SS pins are actively pulled to ground in this shutdown state.

Once the RUN pin voltage is above 1.22V, both channels power up. A soft-start current of 1.25µA then starts to charge their soft-start capacitors. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage of each channel according to the ramp rate on its

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TK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to 0.6V on the TK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.6 \bullet \frac{C_{SS}}{1.25\mu A}$$

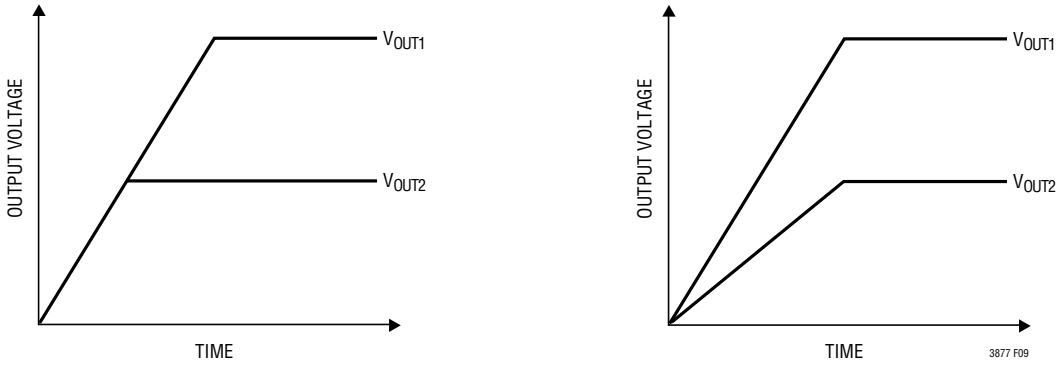
Regardless of the mode selected by the MODE/PLLIN pin, the regulator will always start in pulse-skipping mode up to TK/SS = 0.5V. Between TK/SS = 0.5V and 0.56V, it will operate in forced continuous mode and revert to the selected mode once TK/SS > 0.56V. The output ripple is minimized during the 60mV forced continuous mode window, ensuring a clean PGOOD signal.

After the RUN pin is higher than 1.22V, the TK/SS can still be actively pull down to ground by external logic. The converter will attempt to regulate the output to zero volts. This function provides a way to sequence the outputs between channels or another supply.

When the channel is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply's voltage. Note that the small soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistive divider value to be small enough to make this error negligible. In order to track down another channel or supply after the soft-start phase expires, the LTC3877 is forced into continuous mode of operation as soon as V_{FB} is below the undervoltage threshold of 0.55V regardless of the setting on the MODE/PLLIN pin. However, the LTC3877 should always be set in force continuous mode tracking down when there is no load. After TK/SS drops below 0.1V, its channel will operate in discontinuous mode.

The LTC3877 allows the user to program how its output ramps up and down by means of the TK/SS pins. Through these pins, the output can be set up to either coincidentally or ratiometrically track another supply's output, as shown in Figure 9. In the following discussions, V_{OUT1} refers to the LTC3877's output 1 as a master channel and V_{OUT2} refers to the LTC3877's output 2 as a slave channel. In practice, though, either phase can be used as the master. To implement the coincident tracking in Figure 9a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the TK/SS pin of the slave channel. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in Figure 10a. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking in Figure 9b, the ratio of the V_{OUT2} divider should be exactly the same as the master channel's feedback divider shown in Figure 10b. By selecting different resistors, the LTC3877 can achieve different modes of tracking including the two in Figure 9.

So which mode should be programmed? While either mode in Figure 9 satisfies most practical applications, some tradeoffs exist. The ratiometric mode saves a pair of resistors, but the coincident mode offers better output regulation. When the master channel's output experiences



(9a) Coincident Tracking

(9b) Ratiometric Tracking

Figure 9. Two Different Modes of Output Voltage Tracking

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(10a) Coincident Tracking Setup

(10b) Ratiometric Tracking Setup

Figure 10. Setup for Coincident and Ratiometric Tracking

dynamic excursion (under load transient, for example), the slave channel output will be affected as well. For better output regulation, use the coincident tracking mode instead of ratiometric.

Pre-Biased Output at Start-Up

There may be situations that require the power supply to start up with a pre-bias on the output capacitors. In this case, it is desirable to start up without discharging that output pre-bias. The LTC3877 can safely power up into a pre-biased output without discharging it. The LTC3877 accomplishes this by disabling both TG and BG until the TK/SS pin voltage and the internal soft-start voltage are above the V_{FB} pin voltage. When V_{FB} is higher than TK/SS or the internal soft-start voltage, the error amp output is railed low. The control loop would turn BG on, which would discharge the output. Disabling BG and TG prevents the pre-biased output voltage from being discharged. When TK/SS and the internal soft-start both cross 500mV or V_{FB}, whichever is lower, TG and BG are enabled. If the pre-bias is higher than the OV threshold, the bottom gate is turned on immediately to pull the output back into the regulation window.

$INTV_{CC}$ Regulators and $EXTV_{CC}$

The LTC3877 features a PMOS LDO that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and much of the LTC3877's internal circuitry. The linear regulator regulates the voltage at the $INTV_{CC}$ pin to 5.5V when V_{IN} is greater than 6V. $EXTV_{CC}$ connects to $INTV_{CC}$ through a P-channel MOSFET and can supply the needed power when its voltage is higher than 4.7V. Each of these can supply a peak current of 100mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3877 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the 5.5V linear regulator or $EXTV_{CC}$. When the voltage on the $EXTV_{CC}$ pin is less than 4.7V, the linear regulator is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, the LTC3877 $INTV_{CC}$ current is limited to less than 42.6mA from a 38V supply in the UK package and not using the $EXTV_{CC}$ supply:

$$T_J = 70°C + (42.6mA)(34V)(31°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE/PLLIN = SGND) at maximum V_{IN}. When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the $INTV_{CC}$ linear regulator is turned off and the $EXTV_{CC}$ is connected to the $INTV_{CC}$. The $EXTV_{CC}$ remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. Using the $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from one of the LTC3877's switching regulator outputs during normal operation and from the $INTV_{CC}$ when the output

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is out of regulation (e.g., start-up, short-circuit). If more current is required through the $EXTV_{CC}$ than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Do not apply more than 6V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} \leq V_{IN}$ at all times.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency). Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (42.6mA)(5V)(34°C/W) = 77°C$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5.5V regulator resulting in an efficiency penalty at high input voltages.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If a 5V external supply is available, it may be used to power $EXTV_{CC}$ provided it is compatible with the MOSFET gate drive requirements.
4. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V.

For applications where the main input power is below 5.5V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5.5V input with a 1Ω or 2.2Ω resistor as shown in Figure 11 to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low due to the dropout voltage. Make sure the $INTV_{CC}$ voltage is at or exceeds the $R_{DS(ON)}$ test voltage for the MOSFET, which is typically 4.5V for logic level devices.

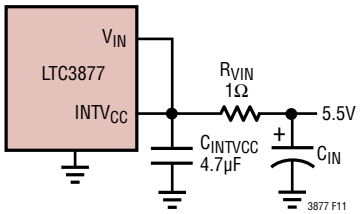

Figure 11. Setup for a 5.5V Input

Topside MOSFET Driver Supply (C_B, DB)

External bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltages for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged though external diode DB from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply:

$$V_{BOOST} = V_{IN} + V_{INTVCC} – V_{DB}$$

Where V_{DB} is the boost diode forward voltage drop.

The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Undervoltage Lockout

The LTC3877 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3.7V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 500mV of precision hysteresis.

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Another highly recommended way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough. An extra 4.5µA of current flows out of the RUN pin once the RUN pin voltage passes 1.22V. One can program the hysteresis of the run comparator by adjusting the values of the resistive divider. It is recommended that for applications where V_{IN} is below 5.5V, do not turn on the LTC3877 until V_{IN} ramps above 4.5V, while for applications where V_{IN} is equal or higher than 5.5V, do not turn on the LTC3877 until V_{IN} ramps above 5.5V.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[\left(V_{OUT}\right)\left(V_{IN}-V_{OUT}\right)\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3877, ceramic capacitors can also be used for C_{IN}. Always consult the capacitor manufacturer if there is any question.

The benefit of the LTC3877 2-phase operation can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The sources of the top MOSFETs should be placed within 1cm of each other and share common C_{IN}(s). Separating the sources and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3877, is also suggested. A 2.2Ω to 10Ω resistor placed between C_{IN} and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the equivalent series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR+\frac{1}{8fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

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Table 2. VID Output Voltage Programming

VID5	VID4	VID3	VID2	VID1	VID0	OUTPUT VOLTAGE (mV)
0	0	0	0	0	0	600
0	0	0	0	0	1	610
0	0	0	0	1	0	620
0	0	0	0	1	1	630
0	0	0	1	0	0	640
0	0	0	1	0	1	650
0	0	0	1	1	0	660
0	0	0	1	1	1	670
0	0	1	0	0	0	680
0	0	1	0	0	1	690
0	0	1	0	1	0	700
0	0	1	0	1	1	710
0	0	1	1	0	0	720
0	0	1	1	0	1	730
0	0	1	1	1	0	740
0	0	1	1	1	1	750
0	1	0	0	0	0	760
0	1	0	0	0	1	770
0	1	0	0	1	0	780
0	1	0	0	1	1	790
0	1	0	1	0	0	800
0	1	0	1	0	1	810
0	1	0	1	1	0	820
0	1	0	1	1	1	830
0	1	1	0	0	0	840
0	1	1	0	0	1	850
0	1	1	0	1	0	860
0	1	1	0	1	1	870
0	1	1	1	0	0	880
0	1	1	1	0	1	890
0	1	1	1	1	0	900
0	1	1	1	1	1	910
1	0	0	0	0	0	920
1	0	0	0	0	1	930
1	0	0	0	1	0	940
1	0	0	0	1	1	950
1	0	0	1	0	0	960
1	0	0	1	0	1	970
1	0	0	1	1	0	980

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VID5	VID4	VID3	VID2	VID1	VID0	OUTPUT VOLTAGE (mV)
1	0	0	1	1	1	990
1	0	1	0	0	0	1,000
1	0	1	0	0	1	1,010
1	0	1	0	1	0	1,020
1	0	1	0	1	1	1,030
1	0	1	1	0	0	1,040
1	0	1	1	0	1	1,050
1	0	1	1	1	0	1,060
1	0	1	1	1	1	1,070
1	1	0	0	0	0	1,080
1	1	0	0	0	1	1,090
1	1	0	0	1	0	1,100
1	1	0	0	1	1	1,110
1	1	0	1	0	0	1,120
1	1	0	1	0	1	1,130
1	1	0	1	1	0	1,140
1	1	0	1	1	1	1,150
1	1	1	0	0	0	1,160
1	1	1	0	0	1	1,170
1	1	1	0	1	0	1,180
1	1	1	0	1	1	1,190
1	1	1	1	0	0	1,200
1	1	1	1	0	1	1,210
1	1	1	1	1	0	1,220
1	1	1	1	1	1	1,230

Setting Output Voltage

When VID_EN is LOW, depending on the Channel 1's configuration, the LTC3877 output voltages are either each set by an external feedback resistive divider carefully placed across the output, as shown in Figure 2b and 2c, or placed near the IC for Channel 1, as shown in Figure 2a. If SNSD+ pins are grounded, the connections in Figure 2b can allow Channel 1's output up to 5V, while the connections in Figure 2a allows Channel 1's output up to 3.5V. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_{D1}}{R_{D2}}\right)$$

To improve the frequency response, a feed-forward capacitor, C_{F1}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the drive TG, BG or the SW lines.

When VID_EN is HIGH, the LTC3877's internal resistor bank will determine the output voltage. The VID is a 6-bit parallel input DAC that programs the output voltage from 0.6V to 1.23V in 10mV steps as shown in Table 2.

During VID transitions, continuous conduction mode will be applied to channel 1 (or to both channels, if CHL_SEL is asserted) for 11 switching cycles to speed up output voltage transition at low load conditions.

APPLICATIONS INFORMATION

Fault Conditions: Current Limit and Current Foldback

The LTC3877 includes current foldback to help limit load current when the output is shorted to ground. If the output voltage falls below 50% of its nominal level, then the maximum sense voltage is progressively lowered from its maximum programmed value to one-third of the maximum value. Foldback current limiting is disabled during the soft-start or tracking up. Under short-circuit conditions with very low duty cycles, the LTC3877 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC3877 (≈ 40ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{IN}}{L}$$

The resulting short-circuit current is:

$$I_{SC} = \frac{1/3\,V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2}\Delta I_{L(SC)}$$

Overcurrent Fault Recovery

When the output of the power supply is loaded beyond its preset current limit, the regulated output voltage will collapse depending on the load. The output may be shorted to ground through a very low impedance path or it may be a resistive short, in which case the output will collapse partially, until the load current equals the preset current limit. The controller will continue to source current into the short. The amount of current sourced depends on the I_{LIM} pin setting and the V_{FB} voltage as shown in the Current foldback graph in the Typical Performance Characteristics section. Upon removal of the short, the output soft starts using the internal soft-start, thus reducing output overshoot. In the absence of this feature, the output capacitors would have been charged at current limit, and in applications with minimal output capacitance this may have resulted in output overshoot. Current limit foldback is not disabled during an overcurrent recovery. The load must step below the folded back current limit threshold in order to restart from a hard short.

Thermal Protection

Excessive ambient temperatures, loads and inadequate airflow or heat sinking can subject the chip, inductor, FETs, etc. to high temperatures. This thermal stress reduces component life and if severe enough, can result in immediate catastrophic failure. To protect the power supply from undue thermal stress, the LTC3877 has a fixed chip temperature-based thermal shutdown. The internal thermal shutdown is set for approximately 160°C with 10°C of hysteresis. When the chip reaches 160°C, both TG and BG are disabled until the chip cools down below 150°C.

Phase-Locked Loop and Frequency Synchronization

The LTC3877 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the MODE/PLLIN pin. The turn-on of controller 2's top MOSFET is thus 180 degrees out-of-phase with the external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 10µA of current flowing out of the FREQ pin. This allows the user to use a single

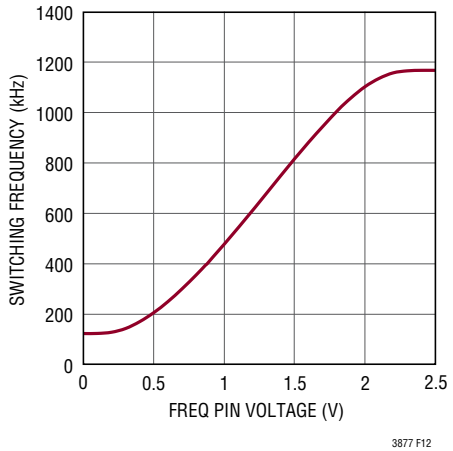


Figure 12. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

APPLICATIONS INFORMATION

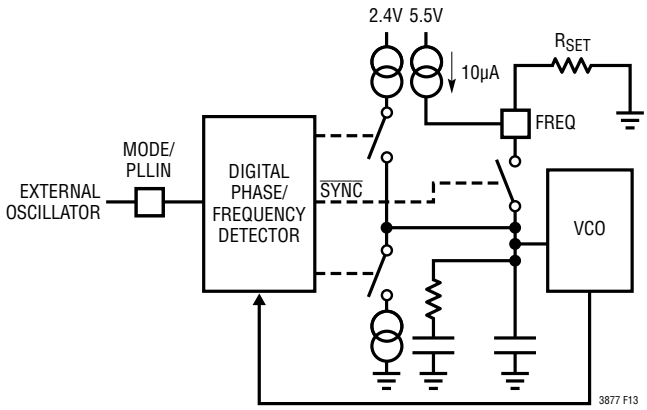


Figure 13. Phase-Locked Loop Block Diagram

resistor to GND to set the switching frequency when no external clock is applied to the MODE/PLLIN pin. The internal switch between FREQ pin and the integrated PLL filter network is ON, allowing the filter network to be pre-charged to the same voltage potential as the FREQ pin. The relationship between the voltage on the FREQ pin and the operating frequency is shown in Figure 12 and specified in the Electrical Characteristic table. If an external clock is detected on the MODE/PLLIN pin, the internal switch mentioned above will turn off and isolate the influence of FREQ pin. Note that the LTC3877 can only be synchronized to an external clock whose frequency is within range of the LTC3877's internal VCO. This is guaranteed to be between 250kHz and 1MHz. A simplified block diagram is shown in Figure 13.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the filter network. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor holds the voltage.

Typically, the external clock (on MODE/PLLIN pin) input high threshold is 1.6V, while the input low threshold is 1V. It is not recommended to apply the external clock when the IC is in shutdown.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC3877 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{(V_{IN} \bullet f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase. The minimum on-time for the LTC3877 is approximately 40ns, with reasonably good PCB layout, minimum 30% inductor current ripple and at least 2mV ripple on the current sense signal. The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak sense voltage decreases the minimum on-time gradually increases to 60ns. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3877 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

APPLICATIONS INFORMATION

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, IGATECHG = f(QT + QB), where QT and QB are the gate charges of the topside and bottom side MOSFETs.

   Supplying $INTV_{CC}$ power through $EXTV_{CC}$ from an output-derived source will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. Using $EXTV_{CC}$ reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, and current sense resistor (if used). In continuous mode, the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 10mΩ, R_L = 10mΩ, R_{SENSE} = 5mΩ, then the total resistance is 25mΩ. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A for a 5V output, or a 3% to 12% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   $$\text{TRANSITION LOSS} = (1.7)\, V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. The LTC3877 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet$ (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem.

The availability of the ITH pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Typical Application circuit will provide an adequate starting point for most applications.

APPLICATIONS INFORMATION

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 14. Figure 15 illustrates the current waveforms present in the various branches of a 2-phase synchronous regulators operating in continuous mode.

Check the following in your layout:

1. Are the top N-channel MOSFETs M1 and M3 located within 1cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.
2. Are the signal and power grounds kept separate? The combined IC ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The V_{FB}, V_{OSNS}, and I_{TH} traces should be as short as possible. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.
3. Are the $SNSD^+$, $SNSA^+$ and $SNS^–$ printed circuit traces routed together with minimum PC trace spacing? The filter capacitors between $SNSD^+$, $SNSA^+$ and $SNS^–$ should be as close as possible to the pins of the IC. Connect the $SNSD^+$ and $SNSA^+$ pins to the filter resistors as illustrated in Figure 4b.
4. Do the (+) plates of C_{IN} connect to the drain of the topside MOSFET as closely as possible? This capacitor provides the pulsed current to the MOSFET.
5. Keep the switching nodes, SW, BOOST and TG away from sensitive small-signal nodes ($SNSD^+$, $SNSA^+$, $SNS^–$, $V_{OSNS1}{}^+$, $V_{OSNS1}{}^–$, V_{FB1}, $V_{FB2}{}^+$, $V_{FB2}{}^–$). Ideally the SW, BOOST and TG printed circuit traces should be routed away and separated from the IC and especially the quiet side of the IC. Separate the high dv/dt traces from sensitive small-signal nodes with ground traces or ground planes.

APPLICATIONS INFORMATION

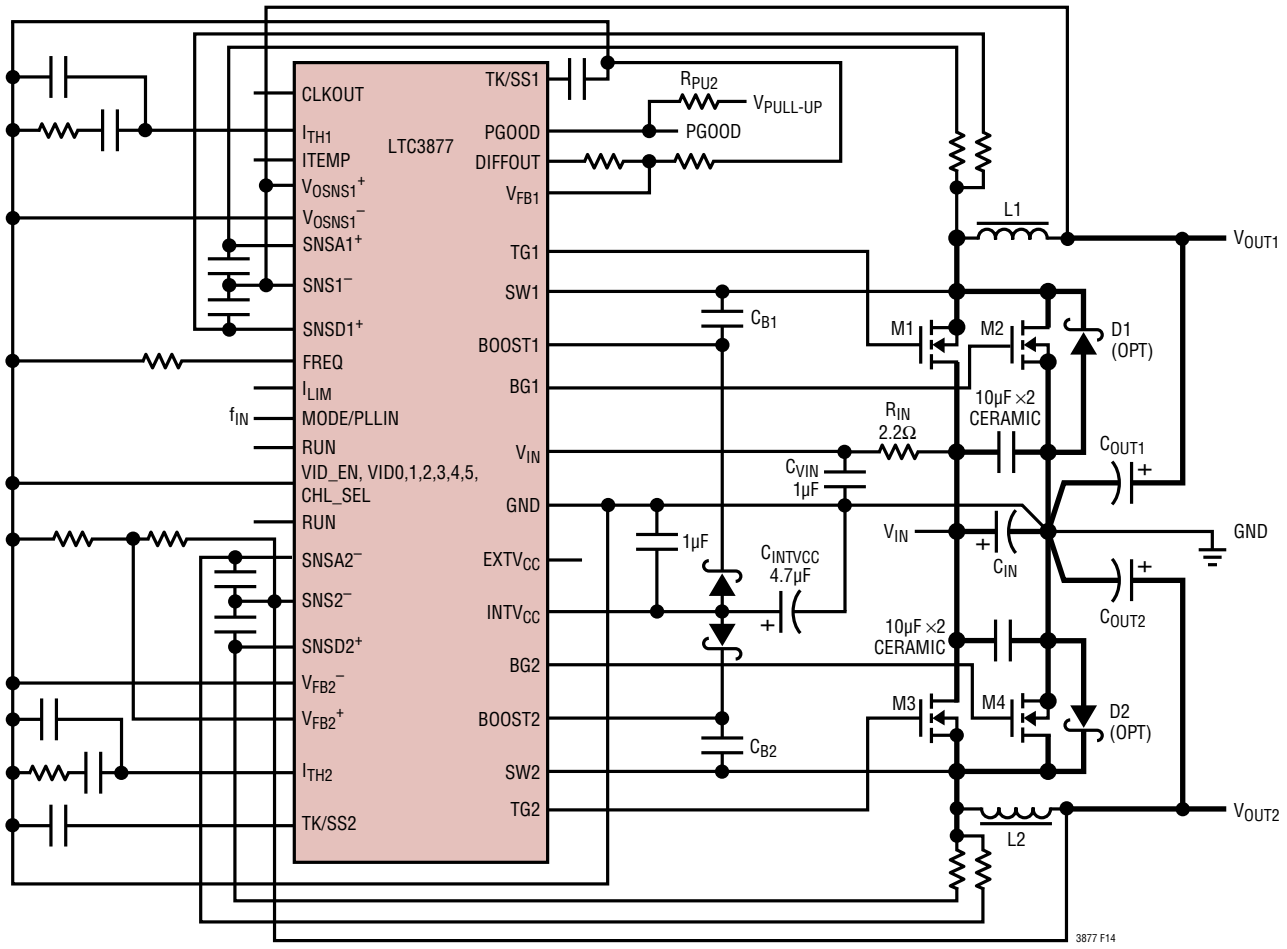


Figure 14. Recommended Printed Circuit Layout Diagram

6. The $INTV_{CC}$ bypassing capacitor should be placed immediately adjacent to the IC between the $INTV_{CC}$ pin and PGND plane. A 1µF ceramic capacitor of the X7R or X5R type is small enough to fit very close to the IC to minimize the ill effects of the large current pulses drawn to drive the bottom MOSFETs. An additional 4.7µF to 10µF of ceramic, tantalum or other very low ESR capacitance is recommended in order to keep the internal IC supply quiet.
7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ bypassing capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.
8. Use a low impedance source such as a logic gate to drive the MODE/PLLIN pin and keep the lead as short as possible.

APPLICATIONS INFORMATION

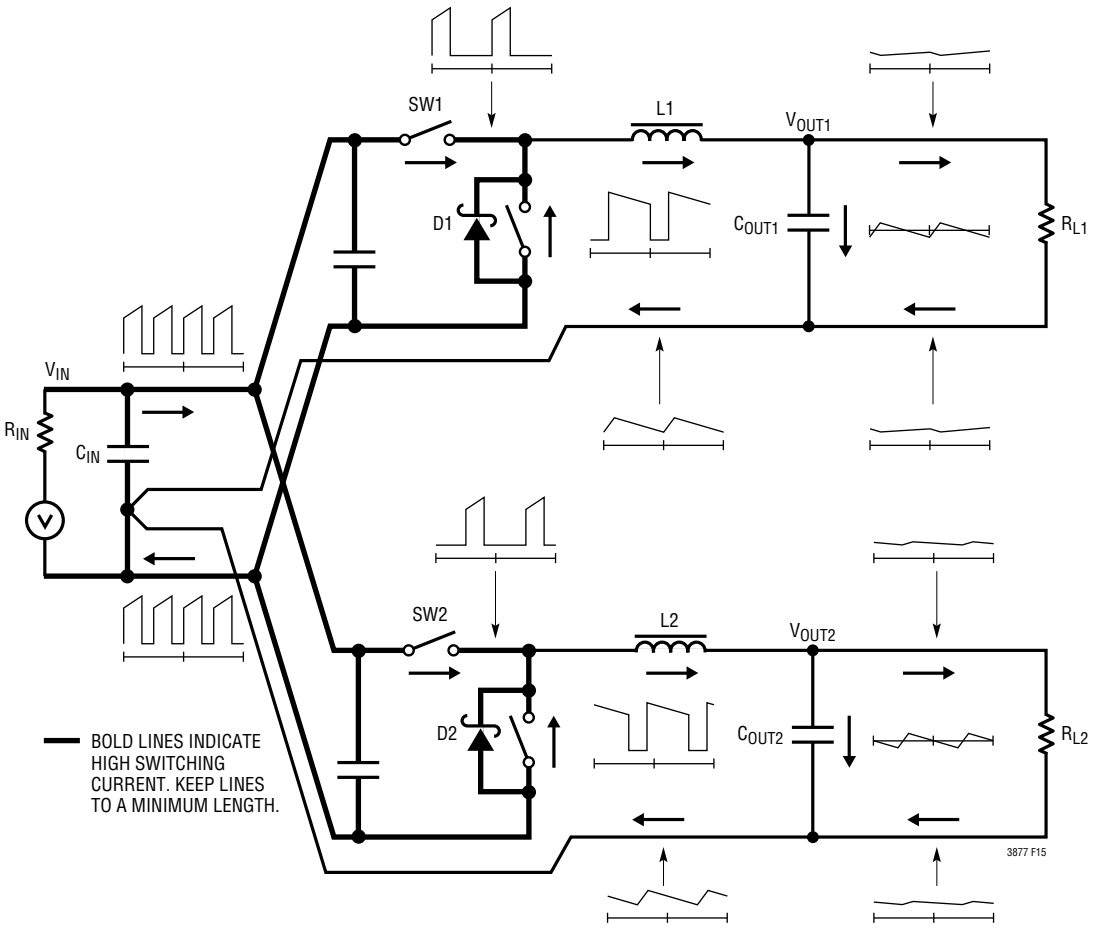


Figure 15. Branch Current Waveforms

9. The 47pF to 330pF ceramic capacitor between the ITH pin and signal ground should be placed as close as possible to the IC. Figure 15 illustrates all branch currents in a switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high switching current paths to a small physical size. High electric and magnetic fields will radiate from these loops just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the noise generated by a switching regulator. The ground terminations of the synchronous MOSFET and Schottky diode should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. External OPTI-LOOP® compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

APPLICATIONS INFORMATION

PC Board Layout Debugging

Start with one controller at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation. The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a sub-harmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

Design Example

As a design example for a single output dual phase high current regulator, assume V_{IN} = 12V(nominal), V_{IN} = 20V(maximum), V_{OUT} = 0.6V to 1.2V, $I_{MAX}1,2$ = 30A, and f = 400kHz (see Figure 16). $I_{MAX}1,2$ is the maximum DC load current per each phase.

In addition to connecting the outputs of the power stages together, a few steps are necessary to configure the LTC3877 for a two-phase single output controller. First, tie CHL_SEL to $INTV_{CC}$. Then, connect TK/SS1 to TK/SS2, and connect ITH1 to ITH2. Finally, Short the V_{FB1} pins and V_{FB2}^{+} pins together and short V_{FB2}^{-} to signal ground. With VID_EN low, the regulated output voltages are determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_{D1}}{R_{D2}}\right)$$

For an output voltage of 0.9V, set R_{D1} = 10k and R_{D2} = 20k.

The frequency is set by biasing the FREQ pin to 866mV (see Figure 12).

The inductance values are based on a 45% maximum ripple current assumption (13.5A for each channel). The highest value of ripple current occurs at the maximum input voltage and maximum output voltage, therefore:

$$L \geq \frac{V_{OUT(MAX)}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT(MAX)}}{V_{IN(MAX)}}\right)$$

The minimum inductor value is 0.21µH. The Würth 744301025, 0.25µH inductor, is chosen. At the nominal input voltage (12V) and maximum output voltage (1.2V), the ripple current will be:

$$\Delta I_{L(NOM)} = \frac{V_{OUT(MAX)}}{f \bullet L}\left(1 - \frac{V_{OUT(MAX)}}{V_{IN(NOM)}}\right)$$

APPLICATIONS INFORMATION

It will have 11A (37%) ripple. The peak inductor current, I_{PEAK}, will be the maximum DC value plus one-half the ripple current, or 35.5A.

The minimum on-time occurs at the maximum V_{IN}, and minimum V_{OUT} and should not be less than 40ns:

$$t_{ON(MIN)} = \frac{V_{OUT(MIN)}}{V_{IN(MAX)}(f)} = \frac{0.6V}{20V(400kHz)} = 75ns$$

DCR sensing is used in this circuit. If C1 and C2 are chosen to be 220nF, based on the chosen 0.25µH inductor with 0.32mΩ DCR, R1 and R2 can be calculated as:

$$R1 = \frac{L}{DCR \bullet C1} = 3.55k$$

$$R2 = \frac{L}{DCR \bullet C2 \bullet 5} = 710\Omega$$

Choose R1 = 3.57k and R2 = 715Ω.

The maximum DCR of the inductor is 0.34mΩ. The $V_{SENSE(MAX)}$ is calculated as:

$$V_{SENSE(MAX)} = I_{PEAK} \bullet DCR_{MAX} = 12mV$$

The current limit is chosen to be 15mV. If temperature variation is considered, please refer to Inductor DCR Sensing Temperature Compensation with NTC Thermistor.

The power dissipation on the topside MOSFET can be easily estimated. Choosing an Infineon BSC050NE2LS MOSFET results in: $R_{DS(ON)}$ = 7.1mΩ (max), V_{MILLER} = 2.8V, $C_{MILLER} \cong$ 35pF. At maximum input voltage with T_J (estimated) = 75°C and maximum V_{OUT}:

$$P_{MAIN} = \frac{1.2V}{20V}(30A)^2\left[1+(0.005)(75°C-25°C)\right]\bullet$$
$$(0.0071\Omega)+(20V)^2\left(\frac{30A}{2}\right)(2\Omega)(35pF)\bullet$$
$$\left[\frac{1}{5.5V-2.8V}+\frac{1}{2.8V}\right](400kHz)$$
$$= 479mW + 122mW$$
$$= 601mW$$

For a 0.32mΩ DCR, a short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{(1/3)15mV}{0.32m\Omega} - \frac{1}{2}\left(\frac{40ns(20V)}{0.25\mu H}\right) = 14A$$

An Infineon BSC010NE2LS, $R_{DS(ON)}$ = 1.1mΩ, is chosen for the bottom FET. The resulting power loss at minimum V_{OUT} and maximum V_{IN} is:

$$P_{SYNC} = \frac{20V-0.6V}{20V}(30A)^2 \bullet$$
$$\left[1+(0.005)\bullet(75°C-25°C)\right]\bullet 0.0011\Omega = 1.2W$$

C_{IN} is chosen for an equivalent RMS current rating of at least 13.7A. C_{OUT} is chosen with an equivalent series resistance (ESR) of 4.5mΩ for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage.

The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.0045\Omega \bullet 11A = 49.5mV_{P-P}$$

Further reductions in output voltage ripple can be made by placing a 100µF ceramic capacitor across C_{OUT}.

APPLICATIONS INFORMATION

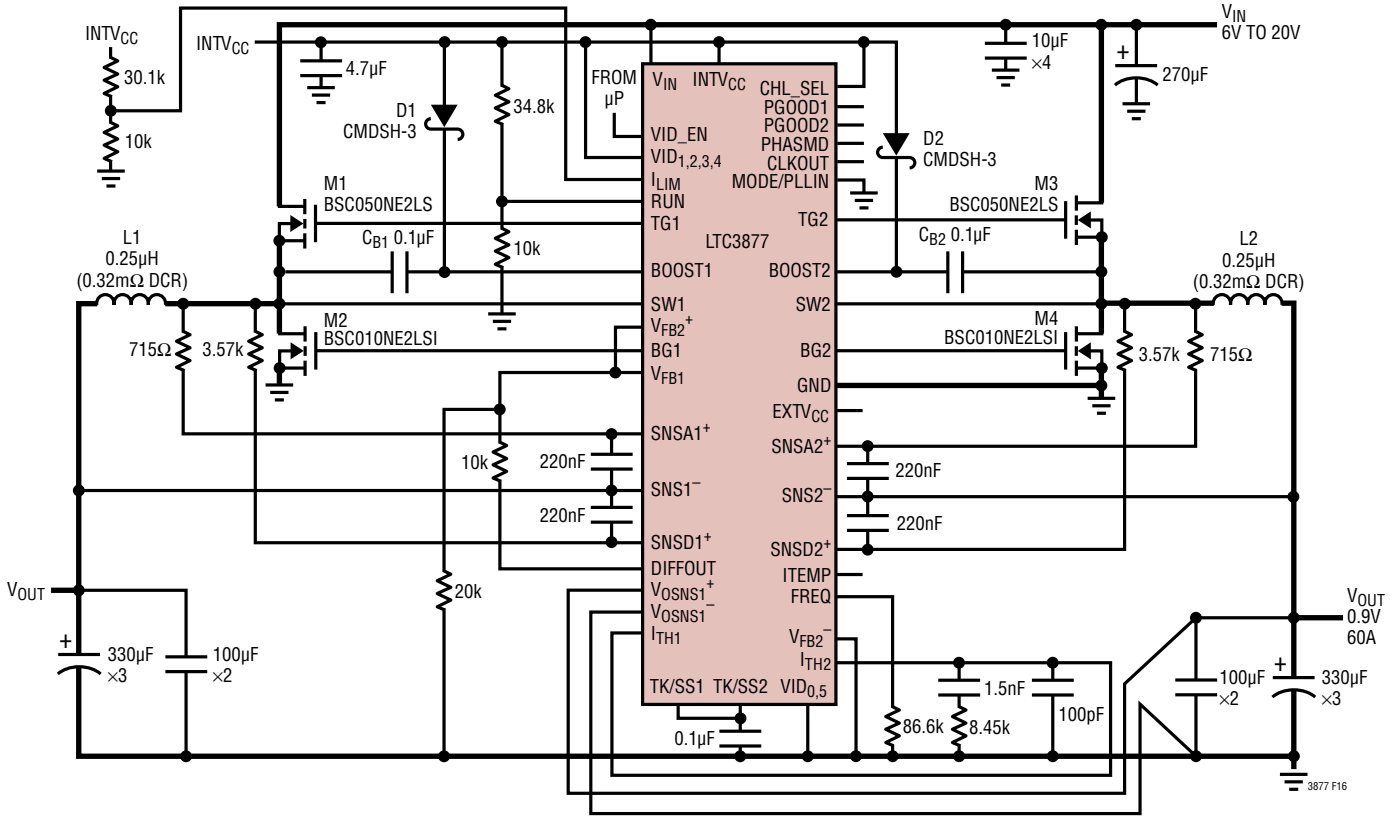


Figure 16. Dual Phase 0.9V, 60A Power System with Ultra Low DCR Sensing

APPLICATIONS INFORMATION

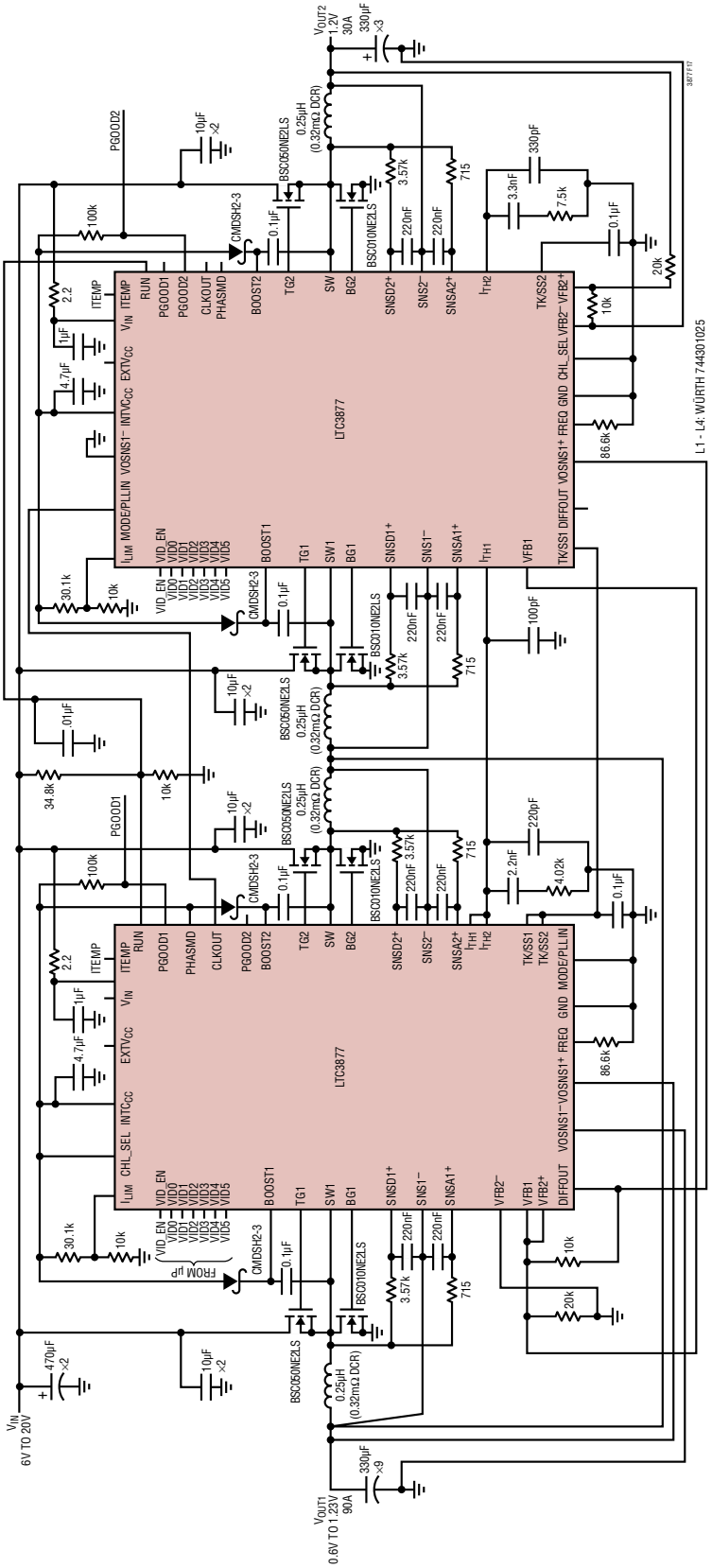


Figure 17. 3 + 1 Converter: 0.6V to 1.23V at 90A and 1.2V at 30A

APPLICATIONS INFORMATION

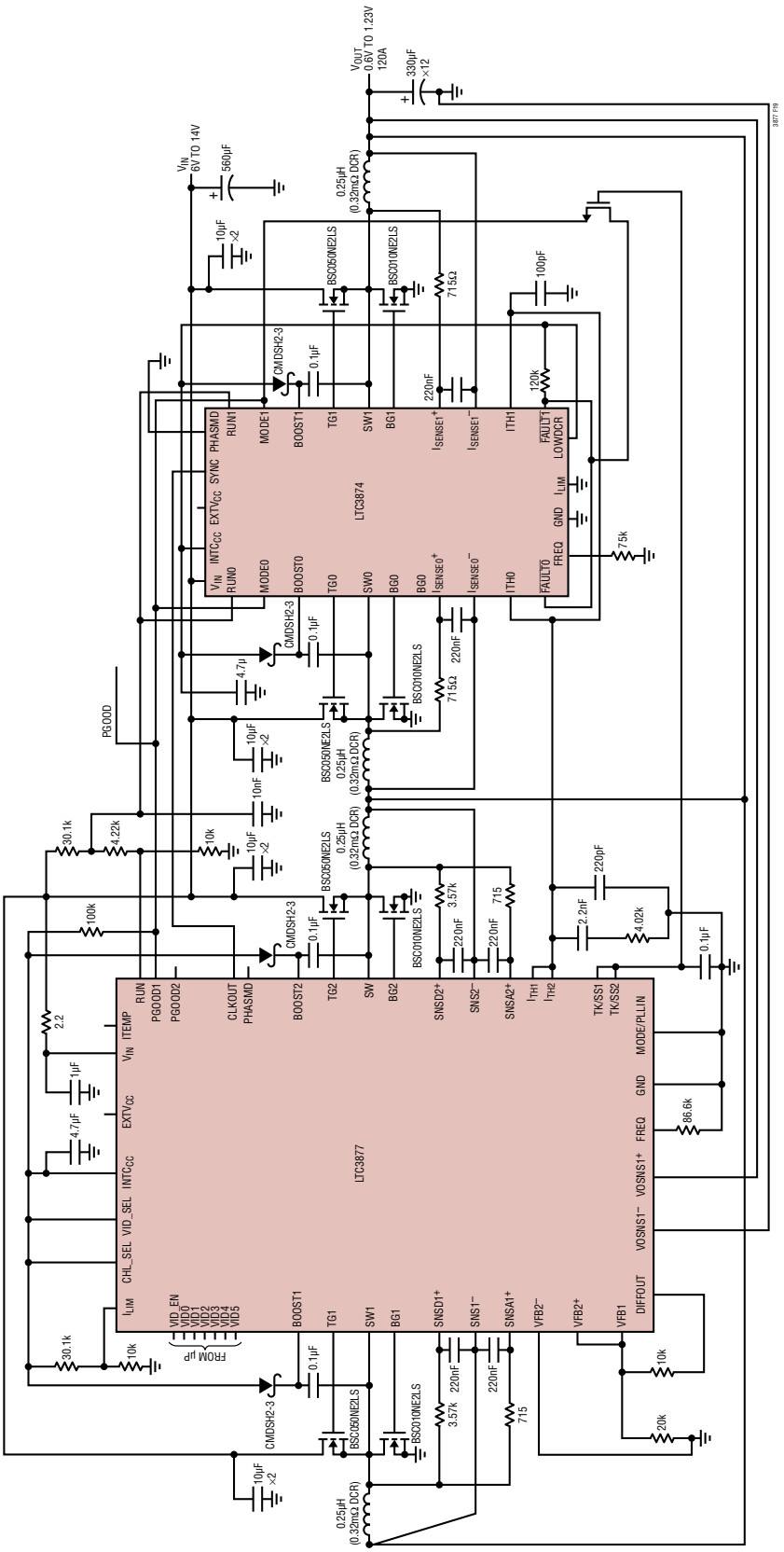
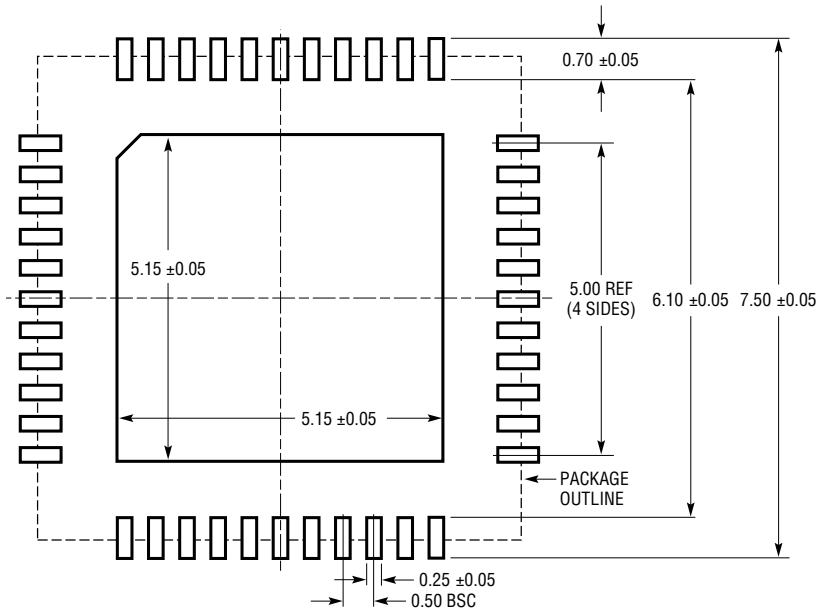


Figure 18. Four Phase, 120A VID-Controlled Converter Using LTC3877 and LTC3874

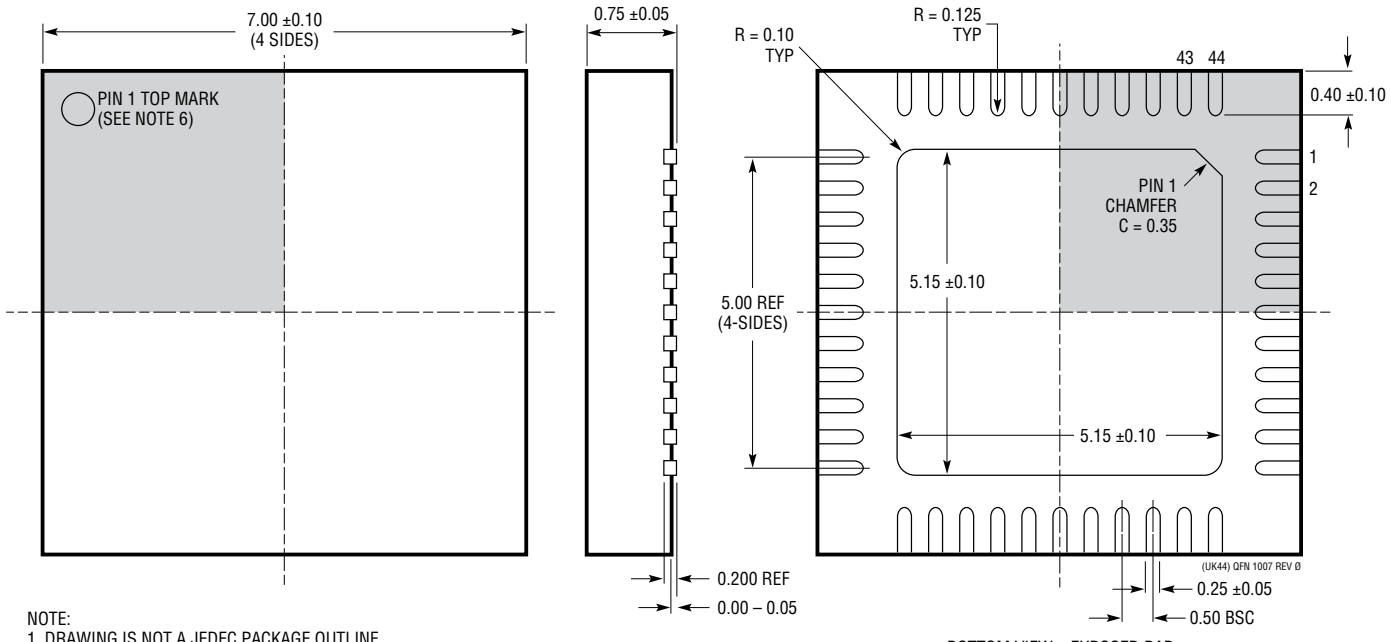
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UK Package
44-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1763 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

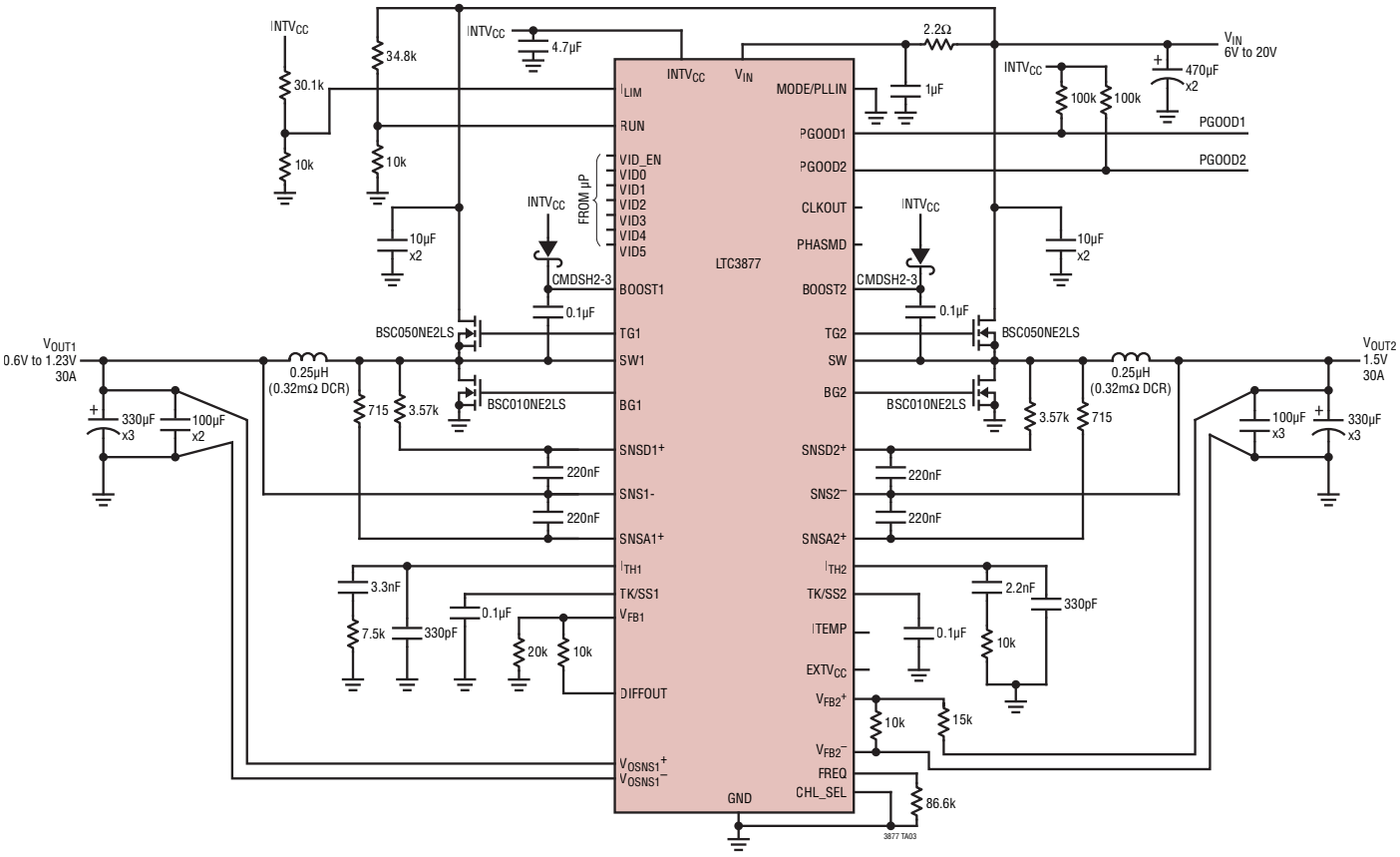


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE.
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Dual Output, 400kHz Converter with Fixed and VID-Controlled Outputs



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4630/LTM4630-1	Dual 18A or Single 36A DC/DC µModule Regulator	Accurate Phase-to-Phase Current Sharing, Fast Transient Response, 4.5V≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 1.8V
LTC3774	Dual, Mulitphase Current Mode Synchronous Step-Down DC/DC Controller for Sub-Milliohm DCR Sensing with Redundancy Support	Operates with Power Blocks, DrMOS Devices or External Drives/MOSFETs, 4.5V ≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 3.5V
LTC3855	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Differential Output Sensing and DCR Temperature Compensation	PLL Fixed Frequency 250kHz to 770kHz, 4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 12V
LTC3838/LTC3838-1/ LTC3838-2	Dual, Fast, Accurate Step- Down Controlled On-Time DC/DC Controller with Differential Output Sensing	Synchronizable Fixed Frequency 200kHz to 2MHz, 4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5.5V
LTC3861/LTC3861-1	Dual, Multiphase, Synchronous Step-Down Voltage Mode DC/DC Controller with Diff Amp and Accurate Current Sharing	Operates with Power Blocks, DrMOS Devices or External Drivers/MOSFETs, 3V ≤ V_{IN} ≤ 24V
LTC3856	Single Output, Dual Channel Synchronous Step-Down DC/DC Controller with Differential Output Sensing	Phase-Lockable Fixed 250kHz to 770kHz Frequency, 4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5V
LTC3875	Dual, Multiphase Synchronous Current Mode Controller with Sub-mΩ DCR Sensing and Temperature Compensation	4.5V ≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 3.5V/5V Excellent Current Share When Paralleled
LTC3866	Single Output Current Mode Synchronous Controller with Sub-mΩ DCR Sensing	4.5V≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 3.5V Fixed 250kHz to 770kHz Frequency
LTC3874	PolyPhase Step-Down Synchronous Slave Controller with Sub-mΩ DCR Sensing	Phase Extender for High Phase Count Voltage Rails, Accurate Phase-to-Phase Current Sharing, Sub-mΩ DCR Current Sensing, 4.5V ≤ V_{IN} ≤ 38V

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