



**THE DATASHEET OF
FS32V234CTN1VUB**



S32V234

S32V234 Data Sheet

Features

- ARM® Cortex®-A53, 64-bit CPU
 - Up to 1000 MHz Quad ARM Cortex-A53
 - 32 KB/32 KB I-/D- L1 Cache
 - NEON MPE co-processor
 - Dual precision FPU
 - 2 clusters with 2 CPUs and 256 KB L2 cache each
 - Memory Management Unit
 - GIC Interrupt Controller
 - ECC/parity error support for its memories
 - Generic timers
 - Fault encapsulation by hardware for redundant executed application software on multiple core cluster
- ARM Cortex-M4, 32-bit CPU
 - Up to 133 MHz
 - 16 KB/16 KB I-/D- L1 Cache
 - 32+32 KB tightly coupled memory (TCM)
 - ECC/parity support for its memories
- Clocks
 - Phase Locked Loops (PLLs)
 - 1 external crystal oscillator (FXOSC)
 - 1 FIRC oscillator
- System protection and power management features
 - Flexible run modes to consume low power based on application needs
 - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
 - Power gating of unused A53 cores and GPU
 - Low and high voltage warning and detect
 - Hardware CRC module to support fast cyclic redundancy checks (CRC)
 - 120-bit unique chip identifier
 - Hardware watchdog
 - eDMA controller with 32 channels (with DMAMUX)
 - Extended Resource Domain Controller
- Safety concept
 - ISO 26262, ASIL level target
 - Measures to detect faults in memory and logic
 - Measures to detect single point and latent faults
 - Quantitative out of context analysis of functional safety (FMEDA) tailored to application specifics
 - Safety manual and FMEDA report available
- Security
 - CSE with 16 KB of on-chip Secure RAM and ROM.
 - ARM TrustZone (TZ) architecture support
 - Boot from NOR flash with AES-128 (CTR)
 - On-Chip One-Time Programmable element Controller (OCOTP_CTRL) with on chip electrical fuse array.
 - System JTAG Controller (SJC)
- Debug functionality
 - Standard JTAG and Compact JTAG
 - 16-bit Trace port, Serial Wire Output port
- Timers
 - General purpose timers (FTM)
 - Two Periodic Interrupt Timer (PIT)
 - IEEE 1588 Timers (part of Ethernet Subsystem)
- Analog
 - 1x 12-bit 1.8 V SAR ADC with self-test
- Communications
 - UART(w/ LIN2.11)
 - Serial peripheral interface (SPI)
 - I2C blocks
 - PCI express 2.0 with endpoint and root complex support
 - LFAST serial link
 - 1 GBit Ethernet with PTP IEEE 1588
 - FD-CAN
 - FlexRay Dual Channel, Version 2.1 RevA

- Memory interfaces
 - 32-bit DRAM Controller with support for LPDDR2/DDR3/DDR3L - Data rate of up to 1066 MT/s at 533 MHz clock frequency with ECC (SEC-DED-TED) triple error detection support for subregion
 - QuadSPI supporting Execute-In-Place (XIP)
 - Boot flash fault detection and correction using two-dimensional parity.
 - Triple fault detection and single fault correction scheme for external DDR-RAM including address/page fault detection.
- Video input interfaces, Image processing, graphics processing, display
 - Display Control Unit (2D-ACE) with 24-bit RGB, GPU frame buffer decoding
 - GPU GC3000 with frame buffer compression
 - 2x VIU (Video interface unit) for camera input
 - 2x MIPICSI2 with four lanes for camera input (support 1080 pixel @ 30 fps)
 - Image signal processor (ISP), supporting 2x1 or 1x2 megapixel @ 30 fps and 4x2 megapixel for subset of functions (exposure control, gamma correction)
 - 2x APEX2-CL Image cognition processor. APEX-642CL comprises two Array Processing Unit (APU) cores configurable as single SIMD engine with 64 16-bit Computational Units (CU), or configurable as two core MIMD engines with 32 16-bit CUs each.
 - CUs are comprised of four Functional Units: 16-bit Multiplier, Load Store Unit, ALU, and Shifter
 - JPEG video decoder (8/12-bit)
 - H.264 video decoder (8/10/12-bit), High-intra and constrained baseline formats
 - H.264 video encode (8/10/12-bit), High-intra only
 - Fast DMA for data transfers between DRAM and System RAM with CRC
- Human-Machine Interface (HMI)
 - GPIO pins with interrupt support, DMA request capability, digital glitch filter
 - Configurable slew rate and drive strength on all output pins
- System RAM
 - 4 MB On-Chip System RAM with ECC

Table of Contents

| | | | | | |
|---------|--|----|---------|---|----|
| 1 | Block diagram..... | 5 | 6.4 | DDR SDRAM Specific Parameters (DDR3, DDR3L, and LPDDR2)..... | 31 |
| 2 | Family comparison..... | 5 | 6.4.1 | DDR3 and DDR3L timing parameters | 31 |
| 2.1 | Feature Set..... | 5 | 6.4.2 | DDR3 and DDR3L read cycle..... | 33 |
| 3 | Ordering parts..... | 8 | 6.4.3 | DDR3 and DDR3L write cycle..... | 34 |
| 3.1 | Ordering information..... | 8 | 6.4.4 | LPDDR2 timing parameter..... | 35 |
| 4 | General..... | 9 | 6.4.5 | LPDDR2 read cycle..... | 37 |
| 4.1 | Operation above maximum operating conditions..... | 9 | 6.4.6 | LPDDR2 write cycle..... | 38 |
| 4.2 | Recommended operating conditions..... | 9 | 6.5 | Communication modules..... | 39 |
| 4.3 | Power Management Controller (PMC) electrical specifications..... | 10 | 6.5.1 | DSPI timing..... | 39 |
| 4.4 | Power consumption..... | 12 | 6.5.2 | Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC)..... | 43 |
| 4.5 | Electrostatic discharge (ESD) specifications..... | 13 | 6.5.2.1 | SDR mode timing specifications..... | 43 |
| 4.6 | Electromagnetic Compatibility (EMC) specifications..... | 13 | 6.5.2.2 | DDR mode timing specifications..... | 45 |
| 4.7 | PCB routing guidelines..... | 14 | 6.5.3 | LFAST electrical characteristics..... | 48 |
| 5 | I/O parameters..... | 15 | 6.5.3.1 | LFAST interface timing diagrams..... | 48 |
| 5.1 | General purpose I/O parameters..... | 15 | 6.5.3.2 | LFAST Interface electrical characteristics..... | 49 |
| 5.1.1 | GPIO speed at various voltage levels..... | 15 | 6.5.4 | FlexRay..... | 50 |
| 5.1.2 | DC electrical specifications..... | 17 | 6.5.4.1 | FlexRay timing parameters..... | 50 |
| 5.2 | DDR pads..... | 18 | 6.5.4.2 | TxEN..... | 50 |
| 5.2.1 | DDR3 mode..... | 18 | 6.5.4.3 | TxD..... | 51 |
| 5.2.1.1 | DDR3 mode DC electrical specifications..... | 18 | 6.5.4.4 | RxD..... | 52 |
| 5.2.2 | DDR3L mode..... | 19 | 6.5.5 | Ethernet Controller (ENET) Parameters..... | 53 |
| 5.2.2.1 | DDR3L mode DC electrical specifications..... | 19 | 6.5.5.1 | Ethernet Switching Specifications..... | 53 |
| 5.2.3 | LPDDR2 mode..... | 19 | 6.5.5.2 | Receive and Transmit signal timing specifications for RMIi interfaces..... | 53 |
| 5.2.3.1 | LPDDR2 mode DC electrical specifications..... | 19 | 6.5.5.3 | Receive and Transmit signal timing specifications for MII interfaces..... | 54 |
| 5.3 | Boot Configuration Pins Specification..... | 20 | 6.5.5.4 | Receive and Transmit signal timing specifications for RGMII interfaces..... | 56 |
| 6 | Peripheral operating requirements and behaviors..... | 20 | 6.5.5.5 | MII/RMIi Serial Management channel timing (MDC/MDIO)..... | 57 |
| 6.1 | Analog modules..... | 20 | 6.5.6 | PCI Express specifications..... | 58 |
| 6.1.1 | ADC electrical specifications..... | 20 | 6.5.7 | IIC timing..... | 59 |
| 6.1.1.1 | Input equivalent circuit..... | 21 | 6.5.8 | LINFlex timing..... | 60 |
| 6.1.2 | Thermal Monitoring Unit (TMU)..... | 23 | 6.6 | Display modules..... | 61 |
| 6.2 | Clocks and PLL interfaces modules..... | 23 | 6.6.1 | Display Control Unit (2D-ACE) Parameters..... | 61 |
| 6.2.1 | Main oscillator electrical characteristics..... | 23 | 6.6.1.1 | Interface to TFT panels..... | 61 |
| 6.2.2 | 48 MHz FIRC electrical characteristics..... | 24 | | | |
| 6.2.3 | PLL electrical specifications..... | 24 | | | |
| 6.2.4 | DFS electrical specifications..... | 25 | | | |
| 6.2.5 | LFAST PLL Electrical Specifications..... | 25 | | | |
| 6.3 | Memory interfaces..... | 26 | | | |
| 6.3.1 | QuadSPI AC specifications..... | 26 | | | |

| | | | | | |
|---------|--|----|------|--|----|
| 6.6.1.2 | Interface to TFT LCD Panels—Pixel Level Timings..... | 62 | 7 | Thermal attributes..... | 75 |
| 6.6.1.3 | Interface to TFT LCD panels—access level..... | 63 | 7.1 | Thermal attributes..... | 75 |
| 6.6.2 | Video input unit (VIU) timing specifications..... | 64 | 8 | Dimensions..... | 76 |
| 6.6.3 | MIPICSI2 D-PHY electrical and timing parameters.... | 65 | 8.1 | Obtaining package dimensions | 76 |
| 6.6.3.6 | NOTICE OF DISCLAIMER..... | 68 | 9 | Pinouts..... | 76 |
| 6.7 | Debug specifications..... | 69 | 9.1 | Package pinouts and signal descriptions..... | 76 |
| 6.7.1 | JTAG interface timing..... | 69 | 10 | Reset sequence..... | 76 |
| 6.7.2 | Debug trace timing specifications..... | 73 | 10.1 | Reset sequence duration..... | 76 |
| 6.8 | Wakeup Unit (WKPU) AC specifications..... | 74 | 10.2 | Boot performance matrix..... | 77 |
| 6.9 | RESET pin glitch filter specifications..... | 74 | 10.3 | Reset sequence description..... | 78 |
| 6.10 | External interrupt timing (IRQ pin)..... | 74 | 11 | Power sequencing requirements..... | 80 |
| | | | 12 | Revision history..... | 81 |

1 Block diagram

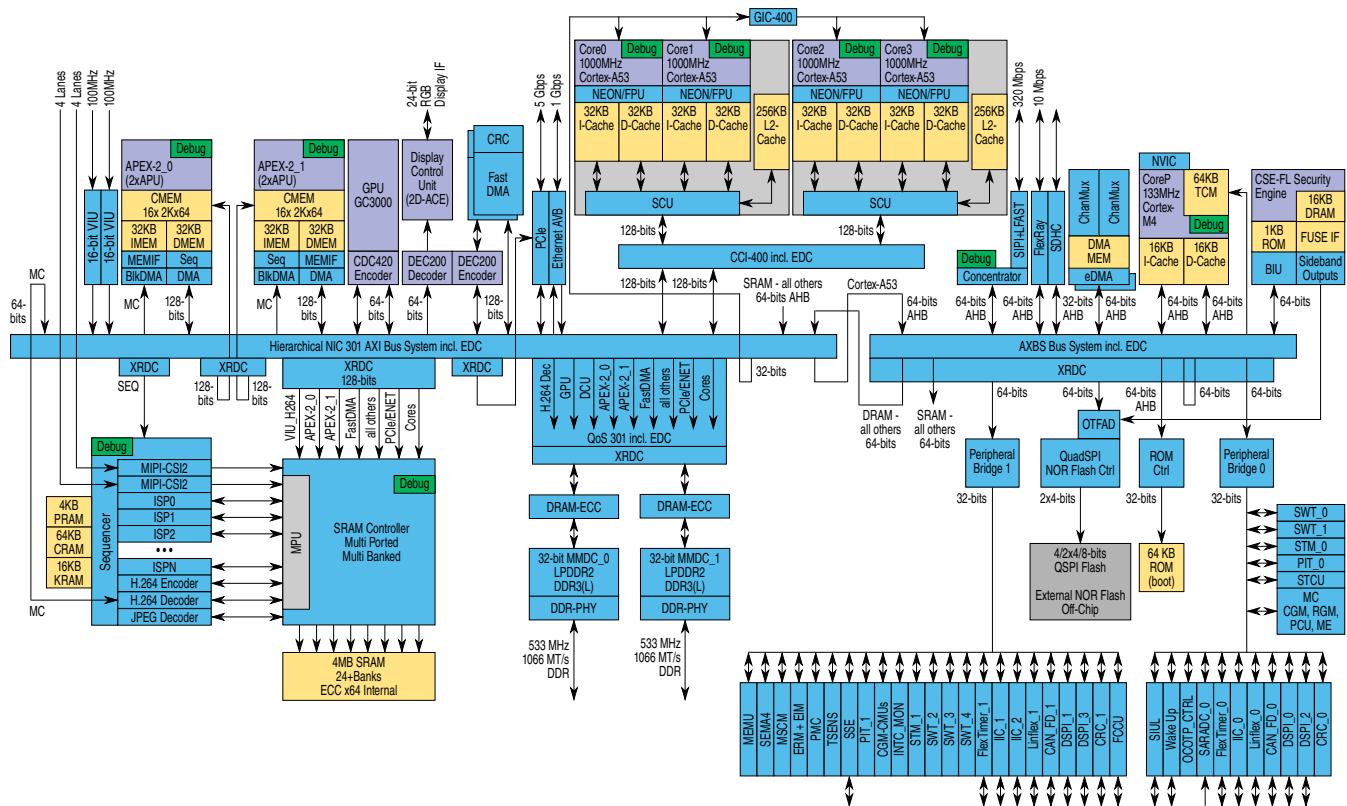


Figure 1. Block diagram

2 Family comparison

2.1 Feature Set

This family of devices supports the following features:

Table 1. Feature Set

| Feature | S32V234 | S32V232 |
|---------------------|---|---|
| ARM Cortex-A53 Core | <ul style="list-style-type: none"> Up to 1000 MHz Quad ARM Cortex-A53 32 KB/32 KB I-/D- L1 Cache NEON MPE co-processor Dual precision FPU 256 KB L2 Cache per cluster MMU GIC interrupt controller | <ul style="list-style-type: none"> Up to 1000 MHz Dual ARM Cortex-A53 (single cluster) The remaining features are same as S32V234 |

Table continues on the next page...

Table 1. Feature Set (continued)

| Feature | S32V234 | S32V232 |
|--|---|---|
| | <ul style="list-style-type: none"> ECC/parity error support for its memories Generic timers | |
| ARM Cortex-M4 Core | <ul style="list-style-type: none"> Up to 133 MHz 16 KB/16 KB I-/D- L1 Cache 32+32 KB tightly coupled memory (TCM) ECC/parity support for its memories | <ul style="list-style-type: none"> Same as S32V234 |
| Clocks | <ul style="list-style-type: none"> Phase Locked Loops (PLLs) 1 external crystal oscillators (FXOSC) 1 FIRC | <ul style="list-style-type: none"> Same as S32V234 |
| System, protection and power management features | <ul style="list-style-type: none"> Flexible run modes to consume lower power based on application needs. Peripheral clock enable registers can disable clocks to unused modules, thereby reducing currents Low and high voltage warning and detect Hardware CRC module to support fast cyclic redundancy checks (CRC) 120-bit unique chip identifier Hardware watchdog Safe eDMA controller with 32 channels (with DMAMUX) Extended Resource Domain Controller | <ul style="list-style-type: none"> Same as S32V234 |
| Safety concept | <ul style="list-style-type: none"> ISO 26262, ASIL level target as per safety concept Measures detecting faults in memory and logic Measures to detect single point and latent faults Quantitative out of context analysis of functional safety (FMEDA) tailored to application specifics Safety manual and FMEDA report available Boot flash authentication and fault detection and correction using AES-128 and two-dimensional parity. Double and triple fault detection and single fault correction scheme for external DDR-RAM including address/page fault detection. Fault encapsulation by hardware for redundant executed application software on multiple core cluster. Structural software based self test routines providing high diagnostic coverage. | <ul style="list-style-type: none"> Same as S32V234 |
| Debug | <ul style="list-style-type: none"> Standard JTAG 16-bit Trace port, Serial Wire Output port | <ul style="list-style-type: none"> Same as S32V234 |
| Timers | <ul style="list-style-type: none"> General purpose timers (FTM) | <ul style="list-style-type: none"> Same as S32V234 |

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Table 1. Feature Set (continued)

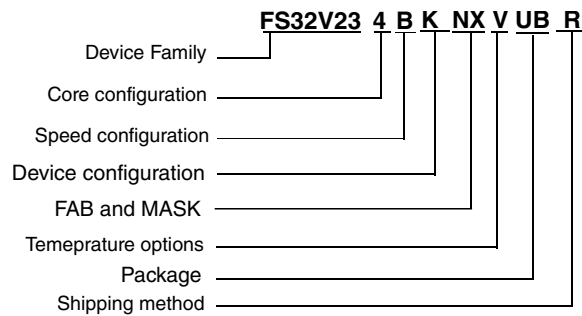
| Feature | S32V234 | S32V232 |
|--|--|--|
| | <ul style="list-style-type: none"> • Two Periodic Interrupt Timer (PIT) • IEEE 1588 Timers (part of Ethernet Subsystem) | |
| Communications | <ul style="list-style-type: none"> • UART(w/ LIN2.1) • Serial peripheral interface (SPI) • I2C blocks • PCI express 2.0 with endpoint and root complex support • LFAST serial link • 1 GBit Ethernet with PTP IEEE 1588 • FD-CAN • Flexray Dual Channel, Version 2.1 RevA | <ul style="list-style-type: none"> • Same as S32V234 |
| Memory Interfaces | <ul style="list-style-type: none"> • 32-bit DRAM Controller with support for LPDDR2/DDR3/DDR3L - Data rate of up to 1066 MT/s at 533 MHz clock frequency with ECC (SEC-DED-TED) single error correction, double error detection, and triple error detection support for subregion • Dual QuadSPI supporting Execute-In-Place (XIP) | <ul style="list-style-type: none"> • Same as S32V234 |
| Video input interfaces, Image processing, graphics processing, display | <ul style="list-style-type: none"> • Display Control Unit (2D-ACE) with 24-bit RGB, GPU framebuffer decoding • GPU GC3000 with frame buffer compression • 2x Video interface unit (VIU) for camera input • 2x CSI with 4 lanes for camera input (support 1080p @ 30fps) • Image signal processor (ISP), supporting 2x1 or 1x2 MPixel @ 30fps and 4x1 MPixel for subset of functions (exposure control, gamma correction) • 2x APEX2-CL Image cognition processor • JPEG video decoder (8/12-bit) • H.264 video decoder (8/10/12-bit), High-intra and constrained baseline formats • H.264 video encoder (8/10/12-bit), I-frames only • Safe Fast DMA for data transfers between DRAM and System RAM with CRC | <ul style="list-style-type: none"> • Same as S32V234 |
| Analog | <ul style="list-style-type: none"> • 1x 12-bit SAR ADC with self-test | <ul style="list-style-type: none"> • Same as S32V234 |
| Human-Machine Interface (HMI) | <ul style="list-style-type: none"> • SIUL, GPIO pins with interrupt support, DMA request capability, digital glitch filter. • Configurable slew rate and drive strength on all output pins | <ul style="list-style-type: none"> • Same as S32V234 |
| System RAM | <ul style="list-style-type: none"> • 4 MB On-Chip System RAM with ECC | <ul style="list-style-type: none"> • 3 MB On-Chip System RAM with ECC |
| Power Consumption | <ul style="list-style-type: none"> • Run modes: | <ul style="list-style-type: none"> • Same as S32V234 |

Table 1. Feature Set

| Feature | S32V234 | S32V232 |
|---------|--|---------|
| | <ul style="list-style-type: none"> Frequency scaling and clock gating for processing blocks and peripherals in run mode | |

3 Ordering parts

3.1 Ordering information



| | | | | | |
|---------------------------------------|--|--------------------------------------|--|----------------|---|
| Temperature options | Core configuration | Shipping method | Speed configuration | Package | FAB and MASK |
| C = -40 to 105°C V = -40 to 125 °C | 2 = Dual Arm Cortex - A53 4 = Quad Arm Cortex - A53 | R = Tape and reel (blank) = Trays | B = Arm Cortex - A53 @800 MHz C = Arm Cortex - A53 @1 GHz | UB =621 FBGA | NX = X is mask identifier e.g. 1, 2 etc |

Device configuration*

| | ISP | 3D GPU | CSE | Low power (leakage based) | eIQ Auto |
|---|-----|--------|-----|---------------------------|-------------|
| K | Yes | No | Yes | No | K becomes Q |
| L | Yes | No | Yes | Yes | L becomes R |
| M | Yes | Yes | No | No | M becomes S |
| O | Yes | Yes | Yes | No | O becomes T |
| J | Yes | No | No | Yes | J becomes U |

* All combinations are not orderable

NOTE

Not all combinations are orderable. For the latest information on orderable parts check [https:// www.nxp.com/s32v234](https://www.nxp.com/s32v234) Buy/ Parametrics section.

4 General

4.1 Operation above maximum operating conditions

Table 2. Operation above maximum operating conditions

| 1.8 V DGO Voltage Domain | | | |
|---------------------------------|--------|------------|------------|
| Electrical Specifications | Value | Conditions | Junct Temp |
| Absolute Maximum Supply Voltage | 3.0 V | < 60 s | 25 °C |
| Absolute Maximum Supply Voltage | 2.3 V | < 10 hr | 25 °C |
| Core Voltage Domain | | | |
| Electrical Specifications | Value | Conditions | Junct Temp |
| Absolute Maximum Supply Voltage | 1.29 V | < 60 s | 25 °C |
| Absolute Maximum Supply Voltage | 1.1 V | < 10 hr | 25 °C |
| 3.3 V DGO Voltage Domain | | | |
| Electrical Specifications | Value | Conditions | Junct Temp |
| Absolute Maximum Supply Voltage | 4.95 V | < 60 s | 25 °C |
| Absolute Maximum Supply Voltage | 4.29 V | < 10 hr | 25 °C |

4.2 Recommended operating conditions

Table 3. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------------|---|------------|-------|-------|------|
| V _{DD_GPI00} | 3.3 V I/O segment GPIO00 supply voltage | — | 3.15 | 3.6 | V |
| V _{DD_GPIO<n=1,2>} | 1.8 V input/output supply voltage | — | 1.71 | 1.95 | V |
| V _{DD_HV_IO_VIU0} | 3.3 V input/output supply voltage | — | 3.15 | 3.6 | V |
| V _{DD_HV_IO_VIU1} | | | | | |
| V _{DD_HV_IO_DIS} | | | | | |
| V _{DD_HV_IO_FL A} | | | | | |
| V _{DD_HV_IO_ETH} | 1.5 V I/O supply voltage | — | 1.425 | 1.575 | V |
| | 1.8 V I/O supply voltage | — | 1.71 | 1.95 | V |
| | 2.5 V I/O supply voltage | — | 2.375 | 2.625 | V |

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|--|------------|-------|------------------|------|
| | 3.3 V I/O supply voltage | — | 3.15 | 3.6 | V |
| V _{SS} | Common ground voltage ¹ | — | 0 | 0 | V |
| V _{DD_LV_CORE_SOC} , V _{DD_LV_CORE_ARM} , V _{DD_LV_CORE_GPU} | 1.0 V core domain supply voltage ² | — | 0.95 | 1.05 | V |
| V _{DD_HV_CSI} | 1.8 V supply voltage (for MIPICSI2 D PHY) | — | 1.71 | 1.95 | V |
| V _{DD_LV_CSI} | 1.0 V supply voltage (for MIPICSI2 D PHY) | — | 0.95 | 1.05 | V |
| V _{DD_HV_PLL} , V _{DD_HV_LFASTPLL} , V _{DD_HV_FXOSC} , V _{DD_HV_PMC} , V _{DDIO_LFAST} , V _{DD_HV_EFUSE} , V _{DD_HV_DDR} | 1.8 V supply voltage (for analog circuits, PLLs) | — | 1.71 | 1.95 | V |
| V _{DD_LV_PLL} V _{DD_LV_POST} | 1.0 V supply voltage (for analog circuits, PLLs) | — | 0.95 | 1.05 | V |
| V _{REFH_ADC} | 1.8 V ADC high reference voltage | — | 1.71 | 1.95 | V |
| V _{DD_HV_ADV} | 1.8 V ADC supply voltage | — | 1.71 | 1.95 | V |
| V _{SS_HV_ADV} | ADC ground and low reference voltage | — | 0 | 0 | V |
| V _{REFL_ADC} | 1.8 V ADC supply ground | — | 0 | 0 | V |
| V _{DD_DDR_IO} | DDR I/O supply voltage LPDDR2 | — | 1.14 | 1.30 | V |
| | DDR I/O supply voltage DDR3 | — | 1.425 | 1.575 | V |
| | DDR I/O supply voltage DDR3L | — | 1.283 | 1.45 | V |
| P _{CIE_VP} | PCIe supply voltages | — | 0.95 | 1.05 | V |
| P _{CIE_VPH} | | — | 1.71 | 1.95 | V |
| T _A | Ambient temperature | — | -40 | 105 ³ | °C |
| T _J | Junction temperature under bias | — | -40 | 125 | °C |
| T _{STG} | Storage temperature range | — | -55 | 150 | °C |
| TV _{DD} | Supply ramp rate for all supplies on the device | — | 0.05 | 25 | V/ms |

1. All the grounds viz. V_{SS}, V_{SS_FXOSC}, and V_{SS_HV_ADV} are tied together at the package level.
2. V_{DD_LV_CORE_SOC}, V_{DD_LV_CORE_ARM}, and V_{DD_LV_CORE_GPU} supply balls should all be connected together to one power plane and one regulator to avoid voltage level differences. If the GPU is power gated as it is not used, the V_{DD_LV_CORE_GPU} supply balls have to be statically connected to the ground plane. If the second ARM CPUs per cluster is power gated as they are not used, the V_{DD_LV_CORE_ARM} supply balls have to be statically connected to the ground plane.
3. Maximum ambient temperature requires management of the heat dissipation to ensure the device junction temperature does not exceed the maximum.

4.3 Power Management Controller (PMC) electrical specifications

PMC is composed of the following blocks:

- Low voltage detector (LVD_33_PMC) for 3.3 V VDD_GPIO0 supply (GPIO segment and PMC) and Low Voltage Detector for FIRC (VDD_HV_FXOSC)
- Low voltage detector (LVD_18) for VDD_HV_PMC
- Low voltage detector (LVD_18) for VDD_HV_FXOSC
- High voltage detector (HVD_18) for VDD_HV_PMC
- Low voltage detector (LVD_CORE) for VDD_LV_CORE_SOC
- High voltage detector (HVD_CORE) for VDD_LV_CORE_SOC
- Power on Reset (POR)

Table 4. PMC electrical specifications

| Supply | Parameter | Conditions | Threshold | Min | Typical | Max | Status during power-up | Unit |
|-----------------|----------------------------------|------------|------------------|------|---------|------|------------------------|------|
| VDD_LV_CORE_SOC | low voltage monitoring | Native | VTL ¹ | 836 | 880 | 924 | Enabled | mV |
| | | | VTH ² | 850 | 895 | 940 | | |
| | | Trimmed | VTL | 896 | 910 | 924 | | |
| | | | VTH | 911 | 925 | 946 | | |
| VDD_LV_CORE_SOC | high voltage monitoring | Trimmed | VTL | 1049 | 1065 | 1093 | Disabled | mV |
| | | | VTH | 1064 | 1080 | 1093 | | |
| VDD_HV_PMC | PMC supply low voltage monitor | Native | VTL | 1511 | 1590 | 1670 | Enabled | mV |
| | | | VTH | 1525 | 1605 | 1685 | | |
| | | Trimmed | VTL | 1620 | 1650 | 1680 | | |
| | | | VTH | 1635 | 1665 | 1695 | | |
| VDD_HV_PMC | PMC supply high voltage monitor | Trimmed | VTL | 2004 | 2045 | 2086 | Disabled | mV |
| | | | VTH | 2019 | 2060 | 2101 | | |
| VDD_GPIO0 | low voltage monitor | Native | VTL | 2727 | 2870 | 3014 | Enabled | mV |
| | | | VTH | 2746 | 2890 | 3035 | | |
| | | Trimmed | VTL | 2857 | 2915 | 2973 | | |
| | | | VTH | 2876 | 2935 | 2994 | | |
| VDD_HV_FXOSC | FXOSC supply low voltage monitor | Native | VTL | 1511 | 1590 | 1670 | Enabled | mV |
| | | | VTH | 1525 | 1605 | 1685 | | |
| | | Trimmed | VTL | 1620 | 1650 | 1680 | | |
| | | | VTH | 1635 | 1665 | 1695 | | |
| PMC_BGREF | PMC Band Gap Reference value | Trimmed | – | 1176 | 1200 | 1224 | Enabled | mV |

1. Lower threshold/assert point
2. Upper threshold/release point

4.4 Power consumption

The following table shows the power consumption data. These specifications are subject to change per device characterization.

Table 5. Power consumption

| Parameter | Description | Max Values | |
|--------------------------------------|---|----------------------|---------------------|
| | | 125C T _j | 105C T _j |
| VDD_LV_CORE (Static) ^{1, 2} | S32V234BL Device in reset | 3 A | 2.3 A |
| | S32V232BM Device in reset | 6.0 A | 4.5 A |
| | S32V234CO Device in reset | 6.4 A | 4.8 A |
| | S32V234CK Device in reset | 4.8 A | 3.5 A |
| | S32V232BL Device in reset | 2.7 A | 2.0 A |
| | S32V232CK Device in reset | 4.4 A | 3.2 A |
| VDD_LV_CORE (Dynamic) | 4x A53 CPU with Dhrystone MIPS running on each CPU @ 1 GHz ³ | 1.4 A | |
| VDD_HV_CSI | Current for both MIPICSI2 interfaces operating as per 1) RX Operation at 1.5 Gbps per MIPICSI2 2) MIPICSI2 not used (IP Powered and Disabled) | 1) 10 mA 2) 1 mA | |
| VDD_LV_CSI | Current for both MIPICSI2 interfaces operating as per 1) RX Operation at 1.5 Gbps per MIPICSI2 2) MIPICSI2 not used (IP Powered and Disabled) | 1) 40 mA 2) 13 mA | |
| VDD_HV_PLL | All five PLLs operating at 1 GHz VCO frequency | 35 mA | |
| VDD_HV_LFASTPLL | Use case: 1) PLL operating with 320 MHz (LFAST used) 2) PLL not operational (LFAST not used) | 1) 26 mA 2) .1 mA | |
| VDD_HV_FXOSC | Shared supply for FXOSC operating with 40 MHz crystal and FIRC oscillator | 5 mA | |
| VDD_HV_PMC | As per default usage (no use case differentiation) | 10 mA | |
| VDD_HV_EFUSE | Use case: 1) eFuse programming happening | 1) 10 mA | |

Table continues on the next page...

Table 5. Power consumption (continued)

| Parameter | Description | Max Values | |
|--------------|---|----------------------|---------------------|
| | | 125C T _j | 105C T _j |
| VDD_LV_PLL | All five PLLs operating at 1 GHz VCO frequency | 80 mA | |
| PCIE_VP | Use case: 1) 5 GHz operation (PCIe 2.0) 2) Reset/idle | 1) 80 mA 2) 30 mA | |
| PCIE_VPH | Use case: 1) 5 GHz operation (PCIe 2.0) 2) Reset/idle | 1) 50 mA 2) 20 mA | |
| VDD_HV_ADV | ADC operational | 1 mA | |
| VDD_REFH_ADC | Voltage reference for ADC | 80 μA | |

1. Data represented is at 125 °C T_j and 1.01 V vdd conditions
2. Includes SoC, GPU, and ARM supply combinations depending on use case description.
3. Adder to the static idd current component. 4xCortex A53 executing Dhrystone MIPS in AArch64 and the interconnect, System RAM, FastDMA, Cortex M4, peripheral bridges, FCCU, CSE, MEMU, PCIe, and STCU are clocked - static power consumption excluded.

4.5 Electrostatic discharge (ESD) specifications

Electrostatic discharges are applied to the pins of each sample in conformity with AEC-Q100-002/-011 to meet the HBM and CDM ratings described below.

Table 6. ESD ratings¹

| Symbol | Parameter | Conditions | Class | Max value ² | Unit |
|-----------------------|--|---|-------|------------------------|------|
| V _{ESD(HBM)} | Electrostatic discharge (Human Body Model) | T _A = 25 °C conforming to AEC-Q100-002 | H1C | 2000 | V |
| V _{ESD(CDM)} | Electrostatic discharge (Charged Device Model) | T _A = 25 °C conforming to AEC-Q100-011 | C3A | 500 | V |

1. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
2. Data based on characterization results, not tested in production.

4.6 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

4.7 PCB routing guidelines

DDR3/DDR3L PCB design

- CLK/Address/Commands
 - Route with 50 ohm controlled impedance and differential pair (CLK) with 100 ohm controlled impedance
 - Use Fly by topology in case of multiple memory components
 - Address and command lines Terminated to VTT with 50 ohm
 - Recommended to be referenced with Ground-plane or Power-plane
 - Address/Cmd to be routed within 66 mils with respect to CLK and to be matched from controller to memory; memory to memory as well
 - All traces to be routed in internal layers
 - Preference is to use only two layers for routing this group
 - Limit the via number to less than three

NOTE

The differential clock lines on the DDR3 interface should use AC termination scheme, with a 0.1 μ F series capacitor and referenced to DDR IO supply ($V_{DD_DDR_IO}$).

- Data/Strobe
 - Route with 50 ohm controlled impedance and differential pair (DQS strobe) with 100 ohm controlled impedance
 - Data to be routed within 33 mils with respect to respective strobe
 - To be referenced with Ground
 - All traces to be routed in internal layers
 - Strictly to be routed in only two layers
 - Avoid more than two vias

LPDDR2 PCB design

- CLK/Address/Commands
 - Route with 50 ohm controlled impedance and differential pair (CLK) with 100 ohm controlled impedance
 - To be referenced with Power, not Ground
 - Address/Cmd to be routed within 66 mils with respect to CLK and to be matched from controller to memory
 - All traces to be routed in internal layers and delay should be less than 150 ps
 - Preference is to use only two layers for routing this group
 - Limit the via number to less than three
- Data/Strobe
 - Route with 50 ohm controlled impedance and differential pair (DQS strobe) with 100 ohm controlled impedance

- Data to be routed within 33 mils with respect to respective strobe
- To be referenced with Ground
- All traces to be routed in internal layers and delay should be less than 150 ps
- Strictly to be routed in only two layers
- Avoid more than two vias

GPIO Interfaces

- QuadSPI
 - Put 22 ohm series termination on board when operating with SIUL2_MSCR n [DSE] 111
- TRACE
 - Put 22 ohm series termination on board when operating with SIUL2_MSCR n [DSE] 111
- ENET
 - Put 22 ohm series termination on board when operating with SIUL2_MSCR n [DSE] 111

5 I/O parameters

5.1 General purpose I/O parameters

5.1.1 GPIO speed at various voltage levels

NOTE

Rise/fall times numbers in Datasheet are guaranteed by design; to obtain actual rise/fall times parameters with specific packages and boards, use appropriate I/O IBIS model.

Table 7. GPIO rise/fall times (1.8 V range)

| Parameter | Symbol | Drive strength SIUL2_MSCR n [DSE] | Slew rate | Test conditions | Typ | Max | Unit |
|---|--------|--|--------------|--------------------|-----|------------------------|------|
| IO output transition time, rise/fall ¹ | tpr | 001 | slow fast | 15 pF Cload on pad | | 7.17/7.55 | ns |
| | | 010 | slow fast | | | 3.14/3.31 2.66/3.04 | |
| | | 011 | slow fast | | | 2.56/2.51 1.97/2.20 | |
| | | 100 | slow | | | 3.08/3.02 | |

Table continues on the next page...

Table 7. GPIO rise/fall times (1.8 V range) (continued)

| Parameter | Symbol | Drive strength SIUL2_MSCRn[D SE] | Slew rate | Test conditions | Typ | Max | Unit |
|-----------|--------|--|--------------|--------------------|-----|-----------|------|
| | | | fast | | | 2.59/2.58 | |
| | | 101 | slow | | | 2.56/2.42 | |
| | | | fast | | | 1.84/1.96 | |
| | | 111 | slow | | | 1.82/1.67 | |
| | | | fast | | | 1.13/1.24 | |

1. Max condition: wcs model, 0.9 V vddi, 1.62 V ovdd, and 125 °C. Input transition time is 120 ps.
 Slow slew rate means SIUL2_MSCRn[SRE] = '00', fast slew rate means SIUL2_MSCRn[SRE] = '11'

Table 8. GPIO rise/fall times (2.5 V range)

| Parameter | Symbol | Drive strength SIUL2_MSCRn[D SE] | Slew rate | Test conditions | Typ | Max | Unit |
|---|-----------|--|--------------|-----------------------|-----|-----------|------|
| IO output transition time, rise/fall ¹ | tpr | 001 | slow | 15 pF Cload on pad | | 7.41/8.22 | ns |
| | | | fast | | | 7.36/8.16 | |
| | | 010 | slow | | | 3.30/3.74 | |
| | | | fast | | | 2.76/3.38 | |
| | | 011 | slow | | | 3.44/3.04 | |
| | | | fast | | | 2.75/2.55 | |
| | | 100 | slow | | | 4.05/3.54 | |
| fast | 3.56/2.97 | | | | | | |
| 101 | slow | 3.39/2.93 | | | | | |
| | fast | 2.72/2.47 | | | | | |
| 111 | slow | 2.31/2.03 | | | | | |
| | fast | 1.80/1.75 | | | | | |

1. Max condition for tpr: wcs model, 0.9 V vddi, 2.25 V ovdd, and 125 °C. Input transition time is 125 ps. Slow slew rate means SIUL2_MSCRn[SRE] = '00', fast slew rate means SIUL2_MSCRn[SRE] = '11'

Table 9. GPIO rise/fall times (3.3 V range)

| Parameter | Symbol | Drive strength SIUL2_MSCRn[D SE] | Slew rate | Test conditions | Typ | Max | Unit |
|---|--------|--|--------------|-----------------------|-----|-----------|------|
| IO output transition time, rise/fall ¹ | tpr | 001 | slow | 15 pF Cload on pad | | 7.75/8.45 | ns |
| | | | fast | | | 7.65/8.39 | |
| | | 010 | slow | | | 3.49/3.89 | |
| | | | fast | | | 2.84/3.52 | |
| | | 011 | slow | | | 3.47/3.16 | |
| | | | fast | | | 2.90/2.73 | |

Table continues on the next page...

Table 9. GPIO rise/fall times (3.3 V range) (continued)

| Parameter | Symbol | Drive strength SIUL2_MSCRn[D SE] | Slew rate | Test conditions | Typ | Max | Unit |
|-----------|--------|--|--------------|--------------------|-----|-----------|------|
| | | 100 | slow | | | 4.09/3.58 | |
| | | | fast | | | 3.73/3.07 | |
| | | 101 | slow | | | 3.29/3.00 | |
| | | | fast | | | 2.68/2.37 | |
| | | 111 | slow | | | 2.23/2.18 | |
| | | | fast | | | 1.47/1.57 | |

1. Max condition for tpr: wcs model, 0.9 V vddi, 2.97 V ovdd, and 125 °C. Input transition time is 120 ps.
slow slew rate means SIUL2_MSCRn[SRE] = '00', fast slew rate means SIUL2_MSCRn[SRE] = '11'

NOTE

The maximum rise time for all GPIO pins is 1 ms. Input pins do not support hysteresis, therefore very slow ramps (like the ones generated by an RC circuit with a large RC value) can induce bounces in the input read state during the transition from logic low to logic high or vice versa.

5.1.2 DC electrical specifications**Table 10. DC electrical specifications**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|------------------------|---------------------------------|-----------------------|-------------------------|-----|----------|------|
| Voh | High-level output voltage | Ioh=-100 µA | ovdd ¹ -0.15 | — | — | V |
| Vol | Low-level output voltage | Iol=100 µA | — | — | 0.15 | V |
| Vihf | High-Level DC input voltage | — | 0.7*ovdd | — | ovdd | V |
| Vil | Low-Level DC input voltage | — | 0 | — | 0.2*ovdd | V |
| lin ² | Input current (no pull-up/down) | Vin = ovdd or 0 | — | — | 8 | µA |
| lin_33pu ² | Input current (33 kilohm PU) | Vin = 0 Vin = ovdd | — | — | 220 6 | µA |
| lin_50pu ² | Input current (50 kilohm PU) | Vin = 0 Vin = ovdd | — | — | 150 6 | µA |
| lin_100pu ² | Input current (100 kilohm PU) | Vin = 0 Vin = ovdd | — | — | 60 6 | µA |
| lin_100pd ² | Input current (100 kilohm PD) | Vin = 0 Vin = ovdd | — | — | 8 50 | µA |

1. ovdd is the IO supply for the pads.
2. Max condition: bcs model, 3.6 V, and 125 °C. These values are for I/O buffers.

NOTE

After bootup, application software should switch to manual voltage detect mode using VSEL_x settings of SRC_GPR14 register to ensure optimum performance of the GPIO pads. Please refer to SRC chapter in the Reference Manual for the register details.

Table 11. Current-draw Characteristics for DDR_VREF

| Symbol | Parameter | Min | Max | Unit |
|----------|---|-----|-----|------|
| DDR_VREF | Current-draw characteristics for DDR_VREF | — | 1 | mA |

5.2 DDR pads**5.2.1 DDR3 mode****5.2.1.1 DDR3 mode DC electrical specifications****Table 12. DDR3 mode DC electrical specifications**

| Parameter | Symbol | Test conditions | Min | Typ | Max | Unit |
|---|-----------------------|-----------------------------|------------|----------|------------|------------|
| High-level output voltage | Voh | Ioh=-100 μ A | 0.8*ovdd | — | — | V |
| Low-level output voltage | Vol | Iol=100 μ A | — | — | 0.2*ovdd | V |
| High-level DC input voltage | Vih (DC) | — | Vref + 0.2 | — | ovdd | V |
| High-level DC input voltage | Vil (DC) | — | ovss | — | Vref - 0.2 | V |
| Input reference voltage | Vref | — | 0.49*ovdd | 0.5*ovdd | 0.51*ovdd | V |
| Termination voltage ¹ | Vtt ² | — | — | 0.5*ovdd | — | V |
| Input current (no pullup/pulldown) ³ | Iin | Vi = 0 or ovdd | — | — | 5 | μ A |
| Pullup/pulldown impedance mismatch | MMpupd | 34 Ohm full strength driver | -10 | — | +10 | % |
| Driver 240 Ohm unit calibration resolution | Rres | — | — | — | 10 | Ω |
| Rkeep ⁴ | Pad keeper resistance | — | 20 | — | 50 | k Ω |

1. Vtt is expected to track ovdd/2.

2. Vtt is not applied directly to the device. Minimum and Maximum values are system dependant.

3. Typ condition: typ model, 1.5V, and 25 °C. Max condition: bcs model, 1.575V, and -40 °C. Min condition: wcs model, 1.425V, and 125 °C.

4. Typ condition: typ model, 1.5 V, and 25 °C, max condition: wcs model, 1.425 V, and 125 °C, min condition: bcs model, 1.575 V, and -40 °C.

5.2.2 DDR3L mode

5.2.2.1 DDR3L mode DC electrical specifications

Table 13. DDR3L mode DC electrical specifications

| Parameter | Symbol | Test conditions | Min | Typ | Max | Unit |
|---|-----------------------|--------------------|------------|----------|------------|------------|
| High-level output voltage | Voh | Ioh = -100 μ A | 0.8*ovdd | — | — | V |
| Low-level output voltage | Vol | Iol = 100 μ A | — | — | 0.2*ovdd | V |
| High-level DC input voltage | Vih (DC) | — | Vref + 0.2 | — | ovdd | V |
| High-level DC input voltage | Vil (DC) | — | ovss | — | Vref - 0.2 | V |
| Input reference voltage | Vref | — | 0.49*ovdd | 0.5*ovdd | 0.51*ovdd | V |
| Vref current draw | Icc-vref | — | — | — | 1 | mA |
| Termination voltage | Vtt ¹ | — | — | 0.5*ovdd | — | V |
| Input current (no pullup/pulldown) | Iin | Vi = 0 or ovdd | — | — | 5 | μ A |
| Pullup/pulldown impedance mismatch (full strength driver) | MMpupd | — | -10 | — | +10 | % |
| Driver unit (240 Ohm) calibration resolution | Rres | — | — | — | 10 | Ω |
| Rkeep | Pad keeper resistance | — | 20 | — | 50 | k Ω |

1. Vtt is not applied directly to the device. Minimum and Maximum values are system dependant.

5.2.3 LPDDR2 mode

5.2.3.1 LPDDR2 mode DC electrical specifications

Table 14. LPDDR2 mode DC electrical specifications

| Parameter | Symbol | Test conditions | Min | Typ | Max | Unit |
|---|----------|-----------------------------|-------------|----------|-------------|----------|
| High-level output voltage | Voh | Ioh = -100 μ A | 0.9*ovdd | — | — | V |
| Low-level output voltage | Vol | Iol = 100 μ A | — | — | 0.1*ovdd | V |
| Input reference voltage | Vref | — | 0.49*ovdd | 0.5*ovdd | 0.51*ovdd | V |
| High-level DC input voltage | Vih (DC) | — | Vref + 0.17 | — | ovdd | V |
| High-level DC input voltage | Vil (DC) | — | ovss | — | Vref - 0.17 | V |
| Input current (no pullup/pulldown) ¹ | Iin | Vi = ovdd or 0 | — | — | 5 | μ A |
| Pullup/pulldown impedance mismatch | MMpupd | 34 Ohm full strength driver | -15 | — | +15 | % |
| Driver 240 Ohm unit calibration resolution | Rres | — | — | — | 10 | Ω |

Table continues on the next page...

Table 14. LPDDR2 mode DC electrical specifications (continued)

| Parameter | Symbol | Test conditions | Min | Typ | Max | Unit |
|--------------------|-----------------------|-----------------|-----|-----|-----|------|
| Rkeep ² | Pad keeper resistance | — | 20 | — | 50 | kΩ |

1. Typ condition: typ model, 1.2 V, and 25 °C. Max condition: bcs model, 1.32 V, and -40 °C. Min condition: wcs model, 1.14 V, and 125 °C.
2. Typ condition: typ model, 1.2 V, and 25 °C, max condition: wcs model, 1.14 V, and 125 °C, min condition: bcs model, 1.32 V, and -40 °C.

5.3 Boot Configuration Pins Specification

Value driven on RCON and BOOTMOD pins should be stable for at least 1 μs after RESET pin is deasserted.

NOTE

External pull up/down resistors must be used on the BOOTMOD pins in order to ensure latching at the correct state.

NOTE

NXP would anticipate that most customers would use the boot from fuses option in a production environment. However, there is no reliability impact if the device is configured by RCON rather than fuses.

6 Peripheral operating requirements and behaviors

6.1 Analog modules

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

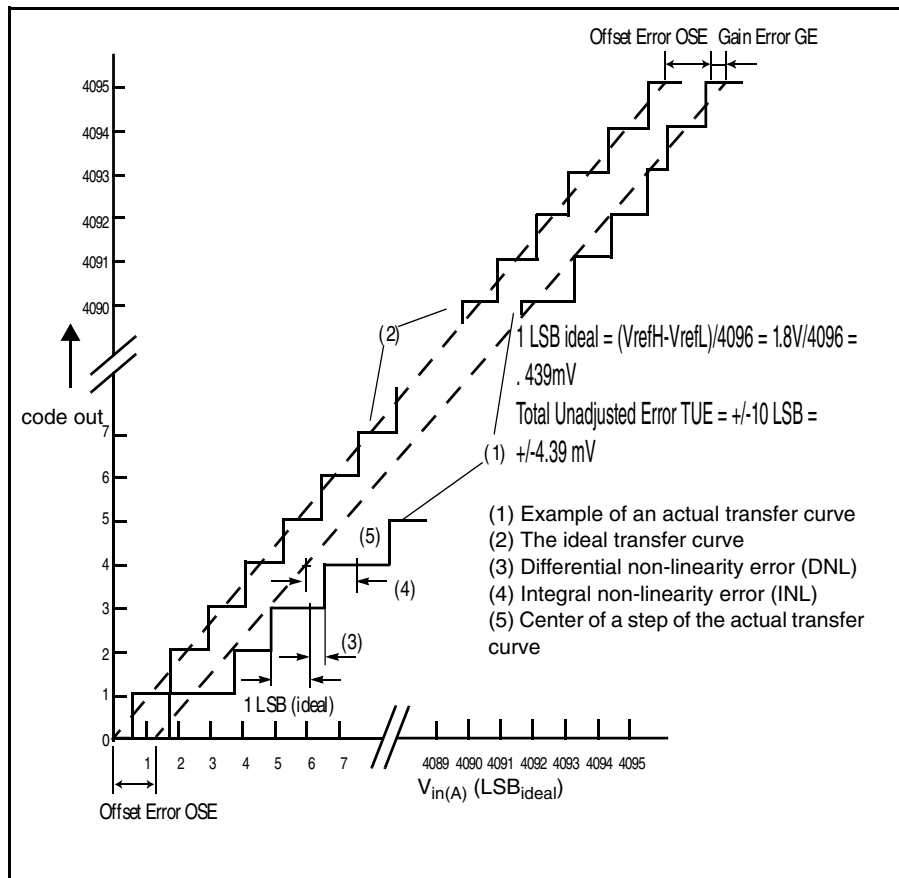


Figure 2. ADC characteristics and error definitions

NOTE

While measuring scaled supply voltages on ADC Channels, Maximum (+5/-10%) variation can be expected .

6.1.1.1 Input equivalent circuit

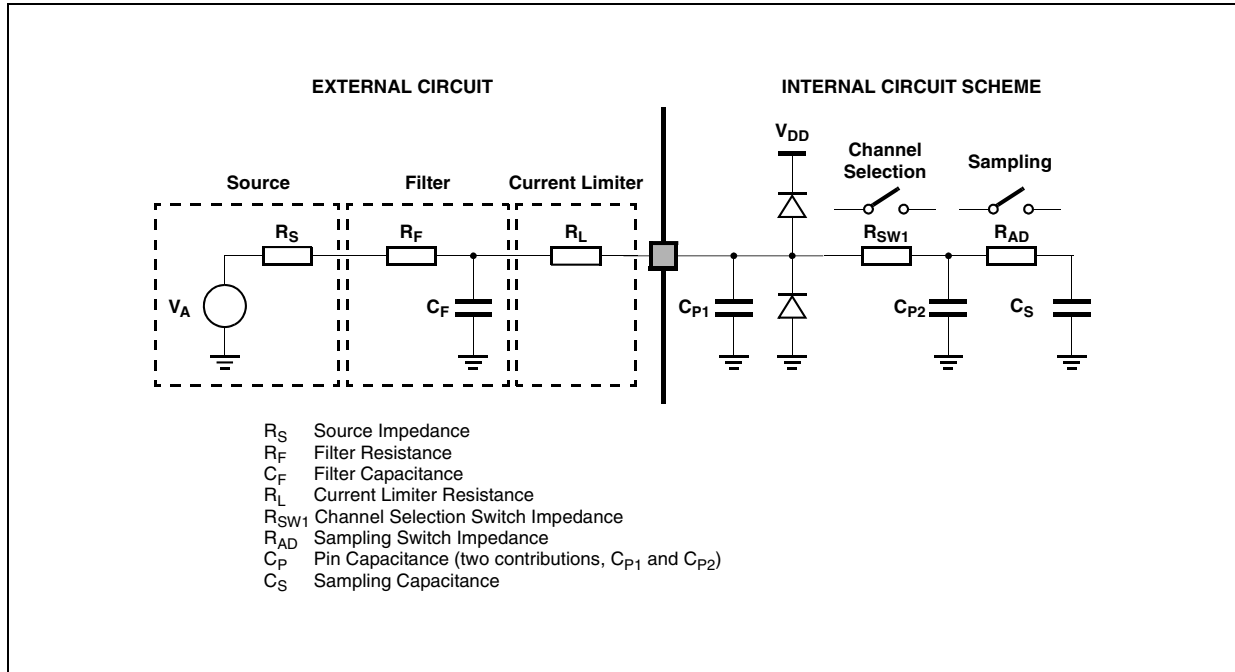


Figure 3. Input equivalent circuit

Table 15. ADC conversion characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|---|------------|------|-----|------|----------|
| f_{CK} | ADC Input Clock frequency (Bus clock) | — | 20 | — | 80 | MHz |
| f_{AD_clk} | ADC Conversion clock frequency ¹ | — | 20 | — | 40 | MHz |
| f_s | Sampling frequency | — | — | — | 0.5 | MHz |
| t_{sample} | Sample time ² | — | 500 | — | — | ns |
| t_{conv} | Conversion time ³ | — | 1400 | — | — | ns |
| C_S | ADC input sampling capacitance | — | — | — | 5 | pF |
| C_{P1} | ADC input pin capacitance 1 | — | — | — | 5 | pF |
| C_{P2} | ADC input pin capacitance 2 | — | — | — | 0.8 | pF |
| R_{SW1} | Internal resistance of analog source | — | — | — | 875 | Ω |
| R_{AD} | Internal resistance of analog source | — | — | — | 825 | Ω |
| INL ⁴ | Integral non linearity | — | -3 | — | 3 | LSB |
| DNL | Differential non linearity | — | -2 | — | 2 | LSB |
| OFS | Offset error | — | -6 | — | 6 | LSB |
| GNE | Gain error | — | -6 | — | 6 | LSB |
| Input (single ADC channel) | Max leakage | 125C | — | — | 2000 | nA |
| TUE | Total unadjusted error | — | -8 | — | 8 | LSB |

1. Please see description of Clock & reset section in ADC chapter in Reference Manual for details. User need to generate AD_clk = 40 MHz for 0.5 MSPS operation. For example, if $f_{ck} = 80$ MHz, configure MCR[8].ADCLKSE = 0 and MCR[4].ADCLKDIV = 0 (default).
2. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming. For internal ADC channels, the minimum sampling time required is 3 microsecond.
3. This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
4. Specifications are quoted here for input signal ranging from 150 mV to VDD_HV_ADC - 150 mV. For signals outside this range, the Specifications may degrade beyond limits specified in this table.

6.1.2 Thermal Monitoring Unit (TMU)

The following table describes TMU electrical characteristics.

Table 16. TMU electrical characteristics

| Symbol | Parameter | Conditions | Value | | | Unit |
|------------|------------------------------|---------------------------------------|-------|-----|-----|-------|
| | | | Min | Typ | Max | |
| T_j | Temperature monitoring range | — | -40 | — | 125 | °C |
| T_{SENS} | Sensitivity | — | — | 2.5 | — | mV/°C |
| T_{ACC} | Accuracy | $T_J = -40\text{ °C to }40\text{ °C}$ | -10 | — | +10 | °C |
| | | $T_J = 40\text{ °C to }125\text{ °C}$ | -6 | — | +6 | °C |

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

The device provides an oscillator/resonator driver of a Pierce-type structure.

Table 17. Main oscillator electrical characteristics

| Symbol | Parameter | Conditions | Value | | | Unit |
|-----------------|---------------------------------------|--|-----------------|------|---------------------------|------|
| | | | Min | Typ | Max | |
| $f_{FXOSCHS}$ | Oscillator frequency | — | — | 40.0 | n/a | MHz |
| $T_{FXOSCHSSU}$ | Oscillator start-up time | $f_{FXOSCHS} = 40\text{ MHz}$ | — | — | 2 ¹ | ms |
| V_{IH} | Input high level CMOS Schmitt Trigger | $V_{ref} = 0.5 * V_{DD_HV_FXOSC}$ where VDD_HV_FXOSC is FXOSC HV Supply | $V_{ref} + 0.5$ | — | $V_{DD_HV_FXOSC} - 0.5$ | V |
| V_{IL} | Input low level CMOS Schmitt Trigger | $V_{ref} = 0.5 * V_{DD_HV_FXOSC}$ where VDD_HV_FXOSC is FXOSC HV Supply | 0 | — | $V_{ref} - 0.5$ | V |

Clocks and PLL interfaces modules

- The start-up time is dependent upon crystal characteristics, board leakage, etc, high ESR and excessive capacitive loads can cause long start-up time

Following crystals are used in internal crystal oscillator validation:

- NX3225 – 40 MHz; Load capacitance = 8 pF
- NX5032 – 40 MHz; Load capacitance = 8 pF

6.2.2 48 MHz FIRC electrical characteristics

Table 18. FIRC electrical specifications

| Symbol | Parameter | Conditions | Value | | | Unit |
|---------------------|--|------------|-------|-----|-----|------|
| | | | Min | Typ | Max | |
| f_{Target} | FIRC target frequency (trimmed) | — | — | 48 | — | MHz |
| δF_{var_T} | FIRC frequency variation with respect to supply and temperature after process trimming | — | -10 | — | +10 | % |

6.2.3 PLL electrical specifications

Table 19. PLL electrical characteristics ¹

| Symbol | Parameter | Conditions | Value | | | Unit |
|-------------------|---|------------|-----------------|-----|------------------|------|
| | | | Min | Typ | Max | |
| f_{PLLIN} | PLL input clock ² | — | 20 ³ | — | 40 ³ | MHz |
| Δ_{PLLIN} | PLL input clock duty cycle ² | — | 40 | — | 60 | % |
| $t_{PLLLOCK}$ | PLL lock time | — | — | — | 100 | μs |
| Δ_{PLLT} | Period jitter | — | — | — | 150 | ps |
| Δ_{PLLTIE} | TIE | — | — | — | 560 | ps |
| f_{PLLMOD} | SSCG modulation frequency | — | — | — | 32 | kHz |
| δ_{PLLMOD} | SSCG modulation depth (Down Spread) | — | 0.50 | — | 2.7 ⁴ | % |

- The jitter values are guaranteed for following conditions:
 - Measurement being done on LFAST TX pad with observed frequency greater than 250 M and less than 320 M
 - Minimum SOC activity - Operations required to observe clock must be functional.
 - Maximum frequency change in SSCG modulation is limited by following relation: Modulation Depth * VCO Frequency < PLL Reference (PFD) Frequency
- PLL0IN clock retrieved from either internal RCOSC or external FXOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.
- The PLLIN clock is the frequency after the PREDIV(Pre-divider) value division, and before the Phase detector block. Please refer to the PLLs section of clocking chapter in the Reference Manual.

4. STEPSIZE x STEPNO < 18432

For the PLL frequencies supported by this device, refer to the Table - "PLL frequencies" in the "Clocking" chapter of the Reference Manual.

6.2.4 DFS electrical specifications

DFS takes input clock from PLL output. Here is relation between input and output clock of each phase divider:

$$F(\text{dfsclockout}) = F(\text{dfsclockin}) / [\text{mfi} + (\text{mfn}/256)]$$

mfi : integer part of division [1:255]

mfn: Fractional part of division [1:255]

Table 20. DFS electrical specification¹

| Parameter | Min | Typical | Max | Unit |
|-----------------|-----|---------|------|------|
| Input Frequency | 800 | — | 1066 | MHz |
| Period jitter | — | — | 300 | ps |
| TIE | — | — | 600 | ps |

1. DFSes mfi, mfn and frequencies are defined and restricted as per Reference Manual. See the table "DFS (mfi, mfn) settings" in the "Clocking" chapter of the Reference Manual for the supported mfi and mfn combinations.

6.2.5 LFAST PLL Electrical Specifications

The following table lists AC specification of the LFAST PLL block.

Table 21. LFAST PLL Interface AC Specifications

| Parameter | Min | Typical | Max | Unit |
|-------------------------------------|-----|---------|-------------------|------|
| PLL input clock | 10 | — | 26 | MHz |
| PLL VCO Frequency | 312 | — | 320 | MHz |
| Phase Lock time | — | — | 50 | μs |
| RMS Period Jitter | — | — | 40 ¹ | ps |
| Long Term Jitter ² | — | 84 | — | ps |
| Random Jitter | — | — | — | ps |
| Deterministic Jitter | — | 80 | — | ps |
| Total Jitter @ BER 10 ⁻⁹ | — | 1.09 | 1.31 ³ | ns |

1. When SysClk = 26 MHz

2. VCO clock measured over 100 μs acquisition at ZipWire TX LVDS across 100 ohm load

3. Only Total Jitter is given a maximum specification as variation of Random and Deterministic jitter is not critical. Any combined Random and Deterministic jitter yielding a Total Jitter @ 10⁻⁹ BER is within maximum specification and is acceptable

6.3 Memory interfaces

6.3.1 QuadSPI AC specifications

- Measurements are with a load of 35 pF on output pins. Input slew: 1 ns, SIUL2_MSCR n [DSE] = 111, and SIUL2_MSCR n [SRE] = 11
- QuadSPI input timing is with 15 pF load on flash output.
- QuadSPI_MCR[DQS_EN] must be set as 1 for SDR READ

NOTE

These are not necessarily the default configuration after chip resets. You must ensure the above chip configuration to match the measurements in this section.

The following table lists various QuadSPI modes and their corresponding configurations. Please refer to the device Reference Manual for register and bit descriptions.

Table 22. QuadSPI read/write settings

| Modes supported by QuadSPI | | QuadSPI_MCR[DDR_EN] | QuadSPI_MCR[DQS_EN] | QuadSPI_MCR[DQS_CD] | QuadSPI_MCR[REF_CLK_SEL] | QuadSPI_MCR[DQS_MDSL] | QuadSPI_SO_CCR [FDCC_FB] | QuadSPI_SO_CCR [FDCC_FA] | QuadSPI_FLSHCR[TDH] |
|----------------------------|---|---------------------|---------------------|---------------------|--------------------------|-----------------------|----------------------------|----------------------------|---------------------|
| SDR mode | Internal DQS mode | 0 | 1 | 000 | 1 | 1 | 39h @ 3.3 V 3Fh @ 1.8 V | 39h @ 3.3 V 3Fh @ 1.8 V | 00 |
| | External DQS mode (supported by HyperFlash) | 1 | 1 | 000 | 0 | 0 | 00h | 00h | 01 |

SDR mode

For SDR mode, QuadSPI_MCR[DQS_EN] must be set as '1'.

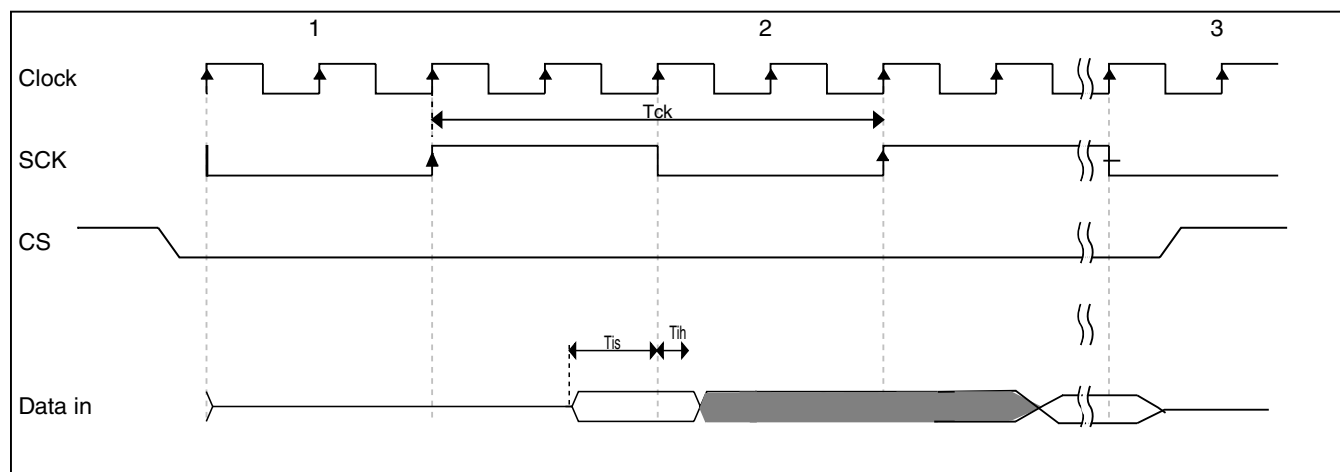


Figure 4. QuadSPI input timing (SDR mode) diagram

NOTE

- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.
- All board delays need to be added appropriately
- Input hold time being negative does not have any implication or max achievable frequency

Table 23. QuadSPI input timing (SDR mode) specifications

| Symbol | Parameter | Value | | Unit |
|-----------|------------------------------|-------|-----|------|
| | | Min | Max | |
| T_{is} | Setup time for incoming data | 2.5 | — | ns |
| T_{ih} | Hold time for incoming data | 1 | — | ns |
| F_{SCK} | SCK clock frequency | — | 104 | MHz |

Memory interfaces

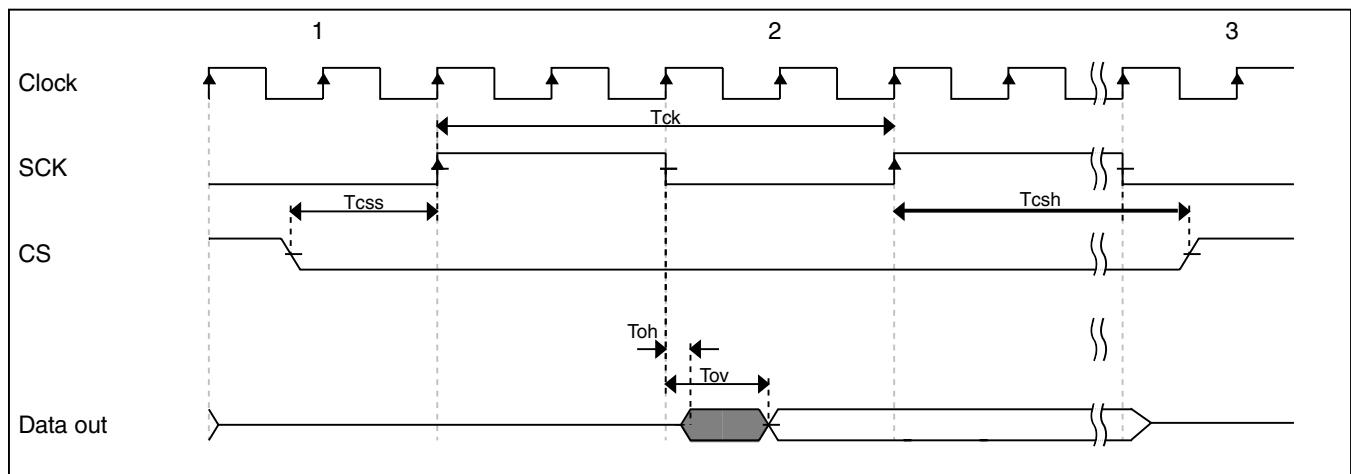


Figure 5. QuadSPI output timing (SDR mode) diagram

Table 24. QuadSPI output timing (SDR mode) specifications

| Symbol | Parameter | Value | | Unit |
|-----------|-------------------------------|-------|-----|------|
| | | Min | Max | |
| T_{ov} | Output Data Valid | — | 1.5 | ns |
| T_{oh} | Output Data Hold | -1.5 | — | ns |
| F_{SCK} | SCK clock frequency | — | 104 | MHz |
| T_{css} | Chip select output setup time | 2 | — | ns |
| T_{csh} | Chip select output hold time | 1 | — | ns |

NOTE

For any frequency setup and hold specifications of the memory should be met.

DDR mode

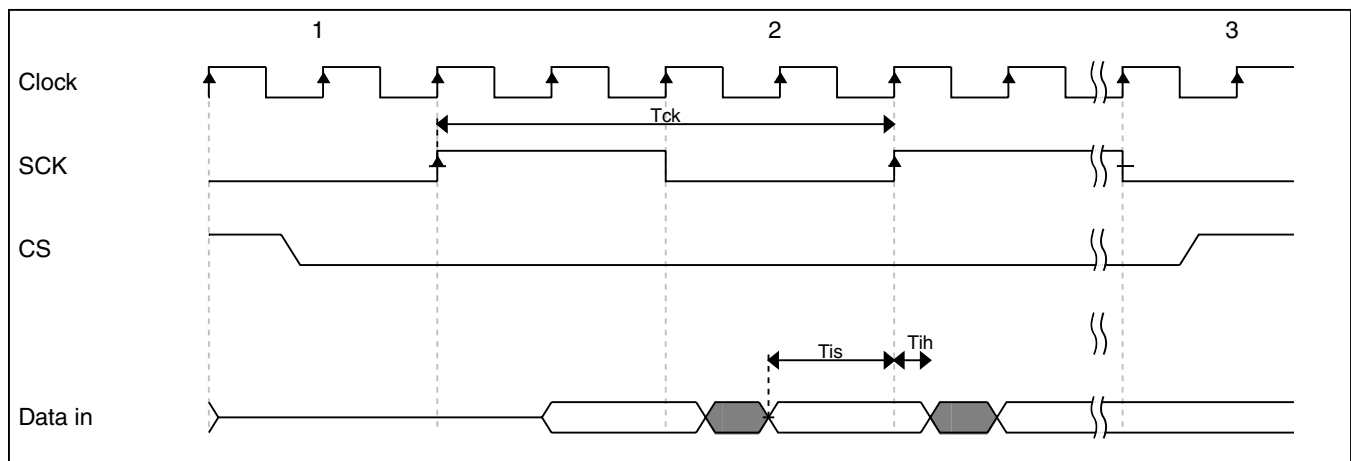
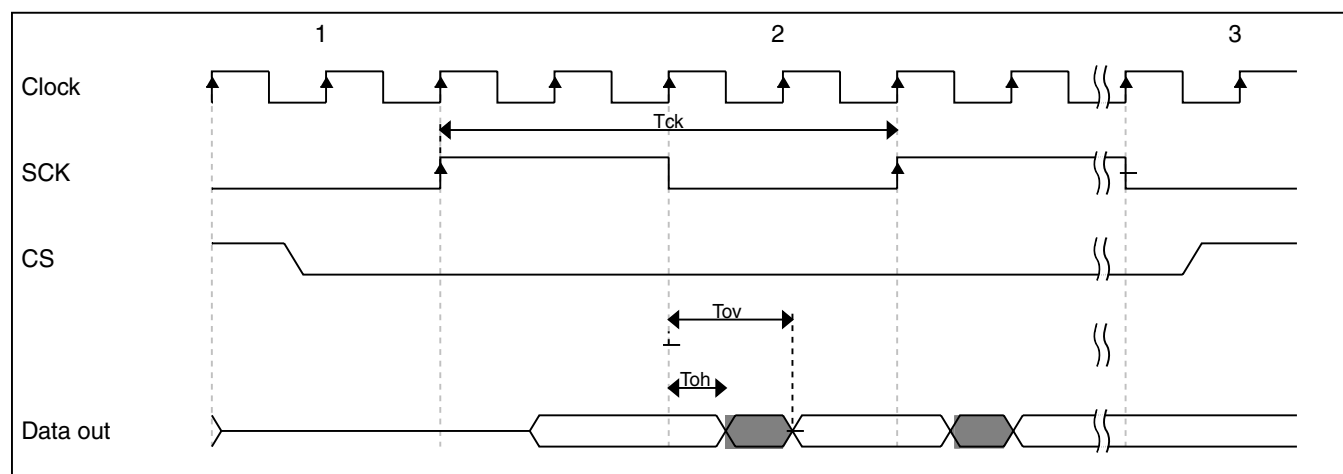


Figure 6. QuadSPI input timing (DDR mode) diagram

Table 25. QuadSPI input timing (DDR mode) specifications

| Symbol | Parameter | Value | | Unit | Configuration |
|-----------|------------------------------|--------------------------|--|------|------------------------------|
| | | Min | Max | | |
| T_{is} | Setup time for incoming data | 2.5 @ 3.3 V 2 @ 1.8 V | — | ns | — |
| T_{ih} | Hold time for incoming data | 1.5 | — | ns | — |
| F_{SCK} | SCK Clock Frequency | — | 50 (Internal DQS) @ 3.3 V 56 (Internal DQS) @ 1.8 V | MHz | See Table 22 |

**Figure 7. QuadSPI output timing (DDR mode) diagram****Table 26. QuadSPI output timing (DDR mode) specifications**

| Symbol | Parameter | Value | | Unit |
|----------|-------------------|-----------------------------|-----------------------------|------|
| | | Min | Max | |
| T_{ov} | Output Data Valid | — | $1/(4 \cdot F_{SCK}) + 1.5$ | ns |
| T_{oh} | Output Data Hold | $1/(4 \cdot F_{SCK}) - 1.5$ | — | ns |

HyperFlash mode

Maximum clock frequency = 100 MHz.

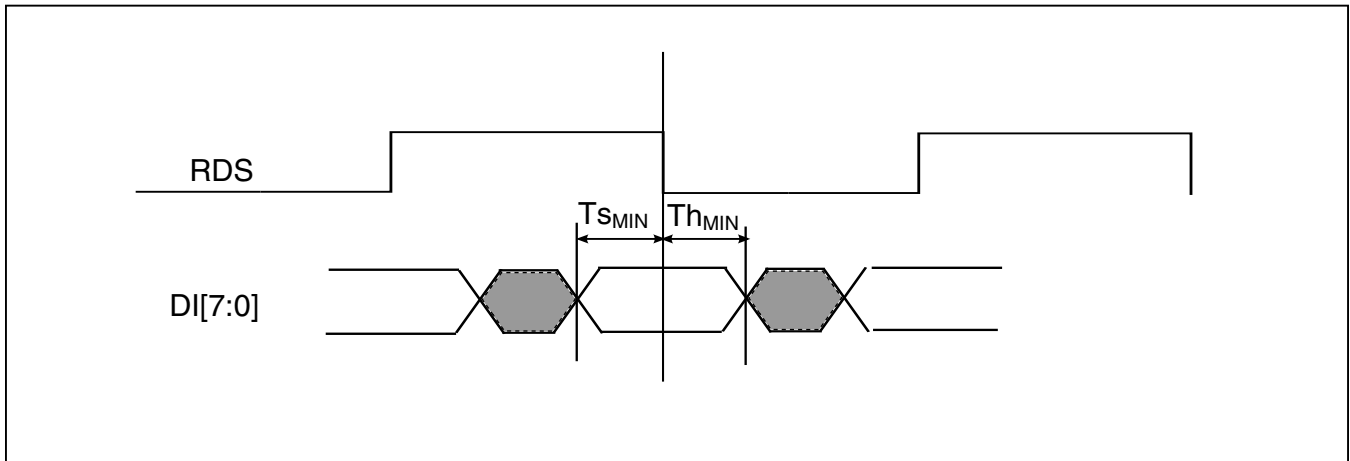


Figure 8. QuadSPI input timing (HyperFlash mode) diagram

Table 27. QuadSPI input timing (HyperFlash mode) specifications

| Symbol | Parameter | Value | | Unit |
|------------|------------------------------|-------|-----|------|
| | | Min | Max | |
| T_{SMIN} | Setup time for incoming data | 0.950 | — | ns |
| T_{hMIN} | Hold time for incoming data | 0.950 | — | ns |

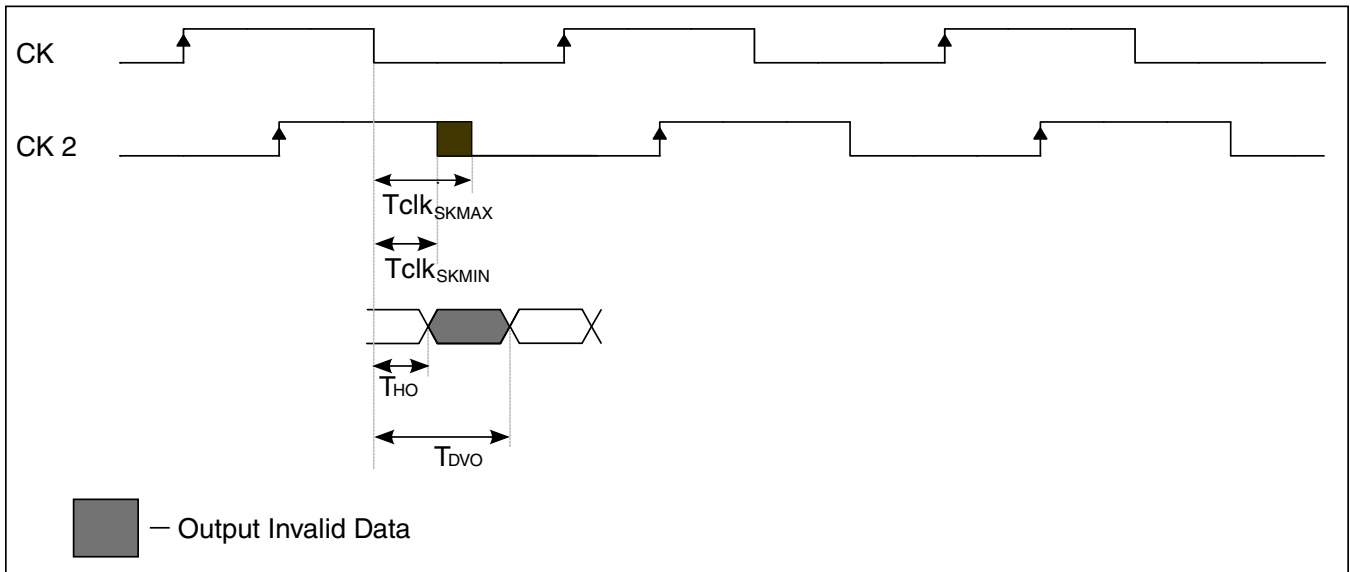


Figure 9. QuadSPI output timing (HyperFlash mode) diagram

Table 28. QuadSPI output timing (HyperFlash mode) specifications

| Symbol | Parameter | Value | | Unit |
|-------------|-------------------|-------|-----|------|
| | | Min | Max | |
| T_{dvMAX} | Output Data Valid | — | 3.7 | ns |
| T_{ho} | Output Data Hold | 1 | — | ns |

Table continues on the next page...

Table 28. QuadSPI output timing (HyperFlash mode) specifications (continued)

| Symbol | Parameter | Value | | Unit |
|-----------------------|--------------------|-------------|-------------|------|
| | | Min | Max | |
| Tclk _{SKMAX} | Ck to Ck2 skew max | — | T/4 + 0.150 | ns |
| Tclk _{SKMIN} | Ck to Ck2 skew min | T/4 – 0.150 | — | ns |

6.4 DDR SDRAM Specific Parameters (DDR3, DDR3L, and LPDDR2)

6.4.1 DDR3 and DDR3L timing parameters

NOTE

Operating voltages of DDR3 and DDR3L are different.

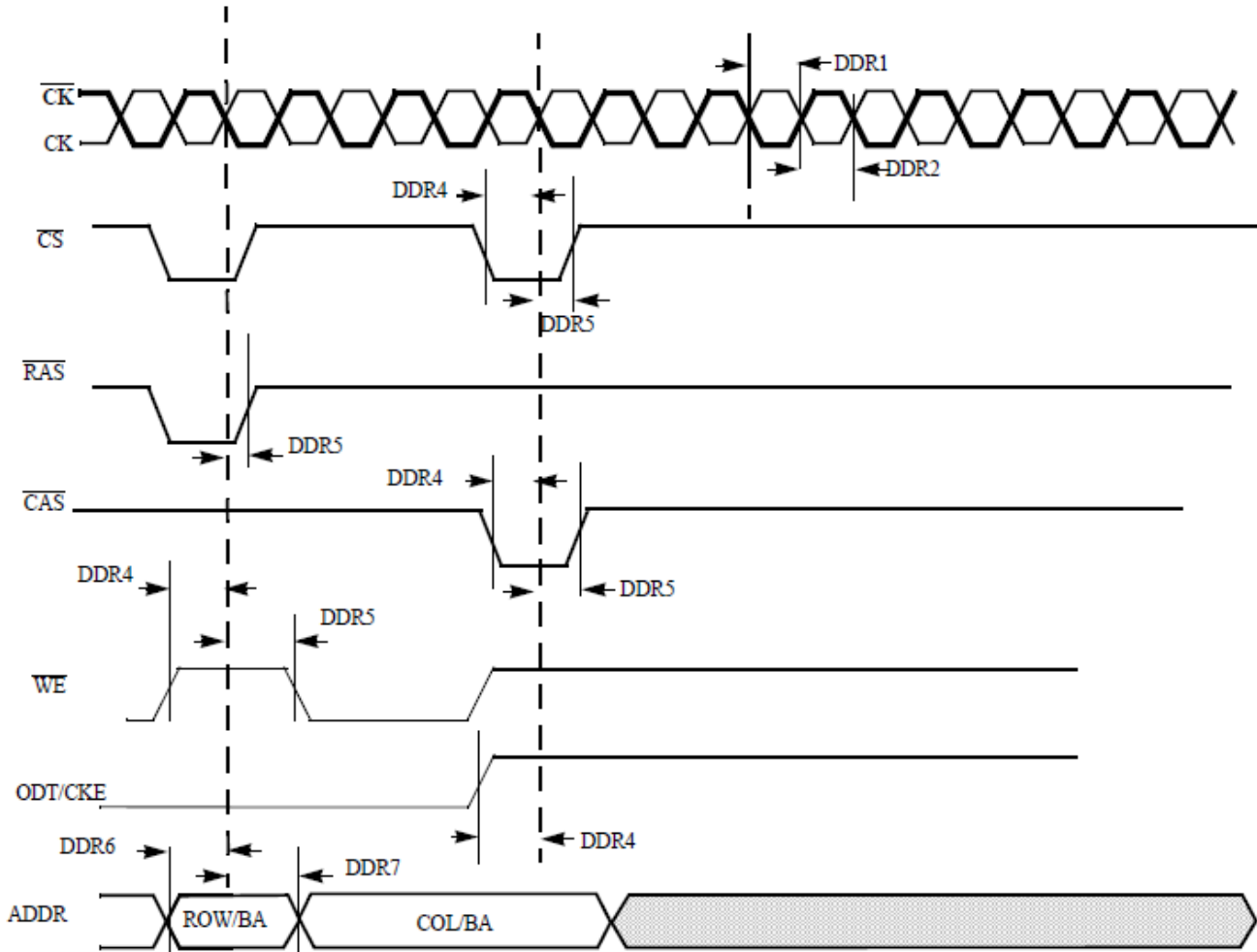


Figure 10. DDR3 and DDR3L command and address timing parameters

NOTE

RESET pin has an external weak pull DOWN requirement if DDR3 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

RESET pin has an external weak pull UP requirement if DDR3 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has an external weak pull down requirement.

NOTE

DDR3 and DDR3L timing parameters are compliant with JESD79-3F and JESD79-3-1A.01 specifications respectively.

Table 29. DDR3 and DDR3L timing parameter

| ID | Parameter | Symbol | CK = 533 MHz | | Unit |
|------|---------------------------------------|--------|--------------|------|-----------|
| | | | Min | Max | |
| DDR1 | CK clock high-level width | tCH | 0.47 | 0.53 | tCK (avg) |
| DDR2 | CK clock low-level width | tCL | 0.47 | 0.53 | tCK (avg) |
| DDR4 | CS, RAS, CAS, CKE, WE, ODT setup time | tIS | 280 | — | ps |
| DDR5 | CS, RAS, CAS, CKE, WE, ODT hold time | tIH | 300 | — | ps |
| DDR6 | Address output setup time | tIS | 280 | — | ps |
| DDR7 | Address output hold time | tIH | 300 | — | ps |

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

6.4.2 DDR3 and DDR3L read cycle

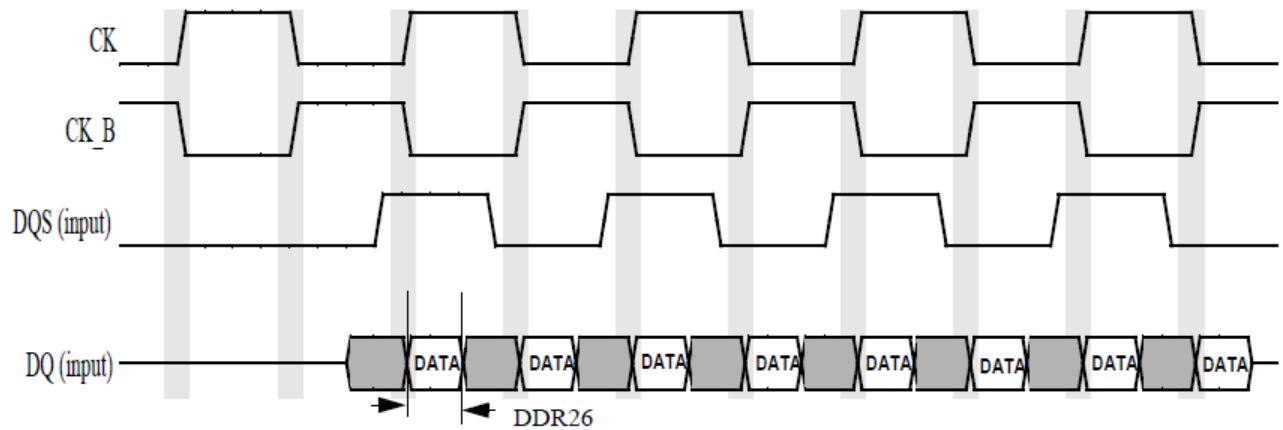


Figure 11. DDR3 and DDR3L read cycle

Table 30. DDR3 and DDR3L read cycle

| ID | Parameter | Symbol | CK = 533 MHz | | Unit |
|-------|--|--------|--------------|-----|------|
| | | | Min | Max | |
| DDR26 | Minimum required DQ valid window width | — | 563 | — | ps |

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

6.4.3 DDR3 and DDR3L write cycle

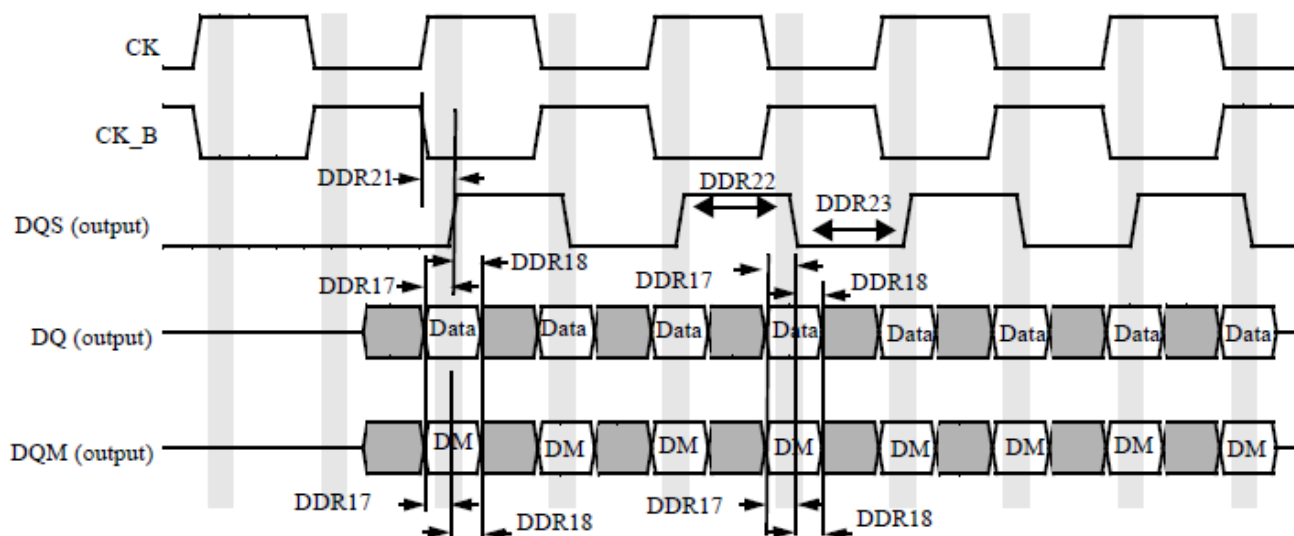


Figure 12. DDR3 and DDR3L write cycle

Table 31. DDR3 and DDR3L write cycle

| ID | Parameter | Symbol | CK = 533 MHz | | Unit |
|-------|---|--------|--------------|-------|-----------|
| | | | Min | Max | |
| DDR17 | DQ and DQM setup time to DQS (differential strobe) | tDS | 206 | — | ps |
| DDR18 | DQ and DQM hold time to DQS (differential strobe) | tDH | 280 | — | ps |
| DDR21 | DQS latching rising transitions to associated clock edges | tDQSS | -0.25 | +0.25 | tCK (avg) |
| DDR22 | DQS high level width | tDQSH | 0.45 | 0.55 | tCK (avg) |
| DDR22 | DQS low level width | tDQSL | 0.45 | 0.55 | tCK (avg) |

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

6.4.4 LPDDR2 timing parameter

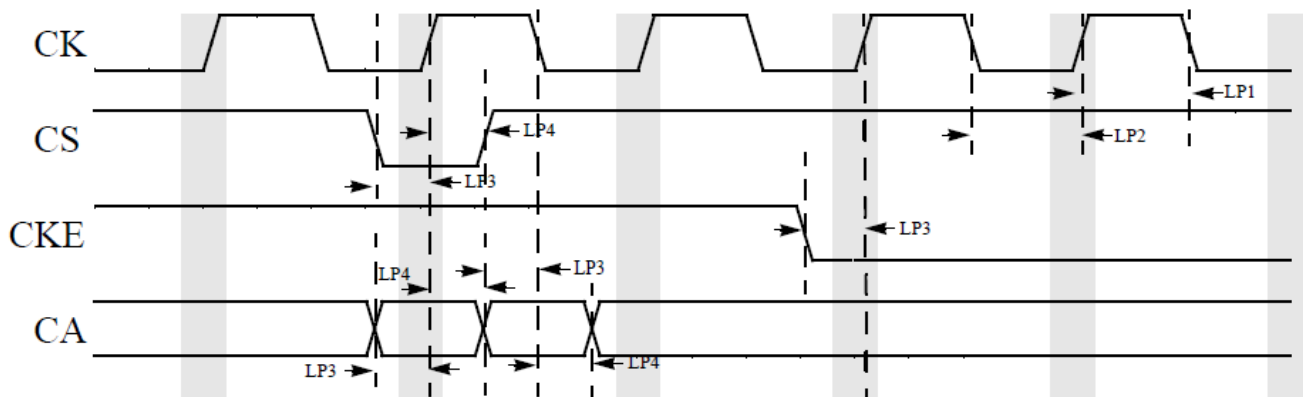


Figure 13. LPDDR2 command and address timing parameter

NOTE

RESET pin has a external weak pull DOWN requirement if LPDDR2 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

RESET pin has a external weak pull UP requirement if LPDDR2 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has a external weak pull down requirement.

NOTE

LPDDR2 timing parameters are compliant with JESD209-2B specification.

Table 32. LPDDR2 timing parameter

| ID | Parameter | Symbol | CK = 533 MHz | | Unit |
|-----|------------------------------|-----------|--------------|------|-----------|
| | | | Min | Max | |
| LP1 | SDRAM clock high-level width | tCH (avg) | 0.45 | 0.55 | tCK (avg) |
| LP2 | SDRAM clock LOW-level width | tCL (avg) | 0.45 | 0.55 | tCK (avg) |
| LP3 | CS, CKE setup time | tIS | 235 | — | ps |
| LP4 | CS, CKE hold time | tIH | 250 | — | ps |
| LP3 | CA setup time | tIS | 235 | — | ps |
| LP4 | CA hold time | tIH | 250 | — | ps |

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

6.4.5 LPDDR2 read cycle

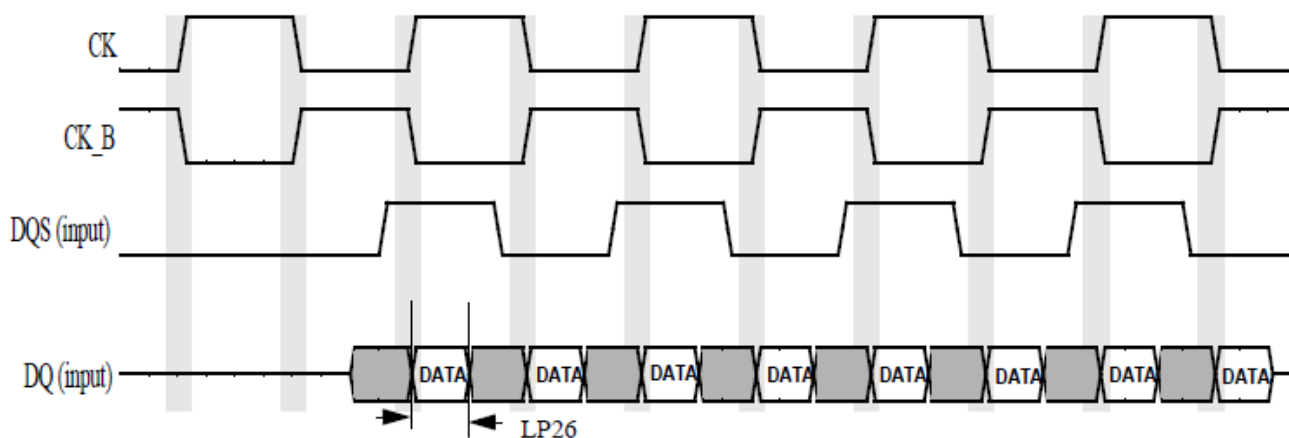


Figure 14. LPDDR2 read cycle

Table 33. LPDDR2 read cycle

| ID | Parameter | Symbol | CK = 533 MHz | | Unit |
|------|---|--------|--------------|-----|------|
| | | | Min | Max | |
| LP26 | Minimum required DQ valid window width for LPDDR2 | — | 364 | — | ps |

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

6.4.6 LPDDR2 write cycle

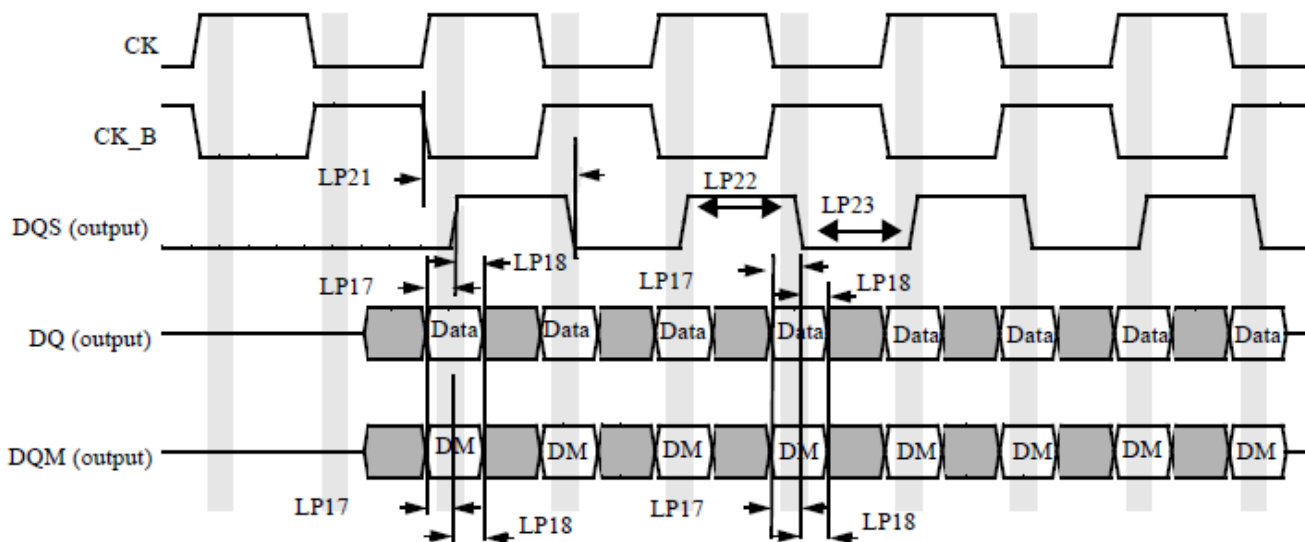


Figure 15. LPDDR2 write cycle

Table 34. LPDDR2 write cycle

| ID | Parameter | Symbol | CK = 533 MHz | | Unit |
|------|---|--------|--------------|------|-----------|
| | | | Min | Max | |
| LP17 | DQ and DQM setup time to DQS (differential strobe) | tDS | 280 | — | ps |
| LP18 | DQ and DQM hold time to DQS (differential strobe) | tDH | 220 | — | ps |
| LP21 | DQS latching rising transitions to associated clock edges | tDQSS | 0.75 | 1.25 | tCK (avg) |
| LP22 | DQS high level width | tDQSH | 0.4 | — | tCK (avg) |
| LP23 | DQS low level width | tDQSL | 0.4 | — | tCK (avg) |

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

6.5 Communication modules

6.5.1 DSPI timing

Measurements are with a load of 45 pF on output pins. Input slew = 1 ns, SIUL2_MSCRn[DSE] = 101, and SIUL2_MSCRn[SRE] = 11.

NOTE

These are not necessarily the default configuration after chip resets. You must ensure the above chip configuration to match the measurements in this section.

Table 35. DSPI timing

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|-----|-------------------|--------------------------------|--|---------------------------|---------------------------|------|
| 1 | t _{SCK} | DSPI cycle time | Master (MTFE = 0) | 40 ¹ | - | ns |
| | | | Slave (MTFE = 0) | 40 | - | |
| | | | Slave Receive Only Mode ² | 16 | - | |
| 2 | t _{CSC} | PCS to SCK delay | - | 16 ³ | - | ns |
| 3 | t _{ASC} | After SCK delay | - | 16 ⁴ | - | ns |
| 4 | t _{SDC} | SCK duty cycle | - | t _{SCK} /2 - 1.5 | t _{SCK} /2 + 1.5 | ns |
| 5 | t _A | Slave access time | \overline{SS} active to SOUT valid | - | 40 | ns |
| 6 | t _{DIS} | Slave SOUT disable time | \overline{SS} inactive to SOUT High-Z or invalid | - | 15 | ns |
| 7 | t _{PCSC} | PCSx to \overline{PCSS} time | - | 13 | - | ns |
| 8 | t _{PASC} | \overline{PCSS} to PCSx time | - | 13 | - | ns |
| 9 | t _{SUI} | Data setup time for inputs | Master (MTFE = 0) | 15 | - | ns |
| | | | Slave | 2 | - | |
| | | | Master (MTFE = 1, CPHA = 0) | 6 | - | |
| | | | Master (MTFE = 1, CPHA = 1) | 20 | - | |
| 10 | t _{HI} | Data hold time for inputs | Master (MTFE = 0) | -4 | - | ns |
| | | | Slave | 4 | - | |
| | | | Master (MTFE = 1, CPHA = 0) | 11 | - | |
| | | | Master (MTFE = 1, CPHA = 1) | -4 | - | |
| 11 | t _{SUO} | Data valid (after SCK edge) | Master (MTFE = 0) | - | 4 | ns |
| | | | Slave | - | 16 | |
| | | | Master (MTFE = 1, CPHA = 0) | - | 12 | |
| | | | Master (MTFE = 1, CPHA = 1) | - | 4 | |
| 12 | t _{HO} | Data hold time for outputs | Master (MTFE = 0) | -2 | - | ns |
| | | | Slave | 3 | - | |
| | | | Master (MTFE = 1, CPHA = 0) | 5 | - | |
| | | | Master (MTFE = 1, CPHA = 1) | -2 | - | |

Communication modules

1. SMPL_PTR should be set to 1. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is ≥ 3 .
2. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.
3. This value of 16 ns is with the configuration prescaler values: SPI_CTARn[PCSSCK] - "PCS to SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[CSSCK] - "PCS to SCK Delay Scaler" configuration is "2" (0000h).
4. This value of 16 ns is with the configuration prescaler values: SPI_CTARn[PASC] - "After SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[ASC] - "After SCK Delay Scaler" configuration is "2" (0000h).

NOTE

DSPI Timing specs on this chip are valid with Slave in Classic Mode only.

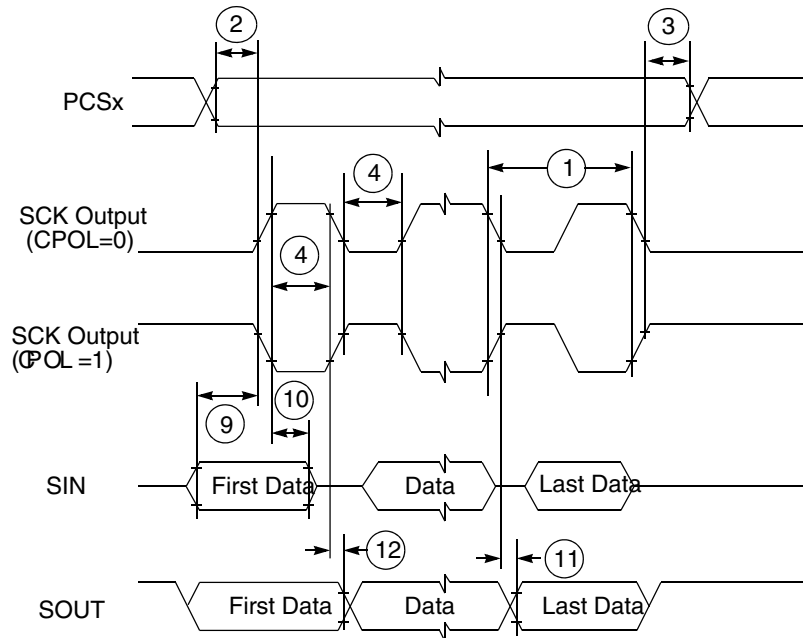


Figure 16. DSPI classic SPI timing — master, CPHA = 0

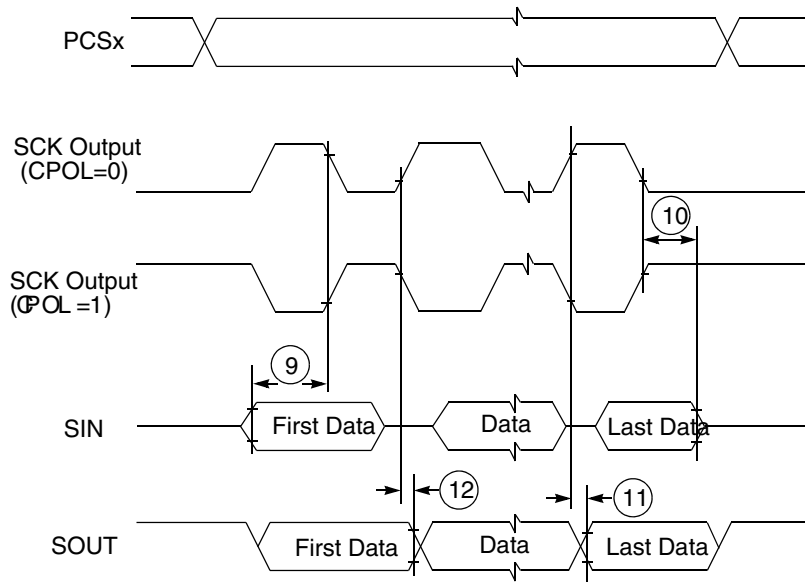


Figure 17. DSPI classic SPI timing — master, CPHA = 1

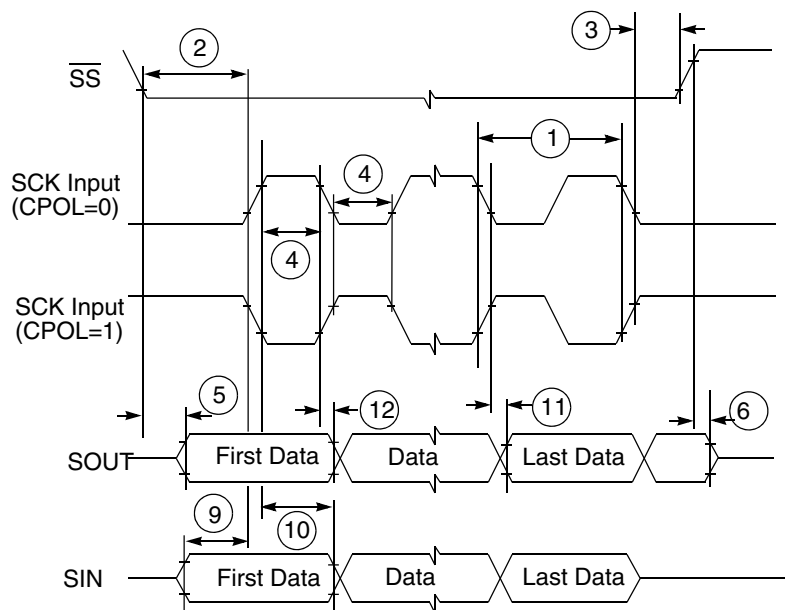


Figure 18. DSPI classic SPI timing — slave, CPHA = 0

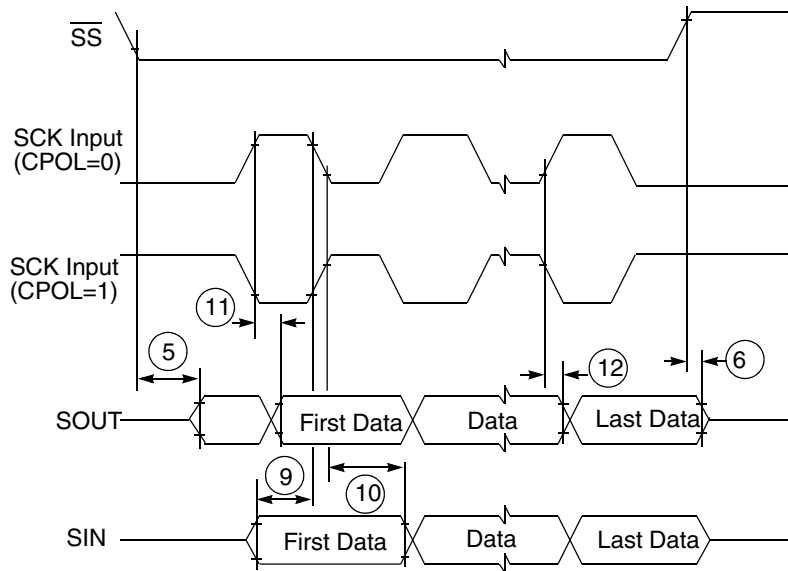


Figure 19. DSPI classic SPI timing — slave, CPHA = 1

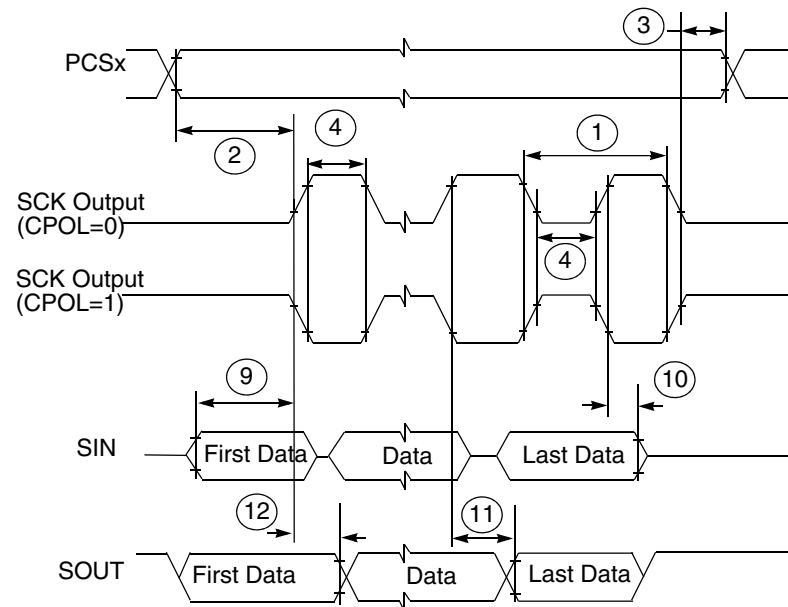


Figure 20. DSPI modified transfer format timing — master, CPHA = 0

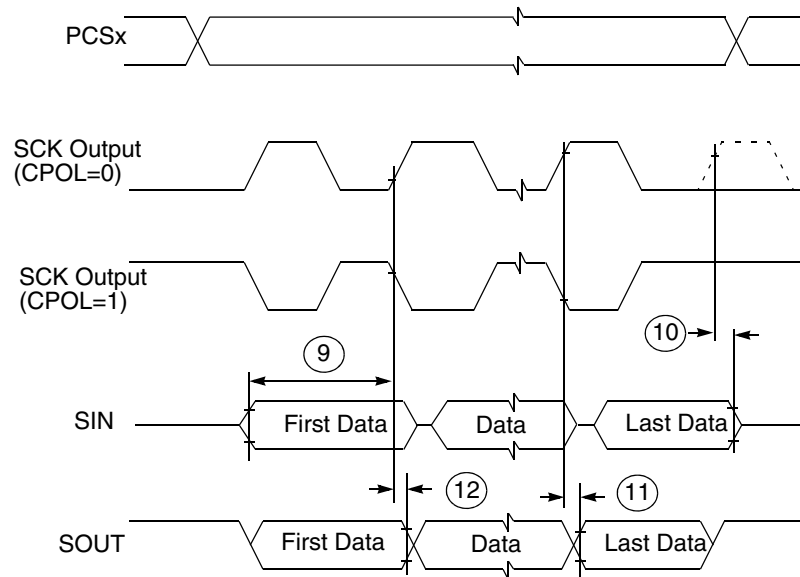


Figure 21. DSPI modified transfer format timing — master, CPHA = 1

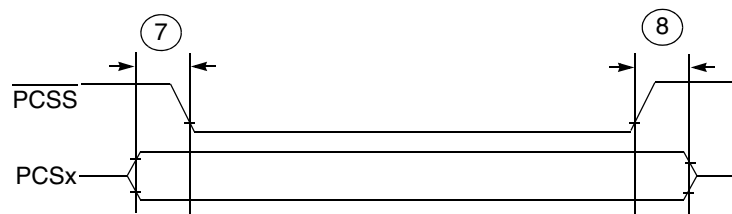


Figure 22. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

6.5.2 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC)

Booting from eMMC must be at voltage of 3.3 V. The operation at 1.8 V is possible only during run-time, that is after the boot has completed. This voltage restriction during booting does not apply to SD/SDIO/SDHC/SDXC modes.

Measurements are with a load of 40 pF on output pins. Input slew = 1 ns, SIUL2_MSCRn[DSE] = 101, and SIUL2_MSCRn[SRE] = 11.

uSDHC_VEND_SPEC[CMD_OE_PRE_EN] field should be programmed to 1 for proper functioning of uSDHC external interface.

NOTE

These are not necessarily the default configuration after chip resets. You must ensure the above chip configuration to match the measurements in this section.

6.5.2.1 SDR mode timing specifications

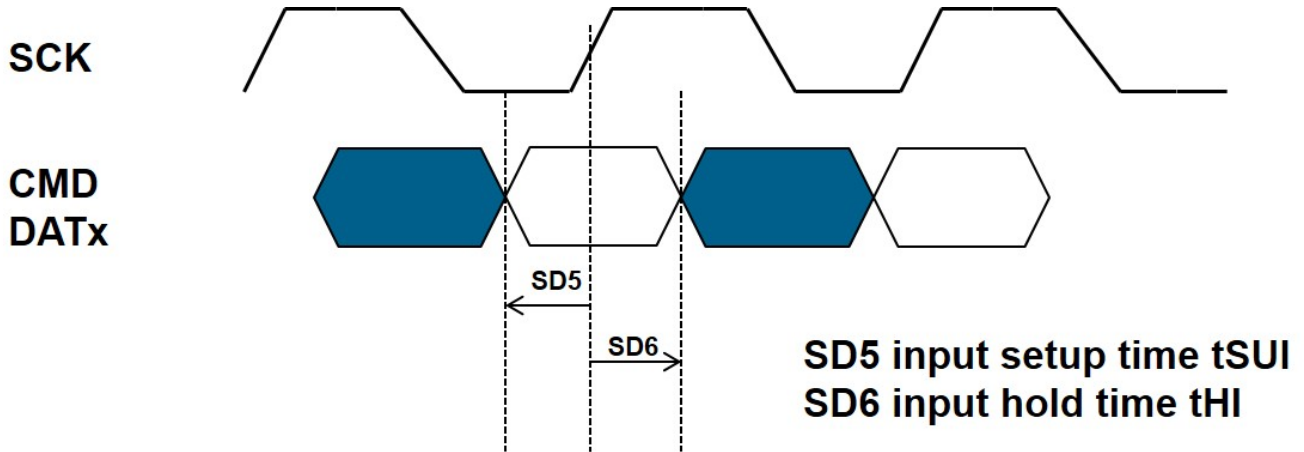


Figure 23. SDR CMD-DATx Read Timing

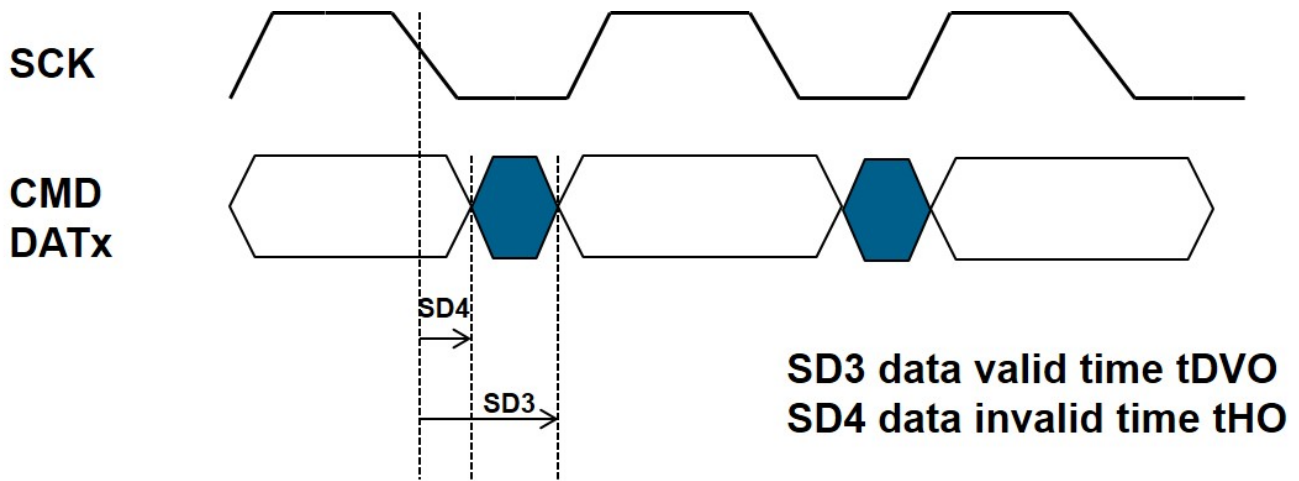


Figure 24. SDR CMD-DATx Write Timing

Table 36. SDR mode timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|---|------------|-----|-------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (Low Speed) | f_{PP}^1 | 0 | 400 | kHz |
| | Clock Frequency (SD/SDIO Full Speed/High Speed) | f_{PP}^2 | 0 | 25/50 | MHz |
| | Clock Frequency (MMC Full Speed/High Speed) | f_{PP}^3 | 0 | 20/52 | MHz |
| | Clock Frequency (Identification Mode) | f_{OD} | 100 | 400 | kHz |
| SD2 | Clock Duty Cycle | t_{DC} | 45 | 55 | % |
| eSDHC Output/Card Inputs CMD, DAT (Reference to CLK) | | | | | |

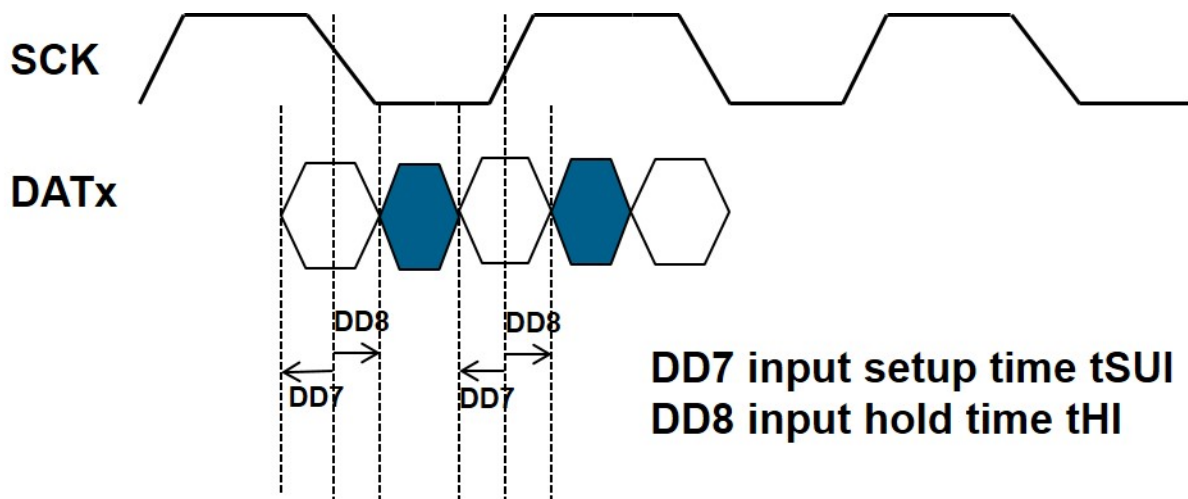
Table continues on the next page...

Table 36. SDR mode timing specification (continued)

| ID | Parameter | Symbols | Min | Max | Unit |
|--|---------------------------|-----------|------|-----|------|
| SD3 | CLK to Data/CMD Valid | t_{DVO} | — | 3.2 | ns |
| SD4 | CLK to Data/CMD Invalid | t_{HO} | -6.3 | — | ns |
| eSDHC Input/Card Outputs CMD, DAT (Reference to CLK) | | | | | |
| SD5 | DATA/CMD Input Setup time | t_{SUI} | 4.5 | — | ns |
| SD6 | DATA/CMD Input Hold time | t_{HI} | 0 | — | ns |

1. In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
2. In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
3. In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

6.5.2.2 DDR mode timing specifications

**Figure 25. DDR Data Read timing**

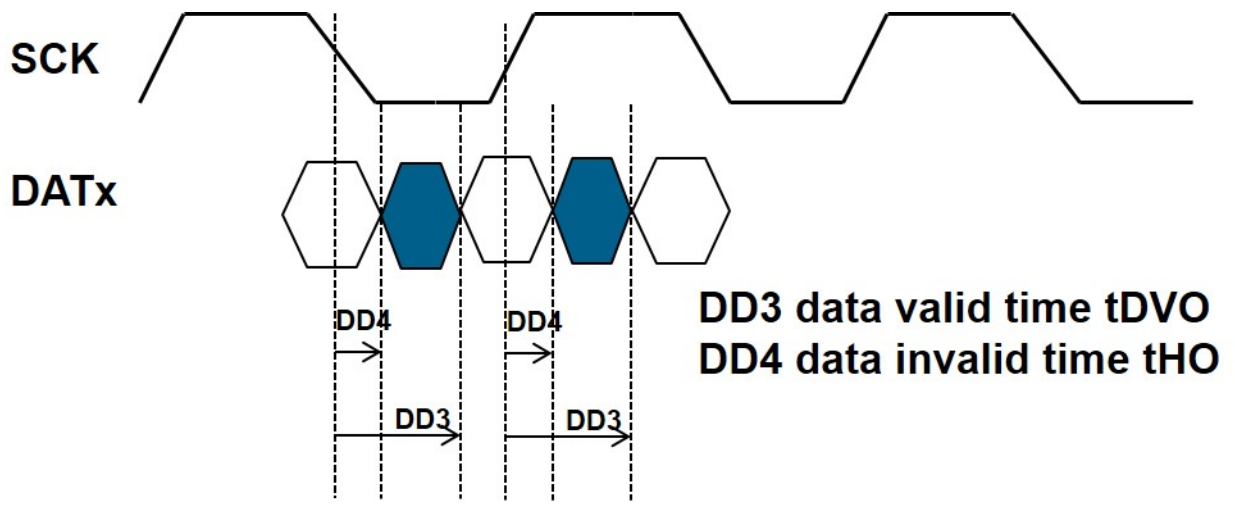


Figure 26. DDR DATA Write timing

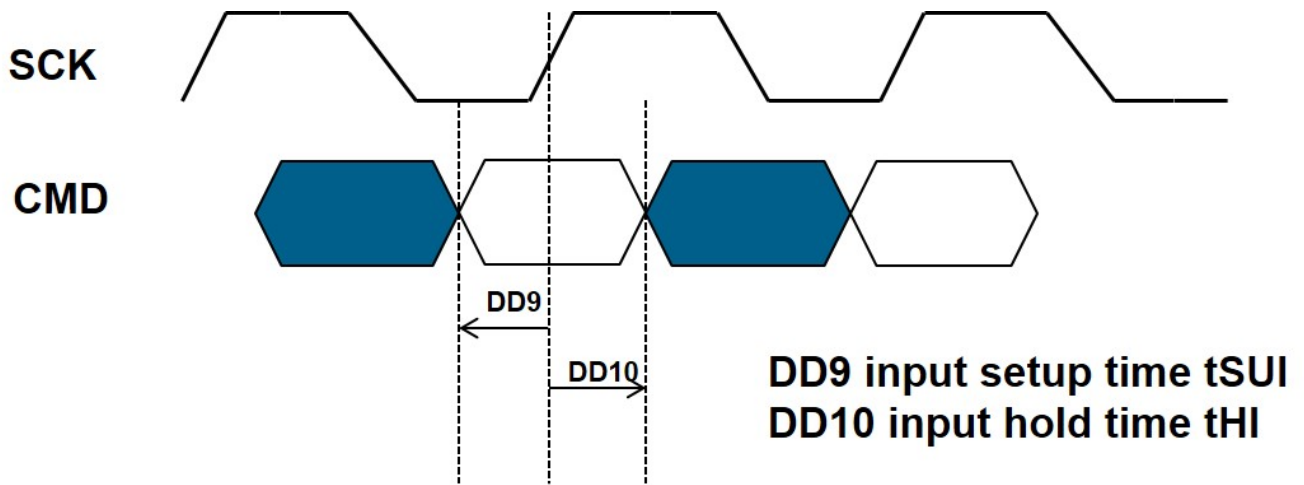


Figure 27. DDR CMD Read Timing

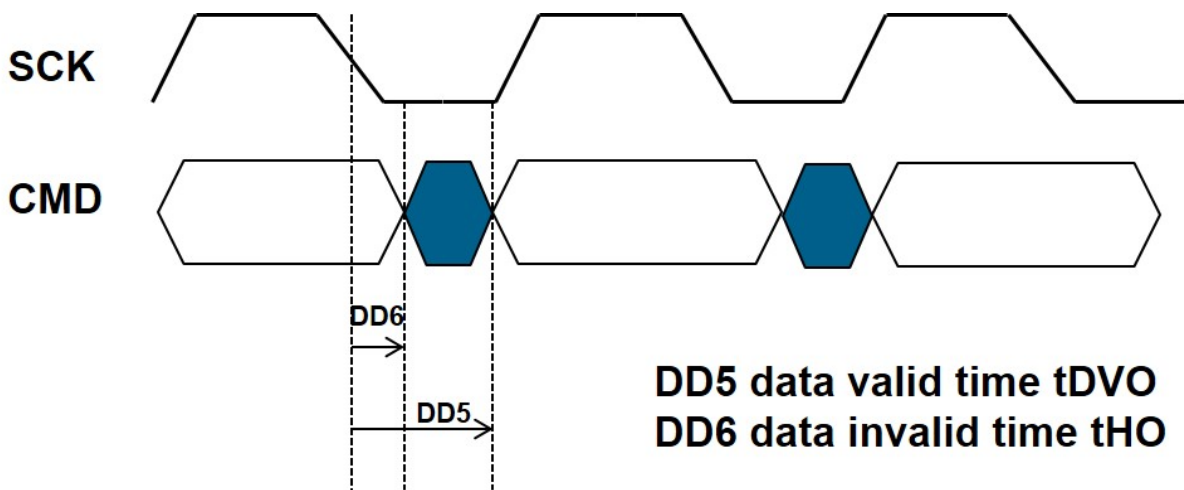


Figure 28. DDR CMD Write Timing

Table 37. DDR mode timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|-------------------------------|-----------|------|------|------|
| Card Input Clock | | | | | |
| DD1 | Clock Frequency (eMMC4.4 DDR) | f_{PP} | 0 | 52 | MHz |
| DD1 | Clock Frequency (SD3.0 DDR) | f_{PP} | 0 | 50 | MHz |
| DD2 | Clock Duty Cycle | t_{DC} | 45 | 55 | % |
| uSDHC Output/Card Inputs CMD, DAT (Reference to CLK) | | | | | |
| DD3 | CLK to Data Valid | t_{DVO} | — | 6.2 | ns |
| DD4 | CLK to Data Invalid | t_{HO} | 2.5 | — | ns |
| DD5 | CLK to CMD Valid | t_{DVO} | — | 3.25 | ns |
| DD6 | CLK to CMD Invalid | t_{HO} | -6.2 | — | ns |
| uSDHC Input/Card Outputs CMD, DAT (Reference to CLK) | | | | | |
| DD7 | Data Input Setup Time | t_{SUI} | 2.3 | — | ns |
| DD8 | Data Input Hold Time | t_{HI} | 1.5 | — | ns |
| DD9 | CMD Input Setup Time | t_{SUI} | 4.5 | — | ns |
| DD10 | CMD Input Hold Time | t_{HI} | 0 | — | ns |

6.5.3 LFAST electrical characteristics

6.5.3.1 LFAST interface timing diagrams

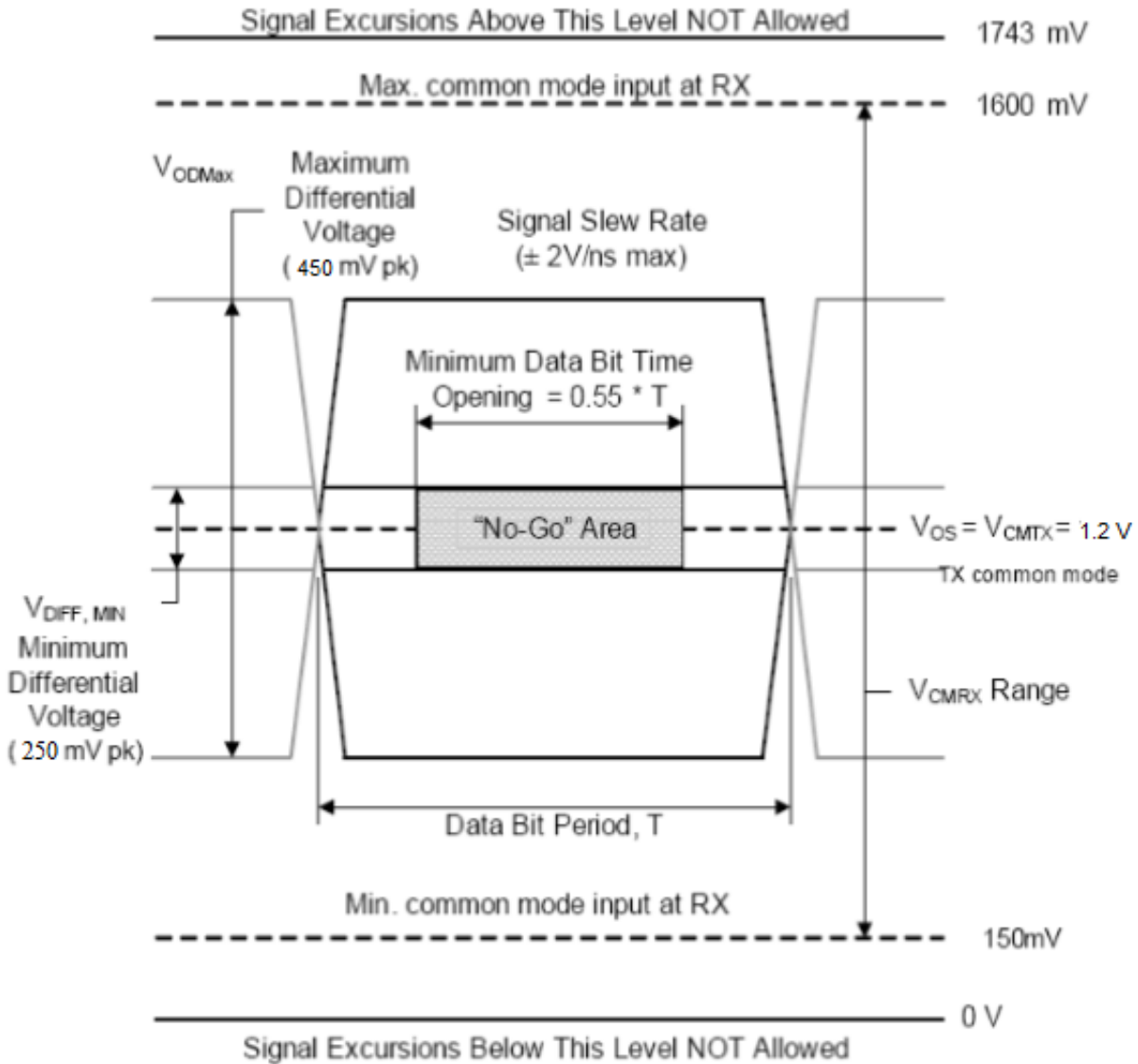


Figure 29. LFAST timing definition

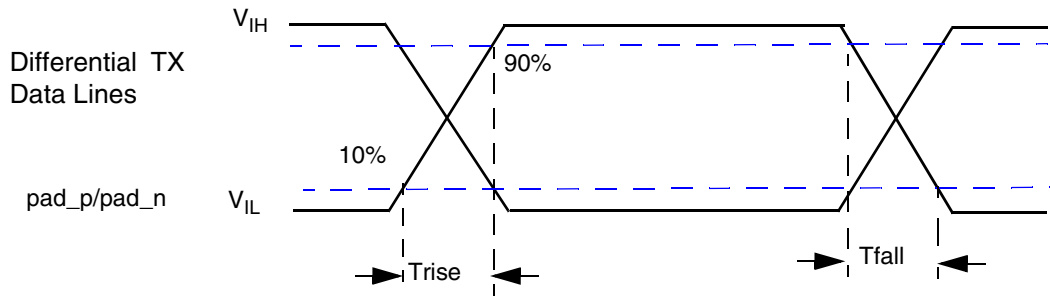


Figure 30. Rise/fall time

6.5.3.2 LFAST Interface electrical characteristics

Table 38. LFAST electrical characteristics

| Symbol | Parameter | Conditions | Value ¹ | | | Unit |
|------------------------------------|--|-------------------------------|--------------------|---------|------------------|------|
| | | | Min | Typ | Max | |
| V _{DDIO_LFAST} | Operating supply conditions | — | 1.71 | — | 1.95 | V |
| <i>Data Rate</i> | | | | | | |
| DATARATE | Data rate | — | — | 312/320 | Typ+0.1% | Mbps |
| <i>STARTUP</i> | | | | | | |
| T _{STRT_BIAS} | Bias startup time ² | — | — | 0.5 | 3 | μs |
| <i>TRANSMITTER</i> | | | | | | |
| V _{OS_DRF} | Common mode voltage | — | 1.1 | 1.2 | 1.475 | V |
| ΔV _{OD_DRF} | Differential output voltage swing (terminated) | — | 250 | 350 | 450 | mV |
| T _{TR_DRF} | Rise/Fall time (20% - 80% of swing) ³ | — | 0.1 | — | 0.73 | ns |
| C _{OUT_DRF} | Capacitance ⁴ | — | — | — | 5 | pF |
| <i>RECEIVER</i> | | | | | | |
| V _{ICOM_DRF} | Common mode voltage | — | 0.15 ⁵ | — | 1.5 ⁶ | V |
| ΔV _{I_DRF} | Differential input voltage | V _{ICOM_DRF} > 1.4 V | 150 | — | — | mV |
| | | V _{ICOM_DRF} ≤ 1.4 V | 100 | — | — | mV |
| R _{IN_DRF} | Terminating resistance | — | 80 | 100 | 150 | Ω |
| C _{IN_DRF} | Capacitance ⁷ | — | — | 3.5 | 6 | pF |
| L _{IN_DRF} | Parasitic Inductance ⁸ | — | — | 5 | 10 | nH |
| <i>LFAST Clock characteristics</i> | | | | | | |
| F _{RF_REF} | SysClk Frequency | — | 10 | — | 26 | MHz |
| ERR _{REF} | SysClk Frequency Error | — | -1 | — | 1 | % |
| DC _{REF} | SysClk Duty Cycle | — | 45 | — | 55 | % |

1. All values need to be confirmed during device characterization.
2. Startup time is defined as the time taken by LFAST current reference block for settling bias current after its pwr_down (power down) has been deasserted. LFAST functionality is guaranteed only after the startup time.
3. Rise/fall time is defined for 20 to 80% signal voltage levels, at 2pF Cloud and 100 Ohm termination resistor load.
4. Total lumped capacitance including silicon, package pin and bond wire. Application board simulation needed to verify LFAST template compliancy.
5. Absolute min = 0.15 V - (250 mV/2) = 0.025 V

- 6. Absolute max = 1.5 V + (450 mV/2) = 1.725 V
- 7. Total capacitance including silicon, package pin and bond wire
- 8. Total inductance including silicon, package pin and bond wire

6.5.4 FlexRay

6.5.4.1 FlexRay timing parameters

This section provides the FlexRay interface timing characteristics for the input and output signals. These numbers are recommended per the FlexRay Electrical Physical Layer Specification, Version 3.0.1, and subject to change per the final timing analysis of the device.

6.5.4.2 TxEN

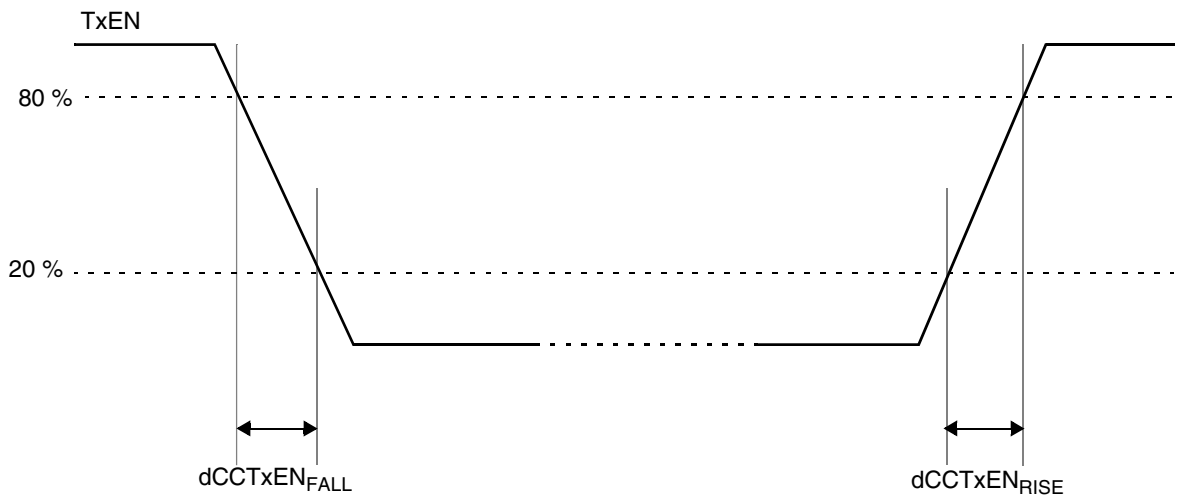


Figure 31. TxEN signal

Table 39. TxEN output characteristics¹

| Name | Description | Min | Max | Unit |
|-----------------------|--|-----|-----|------|
| dCCTxEN_RISE25 | Rise time of TxEN signal at CC | - | 9 | ns |
| dCCTxEN_FALL25 | Fall time of TxEN signal at CC | - | 9 | ns |
| dCCTxEN ₀₁ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | - | 25 | ns |
| dCCTxEN ₁₀ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | - | 25 | ns |

1. TxEN pin load maximum 25 pF.

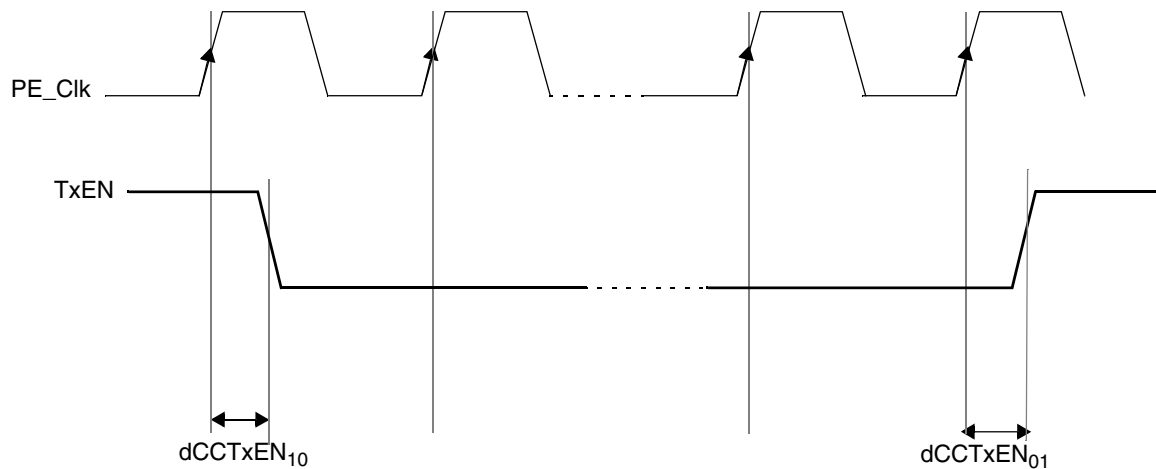


Figure 32. TxEN signal propagation delays

6.5.4.3 TxD

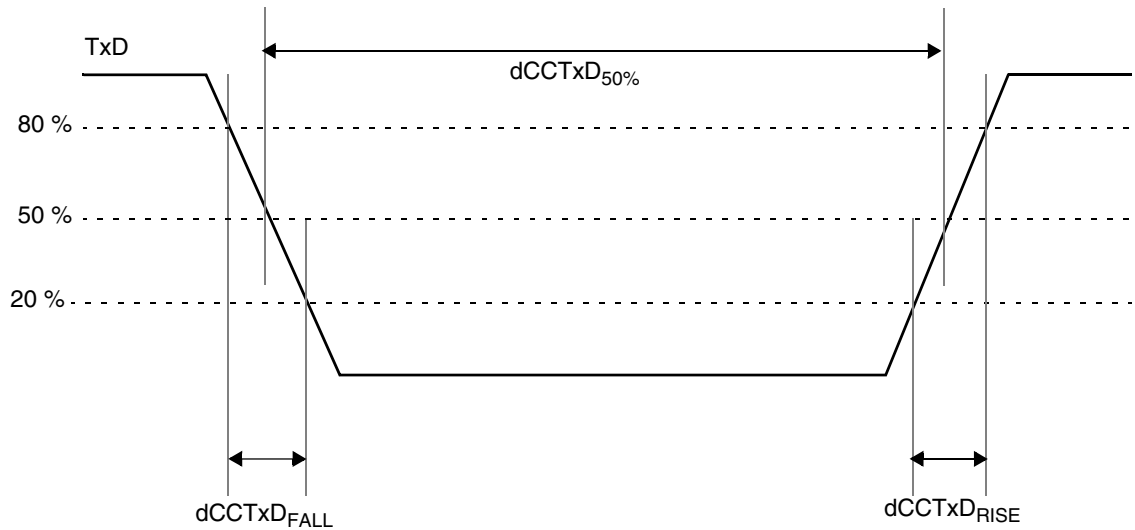


Figure 33. TxD signal

Table 40. TxD output characteristics

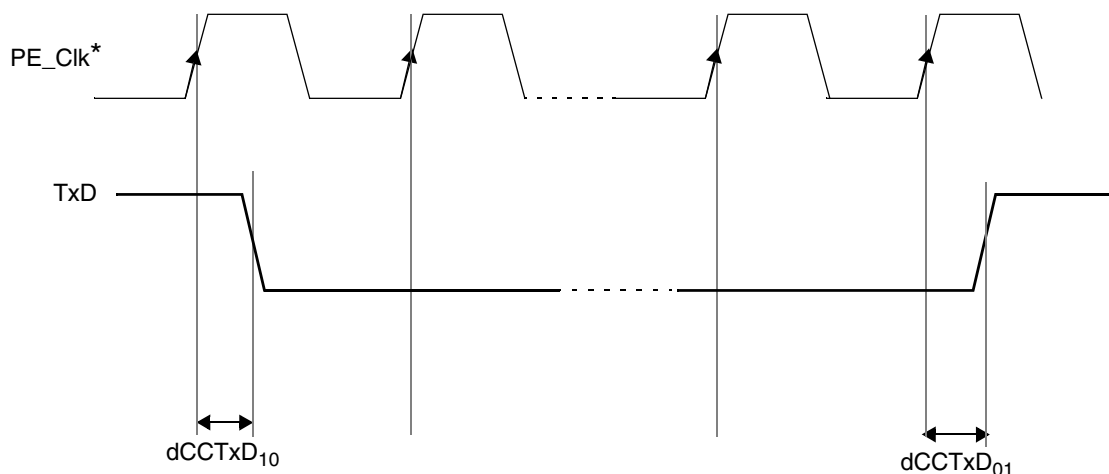
| Name | Description ¹ | Min | Max | Unit |
|--|--|-------|------|------|
| dCCTxAsym | Asymmetry of sending CC @ 25 pF load (=dCCTxD _{50%} - 100 ns) | -2.45 | 2.45 | ns |
| dCCTxD _{RISE25} +dCCTxD _{FALL25} | Sum of Rise and Fall time of TxD signal at the output | - | 9 | ns |

Table continues on the next page...

Table 40. TxD output characteristics (continued)

| Name | Description ¹ | Min | Max | Unit |
|----------------------|--|-----|-----|------|
| dCCTxD ₀₁ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | - | 25 | ns |
| dCCTxD ₁₀ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | - | 25 | ns |

1. TxD pin load maximum 25 pF.



*FlexRay Protocol Engine Clock

Figure 34. TxD signal propagation delays

6.5.4.4 RxD

Table 41. RxD input characteristics

| Name | Description | Min | Max | Unit |
|----------------------|---|-----|-----|------|
| C_CCRxD | Input capacitance on RxD pin | - | 7 | pF |
| uCCLogic_1 | Threshold for detecting logic high | 35 | 70 | % |
| uCCLogic_0 | Threshold for detecting logic low | 30 | 65 | % |
| dCCRxD ₀₁ | Sum of delay from actual input to the D input of the first FF, rising edge | - | 10 | ns |
| dCCRxD ₁₀ | Sum of delay from actual input to the D input of the first FF, falling edge | - | 10 | ns |

6.5.5 Ethernet Controller (ENET) Parameters

6.5.5.1 Ethernet Switching Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. For MII and RMII mode, output load is equal to 25 pF and pad settings are $SIUL2_MSCRn[DSE] = 101$ and $SIUL2_MSCRn[SRE] = 11$. For RGMII, output load is 5 pF and pad settings are $SIUL2_MSCRn[DSE] = 111$ and $SIUL2_MSCRn[SRE] = 11$.

NOTE

These are not necessarily the default configuration after chip resets. You must ensure the above chip configuration to match the measurements in this section.

6.5.5.2 Receive and Transmit signal timing specifications for RMII interfaces

This section provides timing specifications that meet the requirements for RMII interfaces for a range of transceiver devices.

Table 42. Receive signal timing for RMII interfaces

| Symbol | Characteristic | RMII Mode | | Unit |
|--------|---|-----------|-----|-----------------|
| | | Min | Max | |
| — | EXTAL frequency (RMII input clock RMII_CLK) | — | 50 | MHz |
| E3, E7 | RMII_CLK pulse width high | 35% | 65% | RMII_CLK period |
| E4, E8 | RMII_CLK pulse width low | 35% | 65% | RMII_CLK period |
| E1 | RXD[1:0], CVS_DV, RXER to RMII_CLK setup | 4 | — | ns |
| E2 | RMII_CLK to RXD[1:0], CRS_DV, RXER hold | 2 | — | ns |
| E6 | RMII_CLK to TXD[1:0], TXEN valid | — | 14 | ns |
| E5 | RMII_CLK to TXD[1:0], TXEN invalid | 2 | — | ns |

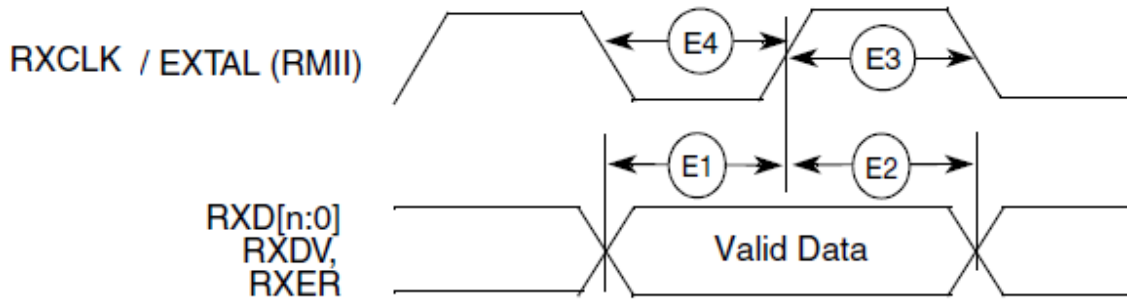


Figure 35. RMIi receive signal timing diagram

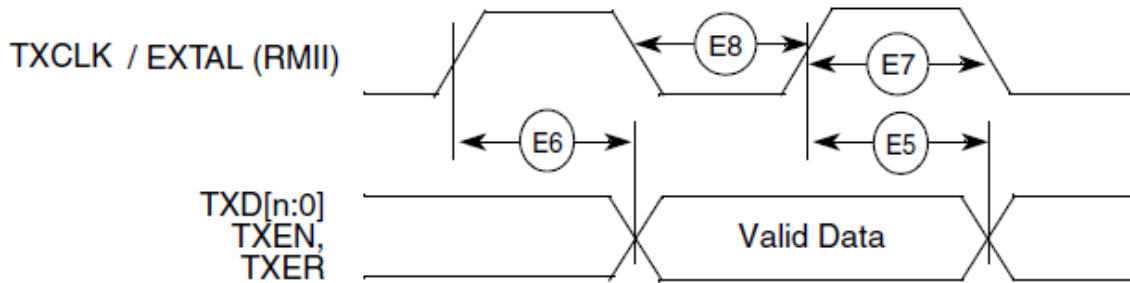


Figure 36. RMIi transmit signal timing diagram

6.5.5.3 Receive and Transmit signal timing specifications for MII interfaces

This section provides timing specifications that meet the requirements for MII interfaces for a range of transceiver devices.

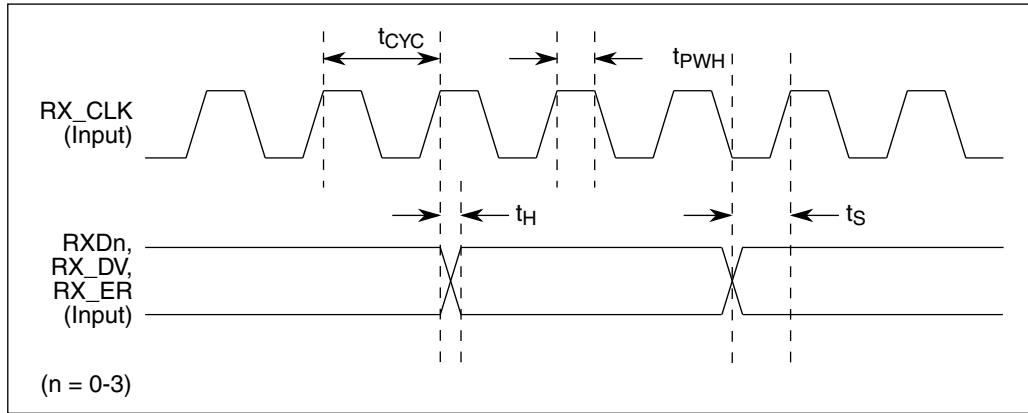


Figure 37. MII receive signal timing diagram

Table 43. Receive signal timing for MII interfaces

| Characteristic | Symbol | MII Mode | | | Unit |
|--------------------------------------|-----------|----------|--------|-----|------|
| | | Min | Typ | Max | |
| RX_CLK clock period (100/10 MBPS) | t_{CYC} | - | 40/400 | - | ns |
| RX_CLK duty cycle, t_{PWH}/t_{CYC} | - | 35 | 50 | 65 | % |
| Input setup time before RX_CLK | t_S | 5 | - | - | ns |
| Input hold time after RX_CLK | t_H | 5 | - | - | ns |

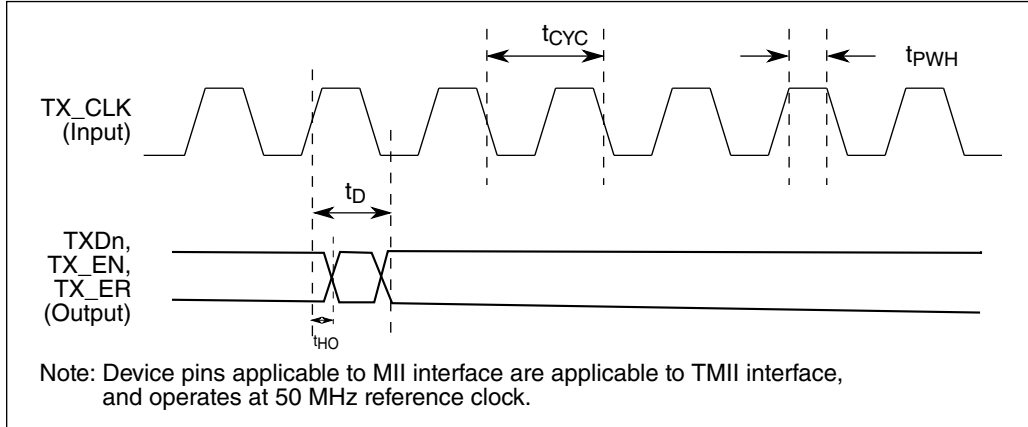


Figure 38. MII transmit signal timing diagram

Table 44. Transmit signal timing for MII interfaces

| Characteristic | Symbol | MII Mode | | | Unit |
|--------------------------------------|-----------|----------|--------|-----|------|
| | | Min | Typ | Max | |
| TX_CLK clock period (100/10 MBPS) | t_{CYC} | - | 40/400 | - | ns |
| TX_CLK duty cycle, t_{PWH}/t_{CYC} | - | 35 | 50 | 65 | % |
| TX_CLK to Output Valid | t_D | - | - | 25 | ns |
| TX_CLK to Output Invalid | t_{HO} | 2 | - | - | ns |

6.5.5.4 Receive and Transmit signal timing specifications for RGMII interfaces

This section provides timing specs that meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 45. Receive signal timing for RGMII interfaces

| Characteristic | Symbol | RGMII Mode | | | Unit |
|--|--------------------------|------------|-----|------|------|
| | | Min | Typ | Max | |
| Clock cycle duration | T_{cyc} ¹ | 7.2 | — | 8.8 | ns |
| Data to clock output skew at transmitter | T_{skewT} ² | -500 | — | 500 | ps |
| Data to clock input skew at receiver | T_{skewR} ³ | 1 | — | 2.6 | ns |
| Duty cycle for Gigabit | Duty_G ³ | 45 | — | 55 | % |
| Duty cycle for 10/100T | Duty_T ³ | 40 | — | 60 | % |
| Rise/fall time (20–80%) | Tr/Tf | - | — | 0.75 | ns |

- For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.
- For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.5 ns and less than 2 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{cyc} of the lowest speed transitioned between.

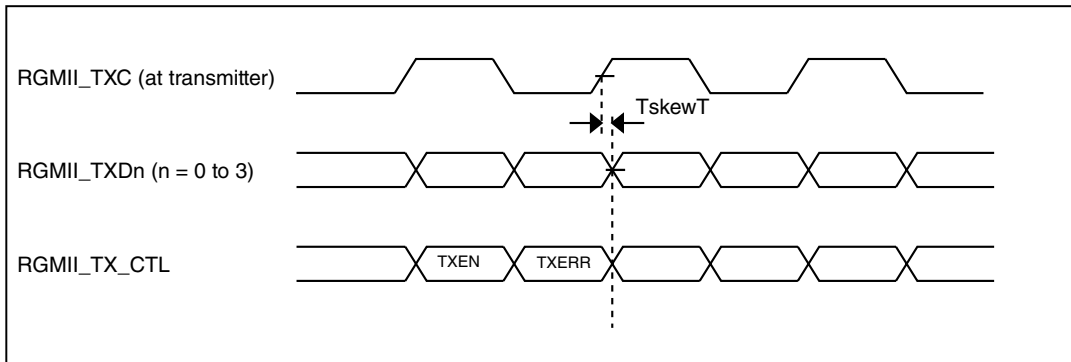


Figure 39. RGMII Transmit signal timing diagram original

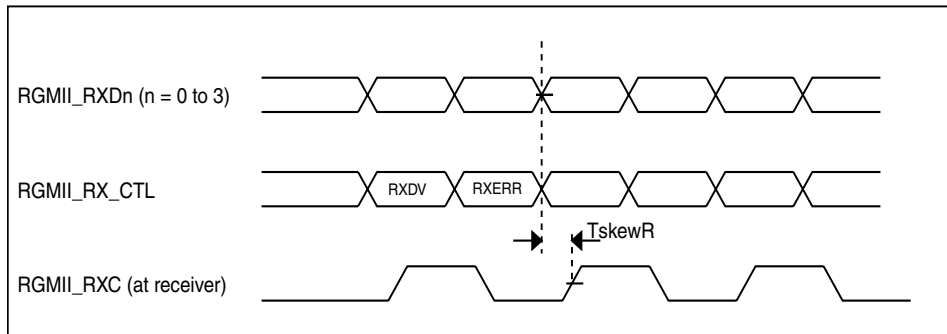


Figure 40. RGMII Receive signal timing diagram original

6.5.5.5 MII/RMII Serial Management channel timing (MDC/MDIO)

Output load is equal to 45 pF and pad settings are SIUL2_MSCRn[DSE] = 101 and SIUL2_MSCRn[SRE] = 11.

NOTE

These are not necessarily the default configuration after chip resets. You must ensure the above chip configuration to match the measurements in this section.

Ethernet works with a maximum frequency of MDC at 2.5 MHz. ENET_MSCR [HOLDTIME] should be set to 010 when Module Clock = 133 MHz. MDIO pin must have external pull up.

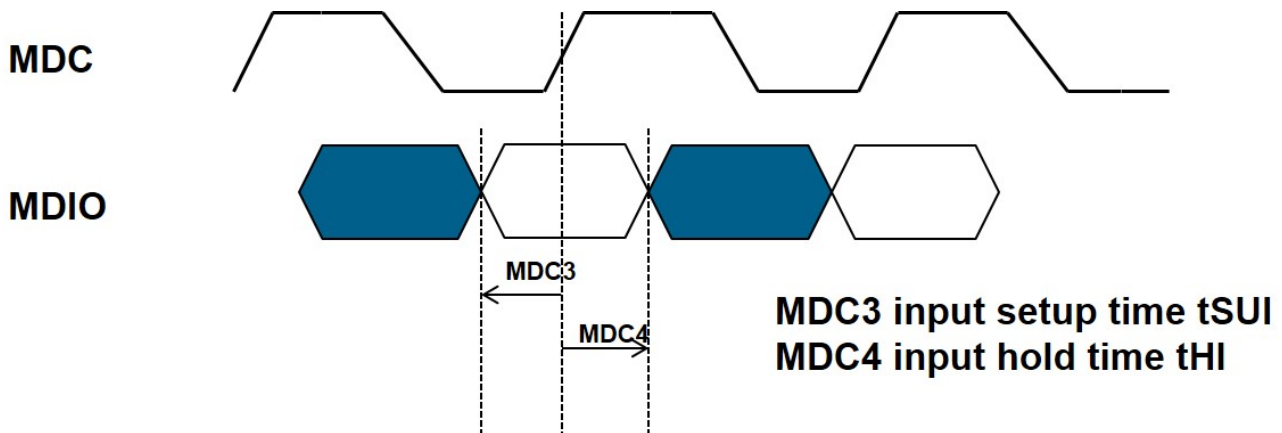


Figure 41. MDIO input timing

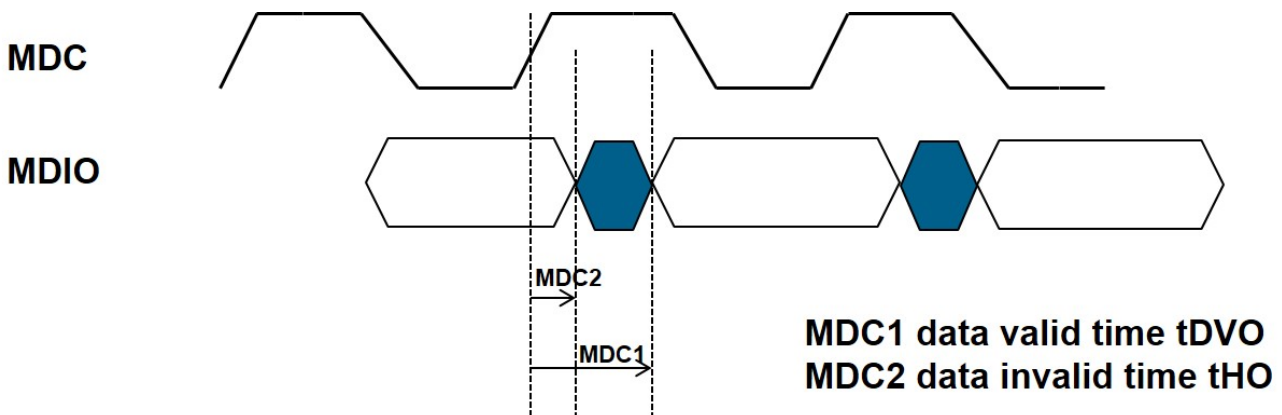


Figure 42. MDIO output timing

Table 46. MDIO interface timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|------|------------------|-----------|-----|-----|------|
| MDCO | Clock Duty Cycle | t_{MDC} | 40 | 60 | % |

Table continues on the next page...

Table 46. MDIO interface timing specification (continued)

| ID | Parameter | Symbols | Min | Max | Unit |
|--------------------|-----------------------|-----------|-----|-----|------|
| MDIO Output Timing | | | | | |
| MDC1 | MDC to MDIO Valid | t_{DVO} | — | 50 | ns |
| MDC2 | MDC to MDIO Invalid | t_{HO} | 10 | — | ns |
| MDIO Input Timing | | | | | |
| MDC3 | MDIO Input Setup time | t_{SUI} | 50 | — | ns |
| MDC4 | MDIO Input Hold time | t_{HI} | 0 | — | ns |

6.5.6 PCI Express specifications

The PCI Express link conforms to the *PCI Express Base Specification*, Revision 2.1. The following summary of Transmitter and Receiver specifications are copied directly from the Base Specification. Consult the Base Specification for additional details.

Table 47. PCI Express transmitter specifications¹

| Symbol | Parameter | 2.5 GT/s | 5.0 GT/s | Units |
|-----------------------------------|--|------------------------------|------------------------------|--------|
| UI | Unit Interval | 399.88 (min) 400.12 (max) | 199.94 (min) 200.06 (max) | ps |
| $V_{TX-DIFF-PP}$ | Differential p-p Tx voltage swing | 0.8 (min) 1.2 (max) | 0.8 (min) 1.2 (max) | V |
| $V_{TX-DE-RATIO-3.5dB}$ | Tx de-emphasis level ratio | 3.0 (min) 4.0 (max) | 3.0 (min) 4.0 (max) | dB |
| $V_{TX-DE-RATIO-6dB}$ | Tx de-emphasis level | N/A | 5.5 (min) 6.5 (max) | dB |
| $T_{MIN-PULSE}$ | Instantaneous lone pulse width | Not specified | 0.9 (min) | UI |
| T_{TX-EYE} | Transmitter Eye including all jitter sources | 0.75 (min) | 0.75 (min) | UI |
| $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and max deviation from the median | 0.125 (max) | Not specified | UI |
| $T_{TX-HF-DJ-DD}$ | Tx deterministic jitter > 1.5 MHz | Not specified | 0.15 (max) | UI |
| $T_{TX-LF-RMS}$ | Tx RMS jitter < 1.5 MHz | Not specified | 3.0 | ps RMS |
| BW_{TX-PLL} | Maximum Tx PLL bandwidth | 22 (max) | 16 (max) | MHz |
| $BW_{TX-PLL-LO-3dB}$ | Minimum Tx PLL BW for 3 dB peaking | 1.5 (min) | 8 (min) | MHz |
| $BW_{TX-PLL-LO-1dB}$ | Minimum Tx PLL BW for 1 dB peaking | Not specified | 5 (min) | MHz |
| $PKG_{TX-PLL2}$ | Tx PLL peaking with 5 MHz min BW | Not specified | 1.0 (max) | dB |

- See Table 4-9 2.5 and 5.0 GT/s Transmitter Specifications in PCI Express Base Specification for further details.

Table 48. PCI Express receiver specifications¹

| Symbol | Parameter | 2.5 GT/s | 5.0 GT/s | Units |
|---------------------|---|------------------------------|------------------------------|-------|
| UI | Unit Interval | 399.88 (min) 400.12 (max) | 199.94 (min) 200.06 (max) | ps |
| $V_{RX-DIFF-PP-CC}$ | Differential Rx peak-peak voltage for common Refclk Rx architecture | 0.175 (min) 1.2 (max) | 0.120 (min) 1.2 (max) | V |
| T_{RX-EYE} | Receiver eye time opening | 0.40 (min) | N/A | UI |
| $T_{RX-TJ-CC}$ | Max Rx inherent timing error | N/A | 0.40 (max) | UI |
| $T_{RX-DJ-DD-CC}$ | Max Rx inherent deterministic timing error | N/A | 0.30 (max) | UI |

- See Table 4-12 2.5 and 5.0 GT/s Receiver Specifications in PCI Express Base Specification for further details.

6.5.7 IIC timing

Table 49. IIC SCL and SDA input timing specifications

| Number | Symbol | | Parameter | Value | | Unit |
|--------|--------|---|--|---|-----|---------------------------|
| | | | | Min | Max | |
| 1 | — | D | Start condition hold time | 2 | — | IP bus cycle ¹ |
| 2 | — | D | Clock low time | 8 | — | IP bus cycle ¹ |
| 4 | — | D | Data hold time | 25 | — | ns |
| 6 | — | D | Clock high time | 4 | — | IP bus cycle ¹ |
| 7 | — | D | Data setup time | 250 (standard mode); 100 (fast mode) ² | | ns |
| 8 | — | D | Start condition setup time (for repeated start condition only) | 2 | — | IP bus cycle ¹ |
| 9 | — | D | Stop condition setup time | 2 | — | IP bus cycle ¹ |

- Inter Peripheral Clock is the clock at which the IIC peripheral is working in the device

2. pg_clk frequency should be greater than 5 MHz for standard mode and 20 MHz for fast mode.

Table 50. IIC SCL and SDA output timing specifications

| Number | Symbol | | Parameter | Value | | Unit |
|----------------|--------|---|--|-------|------|---------------------------|
| | | | | Min | Max | |
| 1 ¹ | — | D | Start condition hold time | 6 | — | IP bus cycle ² |
| 2 ¹ | — | D | Clock low time | 10 | — | IP bus cycle ¹ |
| 3 ³ | — | D | SCL/SDA rise time | — | 99.6 | ns |
| 4 ¹ | — | D | Data hold time | 7 | — | IP bus cycle ¹ |
| 5 ¹ | — | D | SCL/SDA fall time | — | 99.5 | ns |
| 6 ¹ | — | D | Clock high time | 10 | — | IP bus cycle ¹ |
| 7 ¹ | — | D | Data setup time | 2 | — | IP bus cycle ¹ |
| 8 ¹ | — | D | Start condition setup time (for repeated start condition only) | 20 | — | IP bus cycle ¹ |
| 9 ¹ | — | D | Stop condition setup time | 11 | — | IP bus cycle ¹ |

1. Programming IBFD (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.
2. Inter Peripheral Clock is the clock at which the I2C peripheral is working in the device.
3. Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pullup resistor values.

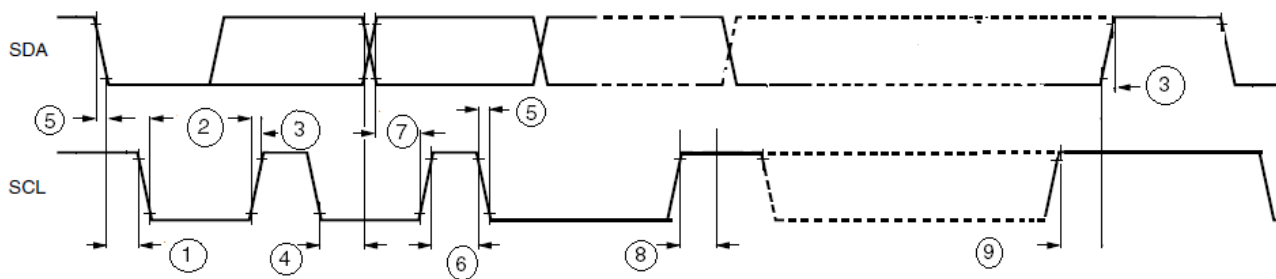


Figure 43. IIC input/output timing

6.5.8 LINFlex timing

The maximum bit rate is 1.875 MBit/s.

6.6 Display modules

6.6.1 Display Control Unit (2D-ACE) Parameters

6.6.1.1 Interface to TFT panels

This section provides the LCD interface timing for a generic active matrix color TFT panel.

Measurements are with a load of 20 pF on output pins. Input slew = 1 ns, SIUL2_MSCR n [DSE] = 111, and SIUL2_MSCR n [SRE] = 11.

NOTE

These are not necessarily the default configuration after chip resets. You must ensure the above chip configuration to match the measurements in this section.

In the figure below¹, signals are shown with positive polarity. The sequence of events for active matrix interface timing:

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 150 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

1. LD[23:0]" signal is "line data," an aggregation of the 2D-ACE's RGB signals—R[0:7], G[0:7] and B[0:7].

Display modules

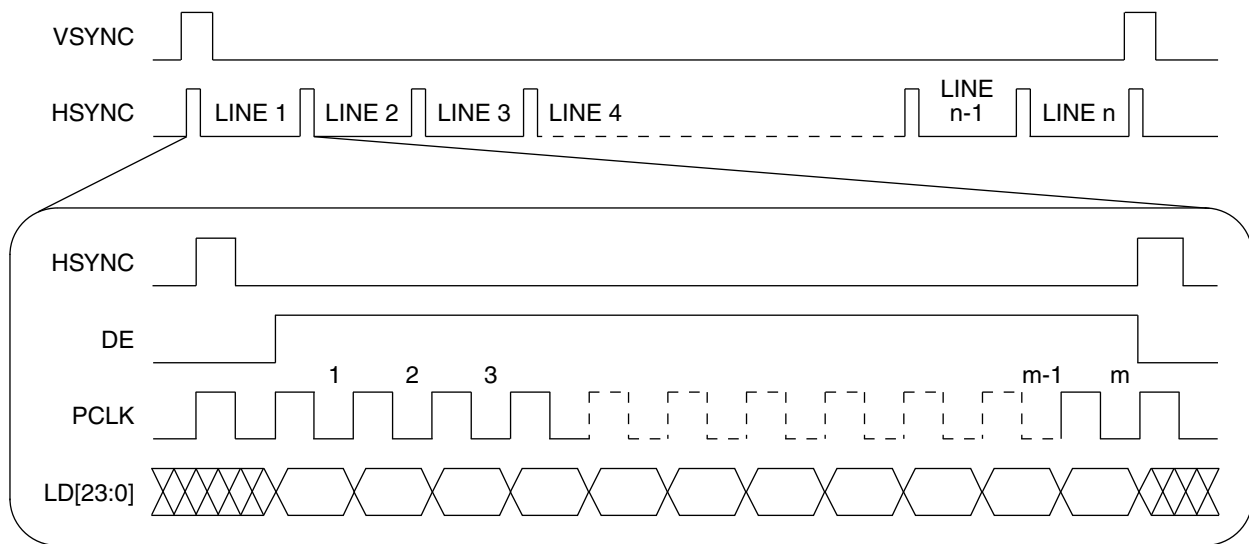


Figure 44. TFT LCD interface timing overview

6.6.1.2 Interface to TFT LCD Panels—Pixel Level Timings

This section provides the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the figure below are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high. Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the clock divide . The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

Table 51. LCD interface timing parameters—horizontal and vertical

| Symbol | Characteristic | | Unit |
|-----------|----------------------------|--|------|
| t_{PCP} | Display pixel clock period | 6.66 | ns |
| t_{PWH} | HSYNC pulse width | $PW_H * t_{PCP}$ | ns |
| t_{BPH} | HSYNC back porch width | $BP_H * t_{PCP}$ | ns |
| t_{FPH} | HSYNC front porch width | $FP_H * t_{PCP}$ | ns |
| t_{SW} | Screen width | $DELTA_X * t_{PCP}$ | ns |
| t_{HSP} | HSYNC (line) period | $(PW_H + BP_H + FP_H + DELTA_X) * t_{PCP}$ | ns |
| t_{PWV} | VSYNC pulse width | $PWV * t_{HSP}$ | ns |
| t_{BPV} | VSYNC back porch width | $BP_V * t_{HSP}$ | ns |
| t_{FPV} | VSYNC front porch width | $FP_V * t_{HSP}$ | ns |

Table continues on the next page...

Table 51. LCD interface timing parameters—horizontal and vertical (continued)

| Symbol | Characteristic | | Unit |
|-----------|----------------------|--|------|
| t_{SH} | Screen height | $DELTA_Y * t_{HSP}$ | ns |
| t_{VSP} | VSYNC (frame) period | $(PW_V + BP_V + FP_V + DELTA_Y) * t_{HSP}$ | ns |

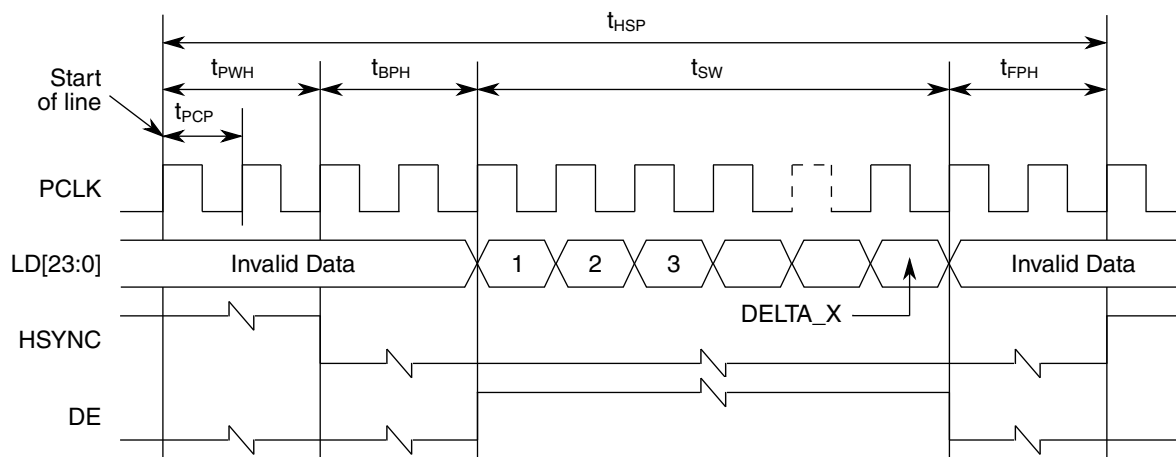


Figure 45. Horizontal sync timing

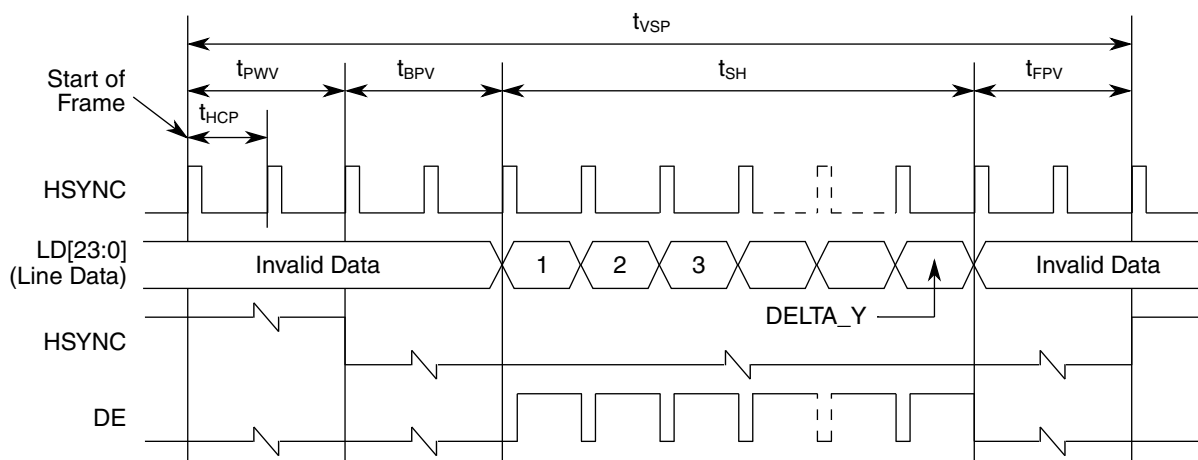


Figure 46. Vertical sync pulse

6.6.1.3 Interface to TFT LCD panels—access level

This section provides the access level timing parameters of the LCD interface.

Table 52. LCD Interface Timing Parameters—Access Level

| Symbol | Description | Min | Max | Unit |
|-----------|---|------|-----|------|
| t_{CKP} | Pixel Clock Period | 6.66 | — | ns |
| t_{DV} | TFT interface data valid after pixel clock | — | 3 | ns |
| t_{DV} | TFT interface HSYNC valid after pixel clock | — | 3 | ns |

Table continues on the next page...

Table 52. LCD Interface Timing Parameters—Access Level (continued)

| Symbol | Description | Min | Max | Unit |
|----------|--|-----|-----|------|
| t_{DV} | TFT interface VSYNC valid after pixel clock | — | 3 | ns |
| t_{DV} | TFT interface DE valid after pixel clock | — | 3 | ns |
| t_{HO} | TFT interface output hold time for data and control bits | 0 | — | ns |
| | Relative skew between the data bits | — | 1.5 | ns |

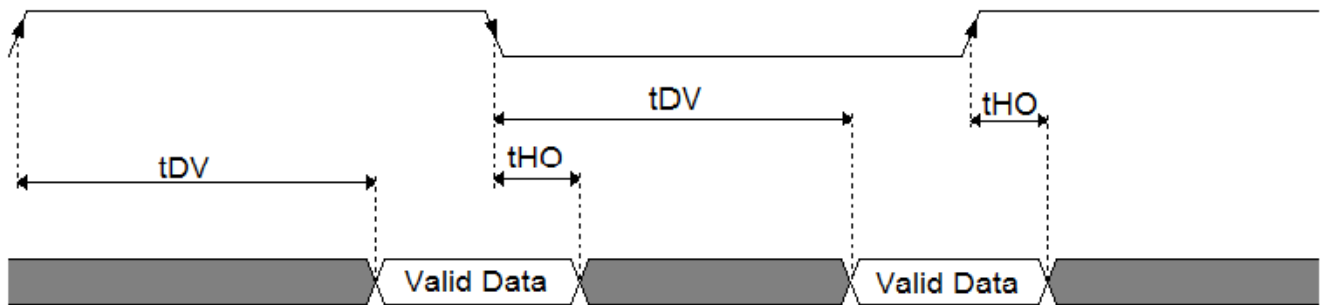


Figure 47. LCD Interface Timing Parameters—Access Level

6.6.2 Video input unit (VIU) timing specifications

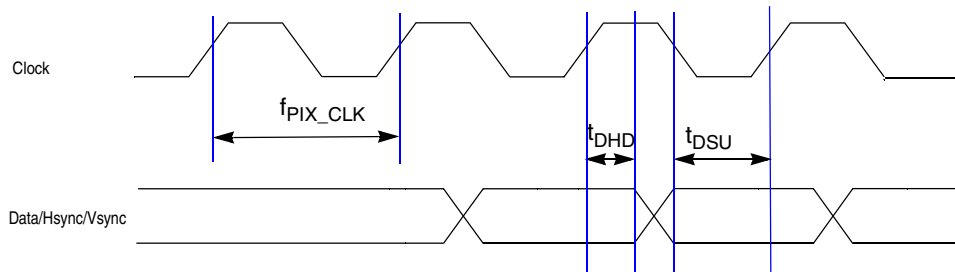


Figure 48. VIU timing diagram

Table 53. VIU timing parameters

| Parameter | Description | Min | Typ | Max | Unit |
|---------------|---------------------------------|-----|-----|-----|------|
| f_{PIX_CK} | VIU pixel clock frequency | — | — | 100 | MHz |
| t_{DSU} | VIU Data/Hsync/Vsync setup time | 3 | — | — | ns |
| t_{DHD} | VIU Data/Hsync/Vsync hold time | 1 | — | — | ns |

6.6.3 MIPICSI2 D-PHY electrical and timing parameters

The MIPICSI2 D-PHY² is compliant with MIPICSI2 version 1.0, D-PHY specification Rev. 1.01.00 (for MIPICSI2 sensor port x4 lanes)

6.6.3.1 Electrical and timing Information

Table 54. Electrical and timing Information

| Symbol | Parameters | Test conditions | Min | Typ | Max | Unit |
|---|--|-----------------|-----|-----|-----|------|
| HS Line Receiver DC Specifications | | | | | | |
| V _{IDTH} | Differential input high voltage threshold | | - | - | 70 | mV |
| V _{IDTL} | Differential input low voltage threshold | | -70 | - | - | mV |
| V _{IHHS} | Single ended input high voltage | | - | - | 460 | mV |
| V _{ILHS} | Single ended input low voltage | | -40 | - | - | mV |
| V _{CMRXDC} | Input common mode voltage | | 70 | - | 330 | mV |
| V _{TERM-EN} | Single-ended threshold for HS termination enable | | - | - | 450 | mV |
| Z _{ID} | Differential input impedance | | 80 | - | 125 | ohm |
| LP Line Receiver DC Specifications | | | | | | |
| V _{ILLP} | Input low voltage | | - | - | 550 | mV |
| V _{IHLP} | Input high voltage | | 880 | - | - | mV |
| V _{IL-ULPS} | Input low voltage (ultra low power state) | | - | - | 300 | mV |
| V _{HYST} | Input hysteresis | | 25 | - | - | mV |

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6.6.3.2 D-PHY signaling levels

The signal levels are different for differential HS mode and single-ended LP mode. The figure below shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

Table 55. D-PHY RX calibrator specifications

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|---|-----|-----|-----|------|
| REXT | External reference resistor, 1% accuracy, for autocalibration | - | 15 | - | KΩ |
| T cal | Time from when PD_RX signal goes low to when CALCOMPL goes high | - | 2 | - | μs |

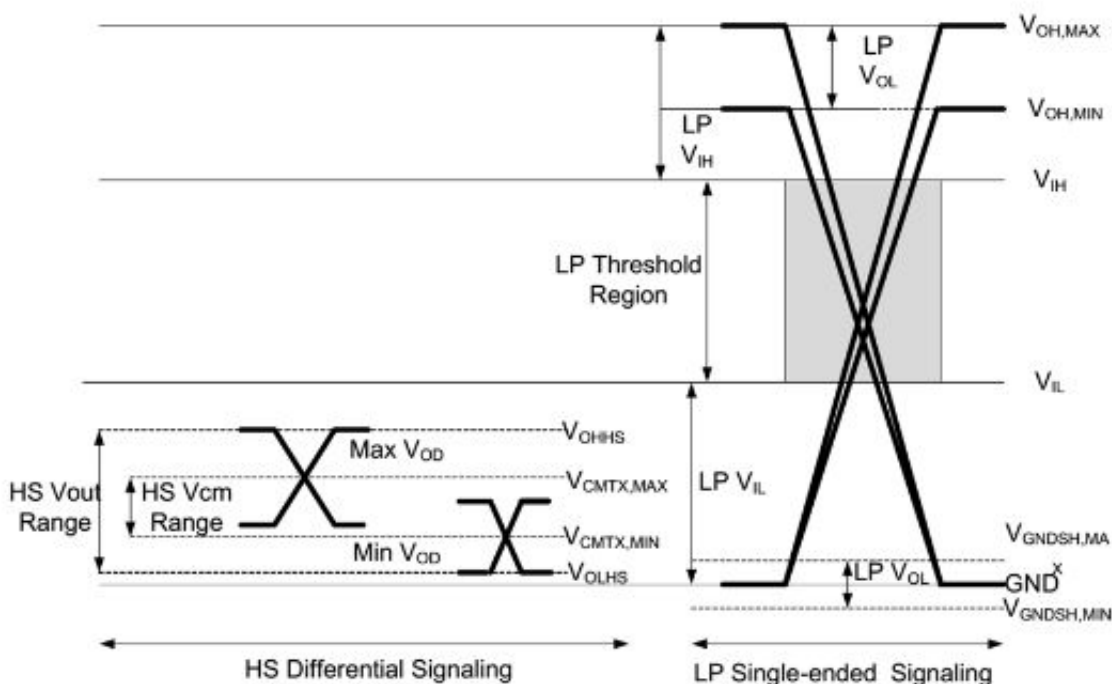


Figure 49. D-PHY signaling levels

6.6.3.3 D-PHY switching characteristics

Table 56. D-PHY switching characteristics

| Symbol | Parameters | Test conditions | Min | Typ | Max | Unit |
|---|------------|-----------------|-----|-----|-----|------|
| HS Line Receiver AC Specifications | | | | | | |

Table continues on the next page...

Table 56. D-PHY switching characteristics (continued)

| Symbol | Parameters | Test conditions | Min | Typ | Max | Unit |
|--|--|--|-----|-----|------|------|
| - | Maximum serial data rate | On DATAP/N inputs. 80 OHM<= RL <= 125 OHM | 80 | - | 1500 | Mbps |
| Δ VCMRX(HF) | Common mode interference beyond 450 MHz | | - | - | 100 | mVpp |
| Δ VCMRX(LF) | Common mode interference between 50 MHz and 450 MHz | | -50 | - | 50 | mVpp |
| CCM | Common mode termination | | - | - | 60 | pF |
| LP Line Receiver AC Specification | | | | | | |
| eSPIKE | Input pulse rejection | | - | - | 300 | Vps |
| TMIN | Minimum pulse response | | 20 | - | - | ns |
| VINT | Pk-to-Pk interference voltage | | - | - | 200 | mV |
| fINT | Interference frequency | | 450 | - | - | MHz |

6.6.3.4 Low-Power Receiver timing

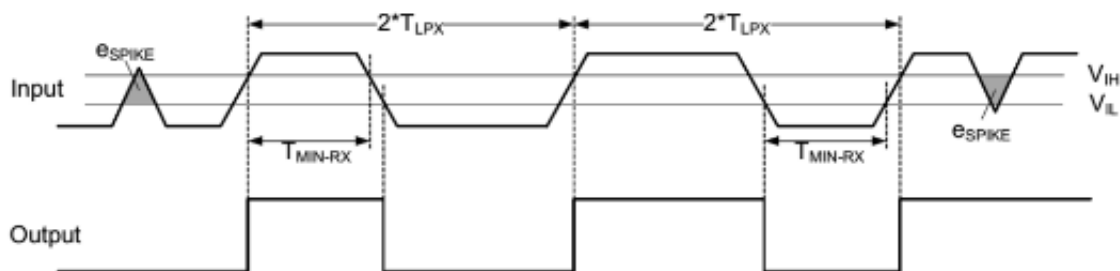


Figure 50. Input Glitch Rejection of Low-Power Receivers

6.6.3.5 Data to Clock timing

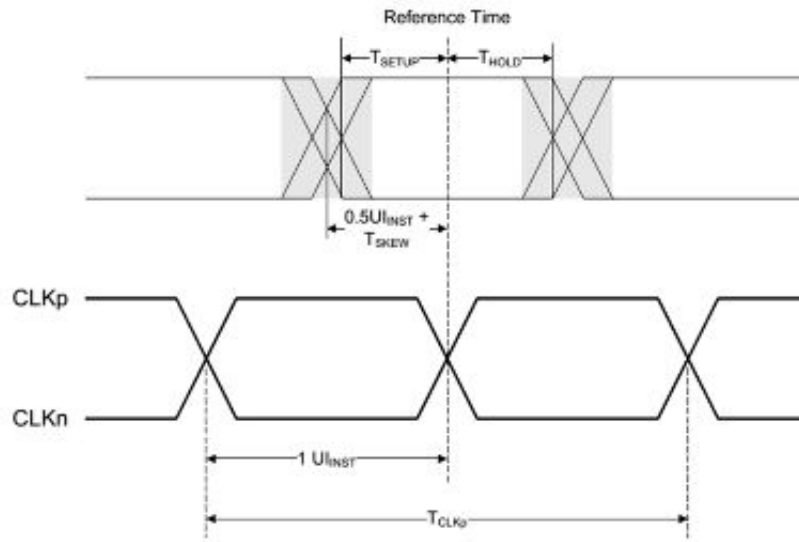


Figure 51. Data to Clock timing definition

Table 57. Data to Clock timing specifications

| Symbol | Parameters | Test conditions | Min | Typ | Max | Unit |
|--------------------|--------------------------|-----------------|-------------------|-----|------|--------------------|
| TCLK _P | Clock Period | — | 1.33 | — | 25 | ns |
| UI _{INST} | UI Instantaneous | — | .667 | — | 12.5 | ns |
| T _{SETUP} | Data to Clock Setup Time | — | 0.2 ¹ | — | — | UI _{INST} |
| | | | 0.15 ² | — | — | UI _{INST} |
| T _{HOLD} | Clock to Data Hold Time | — | 0.2 ¹ | — | — | UI _{INST} |
| | | | 0.15 ² | — | — | UI _{INST} |

1. when D-PHY is supporting maximum data rate > 1 Gbps.
2. when D-PHY is supporting maximum data rate = 1 Gbps.

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6.7 Debug specifications

6.7.1 JTAG interface timing

Measurements are with a load of 45 pF on output pins. Input slew = 1 ns, SIUL2_MSCR n [DSE] = 101, and SIUL2_MSCR n [SRE] = 11.

NOTE

These are not necessarily the default configuration after chip resets. You must ensure the above chip configuration to match the measurements in this section.

Table 58. JTAG pin AC electrical characteristics¹

| # | Symbol | Characteristic | Min | Max | Unit |
|----|---------------------------------------|--|-----------------|------------------|------|
| 1 | t _{JCYC} | JTAG/SWD TCK Cycle Time ² | 25 ³ | - | ns |
| | | CJTAG TCK Cycle Time | 50 ⁴ | - | ns |
| 2 | t _{JDC} | TCK Clock Pulse Width | 40 | 60 | % |
| 3 | t _{TCKRISE} | TCK Rise and Fall Times (40% - 70%) | - | 1 | ns |
| 4 | t _{TMSS} , t _{TDIS} | TMS, TDI Data Setup Time | 5 | - | ns |
| 5 | t _{TMSH} , t _{TDIH} | TMS, TDI Data Hold Time | 5 | - | ns |
| 6 | t _{TDOV} | TCK Low to TDO Data Valid | - | 18 ⁵ | ns |
| 7 | t _{TDOI} | TCK Low to TDO Data Invalid | 0 | - | ns |
| 8 | t _{TDOHZ} | TCK Low to TDO High Impedance | - | 18 | ns |
| 9 | t _{JCMPW} | JCOMP Assertion Time | 100 | - | ns |
| 10 | t _{JCMPS} | JCOMP Setup Time to TCK Low | 40 | - | ns |
| 11 | t _{BSDV} | TCK Falling Edge to Output Valid | - | 600 ⁶ | ns |
| 12 | t _{BSDVZ} | TCK Falling Edge to Output Valid out of High Impedance | - | 600 | ns |
| 13 | t _{BSDHZ} | TCK Falling Edge to Output High Impedance | - | 600 | ns |
| 14 | t _{BSDST} | Boundary Scan Input Valid to TCK Rising Edge | 15 | - | ns |
| 15 | t _{BSDHT} | TCK Rising Edge to Boundary Scan Input Invalid | 15 | - | ns |

1. These specifications apply to boundary scan, JTAG and CJTAG, and serial wire debug modes.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Cycle time is 25 ns assuming full cycle timing. Cycle time is 50 ns assuming half cycle timing
4. Cycle time is 50 ns assuming full cycle timing. Cycle time is 100 ns assuming half cycle timing
5. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
6. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

Table 59. PCIe JTAG AC electrical characteristics¹

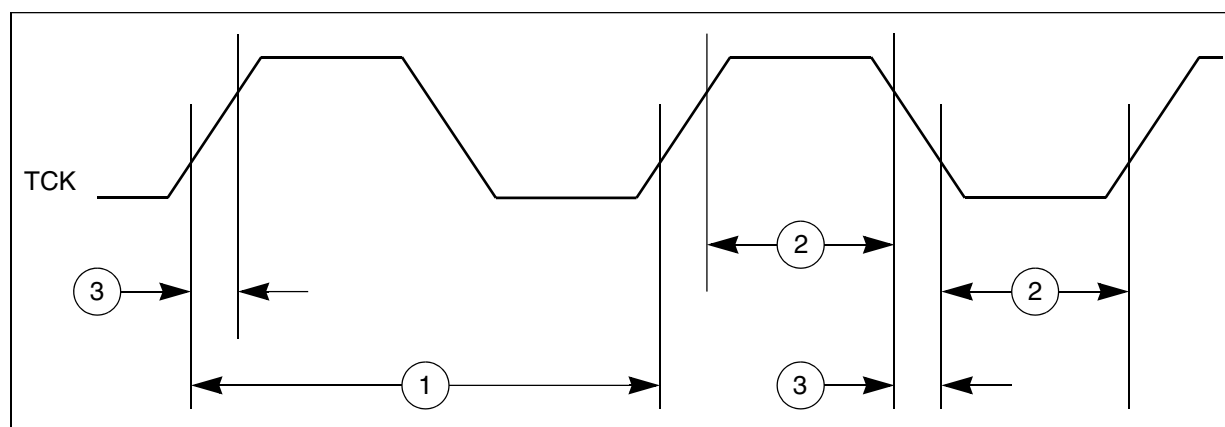
| # | Symbol | Characteristic | Min | Max | Unit |
|---|---------------------------------------|-------------------------------------|-----------------|-----------------|------|
| 1 | t _{JCYC} | TCK Cycle Time ² | 25 ³ | - | ns |
| 2 | t _{JDC} | TCK Clock Pulse Width | 40 | 60 | % |
| 3 | t _{TCKRISE} | TCK Rise and Fall Times (40% - 70%) | - | 1 | ns |
| 4 | t _{TMSS} , t _{TDIS} | TMS, TDI Data Setup Time | 5 | - | ns |
| 5 | t _{TMSH} , t _{TDIH} | TMS, TDI Data Hold Time | 5 | - | ns |
| 6 | t _{TDOV} | TCK Low to TDO Data Valid | - | 21 ⁴ | ns |
| 7 | t _{TDOI} | TCK Low to TDO Data Invalid | 0 | - | ns |
| 8 | t _{TDOHZ} | TCK Low to TDO High Impedance | - | 21 | ns |
| 9 | t _{JCMPW} | JCOMP Assertion Time | 100 | - | ns |

Table continues on the next page...

Table 59. PCIe JTAG AC electrical characteristics¹ (continued)

| # | Symbol | Characteristic | Min | Max | Unit |
|----|-------------|--|-----|------------------|------|
| 10 | t_{JCMPS} | JCOMP Setup Time to TCK Low | 40 | - | ns |
| 11 | t_{BSDV} | TCK Falling Edge to Output Valid | - | 600 ⁵ | ns |
| 12 | t_{BSDVZ} | TCK Falling Edge to Output Valid out of High Impedance | - | 600 | ns |
| 13 | t_{BSDHZ} | TCK Falling Edge to Output High Impedance | - | 600 | ns |
| 14 | t_{BSDST} | Boundary Scan Input Valid to TCK Rising Edge | 15 | - | ns |
| 15 | t_{BSDHT} | TCK Rising Edge to Boundary Scan Input Invalid | 15 | - | ns |

1. These specifications apply to boundary scan, JTAG and CJTAG, and serial wire debug modes.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency.
3. Cycle time is 25 ns assuming full cycle timing. Cycle time is 50 ns assuming half cycle timing.
4. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
5. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

**Figure 52. JTAG test clock input timing**

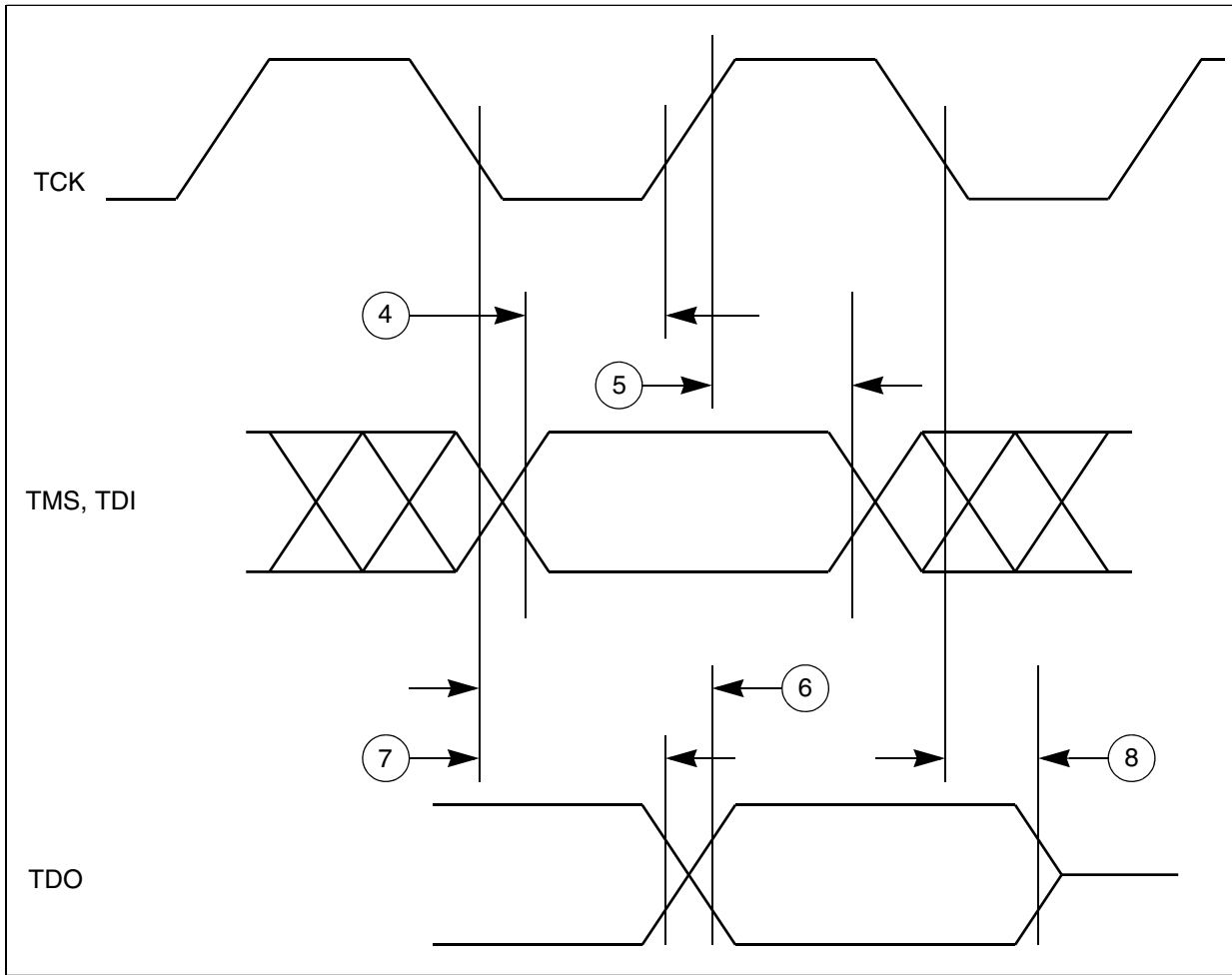


Figure 53. JTAG test access port timing

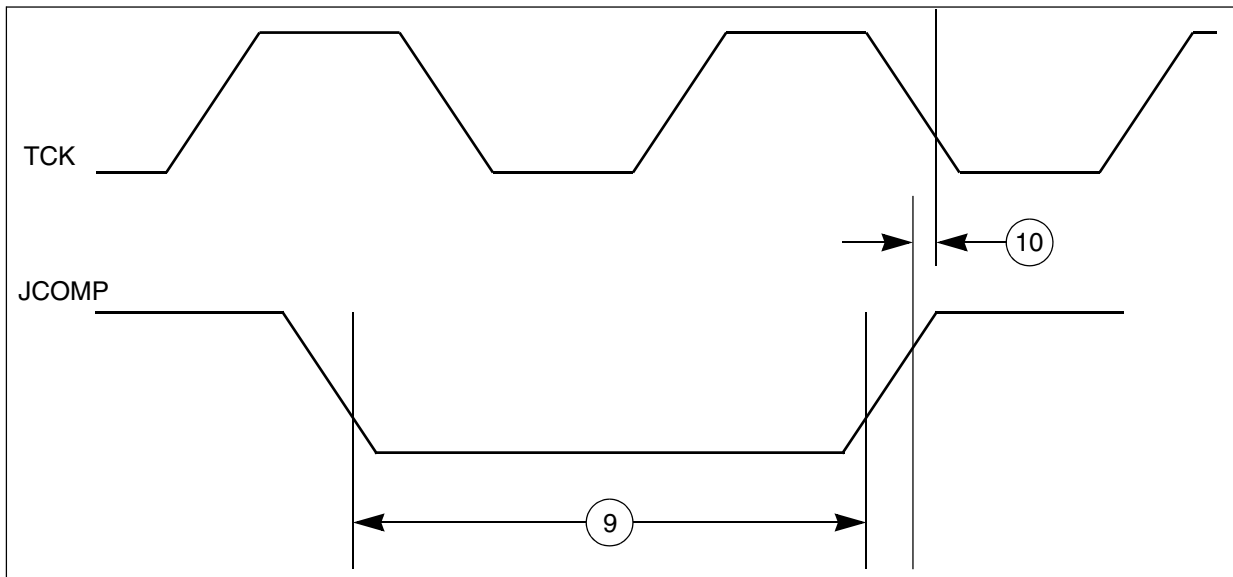


Figure 54. JTAG JCOMP timing

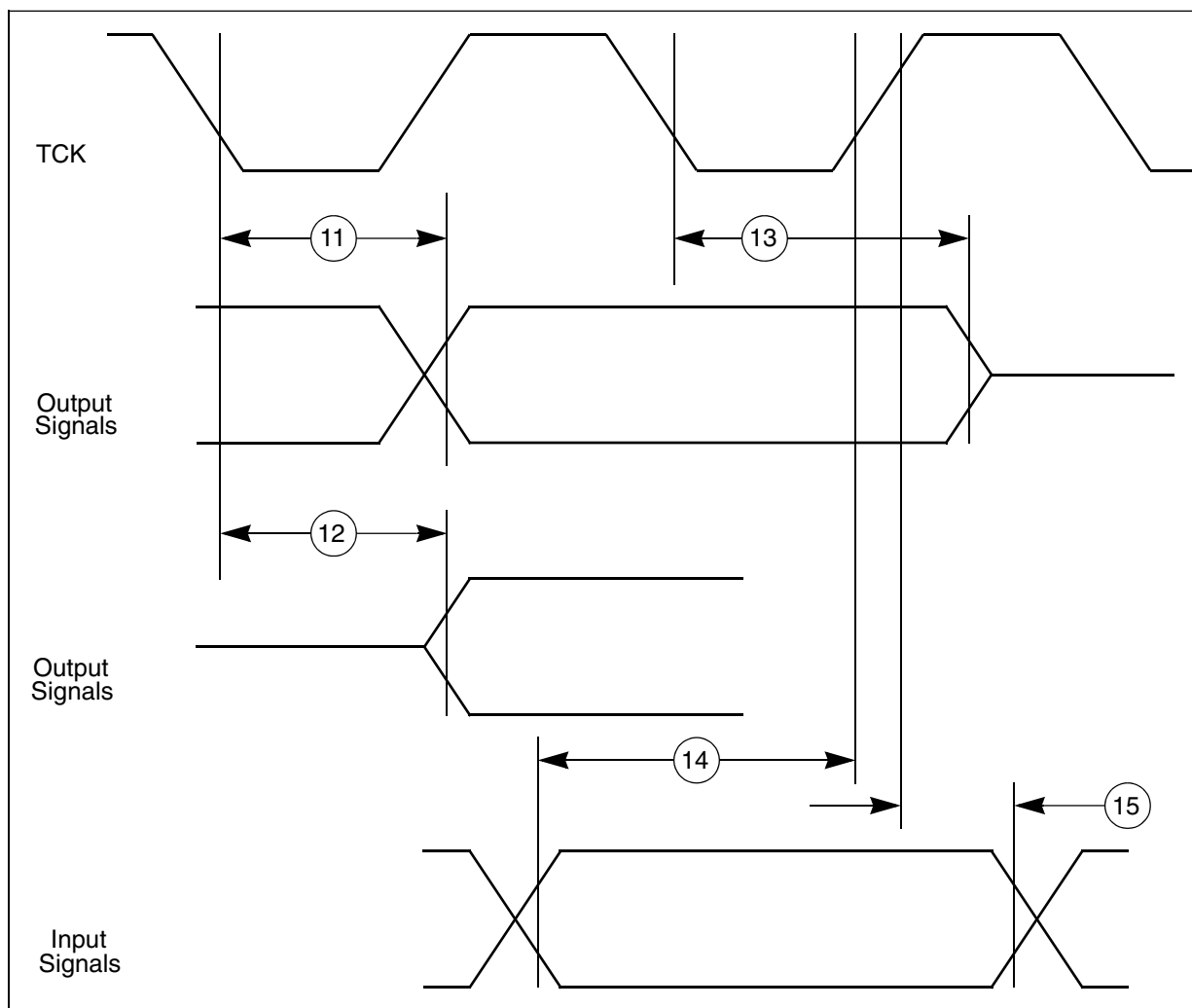


Figure 55. JTAG boundary scan timing

6.7.2 Debug trace timing specifications

Measurements are with a load of 20 pF on output pins. Input slew = 1 ns, SIUL2_MSCRn[DSE] = 111, and SIUL2_MSCRn[SRE] = 11.

NOTE

These are not necessarily the default configuration after chip resets. You must ensure the above chip configuration to match the measurements in this section.

Table 60. Debug trace operating behaviors

| Symbol | Description | Min. | Max. | Typical | Unit |
|------------------|-----------------|------|------|---------|------|
| T _{cyc} | Clock frequency | — | 150 | — | MHz |
| T _{wl} | Low pulse width | 2.8 | — | 2.95 | ns |

Table continues on the next page...

Table 60. Debug trace operating behaviors (continued)

| Symbol | Description | Min. | Max. | Typical | Unit |
|----------|-------------------|------|------|---------|------|
| T_{wh} | High pulse width | 2.8 | — | 2.95 | ns |
| t_{DV} | Data output valid | — | 2.2 | 1.3 | ns |
| t_{HO} | Data output hold | 0 | — | 0 | ns |

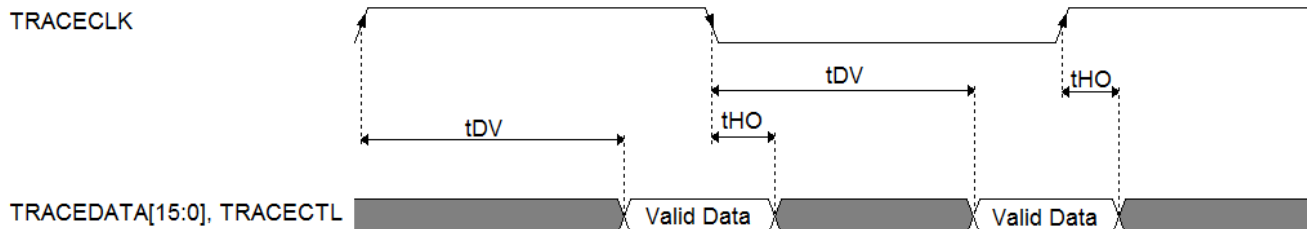


Figure 56. TRACE_CLKOUT specifications

6.8 Wakeup Unit (WKPU) AC specifications

Table 61. WKPU glitch filter specifications

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|----------------------------------|-----|-----|-----|------|
| W_{FNMI} | NMI pulse width that is rejected | - | - | 20 | ns |
| W_{NFNMI} | NMI pulse width that is passed | 400 | - | - | ns |

6.9 RESET pin glitch filter specifications

Table 62. RESET pin glitch filter specifications

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------|------------------------------------|-----|-----|-----|------|
| W_{FRESET} | RESET pulse width that is rejected | - | - | 20 | ns |
| $W_{NFRESET}$ | RESET pulse width that is passed | 400 | - | - | ns |

6.10 External interrupt timing (IRQ pin)

Table 63. External interrupt timing

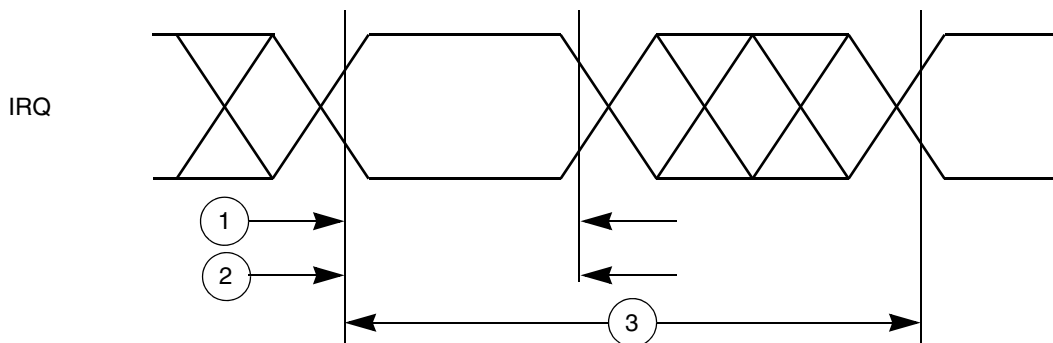
| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|-----|------------|---------------------|------------|-----|-----|-----------|
| 1 | t_{IPWL} | IRQ pulse width low | - | 3 | - | t_{CYC} |

Table continues on the next page...

Table 63. External interrupt timing (continued)

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|-----|------------|------------------------------------|------------|-----|-----|-----------|
| 2 | t_{IPWH} | IRQ pulse width high | - | 3 | - | t_{CYC} |
| 3 | t_{ICYC} | IRQ edge to edge time ¹ | - | 6 | - | t_{CYC} |

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

**Figure 57. External interrupt timing**

7 Thermal attributes

7.1 Thermal attributes

Table 64. Thermal Resistance Data

| Symbol | Parameter | Conditions | Estimate s (w/ Lid) | Unit |
|--------------------|---|-------------------------|---------------------------|-----------------------------|
| $R_{\theta JA}$ | Junction to Ambient Natural Convection ¹ | Single layer board (1s) | 29 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Junction to Ambient Natural Convection ¹ | Four layer board (2s2p) | 18 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta JMA}$ | Junction to Ambient (@200 ft/min) ¹ | Single layer board (1s) | 20 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta JMA}$ | Junction to Ambient (@200 ft/min) ¹ | Four layer board (2s2p) | 13 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta JB}$ | Junction to Board ² | Four layer board (2s2p) | 6 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta JCTop}$ | Junction to Case (Top) ² | Four layer board (2s2p) | 1 | $^{\circ}\text{C}/\text{W}$ |
| | Junction to Lid Top ³ | Four layer board (2s2p) | 0.32 | $^{\circ}\text{C}/\text{W}$ |

1. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
3. Junction-to-Lid-Top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

| Package | Body size | Pitch | NXP document number |
|------------|---------------|---------|---------------------|
| 621 FC-BGA | 17 mm x 17 mm | 0.65 mm | 98ASA00819D |

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1 Reset sequence duration

[Table 65](#) specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in [Reset sequence description](#).

Table 65. RESET sequences¹

| No. | Symbol | Parameter | T _{Reset} | | | Unit |
|-----|-------------------|---|--------------------|-----|-----|------|
| | | | Min | Typ | Max | |
| 1 | T _{DRB} | Destructive Reset Sequence, All LBIST/MBIST enabled | 25 | — | ~50 | ms |
| 2 | T _{DR} | Destructive Reset Sequence, BIST disabled | 50 | — | 90 | μs |
| 3 | T _{ERLB} | External Reset Sequence Long, Unsecure Boot, BIST enabled | 25 | — | ~50 | ms |

Table continues on the next page...

Table 65. RESET sequences¹ (continued)

| No. | Symbol | Parameter | T _{Reset} | | | Unit |
|-----|------------------|---|--------------------|-----|-----|------|
| | | | Min | Typ | Max | |
| 4 | T _{FRL} | Functional Reset Sequence Long, Unsecure Boot, BIST disabled | 50 | — | 90 | μs |
| 5 | T _{FRS} | Functional Reset Sequence Short, Unsecure Boot, BIST disabled | 2 | — | 7 | μs |

1. All the Reset durations assume boot code execution time for Execute-in-place for QuadSPI booting, Unsecure mode with Trimmed FIRC module. Boot code is using execution using PLL and no DCD download is assumed. Secure Boot duration and DCD download time is dependent on the given application image. DCD downloads and application image download/authentication times will be over and above these durations.

10.2 Boot performance matrix

Total Boot execution time will be the addition of DCD execution time to configure DDR and application image download time.

Table 66. Boot execution time

| Boot source | QSPI_CLOCK | CSE_CLOCK | CM4 clock (core counter register clock) | QSPI configuration | SRAM (FAST BOOT) Non secure | DCD execution time for DDR | DDR(FAST BOOT) | DDR(FAST BOOT) | DDR(FAST BOOT) | DDR(FAST BOOT) | Authentication time from DDR | Authentication time from DDR | Authentication time from DDR |
|--------------------------------|------------|-----------|---|--------------------|-----------------------------|----------------------------|----------------|----------------|----------------|----------------|------------------------------|------------------------------|------------------------------|
| Boot Length in bytes | 100 MHz | 133 MHz | 133 MHz | HyperFlash | 4Mbytes | NA | 4 MB | 256 KB | 128 KB | 32 KB | NA | NA | NA |
| Authentication Length in bytes | 100 MHz | 133 MHz | 133 MHz | HyperFlash | NA | NA | NA | NA | NA | NA | 256 KB | 128 KB | 32 KB |
| Time in ms | 100 MHz | 133 MHz | 133 MHz | HyperFlash | 27.302 | 3.47 | 25.347 | 1.63 | 0.819 | 0.211 | 7.416525 | 4.154055 | 1.7064075 |

Reset sequence

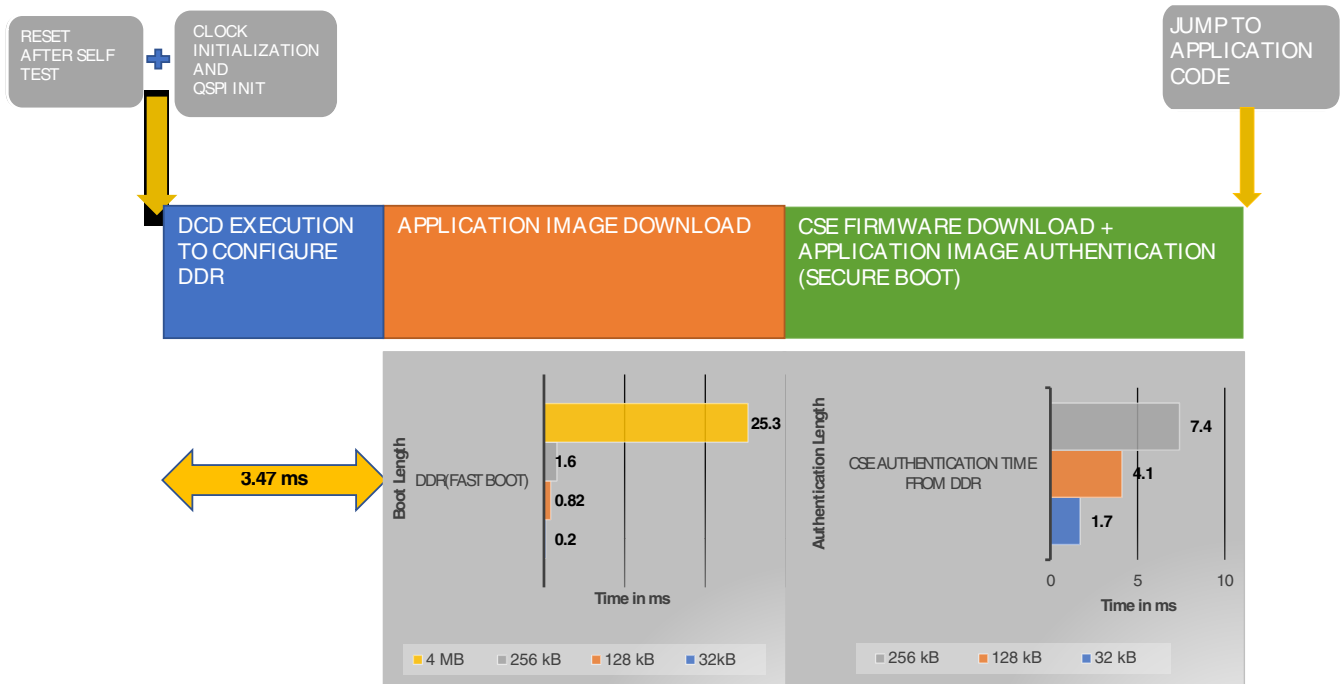


Figure 58. Boot diagram

10.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in [Table 65](#).

The application code execution starts when boot code has finished all the mandatory tasks and jumps over the downloaded image. The download time and authentication time will vary as per Application code image size.

"EXT_POR" pin (Active Low) is required to be de-asserted after external supplies became stable. Deassertion of EXT_POR pin triggers the start of reset sequence.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET (Active-low) signal pin.

NOTE

RESET (Active-low) is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor (10-15 kilohm) which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET (Active-low) in the following figures indicates the time when the device stops

driving it low. The reset sequence durations given in [Table 65](#) are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET (Active-low) asserted low beyond the last Phase3.

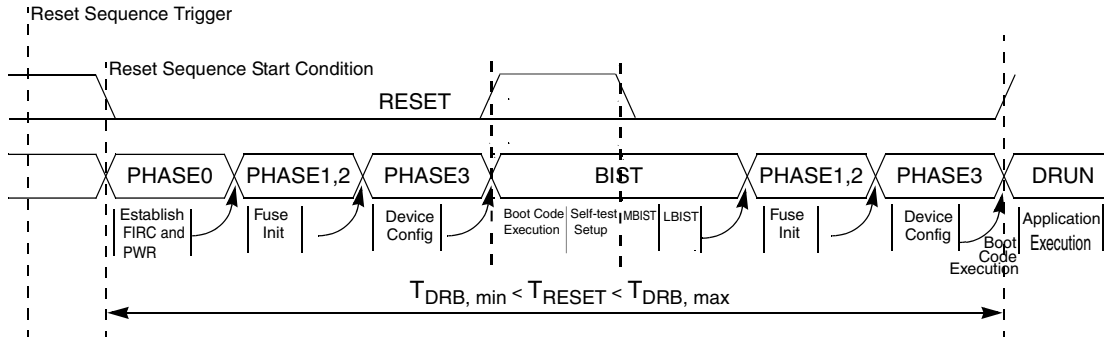


Figure 59. Destructive reset sequence, BIST enabled

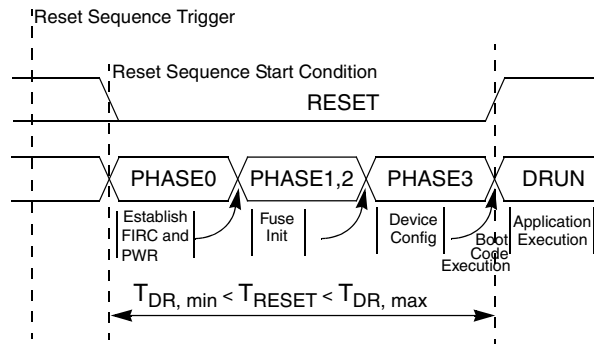


Figure 60. Destructive reset sequence, BIST disabled

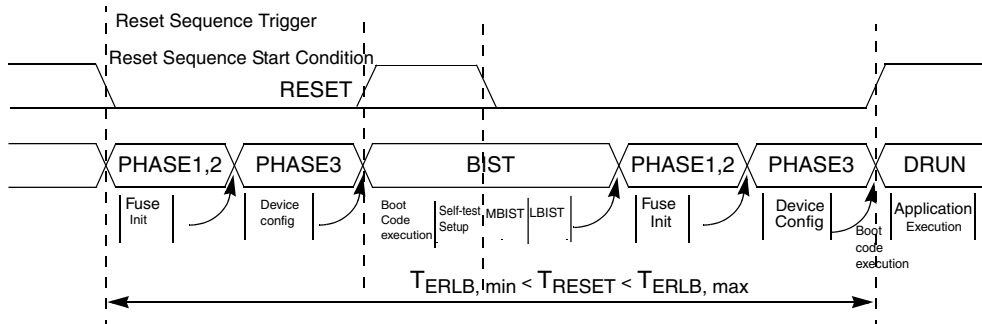


Figure 61. External reset sequence long, BIST enabled

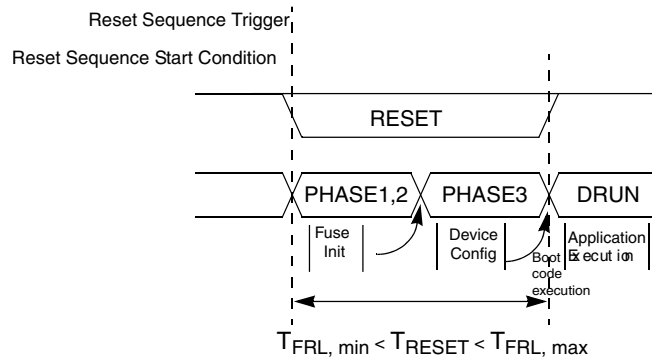


Figure 62. Functional reset sequence long

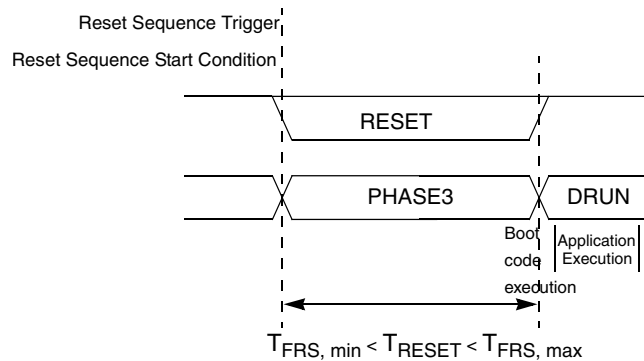


Figure 63. Functional reset sequence short

The reset sequences shown in [Figure 62](#) and [Figure 63](#) are triggered by functional reset events. RESET (Active-low) is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET (Active-low) low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Power sequencing requirements

While designing the system, it is important to take care of following constraints:

- P_{CIE_VP} and P_{CIE_VPH} supplies should be powered up within 50 ms of each other.
- V_{DD_HV_CSI} and V_{DD_LV_CSI} supplies should be powered up within 50 ms of each other.
- V_{REFH_ADC} should never differ from V_{DD_HV_ADV} by more than 100 mV at any time including during power-up or power-down.

- DDR0_VREF0 and DDR1_VREF0 supplies are expected to be 0.5 of $V_{DD_DDR0_IO}$ and $V_{DD_DDR1_IO}$ supplies and are to track $V_{DD_HV_DDR0}$ and $V_{DD_HV_DDR1}$ supply variations as measured at the receiver. Peak-to-Peak noise on DDR0_VREF0 and DDR1_VREF0 supplies should be between +/- 15 mV.
- The maximum rise time for the POR and RESET signal is 1 ms. Very slow ramps can induce bounces in the input read state during the transition from logic low to logic high, which causes the part getting locked in a self-reset loop. Any external noise on this pin can increase the problem.

NOTE

VDD_HV_ADV must be powered for using LFAST interface.

Each supply group mentioned in the table below can be independently powered up/down from the other supply groups. Power supplies in the same group must be powered up/down together. Supply groups belonging to the same supply domain can be ganged together on board level (with appropriate noise isolation) to allow these groups to power up/down together. Following supply groups have been tested for power sequencing tests:

Table 67. Supply groups tested for power sequencing

| Supply Group No. | Voltage domain | S32V234 power supplies |
|------------------|-------------------------|---|
| 1 | 3.3 V | V_{DD_GPIO0} |
| 2 | 1.8 V/3.3 V | V_{DD_GPIO1} |
| 3 | 1.8 V/3.3 V | V_{DD_GPIO2} |
| 4 | 1.8 V/3.3 V | $V_{DD_HV_IO_VIU0}$ |
| 5 | 1.8 V/3.3 V | $V_{DD_HV_IO_VIU1}$ |
| 6 | 1.8 V/3.3 V | $V_{DD_HV_DIS}$ |
| 7 | 1.8 V/3.3 V | $V_{DD_HV_IO_FLA}$ |
| 8 | 1.5 V/1.8 V/2.5 V/3.3 V | $V_{DD_HV_IO_ETH}$ |
| 9 | 1.8 V | $V_{DD_HV_PLL}$, $V_{DD_HV_LFASTPLL}$, $V_{DD_HV_FXOSC}$, $V_{DD_HV_PMC}$, $V_{DD_HV_EFUSE}$, $V_{DD_HV_DDR}$, P_{CIE_VPH} , $V_{DD_HV_CSI}$, V_{DDIO_LFAST} |
| 10 | 1.0 V | $V_{DD_LV_CORE_SOC}$, $V_{DD_LV_CORE_ARM}$, $V_{DD_LV_GPU}$, $V_{DD_LV_PLL}$, P_{CIE_VP} , $V_{DD_LV_CSI}$ |
| 11 | 1.8 V | $V_{DD_HV_ADV}$, V_{REFH_ADC} |
| 12 | 1.2 V/1.35 V/1.5 V | $V_{DD_DDR_IO}$ |

12 Revision history

Table 68. Revision history

| Revision | Date | Description of changes |
|----------|---------|------------------------|
| 1 | 03/2015 | Initial release. |

Table continues on the next page...

Table 68. Revision history (continued)

| Revision | Date | Description of changes |
|----------|---------|--|
| 2 | 06/2015 | <p>Overall:</p> <ul style="list-style-type: none"> Editorial changes. <p>Added topic PCB routing guidelines.</p> <p>Added topic RESET pin glitch filter specifications.</p> <p>In Table 15, added the sentence "For internal ADC channels, the minimum sampling time required is 3 microsecond" in the foot note on "Sample time".</p> <p>In Power Management Controller (PMC) electrical specifications, changed the introductory paragraph. Added Low Voltage Detector for IRC (VDD_HV_OSC).</p> <p>In Table 3, modified minimum value of 3.3 V input/output supply voltage.</p> <p>In Reset sequence description, updated both "External reset sequence long, BIST enabled" and "Destructive reset sequence, BIST enabled" images.</p> <p>In Table 17, updated the condition of Oscillator start-up time from $f_{OSC} = 24,40 \text{ MHz}$ to $f_{FXOSCHS} = 24,40 \text{ MHz}$.</p> <p>In Power sequencing requirements, changed VREFL_ADC to VREFH_ADC, VDD_HV_CSI1/2 to VDD_HV_CSI, and VDD_LV_CSI1/2 to VDD_LV_CSI.</p> <p>In Table 10, added footnote in ovdd.</p> <p>In Table 5, changed VS4 to S32V234 and VS2 to S32V232.</p> <p>Made extensive changes in QuadSPI AC specifications.</p> <p>In Table 3, added Supply ramp rate specifications.</p> <p>In Table 5, changed maximum value of vdd_hv_pll from 30 mA to 35 mA and maximum value of vdd_lv_pll from 55 mA to 80 mA.</p> <p>In DDR3 and DDR3L timing parameters, added a note.</p> <p>In Table 29, updated the table title to include DDR3L. Also updated minimum value of DDR4, DDR5, DDR6, and DDR7 and changed units of DDR1 and DDR2.</p> <p>In Table 30, updated the table title to include DDR3L. Also updated minimum value of DDR26.</p> <p>In Table 31, updated the table title to include DDR3L. Updated minimum values of DDR17 and DDR18, and units of DDR21 and DDR22.</p> <p>In Table 32, updated LP1 and LP2 symbols and units.</p> <p>In Figure 15, changed figure title from "LPDDR3 write cycle" to "LPDDR2 write cycle".</p> <p>In Table 34, updated minimum value of LP18, and minimum and maximum value of LP21. Also updated units of LP21, LP22, and LP23.</p> <p>Updated topic titles DDR SDRAM Specific Parameters (DDR3, DDR3L, and LPDDR2), DDR3 and DDR3L timing parameters, DDR3 and DDR3L read cycle, and DDR3 and DDR3L write cycle.</p> <p>Updated figure titles Figure 10, Figure 11, and Figure 12.</p> <p>In Reset sequence description, added value of external pull up resistor as 10-15 kilohm.</p> <p>In Table 18, modified the parameter "IRCOSC frequency variation afterprocess trimming" to "IRCOSC frequency variation with respect to supply and temperature after process trimming".</p> <p>Updated Table 16.</p> <p>In Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC), added the sentence "uSDHC_VEND_SPEC[CMD_OE_PRE_EN] field should be programmed to 1 for proper functioning of uSDHC external interface".</p> <p>In Table 59, updated maximum value of TCK Rise and Fall Times.</p> |

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Table 68. Revision history (continued)

| Revision | Date | Description of changes |
|----------|---------|--|
| | | <p>In Table 58, updated minimum value of TCK Cycle Time and the footnote. Also, added CJTAG TCK Cycle Time and updated maximum value of TCK Rise and Fall Times.</p> <p>Added DDR3L mode and DDR3L mode DC electrical specifications.</p> <p>Removed LPDDR2 I/O AC specifications.</p> <p>Deleted the word "Dual" from "Dual QuadSPI supporting Execute-In-Place (XIP)" in "Features" section as there is only one QuadSPI.</p> <p>Changed all instances of XOSC to FXOSC throughout the document.</p> <p>Changed all instances of MIPI-CSI2, MIPI, and CSI2 to MIPICSI2 throughout the document.</p> |
| 2.1 | 06/2015 | <p>Overall:</p> <ul style="list-style-type: none"> • Editorial changes. |
| 3 | 04/2017 | <ul style="list-style-type: none"> • Editorial changes. • Updated Figure 1. • Modified Figure 4. • Modified Figure 6. • Modified Figure 7. • Updated Figure 29. • Updated Figure 38. • Updated Figure 43. • Updated Figure 48. • Removed Figure "DSPI modified transfer format timing – slave, CPHA = 0" and Figure "DSPI modified transfer format timing — slave, CPHA = 1". • In Table 1, updated ARM Cortex-A53 Core feature for S32V232 from "Up to 600 MHz Quad ARM Cortex-A53" to "Up to 800 MHz Dual ARM Cortex-A53 (single cluster)". • In Table 3 : <ul style="list-style-type: none"> • added the footnote "All the grounds viz. VSS, VSS_XOSC, VSS_PMC and VSS_HV_ADV are tied together at the package level" in Common ground voltage. • minimum operating voltage of $V_{DD_HV_IO_ETH}$ has been changed from 1.71 V to 1.5 V, and maximum value of DDR I/O supply voltage LPDDR2 changed from 1.26 V to 1.30 V. • parameter "Supply ramp rate" has been changed to "Supply ramp rate for all supplies on the device" • added LFAST IO bank supply (V_{DDIO_LFAST}) in the list of symbols for "1.8 V supply voltage (for analog circuits, PLLs)" • In Table 4 : <ul style="list-style-type: none"> • added Band Gap Reference value of PMC. • maximum value of trimmed VTH threshold of VDD_LV_CORE_SOC (low voltage monitoring) has been changed from 939 to 946 mV, and maximum values of trimmed VTL and VTH threshold of VDD_LV_CORE_SOC (high voltage monitoring) have been changed from 1081 to 1093, and 1096 to 1093 mV, respectively. • In Table 5 : <ul style="list-style-type: none"> • modified table footnotes to clarify that power numbers are estimated for 1.01 V and 125 °C. • VDD_HV_LFASTPLL Simulation values (Maximum) and Maximum Values of Use cases "PLL operating with 320 MHz (LFAST used)" and "PLL not operational (LFAST not used)" have been modified. • use case "eFuse reading happening" of VDD_HV_EFUSE and its specifications are removed. • max simulation values of MIPICSI2 interface operating as per MIPICSI not used (not powered?) in VDD_HV_CSI and VDD_LV_CSI have been changed from .1 mA to 1.6 mA and 11 mA to 15 mA. • for PCIE_VP and PCIE_VPH, Powered down (leakage only) use case has been changed to Reset/idle. Max simulation values for PCIE_VP and PCIE_VPH (Reset/idle) |

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Table 68. Revision history

| Revision | Date | Description of changes |
|----------|------|--|
| | | <p>use cases are removed, and PCIE_VPH (5 GHz operation) use case has been changed from 30 to 32 mA. Max values of both PCIE_VP and PCIE_VPH (for both cases) have been included.</p> <ul style="list-style-type: none"> • modified the table heading. Removed Front Camera (w power binning) from VDD_LV_CORE and updated max values for “Adder 4x A53 CPU with Dhrystone MIPS running on each CPU @1 GHz” from 1.0 A to 1.4 A. • removed "Simulation values" column. • PCIE_VPH limits changed for “5 GHz operation (PCIe 2.0)” from 40 mA to 50 mA and “Reset/Idle” from 11 mA to 20 mA. • minimum and maximum values of PMC Band Gap Reference value have been changed from 1185 to 1176 mV, and 1215 to 1224 mV respectively. • In Table 10 : <ul style="list-style-type: none"> • added the note “After bootup, application software should switch to manual voltage detect mode using VSEL_x settings of SRC_GPR14 register to ensure optimum performance of the GPIO pads. Please refer to SRC chapter in the Reference Manual for the register details.” • changed the maximum value of Input current (no pull-up/down) from 1 to 8 μA. • removed “Input Hysteresis” • maximum value of parameter “Input current (50 kilohm PU)” has been changed from 100 to 150 μA. • maximum value of parameter “Input current (100 kilohm PU)” has been changed from 50 to 60 μA. • removed parameter “pad keeper resistance” and “maximum external resistor value that is guaranteed to overdrive the pad keeper”. • maximum value of parameter “Input current (50 kilohm PD)” with test condition $V_{in}=0$ has been changed from 1 to 8 μA. Also, when $V_{in} = V_{dd}$, maximum value of Input current (33 kilohm PU), Input current (50 kilohm PU), and Input current (100 kilohm PU) have been changed from 1 to 6 μA. • test conditions “Ioh=-1 mA” changed to “Ioh=-100 μA” and “Ioh= 1 mA” changed to “Ioh=-100 μA”. • In Table 12, Table 13, and Table 14, <ul style="list-style-type: none"> • Added V_{ih} (DC) and V_{il} (DC) specifications . • All tri-state supply current items are removed and updated test conditions of “High-level output voltage” and “Low-level output voltage”. • Maximum value of parameter “ Input current (no pullup/pulldown)” has been changed from 3 to 5 μA, 3 to 5 μA, and 2.5 to 5 μA, respectively. • In Table 12, removed parameter “Rod_keep”. Updated minimum, typical, and maximum value of parameter Rkeep. • In Table 13, removed parameter “Rod_keep”. • In Table 14, removed parameter “Rod_keep” and deleted footnote “Note that the Jedec LPDDR2 specification (JESD209-2B) supersedes any specification in this document”. • In Table 15 <ul style="list-style-type: none"> • updated ADC Input Clock frequency • added ADC Conversion clock frequency • removed conditions of Sample time and Conversion time • removed all information about parameter “Max positive/negative injection” and modified “Total unadjusted error” in “TUE”. • In Table 17, modified the minimum and maximum values of V_{IH} and V_{IL}. • In Table 19 : <ul style="list-style-type: none"> • Changed maximum value of SSCG modulation depth from -6% to -5.4%, and added condition $STEP_SIZE \times STEP_NO < 18432$. • Removed “PLL VCO frequency” and “PLL output clock PHI0”, and deleted footnote “All PLLs have same specifications. PLL programming should take maximum clock frequencies as per Reference Manual recommendation”. • Added Table 19. |

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Table 68. Revision history

| Revision | Date | Description of changes |
|----------|------|---|
| | | <ul style="list-style-type: none"> • In Table 21 : <ul style="list-style-type: none"> • unit for Total Jitter has been changed from ps to ns. • removed max Deterministic and max Random jitter specifications; added footnote in max Total Jitter. • In Table 22 : <ul style="list-style-type: none"> • Made modification in DDR mode. • Updated values of QuadSPI_SOCCR[FDCC_FB] and QuadSPI_SOCCR[FDCC_FA] for SDR and DDR mode (internal DQS Mode) and added footnote "Device qualification is not complete." • Deleted Table "QuadSPI input timing (DDR mode) specifications with learning" • In Table 24 changed Minimum value of Chip select output setup time and Chip select output hold time. • In Table 25 <ul style="list-style-type: none"> • changed maximum value of SCK Clock Frequency and updated configuration. Also, changed table caption • changed the minimum value of "Setup time for incoming data". • In Table 26 : <ul style="list-style-type: none"> • deleted "Chip select output setup time" and "Chip select output hold time". • changed the maximum value of "Output Data Valid" and minimum value of "Output Data Hold". • In Table 27, updated minimum value of parameters "Setup time for incoming data" and "Hold time for incoming data". • In Table 28, updated maximum value of "Ck to Ck2 skew max" and minimum value of "Ck to Ck2 skew min". • In Table 29 changed symbol and minimum value of DDR4, DDR5, DDR6, and DDR7. • In Table 30 modified minimum value of DDR26 from 540 to 563 ps. • In Table 31 changed the symbol and minimum value of DDR17 and DDR18. • In Table 32 changed the symbol and minimum value of parameters CKE setup time, CKE hold time, CA setup time, and CA hold time. • In Table 33 changed the minimum value of LP26. • In Table 34 changed the symbol and minimum value of LP17 and LP18. • In Table 35 : <ul style="list-style-type: none"> • Updated footnotes to include changes in PCSSCK, CSSCK, PASC, ASC values. • Updated footnotes in minimum timing of parameter DSPI cycle time, PCS to SCK delay, and After SCK delay. • In Table 36 changed the heading of table from "SD/eMMC4.3 interface timing specification" to "SDR mode timing specification". • In Table 37 changed the heading of table from "SD3.0/eMMC4.5 interface timing specification" to "DDR mode timing specification" and updated parameter "Clock Frequency (eMMC4.5 DDR)" to "Clock Frequency (eMMC4.4 DDR)". • In Table 38 : <ul style="list-style-type: none"> • updated min, typ, and max values of V_{OS_DRF} and $I_{\Delta VOD_DRF}$ • deleted R_{OUT_DRF} and V_{HYS_DRF} • modified R_{IN_DRF} • added LFAST Clock characteristics • parameter Rise/Fall time (10% - 90% of swing) is changed to Rise/Fall time (20% - 80% of swing) and minimum and maximum values of the parameter have been changed from 0.26 to 0.1 ns and 1.5 to 0.73 ns. • added footnote "Rise/fall time is defined for 20 to 80% signal voltage levels, at 2pF Cload and 100 Ohm termination resistor load". • Updated minimum and maximum value of "Common mode voltage" (Transmitter) from 1.125 to 1.1 V and 1.375 to 1.475 V. • Updated maximum value of "Common mode voltage" (Receiver) from 1.6 to 1.5 V. |

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Table 68. Revision history

| Revision | Date | Description of changes |
|----------|------|--|
| | | <ul style="list-style-type: none"> • Updated the footnote in minimum and maximum values of “Common mode voltage” (Receiver). • Changed minimum value of “Differential input voltage” (Receiver) from 100 to 150 mV. • In Table 43 changed minimum and maximum value of RX_CLK duty cycle. • In Table 44 : <ul style="list-style-type: none"> • changed minimum and maximum value of TX_CLK duty cycle and minimum value of Out delay from TX_CLK. • included "TX_CLK to Output Valid" and "TX_CLK to Output Invalid". • In Table 45 removed the foot note from "Characteristic". • In Table 49 : <ul style="list-style-type: none"> • Changed minimum value of “Data hold time0” and “Data setup time” from 0 to 25 ns, and 0 to 250 (standard mode); 100 (fast mode) respectively • Added note "ipg_clk frequency should be greater than 5 MHz for standard mode and 20 MHz for fast mode" to minimum value of “Data setup time” • Updated the column "Number" • In Table 50, minimum value of “Stop condition setup time” has been changed from 10 to 11 IPS bus cycle. • In Table 51, changed Display pixel clock period from 6.4 to 6.66 ns. • In Table 52, changed pixel clock period from 6.36 to 6.66 ns. • In Table 53, changed description "VIU data setup time" to "VIU Data/Hsync/Vsync setup time" and "VIU data hold time" to "VIU Data/Hsync/Vsync hold time". • In Table 54, removed "Contention Line Receiver DC Specifications". • In Table 57, Data to Clock Setup Time and Clock to Data Hold Time are updated to include condition where the PHY is used to a maximum data rate of 1.0Gbps and data rates greater than 1.0Gbps. • In Table 60, updated Clock frequency. • In Table 65 : <ul style="list-style-type: none"> • changed minimum and maximum values of “Destructive Reset Sequence, BIST disabled” from 5 ms to 50 µs and 10 ms to 90 µs • changed minimum and maximum values of “Functional Reset Sequence Long, Unsecure Boot, BIST disabled” from 5 ms to 50 µs and 10 ms to 90 µs • changed minimum and maximum values of ”Functional Reset Sequence Short, Unsecure Boot, BIST disabled” from 5 ms to 2 µs and 6 ms to 7 µs. • Added Table 67 and a paragraph preceding it “Each supply group mentioned in the table below can be independently powered up/down from the other supply groups. Supply domains belonging to the same supply group are supposed to be ganged together on board level (with appropriate noise isolation) to allow this group to power up/down together”. • All IRC and IRCOSC in the document changed to FIRC. • In Features, modified JPEG and H.264 information. • Removed hysteresis information from Features, Table 1, and from Table 10. • Modified content in Family comparison. • Added topic Operation above maximum operating conditions. • Updated Ordering information • In Power consumption, modified the statement “These specifications are design targets and are subject to change per device characterization” to “These specifications are subject to change per device characterization.” • In PCB routing guidelines changed the subheading from "DDR3 PCB design" to "DDR3/DDR3L PCB design". • Added topic GPIO speed at various voltage levels. • In DDR pads, deleted table "DDR operating conditions". • In ADC electrical specifications, Updated the note to “While measuring scaled supply voltages on ADC Channels, Maximum (+5/-10%) variation can be expected .” • In Main oscillator electrical characteristics, added crystal information. • In ADC electrical specifications added the note “While measuring scaled supply voltages on ADC Channels, Maximum 10% variation can be expected”. |

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Table 68. Revision history (continued)

| Revision | Date | Description of changes |
|----------|---------|--|
| | | <ul style="list-style-type: none"> In Thermal Monitoring Unit (TMU), changed all occurrences of "Temperature Sensor" to "Thermal Monitoring Unit". In 48 MHz FIRC electrical characteristics, min and max value of "IRCOSC frequency variation with respect to supply and temperature after process trimming" has been changed from -5 to -10 and +5 to +10 %. In QuadSPI AC specifications deleted sentence "DDR configurations are applicable when used without learning enabled." Added a note in DSPI timing. In Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) changed the introductory paragraph. Renamed topic "SD/eMMC4.3 (Single Data Rate) AC Timing" to "SDR Mode Timing Specifications". In this topic SDR mode timing specifications deleted the introductory paragraph and deleted the existing figure. Two new figures Figure 23 and Figure 24 are added. Modified Table 36. Renamed topic "SD/eMMC4.4/5.0 (Dual Data Rate) eSDHCv3 AC Timing" to "DDR Mode Timing Specifications". In this topic DDR mode timing specifications, deleted the introductory paragraph and replaced the existing figure with four new figures (Figure 25, Figure 26, Figure 27, Figure 28). In DSPI timing changed the note from "DSPI on this chip neither supports interaction with a Slave in MTFE mode nor acts as one" to "DSPI Timing specs on this chip are valid with Slave in Classic Mode only." In Ethernet Switching Specifications, " statement "For RGMII, output load is 15 pF and pad settings are DSE[2:0] = 111 and FSEL[1:0] = 11" is changed to "For RGMII, output load is 5 pF and pad settings are DSE[2:0] = 111 and FSEL[1:0] = 11." Added topic MII/RMII Serial Management channel timing (MDC/MDIO). In Video input unit (VIU) timing specifications heading "Video input unit (VIU) electrical specifications" changed to "Video input unit (VIU) timing specifications". Added topic Boot performance matrix. In Power sequencing requirements : <ul style="list-style-type: none"> added note "VDD_HV_ADV must be powered for using LFAST interface". Changed "VREFH_ADC should never be more than 100 mV above VDD_HV_ADV" to "VREFH_ADC should never differ from VDD_HV_ADV by more than 100 mV at any time including during power-up or power-down". Changed the sentence from "DDR0_VREF0 and DDR1_VREF0 supplies are expected to be 0.5 of VDD_HV_DDR0 and VDD_HV_DDR1 I/O supplies and are to track VDD_HV_DDR0 and VDD_HV_DDR1 supply variations as measured at the receiver" to "DDR0_VREF0 and DDR1_VREF0 supplies are expected to be 0.5 of VDD_DDR0_IO and VDD_DDR1_IO supplies and are to track VDD_HV_DDR0 and VDD_HV_DDR1 supply variations as measured at the receiver". Updated the statement "VDD_HV_CSI and VDD_LV_CSI should be powered up together on board to prevent any electrical crossover currents" to "VDD_HV_CSI and VDD_LV_CSI supplies should be powered up within 50 ms of each other". |
| 3.1 | 07/2017 | <ul style="list-style-type: none"> The only changes between S32V234 Rev 3.1 and Rev 3 is the removal of "Confidential Proprietary" from the footer. |
| 4 | 11/2017 | <ul style="list-style-type: none"> In Ordering information, added a table mentioning the production part numbers with respective feature configurations. In Table 19, updated SSCG modulation depth values. In Features, updated the statement for "APEX2-CL Image cognition processor" to remove the mention of OpenCL 1.2 support. In Features, updated the first statement under "Memory interfaces" with the correct LPDDR2/DDR3/DDR3L operating specs. Updated LPDDR2 and DDR3 operating clock rate and data rate in Figure 1. In Feature Set, updated the "Memory Interfaces" entry for the correct operating data rate and clock rate of LPDDR2 and DDR3. |

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Table 68. Revision history (continued)

| Revision | Date | Description of changes |
|----------|---------|---|
| | | <ul style="list-style-type: none"> In PCB routing guidelines, added a note under the "CLK/Address/Commands" section. And updated the third point under the section for clarification. In Table 3, row 2 and 3 has been split into sub-sections for different I/O voltages. In Table 5, updated max value for VDD_HV_LFASTPLL when "PLL operating with 320 MHz (LFAST used)". Value is changed from 24 mA to 26 mA. In Table 16, updated T_{ADC} at T_J = 40 °C to 125 °C, from +/- 5 °C to +/- 6 °C. In Table 5, updated descriptions for VDD_HV_CSI and VDD_LV_CSI. The string "not powered?" is changed to "IP Powered and Disabled". In Main oscillator electrical characteristics, updated the section to remove references of 24 MHz FXOSC support. In Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC), updated the topic title and added a paragraph describing voltage restriction with eMMC booting. In Table 5, removed the footnotes from the "Max Values" column, and added one to the VDD_LV_CORE entry. In Table 19, updated the frequency values for "PLL input clock". In Table 20, updated the "Input Frequency" values. Updated the specs in following tables: <ul style="list-style-type: none"> Table 29 Table 31 Table 32 Table 34 Removed the table "PLL maximum frequencies" from the section PLL electrical specifications. In DFS electrical specifications, updated mfn division factor from [0:255] to [1:255], and updated the footnote from the Table 20. |
| 5 | 03/2018 | <ul style="list-style-type: none"> This device is qualified now, so removed the footnote from Table 22 that said "Device qualification is not complete." Corrected "Operating Max Supply Voltage" for "3.3 V DGO Voltage Domain" in Table 2 to 3.6 V. Corrected Block diagram to add DRAM-ECC to MMDC_1 block, similar to it was with MMDC_0. Updated the specs for VDD_LV_CORE in Table 5. Updated max values for T_{DRB} and T_{ERLB} in Table 65. |
| 6 | 08/2018 | <ul style="list-style-type: none"> GPIO speed at various voltage levels - Added a note at the end of the section. Power sequencing requirements - Added one new point to the bullet list mentioning the maximum rise time for POR signal. Boot Configuration Pins Specification - Added two notes in this section. Table 56 - Updated "Maximum serial data rate" spec from "80 to 1.5 Gbps" to "80 to 1500 Mbps". Following changes are made throughout the document for better clarification: <ul style="list-style-type: none"> DSE[2:0] changed to SIUL2_MSCRn[DSE]. ipp_dse<1:0> changed to SIUL2_MSCRn[DSE]. FSEL[1:0] changed to SIUL2_MSCRn[SRE]. ipp_fsel changed to SIUL2_MSCRn[SRE]. Deleted the test condition about ipp_do. Added a note to the following sections to clarify that to match with the measurements given in the section you must ensure the configuration mentioned. That may not be the default configuration of the chip after reset. <ul style="list-style-type: none"> QuadSPI AC specifications DSPI timing Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) Ethernet Switching Specifications MII/RMII Serial Management channel timing (MDC/MDIO) Interface to TFT panels |

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Table 68. Revision history (continued)

| Revision | Date | Description of changes |
|----------|---------|--|
| | | <ul style="list-style-type: none"> • JTAG interface timing • Debug trace timing specifications • Electrostatic discharge (ESD) specifications - Removed the VESD(CDM) specs for corner pins. |
| 7 | 08/2018 | <ul style="list-style-type: none"> • GPIO speed at various voltage levels - Added the text "The maximum rise time for all GPIO pins is 1 ms" to the existing note. • Power sequencing requirements - Updated the last bullet to "The maximum rise time for the POR and RESET.....this pin can increase the problem." |
| 8 | 12/2018 | <ul style="list-style-type: none"> • Changed all instances of XOSC to FXOSC throughout the document. • In Table 1 - For S32V232 changed "Up to 800 MHz Dual ARM Cortex-A53 (single cluster)" to "Up to 1000 MHz Dual ARM Cortex-A53 (single cluster)" and in communications row removed all the text and added text "Same as S32V234" for S32V232. • In Ordering information - Changed text from "The orderable part numbers of this chip are in the table below" to "An example of orderable part numbers of this chip are in the table below". • In GPIO speed at various voltage levels - Added the Drive Strength "001" and "010" in the "GPIO rise/fall times (1.8 V range)", "GPIO rise/fall times (2.5 V range)" and "GPIO rise/fall times (3.3 V range)" tables. • In Features - Removed the text "ARM TrustZone (TZ) architecture support" and added text "Secure vs non-secure applications separation supported via ARM v8 exception level support in the ARM Cortex A53 clusters and its extension via XRDC on SoC level". • In Table 5 updated the following: <ul style="list-style-type: none"> • Replaced descriptive text with orderable part number. • Removed @ 125 C from each row. • Split the row "DD_LV_CORE" into "DD_LV_CORE (static)" and "DD_LV_CORE (dynamic)" into separate rows. • Added "T_j" as the temperature in the footnote. • Added further static power entries. Added values for 125 T_j and 105 T_j for VDD_LV_CORE (Static). • Added parameters "VDD_HV_ADV" and "VDD_REFH_ADC". • In DDR3 and DDR3L timing parameters added Note "DDR3 and DDR3L timing parameters are compliant with JESD79-3F and JESD79-3-1A.01 specifications respectively". • In LPDDR2 timing parameter added Note "LPDDR2 timing parameters are compliant with JESD209-2B specification". |
| 9 | 01/2020 | <ul style="list-style-type: none"> • In Ordering information : <ul style="list-style-type: none"> • Added Figure 1. • Added a note "For the latest information on orderable parts please check https://www.nxp.com/s32v234 Buy/Parametrics section". • In Features changed the text from "Secure vs non-secure applications separation supported via ARM v8 exception level support in the ARM Cortex A53 clusters and its extension via XRDC on chip level" to "ARM TrustZone (TZ) architecture support". • In Table 2 removed the "Operating Max Supply Voltage" rows. • Removed the Maximum and Minimum values of V_{tt} and added a footnote in Table 13 and Table 12. • Updated the text from "Supply domains belonging to the same supply group are supposed to be ganged together on board level (with appropriate noise isolation) to allow this group to power up/down together" to "Power supplies in the same group must be powered up/down together. Supply groups belonging to the same supply domain can be ganged together on board level (with appropriate noise isolation) to allow these groups to power up/down together" in Power sequencing requirements. • In Table 38 for I_{ΔV_I_DRF} added the conditions "V_{ICOM_DRF}>1.4 V" and "V_{ICOM_DRF}≤ 1.4 V". |
| 10 | 02/2022 | <ul style="list-style-type: none"> • In Ordering information, added FAB and MASK identifier and Package information. • In Table 1, removed the text from "dual 32-bit array processor" from APEX processor. |

Table 68. Revision history

| Revision | Date | Description of changes |
|----------|------|--|
| | | <ul style="list-style-type: none">• In Reset sequence description, changed "EXT_POR pin (Active Low) is recommended to be de-asserted after external supplies became stable" to "EXT_POR pin (Active Low) is required to be de-asserted after external supplies became stable".• In PCB routing guidelines, changed the wording in DDR3/DDR3L PCB design bullet from "To be referenced with Power, not Ground" to "Recommended to be referenced with Ground-plane or Power-plane".• In Table 3, added Storage temperature range. |

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