THE DATASHEET OF

MMRF1304NR1

Document Number: MMRF1304N
Rev. 0, 12/2013

RoHS

RF Power LDMOS Transistors

High Ruggedness N-Channel Enhancement-Mode Lateral MOSFETs

MMRF1304NR1
MMRF1304GNR1

RF power transistors suitable for both narrowband and broadband CW or pulse applications operating at frequencies from 1.8 to 2000 MHz, such as military radio communications and radar. These devices are fabricated using Freescale's enhanced ruggedness platform and are suitable for use in applications where high VSWRs are encountered.

1.8-2000 MHz, 25 W, 50 V
WIDEBAND
RF POWER LDMOS TRANSISTORS

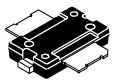
Typical Performance: V_{DD} = 50 Vdc

Frequency (MHz)	Signal Type	P_{out} (W)	G_{ps} (dB)	η_D (%)	IMD (1) (dBc)
1.8 to 30 (2,6)	Two-Tone (10 kHz spacing)	25 PEP	25	51	-30
30-512 (3,6)	Two-Tone (200 kHz spacing)	25 PEP	17.1	30.1	-32
512 (4)	Pulse (100 μsec, 20% Duty Cycle)	25 Peak	25.4	74.5	—
512 (4)	CW	25	25.5	74.7	—
1030 (5)	CW	25	22.5	60	—

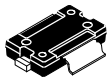
Load Mismatch/Ruggedness

Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage	Result
30 (2)	CW	>65:1 at all Phase Angles	0.23 (3 dB Overdrive)	50	No Device Degradation
512 (3)	CW		1.6 (3 dB Overdrive)		
512 (4)	Pulse (100 μsec, 20% Duty Cycle)		0.14 Peak (3 dB Overdrive)		
512 (4)	CW		0.14 (3 dB Overdrive		
1030 (5)	CW		0.34 (3 dB Overdrive		

1. Distortion products are referenced to one of two tones.
2. Measured in 1.8-30 MHz broadband reference circuit.
3. Measured in 30-512 MHz broadband reference circuit.
4. Measured in 512 MHz narrowband test circuit.
5. Measured in 1030 MHz narrowband test circuit.
6. The values shown are the minimum measured performance numbers across the indicated frequency range.



TO-270-2
PLASTIC
MMRF1304NR1



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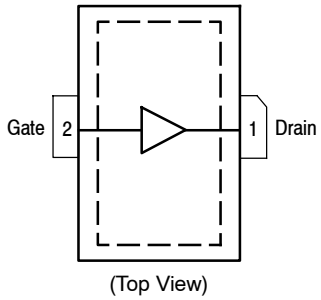
PLASTIC
MMRF1304GNR1



(Top View)

Note: The backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Features

- Wide Operating Frequency Range
- Extreme Ruggedness
- Unmatched, Capable of Very Broadband Operation
- Integrated Stability Enhancements
- Low Thermal Resistance
- Extended ESD Protection Circuit
- In Tape and Reel. R1 Suffix = 500 Units, 24 mm Tape Width, 13-inch Reel.

freescale

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +133	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	-40 to +150	°C
Operating Junction Temperature (1)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case CW: Case Temperature 80°C, 25 W CW, 50 Vdc, I_{DQ} = 10 mA, 512 MHz	$R_{\theta JC}$	1.2	°C/W
Thermal Impedance, Junction to Case Pulse: Case Temperature 77°C, 25 W Peak, 100 μsec Pulse Width, 20% Duty Cycle, 50 Vdc, I_{DQ} = 10 mA, 512 MHz	$Z_{\theta JC}$	0.29	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2, passes 2500 V
Machine Model (per EIA/JESD22-A115)	B, passes 250 V
Charge Device Model (per JESD22-C101)	IV, passes 2000 V

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	400	nAdc
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 50 mA)	$V_{(BR)DSS}$	133	142	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	2	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	7	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 85 μAdc)	$V_{GS(th)}$	1.5	2.0	2.5	Vdc
Gate Quiescent Voltage (V_{DD} = 50 Vdc, I_D = 10 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.0	2.4	3.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 210 mAdc)	$V_{DS(on)}$	—	0.28	—	Vdc
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.26	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	14.2	—	pF
Input Capacitance (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	39.2	—	pF

1. Continuous use at maximum temperature will affect MTTF.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 10 mA, P_{out} = 25 W Peak (5 W Avg.), f = 512 MHz, 100 μsec Pulse Width, 20% Duty Cycle					
Power Gain	G_{ps}	24.0	25.4	27.0	dB
Drain Efficiency	η_D	70.0	74.5	—	%
Input Return Loss	IRL	—	-16	-10	dB

Load Mismatch/Ruggedness (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 10 mA

Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage, V_{DD}	Result
512	Pulse (100 μsec, 20% Duty Cycle)	>65:1 at all Phase Angles	0.14 Peak (3 dB Overdrive)	50	No Device Degradation
	CW		0.14 (3 dB Overdrive)		

1. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.

TYPICAL CHARACTERISTICS

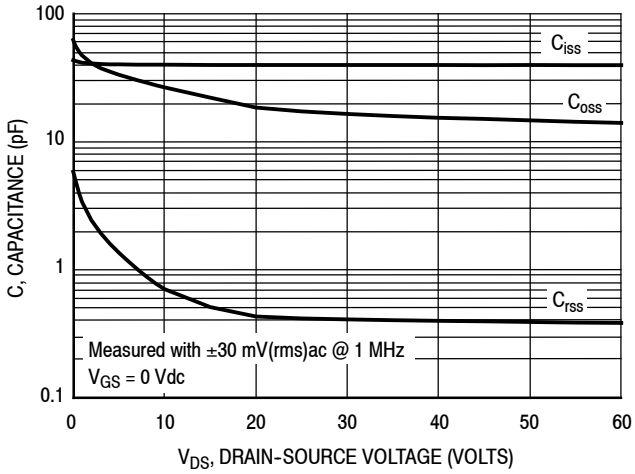


Figure 2. Capacitance versus Drain-Source Voltage

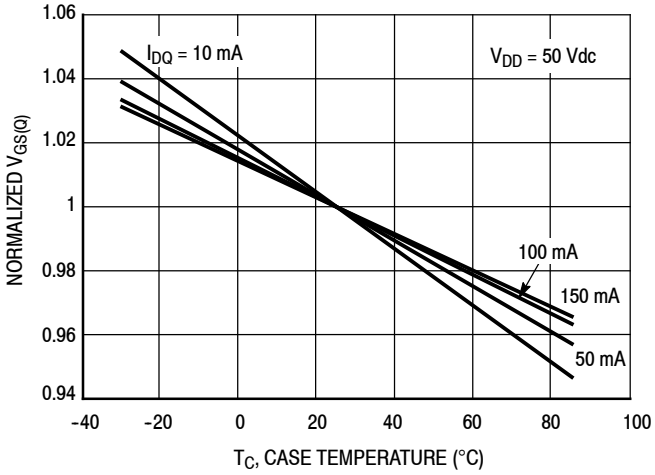
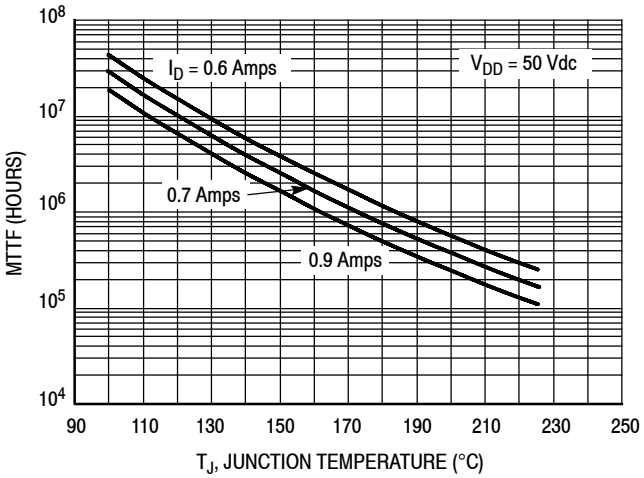


Figure 3. Normalized V_{GS} and Quiescent Current versus Case Temperature

I_{DQ} (mA)	Slope (mV/°C)
10	-2.160
50	-1.790
100	-1.760
150	-1.680

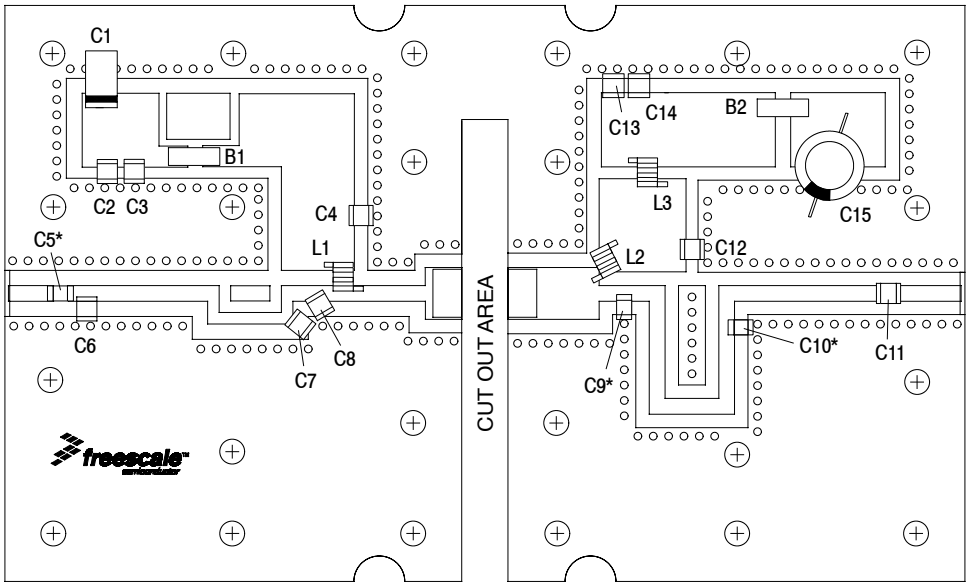


Note: MTTF value represents the total cumulative operating time under indicated test conditions.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 4. MTTF versus Junction Temperature - CW

512 MHz NARROWBAND PRODUCTION TEST FIXTURE



*C5, C9 and C10 are mounted vertically.

Figure 5. MMRF1304NR1 Narrowband Test Circuit Component Layout — 512 MHz

Table 6. MMRF1304NR1 Narrowband Test Circuit Component Designations and Values — 512 MHz

Part	Description	Part Number	Manufacturer
B1, B2	Long Ferrite Beads	2743021447	Fair-Rite
C1	22 μF, 35 V Tantalum Capacitor	T491X226K035AT	Kemet
C2, C13	0.1 μF Chip Capacitors	CDR33BX104AKWY	AVX
C3, C14	0.01 μF Chip Capacitors	C0805C103K5RAC	Kemet
C4, C11, C12	180 pF Chip Capacitors	ATC100B181JT300XT	ATC
C5	18 pF Chip Capacitor	ATC100B180JT500XT	ATC
C6	2.7 pF Chip Capacitor	ATC100B2R7BT500XT	ATC
C7	15 pF Chip Capacitor	ATC100B150JT500XT	ATC
C8	36 pF Chip Capacitor	ATC100B360JT500XT	ATC
C9	4.3 pF Chip Capacitor	ATC100B4R3CT500XT	ATC
C10	13 pF Chip Capacitor	ATC100B130JT500XT	ATC
C15	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
L1	33 nH Inductor	1812SMS-33NJLC	Coilcraft
L2	12.5 nH Inductor	A04TJLC	Coilcraft
L3	82 nH Inductor	1812SMS-82NJLC	Coilcraft
PCB	0.030″, ε_r = 2.55	AD255A	Arlon

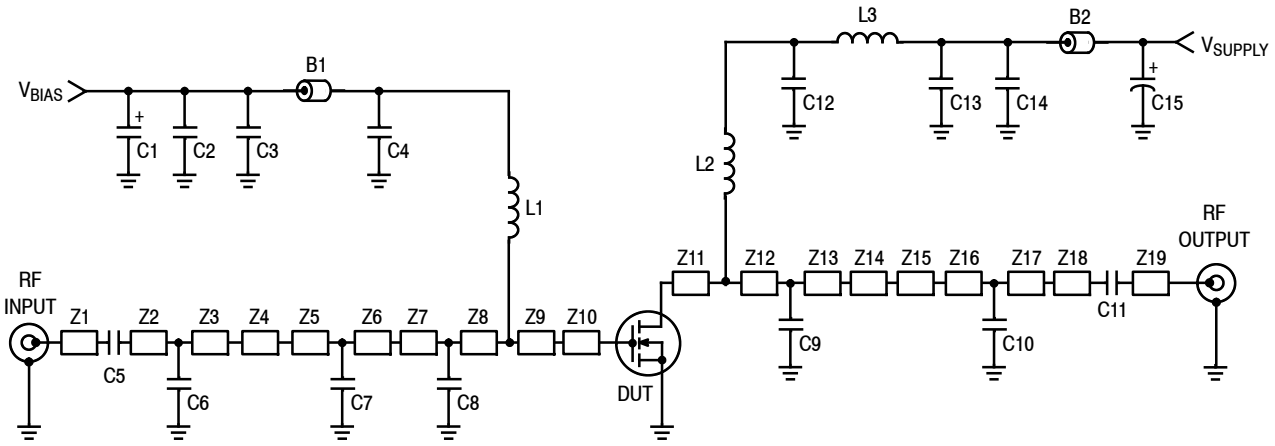


Figure 6. MMRF1304NR1 Narrowband Test Circuit Schematic — 512 MHz

Table 7. MMRF1304NR1 Narrowband Test Circuit Microstrips — 512 MHz

Microstrip	Description
Z1	0.235″ × 0.082″ Microstrip
Z2	0.042″ × 0.082″ Microstrip
Z3	0.682″ × 0.082″ Microstrip
Z4*	0.200″ × 0.060″ Microstrip
Z5	0.324″ × 0.060″ Microstrip
Z6*	0.200″ × 0.060″ Microstrip
Z7	0.067″ × 0.082″ Microstrip
Z8	0.142″ × 0.082″ Microstrip
Z9	0.481″ × 0.082″ Microstrip
Z10	0.190″ × 0.270″ Microstrip

Microstrip	Description
Z11	0.475″ × 0.270″ Microstrip
Z12	0.091″ × 0.082″ Microstrip
Z13	0.170″ × 0.082″ Microstrip
Z14*	0.670″ × 0.082″ Microstrip
Z15	0.280″ × 0.082″ Microstrip
Z16*	0.413″ × 0.082″ Microstrip
Z17*	0.259″ × 0.082″ Microstrip
Z18	0.761″ × 0.082″ Microstrip
Z19	0.341″ × 0.082″ Microstrip

* Line length includes microstrip bends

TYPICAL CHARACTERISTICS — 512 MHz

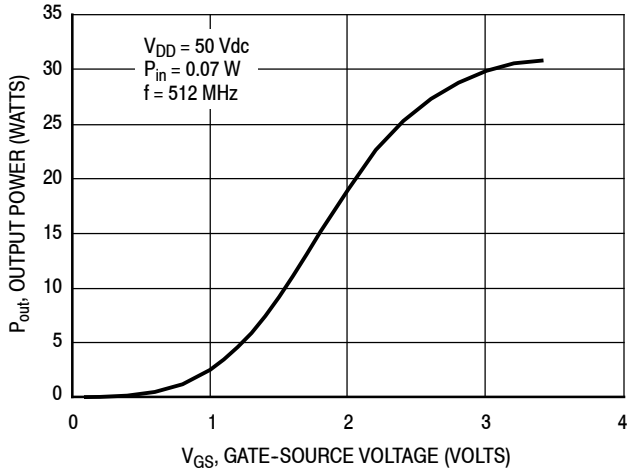
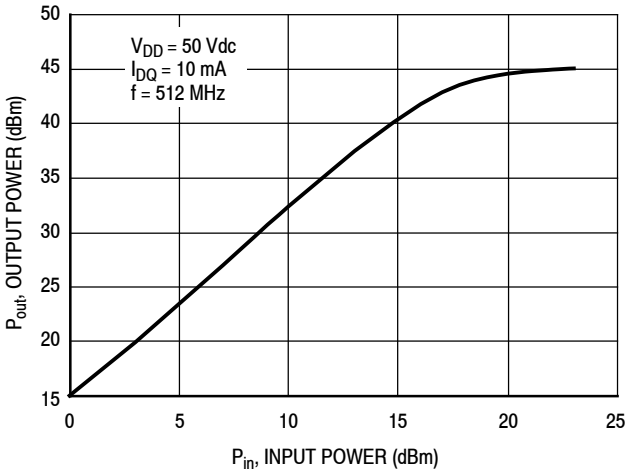


Figure 7. CW Output Power versus Gate-Source Voltage at a Constant Input Power



f (MHz)	P1dB (W)	P3dB (W)
512	27.8	31.4

Figure 8. CW Output Power versus Input Power

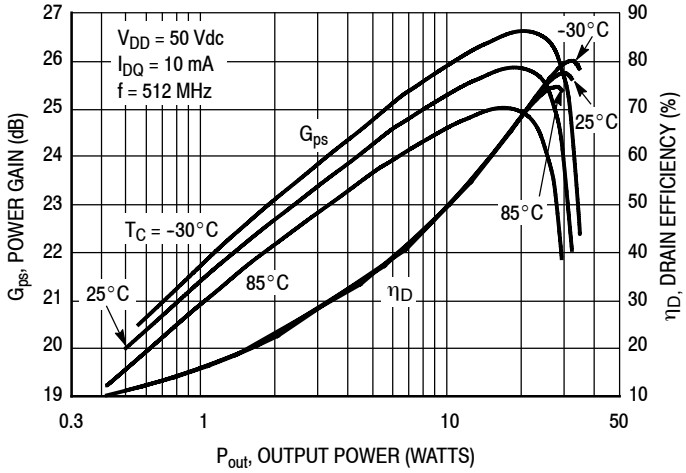


Figure 9. Power Gain and Drain Efficiency versus CW Output Power

512 MHz NARROWBAND PRODUCTION TEST FIXTURE

V_{DD} = 50 Vdc, I_{DQ} = 10 mA, P_{out} = 25 W Peak

f MHz	Z_{source} Ω	Z_{load} Ω
512	1.56 + j11.6	9.5 + j18.3

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

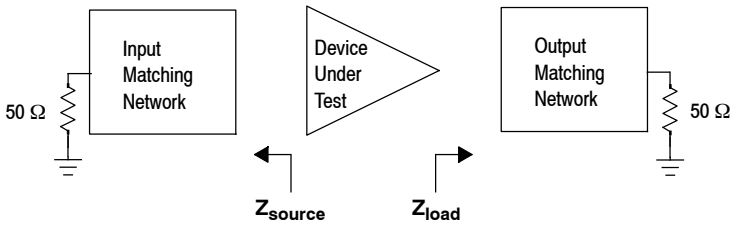
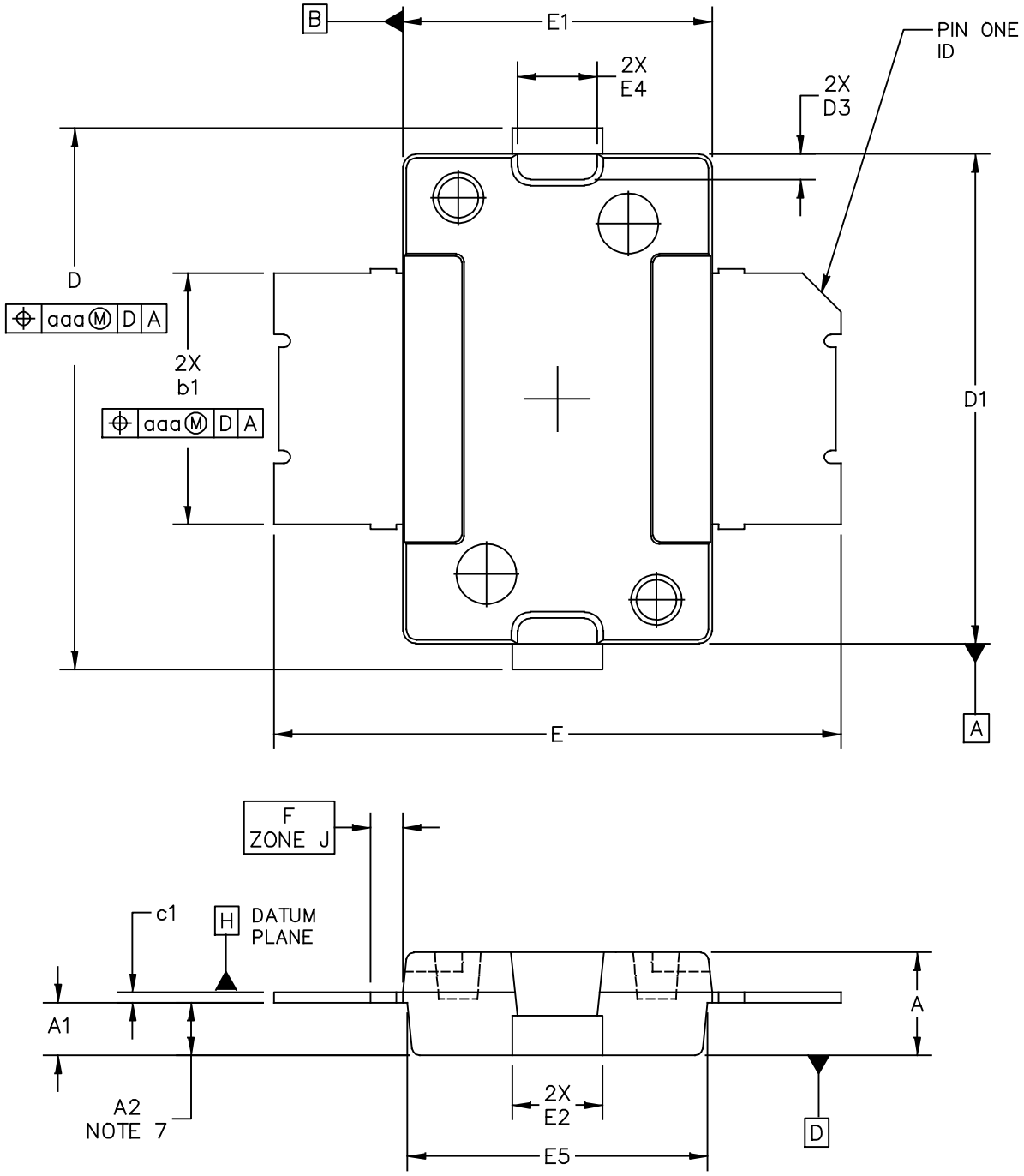


Figure 10. Narrowband Series Equivalent Source and Load Impedance — 512 MHz

PACKAGE DIMENSIONS



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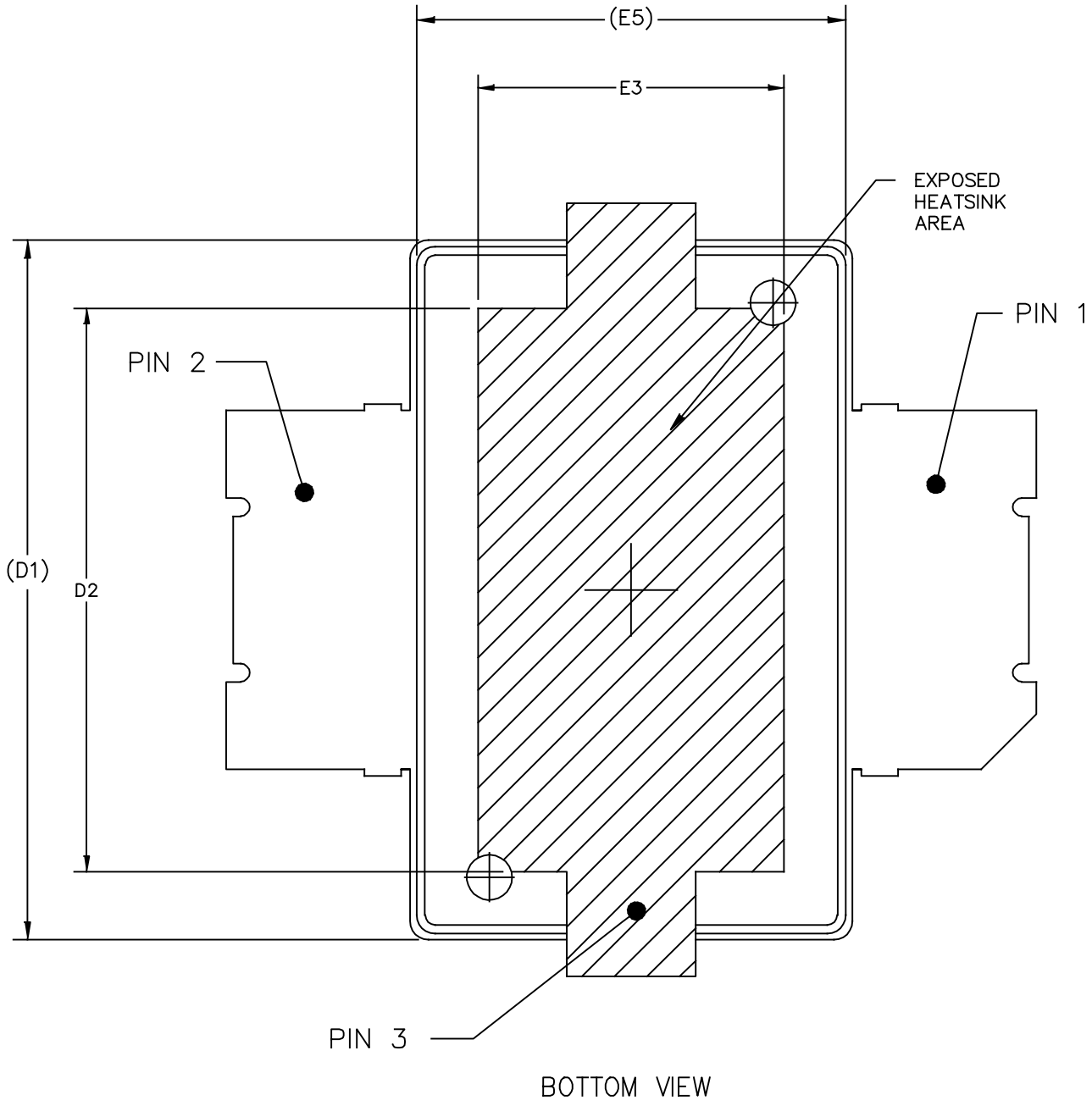
TITLE: TO–270 SURFACE MOUNT	DOCUMENT NO: 98ASH98117A	REV: K
	CASE NUMBER: 1265–09	29 JUN 2007
	STANDARD: JEDEC TO–270 AA	



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	CASE NUMBER: 1265−09	29 JUN 2007
	STANDARD: JEDEC TO−270 AA	

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1 AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION "A2" APPLIES WITHIN ZONE "J" ONLY.

8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. OVERALL LENGTH INCLUDING MOLD PROTRUSION SHOULD NOT EXCEED 0.430 INCH FOR DIMENSION "D" AND 0.080 INCH FOR DIMENSION "E2". DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –D–.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – GATE
PIN 3 – SOURCE

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.193	.199	4.90	5.06
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.416	.424	10.57	10.77	aaa	.004		0.10	
D1	.378	.382	9.60	9.70					
D2	.290	----	7.37	----					
D3	.016	.024	0.41	0.61					
E	.436	.444	11.07	11.28					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	----	3.81	----					
E4	.058	.066	1.47	1.68					
E5	.231	.235	5.87	5.97					

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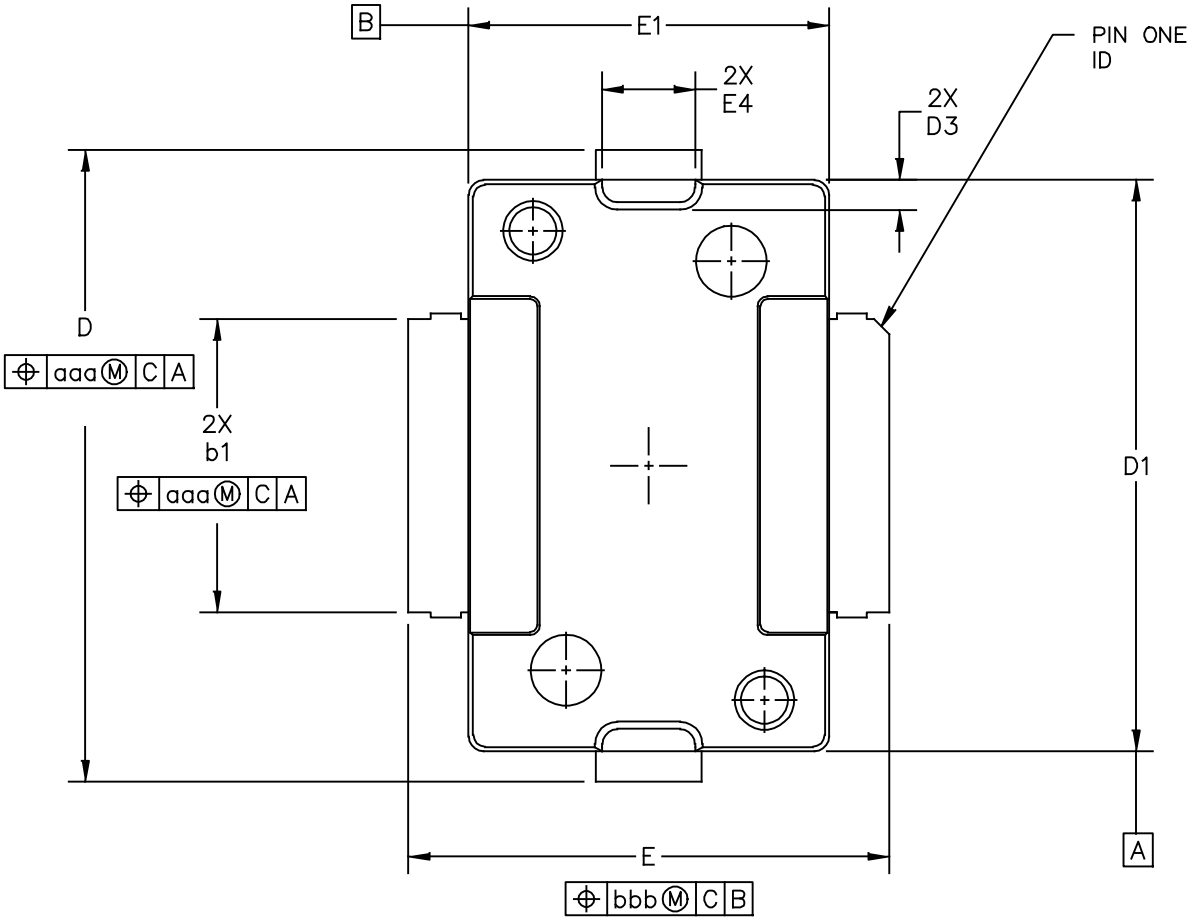
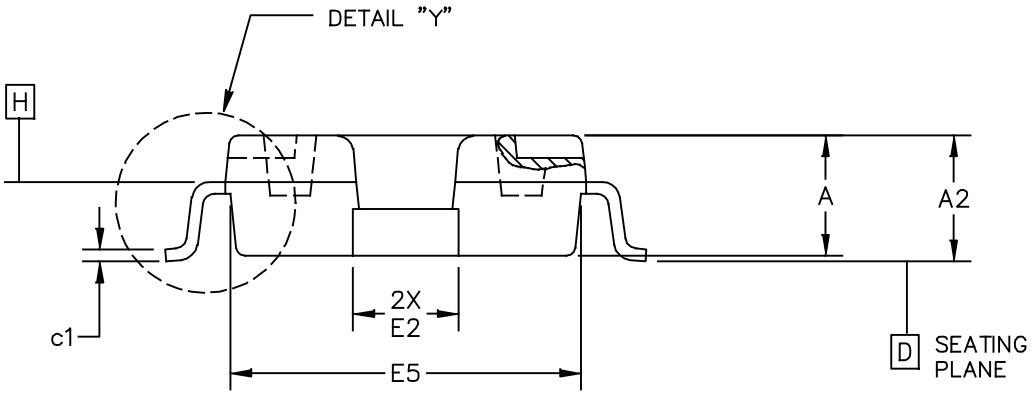
DOCUMENT NO: 98ASH98117A | REV: K

CASE NUMBER: 1265–09 | 29 JUN 2007

STANDARD: JEDEC TO–270 AA





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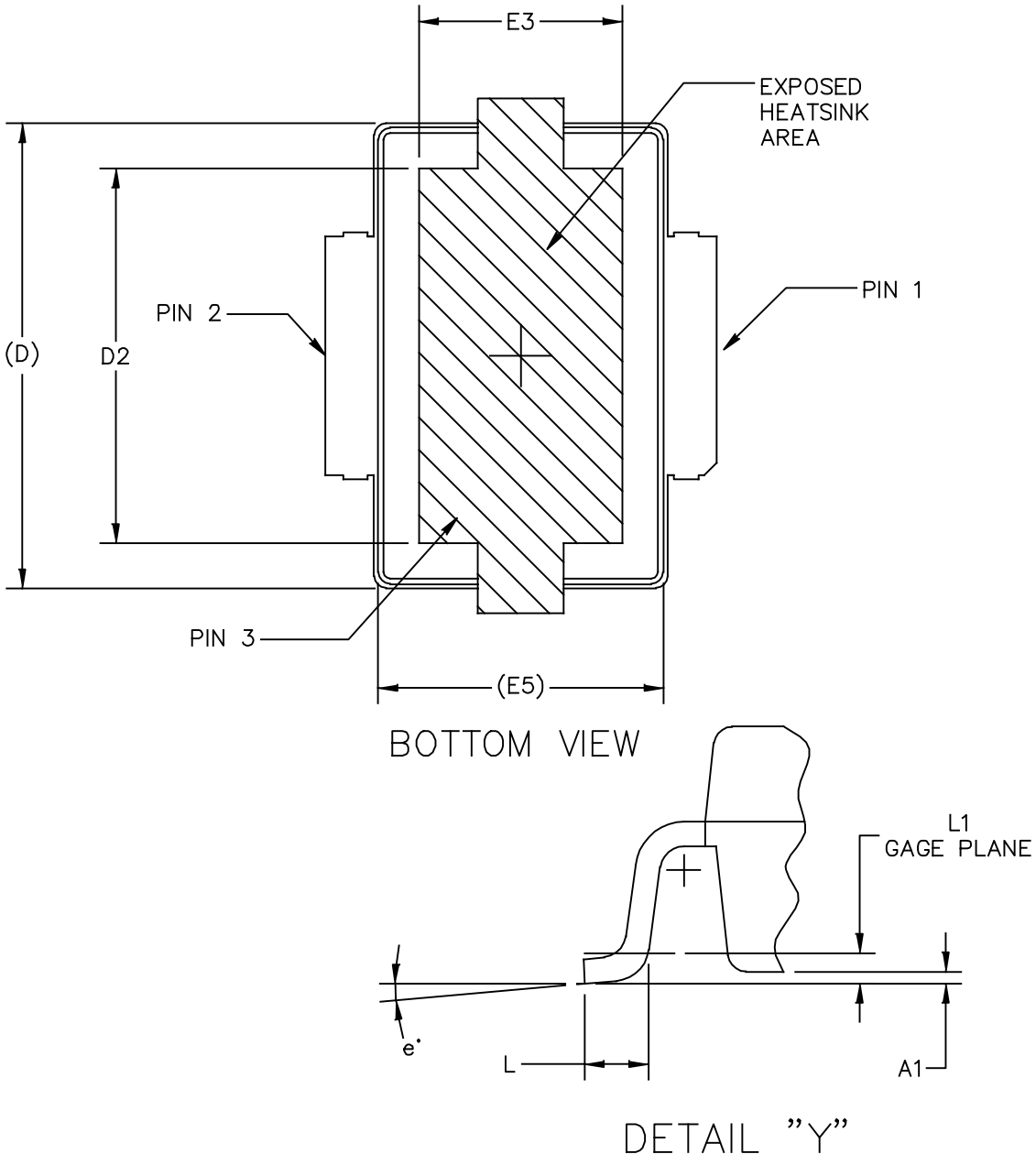
	CASE NUMBER: 1265A–03	02 JUL 2007
	STANDARD: JEDEC TO–270 BA	



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TITLE: TO-270 GULL WING	DOCUMENT NO: 98ASA99301D	REV: C
	CASE NUMBER: 1265A-03	02 JUL 2007
	STANDARD: JEDEC TO-270 BA	

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1 AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .003 PER SIDE. DIMENSIONS "D AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –D–.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – GATE
PIN 3 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.078	.082	1.98	2.08	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.01 BSC		0.25 BSC	
A2	.077	.088	1.96	2.24	b1	.193	.199	4.90	5.06
D	.416	.424	10.57	10.77	c1	.007	.011	0.18	0.28
D1	.378	.382	9.60	9.70	e	2°	8°	2°	8°
D2	.290	–	7.37	–	aaa	.004		0.10	
D3	.016	.024	0.41	0.61					
E	.316	.324	8.03	8.23					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	–	3.81	–					
E4	.058	.066	1.47	1.68					
E5	.231	.235	5.87	5.97					

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TITLE:	DOCUMENT NO: 98ASA99301D	REV: C
TO–270 GULL WING	CASE NUMBER: 1265A–03	02 JUL 2007
	STANDARD: JEDEC TO–270 BA	

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices
- EB38: Measuring the Intermodulation Distortion of Linear Amplifiers

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2013	• Initial Release of Data Sheet

How to Reach Us:

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Document Number: MMRF1304N
Rev. 0, 12/2013

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