THE DATASHEET OF

MB90F342ESPFV-GSE1

www.win-source.net 0086-755-83957316

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MB90350E Series

F^{2}MC-16LX16-bit Microcontrollers

The MB90350E series, loaded 1 channel FULL-CAN* interface and Flash ROM, is general-purpose Cypress 16-bit microcontroller designing for automotive and industrial applications. Its main feature is the on-board CAN interface, which conforms to CAN standard Version2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach.

The power supply (3 V) is supplied to the MCU core from an internal regulator circuit. This creates a major advantage in terms of EMI and power consumption.

The PLL clock multiplication circuit provides an internal 42 ns instruction execution time from an external 4 MHz clock. Also, the clock supervisor function can monitor main clock and sub clock independently.

As the peripheral resources, the unit features a 4-channel Output Compare Unit, 6-channel Input Capture Unit, 2 separate 16-bit free-run timers, 2-channel LIN-UART and 15-channel 8/10-bit A/D converter built-in.

: Controller Area Network (CAN) - License of Robert Bosch GmbH

Features

Clock

- Built-in PLL clock frequency multiplication circuit
- Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 6 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 24 MHz).
- Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed (devices without S-suffix only) .
- Minimum execution time of instruction : 42 ns (when operating with 4-MHz oscillation clock, and 6-time multiplied PLL clock).
- Built-in clock modulation circuit

16 Mbytes CPU memory space

24-bit internal addressing

Instruction system best suited to controller

- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes (23 types)
- Enhanced multiply-divide instructions with sign and RETI instructions

Clock supervisor (MB90x356x and MB90x357x only)

Main clock or sub clock is monitored independently.

Enhanced high-precision computing with 32-bit accumulator

Instruction system compatible with high-level language (C language) and multitask

- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions

Increased processing speed

4-byte instruction queue

Powerful interrupt function

- Powerful 8-level, 34-condition interrupt feature
- Up to 8 channels external interrupts are supported.

Automatic data transfer function independent of CPU

- Extended intelligent I/O service function (EI^{2}OS): up to 16 channels
- DMA: up to 16 channels

Low power consumption (standby) mode

- Sleep mode (a mode that stops CPU operating clock)
- Main timer mode (a timebase timer mode switched from the main clock mode)
- PLL timer mode (a timebase timer mode switched from the PLL clock mode)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU intermittent operation mode

Process

CMOS technology

I/O port

- General-purpose input/output port (CMOS output)
  49 ports (devices without S-suffix : devices that correspond to sub clock)
  51 ports (devices with S-suffix : devices that do not correspond to sub clock)

Sub clock pin (X0A, X1A)

- Yes (using the external oscillation) : devices without S-suffix
- No (using the sub clock mode at internal CR oscillation) : devices with S-suffix

Timer

- Timebase timer, watch timer, watchdog timer : 1 channel

- 8/16-bit PPG timer : 8-bit ∞ 10 channels or 16-bit × 6 channels
- 16-bit reload timer : 2 channels (only Evaluation products has 4 channels)
- 16- bit input/output timer
  - 16-bit free-run timer : 2 channels (FRT0 : ICU0/1, FRT1 : ICU4/5/6/7, OCU4/5/6/7)
  - 16- bit input capture: (ICU) : 6 channels
  - 16-bit output compare : (OCU) : 4 channels

FULL-CAN interface: 1 channel

- Compliant with CAN standard Version2.0 Part A and Part B
- 16 message buffers are built-in
- CAN wake-up function

LIN-UART: 2 channels

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

I^2C interface: 1 channel

Up to 400 kbps transfer rate

DTP/External interrupt: 8 channels, CAN wakeup: 1 channel

Module for activation of extended intelligent I/O service (EI^2OS), DMA, and generation of external interrupt by external input.

Delay interrupt generator module

Generates interrupt request for task switching.

8/10-bit A/D converter: 15 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time : 3 µs (at 24 MHz machine clock, including sampling time)

Address matching detection (Program patch) function

- Address matching detection for 6 address pointers.

Capable of changing input voltage level for port

- Automotive/CMOS-Schmitt (initial level is Automotive in single chip mode)
- TTL level (corresponds to external bus pins only, initial level of these pins is TTL in external bus mode)

Low voltage/CPU operation detection reset (devices with T-suffix)

- Detects low voltage (4.0 V ± 0.3 V) and resets automatically
- Resets automatically when program is runaway and counter is not cleared within interval time
  (approx. 262 ms : external 4 MHz)

Dual operation Flash memory (only devices 128 Kbytes Flash memory)

- Erase/write and read can be executed in the different bank (Upper Bank/Lower Bank) at the same time.

Supported T_A = + 125°C

The maximum operating frequency is 24 MHz* : (at T_A = +125°C) .

Flash security function

- Protects the content of Flash memory
  (MB90F352x, MB90F357x only)

External bus interface

- 4 Mbytes external memory space
  MB90F351E(S), MB90F351TE(S), MB90F352E(S), MB90F352TE(S) : External bus Interface can not be used in internal vector mode. It can be used only in external vector mode.

* : If used exceeding T_A = + 105 °C, be sure to contact Cypress for reliability limitations.

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1. Product Lineup1 (Without Clock supervisor function)

■ Flash memory products

Parameter \ Part Number	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
Type	Flash memory products			
CPU	F^2MC-16LX CPU			
System clock	PLL clock multiplication circuit (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	64 Kbytes Flash memory : MB90F351E(S), MB90F351TE(S) 128 Kbytes Dual operation Flash memory (Erase/write and read can be operated at the same time) : MB90F352E(S), MB90F352TE(S)			
RAM	4 Kbytes			
Emulator-specific power supply*	—			
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No	
Clock supervisor	No			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus			
Operating temperature	−40°C to +125°C			
Package	LQFP-64			
LIN-UART	2 channels			
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 kbps)	1 channel			
A/D converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)			
16-bit reload timer (2 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit Free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit output compare	4 channels			
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

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Parameter \ Part Number	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
16-bit Input capture	6 channels			
	Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge) , signals an interrupt.			
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width×12			
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN interface	1 channel			
	Compliant with CAN standard Version2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.			
External interrupt	8 channels			
	Can be used rising edge, falling edge, starting up by “H”/“L” level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.			
D/A converter	—			
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)			
Flash memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F352E(S) and MB90F352TE(S) only)			
Corresponding evaluation name	MB90V340E-102		MB90V340E-101	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

■ MASK ROM products/Evaluation products

Parameter \ Part Number	MB90351E MB90352E	MB90351TE MB90352TE	MB90351ES MB90352ES	MB90351TES MB90352TES	MB90V340E-101	MB90V340E-102
Type	MASK ROM products				Evaluation products	
CPU	F^2MC-16LX CPU					
System clock	PLL clock multiplication circuit (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64 Kbytes : MB90351E(S), MB90351TE(S) 128 Kbytes : MB90352E(S), MB90352TE(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No		No	Yes
Clock supervisor	No					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40°C to +125°C				—	
Package	LQFP-64				PGA-299	
LIN-UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 kbps)	1 channel				2 channels	
A/D converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit reload timer	2 channels				4 channels	
	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU4/5/6/7.				Free-run Timer 0 corresponds to ICU0/1/2/3, OCU0/1/2/3. Free-run Timer 1 corresponds to ICU4/5/6/7, OCU4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

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Part Number / Parameter	MB90351E MB90352E	MB90351TE MB90352TE	MB90351ES MB90352ES	MB90351TES MB90352TES	MB90V340E-101	MB90V340E-102
16-bit output compare	4 channels				8 channels	
	Signals an interrupt when 16-bit free-run Timer matches output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit input capture	6 channels				8 channels	
	Retains 16-bit free-run timer value by (rising edge, falling edge, or the both edges), signals an interrupt.					
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width×12 8-bit reload registers for H pulse width×12				8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN interface	1 channel				3 channels	
	Compliant with CAN standard Version 2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by “H”/“L” level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash memory	—					
Corresponding evaluation name	MB90V340E-102		MB90V340E-101		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

2. Product Lineup 2 (With Clock supervisor function)

■ Flash memory products

Parameter \ Part Number	MB90F356E MB90F357E	MB90F356TE MB90F357TE	MB90F356ES MB90F357ES	MB90F356TES MB90F357TES
Type	Flash memory products			
CPU	F^2MC-16LX CPU			
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	64 Kbytes Flash memory : MB90F356E(S), MB90F356TE(S) 128 Kbytes Dual operation Flash memory (Erase/write and read can be operated at the same time) : MB90F357E(S), MB90F357TE(S)			
RAM	4 Kbytes			
Emulator-specific power supply*	—			
Sub clock pin (X0A, X1A)	Yes		No	
Clock supervisor	Yes			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 3.5 V to 5.5 V : at using A/D converter/Flash programming 3.5 V to 5.5 V : at using external bus			
Operating temperature range	−40°C to +125°C			
Package	LQFP-64			
LIN-UART	2 channels			
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 kbps)	1 channel			
A/D converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)			
16-bit reload timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit output compare	4 channels			
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

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Parameter \ Part Number	MB90F356E MB90F357E	MB90F356TE MB90F357TE	MB90F356ES MB90F357ES	MB90F356TES MB90F357TES
16-bit input capture	6 channels			
	Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.			
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width×12 8-bit reload registers for H pulse width×12			
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN interface	1 channel			
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.			
External interrupt	8 channels			
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.			
D/A converter	—			
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)			
Flash memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F357x only)			
Corresponding EVA name	MB90V340E-104		MB90V340E-103	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

■ MASK ROM products/Evaluation products

Parameter \ Part Number	MB90356E MB90357E	MB90356TE MB90357TE	MB90356ES MB90357ES	MB90356TES MB90357TES	MB90V340E-103	MB90V340E-104
CPU	F^2MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64 Kbytes :MB90356E(S), MB90356TE(S) 128 Kbytes :MB90357E(S), MB90357TE(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A)	Yes		No		No	Yes
Clock supervisor	Yes					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40°C to +125°C				—	
Package	LQFP-64				PGA-299	
LIN-UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 kbps)	1 channel				2 channels	
A/D converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit reload timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				Free-run Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. Free-run Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

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Parameter \ Part Number	MB90356E MB90357E	MB90356TE MB90357TE	MB90356ES MB90357ES	MB90356TES MB90357TES	MB90V340E-103	MB90V340E-104
16-bit output compare	4 channels				8 channels	
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit input capture	6 channels				8 channels	
	Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.					
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters×12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12				8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters×16 8-bit reload registers for L pulse width×16 8-bit reload registers for H pulse width×16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN interface	1 channel				3 channels	
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash memory	—					
Corresponding EVA name	MB90V340E-104		MB90V340E-103		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

3. Packages and Product Correspondence

Package	MB90V340E-101 MB90V340E-102 MB90V340E-103 MB90V340E-104	MB90351E (S) , MB90351TE (S) MB90F351E (S) , MB90F351TE (S) MB90352E (S) , MB90352TE (S) MB90F352E (S) , MB90F352TE (S) MB90356E (S) , MB90356TE (S) MB90F356E (S) , MB90F356TE (S) MB90357E (S) , MB90357TE (S) MB90F357E (S) , MB90F357TE (S)
PGA-299C-A01	◯	×
FPT-64P-M23 (12.0 mm □, 0.65 mm pitch)	×	◯
FPT-64P-M24 (10.0 mm □, 0.50 mm pitch)	×	◯

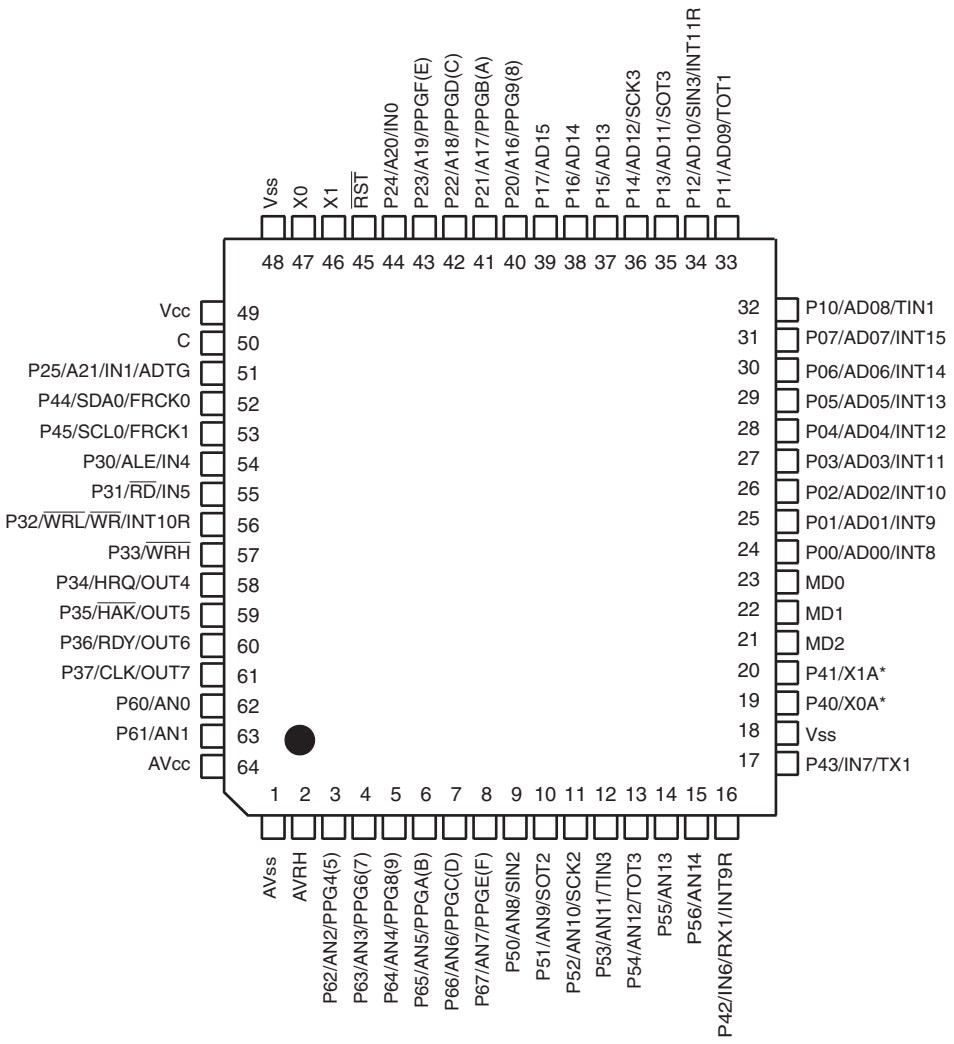
◯ : Yes, × : No

Note : Refer to “Package Dimensions” for detail of each package.

4. Pin Assignments

■ MB90351E (S) , MB90351TE (S) , MB90F351E (S) , MB90F351TE (S) , MB90352E (S) , MB90352TE (S) , MB90F352E (S) , MB90F352TE (S) , MB90356E (S) , MB90356TE (S) , MB90F356E (S) , MB90F356TE (S) , MB90357E (S) , MB90357TE (S) , MB90F357E (S) , MB90F357TE (S)

(TOP VIEW)



(FPT-64P-M23, FPT-64P-M24)

* : Devices without S-suffix : X0A, X1A
Devices with S-suffix : P40, P41

5. Pin Description

Pin No.	Pin name	I/O Circuit type*	Function
46	X1	A	Oscillation output pin
47	X0		Oscillation input pin
45	$\overline{RST}$	E	Reset input pin
3 to 8	P62 to P67	I	General purpose I/O ports
	AN2 to AN7		Analog input pins for A/D converter
	PPG4 (5) , 6 (7) , 8 (9) , A (B) , C (D) , E (F)		Output pins for PPGs
9	P50	O	General purpose I/O port
	AN8		Analog input pin for A/D converter
	SIN2		Serial data input pin for UART2
10	P51	I	General purpose I/O port
	AN9		Analog input pin for A/D converter
	SOT2		Serial data output pin for UART2
11	P52	I	General purpose I/O port
	AN10		Analog input pin for A/D converter
	SCK2		Serial clock I/O pin for UART2
12	P53	I	General purpose I/O port
	AN11		Analog input pin for A/D converter
	TIN3		Event input pin for reload timer3
13	P54	I	General purpose I/O port
	AN12		Analog input pin for A/D converter
	TOT3		Output pin for reload timer3
14, 15	P55, P56	I	General purpose I/O ports
	AN13, AN14		Analog input pins for A/D converter
16	P42	F	General purpose I/O port
	IN6		Data sample input pin for input capture ICU6
	RX1		RX input pin for CAN1
	INT9R		External interrupt request input pin for INT9
17	P43	F	General purpose I/O port
	IN7		Data sample input pin for input capture ICU7
	TX1		TX output pin for CAN1
19, 20	P40, P41	F	General purpose I/O ports (devices with S-suffix and MB90V340E-101/103)
	X0A, X1A	B	X0A : Oscillation input pin for sub clock X1A : Oscillation output pin for sub clock (devices without S-suffix and MB90V340E-102/104)

(Continued)

Pin No.	Pin name	I/O Circuit type*	Function
24 to 31	P00 to P07	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD00 to AD07		Input/output pins of external address data bus lower 8 bits. This function is enabled when the external bus is enabled.
	INT8 to INT15		External interrupt request input pins for INT8 to INT15
32	P10	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD08		Input/output pin for external bus address data bus bit 8. This function is enabled when external bus is enabled.
	TIN1		Event input pin for reload timer1
33	P11	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD09		Input/output pin for external bus address data bus bit 9. This function is enabled when external bus is enabled.
	TOT1		Output pin for reload timer1
34	P12	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD10		Input/output pin for external bus address data bus bit 10. This function is enabled when external bus is enabled.
	SIN3		Serial data input pin for UART3
	INT11R		External interrupt request input pin for INT11
35	P13	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD11		Input/output pin for external bus address data bus bit 11. This function is enabled when external bus is enabled.
	SOT3		Serial data output pin for UART3
36	P14	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD12		Input/output pin for external bus address data bus bit 12. This function is enabled when external bus is enabled.
	SCK3		Clock input/output pin for UART3
37	P15	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD13		Input/output pin for external bus address data bus bit 13. This function is enabled when external bus is enabled.
38	P16	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD14		Input/output pin for external bus address data bus bit 14. This function is enabled when external bus is enabled.

(Continued)

Pin No.	Pin name	I/O Circuit type*	Function
39	P17	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD15		Input/output pin for external bus address data bus bit 15. This function is enabled when external bus is enabled.
40 to 43	P20 to P23	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pins are enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A16 to A19		Output pins for A16 to A19 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins A16 to A19.
	PPG9 (8) PPGB (A) PPGD (C) PPGF (E)		Output pins for PPGs
44	P24	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A20		Output pin for A20 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A20.
	IN0		Data sample input pin for input capture ICU0
51	P25	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A21		Output pin for A21 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A21.
	IN1		Data sample input pin for input capture ICU1
	ADTG		Trigger input pin for A/D converter
52	P44	H	General purpose I/O port
	SDA0		Serial data I/O pin for I^2C 0
	FRCK0		Input pin for the 16-bit Free-run Timer 0
53	P45	H	General purpose I/O port
	SCL0		Serial clock I/O pin for I^2C 0
	FRCK1		Input pin for the 16-bit Free-run Timer 1

(Continued)

Pin No.	Pin name	I/O Circuit type*	Function
54	P30	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	ALE		Address latch enable output pin. This function is enabled when external bus is enabled.
	IN4		Data sample input pin for input capture ICU4
55	P31	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	$\overline{RD}$		Read strobe output pin for data bus. This function is enabled when external bus is enabled.
	IN5		Data sample input pin for input capture ICU5
56	P32	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the $\overline{WR}$/$\overline{WRL}$ pin output disabled.
	$\overline{WR}$/$\overline{WRL}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access. $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
	INT10R		External interrupt request input pin for INT10
57	P33	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode, in external bus 8-bit mode or with the $\overline{WRH}$ pin output disabled.
	$\overline{WRH}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.
58	P34	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT4		Wave form output pin for output compare OCU4
59	P35	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	$\overline{HAK}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT5		Wave form output pin for output compare OCU5
60	P36	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the external ready function disabled.
	RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
	OUT6		Wave form output pin for output compare OCU6

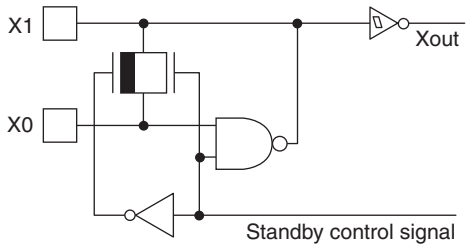
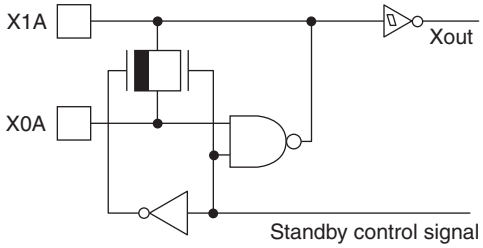
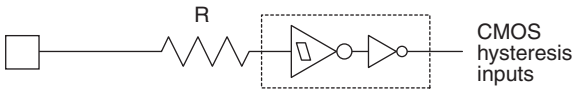
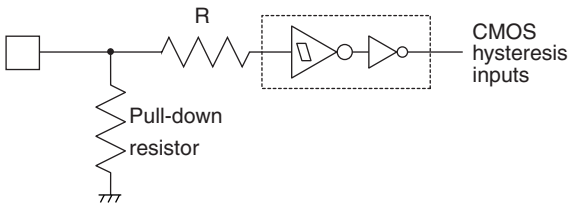
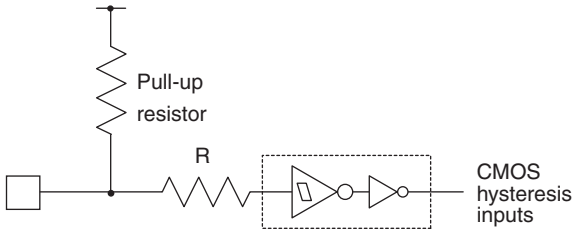
(Continued)

(Continued)

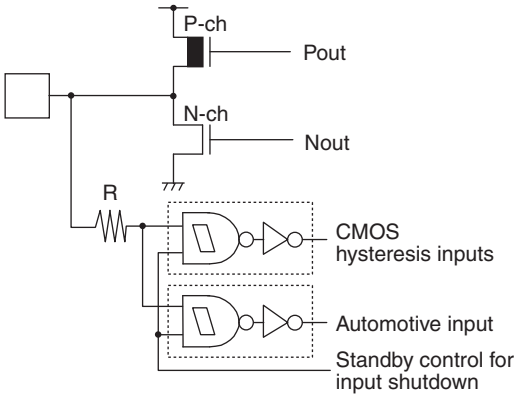
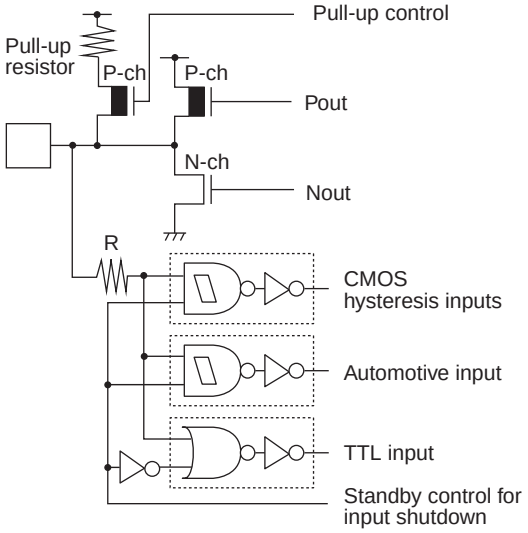
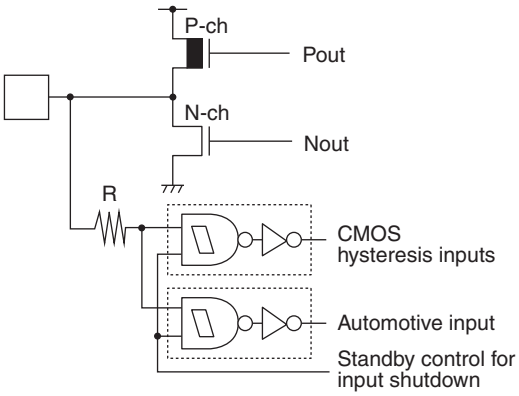
Pin No.	Pin name	I/O Circuit type*	Function
61	P37	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the CLK output disabled.
	CLK		CLK output pin. This function is enabled when both the external bus and CLK output are enabled.
	OUT7		Wave form output pin for output compare OCU7
62, 63	P60, P61	I	General purpose I/O ports
	AN0, AN1		Analog input pins for A/D converter
64	AV_{CC}	K	V_{CC} power input pin for analog circuits
2	AVRH	L	Reference voltage input for the A/D converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
1	AV_{SS}	K	V_{SS} power input pin for analog circuits
22, 23	MD1, MD0	C	Input pins for specifying the operating mode
21	MD2	D	Input pin for specifying the operating mode
49	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
18, 48	V_{SS}	—	Power (0 V) input pins
50	C	K	This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 μF ceramic capacitor.

* : For the I/O circuit type, refer to “I/O Circuit Type”.

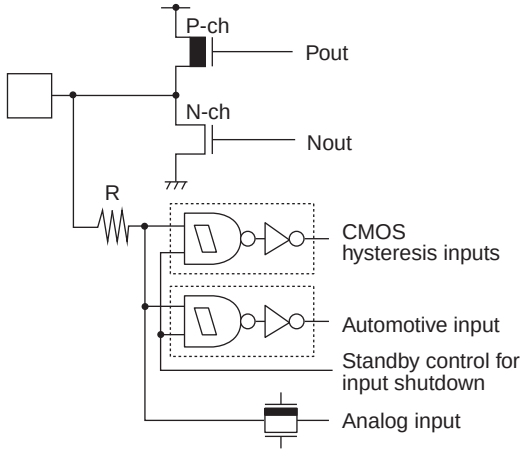
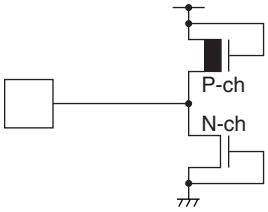
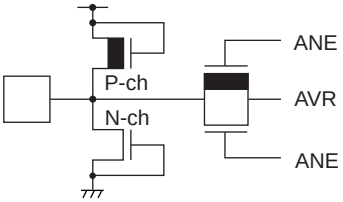
6. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM device CMOS hysteresis input pin ■ Flash memory device CMOS input pin
D		■ MASK ROM device CMOS hysteresis input pin Pull-down resistor value: approx. 50 kΩ ■ Flash memory device CMOS input pin No Pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

(Continued)

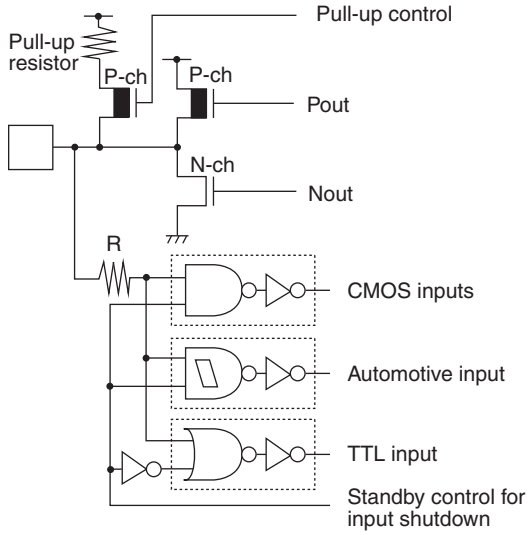
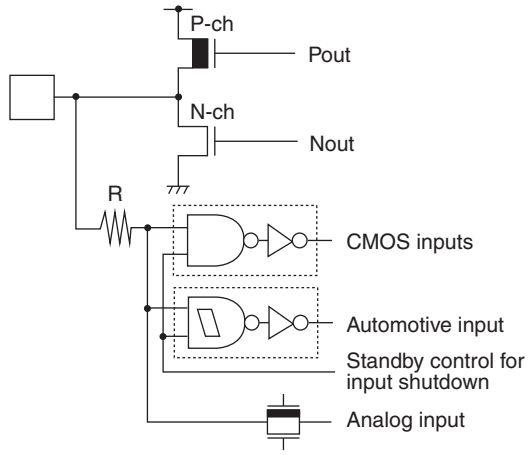
Type	Circuit	Remarks
F		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS hysteresis inputs (With input shutdown function when is standby) ■ Automotive input (With the standby-time input shutdown function)
G		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ TTL input (With the standby-time input shutdown function) ■ Programmable pull-up resistor: approx. 50 kΩ
H		■ CMOS level output (I_{OL} = 3 mA, I_{OH} = −3 mA) ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function)

(Continued)

Type	Circuit	Remarks
I		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ Analog input for A/D converter
K		Protection circuit for power supply input
L		■ With the protection circuit of A/D converter reference voltage power input pin ■ Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH.

(Continued)

(Continued)

Type	Circuit	Remarks
N		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ TTL input (With the standby-time input shutdown function) ■ Programmable pull-up resistor: approx. 50 kΩ
O		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ Analog input for A/D converter

7. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions :

■A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.

■A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.

■The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage (V_{CC}) .

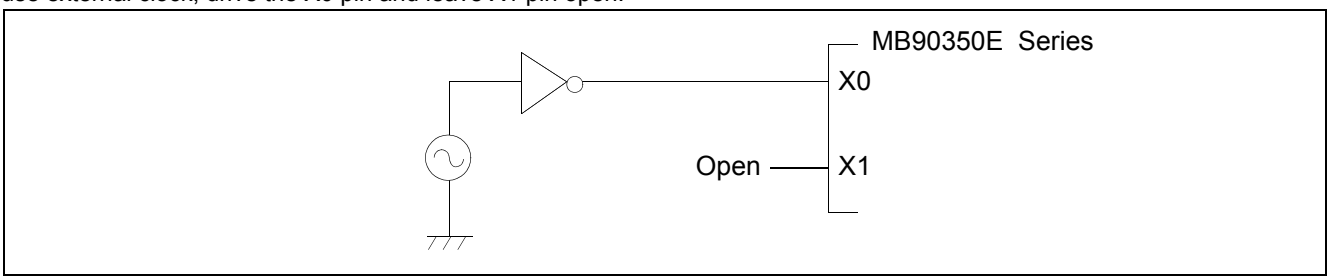
2. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

Unused I/O pins should be set to the output state and can be left open, or the input state with the above described connection.

3. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



4. Precautions for when not using a sub clock signal

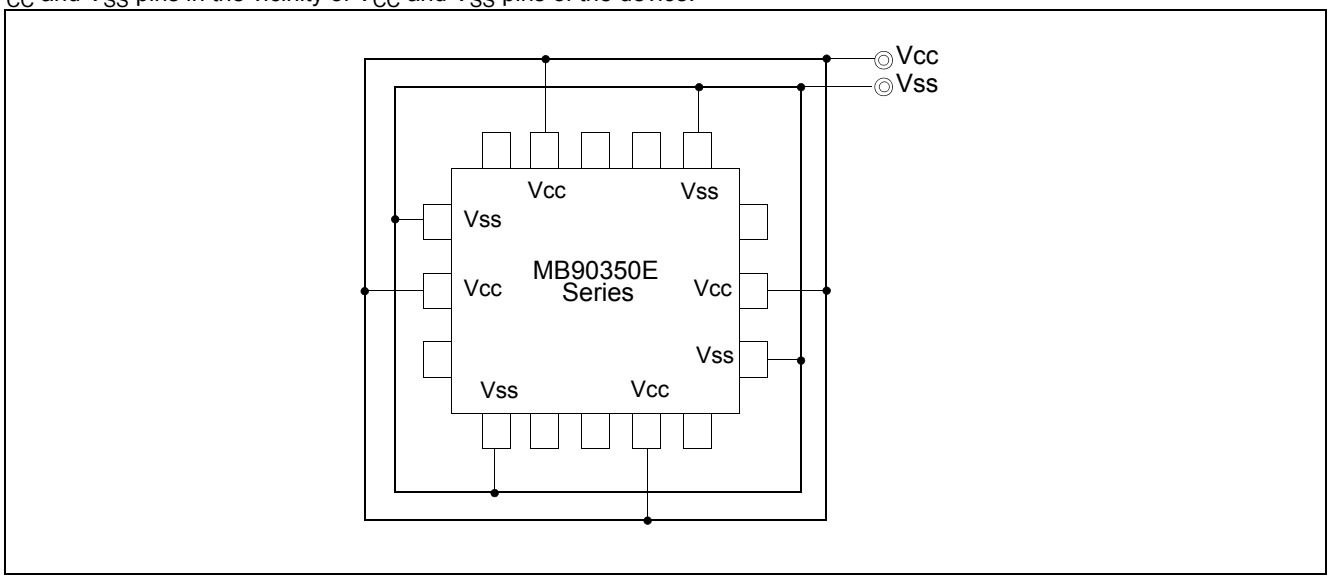
X0A and X1A are oscillation pins for sub clock. If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

5. Notes on during operation of PLL clock mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Cypress will not guarantee results of operations if such failure occurs.

6. Treatment of Power Supply Pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
  Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.
- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



7. Pull-up/down resistors

The MB90350E series does not support internal pull-up/down resistors (Port 0 to Port 3: built-in pull-up resistors). Use external components where needed.

8. Crystal oscillator circuit

Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

9. Turning-on sequence of power supply to A/D converter and analog inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN14) after turning-on the digital power supply (V_{CC}) .Turn-off the digital power after turning off the A/D converter power
supply and analog inputs. In this case, make sure that the power supply voltage does not exceed the rated voltage of the A/D converter (turning on/of the analog and digital power supplies simultaneously is acceptable).

10. Connection of unused pins of A/D converter if A/D converter is not used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

11. Notes on energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at
50 µs or more (0.2 V to 2.7 V) .

12. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/
60 MHz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

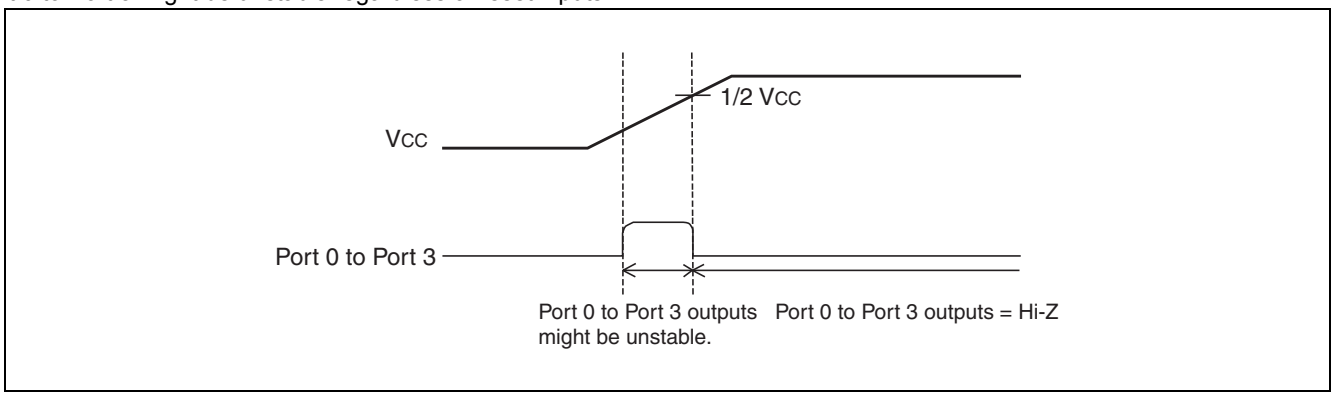
13. Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

14. Port 0 to port 3 output during power-on (External-bus mode)

As shown below, when power is turned on in external-bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable regardless of reset inputs.



15. Setting using CAN function

To use CAN function, please set “1” to DIRECT bit of CAN direct mode register (CDMR).

16. Flash security function

The security byte is located in the area of the Flash memory. If protection code 01_H is written in the security byte, the Flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Please refer to following table for the address of the security byte.

Product name	Flash memory size	Address for security bit
MB90F352E(S) MB90F352TE(S) MB90F357E(S) MB90F357TE(S)	Embedded 1 Mbit Flash memory	$FE0001_H$

17. Operation with T_A = +105°C or more

If used exceeding $T_A = +105°C$, please contact Cypress sales representatives for reliability limitations.

18. Low voltage/CPU operation reset circuit

The low voltage detection reset circuit is a function that monitors power supply voltage in order to detect when a voltage drops below a given voltage level. When a low voltage condition is detected, an internal reset signal is generated.
The CPU operation detection reset circuit is a 20-bit counter that uses oscillation as a count clock and generates an internal reset signal if not cleared within a given time after startup.

(1) Low voltage detection reset circuit

Detection voltage
4.0 V ± 0.3 V

When a low voltage condition is detected, the low voltage detection flag (LVRC : LVRF) is set to “1” and an internal reset signal is output.
Because the low voltage detection reset circuit continues to operate even in stop mode, detection of a low voltage condition generates an internal reset and releases stop mode.

During an internal RAM write cycle, low voltage reset is generated after the completion of writing. During the output of this internal reset, the reset output from the low voltage detection reset circuit is suppressed.

(2) CPU operation detection reset circuit

The CPU operation detection reset circuit is a counter that prevents program runaway. The counter starts automatically after a power-on reset, and must be continually and regularly cleared within a given time. If the given time interval elapses and the counter has not been cleared, a cause such as infinite program looping is assumed and an internal reset signal is generated. The internal reset generated from the CPU operation detection circuit has a width of 5 machine cycles.

Interval time
$2^{20}/F_C$ (approx. 262 ms*)

* : This value assumes the interval time at an oscillation clock frequency of 4 MHz.
During recovery from standby mode, the detection period is the maximum interval plus 20 μs.

This circuit does not operate in modes where CPU operation is stopped.
The CPU operation detection reset circuit counter is cleared under any of the following conditions.

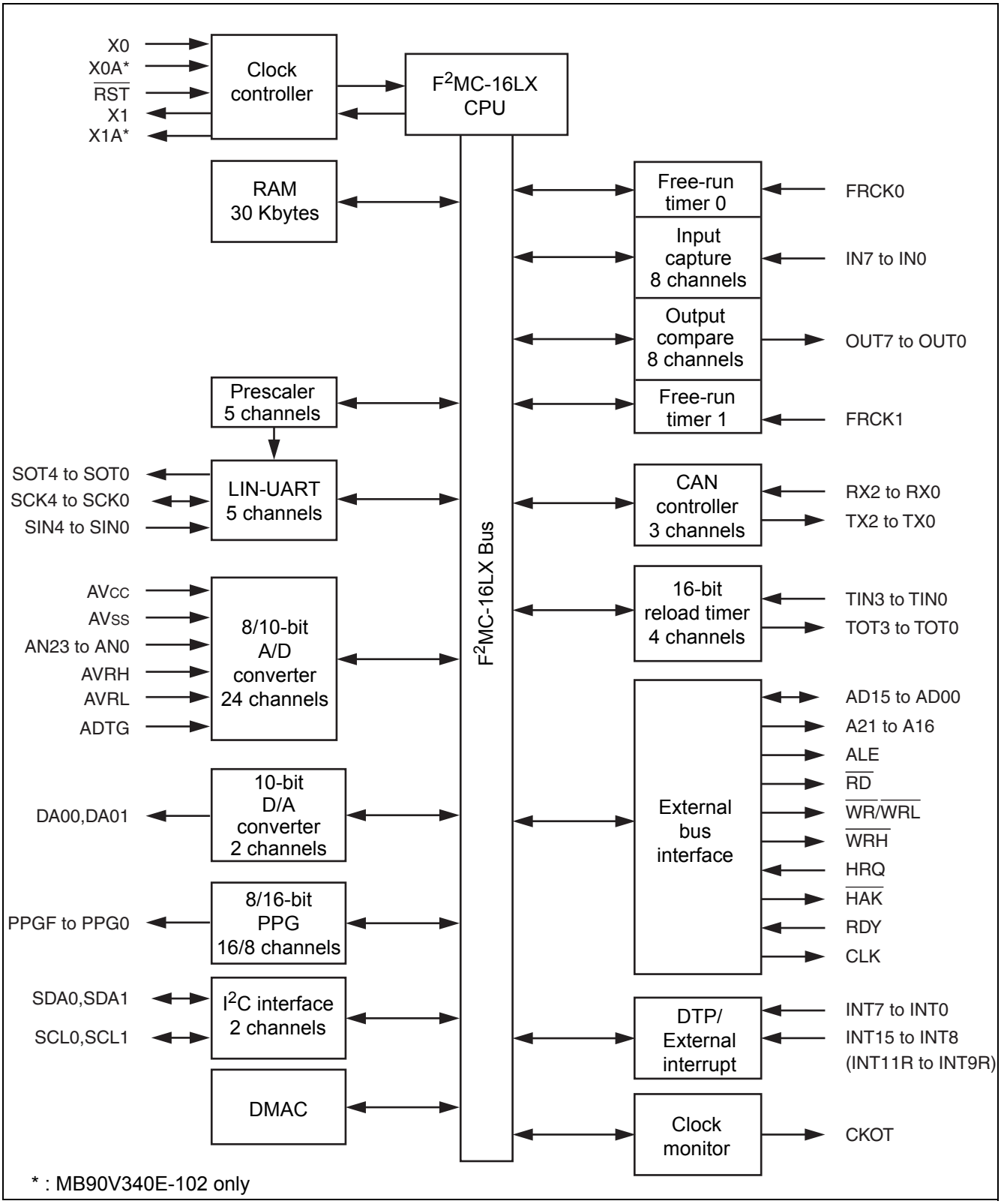
- ■“0” writing to CL bit of LVRC register
- ■Internal reset
- ■Main oscillation clock stop
- ■Transit to sleep mode
- ■Transit to timebase timer mode and watch mode

19. Internal CR oscillation circuit

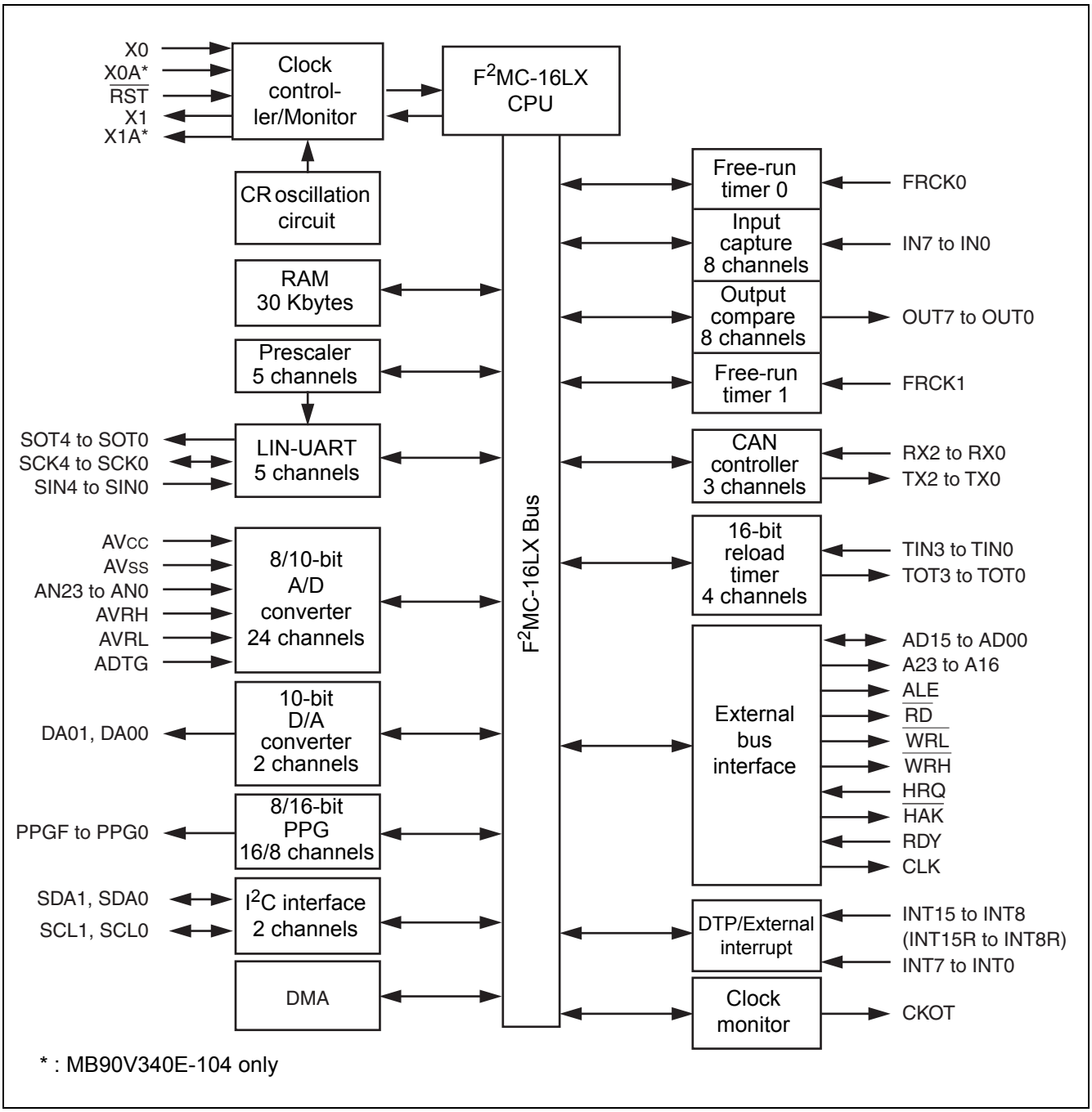
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Oscillation frequency	f_{RC}	50	100	200	kHz
Oscillation stabilization wait time	tstab	—	—	100	μs

8. Block Diagrams

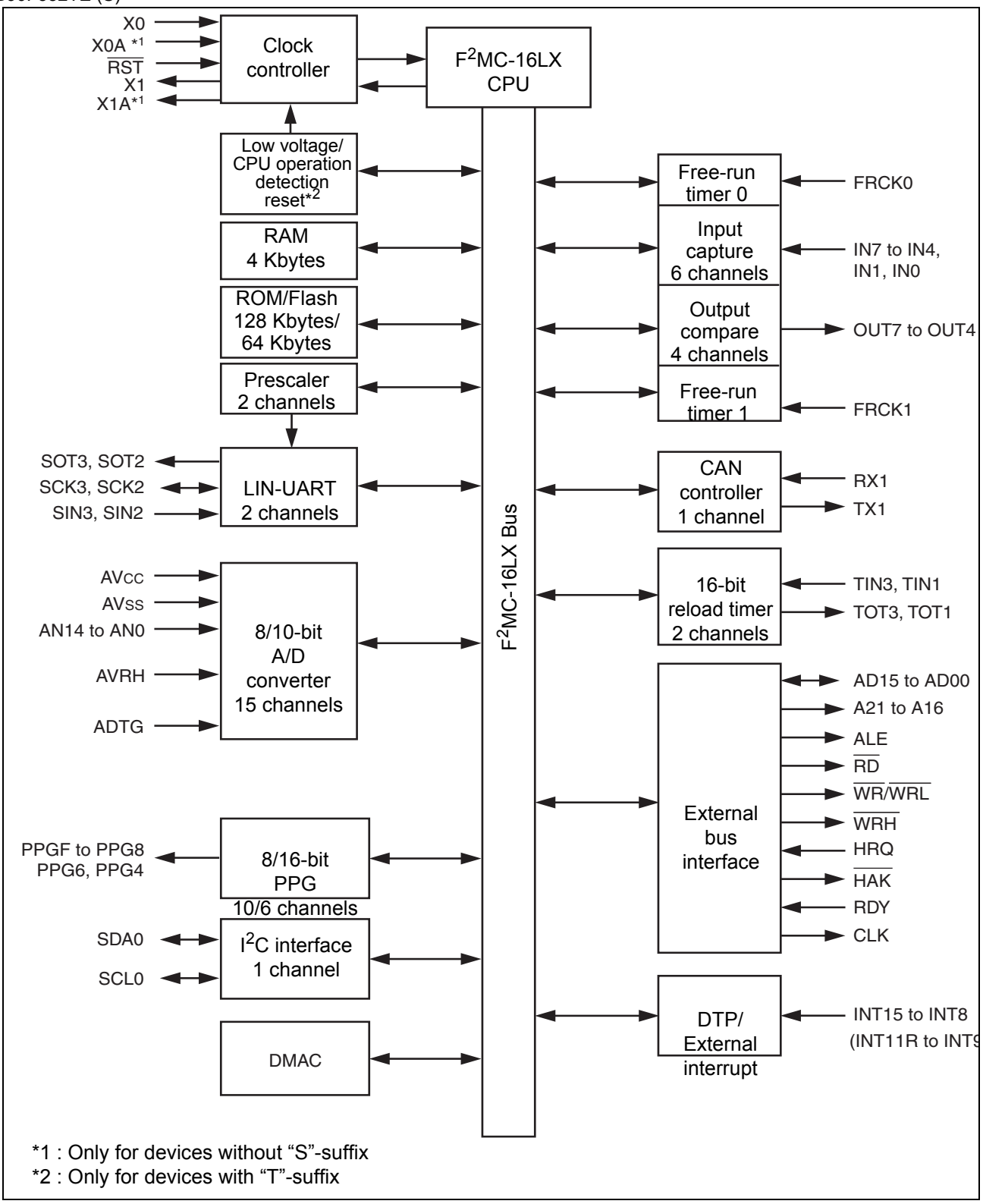
■ MB90V340E-101/102



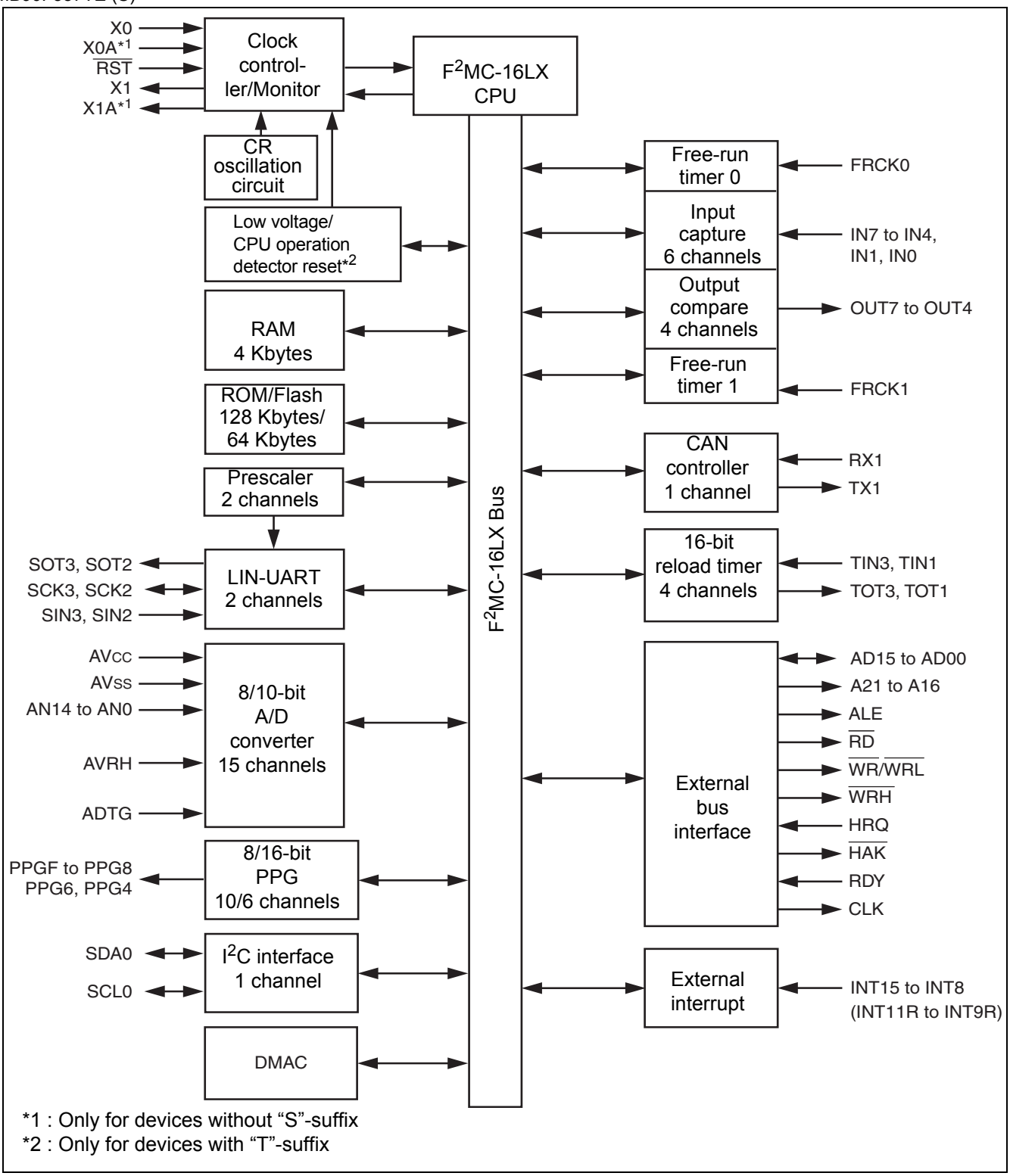
■ MB90V340E-103/104



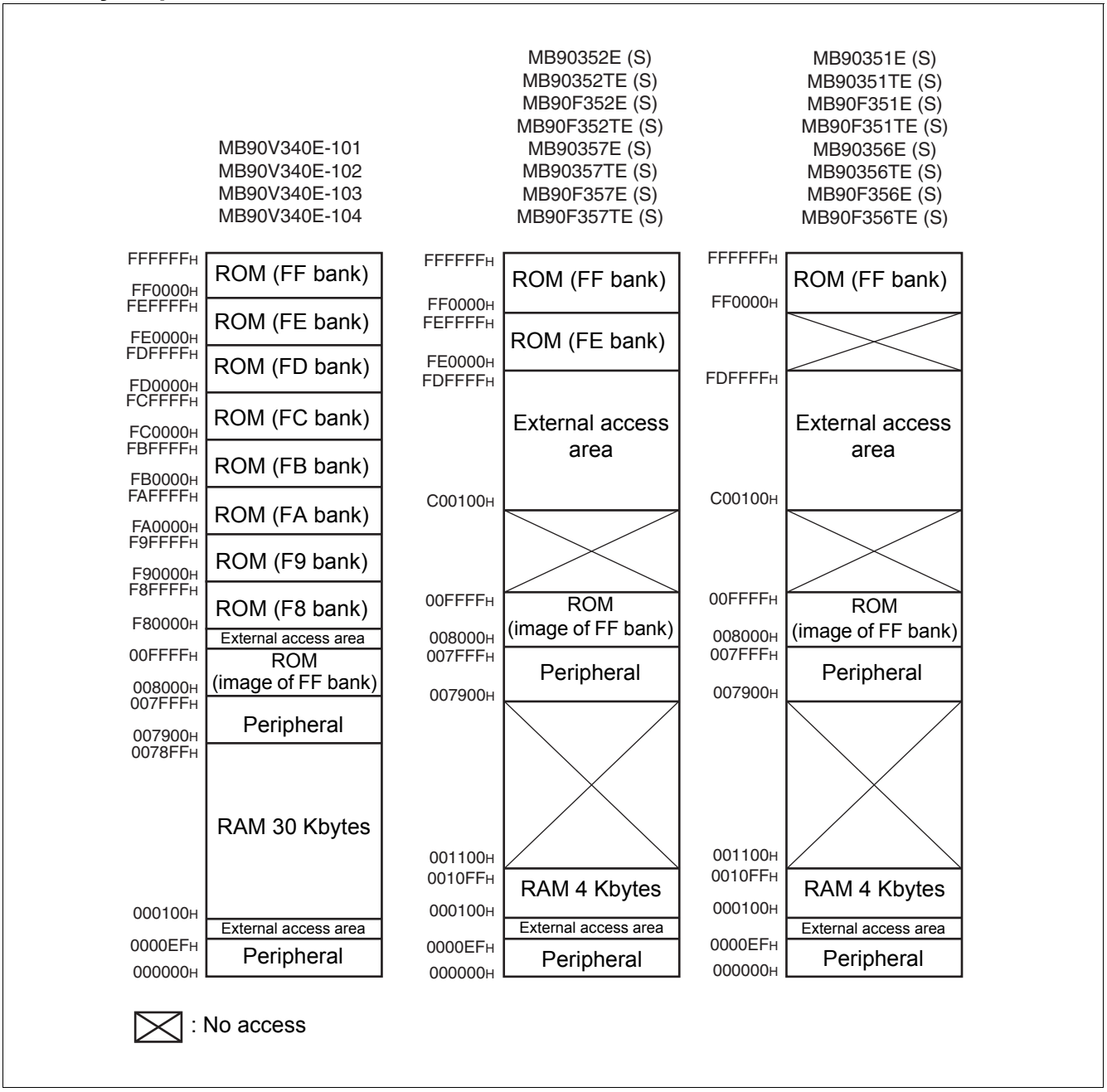
■ MB90351E (S) , MB90351TE (S) , MB90F351E (S) , MB90F351TE (S) , MB90352E (S) , MB90352TE (S) , MB90F352E (S) MB90F352TE (S)



■ MB90356E (S) , MB90356TE (S) , MB90F356E (S) , MB90F356TE (S) , MB90357E (S) , MB90357TE (S) , MB90F357E (S) , MB90F357TE (S)



9. Memory Map



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.

For example, an attempt to access $00C000_H$ practically accesses the value at $FFC000_H$ in ROM.

The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.

The image between $FF8000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF7FFF_H$ is visible only in bank FF.

10. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
000000_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
000001_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
000002_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
000003_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
000004_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
000005_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
000006_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
000007_H to $00000A_H$	Reserved				
$00000B_H$	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111_B
$00000C_H$	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111_B
$00000D_H$	Reserved				
$00000E_H$	Input Level Select Register 0	ILSR0	R/W	Ports	00000000_B
$00000F_H$	Input Level Select Register 1	ILSR1	R/W	Ports	00000000_B
000010_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
000011_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
000012_H	Port 2 Direction Register	DDR2	R/W	Port 2	$XX000000_B$
000013_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
000014_H	Port 4 Direction Register	DDR4	R/W	Port 4	$XX000000_B$
000015_H	Port 5 Direction Register	DDR5	R/W	Port 5	$X0000000_B$
000016_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
000017_H to 000019_H	Reserved				
$00001A_H$	SIN input Level Setting Register	DDRA	W	UART2, UART3	$X00XXXXX_B$
$00001B_H$	Reserved				
$00001C_H$	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000_B
$00001D_H$	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000_B
$00001E_H$	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000_B
$00001F_H$	Port 3 Pull-up Control Register	PUCR3	R/W	Port 3	00000000_B
000020_H to 000037_H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000038_H	PPG 4 Operation Mode Control Register	PPGC4	W, R/W	16-bit Programmable Pulse Generator 4/5	$0X000XX1_B$
000039_H	PPG 5 Operation Mode Control Register	PPGC5	W, R/W		$0X000001_B$
$00003A_H$	PPG 4/5 Count Clock Select Register	PPG45	R/W		$000000X0_B$
$00003B_H$	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000_B
$00003C_H$	PPG 6 Operation Mode Control Register	PPGC6	W, R/W	16-bit Programmable Pulse Generator 6/7	$0X000XX1_B$
$00003D_H$	PPG 7 Operation Mode Control Register	PPGC7	W, R/W		$0X000001_B$
$00003E_H$	PPG 6/7 Count Clock Select Register	PPG67	R/W		$000000X0_B$
$00003F_H$	Reserved				
000040_H	PPG 8 Operation Mode Control Register	PPGC8	W, R/W	16-bit Programmable Pulse Generator 8/9	$0X000XX1_B$
000041_H	PPG 9 Operation Mode Control Register	PPGC9	W, R/W		$0X000001_B$
000042_H	PPG 8/9 Count Clock Select Register	PPG89	R/W		$000000X0_B$
000043_H	Reserved				
000044_H	PPG A Operation Mode Control Register	PPGCA	W, R/W	16-bit Programmable Pulse Generator A/B	$0X000XX1_B$
000045_H	PPG B Operation Mode Control Register	PPGCB	W, R/W		$0X000001_B$
000046_H	PPG A/B Count Clock Select Register	PPGAB	R/W		$000000X0_B$
000047_H	Reserved				
000048_H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit Programmable Pulse Generator C/D	$0X000XX1_B$
000049_H	PPG D Operation Mode Control Register	PPGCD	W,R/W		$0X000001_B$
$00004A_H$	PPG C/D Count Clock Select Register	PPGCD	R/W		$000000X0_B$
$00004B_H$	Reserved				
$00004C_H$	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit Programmable Pulse Generator E/F	$0X000XX1_B$
$00004D_H$	PPG F Operation Mode Control Register	PPGCF	W,R/W		$0X000001_B$
$00004E_H$	PPG E/F Count Clock Select Register	PPGEF	R/W		$000000X0_B$
$00004F_H$	Reserved				
000050_H	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	00000000_B
000051_H	Input Capture Edge Register 0/1	ICE01	R/W, R		$XXX0X0XX_B$
000052_H, 000053_H	Reserved				
000054_H	Input Capture Control Status Register 4/5	ICS45	R/W	Input Capture 4/5	00000000_B
000055_H	Input Capture Edge Register 4/5	ICE45	R		$XXXXXXXX_B$
000056_H	Input Capture Control Status Register 6/7	ICS67	R/W	Input Capture 6/7	00000000_B
000057_H	Input Capture Edge Register 6/7	ICE67	R/W, R		$XXX000XX_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000058_H to $00005B_H$	Reserved				
$00005C_H$	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	$0000XX00_B$
$00005D_H$	Output Compare Control Status Register 5	OCS5	R/W		$0XX00000_B$
$00005E_H$	Output Compare Control Status Register 6	OCS6	R/W	Output Compare 6/7	$0000XX00_B$
$00005F_H$	Output Compare Control Status Register 7	OCS7	R/W		$0XX00000_B$
000060_H	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000_B
000061_H	Timer Control Status Register 0	TMCSR0	R/W		$XXXX0000_B$
000062_H	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000_B
000063_H	Timer Control Status Register 1	TMCSR1	R/W		$XXXX0000_B$
000064_H	Timer Control Status Register 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000_B
000065_H	Timer Control Status Register 2	TMCSR2	R/W		$XXXX0000_B$
000066_H	Timer Control Status Register 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000_B
000067_H	Timer Control Status Register 3	TMCSR3	R/W		$XXXX0000_B$
000068_H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	$000XXXX0_B$
000069_H	A/D Control Status Register 1	ADCS1	R/W		$0000000X_B$
$00006A_H$	A/D Data Register 0	ADCR0	R		00000000_B
$00006B_H$	A/D Data Register 1	ADCR1	R		$XXXXXX00_B$
$00006C_H$	ADC Setting Register 0	ADSR0	R/W		00000000_B
$00006D_H$	ADC Setting Register 1	ADSR1	R/W		00000000_B
$00006E_H$	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W	Low Voltage/CPU Operation Detection Reset	00111000_B
$00006F_H$	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	$XXXXXXX1_B$
000070_H to $00007F_H$	Reserved				
000080_H to $00008F_H$	Reserved for CAN controller 1. Refer to “CAN Controllers”				
000090_H to $00009A_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$00009B_H$	DMA Descriptor Channel Specification Register	DCSR	R/W	DMA	00000000_B
$00009C_H$	DMA Status Register L Register	DSRL	R/W		00000000_B
$00009D_H$	DMA Status Register H Register	DSRH	R/W		00000000_B
$00009E_H$	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000_B
$00009F_H$	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt	$XXXXXXX0_B$
$0000A0_H$	Low-power Consumption Mode Control Register	LPMCR	W,R/W	Low Power Consumption Control Circuit	00011000_B
$0000A1_H$	Clock Selection Register	CKSCR	R,R/W	Low Power Consumption Control Circuit	11111100_B
$0000A2_H$, $0000A3_H$	Reserved				
$0000A4_H$	DMA Stop Status Register	DSSR	R/W	DMA	00000000_B
$0000A5_H$	Automatic Ready Function Selection Register	ARSR	W	External Memory Access	$0011XX00_B$
$0000A6_H$	External Address Output Control Register	HACR	W		00000000_B
$0000A7_H$	Bus Control Signal Selection Register	ECSR	W		$0000000X_B$
$0000A8_H$	Watchdog Control Register	WDTC	R,W	Watchdog Timer	$XXXXX111_B$
$0000A9_H$	Timebase Timer Control Register	TBTC	W,R/W	Timebase timer	$1XX00100_B$
$0000AA_H$	Watch Timer Control Register	WTC	R,R/W	Watch Timer	$1X001000_B$
$0000AB_H$	Reserved				
$0000AC_H$	DMA Enable Register L Register	DERL	R/W	DMA	00000000_B
$0000AD_H$	DMA Enable Register H Register	DERH	R/W		00000000_B
$0000AE_H$	Flash Control Status Register (Flash Devices only. Otherwise reserved)	FMCS	R,R/W	Flash memory	$000X0000_B$
$0000AF_H$	Reserved				
$0000B0_H$	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111_B
$0000B1_H$	Interrupt Control Register 01	ICR01	W,R/W		00000111_B
$0000B2_H$	Interrupt Control Register 02	ICR02	W,R/W		00000111_B
$0000B3_H$	Interrupt Control Register 03	ICR03	W,R/W		00000111_B
$0000B4_H$	Interrupt Control Register 04	ICR04	W,R/W		00000111_B
$0000B5_H$	Interrupt Control Register 05	ICR05	W,R/W		00000111_B
$0000B6_H$	Interrupt Control Register 06	ICR06	W,R/W		00000111_B
$0000B7_H$	Interrupt Control Register 07	ICR07	W,R/W		00000111_B
$0000B8_H$	Interrupt Control Register 08	ICR08	W,R/W		00000111_B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$0000B9_H$	Interrupt Control Register 09	ICR09	W,R/W	Interrupt Control	00000111_B
$0000BA_H$	Interrupt Control Register 10	ICR10	W,R/W		00000111_B
$0000BB_H$	Interrupt Control Register 11	ICR11	W,R/W		00000111_B
$0000BC_H$	Interrupt Control Register 12	ICR12	W,R/W		00000111_B
$0000BD_H$	Interrupt Control Register 13	ICR13	W,R/W		00000111_B
$0000BE_H$	Interrupt Control Register 14	ICR14	W,R/W		00000111_B
$0000BF_H$	Interrupt Control Register 15	ICR15	W,R/W		00000111_B
$0000C0_H$ to $0000C9_H$	Reserved				
$0000CA_H$	External Interrupt Enable Register 1	ENIR1	R/W	External Interrupt 1	00000000_B
$0000CB_H$	External Interrupt Source Register 1	EIRR1	R/W		$XXXXXXXX_B$
$0000CC_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000_B
$0000CD_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000_B
$0000CE_H$	External Interrupt Source Select Register	EISSR	R/W		00000000_B
$0000CF_H$	PLL/Sub clock Control register	PSCCR	W	PLL	$XXXX0000_B$
$0000D0_H$	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	$XXXXXXXX_B$
$0000D1_H$	DMA Buffer Address Pointer M Register	BAPM	R/W		$XXXXXXXX_B$
$0000D2_H$	DMA Buffer Address Pointer H Register	BAPH	R/W		$XXXXXXXX_B$
$0000D3_H$	DMA Control Register	DMACS	R/W		$XXXXXXXX_B$
$0000D4_H$	I/O Register Address Pointer L Register	IOAL	R/W		$XXXXXXXX_B$
$0000D5_H$	I/O Register Address Pointer H Register	IOAH	R/W		$XXXXXXXX_B$
$0000D6_H$	Data Counter L Register	DCTL	R/W		$XXXXXXXX_B$
$0000D7_H$	Data Counter H Register	DCTH	R/W		$XXXXXXXX_B$
$0000D8_H$	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000_B
$0000D9_H$	Serial Control Register 2	SCR2	W,R/W		00000000_B
$0000DA_H$	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000_B
$0000DB_H$	Serial Status Register 2	SSR2	R,R/W		00001000_B
$0000DC_H$	Extended Communication Control Register 2	ECCR2	R,W, R/W		$000000XX_B$
$0000DD_H$	Extended Status/Control Register 2	ESCR2	R/W		00000100_B
$0000DE_H$	Baud Rate Generator Register 20	BGR20	R/W		00000000_B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$0000DF_H$	Baud Rate Generator Register 21	BGR21	R/W	UART2	00000000_B
$0000E0_H$ to $0000EF_H$	Reserved				
$0000F0_H$ to $0000FF_H$	External area				
007900_H to 007907_H	Reserved				
007908_H	Reload Register L4	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	$XXXXXXXX_B$
007909_H	Reload Register H4	PRLH4	R/W		$XXXXXXXX_B$
$00790A_H$	Reload Register L5	PRLL5	R/W		$XXXXXXXX_B$
$00790B_H$	Reload Register H5	PRLH5	R/W		$XXXXXXXX_B$
$00790C_H$	Reload Register L6	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	$XXXXXXXX_B$
$00790D_H$	Reload Register H6	PRLH6	R/W		$XXXXXXXX_B$
$00790E_H$	Reload Register L7	PRLL7	R/W		$XXXXXXXX_B$
$00790F_H$	Reload Register H7	PRLH7	R/W		$XXXXXXXX_B$
007910_H	Reload Register L8	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	$XXXXXXXX_B$
007911_H	Reload Register H8	PRLH8	R/W		$XXXXXXXX_B$
007912_H	Reload Register L9	PRLL9	R/W		$XXXXXXXX_B$
007913_H	Reload Register H9	PRLH9	R/W		$XXXXXXXX_B$
007914_H	Reload Register LA	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	$XXXXXXXX_B$
007915_H	Reload Register HA	PRLHA	R/W		$XXXXXXXX_B$
007916_H	Reload Register LB	PRLLB	R/W		$XXXXXXXX_B$
007917_H	Reload Register HB	PRLHB	R/W		$XXXXXXXX_B$
007918_H	Reload Register LC	PRLLC	R/W	16-bit Programmable Pulse Generator C/D	$XXXXXXXX_B$
007919_H	Reload Register HC	PRLHC	R/W		$XXXXXXXX_B$
$00791A_H$	Reload Register LD	PRLLD	R/W		$XXXXXXXX_B$
$00791B_H$	Reload Register HD	PRLHD	R/W		$XXXXXXXX_B$
$00791C_H$	Reload Register LE	PRLLE	R/W	16-bit Programmable Pulse Generator E/F	$XXXXXXXX_B$
$00791D_H$	Reload Register HE	PRLHE	R/W		$XXXXXXXX_B$
$00791E_H$	Reload Register LF	PRLLF	R/W		$XXXXXXXX_B$
$00791F_H$	Reload Register HF	PRLHF	R/W		$XXXXXXXX_B$
007920_H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	$XXXXXXXX_B$
007921_H	Input Capture Register 0	IPCP0	R		$XXXXXXXX_B$
007922_H	Input Capture Register 1	IPCP1	R		$XXXXXXXX_B$
007923_H	Input Capture Register 1	IPCP1	R		$XXXXXXXX_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007924_H to 007927_H	Reserved				
007928_H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	$XXXXXXXX_B$
007929_H	Input Capture Register 4	IPCP4	R		$XXXXXXXX_B$
$00792A_H$	Input Capture Register 5	IPCP5	R		$XXXXXXXX_B$
$00792B_H$	Input Capture Register 5	IPCP5	R		$XXXXXXXX_B$
$00792C_H$	Input Capture Register 6	IPCP6	R	Input Capture 6/7	$XXXXXXXX_B$
$00792D_H$	Input Capture Register 6	IPCP6	R		$XXXXXXXX_B$
$00792E_H$	Input Capture Register 7	IPCP7	R		$XXXXXXXX_B$
$00792F_H$	Input Capture Register 7	IPCP7	R		$XXXXXXXX_B$
007930_H to 007937_H	Reserved				
007938_H	Output Compare Register 4	OCCP4	R/W	Output Compare 4/5	$XXXXXXXX_B$
007939_H	Output Compare Register 4	OCCP4	R/W		$XXXXXXXX_B$
$00793A_H$	Output Compare Register 5	OCCP5	R/W		$XXXXXXXX_B$
$00793B_H$	Output Compare Register 5	OCCP5	R/W		$XXXXXXXX_B$
$00793C_H$	Output Compare Register 6	OCCP6	R/W	Output Compare 6/7	$XXXXXXXX_B$
$00793D_H$	Output Compare Register 6	OCCP6	R/W		$XXXXXXXX_B$
$00793E_H$	Output Compare Register 7	OCCP7	R/W		$XXXXXXXX_B$
$00793F_H$	Output Compare Register 7	OCCP7	R/W		$XXXXXXXX_B$
007940_H	Timer Data Register 0	TCDT0	R/W	Free-run Timer 0	00000000_B
007941_H	Timer Data Register 0	TCDT0	R/W		00000000_B
007942_H	Timer Control Status Register 0	TCCSL0	R/W		00000000_B
007943_H	Timer Control Status Register 0	TCCSH0	R/W		$0XXXXXXX_B$
007944_H	Timer Data Register 1	TCDT1	R/W	Free-run Timer 1	00000000_B
007945_H	Timer Data Register 1	TCDT1	R/W		00000000_B
007946_H	Timer Control Status Register 1	TCCSL1	R/W		00000000_B
007947_H	Timer Control Status Register 1	TCCSH1	R/W		$0XXXXXXX_B$
007948_H	Timer Register 0/Reload Register 0	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	$XXXXXXXX_B$
007949_H			R/W		$XXXXXXXX_B$
$00794A_H$	Timer Register 1/Reload Register 1	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	$XXXXXXXX_B$
$00794B_H$			R/W		$XXXXXXXX_B$
$00794C_H$	Timer Register 2/Reload Register 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	$XXXXXXXX_B$
$00794D_H$			R/W		$XXXXXXXX_B$
$00794E_H$	Timer Register 3/Reload Register 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	$XXXXXXXX_B$
$00794F_H$			R/W		$XXXXXXXX_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007950_H	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000_B
007951_H	Serial Control Register 3	SCR3	W, R/W		00000000_B
007952_H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000_B
007953_H	Serial Status Register 3	SSR3	R,R/W		00001000_B
007954_H	Extended Communication Control Register 3	ECCR3	R,W, R/W		$000000XX_B$
007955_H	Extended Status Control Register 3	ESCR3	R/W		00000100_B
007956_H	Baud Rate Generator Register 30	BGR30	R/W		00000000_B
007957_H	Baud Rate Generator Register 31	BGR31	R/W		00000000_B
007958_H, 007959_H	Reserved				
007960_H	Clock supervisor Control Register	CSVCR	R, R/W	Clock Supervisor	00011100_B
007961_H to $00796D_H$	Reserved				
$00796E_H$	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	$XXXXXXX0_B$
$00796F_H$	Reserved				
007970_H	I^2C Bus Status Register 0	IBSR0	R	I^2C Interface 0	00000000_B
007971_H	I^2C Bus Control Register 0	IBCR0	W,R/W		00000000_B
007972_H	I^2C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000_B
007973_H		ITBAH0	R/W		00000000_B
007974_H	I^2C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111_B
007975_H		ITMKH0	R/W		00111111_B
007976_H	I^2C 7-bit Slave Address Register 0	ISBA0	R/W		00000000_B
007977_H	I^2C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111_B
007978_H	I^2C data register 0	IDAR0	R/W		00000000_B
007979_H, $00797A_H$	Reserved				
$00797B_H$	I^2C Clock Control Register 0	ICCR0	R/W	I^2C Interface 0	00011111_B
$00797C_H$ to $0079A1_H$	Reserved				
$0079A2_H$	Flash Write Control Register 0	FWR0	R/W	Dual Operation Flash	00000000_B
$0079A3_H$	Flash Write Control Register 1	FWR1	R/W		00000000_B
$0079A4_H$	Sector Change Setting Register 0	SSR0	R/W		$00XXXXX0_B$
$0079A5_H$ to $0079C1_H$	Reserved				
$0079C2_H$	Clock modulator Control Register	CMCR	R, R/W	Clock Modulator	$0001X000_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
$0079C3_H$ to $0079DF_H$	Reserved				
$0079E0_H$	Detect Address Setting Register 0	PADR0	R/W	Address Match Detection 0	$XXXXXXXX_B$
$0079E1_H$	Detect Address Setting Register 0	PADR0	R/W		$XXXXXXXX_B$
$0079E2_H$	Detect Address Setting Register 0	PADR0	R/W		$XXXXXXXX_B$
$0079E3_H$	Detect Address Setting Register 1	PADR1	R/W		$XXXXXXXX_B$
$0079E4_H$	Detect Address Setting Register 1	PADR1	R/W		$XXXXXXXX_B$
$0079E5_H$	Detect Address Setting Register 1	PADR1	R/W		$XXXXXXXX_B$
$0079E6_H$	Detect Address Setting Register 2	PADR2	R/W		$XXXXXXXX_B$
$0079E7_H$	Detect Address Setting Register 2	PADR2	R/W		$XXXXXXXX_B$
$0079E8_H$	Detect Address Setting Register 2	PADR2	R/W		$XXXXXXXX_B$
$0079E9_H$ to $0079EF_H$	Reserved				
$0079F0_H$	Detect Address Setting Register 3	PADR3	R/W	Address Match Detection 1	$XXXXXXXX_B$
$0079F1_H$	Detect Address Setting Register 3	PADR3	R/W		$XXXXXXXX_B$
$0079F2_H$	Detect Address Setting Register 3	PADR3	R/W		$XXXXXXXX_B$
$0079F3_H$	Detect Address Setting Register 4	PADR4	R/W		$XXXXXXXX_B$
$0079F4_H$	Detect Address Setting Register 4	PADR4	R/W		$XXXXXXXX_B$
$0079F5_H$	Detect Address Setting Register 4	PADR4	R/W		$XXXXXXXX_B$
$0079F6_H$	Detect Address Setting Register 5	PADR5	R/W		$XXXXXXXX_B$
$0079F7_H$	Detect Address Setting Register 5	PADR5	R/W		$XXXXXXXX_B$
$0079F8_H$	Detect Address Setting Register 5	PADR5	R/W		$XXXXXXXX_B$
$0079F9_H$ to $007BFF_H$	Reserved				
$007C00_H$ to $007DFF_H$	Reserved for CAN controller 1. Refer to “CAN Controllers”				
$007E00_H$ to $007FFF_H$	Reserved				

Notes : ″ Initial value of “X” represents unknown value.
″ Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results reading unknown value.

11. CAN Controllers

■ Compliant with CAN standard Version2.0 Part A and Part B
- Supports tr12ansmission/reception in standard frame and extended frame formats

■ Supports transmitting of data frames by receiving remote frames

■ 16 transmitting/receiving message buffers
- 29-bit ID and 8-byte data
- Multi-level message buffer configuration

■ Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats

■ Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address CAN1	Register	Abbreviation	Access	Initial Value
000080_H	Message buffer enable register	BVALR	R/W	00000000_B 00000000_B
000081_H				
000082_H	Transmit request register	TREQR	R/W	00000000_B 00000000_B
000083_H				
000084_H	Transmit cancel register	TCANR	W	00000000_B 00000000_B
000085_H				
000086_H	Transmission complete register	TCR	R/W	00000000_B 00000000_B
000087_H				
000088_H	Receive complete register	RCR	R/W	00000000_B 00000000_B
000089_H				
$00008A_H$	Remote request receiving register	RRTRR	R/W	00000000_B 00000000_B
$00008B_H$				
$00008C_H$	Receive overrun register	ROVRR	R/W	00000000_B 00000000_B
$00008D_H$				
$00008E_H$	Reception interrupt enable register	RIER	R/W	00000000_B 00000000_B
$00008F_H$				

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Address CAN1	Register	Abbreviation	Access	Initial Value
$007D00_H$	Control status register	CSR	R/W, W R/W, R	$0XXXX0X1_B$ $00XXX000_B$
$007D01_H$				
$007D02_H$	Last event indicator register	LEIR	R/W	$000X0000_B$ $XXXXXXXX_B$
$007D03_H$				
$007D04_H$	Receive/transmit error counter	RTEC	R	00000000_B 00000000_B
$007D05_H$				
$007D06_H$	Bit timing register	BTR	R/W	11111111_B $X1111111_B$
$007D07_H$				
$007D08_H$	IDE register	IDER	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D09_H$				
$007D0A_H$	Transmit RTR register	TRTRR	R/W	00000000_B 00000000_B
$007D0B_H$				
$007D0C_H$	Remote frame receive waiting register	RFWTR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D0D_H$				
$007D0E_H$	Transmit interrupt enable register	TIER	R/W	00000000_B 00000000_B
$007D0F_H$				
$007D10_H$	Acceptance mask select register	AMSR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D11_H$				
$007D12_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D13_H$				
$007D14_H$	Acceptance mask register 0	AMR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D15_H$				
$007D16_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D17_H$				
$007D18_H$	Acceptance mask register 1	AMR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D19_H$				
$007D1A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D1B_H$				

List of Message Buffers (ID Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C00_H$ to $007C1F_H$	General-purpose RAM	—	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C20_H$	ID register 0	IDR0	R/W	$XXXXXXXX_B$
$007C21_H$				$XXXXXXXX_B$
$007C22_H$				$XXXXXXXX_B$
$007C23_H$				$XXXXXXXX_B$
$007C24_H$	ID register 1	IDR1	R/W	$XXXXXXXX_B$
$007C25_H$				$XXXXXXXX_B$
$007C26_H$				$XXXXXXXX_B$
$007C27_H$				$XXXXXXXX_B$
$007C28_H$	ID register 2	IDR2	R/W	$XXXXXXXX_B$
$007C29_H$				$XXXXXXXX_B$
$007C2A_H$				$XXXXXXXX_B$
$007C2B_H$				$XXXXXXXX_B$
$007C2C_H$	ID register 3	IDR3	R/W	$XXXXXXXX_B$
$007C2D_H$				$XXXXXXXX_B$
$007C2E_H$				$XXXXXXXX_B$
$007C2F_H$				$XXXXXXXX_B$
$007C30_H$	ID register 4	IDR4	R/W	$XXXXXXXX_B$
$007C31_H$				$XXXXXXXX_B$
$007C32_H$				$XXXXXXXX_B$
$007C33_H$				$XXXXXXXX_B$
$007C34_H$	ID register 5	IDR5	R/W	$XXXXXXXX_B$
$007C35_H$				$XXXXXXXX_B$
$007C36_H$				$XXXXXXXX_B$
$007C37_H$				$XXXXXXXX_B$
$007C38_H$	ID register 6	IDR6	R/W	$XXXXXXXX_B$
$007C39_H$				$XXXXXXXX_B$
$007C3A_H$				$XXXXXXXX_B$
$007C3B_H$				$XXXXXXXX_B$
$007C3C_H$	ID register 7	IDR7	R/W	$XXXXXXXX_B$
$007C3D_H$				$XXXXXXXX_B$
$007C3E_H$				$XXXXXXXX_B$
$007C3F_H$				$XXXXXXXX_B$

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Address CAN1	Register	Abbreviation	Access	Initial Value
$007C40_H$	ID register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C41_H$				
$007C42_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C43_H$				
$007C44_H$	ID register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C45_H$				
$007C46_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C47_H$				
$007C48_H$	ID register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C49_H$				
$007C4A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C4B_H$				
$007C4C_H$	ID register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C4D_H$				
$007C4E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C4F_H$				
$007C50_H$	ID register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C51_H$				
$007C52_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C53_H$				
$007C54_H$	ID register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C55_H$				
$007C56_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C57_H$				
$007C58_H$	ID register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C59_H$				
$007C5A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C5B_H$				
$007C5C_H$	ID register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C5D_H$				
$007C5E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C5F_H$				

List of Message Buffers (DLC Registers and Data Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C60_H$	DLC register 0	DLCR0	R/W	$XXXXXXXX_B$
$007C61_H$				
$007C62_H$	DLC register 1	DLCR1	R/W	$XXXXXXXX_B$
$007C63_H$				
$007C64_H$	DLC register 2	DLCR2	R/W	$XXXXXXXX_B$
$007C65_H$				
$007C66_H$	DLC register 3	DLCR3	R/W	$XXXXXXXX_B$
$007C67_H$				
$007C68_H$	DLC register 4	DLCR4	R/W	$XXXXXXXX_B$
$007C69_H$				
$007C6A_H$	DLC register 5	DLCR5	R/W	$XXXXXXXX_B$
$007C6B_H$				
$007C6C_H$	DLC register 6	DLCR6	R/W	$XXXXXXXX_B$
$007C6D_H$				
$007C6E_H$	DLC register 7	DLCR7	R/W	$XXXXXXXX_B$
$007C6F_H$				
$007C70_H$	DLC register 8	DLCR8	R/W	$XXXXXXXX_B$
$007C71_H$				
$007C72_H$	DLC register 9	DLCR9	R/W	$XXXXXXXX_B$
$007C73_H$				
$007C74_H$	DLC register 10	DLCR10	R/W	$XXXXXXXX_B$
$007C75_H$				
$007C76_H$	DLC register 11	DLCR11	R/W	$XXXXXXXX_B$
$007C77_H$				
$007C78_H$	DLC register 12	DLCR12	R/W	$XXXXXXXX_B$
$007C79_H$				
$007C7A_H$	DLC register 13	DLCR13	R/W	$XXXXXXXX_B$
$007C7B_H$				
$007C7C_H$	DLC register 14	DLCR14	R/W	$XXXXXXXX_B$
$007C7D_H$				
$007C7E_H$	DLC register 15	DLCR15	R/W	$XXXXXXXX_B$
$007C7F_H$				

(Continued)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C80_H$ to $007C87_H$	Data register 0 (8 bytes)	DTR0	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C88_H$ to $007C8F_H$	Data register 1 (8 bytes)	DTR1	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C90_H$ to $007C97_H$	Data register 2 (8 bytes)	DTR2	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C98_H$ to $007C9F_H$	Data register 3 (8 bytes)	DTR3	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CA0_H$ to $007CA7_H$	Data register 4 (8 bytes)	DTR4	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CA8_H$ to $007CAF_H$	Data register 5 (8 bytes)	DTR5	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CB0_H$ to $007CB7_H$	Data register 6 (8 bytes)	DTR6	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CB8_H$ to $007CBF_H$	Data register 7 (8 bytes)	DTR7	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CC0_H$ to $007CC7_H$	Data register 8 (8 bytes)	DTR8	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CC8_H$ to $007CCF_H$	Data register 9 (8 bytes)	DTR9	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CD0_H$ to $007CD7_H$	Data register 10 (8 bytes)	DTR10	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CD8_H$ to $007CDF_H$	Data register 11 (8 bytes)	DTR11	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CE0_H$ to $007CE7_H$	Data register 12 (8 bytes)	DTR12	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CE8_H$ to $007CEF_H$	Data register 13 (8 bytes)	DTR13	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

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Address CAN1	Register	Abbreviation	Access	Initial Value
$007CF0_H$ to $007CF7_H$	Data register 14 (8 bytes)	DTR14	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CF8_H$ to $007CFF_H$	Data register 15 (8 bytes)	DTR15	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

12. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI^{2}OS corresponding	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	$FFFFDC_H$	—	—
INT9 instruction	N	—	#09	$FFFFD8_H$	—	—
Exception	N	—	#10	$FFFFD4_H$	—	—
Reserved	N	—	#11	$FFFFD0_H$	ICR00	$0000B0_H$
Reserved	N	—	#12	$FFFFCC_H$		
CAN 1 RX / Input Capture 6	Y1	—	#13	$FFFFC8_H$	ICR01	$0000B1_H$
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	$FFFFC4_H$		
I^2C	N	—	#15	$FFFFC0_H$	ICR02	$0000B2_H$
Reserved	N	—	#16	$FFFFBC_H$		
16-bit Reload Timer 0	Y1	0	#17	$FFFFB8_H$	ICR03	$0000B3_H$
16-bit Reload Timer 1	Y1	1	#18	$FFFFB4_H$		
16-bit Reload Timer 2	Y1	2	#19	$FFFFB0_H$	ICR04	$0000B4_H$
16-bit Reload Timer 3	Y1	—	#20	$FFFFAC_H$		
PPG 4/5	N	—	#21	$FFFFA8_H$	ICR05	$0000B5_H$
PPG 6/7	N	—	#22	$FFFFA4_H$		
PPG 8/9/C/D	N	—	#23	$FFFFA0_H$	ICR06	$0000B6_H$
PPG A/B/E/F	N	—	#24	$FFFF9C_H$		
Timebase Timer	N	—	#25	$FFFF98_H$	ICR07	$0000B7_H$
External Interrupt 8 to 11	Y1	3	#26	$FFFF94_H$		
Watch Timer	N	—	#27	$FFFF90_H$	ICR08	$0000B8_H$
External Interrupt 12 to 15	Y1	4	#28	$FFFF8C_H$		
A/D Converter	Y1	5	#29	$FFFF88_H$	ICR09	$0000B9_H$
Free-run Timer 0 / free-run Timer 1	N	—	#30	$FFFF84_H$		
Input Capture 4/5	Y1	6	#31	$FFFF80_H$	ICR10	$0000BA_H$
Output Compare 4/5	Y1	7	#32	$FFFF7C_H$		
Input Capture 0/1	Y1	8	#33	$FFFF78_H$	ICR11	$0000BB_H$
Output Compare 6/7	Y1	9	#34	$FFFF74_H$		
Reserved	N	10	#35	$FFFF70_H$	ICR12	$0000BC_H$
Reserved	N	11	#36	$FFFF6C_H$		
UART 3 RX	Y2	12	#37	$FFFF68_H$	ICR13	$0000BD_H$
UART 3 TX	Y1	13	#38	$FFFF64_H$		

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Interrupt cause	EI^{2}OS corresponding	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX	Y2	14	#39	$FFFF60_H$	ICR14	$0000BE_H$
UART 2 TX	Y1	15	#40	$FFFF5C_H$		
Flash Memory	N	—	#41	$FFFF58_H$	ICR15	$0000BF_H$
Delayed Interrupt	N	—	#42	$FFFF54_H$		

Y1 : Usable

Y2 : Usable, with EI^{2}OS stop function

N : Unusable

Notes : •The peripheral resources sharing the ICR register have the same interrupt level.
•When the peripheral resources sharing the ICR register use extended intelligent I/O service, only one can use EI^{2}OS at a time.
•When either of the two peripheral resources sharing the ICR register specifies EI^{2}OS, the other one cannot use interrupts.

13. Electrical Characteristics

13.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVRH	V_{SS} − 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$*2
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6.0	V	*3
Maximum Clamp Current	I_{CLAMP}	−4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	—	40	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level maximum overall output current	ΣI_{OL}	—	100	mA	*4
“L” level average overall output current	ΣI_{OLAV}	—	50	mA	*4
“H” level maximum output current	I_{OH}	—	−15	mA	*4
“H” level average output current	I_{OHAV}	—	−4	mA	*4
“H” level maximum overall output current	ΣI_{OH}	—	−100	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	−50	mA	*4
Power consumption	P_D	—	454	mW	
Operating temperature	T_A	−40	+105	°C	
		−40	+125	°C	*6
Storage temperature	T_{STG}	−55	+150	°C	

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*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

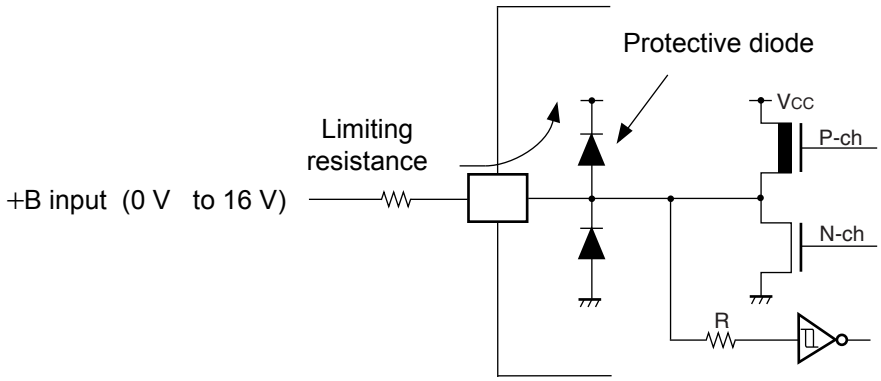
*3: V_I and V_O should not exceed $V_{CC} + 0.3$ V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56, P60 to P67

*5: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56 (for evaluation device : P50 to P55) , P60 to P67

- ″ Use within recommended operating conditions.
- ″ Use at DC voltage (current)
- ″ The +B signal should always be applied a connecting limit resistance between the +B signal and the microcontroller.
- ″ The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- ″ Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- ″ Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- ″ Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- ″ Care must be taken not to leave the +B input pin open.
- ″ Recommended circuit sample:

• Input/output equivalent circuits



*6 : If used exceeding $T_A = +105°C$, be sure to contact Cypress for reliability limitations.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

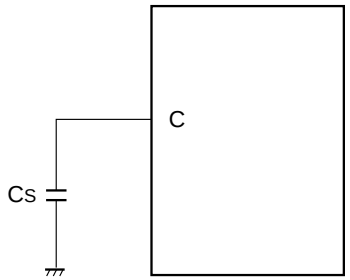
13.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	−40	—	+125	°C	*

* : If used exceeding T_A = +105°C, be sure to contact Cypress for reliability limitations.

″ C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

13.3 DC Characteristics

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50)
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	V_{CC} + 0.3	V	Pin inputs if TTL input levels are selected
	V_{IHS}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P12, P15, P50 inputs if CMOS input levels are selected
	V_{IHI}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P44, P45 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} − 0.3	—	V_{CC} + 0.3	V	MD input pin
"L" level input voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50)
	V_{ILA}	—	—	V_{SS} − 0.3	—	0.5 V_{CC}	V	Pin inputs if Automotive input levels are selected
	V_{ILT}	—	—	V_{SS} − 0.3	—	0.8	V	Pin inputs if TTL input levels are selected
	V_{ILS}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P12, P15, P50 inputs if CMOS input levels are selected
	V_{ILI}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P44, P45 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} − 0.3	—	V_{SS} + 0.3	V	MD input pin
Output "H" voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	V_{CC} − 0.5	—	—	V	
Output "H" voltage	V_{OHI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OH} = −3.0 mA	V_{CC} − 0.5	—	—	V	

(Continued)

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Sym-bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output “L” voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Output “L” voltage	V_{OLI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OL} = 3.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	− 1	—	+ 1	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P25, P30 to P37, $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Except Flash memory devices
Power supply current	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	48	60	mA	
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At writing Flash memory.	—	53	65	mA	Flash memory devices
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At erasing Flash memory.	—	58	70	mA	Flash memory devices
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At Sleep mode.	—	25	35	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, At Main Timer mode	—	0.3	0.8	mA	Devices without “T”-suffix
				—	0.4	1.0	mA	Devices with “T”-suffix
	I_{CTSPLL} [6]		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	

(Continued)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Sym-bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCL}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub clock operation T_A = +25°C	—	70	140	µA	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub clock operation T_A = +25°C	—	100	200	µA	MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation T_A = +25°C	—	100	200	µA	MB90356ES MB90F356ES MB90357ES MB90F357ES
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub clock operation T_A = +25°C	—	120	240	µA	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub clock operation T_A = +25°C	—	150	300	µA	MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation T_A = +25°C	—	150	300	µA	MB90356TES MB90F356TES MB90357TES MB90F357TES

(Continued)

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCLS}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub sleep T_A = +25°C	—	20	50	µA	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub sleep T_A = +25°C	—	60	200	µA	MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T_A = +25°C	—	60	200	µA	MB90356ES MB90F356ES MB90357ES MB90F357ES
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, At sub sleep T_A = +25°C	—	70	150	µA	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub sleep T_A = +25°C	—	110	300	µA	MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T_A = +25°C	—	110	300	µA	MB90356TES MB90F356TES MB90357TES MB90F357TES

(Continued)

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(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCT}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At watch mode T_A = +25°C	—	10	35	µA	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At watch mode T_A = +25°C	—	25	150	µA	MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At watch mode T_A = +25°C	—	25	150	µA	MB90356ES MB90F356ES MB90357ES MB90F357ES
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At watch mode T_A = +25°C	—	60	140	µA	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At watch mode T_A = +25°C	—	80	250	µA	MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At watch mode T_A = +25°C	—	80	250	µA	MB90356TES MB90F356TES MB90357TES MB90F357TES
	I_{CCH}		V_{CC} = 5.0 V, At stop mode, T_A = +25°C	—	7	25	µA	Devices without “T”-suffix
				—	60	130	µA	Devices with “T”-suffix
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, V_{CC}, V_{SS}	—	—	5	15	pF	

13.4 AC Characteristics

13.4.1 Clock Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	1/2 (at PLL stop) When using an oscillation circuit
			4	—	16	MHz	1 multiplied PLL When using an oscillation circuit
			4	—	12	MHz	2 multiplied PLL When using an oscillation circuit
			4	—	8	MHz	3 multiplied PLL When using an oscillation circuit
			4	—	6	MHz	4 multiplied PLL When using an oscillation circuit
			—	—	4	MHz	6 multiplied PLL When using an oscillation circuit
		X0	3	—	24	MHz	1/2 (at PLL stop), When using an external clock
			4	—	24	MHz	1 multiplied PLL When using an external clock
			4	—	12	MHz	2 multiplied PLL When using an external clock
			4	—	8	MHz	3 multiplied PLL When using an external clock
			4	—	6	MHz	4 multiplied PLL When using an external clock
			—	—	4	MHz	6 multiplied PLL When using an external clock
	fCL	X0A, X1A	—	32.768	100	kHz	When using sub clock
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0	41.67	—	333	ns	When using an external clock
	tCYLL	X0A, X1A	10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio should be about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock

(Continued)

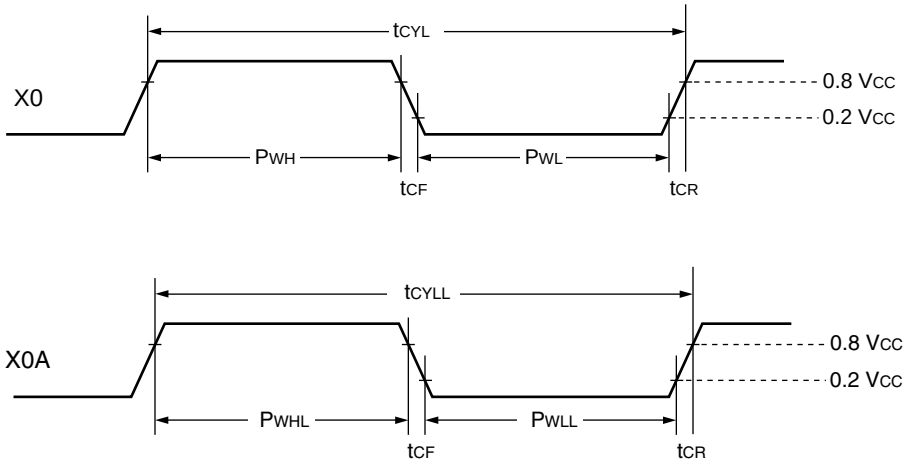
(Continued)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

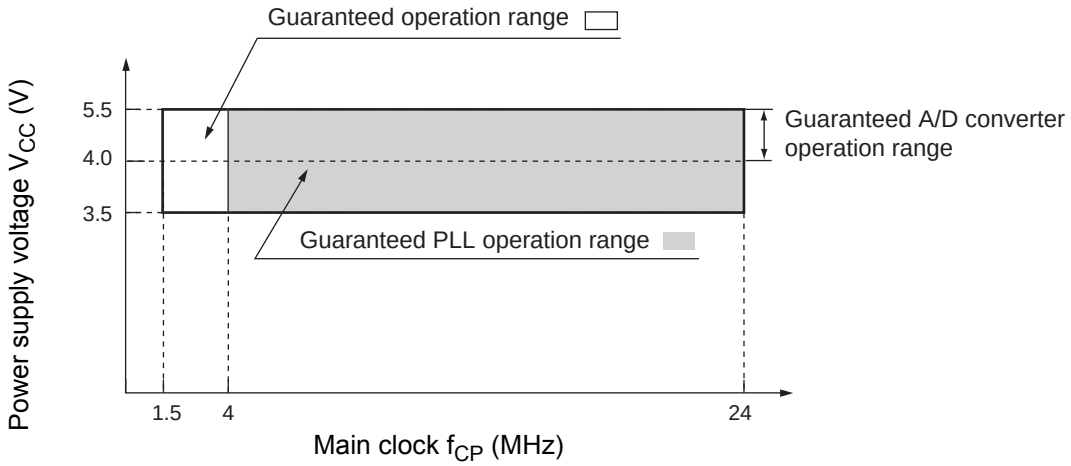
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

*: The limitation is in the range of the clock frequency when PLL is used. Use within the range in graph of "· PLL guaranteed operation range External clock frequency and internal operation clock frequency".

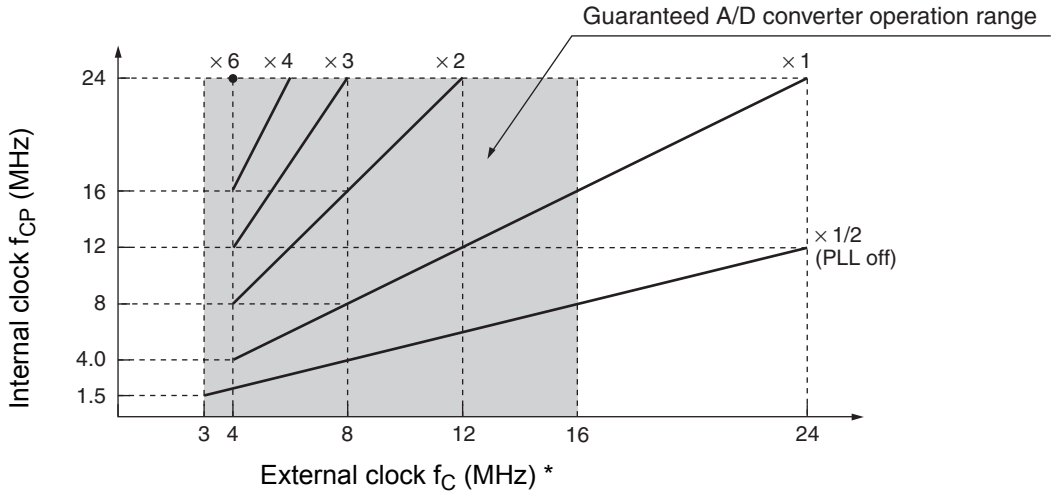
- Clock Timing



• PLL guaranteed operation range



Guaranteed operation range of MB90350E series



* : When using crystal oscillator or ceramic oscillator, the maximum clock frequency is 16 MHz.

External clock frequency and internal operation clock frequency

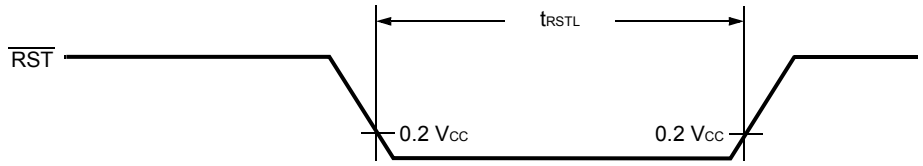
13.4.2 Reset Standby Input

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

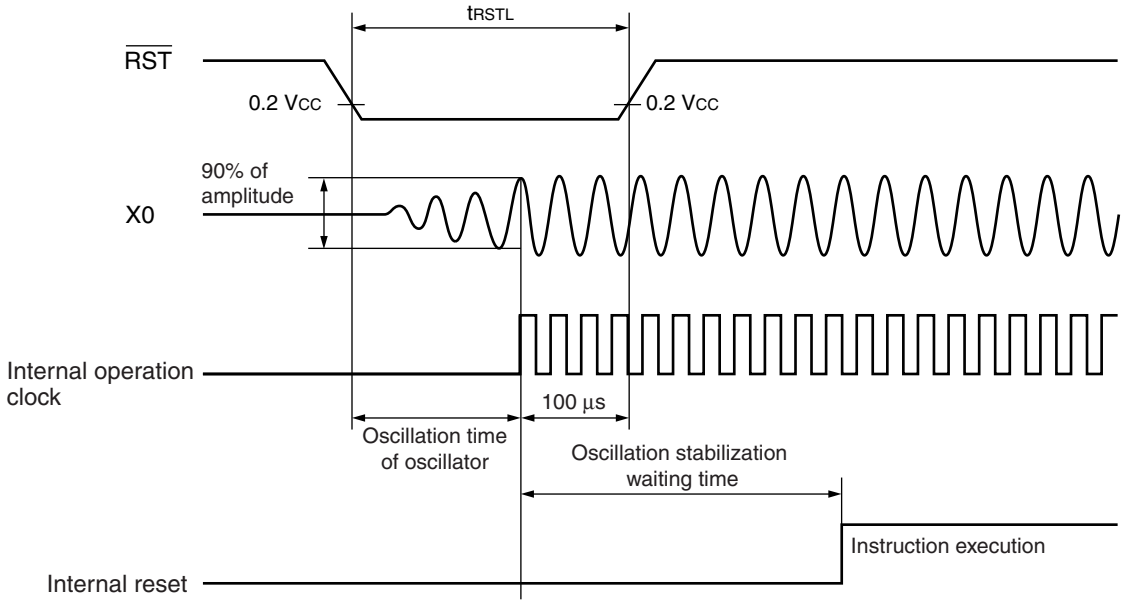
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	–	ns	Under normal operation
			Oscillation time of oscillator* + 100 µs	–	µs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	–	µs	In Main timer mode and PLL timer mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillators, the oscillation time is between hundreds of μs to several ms. With an external clock, the oscillation time is 0 ms.

Under normal operation:



In Stop mode, Sub Clock mode, Sub Sleep mode and, Watch mode:

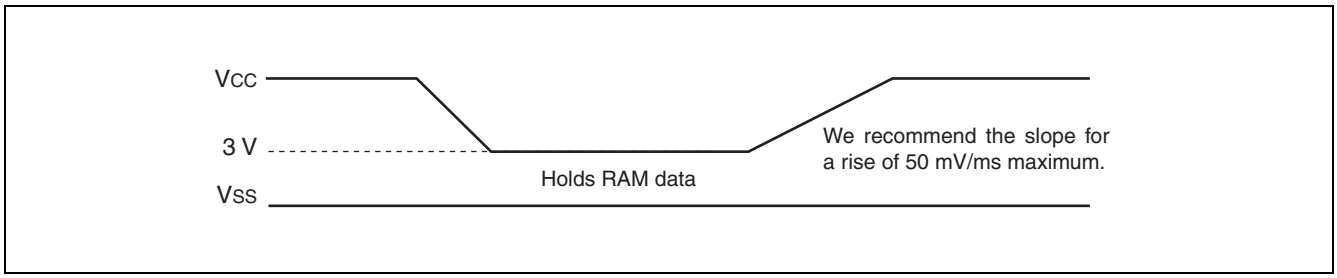


13.4.3 Power On Reset

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Waiting time until power-on

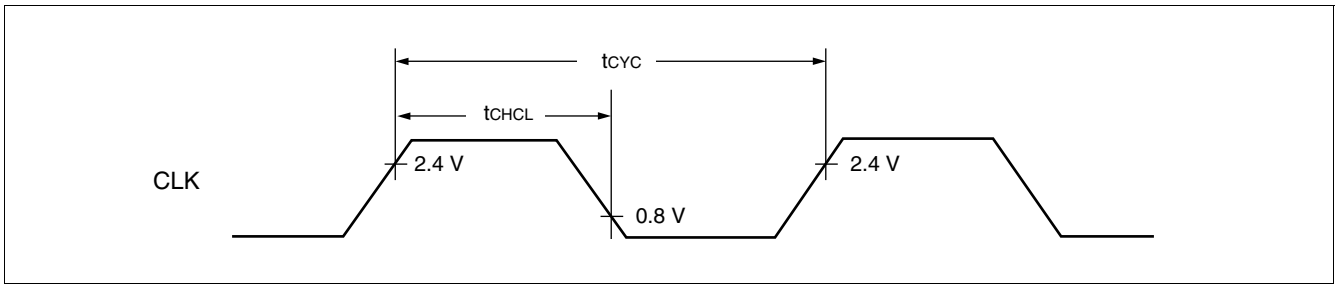
Note : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within
1 V/s, you can operate while using the PLL clock.



13.4.4 Clock Output Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	f_{CP} = 16 MHz
				41.67	—	ns	f_{CP} = 24 MHz
CLK↑ →CLK ↓	t_{CHCL}	CLK	—	20	—	ns	f_{CP} = 16 MHz
				13	—	ns	f_{CP} = 24 MHz

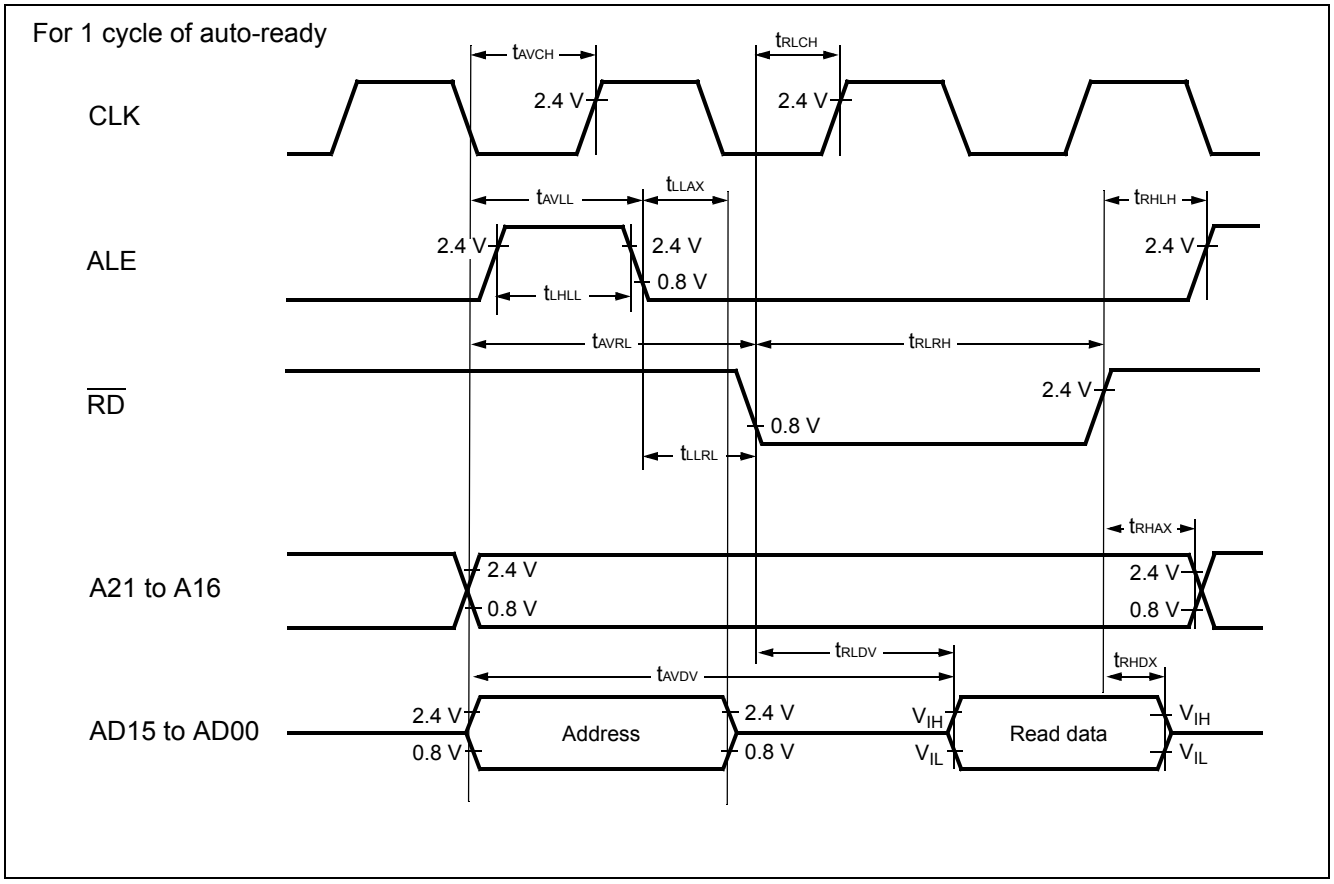


13.4.5 Bus Timing (Read)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, $f_{CP} \leq$ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE	–	$t_{CP}/2 - 10$	–	ns
Valid address → ALE ↓ time	t_{AVLL}	ALE, A21 to A16, AD15 to AD00		$t_{CP}/2 - 20$	–	ns
ALE ↓ → Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	–	ns
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	A21 to A16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	–	ns
Valid address → Valid data input	t_{AVDV}	A21 to A16, AD15 to AD00		–	$5\ t_{CP}/2 - 60$	ns
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$(n^*+3/2)\ t_{CP} - 20$	–	ns
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		–	$(n^*+3/2)\ t_{CP} - 50$	ns
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	–	ns
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	–	ns
$\overline{RD}$ ↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A21 to A16		$t_{CP}/2 - 10$	–	ns
Valid address → CLK ↑ time	t_{AVCH}	A21 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	–	ns
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 15$	–	ns
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	–	ns

* : Number of ready cycles

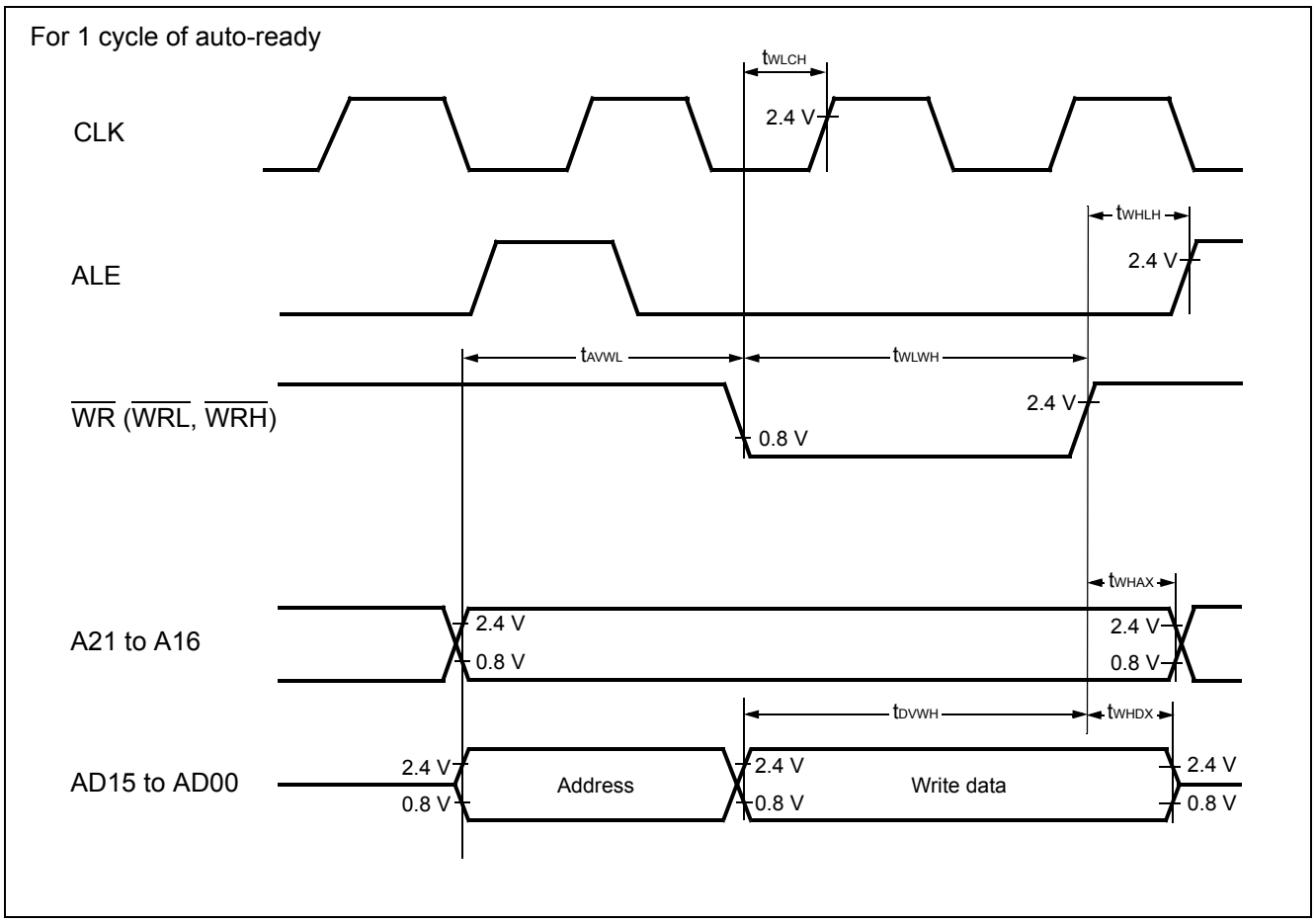

For 1 cycle of auto-ready
CLK
ALE
RD
A21 to A16
AD15 to AD00
tAVCH
tRLCH
2.4 V
tAVLL
tLLAX
tRHLH
0.8 V
tLHLL
tAVRL
tRLRH
tLLRL
tRHAX
tRLDV
tAVDV
tRHDX
Address
Read data
VIH
VIL

13.4.6 Bus Timing (Write)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A21 to A16, AD15 to AD00, $\overline{WR}$	—	t_{CP}–15	—	ns
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		(n*+3/2)t_{CP} – 20	—	ns
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		(n*+3/2)t_{CP} – 20	—	ns
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	—	ns
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A21 to A16, $\overline{WR}$		t_{CP}/2 – 10	—	ns
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	—	ns
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 15	—	ns

* : Number of ready cycles

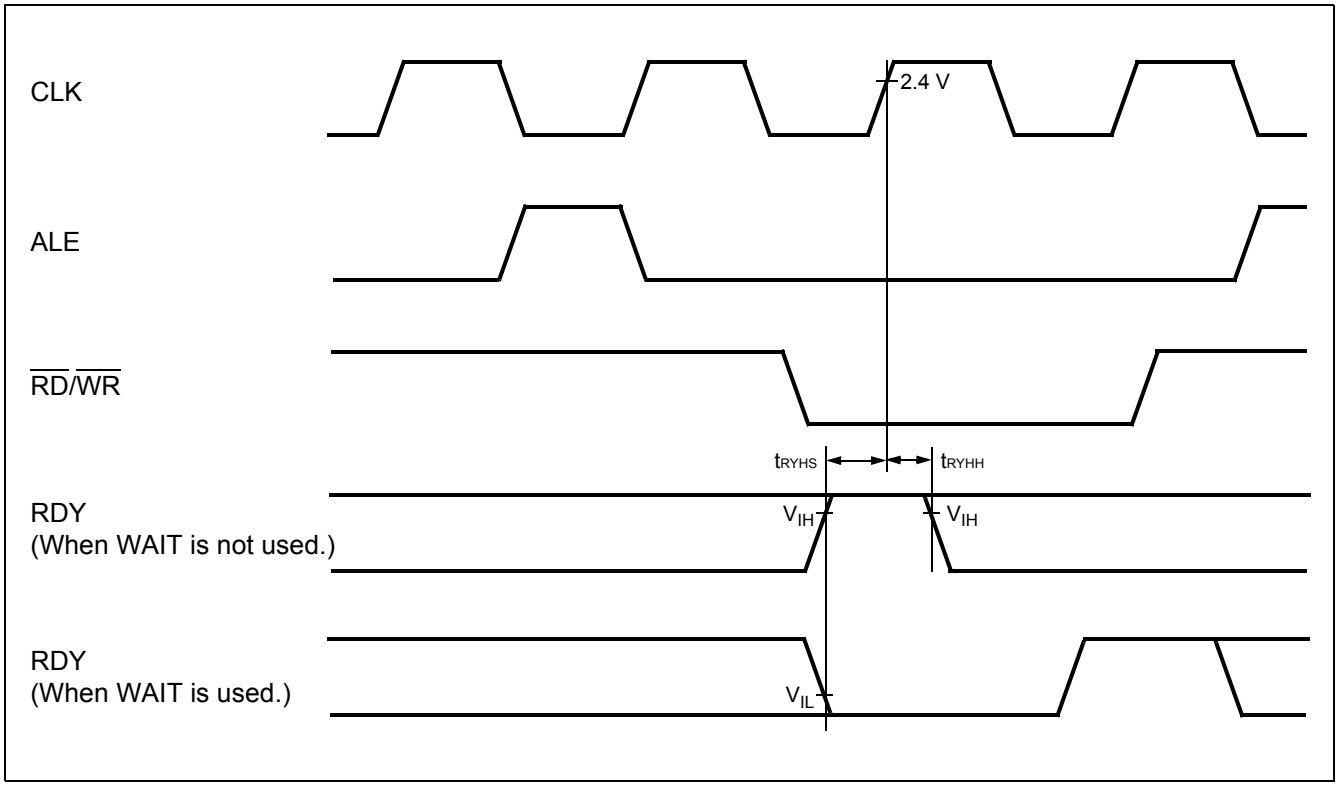


13.4.7 Ready Input Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
RDY set-up time	t_{RYHS}	RDY	—	45	—	ns	f_{CP} = 16 MHz
				32	—	ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY set-up time is insufficient, use the auto-ready function.

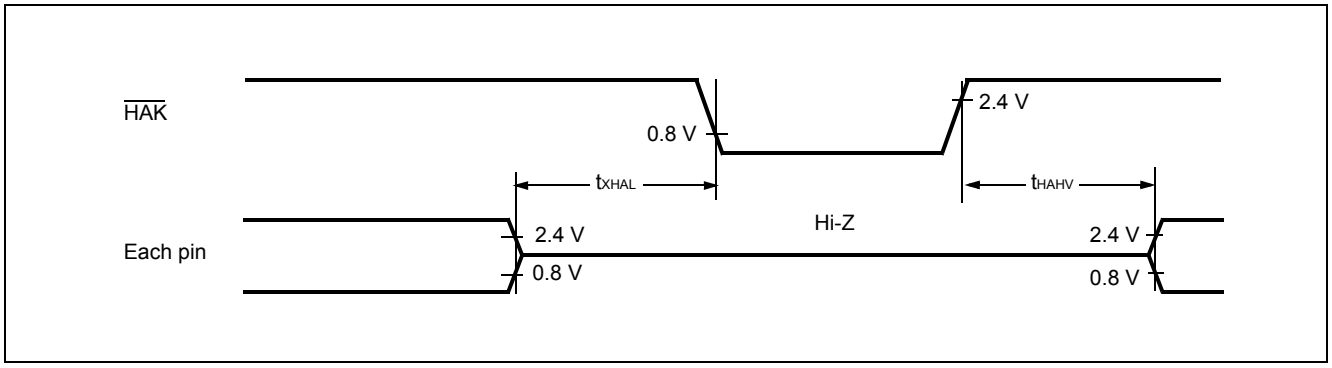


13.4.8 Hold Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units
				Min	Max	
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	–	30	t_{CP}	ns
$\overline{HAK}$ ↑ time → Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns

Note : There is more than 1 machine cycle from when HRQ pin reads in until the $\overline{HAK}$ is changed.



13.4.9 LIN-UART2/3

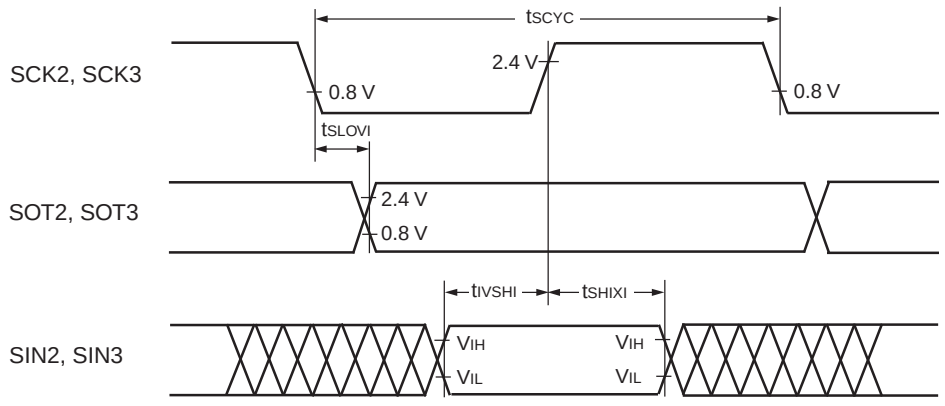
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

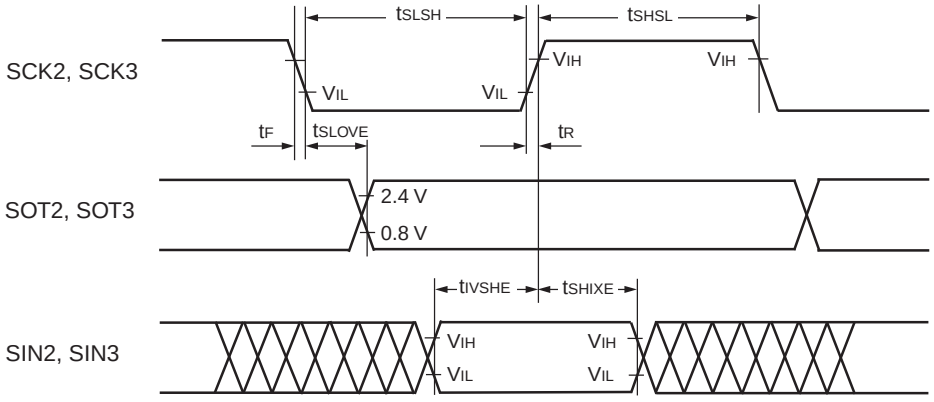
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal shift clock mode output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2, SCK3 SOT2, SOT3		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCK2, SCK3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCK2, SCK3		t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK2, SCK3 SOT2, SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK2, SCK3 SIN2, SIN3		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK2, SCK3		—	10	ns
SCK rise time	t_R	SCK2, SCK3		—	10	ns

Notes :
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

″ Internal Shift Clock Mode



●External Shift Clock Mode



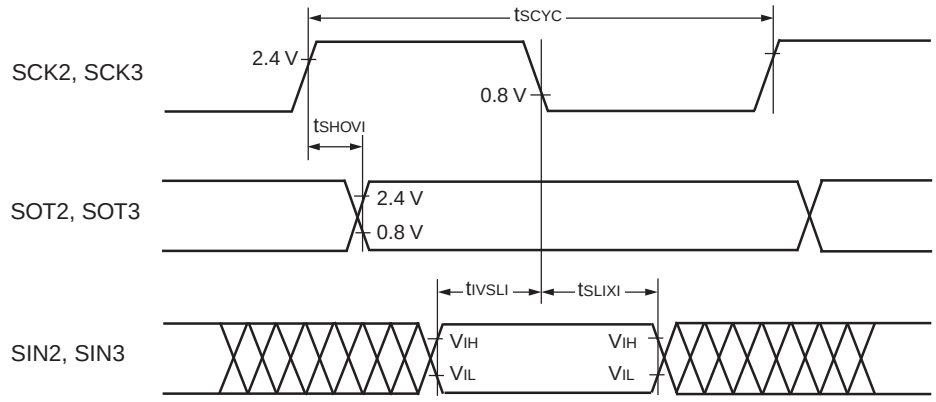
■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

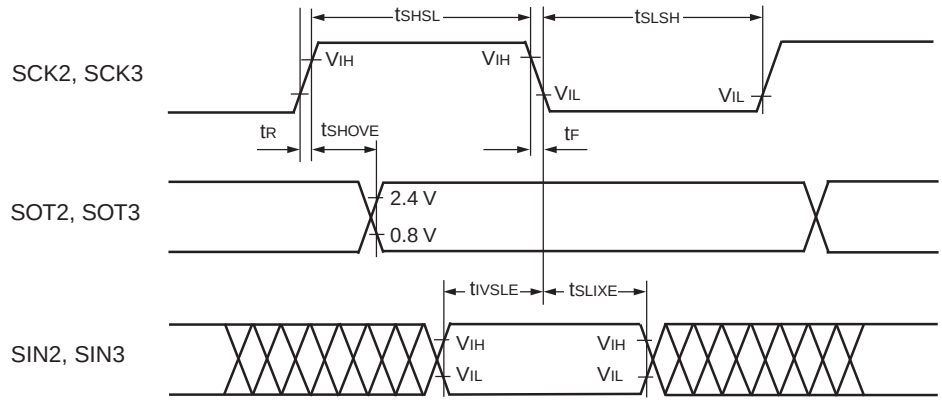
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal shift clock mode output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	–	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2, SCK3 SOT2, SOT3		−50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	–	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK2, SCK3 SIN2, SIN3		0	–	ns
Serial clock “H” pulse width	t_{SHSL}	SCK2, SCK3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	3 t_{CP} - t_R	–	ns
Serial clock “L” pulse width	t_{SLSH}	SCK2, SCK3		t_{CP} + 10	–	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK2, SCK3 SOT2, SOT3		–	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK2, SCK3 SIN2, SIN3		30	–	ns
SCK ↓ → Valid SIN hold time	t_{SLIXE}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 30	–	ns
SCK fall time	t_F	SCK2, SCK3		–	10	ns
SCK rise time	t_R	SCK2, SCK3		–	10	ns

Notes :
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

• Internal Shift Clock Mode



• External Shift Clock Mode

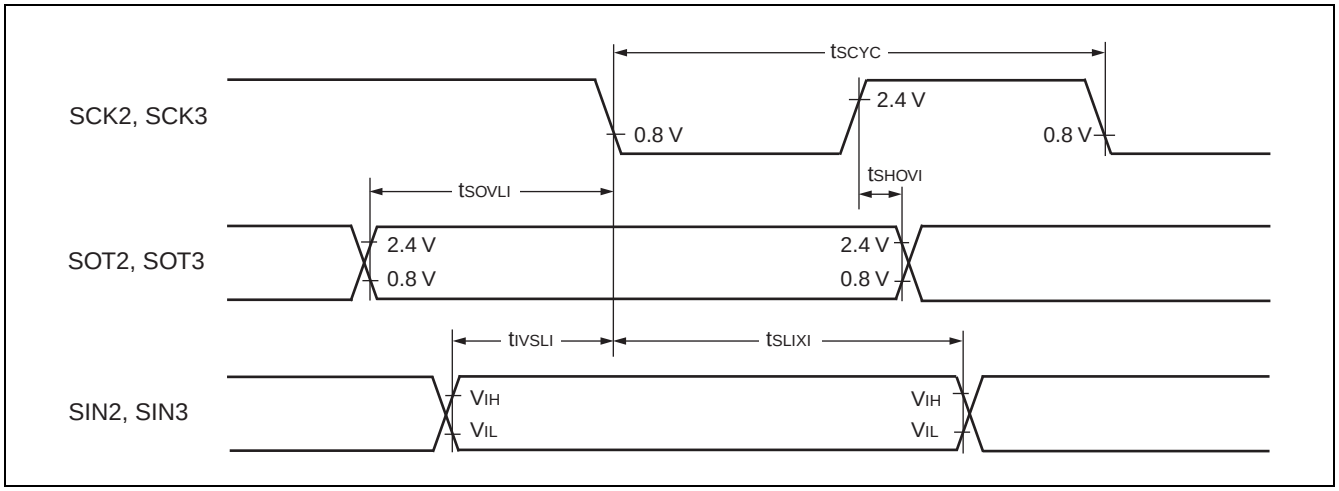


■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal clock operation output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2, SCK3 SOT2, SOT3		–50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK2, SCK3 SOT2, SOT3		3 t_{CP} – 70	—	ns

Notes : • C_L is load capacity value of pins when testing.
• t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.



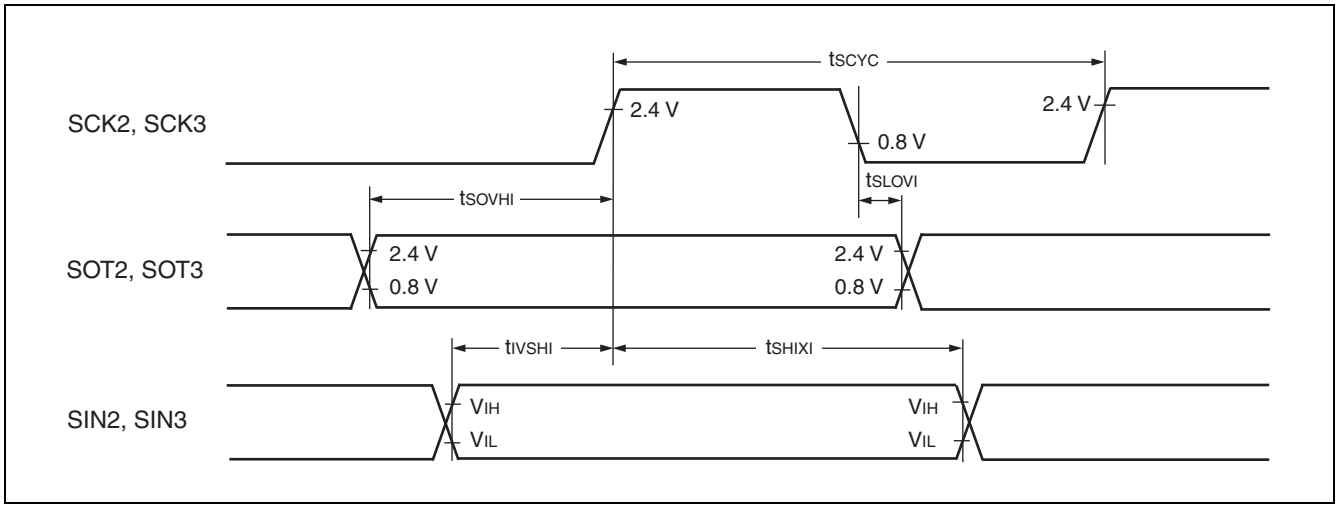
■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal clock operation output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2, SCK3 SOT2, SOT3		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK2, SCK3 SOT2, SOT3		3 t_{CP} – 70	—	ns

Notes : • C_L is load capacity value of pins when testing.

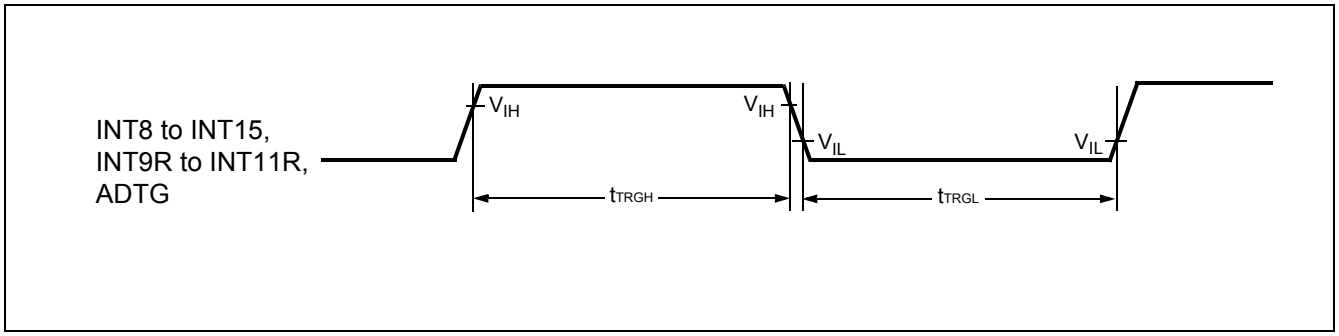
•t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.



13.4.10 Trigger Input Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

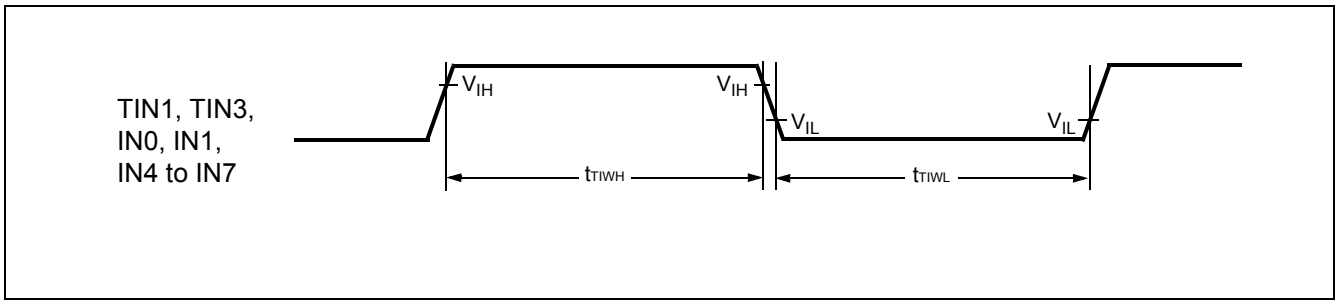
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	5 t_{CP}	—	ns



13.4.11 Timer Related Resource Input Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

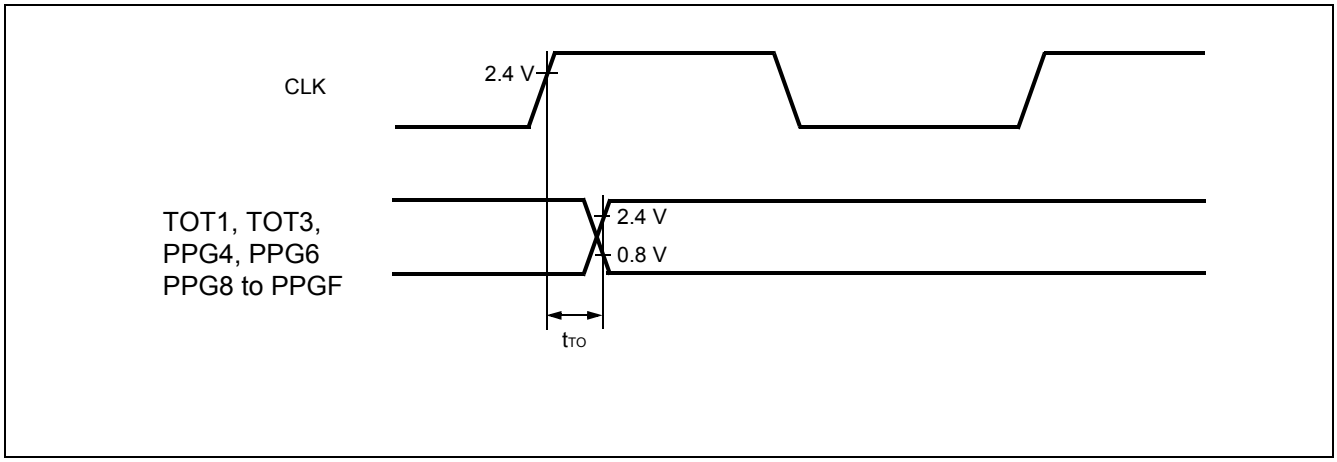
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN1, TIN3,IN0, IN1, IN4 to IN7	—	4 t_{CP}	—	ns



13.4.12 Timer Related Resource Output Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT1, TOT3, PPG4, PPG6, PPG8 to PPGF	—	30	—	ns



13.4.13 I^2C Timing

(T_A = −40°C to +125°C, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time for (repeated) START condition SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250*5	—	100*5	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

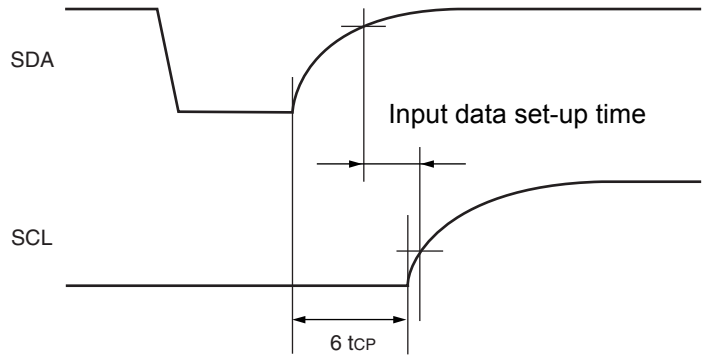
*2 : The maximum t_{HDDAT} has to meet at least that the device does not exceed the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I^2C -bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

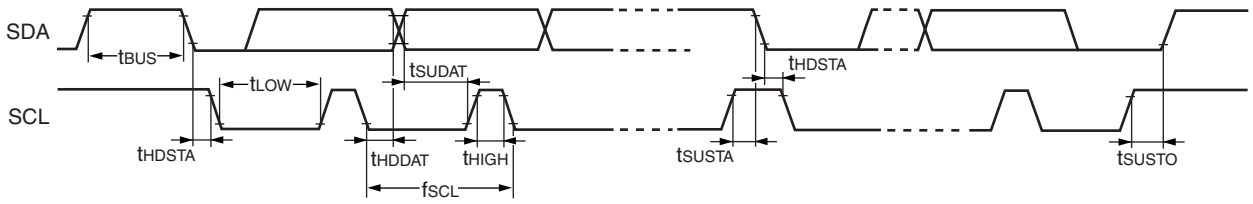
*5 : Refer to "• Note of SDA, SCL set-up time".

• Note of SDA, SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

• Timing definition



13.5 A/D Converter

(T_A = −40°C to +125°C, 3.0 V ≤ AVRH, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN14	AV_{SS} − 1.5×LSB	AV_{SS} + 0.5×LSB	AV_{SS} + 2.5×LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN14	AVRH − 3.5×LSB	AVRH − 1.5×LSB	AVRH + 0.5×LSB	V	
Compare time	—	—	1.0	—	16500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			2.0				4.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	×	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			1.2				4.0 V ≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN14	− 0.3	—	+ 0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN14	AV_{SS}	—	AVRH	V	
Reference voltage range	—	AVRH	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between channels	—	AN0 to AN14	—	—	4	LSB	

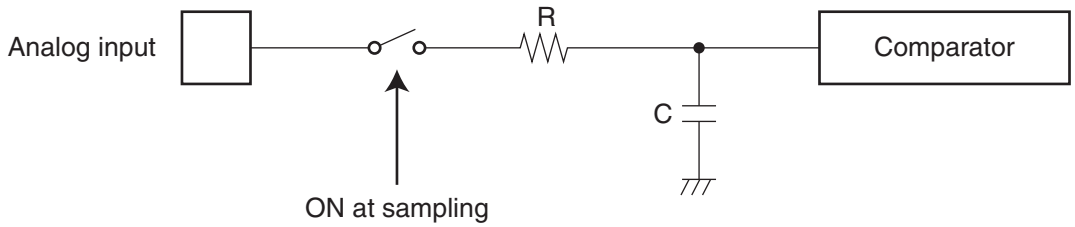
* : If A/D converter is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Notes on A/D Converter Section

■ About the external impedance of the analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting
A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

· Analog input equivalence circuit



MB90F351E(S),MB90F351TE(S),MB90F352E(S),MB90F352TE(S),
MB90F356E(S),MB90F356TE(S),MB90F357E(S),MB90F357TE(S)

	R	C
4.5 V ≤ AV_{CC} ≤ 5.5 V	2.0 kΩ (Max)	16.0 pF (Max)
4.0 V ≤ AV_{CC} ≤ 4.5 V	8.2 kΩ (Max)	16.0 pF (Max)

MB90351E(S),MB90351TE(S),MB90352E(S),MB90352TE(S),
MB90356E(S),MB90356TE(S),MB90357E(S),MB90357TE(S),
MB90V340E-101/102/103/104

	R	C
4.5 V ≤ AV_{CC} ≤ 5.5 V	2.0 kΩ (Max)	14.4 pF (Max)
4.0 V ≤ AV_{CC} ≤ 4.5 V	8.2 kΩ (Max)	14.4 pF (Max)

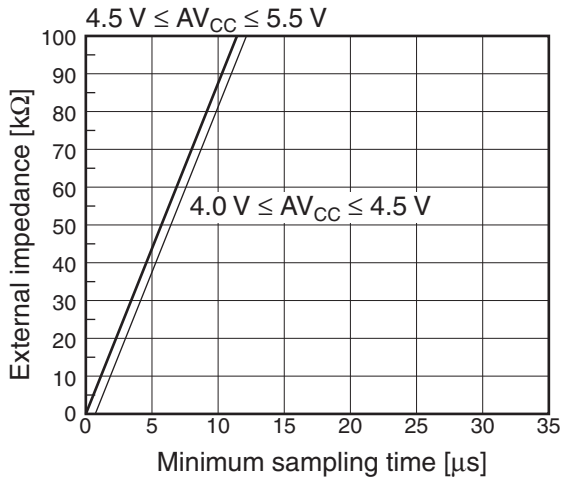
Note : The value is reference value.

■ Flash memory device

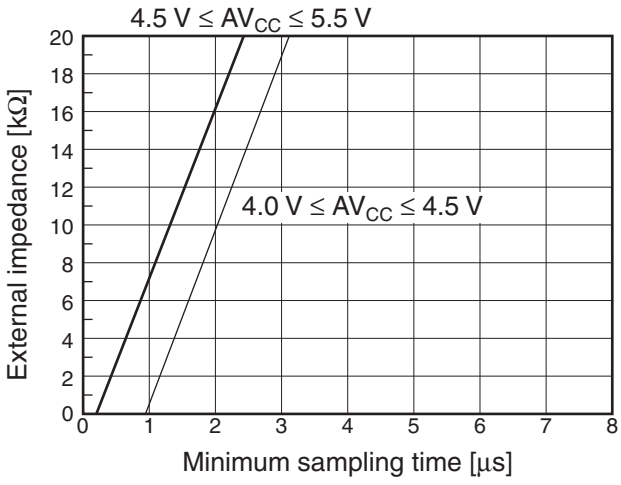
· Relation between External impedance and minimum sampling time

(MB90F351E(S),MB90F351TE(S),MB90F352E(S),MB90F352TE(S),
MB90F356E(S),MB90F356TE(S),MB90F357E(S),MB90F357TE(S))

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]

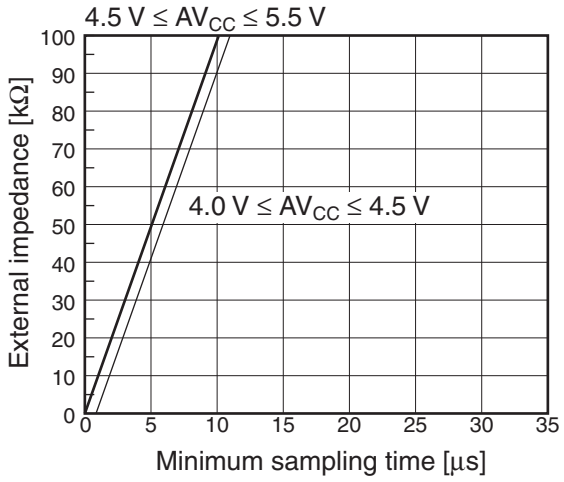


■ MASK ROM device

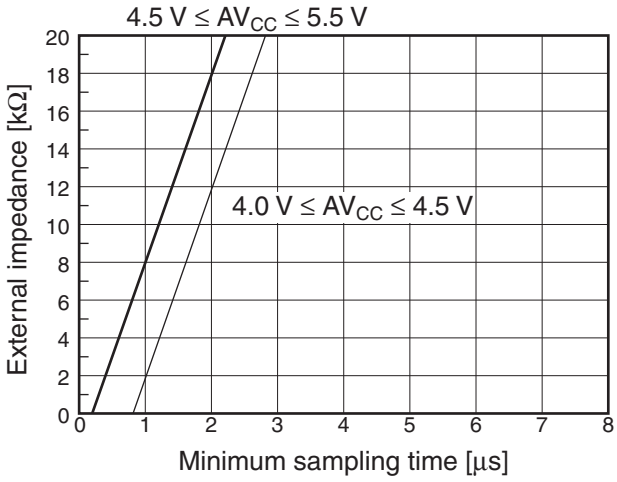
· Relation between External impedance and minimum sampling time

(MB90351E(S),MB90351TE(S),MB90352E(S),MB90352TE(S),MB90356E(S), MB90356TE(S),MB90357E(S),MB90357TE(S),MB90V340E-101/102/103/104)

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20kΩ]

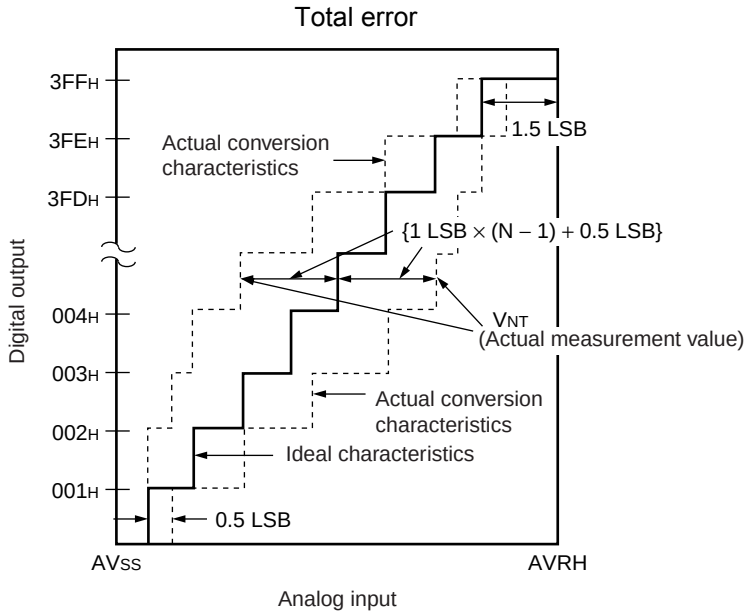


■ About the error

Values of relative errors grow larger, as |AVRH − AV_{SS}| becomes smaller.

13.6 Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by an A/D converter.
Non linearity error	:	Deviation between a line across zero-transition line (“00 0000 0000” ← → “00 0000 0001”) and full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) and actual conversion characteristics.
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	:	Difference between an actual value and a theoretical value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{AVRH - AV_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

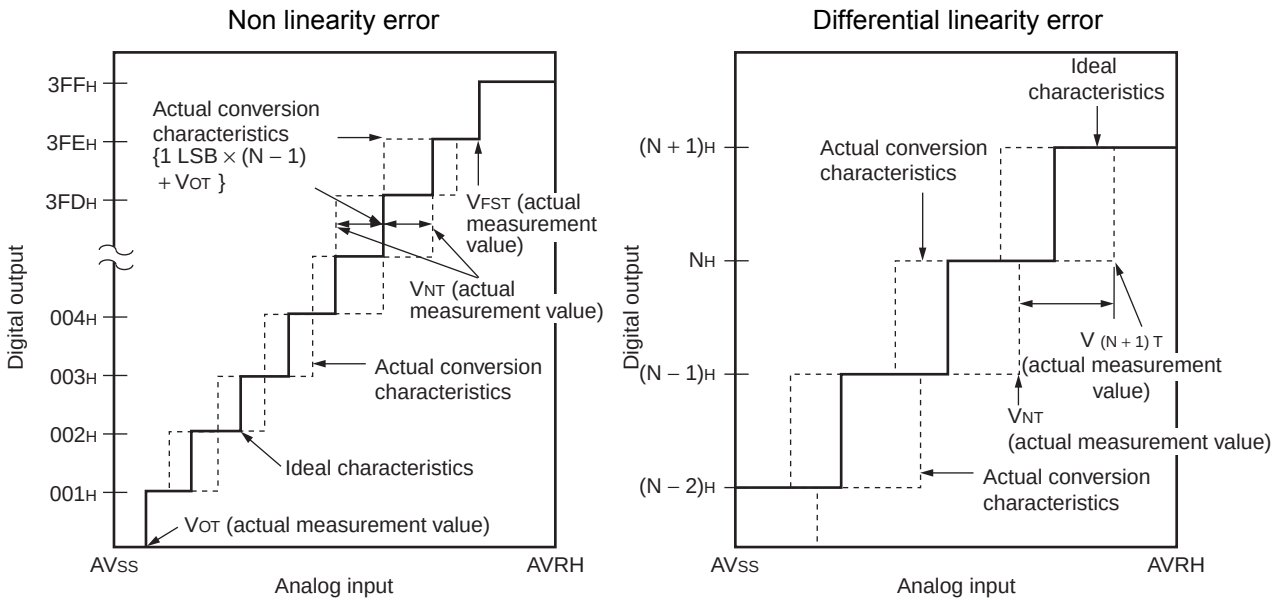
V_{OT} (Ideal value) $= AV_{SS} + 0.5$ LSB [V]

V_{FST} (Ideal value) $= AVRH - 1.5$ LSB [V]

V_{NT} : A voltage at which digital output transits from $(N - 1)_H$ to N_H.

(Continued)

(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H".
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$".

13.7 Flash Memory Program/Erase Characteristics

■ Dual Operation Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T_A = +25°C V_{CC} = 5.0 V	—	0.2	0.5	s	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	64	3600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10000	—	—	cycle	

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Flash memory Data Retention Time	Average T_A = +85°C	20	—	—	year	*

* : Corresponding value comes from the technology reliability evaluation result.
(Using Arrhenius equation to translate high temperature measurements test result into normalized value at +85°C)

14. Ordering Information

Part number	Package	Remarks
MB90F351EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	Flash memory products (64 Kbytes)
MB90F351ESPMC		
MB90F351TEPMC		
MB90F351TESPMC		
MB90F356EPMC		
MB90F356ESPMC		
MB90F356TEPMC		
MB90F356TESPMC		
MB90F352EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ESPMC		
MB90F352TEPMC		
MB90F352TESPMC		
MB90F357EPMC		
MB90F357ESPMC		
MB90F357TEPMC		
MB90F357TESPMC		
MB90351EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	MASK ROM products (64 Kbytes)
MB90351ESPMC		
MB90351TEPMC		
MB90351TESPMC		
MB90356EPMC		
MB90356ESPMC		
MB90356TEPMC		
MB90356TESPMC		
MB90352EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	MASK ROM products (128 Kbytes)
MB90352ESPMC		
MB90352TEPMC		
MB90352TESPMC		
MB90357EPMC		
MB90357ESPMC		
MB90357TEPMC		
MB90357TESPMC		

(Continued)

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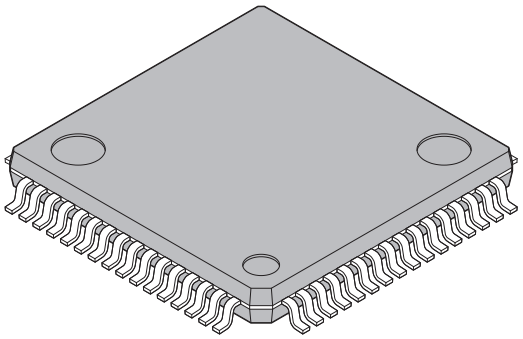
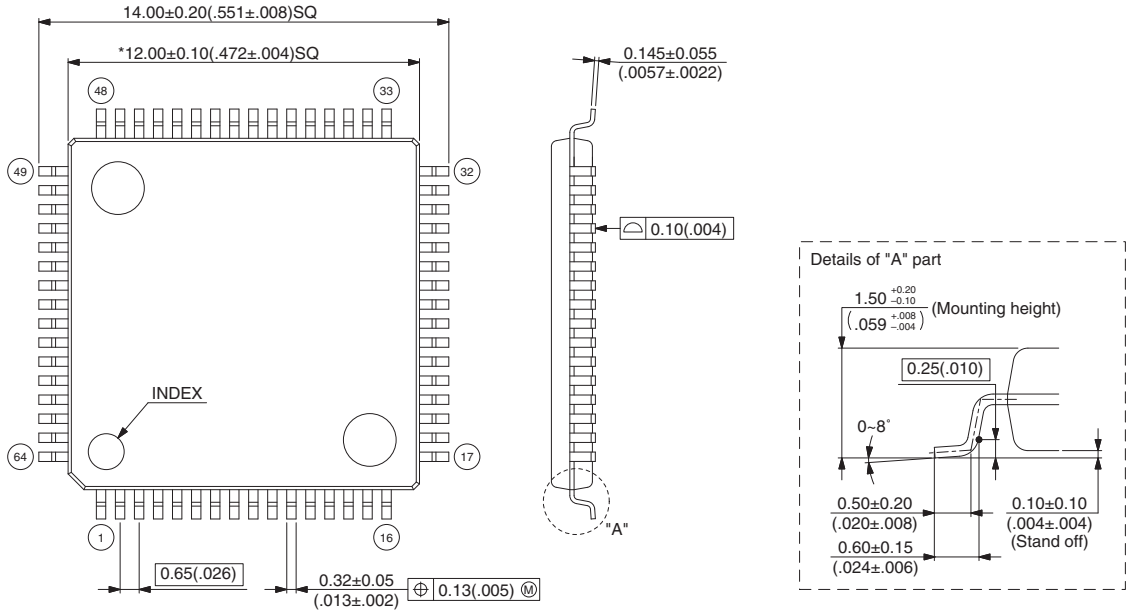
Part number	Package	Remarks
MB90F351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	Flash memory products (64 Kbytes)
MB90F351ESPMC1		
MB90F351TEPMC1		
MB90F351TESPMC1		
MB90F356EPMC1		
MB90F356ESPMC1		
MB90F356TEPMC1		
MB90F356TESPMC1		
MB90F352EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ESPMC1		
MB90F352TEPMC1		
MB90F352TESPMC1		
MB90F357EPMC1		
MB90F357ESPMC1		
MB90F357TEPMC1		
MB90F357TESPMC1		
MB90351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	MASK ROM products (64 Kbytes)
MB90351ESPMC1		
MB90351TEPMC1		
MB90351TESPMC1		
MB90356EPMC1		
MB90356ESPMC1		
MB90356TEPMC1		
MB90356TESPMC1		
MB90352EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	MASK ROM products (128 Kbytes)
MB90352ESPMC1		
MB90352TEPMC1		
MB90352TESPMC1		
MB90357EPMC1		
MB90357ESPMC1		
MB90357TEPMC1		
MB90357TESPMC1		
MB90V340E-101CR	299-pin ceramic PGA PGA-299C-A01	Device for evaluation
MB90V340E-102CR		
MB90V340E-103CR		
MB90V340E-104CR		

14.1 Package Dimensions

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65
(FPT-64P-M23)		

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values

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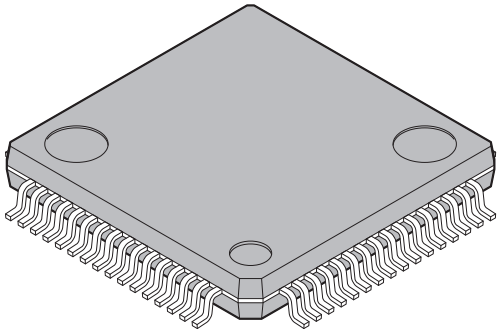
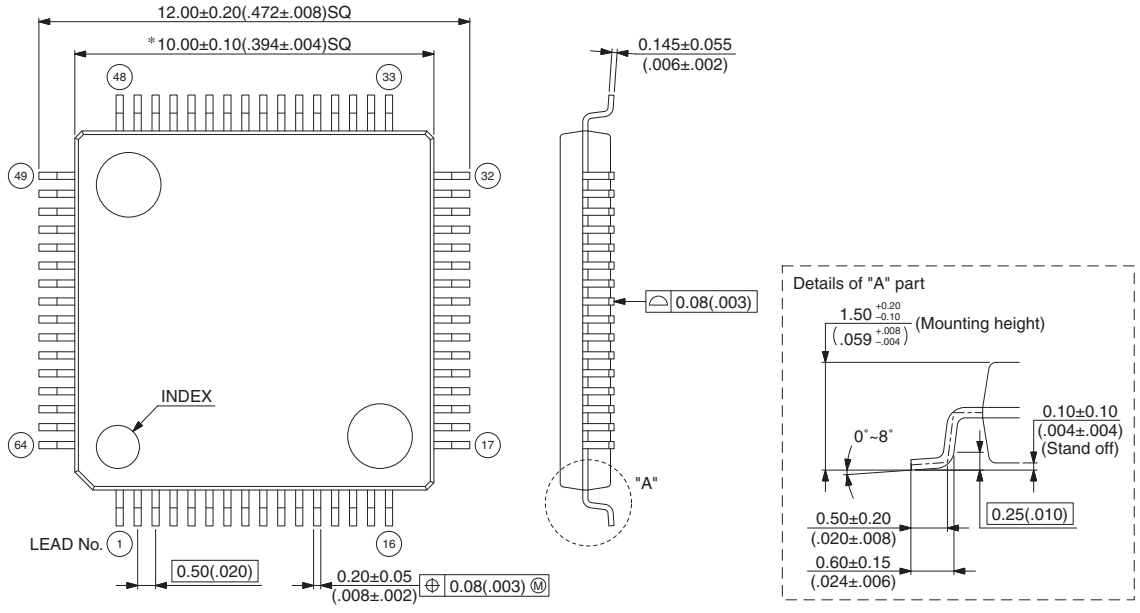
64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-64P-M24)	Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values

15. Major Changes

Page	Section	Change Results
—	—	The following names are changed. UART → LIN-UART 16-bit I/O timer → 16-bit free-run timer
26	Handling Devices	Added the section ”13. Serial Communication”.
51	Electrical Characteristics Absolute Maximum Ratings	Changed the maximum value of power consumption.
63	Electrical Characteristics AC Characteristics	Changed the "(4) Clock Output Timing". Changed the Minimum value of cycle time. (41.76 → 41.67)
69 to 73		Changed the notation of “(9) LIN-UART”.
78	A/D Converter	Changed the notation of “Zero reading voltage” and “full scale reading voltage”.
85	Ordering Information	Changed the part number; MB90V340E-101 → MB90V340E-101CR MB90V340E-102 → MB90V340E-102CR MB90V340E-103 → MB90V340E-103CR MB90V340E-104 → MB90V340E-104CR

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90350E Series F^{2}MC-16LX 16-bit Microcontrollers Document Number: 002-04493				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	10/12/2006	Migrated to Cypress and assigned document number 002-04993. No change to document contents or format.
*A	5193077	AKIH	04/07/2016	Updated to Cypress template

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