THE DATASHEET OF

IMC301AF048XUMA1

IMC300 - iMOTION™ motor controller

High-performance motor control IC with additional microcontroller

IMC300

Features

- Motion Control Engine (MCE) as a ready-to-use control solution for variable speed drives
- Integrated script engine for application control customization
- Integrated drive and system protection features
- Field oriented control (FOC) for permanent magnet synchronous motor (PMSM)
- Flexible space vector PWM for sinusoidal voltage control
- Current sensing via single or leg shunt
- Sensorless operation
- Hall sensor operation using analog or digital Hall
- Integrated analog comparators for over-current protection
- Built-in temperature sensor
- Power factor correction (PFC) control (optional)
- Flexible control input options: UART, Frequency, duty cycle or analog signal
- Certified drive safety functions according to IEC/UL 60730-1 ‘Class B’

CPU subsystem

- High-performance 32-bit ARM® Cortex®-M0 core
- Single-cycle 32-bit hardware multiplier
- 96 MHz MATH co-processor (MATH), consisting of a CORDIC unit for trigonometric calculation and a hardware divider unit
- Nested vectored interrupt controller (NVIC)
- Event request unit (ERU) for programmable processing of external and internal service requests
- System timer (SysTick) for operating system support
- Factory trimmed 48/96 MHz internal clock
- Independent internal clock for window watchdog (WDT) and real time clock (RTC)
- Low-power standby function
- Serial wire debug (SWD) or single pin debug (SPD)

On-chip memories

- 128 kbytes on-chip flash with ECC and prefetch
- 16 kbytes SRAM with parity

Communication peripherals

- Universal serial interface channels (USIC), usable as UART, SPI and I2C interfaces
- MultiCAN+, Full-CAN/Basic-CAN with 2 nodes, 32 message objects (up to 1 MBaud)

Analog frontend peripherals

- ADC with 12-bit resolution, 1MSPS, 2 sample and hold stages and multiple input
- Adjustable gain on ADC inputs
- Up to 6 channels of out of range comparators (ORC)
- Up to 3 fast analog comparators (ACMP)
- Internal temperature sensor (TSE)

Control peripherals

- Capture/compare units 4 (CCU4) for use as general purpose timers
- Capture/compare units 8 (CCU8) for motor control and power conversion
- Position interfaces (POSIF) for hall sensors
- Window watchdog timer (WDT) for safety sensitive applications
- Real time clock module with alarm support (RTC)
- Pseudo random number generator (PRNG), provides random data with fast generation times

Potential applications

- Small and major home appliances
- Fans, Pumps, Compressors
- General purpose variable speed drives

Product validation

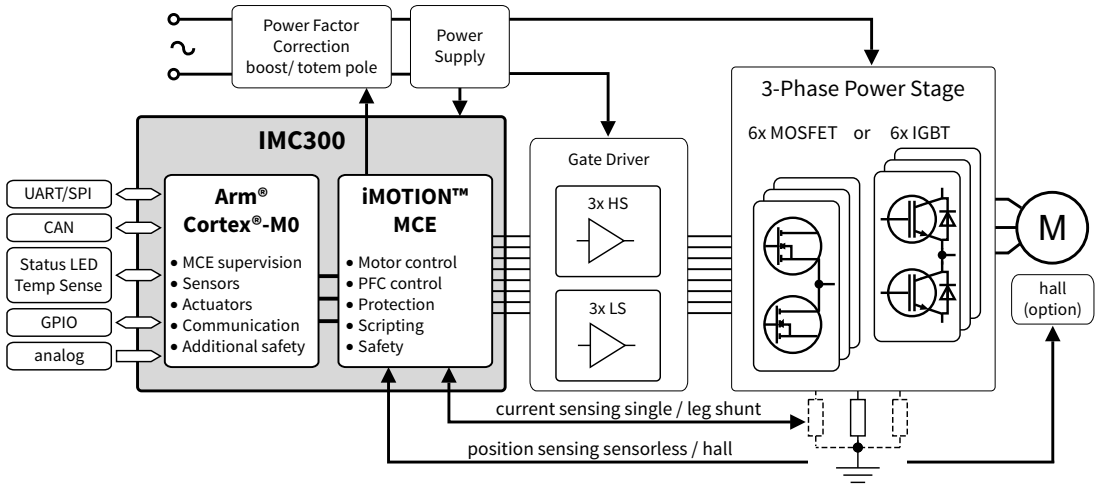
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

iMOTION™ IMC300 is a family of highly integrated ICs for the control of variable speed drives with an additional integrated microcontroller. By integrating both the required hardware and software to perform control of a permanent magnet synchronous motor (PMSM) they provide the shortest time to market for any motor system at the lowest system and development cost.

The motor controller uses the Motion Control Engine (MCE) to create a ready-to-use solution to perform control of a permanent magnet synchronous motor (PMSM) providing the shortest time to market for any motor system at the lowest system and development cost. The integrated script engine allows to add application flexibility without interfering with the motor control algorithm.

The integrated microcontroller is based on an ARM® Cortex® M0 core and runs independently from the MCE.



Ordering information

Product Type	Application	Package
IMC301A-F048	single motor	LQFP-48
IMC301A-F064		LQFP-64
IMC302A-F048	single motor + PFC (boost, totem pole)	LQFP-48
IMC302A-F064		LQFP-64

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1 Block diagram reference

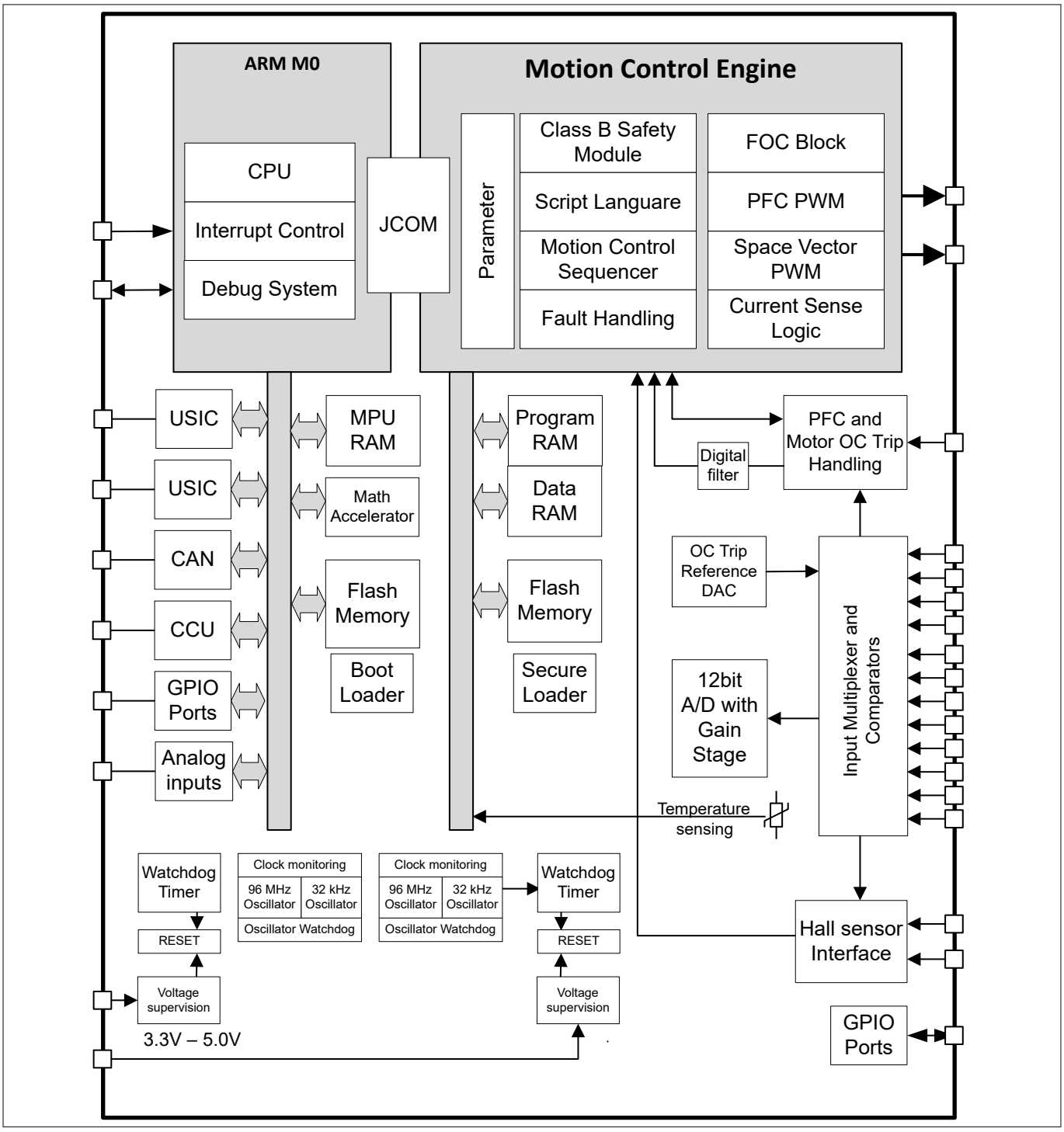

Figure 1 Block diagram reference

2 Pin configuration

2.1 Pin types and pad structure

The pin type is specified as follows:

- P - power
- I - digital input
- O - digital output
- IO – digital input or output
- AIN - analog input
- AO - analog output

Figure 2 shows the pad structure and pin function control configuration for the input and output pins of the controller integrated.

The pin function, type and pull up/pull down circuit configuration are all controlled by the Motion Control Engine. Digital input, output or analog input signals that are not assigned to MCE functions can be assigned to the script engine.

The pin function, type and pull up/pull down circuit configuration are controlled via the respective configuration registers. Details are given in the hardware reference manual.

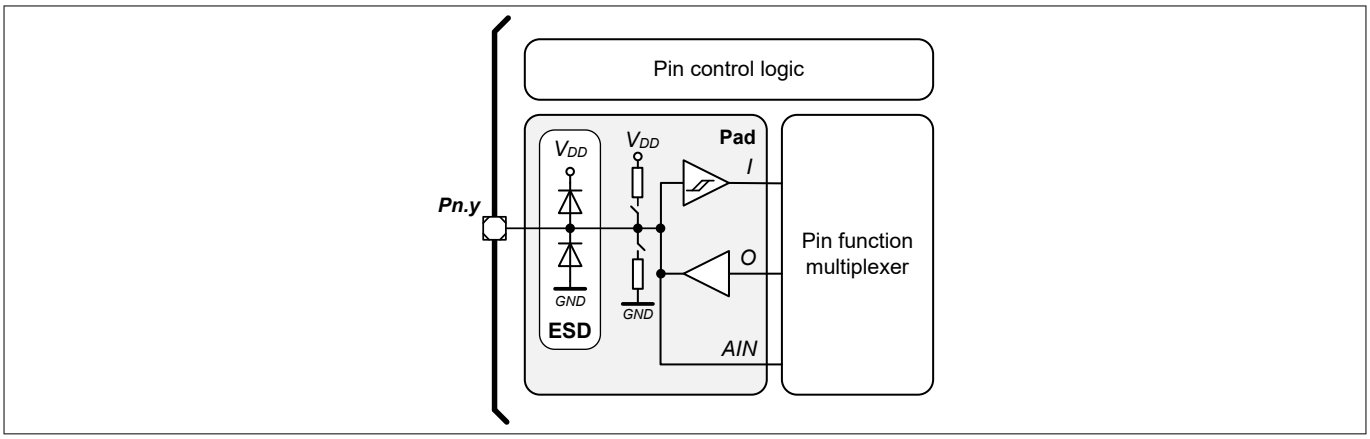

Figure 2 Pin Pad and Function Configuration

The pin function table given below refers to the standard configuration. The pin control or interface functions are defined by the version of software downloaded to the device and may change. Some of the input pins can be configured to have pull up or pull down resistor and some output pins can be configured to push-pull or open drain. This is described in the respective software hardware reference manual.

Pins can serve multiple functions and have to be configured accordingly. Please also refer to the respective pin configuration drawings in this data sheet and the description in the hardware MCE software reference manual.

Pins that do not have any signal assigned are reserved for future use. These pins should be left unconnected and neither be connected to ground nor to the positive supply.

Note: All required reference voltages are generated by an internal DAC, therefore the AO pins like IREF, REFU, REFV, and REFW only require a blocking capacitor.

2.2 Pin configuration IMC301A/ IMC302A

Table 1 Pin list

Signal	Type	IMC301A-F048	IMC301A-F064	IMC302A-F048	IMC302A-F064	Description
Supply						
VDD	Power	21, 28, 38	24, 25, 35, 50	21, 28, 38	24, 25, 35, 50	Supply Voltage
VSS	Power	20, 37	23, 49	20, 37	23, 49	Ground
Motor control						
PWMUL	O	22	29	22	29	PWM output phase U low
PWMUH	O	23	30	23	30	PWM output phase U high
PWMVL	O	24	31	24	31	PWM output phase V low
PWMVH	O	25	32	25	32	PWM output phase V high
PWMWL	O	26	33	26	33	PWM output phase W low
PWMWH	O	27	34	27	34	PWM output phase W high
GK	I	29	36	29	36	Motor gate kill input
VDC	AIN	11	14	11	14	DC bus sensing input
ISS/IU	AIN	15	18	15	18	Current sense input single shunt / phase U
IV	AIN	12	15	12	15	Current sense input phase V
IW	AIN	8	11	8	11	Current sense input phase W
REFU	AO	14	17	14	17	Itrip phase U reference
REFV	AO	13	16	13	16	Itrip phase V reference
REFW	AO	7	10	7	10	Itrip phase W reference
Hall sensor inputs						
AHALL1+	AIN	7	10	7	10	Analog Hall sensor input 1+
AHALL1-	AIN	8	11	8	11	Analog Hall sensor input 1-
AHALL2+	AIN	13	16	13	16	Analog Hall sensor input 2+
AHALL2-	AIN	12	15	12	15	Analog Hall sensor input 2-
HALL1	IO	-	26	-	26	Digital Hall sensor input 1
HALL2	IO	-	27	-	27	Digital Hall sensor input 2
HALL3	IO	-	28	-	28	Digital Hall sensor input 3
Power factor correction						
PFCG0	O	-	-	33	44	PFC gate drive 0
PFCG1	O	-	-	32	43	PFC gate drive 1 (totem pole PFC)
IPFC	AIN	-	-	9	12	PFC current sensing
IPFCREF	AO	-	-	18	21	PFC Itrip reference
IPFCTRIP	AIN	-	-	19	22	PFC Trip

(table continues...)

Table 1 (continued) Pin list

Signal	Type	IMC301A-F048	IMC301A-F064	IMC302A-F048	IMC302A-F064	Description
VAC1	AIN	-	-	17	20	AC voltage sensing input 1
VAC2	AIN	-	-	16	19	AC voltage sensing input 2
Interface						
PGOUT	O	31	42	31	42	Pulse output
NTC	AIN	10	13	10	13	External thermistor input
LED	O	30	41	30	41	Status LED
Communication						
RXD0	I	35	45	35	45	Serial port 0, device programming, receive input
TXD0	O	36	46	36	46	Serial port 0, device programming, transmit output
IR0	I	35	45	35	45	Infrared reception, pin 0
IR1	I	30	39	30	39	Infrared reception, pin 1
Scripting						
AIN1	AIN	7	10	7	10	Analog input 1
AIN2	AIN	8	11	8	11	Analog input 2
AIN3	AIN	9	12	-	-	Analog input 3
AIN4	AIN	10	13	10	13	Analog input 4
AIN7	AIN	13	16	13	16	Analog input 7
AIN8	AIN	14	17	14	17	Analog input 8
AIN10	AIN	16	19	-	-	Analog input 8
AIN11	AIN	17	20	-	-	Analog input 8
GPIO2	IO	32	-	-	-	Digital input/output 2
GPIO3	IO	33	-	-	-	Digital input/output 3
GPIO4	IO	34	-	34	-	Digital input/output 4
GPIO5	IO	18	-	-	-	Digital input/output 5
GPIO6	IO	19	-	-	-	Digital input/output 6
GPIO7	IO	-	21	-	-	Digital input/output 7
GPIO8	IO	-	22	-	-	Digital input/output 8
GPIO9	IO	-	26	-	26	Digital input/output 9
GPIO10	IO	-	27	-	27	Digital input/output 10
GPIO11	IO	-	28	-	28	Digital input/output 11
GPIO12	IO	-	37	-	37	Digital input/output 12
GPIO13	IO	-	38	-	38	Digital input/output 13
GPIO14	IO	-	39	-	39	Digital input/output 14
GPIO15	IO	-	40	-	40	Digital input/output 15

(table continues...)

Table 1 (continued) Pin list

Signal	Type	IMC301A-F048	IMC301A-F064	IMC302A-F048	IMC302A-F064	Description
GPIO16	IO	-	43	-	-	Digital input/output 16
GPIO17	IO	-	44	-	-	Digital input/output 17
IR0	I	35	45	35	45	IR interface 0
IR1	I	30	39	30	39	IR interface 1
Microcontroller						
P0.8	IO	39	51	39	51	Programmable I/O
P0.9	IO	40	52	40	52	Programmable I/O
P0.10 / (XTAL1)	IO	41	53	41	53	Programmable I/O / crystal input 1
P0.11 / (XTAL2)	IO	42	54	42	54	Programmable I/O / crystal input 2
P0.12	IO	43	55	43	55	Programmable I/O
P0.13	IO	44	56	44	56	Programmable I/O
P0.14 / (SWDIO)	IO	45	57	45	57	Programmable I/O / user serial debug I/O
P0.15 / (SWDCLK)	I	46	58	46	58	Programmable I/O / user serial debug clock
P1.0	IO	-	48	-	48	Programmable I/O
P1.1	IO	-	47	-	47	Programmable I/O
P2.0 / (TXD2)	IO/AIN	2	3	2	3	Programmable I/O / analog input / UART2 transmission
P2.1 / (RXD2)	IO/AIN	3	4	3	4	Programmable I/O / analog input / UART2 reception
P2.2	IO/AIN	4	5	4	5	Programmable I/O / analog input
P2.6	IO/AIN	5	6	5	6	Programmable I/O / analog input
P2.8	IO/AIN	-	7	-	7	Programmable I/O / analog input
P2.10	IO/AIN	-	8	-	8	Programmable I/O / analog input
P2.11	IO/AIN	6	9	6	9	Programmable I/O / analog input
P4.0	IO	-	59	-	59	Programmable I/O
P4.1	IO	47	60	47	60	Programmable I/O
P4.2	IO	48	61	48	61	Programmable I/O
P4.3	IO	1	62	1	62	Programmable I/O
P4.4 / (RXD1)	I	-	63	-	63	Programmable I/O / UART1 transmission
P4.5 / (TXD1)	O	-	64	-	64	Programmable I/O / UART1 reception
P4.6	IO	-	1	-	1	Programmable I/O
P4.7	IO	-	2	-	2	Programmable I/O

2.3 Pin configuration drawing IMC301A

The following drawings give the position of the functional pins for the available packages. Only the primary function of the respective pin is shown in the drawings. Depending on the version of the Motion Control Engine (MCE) used pins might provide additional functionality which is given in the respective pin configuration tables.

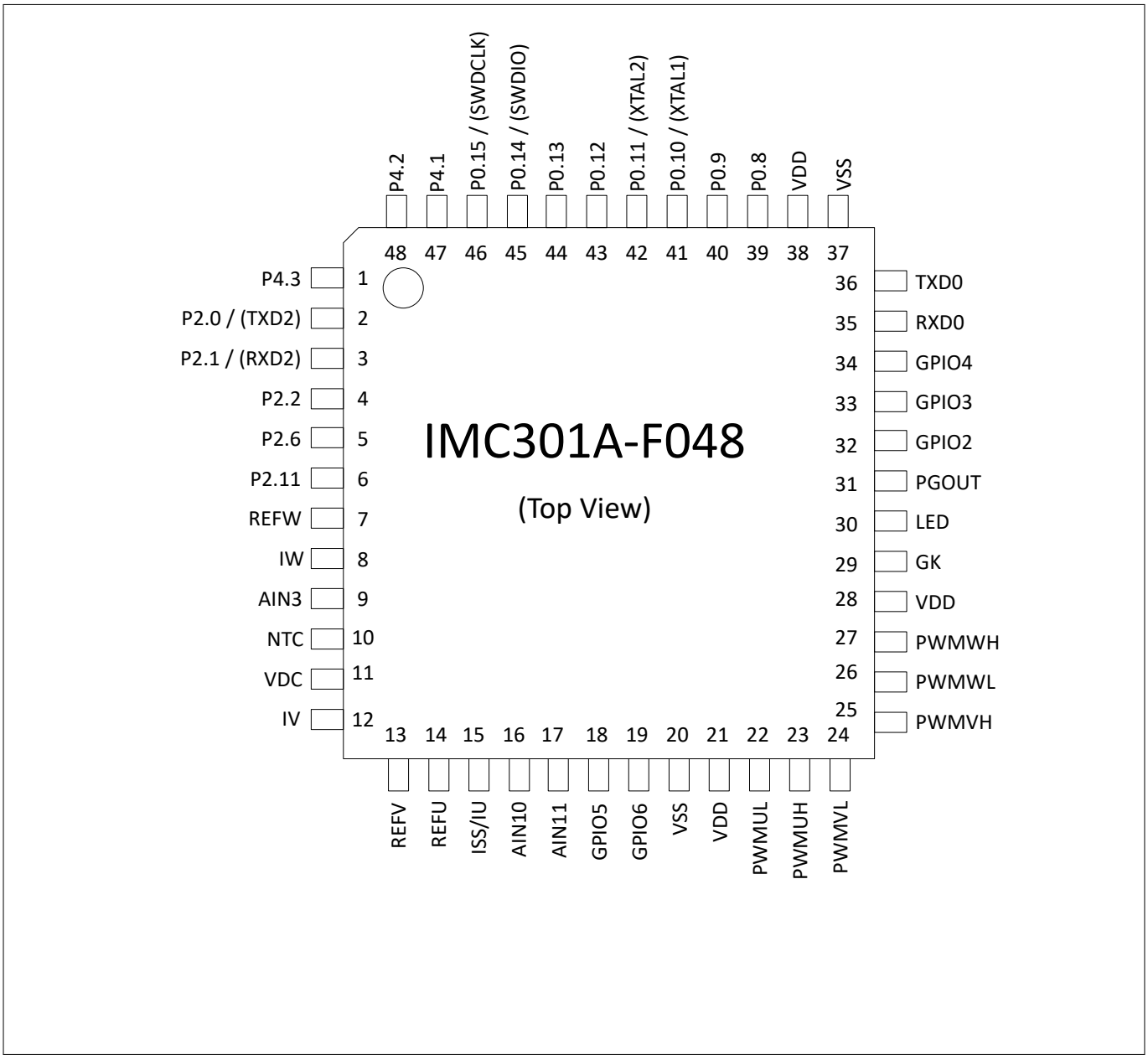

Figure 3 IMC301A-F048

2 Pin configuration

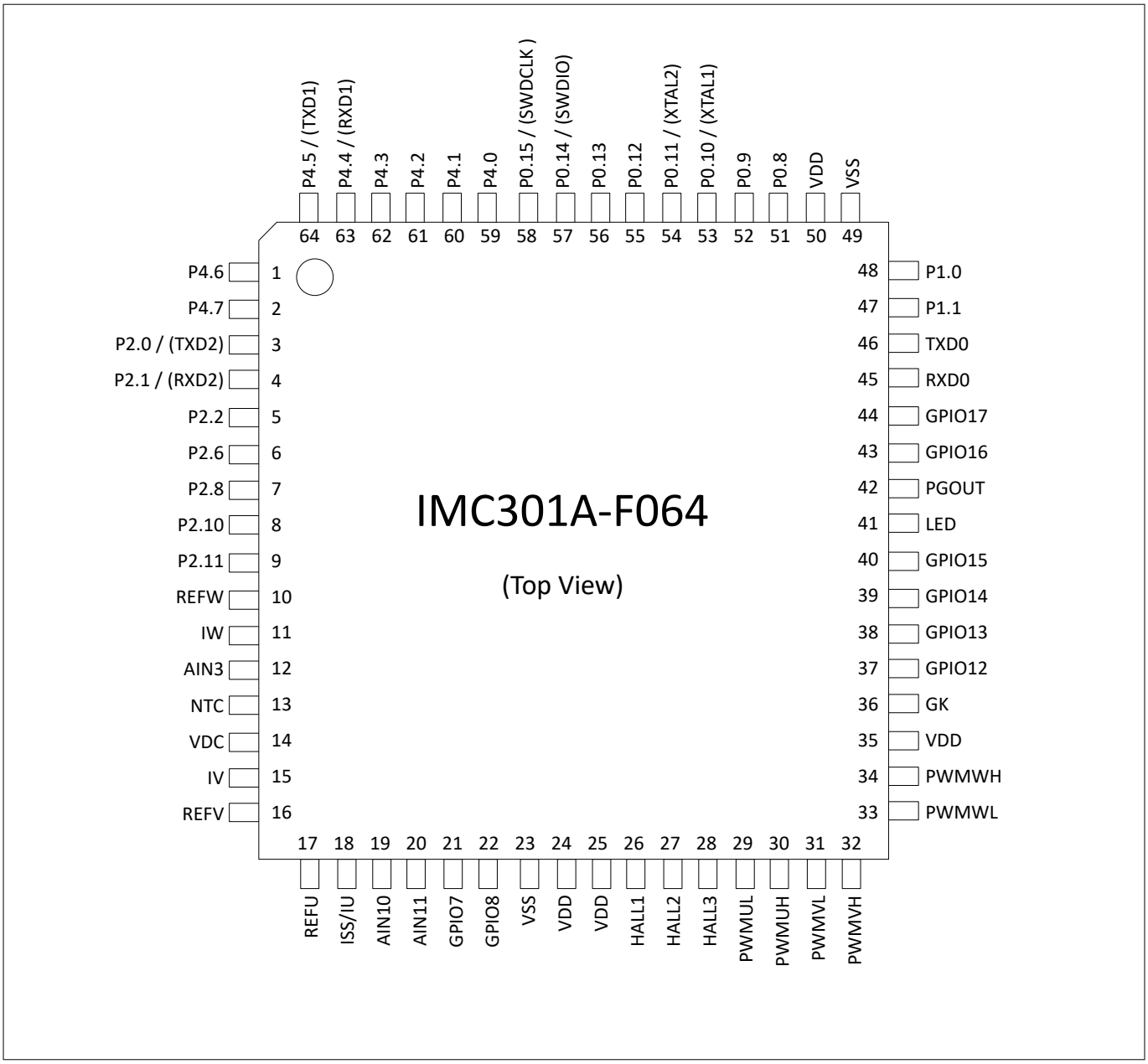

Figure 4 IMC301A-F064

2.4 Pin configuration drawing IMC302A

The following drawings give the position of the functional pins for the available packages. Only the primary function of the respective pin is shown in the drawings. Depending on the version of the Motion Control Engine (MCE) used pins might provide additional functionality which is given in the respective pin configuration tables.

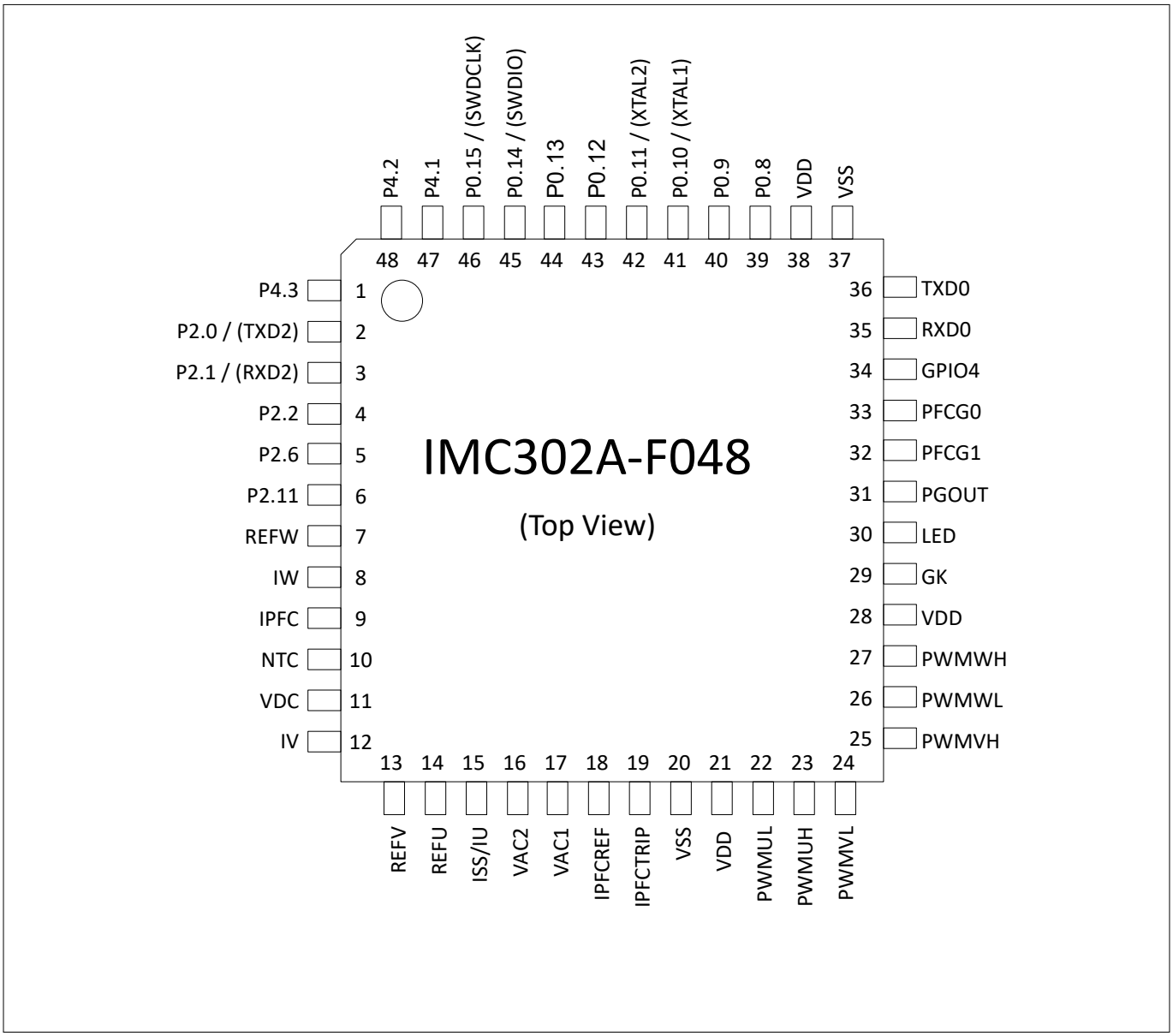

Figure 5 IMC302A-F048

2 Pin configuration

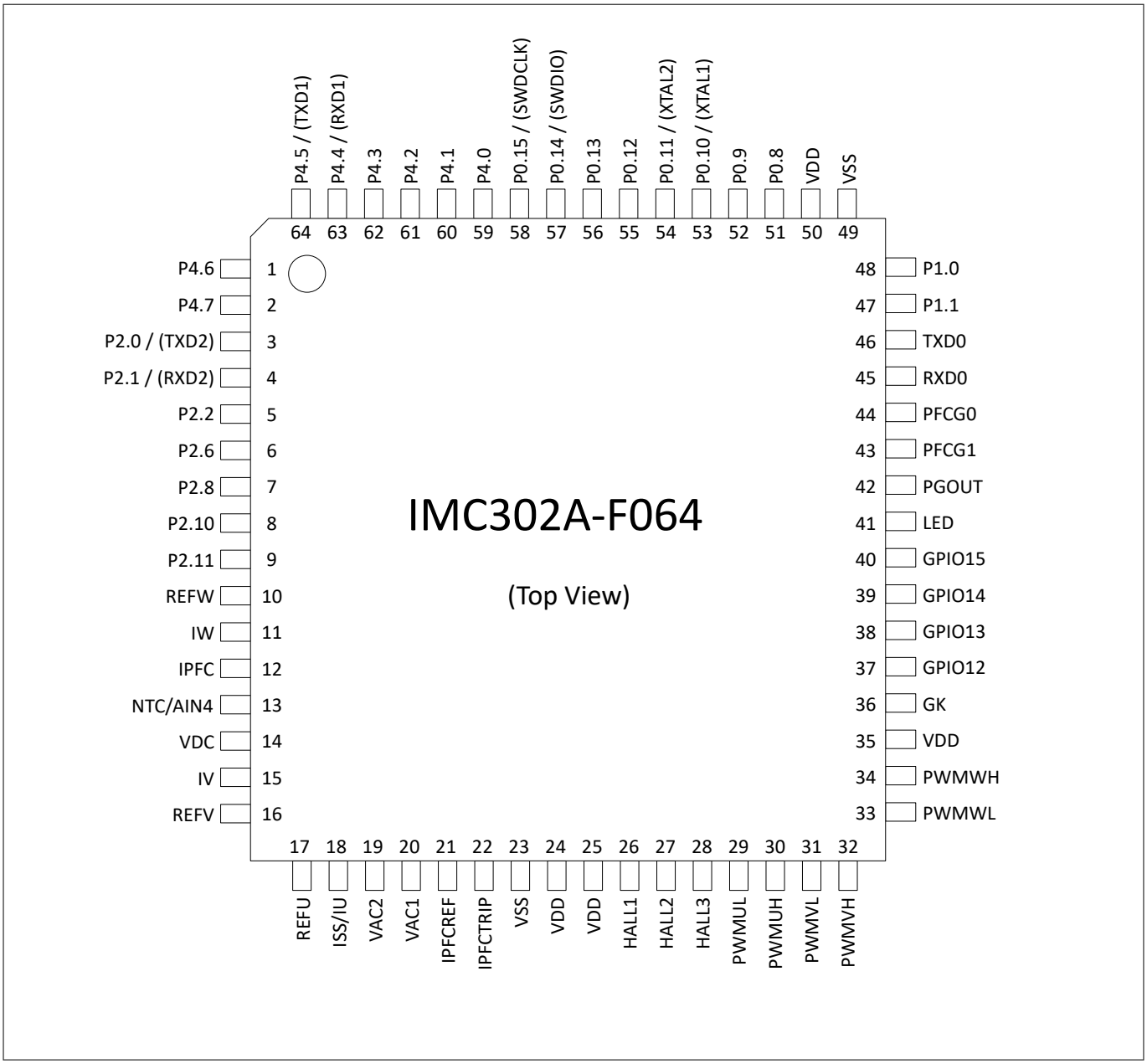

Figure 6 IMC302A-F064

3 Functional description

3.1 Overview

IMC300 architecture is based on a combination of the Motion Control Engine (MCE) with an additional microcontroller using an ARM® Cortex®-M0 core providing the necessary computation power for the permanent magnet motor sensorless or sensored control and an optional PFC control.

The MCE motor control algorithm employs a fast angle sensing at startup and enables low and ultra-high speed operation, and offers either single or leg shunt current sensing. PFC control supports two topologies, namely a single stage boost mode PFC and a totem-pole PFC with fast PWM rate switching to minimize the inductor size. User can configure the motor and PFC parameters for each specific motors and store into the onboard Flash memory. The MCE also contains the UL 607310-1 Software Safety certified library and modules.

The ARM® Cortex®-M0 CPU provides the computation capabilities for additional application flexibility.

A fast inter-processing communication (JCOM) is employed in order to facilitate information sharing between the two processing units – MCE and ARM® Cortex®-M0 MCU.

3.2 Application connection IMC301A with single shunt

The following figure shows the application connection for a single motor configuration. This example is based on a single shunt resistor current sensing configuration.

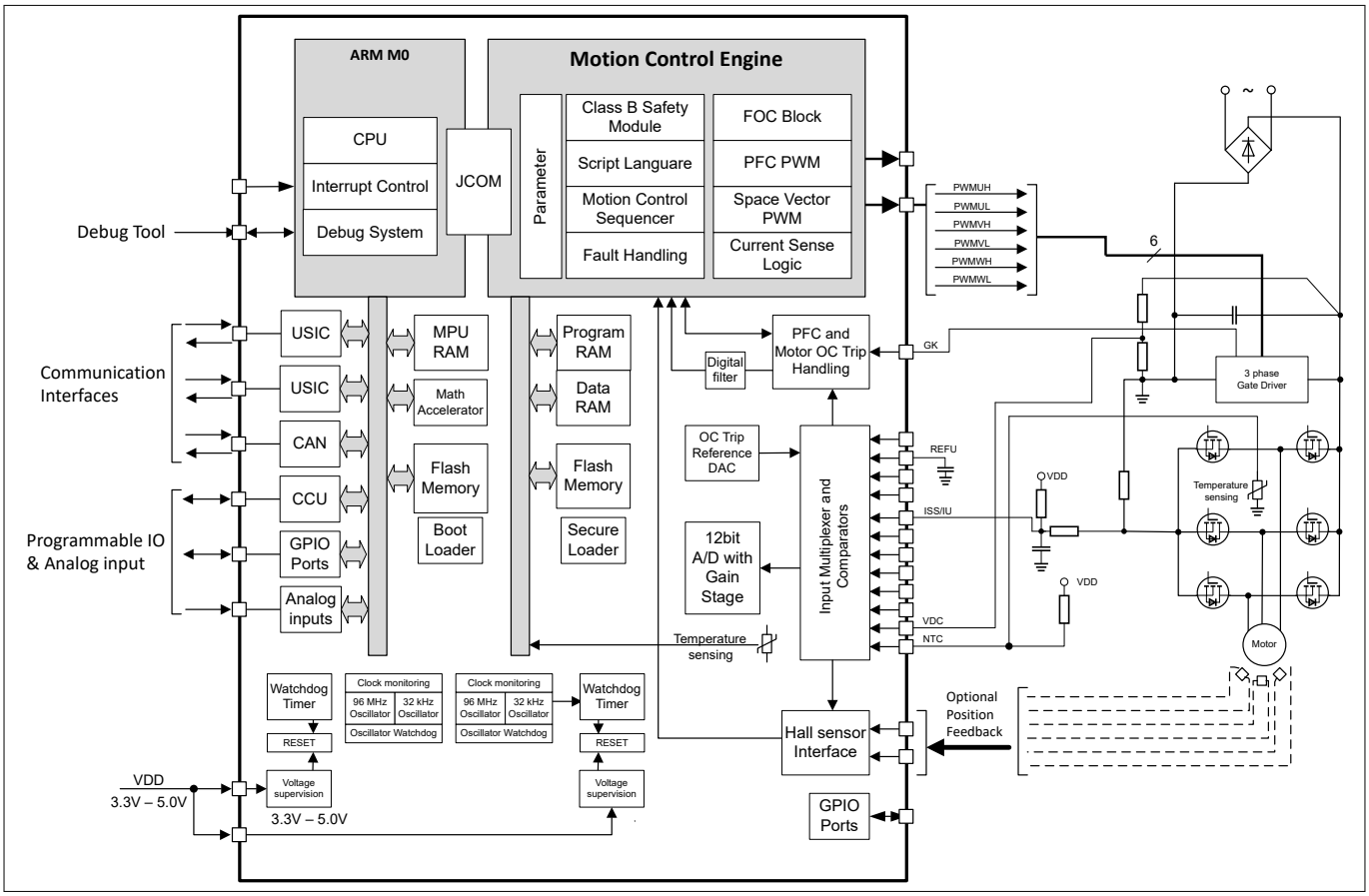

Figure 7 IMC301A application connection single shunt

3.3 Application connection IMC302A with single shunt

The following figure shows the application connection with single shunt current sensing and a boost mode PFC configuration as used for example in the outdoor unit of an air conditioner or heat pump.

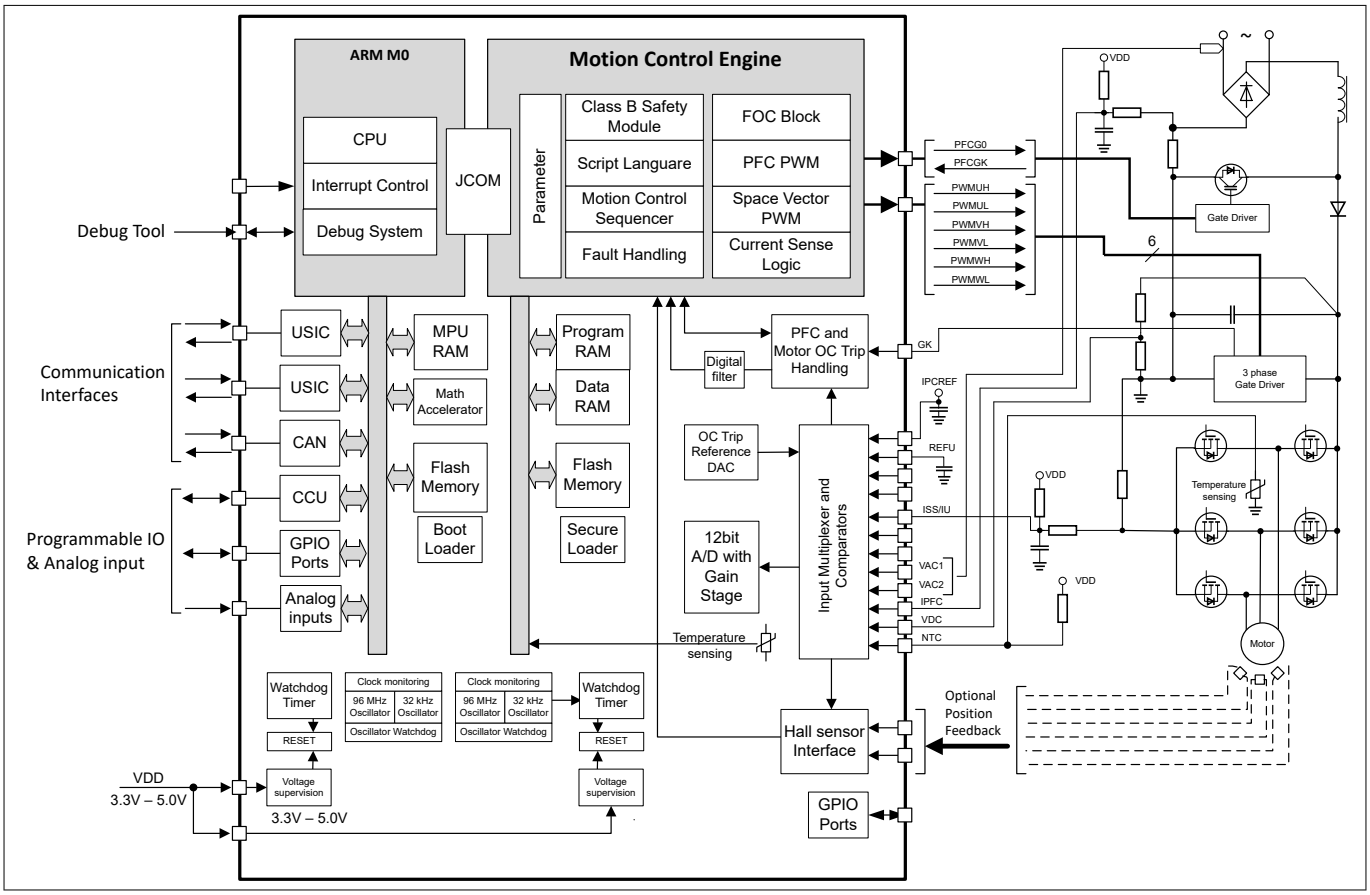

Figure 8 IMC302A application connection single shunt

3.4 Application connection IMC302A with leg shunt

The following figure shows the application connection with leg shunt current sensing and a boost mode PFC configuration as used for example in the outdoor unit of an air conditioner or heat pump.

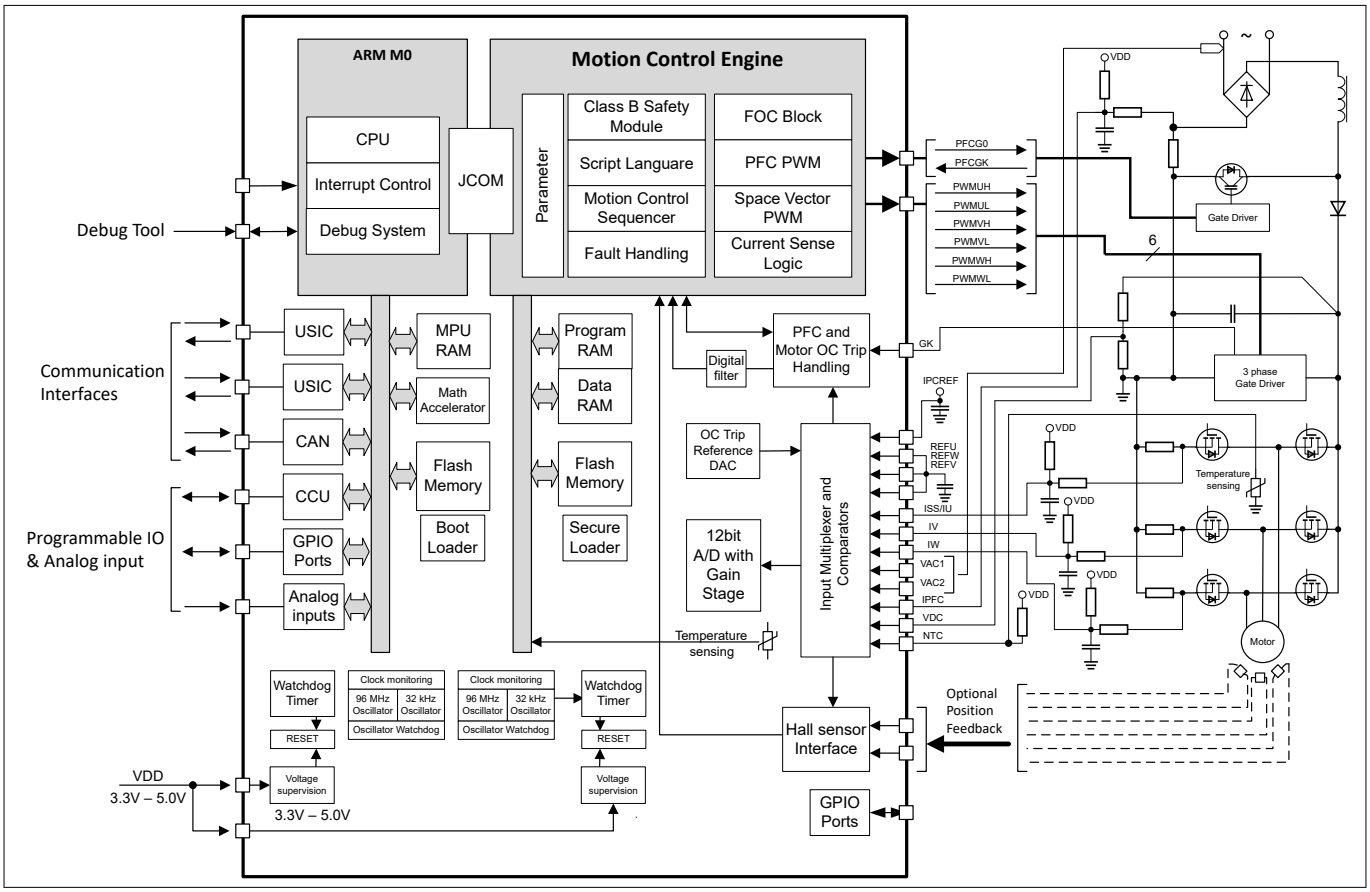

Figure 9 IMC302A application connection leg shunt

4 Electrical characteristics and parameters

4.1 General parameters

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the IMC300 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**

  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the IMC300 and must be regarded for a system design.
- **SR**

  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the IMC300 is designed in.

4.1.2 Absolute maximum ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note or Test Condition
		Min.	Max.		
Ambient temperature	T_A SR	-40	105	°C	
Junction temperature	T_J SR	-40	115	°C	Digital controller
Storage temperature	T_{ST} SR	-40	125	°C	
Lead temperature (soldering, 30 seconds)	T_L SR	---	260	°C	
Digital Controller voltage	V_{DD} SR	-0.3	6	V	
Controller digital and analog pin voltage	V_{ID} SR	-0.3	V_{DD}+0.3	V	
Input current on any controller pin during overload condition	I_{IN} SR	-10	10	mA	
Absolute sum of all controller input currents during overload condition	ΣI_{IN} SR	-50	50	mA	

Note: Characterized, not tested at manufacturing.

Note: Voltages referenced to V_{SS} if not stated otherwise

4.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The table below defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- Operating Conditions are met for
  - pad supply levels (V_{DD})
  - temperature

If a pin current is outside of the Operating Conditions but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 3 Overload Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input current on analog port pins during overload condition	I_{OVA} SR	-3	–	3	mA	
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 10 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DD} and ground are a simplified representation of these ESD protection structures.

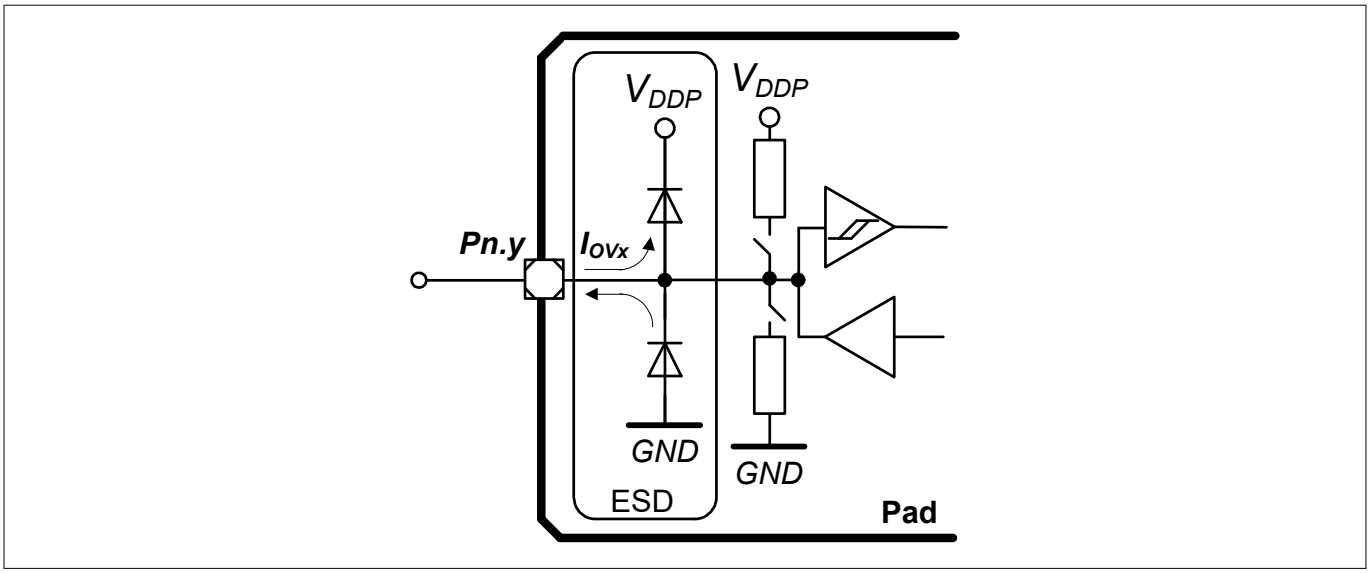

Figure 10 Input Overload Current via ESD structures

Table 4 and Table 5 list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the Absolute maximum ratings must not be exceeded during overload.

Table 4 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DD}$ +(0.3 ... 0.5) V $V_{AIN} = V_{DD}$ + 0.5 V $V_{AREF} = V_{DD}$ + 0.5 V

Table 5 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS}$ - (0.3 … 0.5) V $V_{AIN} = V_{SS}$ - 0.5 V $V_{AREF} = V_{SS}$ - 0.5 V

4.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the IMC300. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 6 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	105	°C	
Junction temperature	T_J SR	-40	–	115	°C	
Digital supply voltage[1)]	V_{DD} SR	3.0	3.3	5.5	V	

1 All supply pins must be driven with the same voltage.

4.2 DC characteristics

4.2.1 Input/Output Characteristics

The table below provides the characteristics of the input/output pins of the controller.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 7 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	0.19 × V_{DD}	V	CMOS Mode
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	0.7 × V_{DD}	–	V	CMOS Mode
Input low voltage on port pins (Large Hysteresis, scripting pins only)	V_{ILPL}	SR	–	0.08 × V_{DD}	V	CMOS Mode
Input high voltage on port pins (Large Hysteresis, scripting pins only)	V_{IHPL}	SR	0.85 × V_{DD}	–	V	CMOS Mode
Output low voltage on port pins	V_{OLP}	CC	–	1.0	V	I_{OL} = 11 mA (V) I_{OL} = 7 mA (3.3 V)
			–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on PWM outputs	V_{OLP1}	CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
			–	0.32	V	I_{OL} = 10 mA (5 V)
			–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins	V_{OHP}	CC	V_{DD} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
			V_{DD} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on PWM outputs	V_{OHP1}	CC	V_{DD} - 0.32	–	V	I_{OH} = -6 mA (5 V)
			V_{DD} - 1.0	–	V	I_{OH} = -8 mA (3.3 V)
			V_{DD} - 0.4	–	V	I_{OH} = -4 mA (3.3 V)
Rise/fall time on PWM outputs[2)]	t_{HCPR}, t_{HCPF}	CC	–	9	ns	50 pF @ 5 V

(table continues...)

Table 7 (continued) Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
			–	12	ns	50 pF @ 3.3 V
Rise/fall time on standard pad	t_R, t_F	CC	–	12	ns	50 pF @ 5 V
			–	15	ns	50 pF @ 3.3 V.
Pin capacitance (digital inputs/outputs)	C_{IO}	CC	–	10	pF	
Pull-up/-down resistor on port pins (if enabled in software)	R_{PUP}	CC	20	50	kΩ	$V_{IN} = V_{SS}$
Input leakage current [3]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DD}$, T_A 105°C
Maximum current per pin standard pin	I_{MP}	SR	-10	11	mA	–
Maximum current per PWM outputs pins	I_{MP1A}	SR	-10	50	mA	–
Maximum current into V_{DD} / out of V_{SS}	I_{MVDD} / I_{MVSS}	SR	–	260	mA	

2 Rise/Fall time parameters are taken with 10% - 90% of supply.
3 An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

4.2.2 Analog to Digital Converter (ADC)

The following table shows the Analog to Digital Converter (ADC) characteristics. This specification applies to all analog input including the analog Hall sensor interface input (AHALLx+/AHALLx-, where x=1,2) as given in the pin configuration list.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 8 ADC Characteristics (Operating Conditions apply)[4)]

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage range	V_{DD} SR	3.0	–	5.5	V	
Analog input voltage range	V_{AIN} SR	V_{SS}- 0.05	–	V_{DD}+ 0.05	V	
Conversion time	t_{C12} CC	–	1.0	–	µs	Defined by SW
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	
Sample time	t_{sample} CC	–	333	–	ns	Defined by SW
RMS noise	EN_{RMS} CC	–	1.5	–	LSB12	
DNL error	EA_{DNL} CC	–	±2.0	–	LSB12	
INL error	EA_{INL} CC	–	±4.0	–	LSB12	
Gain error	EA_{GAIN} CC	–	±0.5	–	%	
Offset error	EA_{OFF} CC	–	±8.0	–	mV	

4.2.3 Analog comparator characteristics

The table below shows the Analog Comparator characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 9 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note or Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	–	V_{DDP} + 0.05	V	includes common mode and differential input voltages
Input Offset	V_{CMPOFF}	CC	–	+/-3	–	mV	High power mode ΔV_{CMP} < 200 mV
Input Hysteresis	V_{HYS}	CC	–	+/-15	–	mV	Defined by SW

4 All parameters are defined for the full supply range if not stated otherwise.

4.2.4 Power Supply Current Controller

The total power supply current defined below consists of a leakage and a switching component for the controller through the V_{DD} pin.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 10 Power supply parameter tableV_{DD}= 5.0V

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Active mode current motor control only	I_{DD1} CC	–	10	20	mA	T_a = 25°C
Active mode current motor control plus PFC	I_{DD2} CC	–	16	20	mA	T_a = 25°C

4.2.5 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 11 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Data Retention Time	t_{RET} CC	10			years	Max. 100 erase / program cycles
Erase Cycles	N_{ECYC} CC			$5*10^4$	cycles	Sum of page and sector erase cycles a page sees
Total Erase Cycles	N_{TECYC} CC			$2*10^6$	cycles	

4.2.6 Embedded microcontroller

4.2.6.1 Analog to digital converters (ADC)

Table 12 shows the Analog to Digital Converter (ADC) characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Timing values adjusted to the clock speed of 48MHz and 32MHz.

Table 12 ADC Characteristics (Operating Conditions apply)[5)]

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	2.0	–	3.0	V	SHSCFG.AREF = 11_B; CALCTR.CALGNSTC = $0C_H$ for f_{SH} = 32 MHz, 12_H for f_{SH} = 48 MHz
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP}-0.05	–	V_{DDP}+0.05	V	
Auxiliary analog reference ground[6)]	V_{REFGND} SR	V_{SSP}-0.05	–	1.0	V	G0CH0
		V_{SSP}-0.05	–	0.2	V	G1CH0
Internal reference voltage (full scale value)	V_{REFINT} CC	5			V	
Switched capacitance of an analog input	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	

(table continues...)

5 The parameters are defined for ADC clock frequencies f_{SH} = 32 MHz for the full supply range, and f_{SH} = 48 MHz at V_{DD_int}, V_{DD_ext} = 5 V. Usage of any other frequencies may affect the ADC performance.

6 The alternate reference ground connection is separate for each converter. This mode, therefore, provides the lowest noise impact.

Table 12 (continued) ADC Characteristics (Operating Conditions apply)[5]

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	
Gain settings	G_{IN} CC	1			–	GNCTRxz.GAINy = 00_B (unity gain)
		3			–	GNCTRxz.GAINy = 01_B (gain g1)
		6			–	GNCTRxz.GAINy = 10_B (gain g2)
		12			–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	5	–	–	1 / f_{ADC}	V_{DD} = 5.0 V, f_{ADCI} = 48 MHz
		3	–	–	1 / f_{ADC}	V_{DD} = 5.0 V, f_{ADCI} = 32 MHz
		3	–	–	1 / f_{ADC}	V_{DD} = 3.3 V, f_{ADCI} = 32 MHz
		30	–	–	1 / f_{ADC}	V_{DD} = 2.0 V, f_{ADCI} = 32 MHz[5]
Conversion time in fast compare mode	t_{CF} CC	9			1 / f_{ADC}	[7]
Conversion time in 12-bit mode	t_{C12} CC	20			1 / f_{ADC}	[7]
Maximum sample rate in 12-bit mode[8]	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC	18			1 / f_{ADC}	[7]
Maximum sample rate in 10-bit mode[8]	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC	16			1 / f_{ADC}	[7]

(table continues...)

5 The parameters are defined for ADC clock frequencies f_{SH} = 32 MHz for the full supply range, and f_{SH} = 48 MHz at V_{DD_int}, V_{DD_ext} = 5 V. Usage of any other frequencies may affect the ADC performance.
7 No pending samples assumed, excluding sampling time and calibration.
8 Includes synchronization and calibration (average of gain and offset calibration).

Table 12 (continued) ADC Characteristics (Operating Conditions apply)[5]

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode[8]	f_{C8} CC	–	–	f_{ADC} / 38.5	–	1 sample pending
		–	–	f_{ADC} / 54.5	–	2 samples pending
RMS noise[9]	EN_{RMS} CC	–	1.5	–2.7	LSB12	DC input, SHSCFG.AREF = 00_B, GNCTRxz.GAINy = 00_B (unity gain), V_{DD} = 5.0 V, $V_{AIN = 2.5\ V}$, 25°C
DNL error	EA_{DNL} CC	–	±2.0	–	LSB12	
INL error	EA_{INL} CC	–	±4.0	–	LSB12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00_B (calibrated)
Gain error with internal reference[10]	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 110°C
		–	±2.0	–	%	SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±8.0	–	mV	Calibrated, V_{DD} = 5.0 V

5 The parameters are defined for ADC clock frequencies f_{SH} = 32 MHz for the full supply range, and f_{SH} = 48 MHz at V_{DD_int}, V_{DD_ext} = 5 V. Usage of any other frequencies may affect the ADC performance.
8 Includes synchronization and calibration (average of gain and offset calibration).
9 This parameter can also be defined as an SNR value: SNR[dB] = 20 × log(A_{MAXeff} / N_{RMS}). With $A_{MAXeff} = 2^N / 2$, SNR[dB] = 20 × log (2048 / N_{RMS}) [N = 12].N_{RMS} = 1.5 LSB12, therefore, equals SNR = 20 × log (2048 / 1.5) = 62.7 dB.
10 Includes error from the reference voltage.

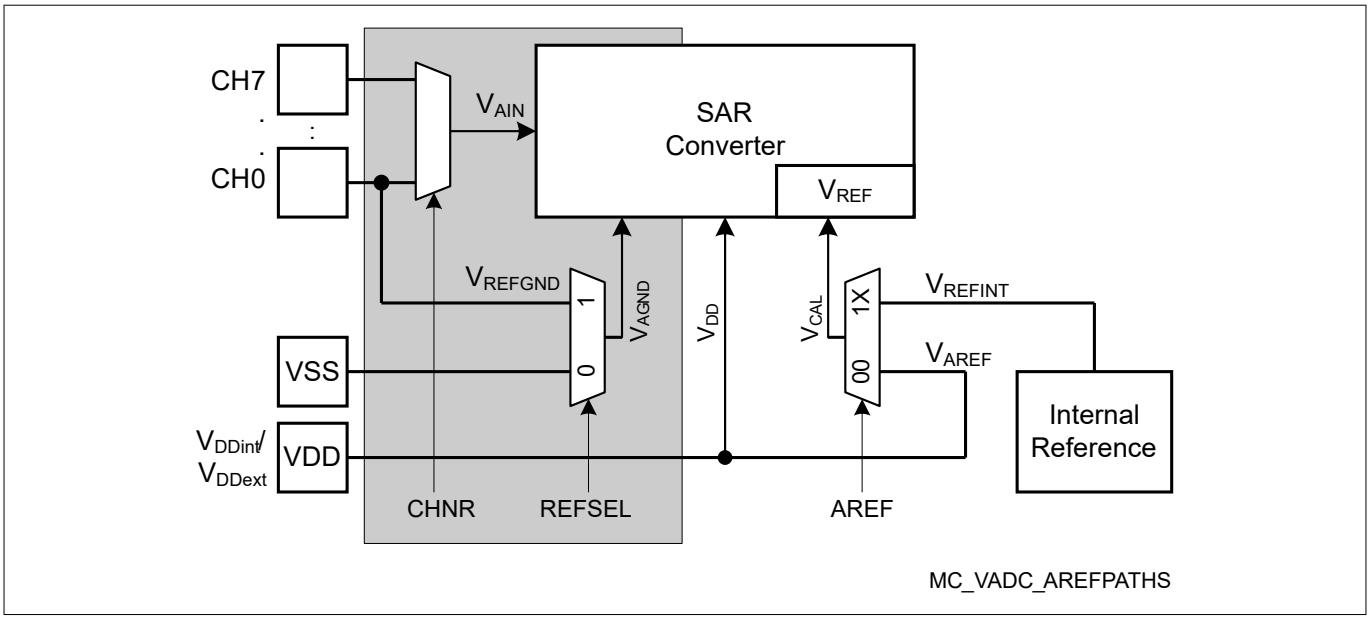

Figure 11 ADC Voltage Supply

4.2.6.2 Out of range comparator (ORC) characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in Table 13 apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

The parameters in Table 13 apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

Table 13 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; V_{DDP} = 3.0 V - 5.5 V; C_L = 0.25pF)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
DC Switching Level	V_{ODC} CC	–	–	180	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS} CC	15	–	54	mV	
Always detected Overvoltage Pulse	t_{OPDD} CC	103	–	–	ns	$V_{AIN} \geq V_{DDP} + 150$ mV
		88	–	–	ns	$V_{AIN} \geq V_{DDP} + 350$ mV
Never detected Overvoltage Pulse	t_{OPDN} CC	–	–	21	ns	$V_{AIN} \geq V_{DDP} + 150$ mV
		–	–	11	ns	$V_{AIN} \geq V_{DDP} + 350$ mV
Detection Delay	t_{ODD} CC	39	–	132	ns	$V_{AIN} \geq V_{DDP} + 150$ mV
		31	–	121	ns	$V_{AIN} \geq V_{DDP} + 350$ mV
Release Delay	t_{ORD} CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 5 V
		57	–	340	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 3.3 V
Enable Delay	t_{OED} CC	–	–	300	ns	ORCCTRL.ENORCx = 1

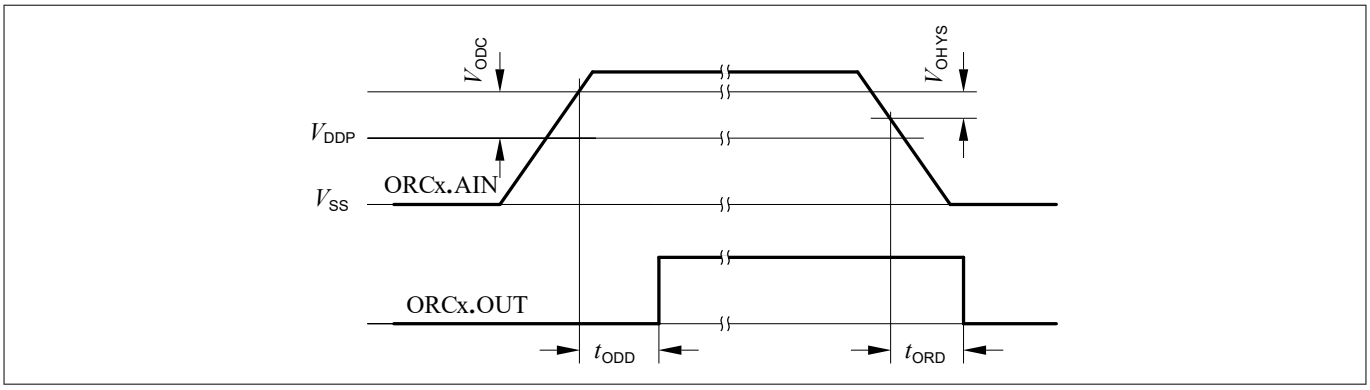

Figure 12 ORCx.OUT Trigger Generation

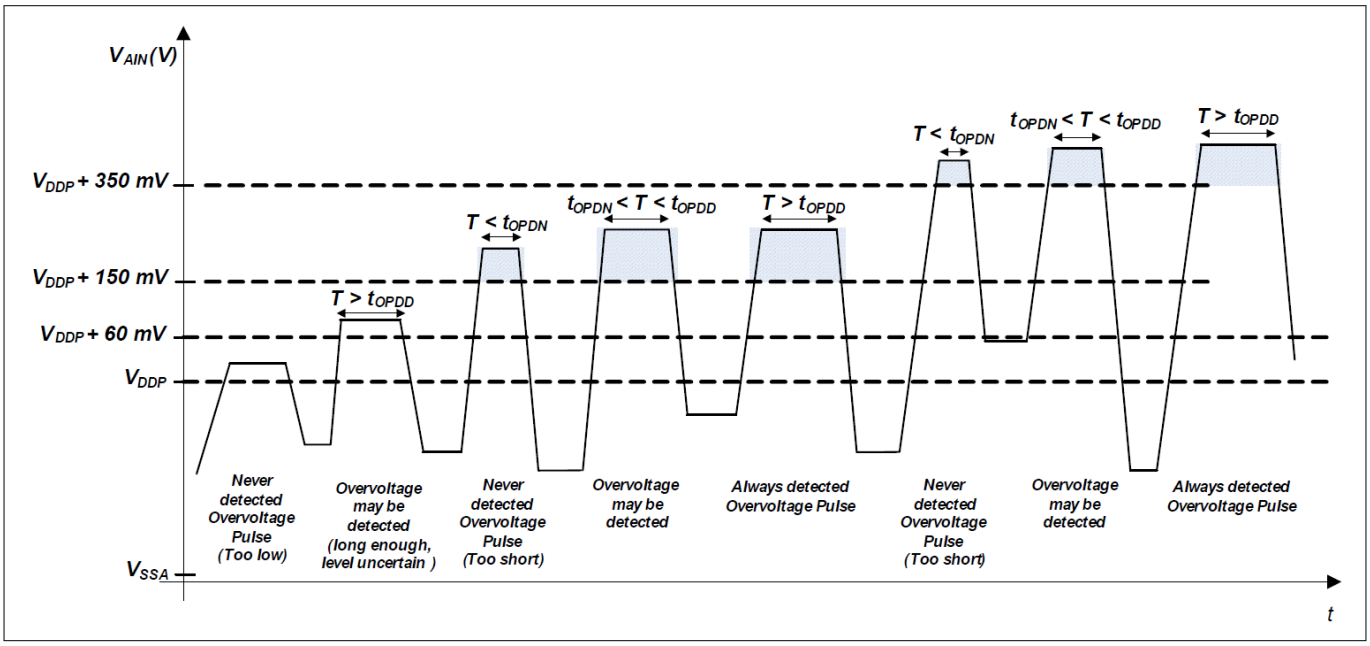

Figure 13 ORC Detection Ranges

4.2.6.3 Analog comparator characteristics

Table 14 below shows the Analog Comparator characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 14 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Notes/ Test Conditions
		Min.	Typ.	Max.		
Input Voltage	V_{CMP} SR	-0.05	–	V_{DDP} + 0.05	V	
Input Offset	V_{CMPOFF} CC	–	+/-3	–	mV	High power mode ΔV_{CMP} < 200 mV

(table continues...)

Table 14 (continued) Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Notes/ Test Conditions
		Min.	Typ.	Max.		
Propagation Delay[11)]	t_{PDELAY} CC	–	25	–	ns	High power mode, ΔV_{CMP} = 100 mV
		–	80	–	ns	High power mode, ΔV_{CMP} = 25 mV
		–	250	–	ns	Low power mode, ΔV_{CMP} = 100 mV
		–	700	–	ns	Low power mode, ΔV_{CMP} = 25 mV
Current Consumption	I_{ACMP} CC	–	100	–	µA	First active ACMP in high power mode, ΔV_{CMP} > 30 mV
		–	66	–	µA	Each additional ACMP in high power mode, ΔV_{CMP} > 30 mV
		–	10	–	µA	First active ACMP in low power mode
		–	6	–	µA	Each additional ACMP in low power mode
Input Hysteresis	V_{HYS} CC	–	+/-15	–	mV	
Filter Delay[11)]	t_{FDELAY} CC	–	5	–	ns	

4.2.6.4 Temperature sensor characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 15 Temperature Sensor Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy[12)]	T_{TSAL} CC	-6	–	6	°C	T_J > 20°C
		-10	–	10	°C	0°C ≤ T_J ≤ 20°C
		–	-/+8	–	°C	T_J < 0°C
Start-up time	t_{TSST} SR	–	–	15	µs	

11 Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.
12 The temperature sensor accuracy is independent of the supply voltage.

The following formula calculates the temperature measured by the temperature sensor in Kelvin [K] from the TSE_MON bit field of the ANATSEMON register.

$$\text{Temperature}[^\circ\text{C}] = \frac{k1 - \sqrt{(k1)^2 - 4(k2 - rx \times k3)}}{2(k2 - rx \times k3)}$$

with :

rx = TSE_MON value in ANATSEMON register

where k1, k2 and k3 values can be found in the flash configuration sector

4.2.6.5 Oscillator pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal/resonator (see Figure 14) or in direct input mode (see Figure 15).

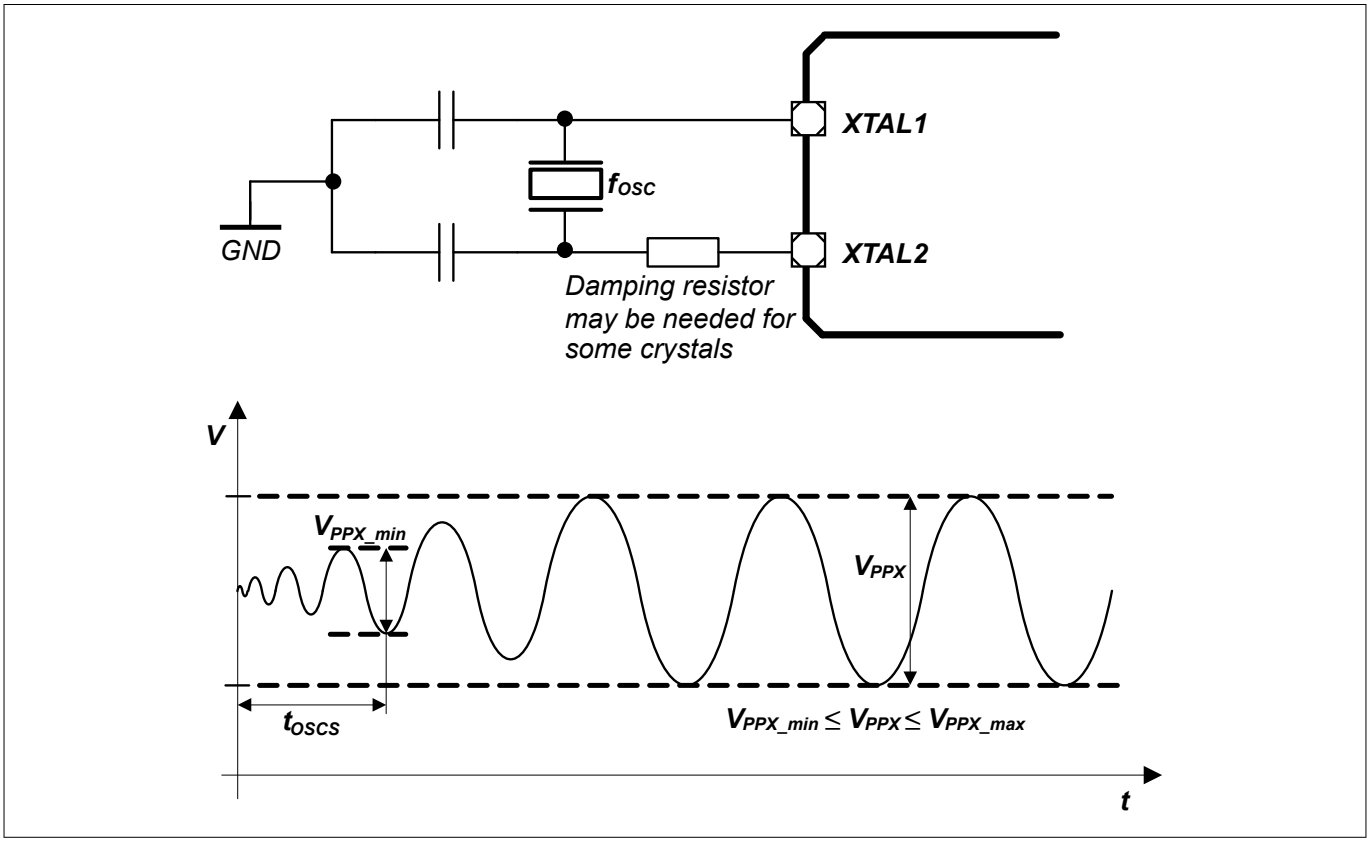

Figure 14 Oscillator in Crystal Mode

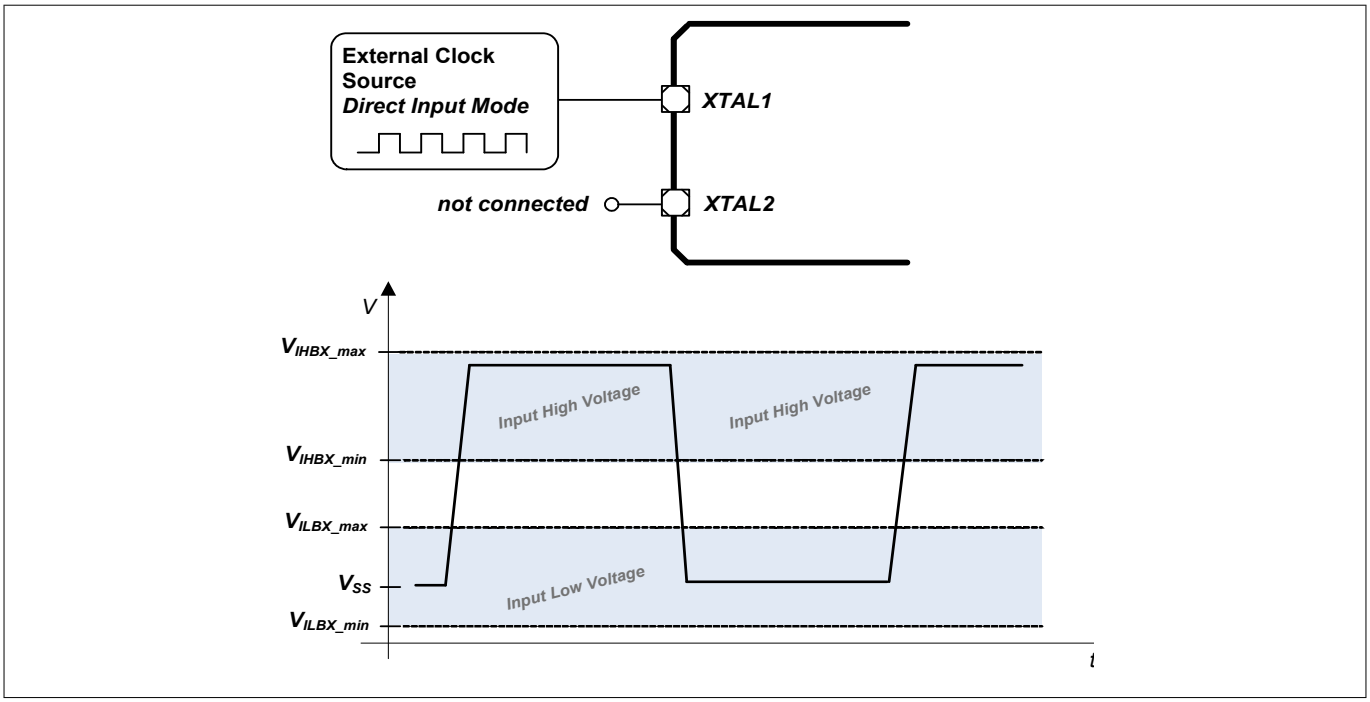

Figure 15 Oscillator in Direct Input Mode

Table 16 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	48	MHz	Direct Input Mode
		4	–	20	MHz	External Crystal Mode
Oscillator start-up time[13)14)]	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.3	–	1.5	V	External Crystal Mode
		-0.3	–	5.5	V	Direct Input Mode
Input amplitude (peak-to-peak) at XTAL1[14)15)]	V_{PPX} SR	0.6	–	1.7	V	External Crystal Mode
Input high voltage at XTAL1[16)]	V_{IHBX} SR	0.8	–	5.5	V	Oscillator disable
Input low voltage at XTAL1[16)]	V_{ILBX} SR	-0.3	–	0.3	V	Oscillator disable

Table 17 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time[17)18)]	t_{OSCS} CC	–	–	5	s	

13 t_{OSCS} is defined from the moment the oscillator is enabled wih SCU_ANAOSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of 0.9 * V_{PPX}.
14 The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
15 If the shaper unit is enabled and not bypassed.
16 If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

4.2.6.6 Flash memory parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Erase time per page / sector	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	t_{PSER} CC	102	152	204	s	
Wake-Up time	t_{WU} CC		32.2		s	
Read time per word	t_a CC		50		ns	
Data Retention Time	t_{RET} CC	10			years	Max. 100 erase / program cycles
Flash Wait States[19)20)]	$N_{WSFLASH}$ CC	0	0	0		f_{MCLK} = 8 MHz
		0	1	1		f_{MCLK} = 16 MHz
		1	2	2		f_{MCLK} = 32 MHz
		2	2	3		f_{MCLK} = 48 MHz
Erase Cycles[21)]	N_{ECYC} CC			$5*10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	N_{TECYC} CC			$2*10^6$	cycles	

17 t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_ANAOSCLPCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 0.9 * V_{PPX}.
18 The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
19 Sum of page erase and sector erase cycles a page sees.
20 Flash wait states are automatically inserted by the Flash module during memory read when needed. Typicalvalues are calculated from the execution of the Dhrystone benchmark program.
21 Sum of page erase and sector erase cycles a page sees.

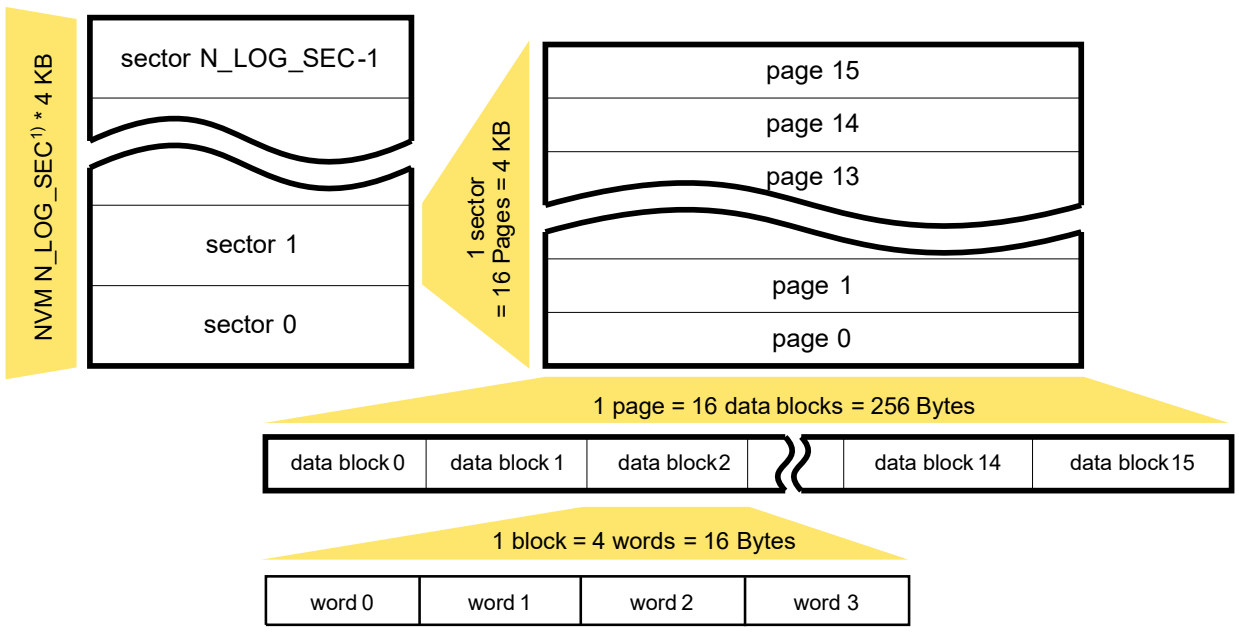

Figure 16 Logical Structure of the Flash

4.2.6.7 Power supply current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Power Supply parameter table; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Active mode current Peripherals enabled $f_{MCLK}f_{PCLK}$in MHz[22]	I_{DDPAE} CC	–	14.1	20[23]	mA	48 / 96
		–	9.8	–	mA	24 / 48
		–	7.8	–	mA	16 / 32
		–	6.4	–	mA	8 / 16
		–	4.4	–	mA	1 / 1
Active mode current Peripherals disabled $f_{MCLK}f_{PCLK}$in MHz[24]	I_{DDPAD} CC	–	6.2	[25]	mA	48 / 96
		–	4.6	–	mA	24 / 48

(table continues...)

22 CPU and all peripherals clock enabled, Flash is in active mode.
23 I_{DDPA} decreases typically by tbd mA when f_{MCLK} decreases by tbd MHz, at constant T_J
24 CPU enabled, all peripherals clock disabled, Flash is in active mode.
25 I_{DDPA} decreases typically by tbd mA when f_{MCLK} decreases by tbd MHz, at constant T_J

Table 19 (continued) Power Supply parameter table; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
		–	3.6	–	mA	16 / 32
		–	3.1	–	mA	8 / 16
		–	1.8	–	mA	1 / 1
Active mode current Code execution from RAM Flash is powered down f_{MCLK} f_{PCLK} in MHz	I_{DDPAR} CC	–	9.6	–	mA	48 / 96
Sleep mode current Peripherals clock enabled f_{MCLK} f_{PCLK} in MHz[26]	I_{DDPSE} CC	–	11.0	–	mA	48 / 96
		–	7.6	–	mA	24 / 48
		–	6.4	–	mA	16 / 32
		–	5.3	–	mA	8 / 16
		–	4.2	–	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash active f_{MCLK} f_{PCLK} in MHz[27]	I_{DDPSD} CC	–	2.8	–	mA	48 / 96
		–	2.2	–	mA	24 / 48
		–	2.0	–	mA	16 / 32
		–	1.9	–	mA	8 / 16
		–	1.7	–	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK} f_{PCLK} in MHz[28]	I_{DDPSR} CC	–	2.2	–	mA	48 / 96
		–	1.7	–	mA	24 / 48
		–	1.4	–	mA	16 / 32
		–	1.2	–	mA	8 / 16
		–	1.1	–	mA	1 / 1
Deep Sleep mode current[29]	I_{DDPDS} CC	–	0.27	–	mA	
Wake-up time from Sleep to Active mode[30]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[31]	t_{DSA} CC	–	290	–	µsec	

26 CPU in sleep, all peripherals clock enabled and Flash is in active mode.
27 CPU in sleep, Flash is in active mode.
28 CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
29 CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
30 CPU in sleep, Flash is in active mode during sleep mode.
31 CPU in sleep, Flash is in powered down mode during deep sleep mode.

Figure 17 shows typical graphs for active mode supply current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.

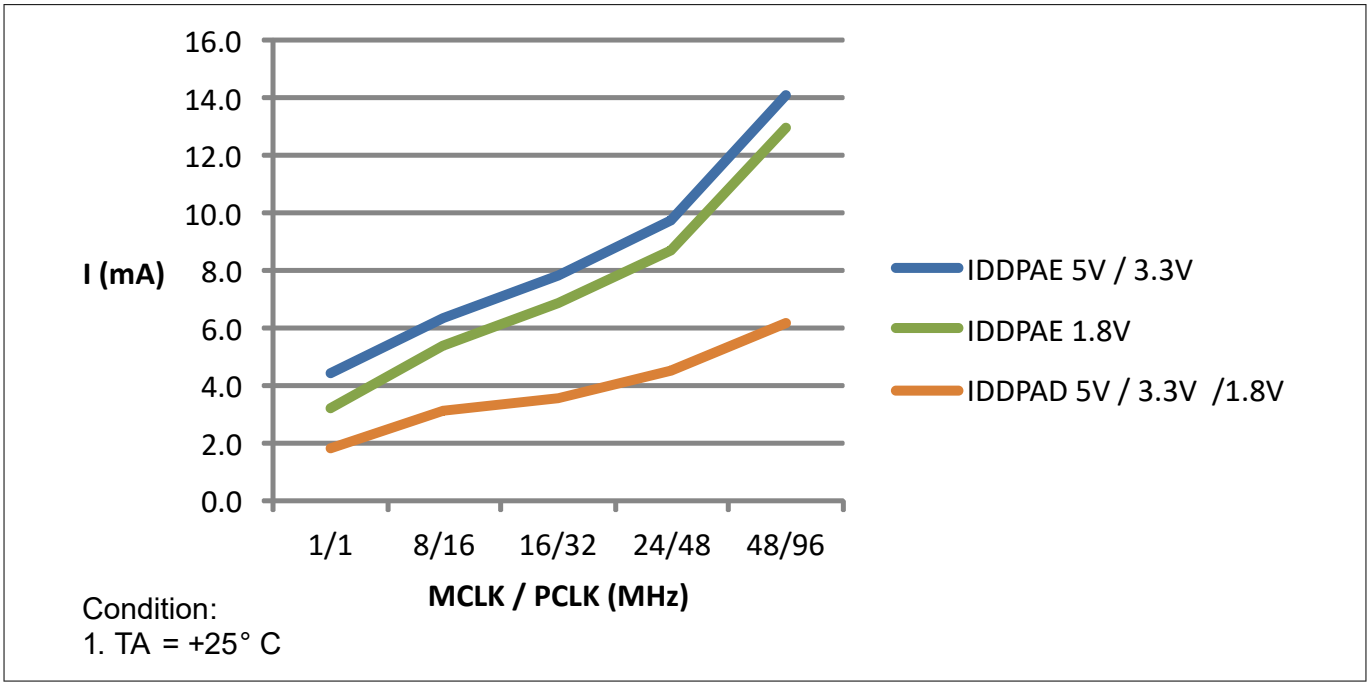

Figure 17 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

Figure 18 shows typical graphs for sleep mode current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.

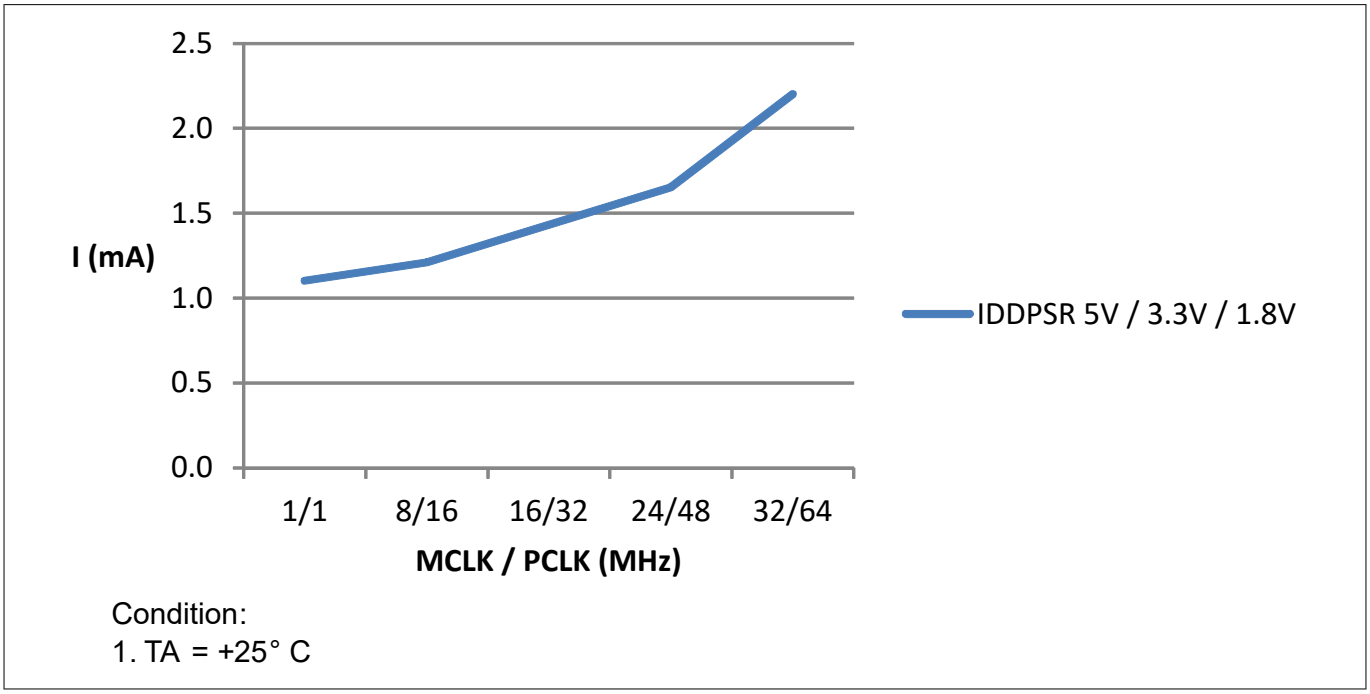

Figure 18 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current I_{DDPSD} over supply voltage V_{DDP} for different clock frequencies

Table 20 provides the active current consumption of some modules operating at 5 V power supply at 25°C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 20 Typical Active Current parameter table

Active Current Consumption	Symbol	Limit Values	Unit[32]	Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	4.14	mA	Modules including Core, SCU, PORT, memories, ANATOP[33]
VADC and SHS	I_{ADCDDC}	3.73	mA	Set CGATCLR0.VADC to 1[34]
USICx	$I_{USIC0DDC}$	1.35	mA	Set CGATCLR0.USIC0 to 1[35]
CCU4x	$I_{CCU40DDC}$	0.99	mA	Set CGATCLR0.CCU40 to 1[36]
CCU8x	$I_{CCU80DDC}$	1.00	mA	Set CGATCLR0.CCU80 to 1[37]
POSIFx	$I_{PIF0DDC}$	1.05	mA	Set CGATCLR0.POSIF0 to 1[38]
LEDTSx	$I_{LTSxDDC}$	1.14	mA	Set CGATCLR0.LEDTSx to 1[39]
BCCU0	$I_{BCCU0DDC}$	0.29	mA	Set CGATCLR0.BCCU0 to 1[40]
MATH	$I_{MATHDDC}$	0.50	mA	Set CGATCLR0.MATH to 1[41]
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1[42]
RTC	I_{RTCDDC}	0.01	mA	Set CGATCLR0.RTC to 1[43]
MultiCAN	$I_{MCANDDC}$	1.38	mA	Set CGATCLR0.MCAN0 to 1[44]

32 Measurement is performed in steps of 1MHz of MCLK/PCLK and the possible maximum module/counter/timer frequency generated from the module prescaler

33 Baseload current is measured with device running in user mode, MCLK=PCLK=48 MHz, with an endless loop in the flash memory. The default clock setting upon reset is 8MHz and measurement is done based on steps of 1MHz. The clock to the modules stated in CGATSTAT0 are gated.

34 Active current is measured with: module enabled, MCLK=48 MHz, running in auto-scan conversion mode

35 Active current is measured with: module enabled, each of the 2 USIC channels sending alternate messages at 57.6 kbaud every 200 ms

36 Active current is measured with: module enabled, MCLK=PCLK=48 MHz, 1 CCU4 slice for PWM switching at 20kHz with duty cycle varying at 10%-90%, 1 CCU4 slice in capture mode for reading period and duty cycle

37 Active current is measured with: module enabled, MCLK=PCLK=48 MHz, 3 CCU8 slices with PWM frequency at 20kHz and a period match interrupt used to toggle duty cycle between 10% and 90%

38 Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96 MHz, hall sensor mode

39 Active current is measured with: module enabled, MCLK=48 MHz, 1 LED column, 6 LED/TS lines, Pad Scheme A with large pad hysteresis config, time slice duration = 1.048 ms

40 Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96MHz, FCLK=0.8 MHz, Normal mode (BCCU clock = FCLK/4), 4 BCCU Channels with packers enabled and 1 Dimming Engine, change color or dim every 1s

41 Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96 MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11

42 Active current is measured with: module enabled, MCLK=48 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1 s

43 Active current is measured with: module enabled, MCLK=48 MHz, Periodic interrupt enabled

44 Active current is measured with: module enabled, MCLK=48 MHz, running at 20 MHz baudrate generator, 1 node activated, 1 transmit and 1 receive object active.

4.3 AC characteristics

4.3.1 Testing Waveforms

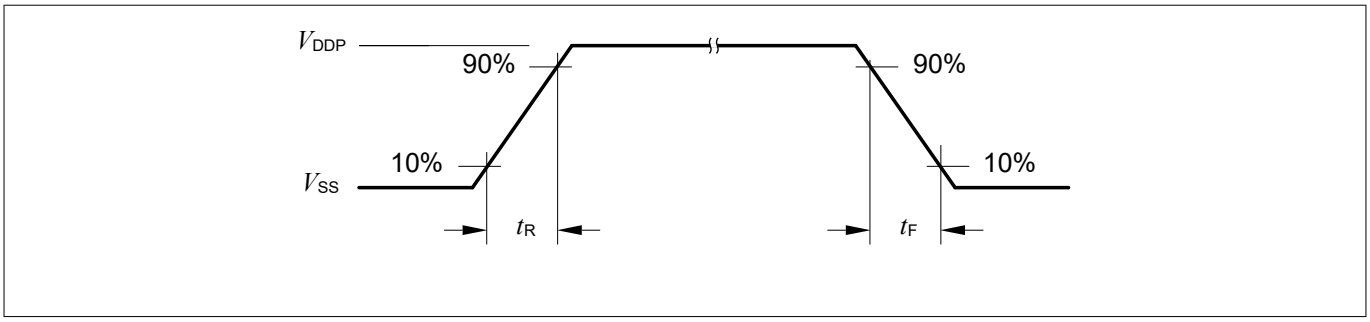

Figure 19 Rise/Fall Time Parameters

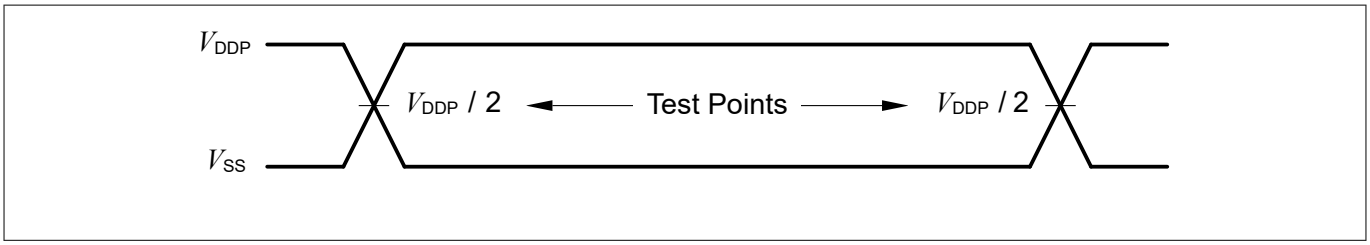

Figure 20 Testing Waveform, Output Delay

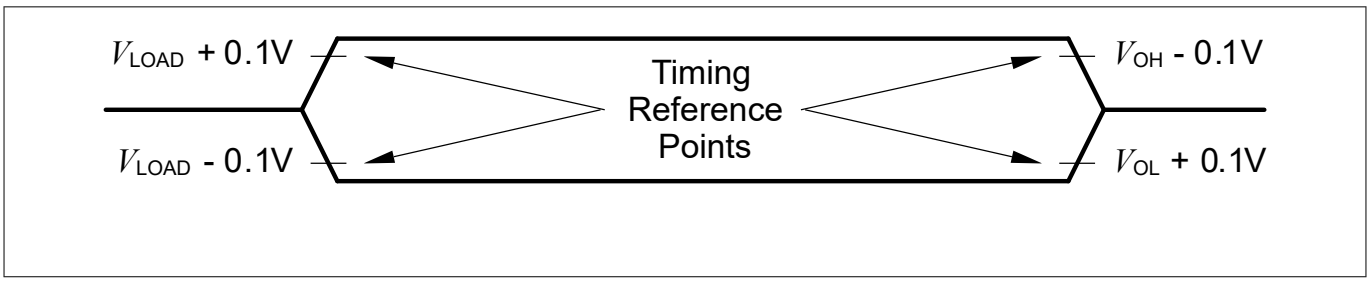

Figure 21 Testing Waveform, Output High Impedance

4.3.2 Power-Up and Supply Threshold Characteristics

This chapter provides the characteristics of the supply threshold for the controller.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DD} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 21 Power-Up and Supply Threshold Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
V_{DD} ramp-up time	t_{RAMPUP} SR	V_{DD}/ $S_{VDDrise}$	–	10^7	µs	
V_{DD} slew rate	S_{VDDOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDD10} SR	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DD}
	$S_{VDDrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDfall}$[45] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[46]
V_{DD} prewarning voltage	V_{DDPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B
V_{DD} brownout reset voltage	V_{DDBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
V_{DD} voltage to ensure defined pad states	V_{DDA} CC	–	1.0	–	V	
Start-up time from power-on reset	t_{SSW} CC	–	260	–	µs	Time to the first user code instruction[47]
Start-up time to PWM on	t_{PWMON} CC	5.2	-	360	ms	Time to PWM enabled

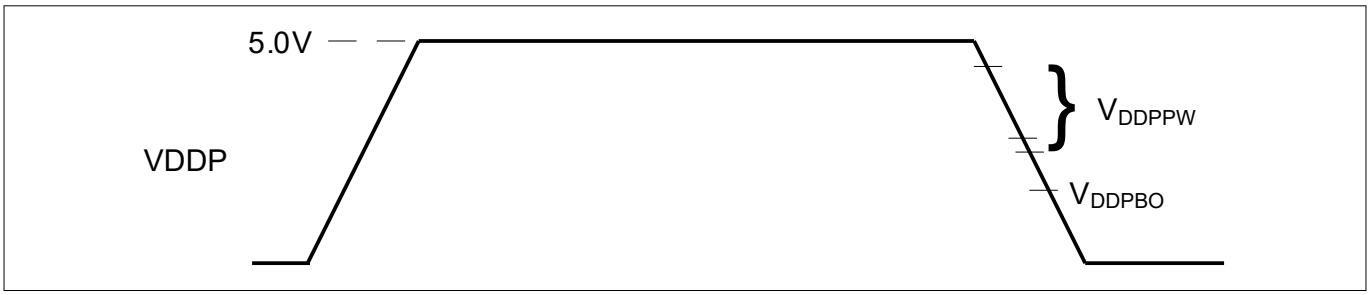

Figure 22 Supply Threshold Parameters

45 A capacitor of at least 100 nF has to be added between VDD and VSS to fulfill the requirement as stated for this parameter.
46 Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.
47 This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 48 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

4.3.3 On-Chip Oscillator Characteristics

Table 22 provides the characteristics of the 96 MHz digital controlled oscillator DCO1. The DCO1 is used as the time base during normal operation.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 22 96 MHz DCO1 Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Nominal frequency	f_{NOM} CC	-	96	-	MHz	under nominal conditions after trimming
Accuracy with adjustment algorithm [48] based on temperature sensor	Δf_{LTTS} CC	-0.6	–	+0.6	%	with respect to f_{NOM}(typ), T_A from 0°C to 105°C
		-1.9	–	+1.0	%	with respect to f_{NOM}(typ), T_A from -25 °C to 105°C
		-2.6	–	+1.3	%	with respect to f_{NOM}(typ), T_A from -40° C to 105 °C
Accuracy	Δf_{LT} CC	-1.7	–	+3.4	%	with respect to f_{NOM}(typ), T_A from 0 ° C to 85 °C
		-3.9	–	+4.0	%	with respect to f_{NOM}(typ), T_A from -40° C to 105 °C

Table 23 provides the characteristics of the 32 kHz digital controlled oscillator used internally as a secondary clock source for the internal watchdog.

Table 23 32 kHz DCO2 Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Nominal frequency	f_{NOM} CC	-	32.75	-	kHz	under nominal conditions[49] after trimming
Accuracy	Δf_{LT} CC	-1.7	–	+3.4	%	with respect to f_{NOM}(typ), T_A from 0 ° C to 85 °C
		-3.9	–	+4.0	%	with respect to f_{NOM}(typ), T_A from -40° C to 105 °C

48 MCE version newer or equal to V1.03.00, clock adjustment algorithm for improved accuracy enabled
49 The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25°C.

4.3.4 Embedded microcontroller

4.3.4.1 Power-up and supply threshold characteristics

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DD} is outside its operating range. The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 24 Power-up and supply threshold characteristics

V_{DD} = 5 V, T_A = 25 °C unless specified otherwise. C = 100 nF between V_{DD} and V_{SS}.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DD} ramp-up time	t_{RAMPUP}	---	---	10^7	µs	---
V_{DD} slew rate	S_{VDDPOP}	---	---	0.1	V/µs	Slope during normal operation
	S_{VDDP10}	---	---	10	V/µs	Slope during fast transient within +/-10% of V_{DD}
	$S_{VDDPrise}$	---	---	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfail}$	---	---	0.25	V/µs	Slope during supply falling out of the +/-10% limits
V_{DD} prewarning voltage	V_{DDPPW}	2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B
V_{DD} brownout reset voltage	V_{DDPBO}	1.55	1.62	1.75	V	Calibrated, before user code starts running
V_{DD} voltage to ensure defined controller pad states	V_{DDPPA}	---	1.0	---	V	---
Start-up time from power on reset	t_{SSW}	---	260	---	µs	Time to the first user code instruction

4.3.4.2 Internal oscillator AC characteristics

Table 25 96 MHz DCO1 oscillator characteristics

V_{DD} = 5 V, T_A = 25 °C unless specified otherwise.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Nominal frequency and accuracy	$DCO1f_{NOM}$	---	96	---	MHz	T_A = 25 °C
		-1.7	---	3.4	%	0 °C < T_A < 85 °C
		-3.9	---	4.0	%	-40 °C < T_A < 105 °C

Table 26 32 kHz DCO2 oscillator characteristics

V_{DD} = 5 V, T_A = 25 °C unless specified otherwise.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Nominal frequency and accuracy	$DCO2f_{NOM}$	---	32.75	---	kHz	T_A = 25 °C
		-1.7	---	3.4	%	0 °C < T_A < 85 °C
		-3.9	---	4.0	%	-40 °C < T_A < 105 °C

Note: These parameters are not subject to production test, but verified by design and/or characterization.

4.3.4.3 Serial wire debug (SWD) port timing

Table 27 SWD interface timing parameters

V_{DD} = 5 V, T_A = 25 °C unless specified otherwise.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SWDCLK high-time	t_1	50	---	500000	ns	---
SWDCLK low-time	t_2	50	---	500000	ns	---
SWDIO input setup to SWDCLK rising edge	t_3	10	---	---	ns	---
SWDIO input hold after SWDCLK rising edge	t_4	10	---	---	ns	---
SWDIO output valid time after SWDCLK rising edge	t_5	---	---	68	ns	C_L = 50 pF
SWDIO output hold time from SWDCLK rising edge	t_6	4	---	---	ns	---

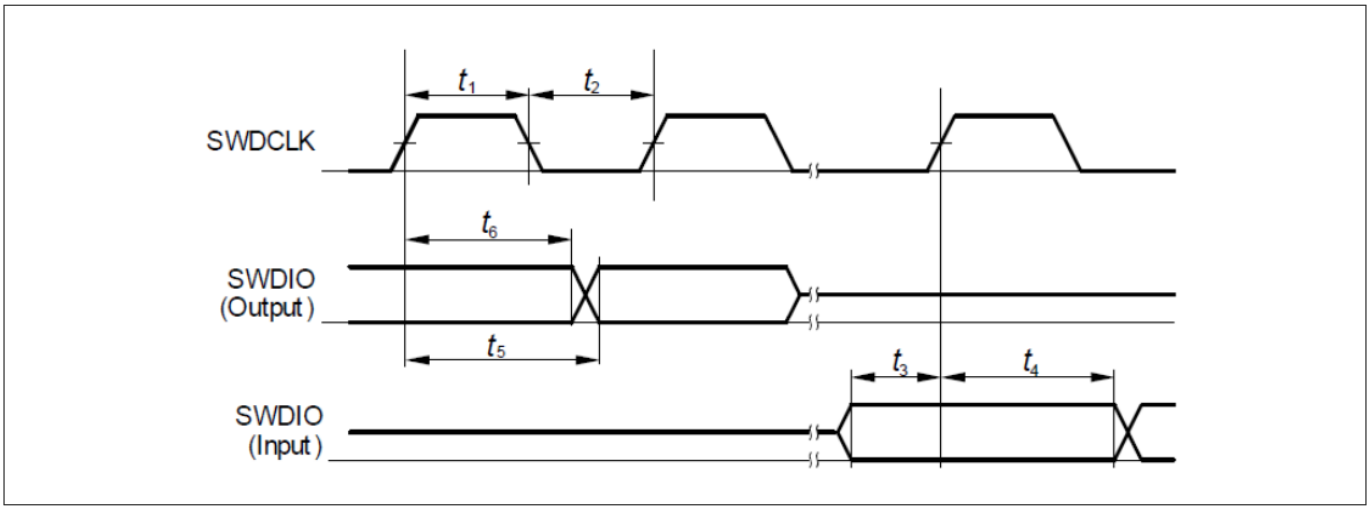

Figure 23 SWD timing

4.3.4.4 SPD timing requirements

The SPD protocol based tool interface access allows debugging the system using a single pin only. The bit frequency is 2 MHz and allows an effective SWD telegram of 1.4 Mbits/s. The protocol is very robust against clock deviations between tool and device.

The optimum SPD decision time between 0B and 1B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 28 Optimum number of sample clocks for SPD

V_{DD} = 5 V, T_A = 25 °C unless specified otherwise.

Sample frequency	Sampling factor	Sample clocks 0_B	Sample clocks 1_B	Effective decision time	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- frequency deviation of the sample clock is +/- 5%
- effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

4.3.4.5 Synchronous serial interface (USIC SPI) timing

Table 29 USIC SPI master mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	4/MCLK	---	---	ns	---
Slave select output SELO active to first SCLKOUT transmit edge	t_1	t_{CLK}/2-28	---	---	ns	---
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	0	---	---	ns	---
Data output DOUT[3:0] valid time	t_3	-28	---	---	ns	---
Receive data input DX0/ DX[5:3] setup time to SCLKOUT receive edge	t_4	75	---	---	ns	---
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	0	---	---	ns	---

Table 30 USIC SPI slave mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	4/MCLK	---	---	ns	---
Select input DX2 setup to first clock input DX1 transmit edge	t_{10}	16	---	---	ns	---
Select input DX2 hold after last clock input DX1 receive edge	t_{11}	17	---	---	ns	---
Receive data input DX0/ DX[5:3] setup time to shift clock receive edge	t_{12}	21	---	---	ns	---
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge	t_{13}	15	---	---	ns	---
Data output DOUT[3:0] valid time	t_{14}	---	---	71	ns	---

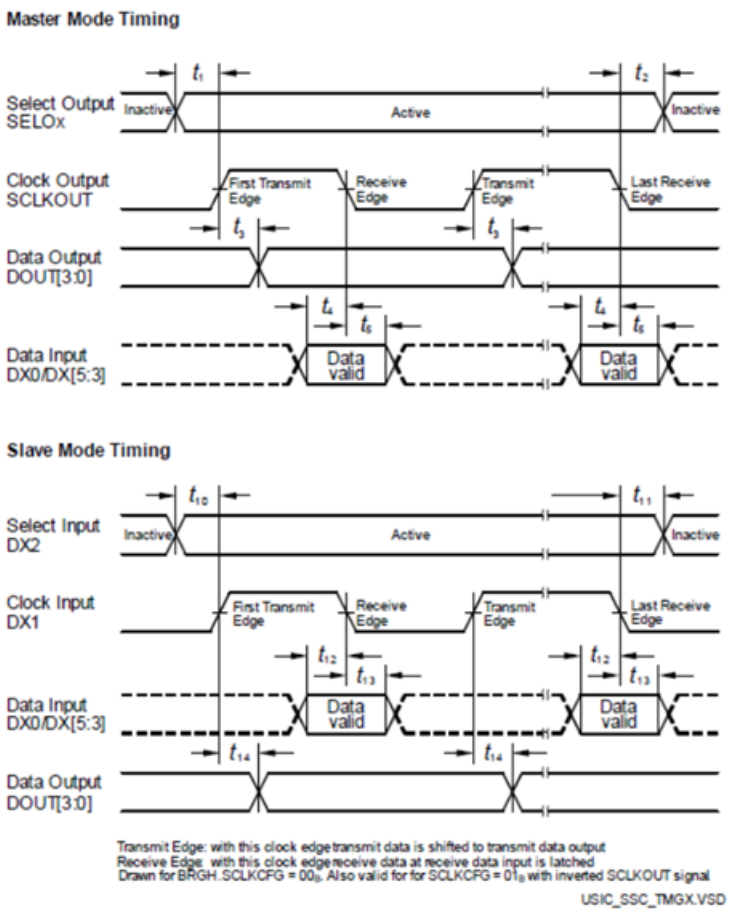

Figure 24 USIC – SPI master/slave mode timing

4.3.4.6 Inter-IC (I2C) interface timing

Table 31 USIC I2C standard mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	---	---	300	ns	---
Rise time of both SDA and SCL	t_2	---	---	1000	ns	---
Data hold time	t_3	0	---	---	µs	---
Data set-up time	t_4	250	---	---	ns	---
LOW period of SCL clock	t_5	4.7	---	---	µs	---
HIGH period of SCL clock	t_6	4.0	---	---	µs	---
Hold time for (repeated) START condition	t_7	4.0	---	---	µs	---
Set-up time for repeated START condition	t_8	4.7	---	---	µs	---

(table continues...)

Table 31 (continued) USIC I2C standard mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Set-up time for STOP condition	t_9	4.0	---	---	µs	---
Bus free time between a STOP and START condition	t_{10}	4.7	---	---	µs	---
Capacitive load for each bus line	C_b	---	---	400	pF	---

Table 32 USIC I2C fast mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	20 + 0.1 x C_b	---	300	ns	---
Rise time of both SDA and SCL	t_2	20 + 0.1 x C_b	---	300	ns	---
Data hold time	t_3	0	---	---	µs	---
Data set-up time	t_4	100	---	---	ns	---
LOW period of SCL clock	t_5	1.3	---	---	µs	---
HIGH period of SCL clock	t_6	0.6	---	---	µs	---
Hold time for (repeated) START condition	t_7	0.6	---	---	µs	---
Set-up time for repeated START condition	t_8	0.6	---	---	µs	---
Set-up time for STOP condition	t_9	0.6	---	---	µs	---
Bus free time between a STOP and START condition	t_{10}	1.3	---	---	µs	---
Capacitive load for each bus line	C_b	---	---	400	pF	---

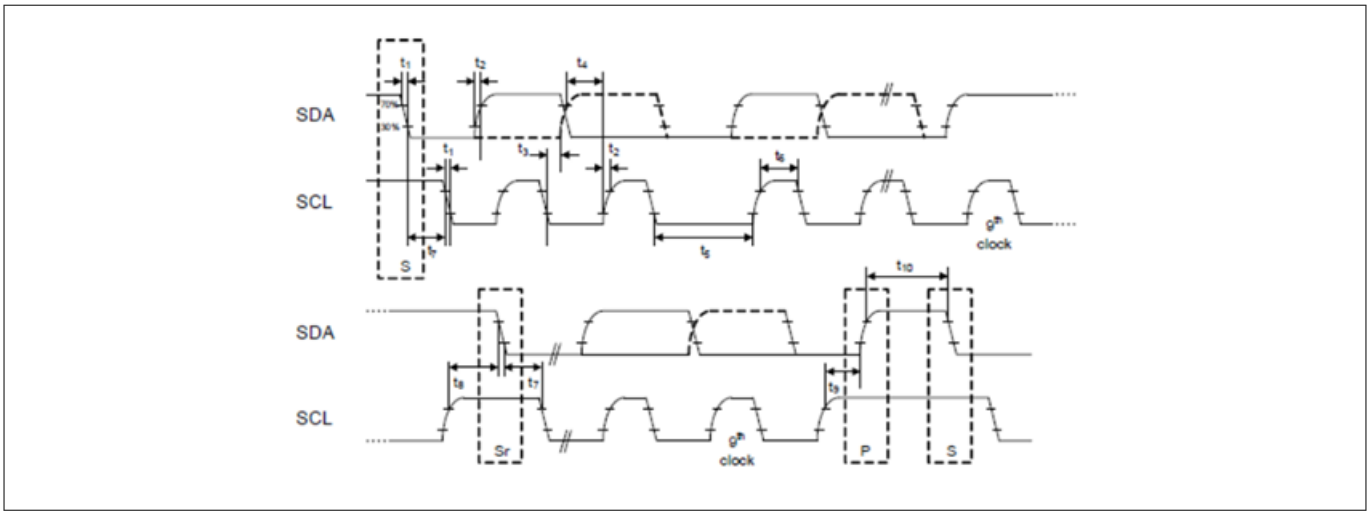

Figure 25 USIC I2C timing

4.4 Motor Control Parameters

The following values are given for reference only. Concrete parameters are defined in the iMOTION™ Motion Control Engine (MCE) software.

4.4.1 PWM Characteristics

Table 33 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Motor PWM Frequency[50)]	f_{PWM}	5	16		kHz	

4.4.2 Current Sensing

Table 34 Motor Current Sensing

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input range	I_{PWM}	V_{SS}-0.05	-	V_{DD}+0.05	V	
Configurable analog gain		-	1/ 3/ 6/ 12	-		
Itrip input range	$I_{PWMTRIP}$	V_{SS}-0.05	-	V_{DD}+0.05	V	
Itrip offset		-	±8	-	mV	
Input capacitance	C_{REF}	-	-	10	pF	REFU, REFV, REFW capacitor

50 Actual min. and max. limits defined in resp. software version

4.4.3 Fault Timing

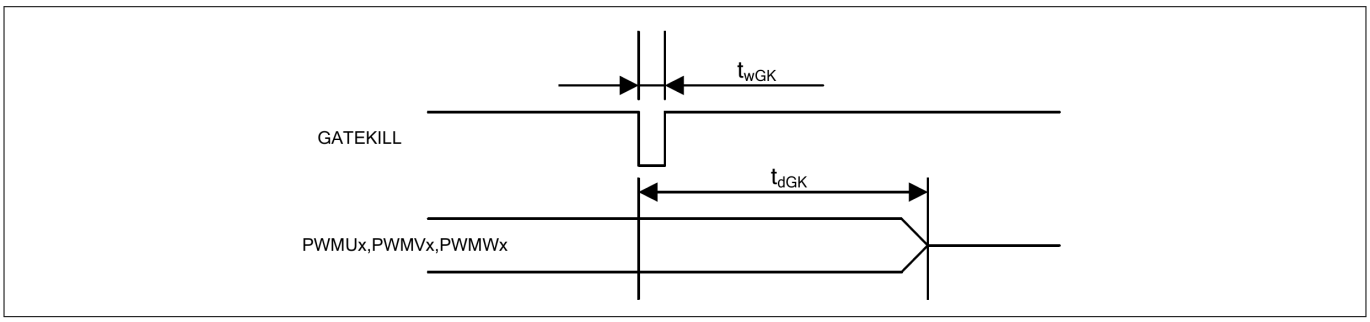

Figure 26 Fault timing

Table 35 Gatekill timing

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
GK pulse width	t_{wGK}	1	-	-	µs	
GK input to PWM shutoff	t_{GK}	-	1.3	-	µs	
Motor Fault reset timing	t_{RESET}	-	1.84	-	ms	fault reset command via UART to PWM reactivation
MCE digital ITRIP filter window	t_{PWMOFF}	0.075	1.0	10	µs	Configurable in software

Note: The ITRIP filter window must be configured according to the rated short circuit withstand time of the respective power stage taking into consideration any delay in external circuitry. For iMOTION™ devices with integrated power stage the value is specified in the Absolute maximum ratings of the device.

4.5 Power Factor Correction (PFC) parameters

The parameters specified for the power factor correction only refer to products that have the respective control algorithm integrated. The PFC switching frequency is configurable and the range depends on the concrete firmware version.

4.5.1 Boost PFC characteristics

Table 36 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
PFC frequency	f_{PFC}	-	20	50	kHz	MCE rev. 1.3
		-	40	120	kHz	MCE rev. 5.1

4.5.2 Totem Pole PFC characteristics

Table 37 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
PFC frequency	f_{PFC}	-	40		kHz	Max defined by SW

4.5.3 PFC Current Sensing

The current sensing specification applies to both PFC algorithms, boost mode and totem pole.

Table 38 PFC Current Sensing

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input range	I_{PFC}	V_{SS}- 0.05	-	V_{DD}+ 0.05	V	V_{DD}= 3.3 or 5.0 V
Configurable analog gain		-	1/ 3/ 6/ 12	-		
PFC Itrip input range	$I_{PFCTRIP}$	V_{SS}-0.05	-	V_{DD}+ 0.05	V	V_{DD}= 3.3 or 5.0 V
Itrip offset		-	± 3	-	mV	Input voltage difference > 200mV
Input capacitance	C_{REF}	-	-	10	pF	PFCREF capacitor

4.5.4 PFC Fault Timing

Table 39 PFC Fault timing

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Itrip to PFC PWM shutoff	t_{PFCOFF}	-	1.18	-	µs	

(table continues...)

Table 39 (continued) PFC Fault timing

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
PFC fault reset timing	t_{RESET}	-	1.0	-	ms	fault reset command via UART to PWM reactivation

4.6 Device Interfaces

iMOTION™ devices provide several interfaces to either control the motor drive in the application or report back its status. The availability of a specific interface depends upon the concrete device chosen as well as the version of the Motion Control Engine (MCE) applied. The following sections and tables specify these interfaces as well as the respective limits. The configuration settings for these interfaces are described in the MCE Reference Manual.

The IMC300 series has an internal interface between the MCE and the embedded microcontroller which is based an a high speed serial link. The driver for the respective protocol is provided in source code. For the specification please refer to the Reference Manual.

Note: These parameters are not subject to production test, but verified by design and/or characterization. Operating conditions apply.

4.6.1 UART Interface

The UART interface is configured as given below.

Table 40 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
UART baud rate		1200	57600	-	Bps	
UART mode		-	8-N-1	-		data-parity-stop bit
UART sampling filter period [51)]	$T_{UARTFIL}$	-	1/16	-	T_{BAUD}	

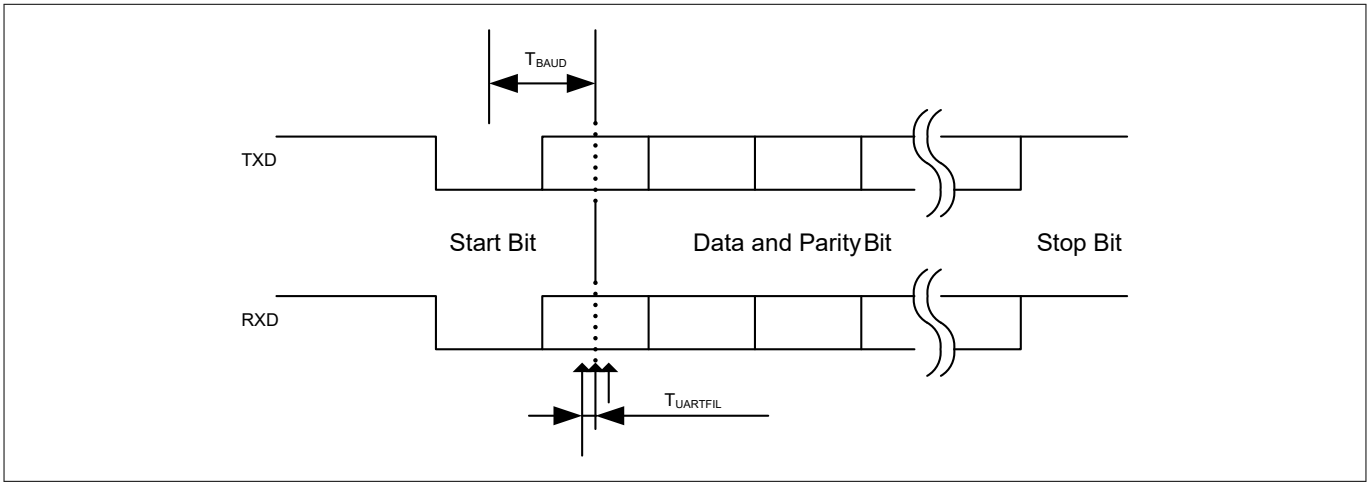

Figure 27 UART timing

51 Each bit including start and stop bit is sampled three times at center of a bit at an interval of 1/16 T_{BAUD}. If three sampled values do not agree, then UART noise error is generated.

4.6.2 Over Temperature Input

The over temperature input can be used to continuously monitor an external temperature sensor like an NTC.

Table 41 Over Temperature Input

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Over Temperature to PWM shutdown	t_{OT}		1.0	2.1	ms	

4.6.3 Pulse Output

The IMC300 series can generate a square wave pulse output in sync with the motor rotation which can be used to monitor the motor speed. The number of pulses to be generated for a full rotation can be configured.

Table 42 Pulse Output

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Pulses per Rotation	*PPR*	4	-	24		
Pulse duty cycle	t_{PPR}	-	50	-	%	

4.6.4 LED Output

The IMC300 series provides an output that can be connected to an LED to give a visual indication of the status of the motor drive.

Table 43 LED Output

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Fault to LED delay	$t_{LEDFAULT}$	-	53	-	ms	
Fault reset to LED delay	$t_{LEDRESET}$	-	1.84	-	ms	
LED blinking frequency	f_{LED}	1		1000	Hz	
LED blinking duty cycle	t_{LED}	5		95	%	

5 Device and package specifications

5.1 Quality declaration

Table 44 Quality Parameters

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR		–	2000	V	ANSI/ESDA/JEDEC-JS-001
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR		–	500	V	ANSI/ESDA/JEDEC-JS-002
Moisture sensitivity level	MSL CC		–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR		–	260	°C	JEDEC J-STD-020D

5.2 SBSL and Chip-IDs

The table below gives the IDs for the individual devices in the IMC300 family. Depending upon the mode either the SBSL-ID (secure boot loader) or the Chip-ID should be used to identify the device. For details refer to the Reference Manual or the iMOTION™ Programming Manual.

Table 45 SBSL-IDs and Chip-IDs

Product Type	Package	Chip-ID	SBSL-ID
IMC301A-F048 (MCE)	LQFP-48	0x1B010006	026add3f080ad5abfb67af2271ea4973
IMC301A-F048 (MCU)	LQFP-48	0x13011006	-
IMC301A-F064 (MCE)	LQFP-64	0x1B01000B	0207810c349410e8be51722b81520cf8
IMC301A-F064 (MCU)	LQFP-64	0x1301100B	-
IMC302A-F048 (MCE)	LQFP-48	0x1B020006	024747b4b61060cf95f7b14a05b1decc
IMC302A-F048 (MCU)	LQFP-48	0x13021006	-
IMC302A-F064 (MCE)	LQFP-64	0x1B02000B	0216ebe1d4cc0767684bacceefae29b2
IMC302A-F064 (MCU)	LQFP-64	0x1302100B	-

5.3 Thermal Characteristics

Table 46 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Thermal resistance Junction-Ambient[52]	$R_{\Theta JA}$ CC	-	t.b.d.	K/W	PG-LQFP-48-11
		-	66.7	K/W	PG-LQFP-64-29

Note: For electrical reasons, it is required to connect an exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

When operating the IMC300 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by

$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$P_{INT} = V_{DD} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as

$P_{IOSTAT} = \Sigma((V_{DD} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL} I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DD}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

52 Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad of VQFN soldered.

5.4 Package Outlines

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: www.infineon.com/packages

5.4.1 Package Outline PG-LQFP-48-11

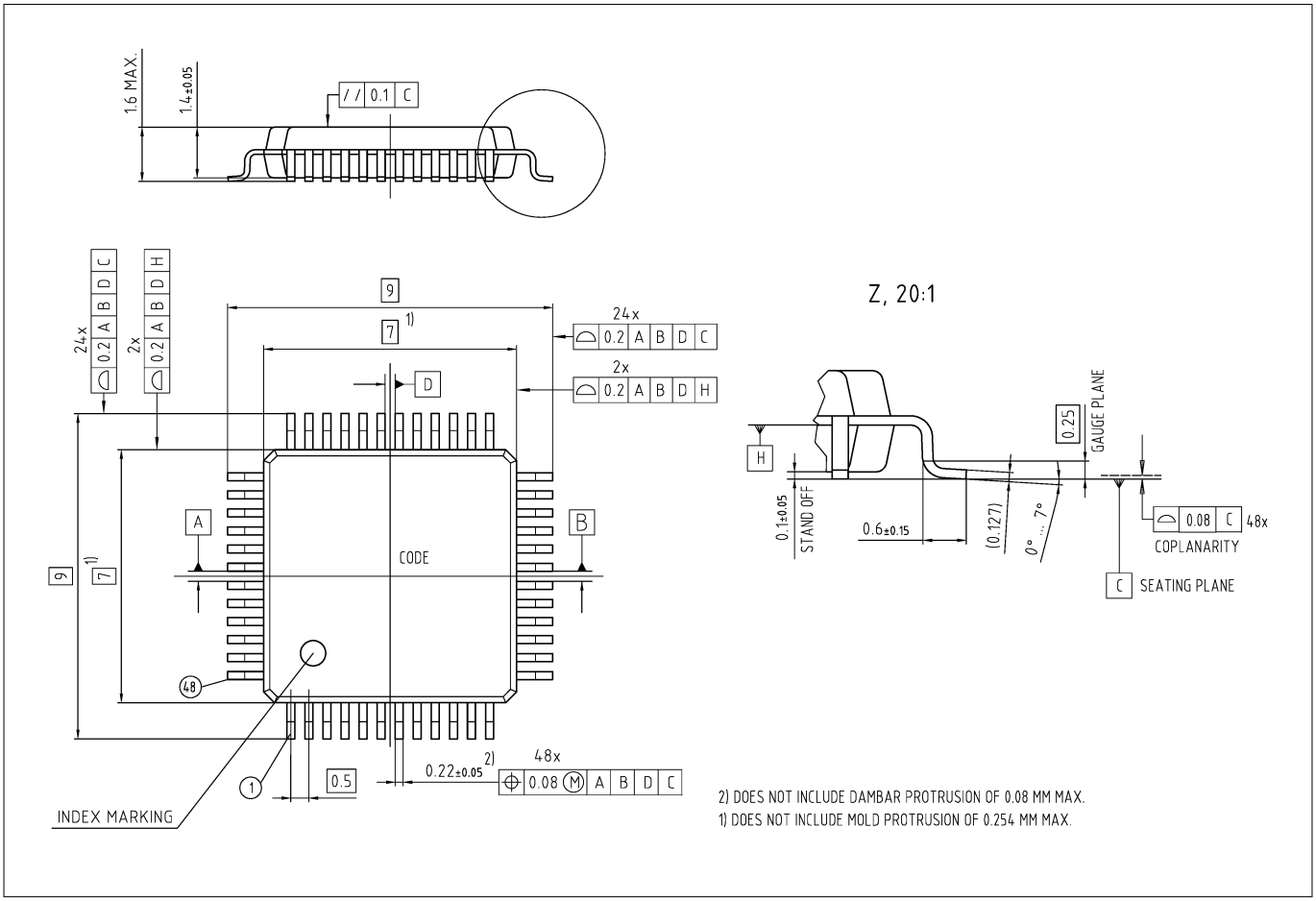

Figure 28 PG-LQFP-48-11

5.4.2 Package Outline PG-LQFP-64-29

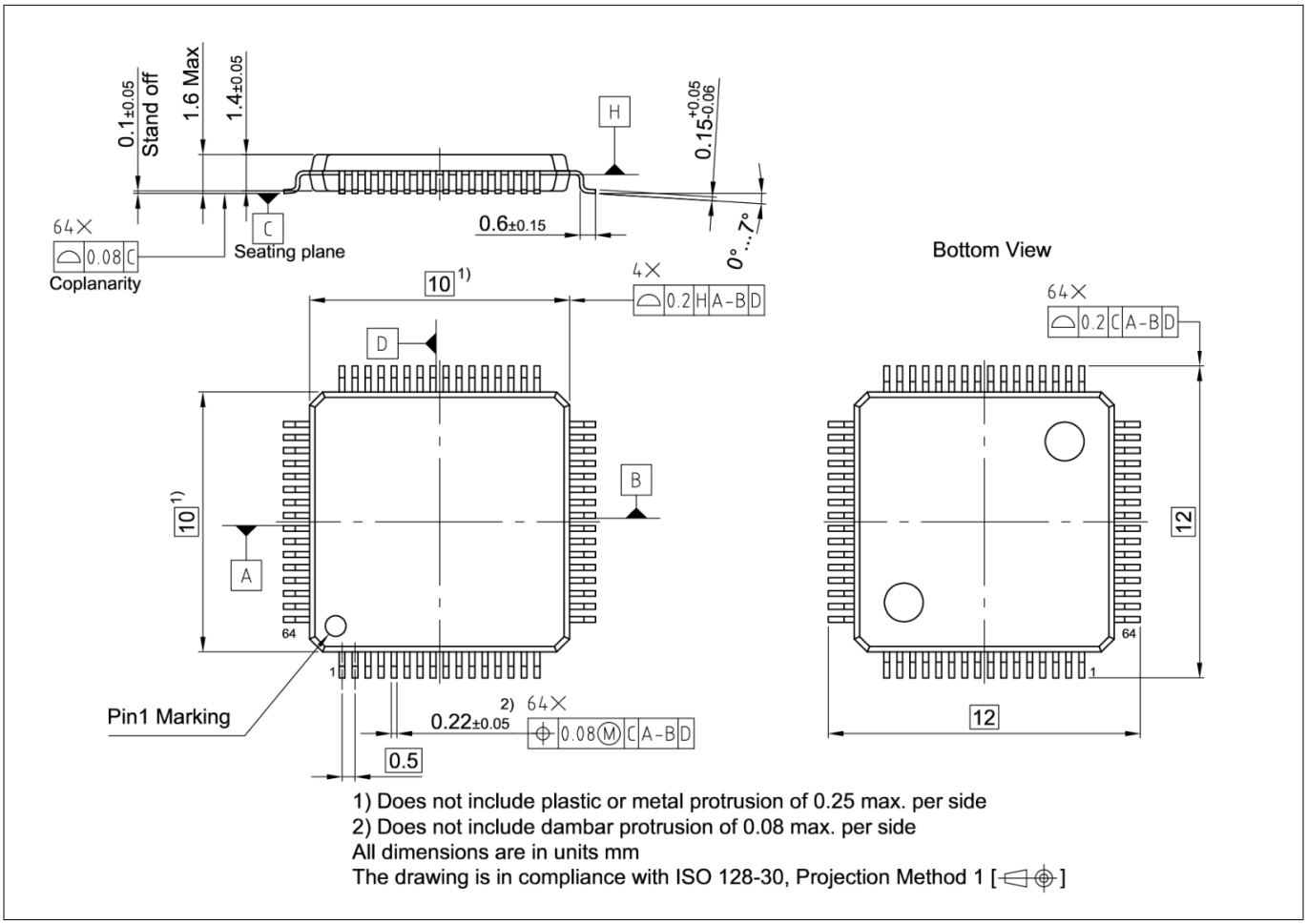

Figure 29 PG-LQFP-64-29

5.5 Part marking information

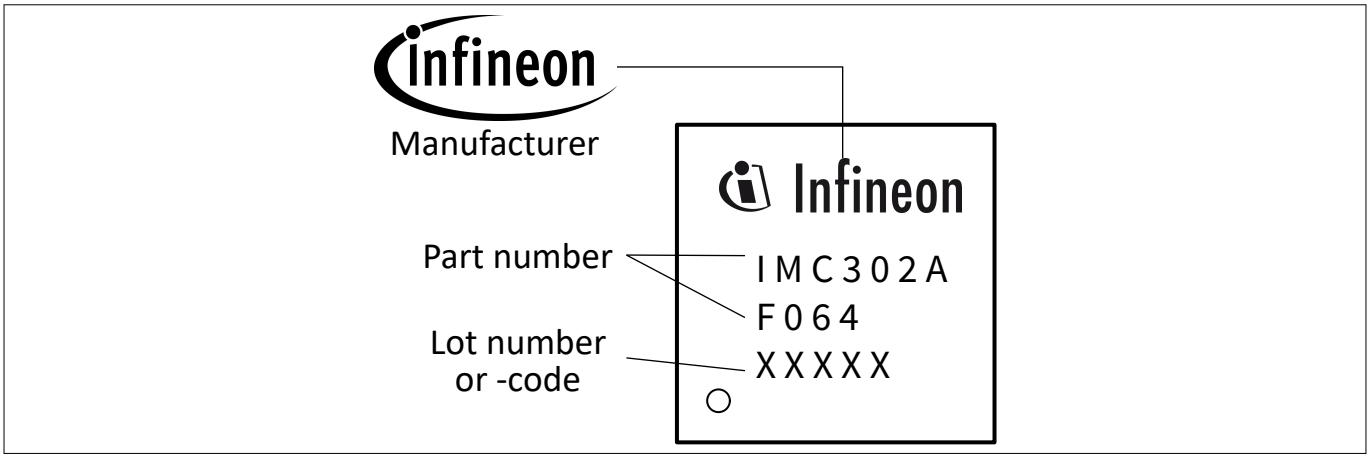

Figure 30 Part marking

6 Revision history

Document version	Date of release	Description of changes
1.0	2019-12-12	• Initial version
1.1	2020-05-11	• Figure and table numbers updated • Table 1 (Pin List) updated • Pin configuration drawings updated • Added DCO accuracy with calibration • Increased maximum motor PWM frequency up to 40 kHz • Application schematics drawings in section 3 updated • Section 5 (Quality Declaration) updated
1.2	2020-10-20	• Table 1 (Pin List) updated
1.3	2023-09-18	• New features pin mapping of IR added

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