THE DATASHEET OF

AD7984BCPZ-RL

18-Bit, 1.33 MSPS PulSAR 10.5 mW ADC in MSOP/LFCSP

Data Sheet **AD7984**

FEATURES

High performance
- **True differential analog input range: ±V_{REF}**
  - **0 V to V_{REF} with V_{REF} between 2.9 V to 5 V**
  - **Easy to drive with the ADA4941**
- **Throughput: 1.33 MSPS**
  - **Zero latency architecture**
- **18-bit resolution with no missing codes**
- **INL: ±2.25 LSB maximum**
- **Dynamic range: 99.7 dB, V_{REF} = 5 V**
- **SNR: 98.5 dB at f_{IN} = 1 kHz, V_{REF} = 5 V**
- **THD: −110.5 dB at f_{IN} = 1 kHz, V_{REF} = 5 V**
- **SINAD: 97.5 dB at f_{IN} = 1 kHz, V_{REF} = 5 V**

Low power dissipation
- **Single-supply 2.5 V operation with 1.8 V/2.5 V/3 V/5 V logic interface**
- **5.3 mW at 1.33 MSPS (VDD only)**
- **10.5 mW at 1.33 MSPS (total)**
- **80 µW at 10 kSPS**

Proprietary serial interface
- **SPI/QSPI/MICROWIRE™/DSP compatible**

Ability to daisy-chain multiple ADCs and busy indicator
10-lead MSOP and 10-lead, 3 mm × 3 mm LFCSP
Wide operating temperature range: −40°C to +85°C

APPLICATIONS

Automated test equipment
Data acquisition systems
Medical instruments
Machine automation

APPLICATION DIAGRAM

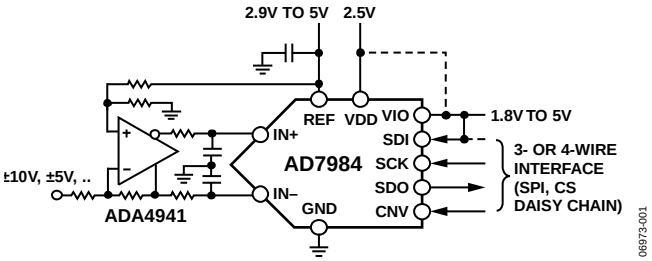


Figure 1.

GENERAL DESCRIPTION

The AD7984[1] is an 18-bit, successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, VDD. It contains a low power, high speed, 18-bit sampling ADC and a versatile serial interface port. On the CNV rising edge, the AD7984 samples the voltage difference between the IN+ and IN− pins. The voltages on these pins usually swing in opposite phases between 0 V and V_{REF}. The reference voltage, REF, is applied externally and can be set independent of the supply voltage, VDD.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single 3-wire bus and provides an optional busy indicator. It is compatible with 1.8 V, 2.5 V, 3 V, and 5 V logic, using the separate VIO supply.

The AD7984 is available in a 10-lead MSOP or a 10-lead LFCSP with operation specified from −40°C to +85°C.

[1] Protected by U.S. Patent 6,703,961.

Table 1. MSOP, LFCSP 16-/18-/20-Bit Precision SAR ADCs and SAR ADC-Based µModule Data Acquisition Solutions

Type	≤100 kSPS	≤250 kSPS	≤500 kSPS	≤1000 kSPS	≤2000 kSPS	µModule Data Acquisition Solutions
Differential						
20-Bit			AD4022[1]	AD4021[1]	AD4020[1]	
18-Bit	AD7989-1[1]	AD7691[1]	AD4011[1]	AD4007[1]	AD4003[1]	
			AD7690[1]	AD7982[1]		
			AD7989-5[1]	AD7984[1]		
16-Bit	AD7684	AD7687[1]	AD7688[1]	AD4005[1]	AD4001[1]	
			AD7693[1]	AD7915[1]		
			AD7916[1]			
Pseudo Differential						
18-Bit			AD4010[1]	AD4006[1]	AD4002[1]	
16-Bit	AD7988-1[1]	AD7685[1]	AD4008[1]	AD4004[1]	AD4000[1]	ADAQ7980
	AD7680	AD7694	AD7988-5[1]	AD7980[1]		ADAQ7988
	AD7683		AD7686[1]	AD7983[1]		

[1] Pin for pin compatible.

Rev. C **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

7/2020—Rev. B to Rev. C

Changes to Features Section, Applications Section, and Table 1 ... 1
Changes to Specifications Section and Table 2 ... 3
Changes to Power Supplies Parameter, Table 3 ... 4
Changes to Timing Specifications Section and Table 4 ... 5
Added Table 5; Renumbered Sequentially ... 6
Deleted Figure 3; Renumbered Sequentially ... 6
Changes to Table 6 ... 7
Added Thermal Resistance Section and Table 7 ... 7
Changes to Figure 22 ... 14
Changes to Driver Amplifier Choice Section and Table 10 ... 15
Changes to Single-to-Differential Driver Section, Voltage Reference Input Section, and Power Supply Section ... 16

7/2014—Rev. A to Rev. B

Changed QFN (LFCSP) to LFCSP ... Throughout
Changes to Features Section and Table 1 ... 1
Added Patent Note, Note 1 ... 1
Changes to Power Supply Section ... 15
Changes to Evaluating the AD7984 Performance Section ... 23
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 24

8/2010—Rev. 0 to Rev. A

Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 24

11/2007—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, REF = 5 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage	IN+, IN−	−0.1		V_{REF} + 0.1	V
Common-Mode Input Range	IN+, IN−	$V_{REF} \times 0.475$	$V_{REF} \times 0.5$	$V_{REF} \times 0.525$	V
Analog Input CMRR	f_{IN} = 450 kHz		67		dB[1]
Leakage Current at 25°C	Acquisition phase		200		nA
Input Impedance		See the Analog Inputs section			
ACCURACY					
No Missing Codes		18			Bits
Differential Linearity Error		−1		+1.5	LSB[2]
Integral Linearity Error		−2.25		+2.25	LSB[2]
Transition Noise			0.95		LSB[2]
Gain Error, T_{MIN} to T_{MAX}[3]		−0.075	±0.022	+0.075	% of FS
Gain Error Temperature Drift			−0.6		ppm/°C
Zero Error, T_{MIN} to T_{MAX}[3]		−700	±100	+700	µV
Zero Temperature Drift			0.3		ppm/°C
Power Supply Sensitivity	VDD = 2.5 V ± 5%		90		dB[1]
THROUGHPUT					
Conversion Rate	VIO > 2.3 V	0		1.33	MSPS
	VIO ≤ 2.3 V	0		833	kSPS
Transient Response	Full-scale step			290	ns
AC ACCURACY					
Dynamic Range	V_{REF} = 5 V		99.7		dB[1]
Signal-to-Noise, SNR	f_{IN} = 1 kHz, V_{REF} = 5 V, T_A = 25°C	96.5	98.5		dB[1]
Spurious-Free Dynamic Range, SFDR	f_{IN} = 10 kHz		112.5		dB[1]
Total Harmonic Distortion[4], THD	f_{IN} = 10 kHz		−110.5		dB[1]
Signal-to-(Noise + Distortion), SINAD	f_{IN} = 10 kHz, V_{REF} = 5 V, T_A = 25°C		98		dB[1]

[1] All specifications expressed in decibels are referred to a full-scale range (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[2] LSB means least significant bit. With the ±5 V input range, one LSB is 38.15 µV.
[3] See Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.
[4] Tested fully in production at f_{IN} = 1 kHz.

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, REF = 5 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		2.9		5.1	V
Load Current	1.33 MSPS		520		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			10		MHz
Aperture Delay			2		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}	VIO > 3 V	−0.3		+0.3 × VIO	V
V_{IH}	VIO > 3 V	0.7 × VIO		VIO + 0.3	V
V_{IL}	VIO ≤ 3 V	−0.3		+0.1 × VIO	V
V_{IH}	VIO ≤ 3 V	0.9 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 18 bits, twos complement			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD		2.375	2.5	2.625	V
VIO		1.71		5.5	V
Standby Current[1, 2]	VDD and VIO = 2.5 V		1.1		mA
Power Dissipation	1.33 MSPS throughput		10.5	14	mW
Energy per Conversion			7.9		nJ/sample
TEMPERATURE RANGE[3]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During acquisition phase.
[3] Contact an Analog Devices, Inc., sales representative for the extended temperature range.

TIMING SPECIFICATIONS

VDD = 2.37 V to 2.63 V, VIO = 2.3 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise noted. See Figure 2 for load conditions.

Table 4.

Parameter[1]	Symbol	Min	Typ	Max	Unit
Throughput Rate				1.33	MSPS
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	300		500	ns
Acquisition Time	t_{ACQ}	250			ns
Time Between Conversions	t_{CYC}	750			ns
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}				
VIO Above 4.5 V		10.5			ns
VIO Above 3 V		12			ns
VIO Above 2.7 V		13			ns
VIO Above 2.3 V		15			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO Above 4.5 V		11.5			ns
VIO Above 3 V		13			ns
VIO Above 2.7 V		14			ns
VIO Above 2.3 V		16			ns
SCK Low Time	t_{SCKL}	4.5			ns
SCK High Time	t_{SCKH}	4.5			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				9.5	ns
VIO Above 3 V				11	ns
VIO Above 2.7 V				12	ns
VIO Above 2.3 V				14	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 3 V				10	ns
VIO Above 2.3 V				15	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	5			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	2			ns
SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$			15	ns

[1] Timing parameters measured with respect to a falling edge are defined as triggered at x% VIO. Timing parameters measured with respect to a rising edge are defined as triggered at y% VIO. For VIO ≤ 3 V, x = 90 and y = 10. For VIO > 3 V, x = 70 and y = 30. The minimum V_{IH} and maximum V_{IL} are used. See the Digital Inputs Specifications in Table 2.

VDD = 2.37 V to 2.63 V, VIO = 1.71 to 2.3 V, T_A = −40°C to +125°C, unless otherwise stated. See Figure 2 for load conditions.

Table 5.

Parameter[1]	Symbol	Min	Typ	Max	Unit
Throughput Rate				833	kSPS
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	300		500	ns
Acquisition Time	t_{ACQ}	250			ns
Time Between Conversions[2]	t_{CYC}	1.2			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	22			ns
SCK Period (Chain Mode)	t_{SCK}	23			ns
SCK Low Time	t_{SCKL}	6			ns
SCK High Time	t_{SCKH}	6			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}		14	21	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}		18	40	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	5			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	10			ns
SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$			22	ns

[1] Timing parameters measured with respect to a falling edge are defined as triggered at x% VIO. Timing parameters measured with respect to a rising edge are defined as triggered at y% VIO. For VIO ≤ 3 V, x = 90 and y = 10. For VIO > 3 V, x = 70 and y = 30. The minimum V_{IH} and maximum V_{IL} are used. See the Digital Inputs Specifications in Table 2.

[2] The time required to clock out N bits of data, t_{READ}, may be greater than t_{ACQ}, depending on the magnitude of VIO. If t_{READ} is greater than t_{ACQ}, the throughput must be limited to ensure that all N bits are read back from the device.

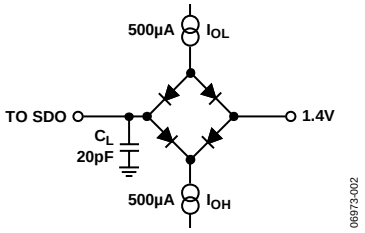


Figure 2. Load Circuit for Digital Interface Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
IN+, IN− to GND[1]	−0.3 V to V_{REF} + 0.3 V or ±130 mA
Supply Voltage	
REF, VIO to GND	−0.3 V to +6.0 V
VDD to GND	−0.3 V to +3.0 V
VDD to VIO	+3 V to −6 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperatures	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] See the Analog Inputs section for an explanation of IN+ and IN−.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 7. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
RM-10	200	44	°C/W
CP-10-9	48.7	2.96	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on use of a 2S2P JEDEC PCB. Refer to the Ordering Guide for more information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

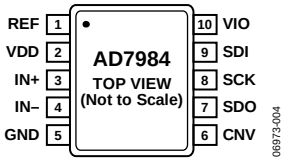


Figure 3. 10-Lead MSOP Pin Configuration

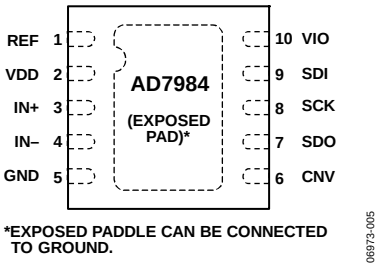


Figure 4. 10-Lead LFCSP Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	REF	AI	Reference Input Voltage. The REF range is 2.9 V to 5.1 V. This pin is referred to the GND pin and should be decoupled closely to the GND pin with a 10 µF capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Differential Positive Analog Input.
4	IN–	AI	Differential Negative Analog Input.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its rising edge, it initiates the conversions and selects the interface mode of the part: chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, the SDO pin is enabled when CNV is low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 18 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).

[1] AI = analog input, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V, REF = 5.0 V, VIO = 3.3 V.

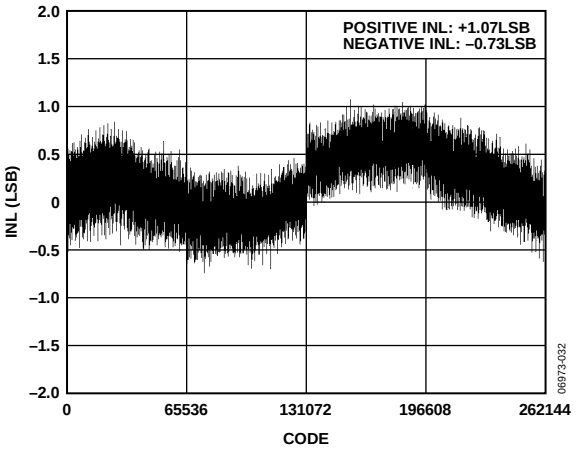


Figure 5. Integral Nonlinearity vs. Code

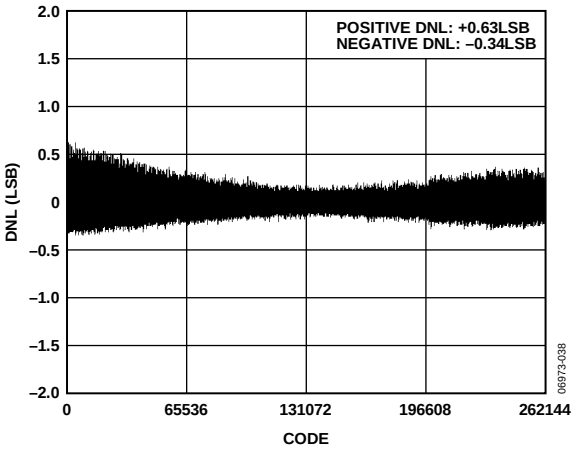


Figure 8. Differential Nonlinearity vs. Code

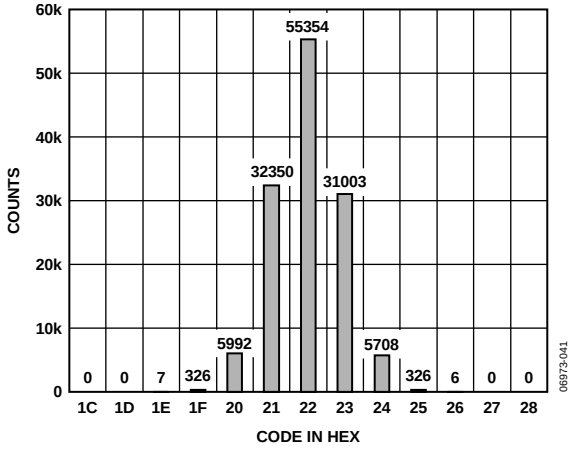


Figure 6. Histogram of a DC Input at the Code Center

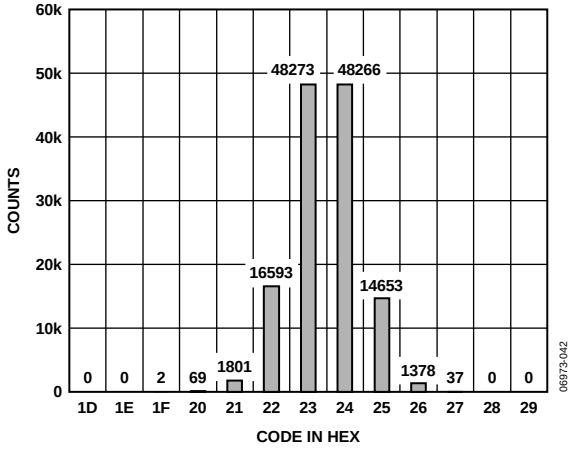


Figure 9. Histogram of a DC Input at the Code Transition

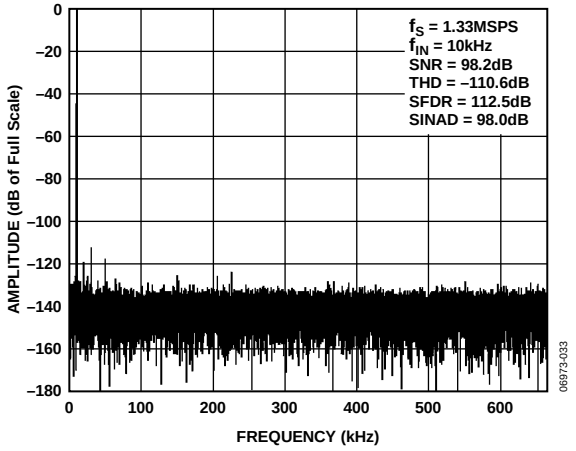


Figure 7. FFT Plot

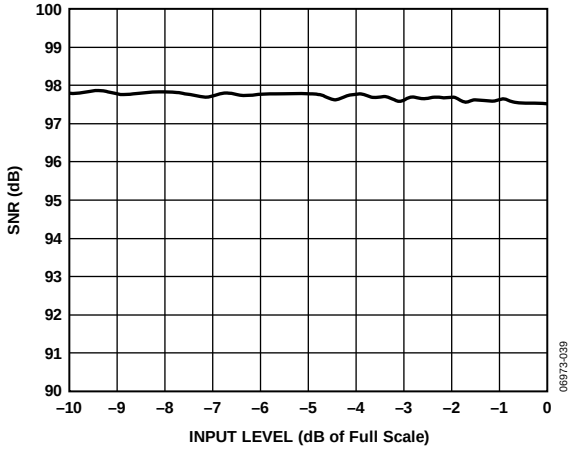


Figure 10. SNR vs. Input Level

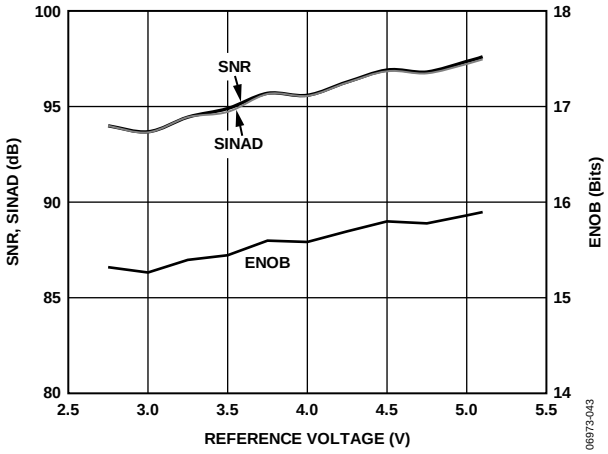


Figure 11. SNR, SINAD, and ENOB vs. Reference Voltage

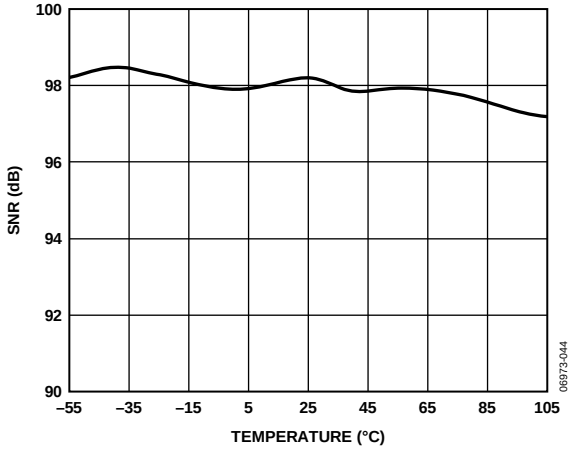


Figure 12. SNR vs. Temperature

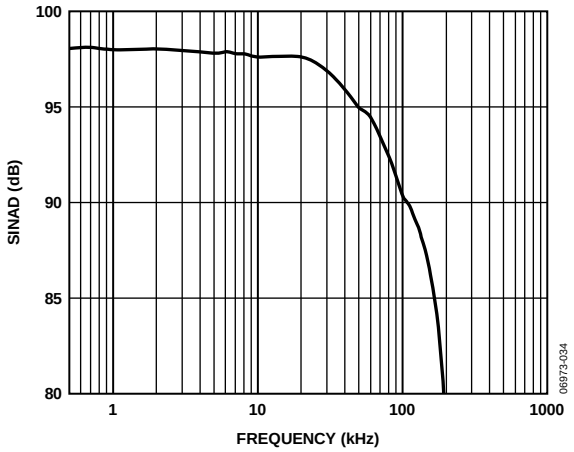


Figure 13. SINAD vs. Frequency

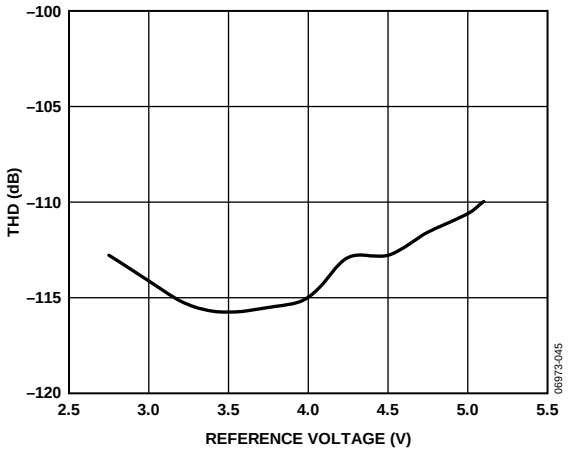


Figure 14. THD vs. Reference Voltage

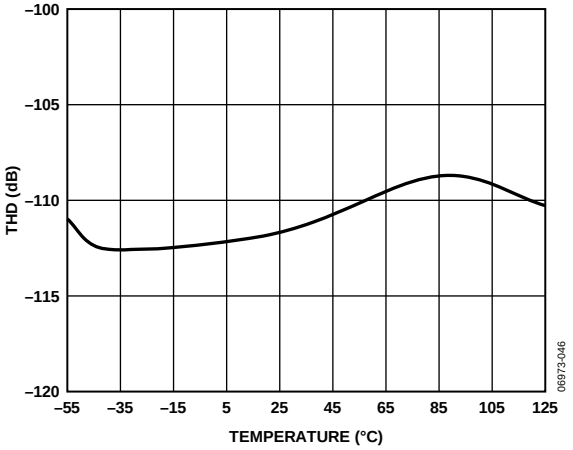


Figure 15. THD vs. Temperature

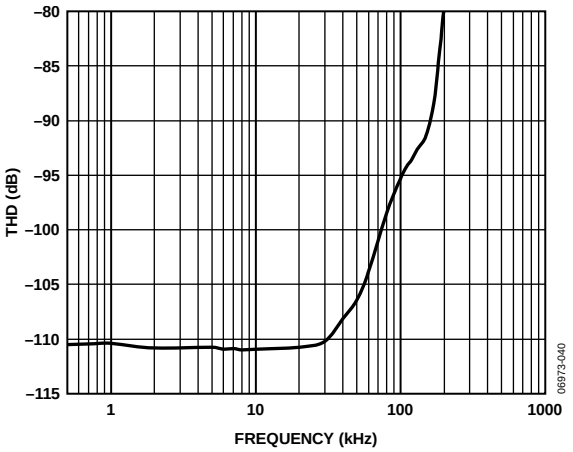


Figure 16. THD vs. Frequency

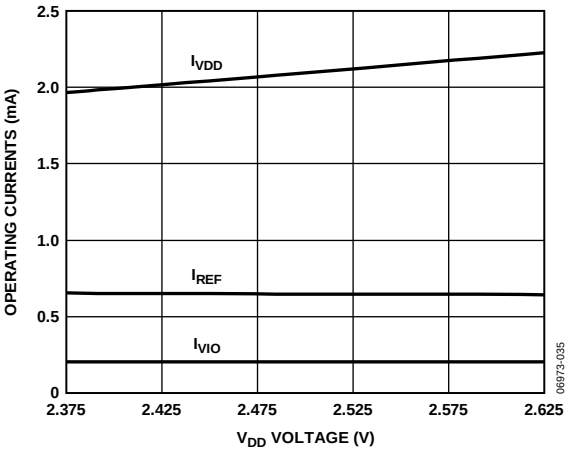


Figure 17. Operating Currents vs. Supply

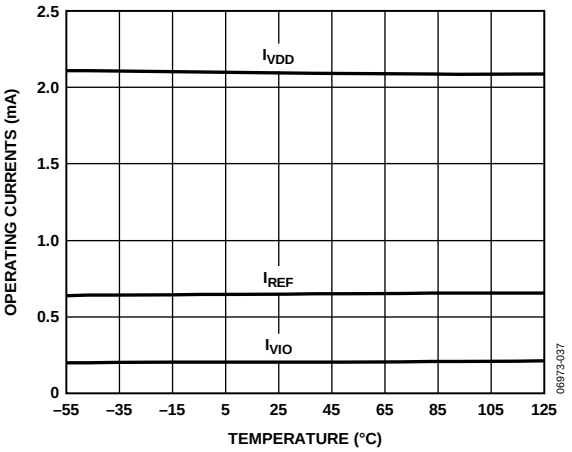


Figure 19. Operating Currents vs. Temperature

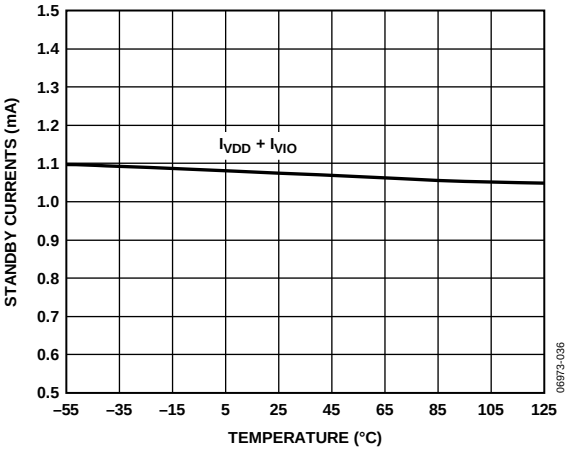


Figure 18. Standby Currents vs. Temperature

TERMINOLOGY

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 21).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
Zero error is the difference between the ideal midscale voltage, that is, 0 V, from the actual voltage producing the midscale output code, that is, 0 LSB.

Gain Error
The first transition (from 100 ... 00 to 100 ... 01) should occur at a level ½ LSB above nominal negative full scale (−4.999981 V for the ±5 V range). The last transition (from 011 … 10 to 011 … 11) should occur for an analog voltage 1½ LSB below the nominal full scale (+4.999943 V for the ±5 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD as follows:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Noise-Free Code Resolution
Noise-free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as

$$Noise\text{-}Free\ Code\ Resolution = \log_2(2^N/Peak\text{-}to\text{-}Peak\ Noise)$$

and is expressed in bits.

Effective Resolution
Effective resolution is calculated as

$$Effective\ Resolution = \log_2(2^N/RMS\ Input\ Noise)$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels. It is measured with a signal at −60 dBF so that it includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay
Aperture delay is the measurement of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

THEORY OF OPERATION

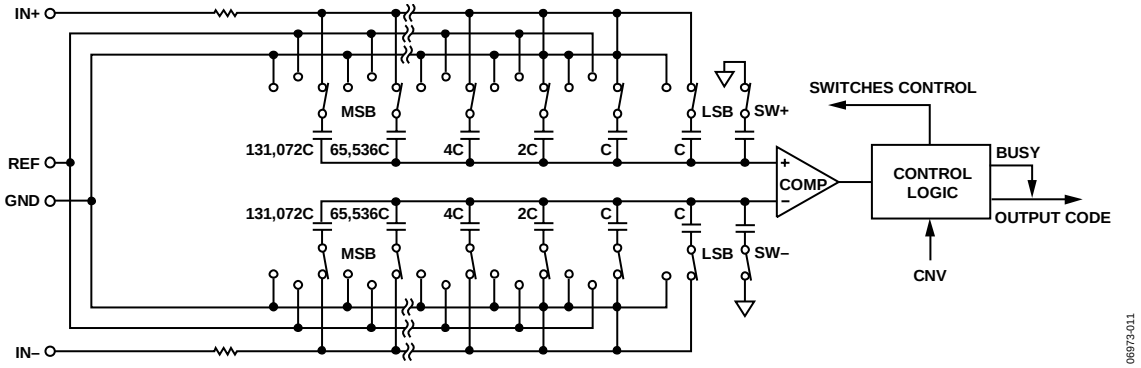


Figure 20. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7984 is a fast, low power, single-supply, precise, 18-bit ADC using a successive approximation architecture and is capable of converting 1,330,000 samples per second (1.33 MSPS).

The AD7984 provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7984 can be interfaced to any 1.8 V to 5 V digital logic family. It is available in a 10-lead MSOP or a tiny 10-lead LFCSP that allows space savings and flexible configurations.

It is pin-for-pin-compatible with the 18-bit AD7982.

CONVERTER OPERATION

The AD7984 is a successive approximation ADC based on a charge redistribution DAC. Figure 20 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 18 binary-weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs IN+ and IN− captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary-weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ ... $V_{REF}/262,144$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7984 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7984 is shown in Figure 21 and Table 9.

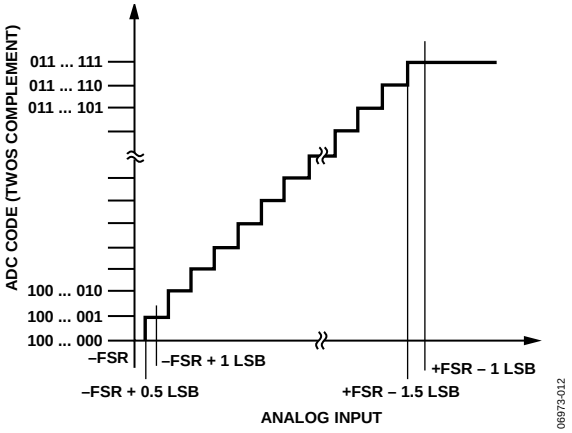


Figure 21. ADC Ideal Transfer Function

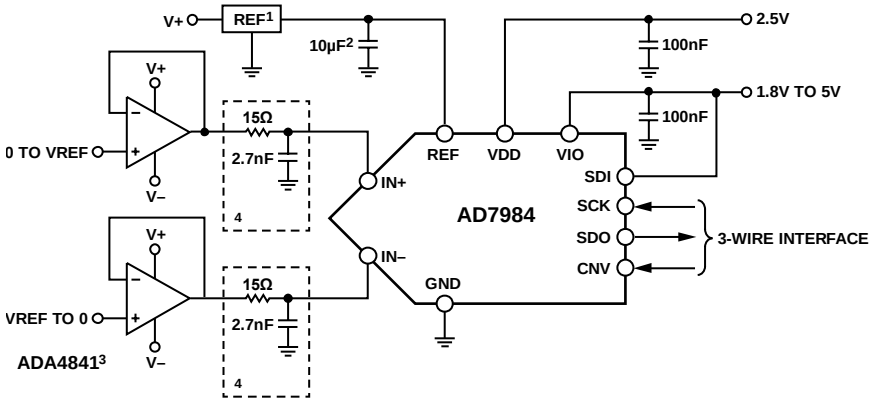
Table 9. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output Code (Hex)
FSR – 1 LSB	+4.999962 V	0x1FFFF[1]
Midscale + 1 LSB	+38.15 µV	0x00001
Midscale	0 V	0x00000
Midscale – 1 LSB	–38.15 µV	0x3FFFF
–FSR + 1 LSB	–4.999962 V	0x20001
–FSR	–5 V	0x20000[2]

[1] This is also the code for an overranged analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{GND}).
[2] This is also the code for an underranged analog input (V_{IN+} – V_{IN-} below V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 22 shows an example of the recommended connection diagram for the AD7984 when multiple supplies are available.



NOTES
[1]SEE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION.
[2]C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
SEE RECOMMENDED LAYOUT IN FIGURE 40 AND FIGURE 41.
[3]SEE DRIVER AMPLIFIER CHOICE SECTION.
[4]RECOMMENDED FILTER CONFIGURATION. SEE THE ANALOG INPUTS SECTION.

Figure 22. Typical Application Diagram with Multiple Supplies

ANALOG INPUTS

Figure 23 shows an equivalent circuit of the input structure of the AD7984.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN+ and IN−. Care must be taken to ensure that the analog input signal does not exceed the reference input voltage (REF) by more than 0.3 V. If the analog input signal exceeds this level, the diodes become forward-biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. However, if the supplies of the input buffer (for example, the supplies of the ADA4841 in Figure 22) are different from those of REF, the analog input signal may eventually exceed the supply rails by more than 0.3 V. In such a case (for example, an input buffer with a short-circuit), the current limitation can be used to protect the part.

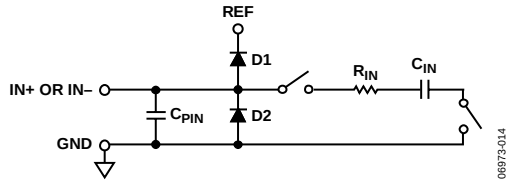


Figure 23. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected.

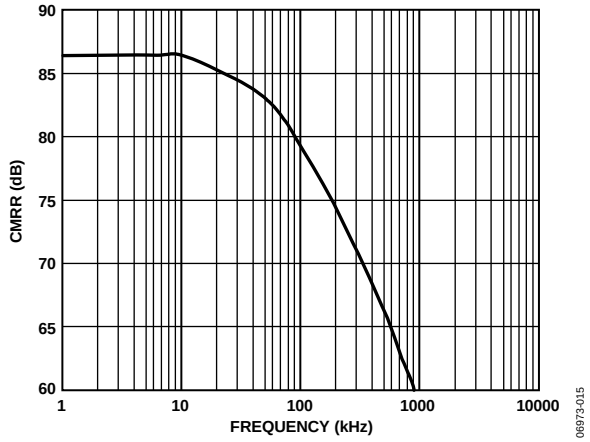


Figure 24. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor.

During the sampling phase, where the switches are closed, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits noise.

When the source impedance of the driving circuit is low, the AD7984 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7984 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7984. The noise from the driver is filtered by the AD7984 analog input circuit's 1-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used. Because the typical noise of the AD7984 is 36.24 µV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left(\frac{36.24}{\sqrt{36.24^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}} \right)$$

  where:
  f_{-3dB} is the input bandwidth, in megahertz, of the AD7984 (10 MHz) or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.

- For ac applications, the driver should have a THD performance commensurate with the AD7984.
- For multichannel multiplexed applications, the driver amplifier and the AD7984 analog input circuit must settle for a full-scale step onto the capacitor array at an 18-bit level (0.0004%, 4 ppm). In the data sheet of the amplifier, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at an 18-bit level and should be verified prior to driver selection.

The Precision ADC Driver Tool can be used to model the settling behavior and to estimate the ac performance of the AD7984 with a selected driver and RC filter.

Table 10. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4805-1/ ADA4805-2	Low noise, small size, and low power
ADA4807-1/ ADA4807-2	Very low noise and high frequency
ADA4841-1/ ADA4841-2	Low noise, low distortion and low power
ADA4941-1	Very low noise, low power single-to-differential
ADA4945-1	Low noise, low distortion, fully differential
LTC6363	Low power, low noise, fully differential

SINGLE-TO-DIFFERENTIAL DRIVER

For applications using a single-ended analog signal, either bipolar or unipolar, the ADA4941-1 single-ended-to-differential driver allows for a differential input into the part. The schematic is shown in Figure 25.

R1 and R2 set the attenuation ratio between the input range and the ADC range (V_{REF}). R1, R2, and C_F are chosen depending on the desired input resistance, signal bandwidth, antialiasing, and noise contribution. For example, for the ±10 V range with a 4 kΩ impedance, R2 = 1 kΩ and R1 = 4 kΩ.

R3 and R4 set the common mode on the IN− input, and R5 and R6 set the common mode on the IN+ input of the ADC. The common mode should be close to $V_{REF}/2$. For example, for the ±10 V range with a single supply, R3 = 8.45 kΩ, R4 = 11.8 kΩ, R5 = 10.5 kΩ, and R6 = 9.76 kΩ.

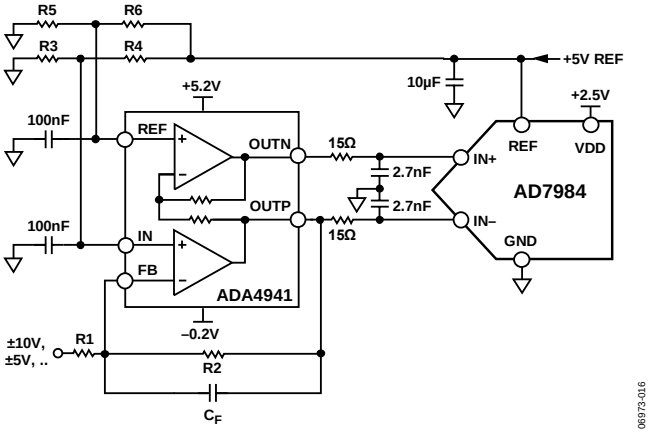


Figure 25. Single-Ended-to-Differential Driver Circuit

VOLTAGE REFERENCE INPUT

The AD7984 voltage reference input, REF, has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source (for example, a reference buffer using the AD8031, the ADA4805-1, or the ADA4807-1), a ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift reference such as the ADR435, ADR445, LTC6655, or ADR4550.

If desired, a reference-decoupling capacitor with values as small as 2.2 µF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

POWER SUPPLY

The AD7984 uses two power supply pins: a core supply (VDD) and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between 1.8 V and 5.5 V. To reduce the number of supplies needed, VIO and VDD can be tied together. When VIO is greater than or equal to VDD, the AD7984 is insensitive to power supply sequencing. In normal operation, if the magnitude of VIO is less than the magnitude of VDD, VIO must be applied before VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 26.

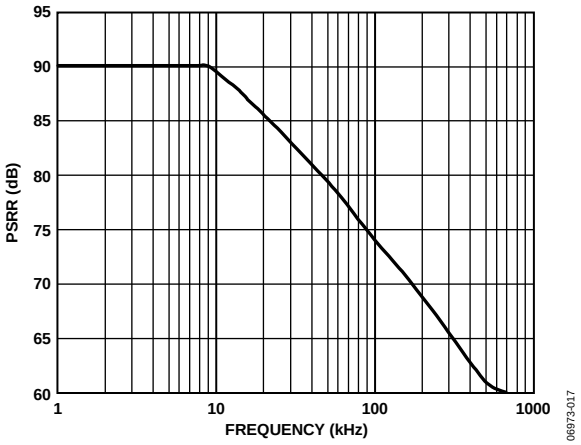


Figure 26. PSRR vs. Frequency

DIGITAL INTERFACE

Although the AD7984 has a reduced number of pins, it offers flexibility in its serial interface modes.

When in $\overline{CS}$ mode, the AD7984 is compatible with SPI, QSPI™, digital hosts, and DSPs. In this mode, the AD7984 can use either a 3-wire or 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

When in chain mode, the AD7984 provides a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The mode in which the part operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high, and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected, the chain mode is always selected.

In either mode, the AD7984 offers the option of forcing a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must timeout the maximum conversion time prior to readback.

The busy indicator feature is enabled

- In $\overline{CS}$ mode if CNV or SDI is low when the ADC conversion ends (see Figure 30 and Figure 34).
- In chain mode if SCK is high during the CNV rising edge (see Figure 38).

$\overline{CS}$ MODE, 3-WIRE WITHOUT BUSY INDICATOR

This mode is usually used when a single AD7984 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 27, and the corresponding timing is given in Figure 28.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. When a conversion is initiated, it continues until completion irrespective of the state of CNV. This can be useful, for example, to bring CNV low to select other SPI devices, such as analog multiplexers; however, CNV must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7984 enters the acquisition phase and goes into standby mode. When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 18th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

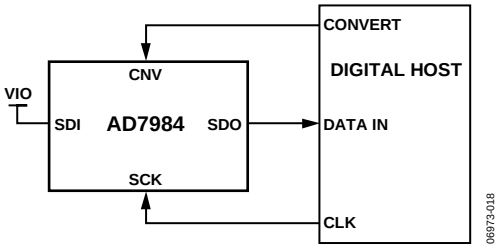


Figure 27. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Connection Diagram (SDI High)

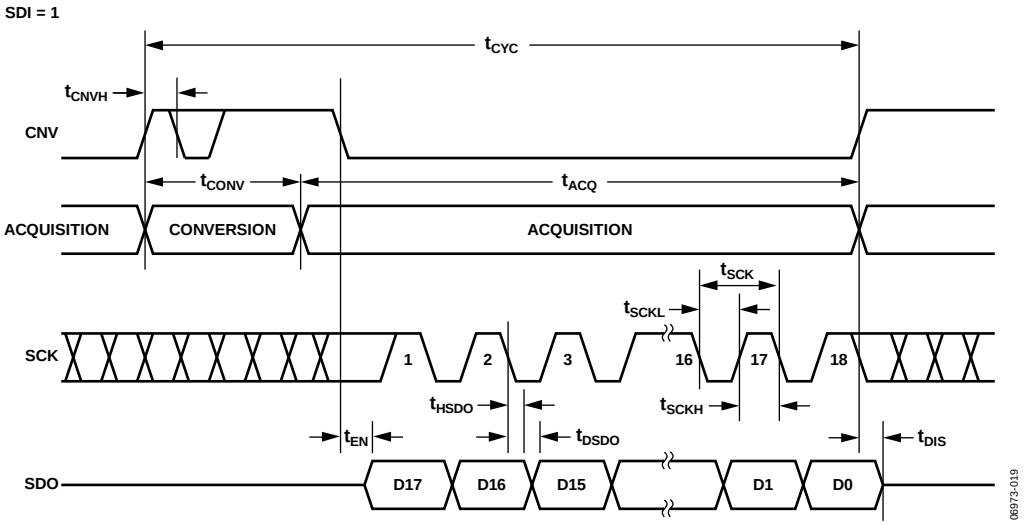


Figure 28. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 3-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7984 is connected to an SPI-compatible digital host having an interrupt input.

The connection diagram is shown in Figure 29, and the corresponding timing is given in Figure 30.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV can be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7984 then enters the acquisition phase and goes into standby mode. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 19th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

If multiple AD7984s are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation.

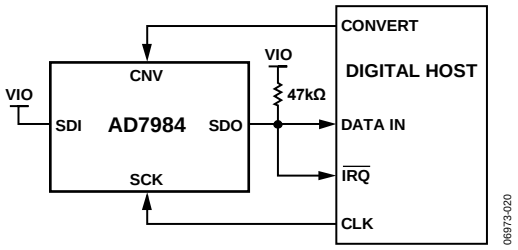


Figure 29. $\overline{CS}$ Mode, 3-Wire with Busy Indicator Connection Diagram (SDI High)

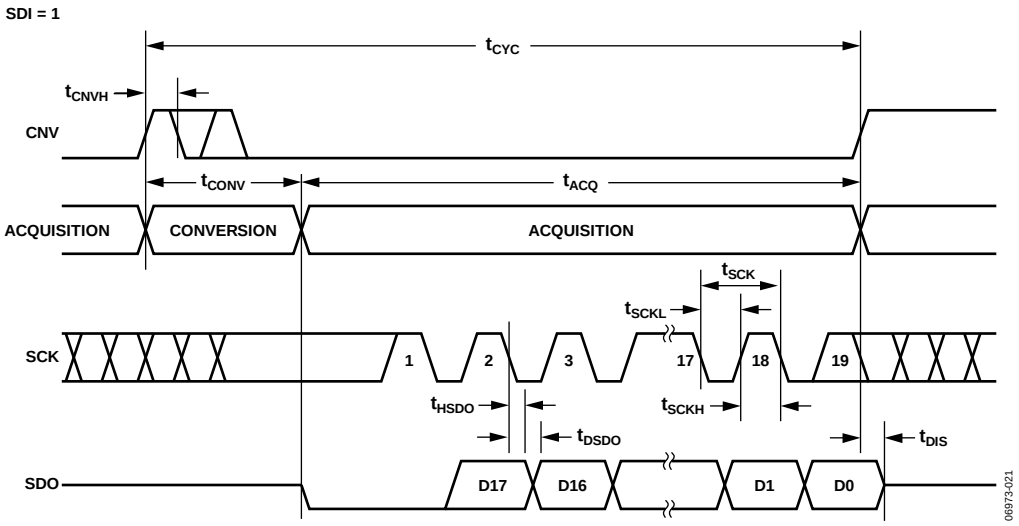


Figure 30. $\overline{CS}$ Mode, 3-Wire with Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 4-WIRE WITHOUT BUSY INDICATOR

This mode is usually used when multiple AD7984s are connected to an SPI-compatible digital host.

A connection diagram example using two AD7984s is shown in Figure 31, and the corresponding timing is given in Figure 32.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7984 enters the acquisition phase and goes into standby mode. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 18th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance and another AD7984 can be read.

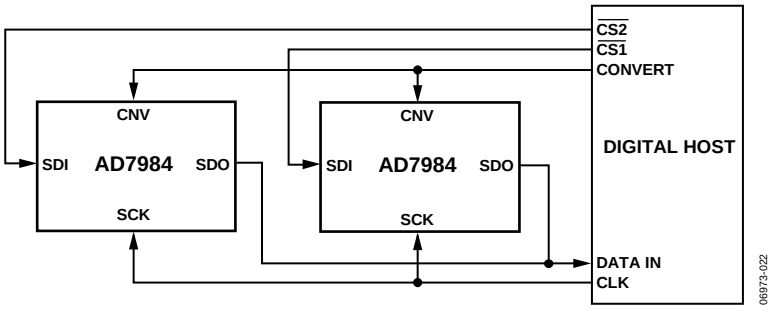


Figure 31. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Connection Diagram

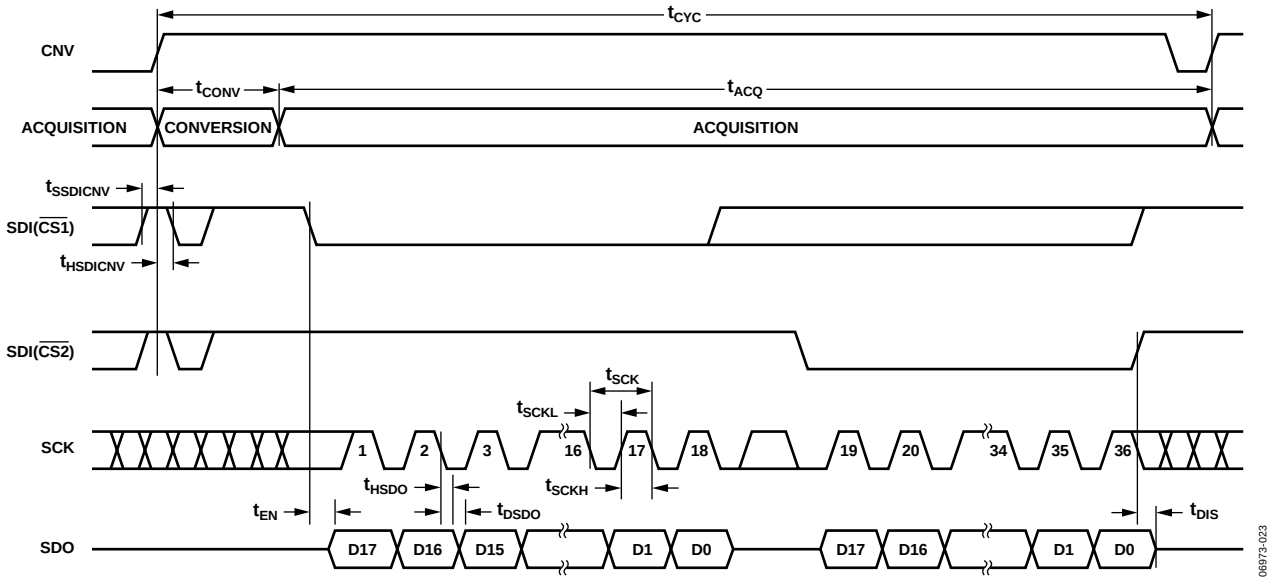


Figure 32. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Serial Interface Timing

$\overline{CS}$ MODE, 4-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7984 is connected to an SPI-compatible digital host with an interrupt input and when it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This independence is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 33, and the corresponding timing is given in Figure 34.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. (If SDI and CNV are low, SDO is driven low.) Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7984 then enters the acquisition phase and goes into standby mode. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 19th SCK falling edge or SDI going high (whichever occurs first), SDO returns to high impedance.

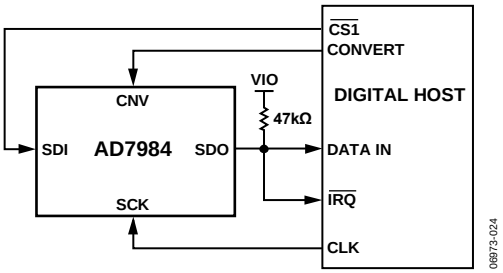


Figure 33. $\overline{CS}$ Mode, 4-Wire with Busy Indicator Connection Diagram

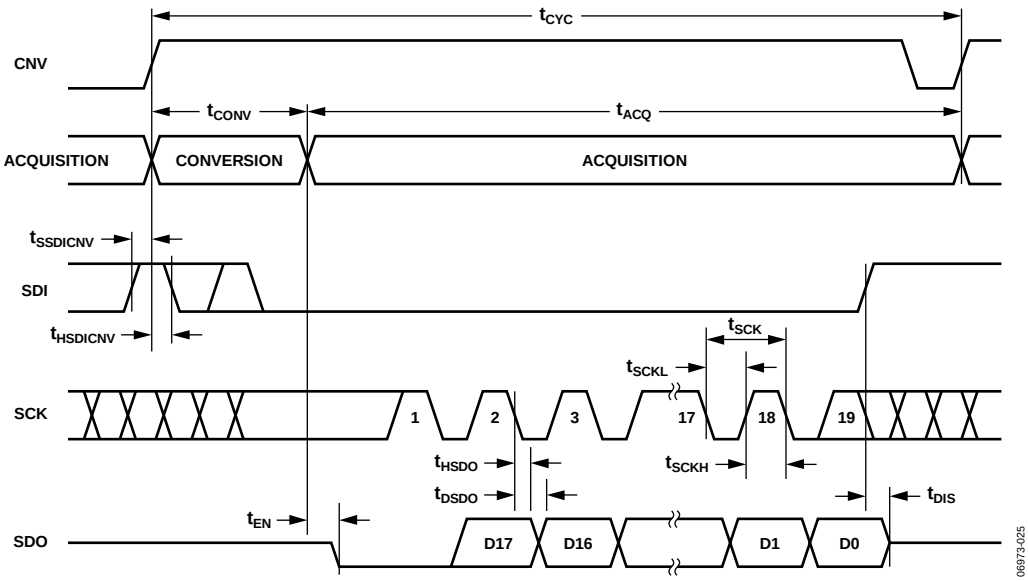


Figure 34. $\overline{CS}$ Mode, 4-Wire with Busy Indicator Serial Interface Timing

CHAIN MODE WITHOUT BUSY INDICATOR

This mode can be used to daisy-chain multiple AD7984s on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7984s is shown in Figure 35, and the corresponding timing is given in Figure 36.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7984 enters the acquisition phase and goes into standby mode. The remaining data bits stored in the internal shift register are clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 18 × N clocks are required to read back the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge will allow a faster reading rate and consequently more AD7984s in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time.

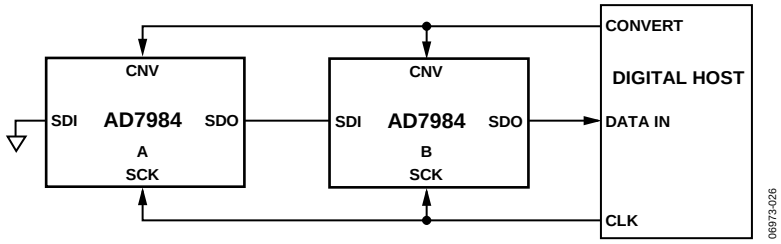


Figure 35. Chain Mode Without Busy Indicator Connection Diagram

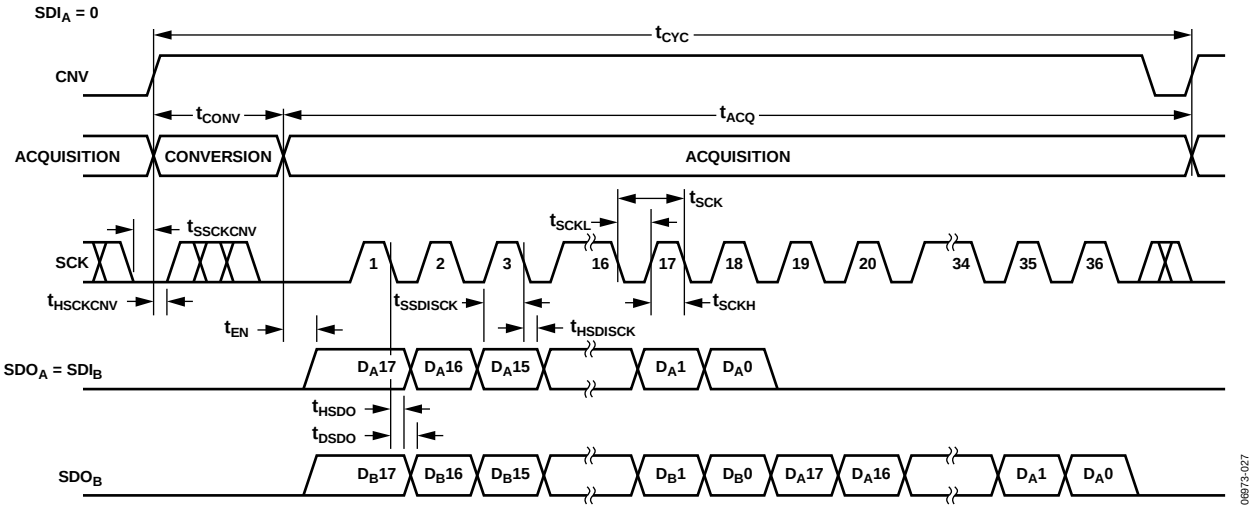


Figure 36. Chain Mode Without Busy Indicator Serial Interface Timing

CHAIN MODE WITH BUSY INDICATOR

This mode can also be used to daisy-chain multiple AD7984s on a 3-wire serial interface while providing a busy indicator. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using three AD7984s is shown in Figure 37, and the corresponding timing is given in Figure 38.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the busy indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the SDO pin of the ADC closest to the digital host (see the AD7984 ADC labeled C in Figure 37) is driven high. This transition on SDO can be used as a busy indicator to trigger the data readback controlled by the digital host. The AD7984 then enters the acquisition phase and goes into standby mode. The data bits stored in the internal shift register are clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 18 × N + 1 clocks are required to read back the N ADCs. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7984s in the chain, provided the digital host has an acceptable hold time.

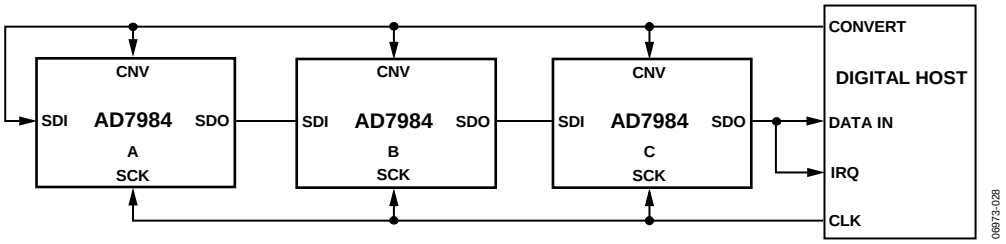


Figure 37. Chain Mode with Busy Indicator Connection Diagram

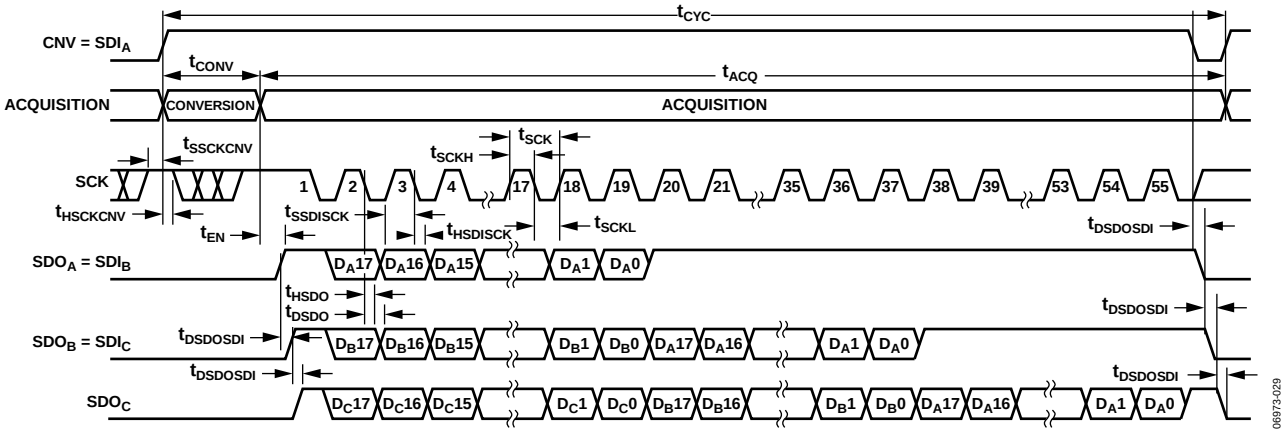


Figure 38. Chain Mode with Busy Indicator Serial Interface Timing

APPLICATION HINTS

LAYOUT

The printed circuit board (PCB) that houses the AD7984 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7984, with its analog signals on the left side and its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7984 is used as a shield. Fast switching signals, such as CNV or clocks, should not run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. The ground plane can be common or split between the digital and analog sections. In the latter case, the planes should be joined underneath the AD7984.

The AD7984 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance traces.

Finally, the power supplies VDD and VIO of the AD7984 should be decoupled with ceramic capacitors, typically 100 nF, placed close to the AD7984 and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

An example of layout following these rules is shown in Figure 39 and Figure 40.

EVALUATING THE AD7984 PERFORMANCE

Other recommended layouts for the AD7984 are outlined in the documentation of the evaluation board for the AD7984 (EVAL-AD7984SDZ). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CB1Z.

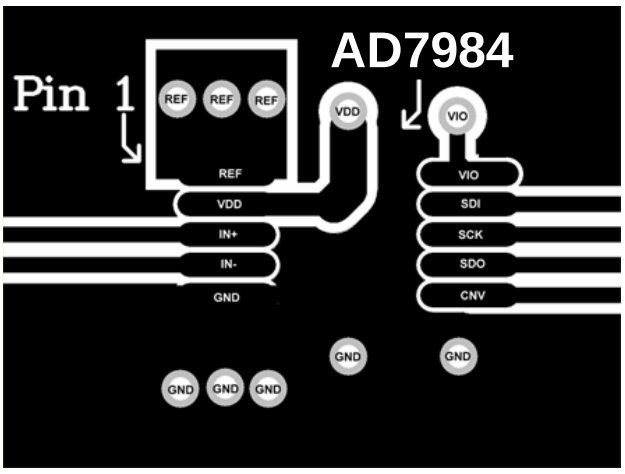


Figure 39. Example Layout of the AD7984 (Top Layer)

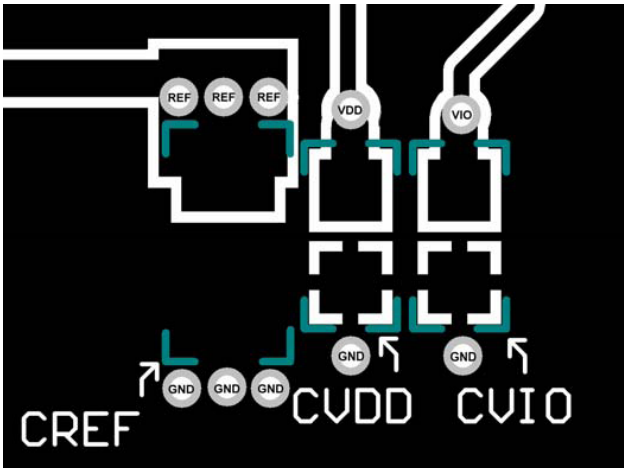


Figure 40. Example Layout of the AD7984 (Bottom Layer)

OUTLINE DIMENSIONS

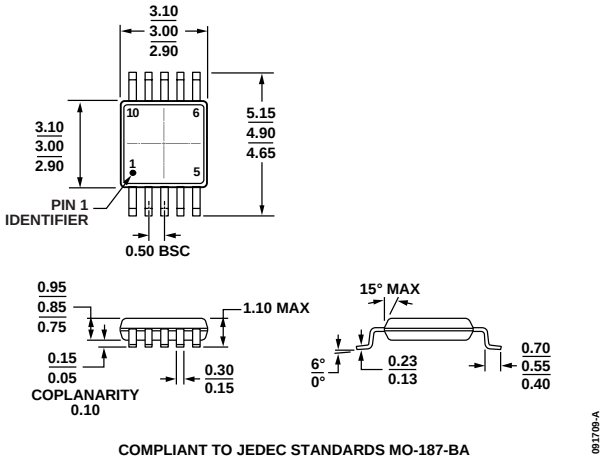


Figure 41. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

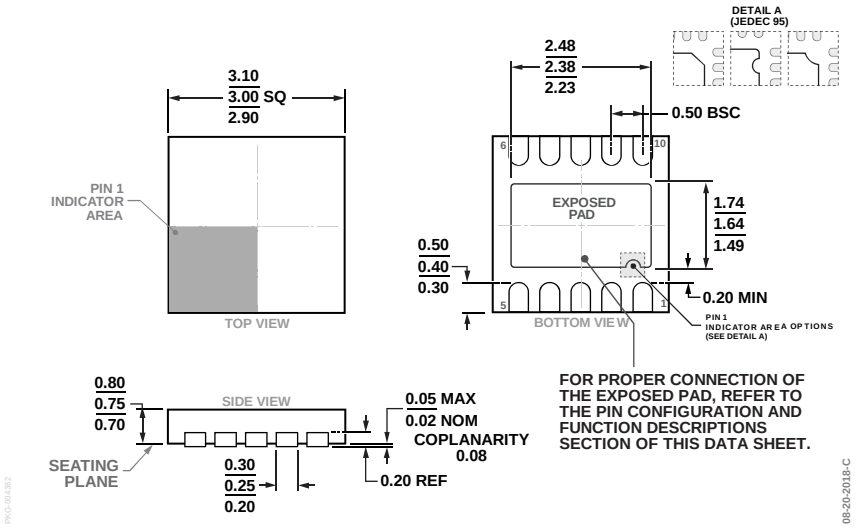


Figure 42. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead (CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
AD7984BRMZ	−40°C to +85°C	10-Lead MSOP	RM-10	Tube, 50	C60
AD7984BRMZ-RL7	−40°C to +85°C	10-Lead MSOP	RM-10	Reel, 1,000	C60
AD7984BCPZ-RL7	−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	Reel, 1,500	C60
AD7984BCPZ-RL	−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	Reel, 5,000	C60
EVAL-AD7984SDZ		Evaluation Board			
EVAL-SDP-CB1Z		Evaluation Board			

[1] Z = RoHS compliant part.
[2] The EVAL-AD7984SDZ board can be used as a standalone evaluation board or in conjunction with the EVAL-SDP-CB1Z for evaluation/demonstration purposes.
[3] The EVAL-SDP-CB1Z board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the SD designator.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View AD7984BCPZ-RL on WIN SOURCE
- Analog Devices Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management