



**THE DATASHEET OF
NVTFS5C670NLWFTAG**



MOSFET - Power, Single N-Channel

60 V, 6.8 mΩ, 70 A

NVTFS5C670NL

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVTFS5C670NLWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | | Symbol | Value | Unit | |
|---|--|---------------------------|-------------|------------------|---|
| Drain-to-Source Voltage | | V_{DSS} | 60 | V | |
| Gate-to-Source Voltage | | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4) | Steady State | $T_C = 25^\circ\text{C}$ | I_D | 70 | A |
| | | $T_C = 100^\circ\text{C}$ | | 49 | |
| Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3) | Steady State | $T_C = 25^\circ\text{C}$ | P_D | 63 | W |
| | | $T_C = 100^\circ\text{C}$ | | 31 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4) | Steady State | $T_A = 25^\circ\text{C}$ | I_D | 16 | A |
| | | $T_A = 100^\circ\text{C}$ | | 11 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 3) | Steady State | $T_A = 25^\circ\text{C}$ | P_D | 3.2 | W |
| | | $T_A = 100^\circ\text{C}$ | | 1.6 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} | 440 | A | |
| Operating Junction and Storage Temperature Range | | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | | I_S | 68 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 3.6 \text{ A}$) | | E_{AS} | 166 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | T_L | 260 | $^\circ\text{C}$ | |

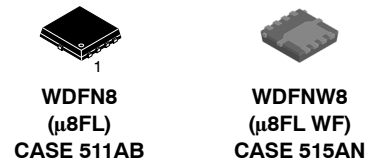
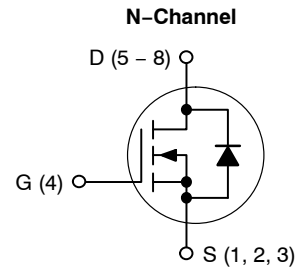
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

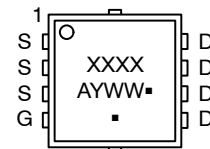
| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Case – Steady State (Note 3) | $R_{\theta JC}$ | 2.4 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 47 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JE51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

| $V_{(BR)DSS}$ | $R_{DS(on) MAX}$ | $I_D MAX$ |
|---------------|------------------|-----------|
| 60 V | 6.8 mΩ @ 10 V | 70 A |
| | 10 mΩ @ 4.5 V | |



MARKING DIAGRAM



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVTFS5C670NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|--------------------------------------|--|------------------------|----|-----|-------|
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 60 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} /T _J | | | 27 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 60 V | T _J = 25°C | | 10 | μA |
| | | | T _J = 125°C | | 250 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = 20 V | | | 100 | nA |

ON CHARACTERISTICS (Note 5)

| | | | | | | |
|-----------------------------------|-------------------------------------|--|-----------------------|------|-----|-------|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 50 μA | 1.2 | | 2.0 | V |
| Threshold Temperature Coefficient | V _{GS(TH)} /T _J | | | -4.7 | | mV/°C |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 35 A | 5.6 | 6.8 | mΩ |
| | | V _{GS} = 4.5 V | I _D = 35 A | 8.0 | 10 | |
| Forward Transconductance | g _{FS} | V _{DS} = 15 V, I _D = 35 A | | 82 | | S |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|---------------------|--|--|------|--|----|
| Input Capacitance | C _{ISS} | V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V | | 1400 | | pF |
| Output Capacitance | C _{OSS} | | | 690 | | |
| Reverse Transfer Capacitance | C _{RSS} | | | 15 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 4.5 V, V _{DS} = 48 V; I _D = 35 A | | 9.0 | | nC |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 48 V; I _D = 35 A | | 20 | | nC |
| Threshold Gate Charge | Q _{G(TH)} | V _{GS} = 10 V, V _{DS} = 48 V; I _D = 35 A | | 2.5 | | nC |
| Gate-to-Source Charge | Q _{GS} | | | 4.5 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 2.0 | | |
| Plateau Voltage | V _{GP} | | | 3.1 | | |

SWITCHING CHARACTERISTICS (Note 6)

| | | | | | | |
|---------------------|---------------------|---|--|----|--|----|
| Turn-On Delay Time | t _{d(ON)} | V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 35 A, R _G = 2.5 Ω | | 11 | | ns |
| Rise Time | t _r | | | 60 | | |
| Turn-Off Delay Time | t _{d(OFF)} | | | 15 | | |
| Fall Time | t _f | | | 4 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|-----------------|---|------------------------|----|-----|-----|----|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 35 A | T _J = 25°C | | 0.9 | 1.2 | V |
| | | | T _J = 125°C | | 0.8 | | |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 35 A | | 34 | | ns | |
| Charge Time | t _a | | | 17 | | | |
| Discharge Time | t _b | | | 17 | | | |
| Reverse Recovery Charge | Q _{RR} | | | 19 | | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

NVTFS5C670NL

TYPICAL CHARACTERISTICS

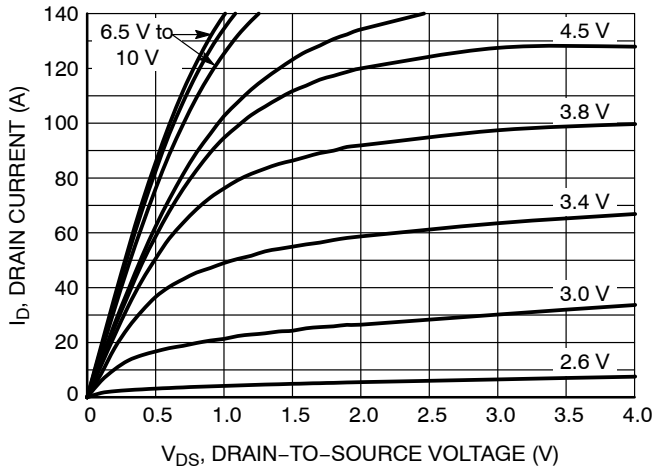


Figure 1. On-Region Characteristics

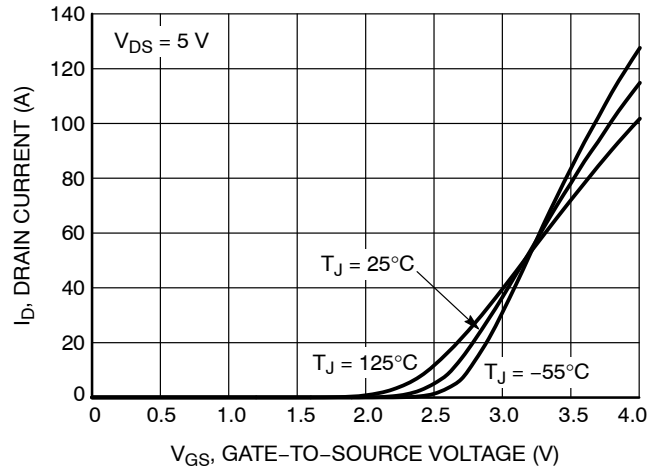


Figure 2. Transfer Characteristics

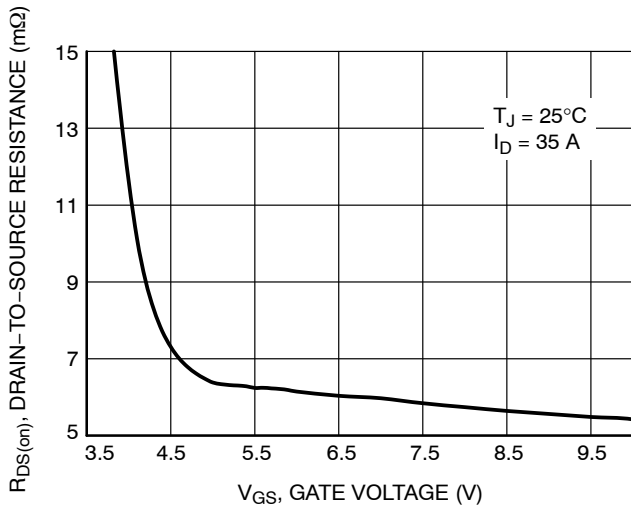


Figure 3. On-Resistance vs. Gate-to-Source Voltage

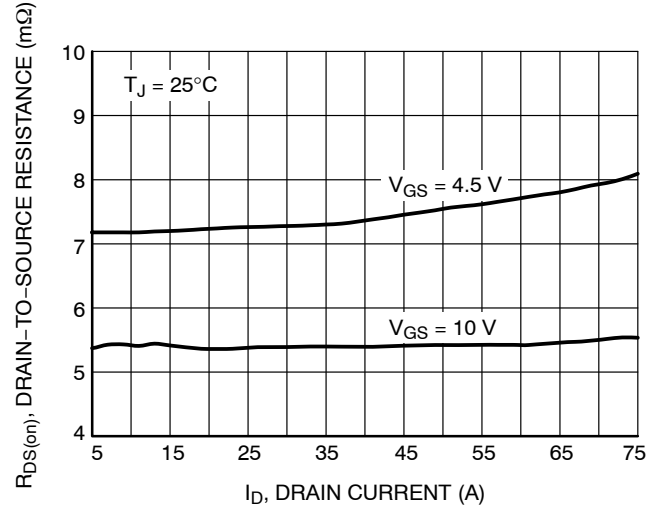


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

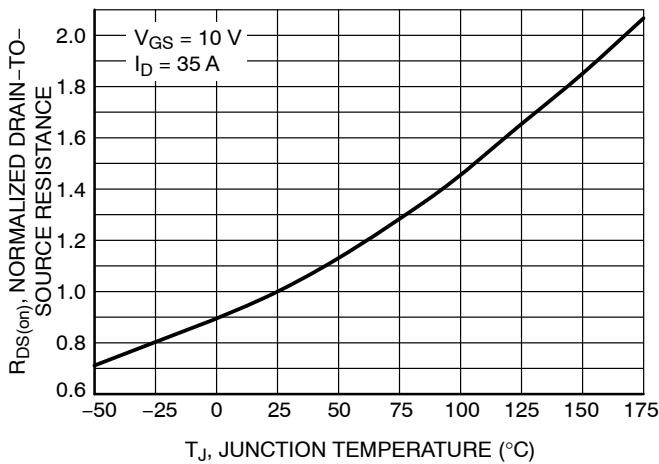


Figure 5. On-Resistance Variation with Temperature

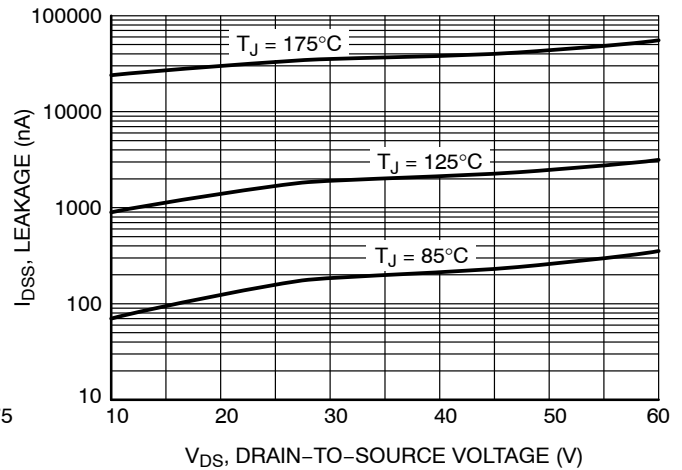


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

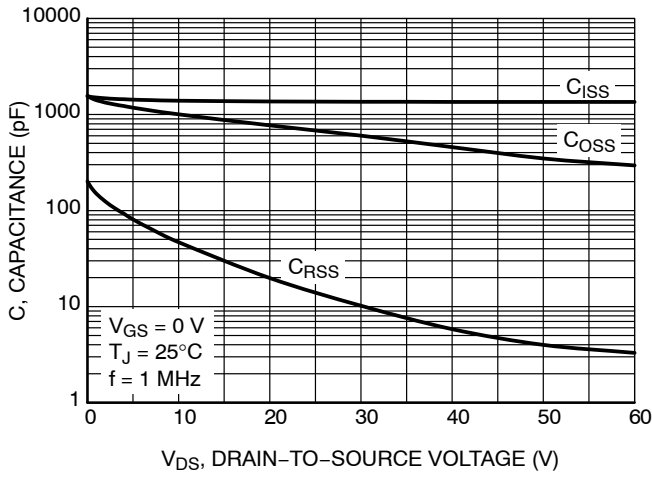


Figure 7. Capacitance Variation

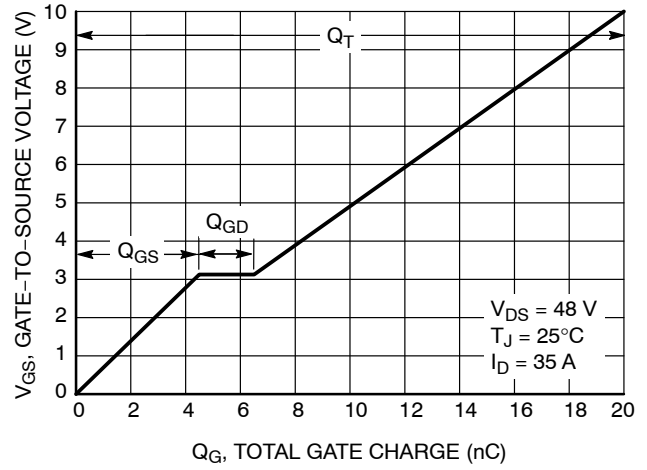


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

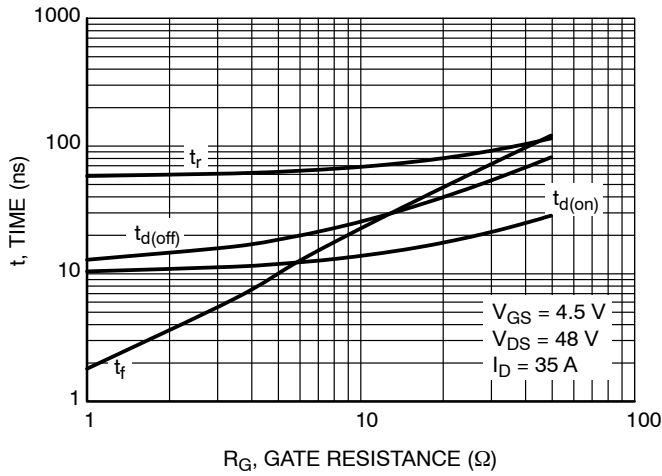


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

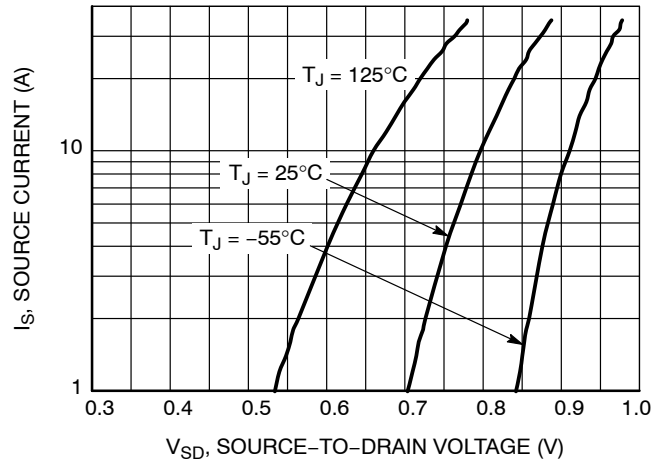


Figure 10. Diode Forward Voltage vs. Current

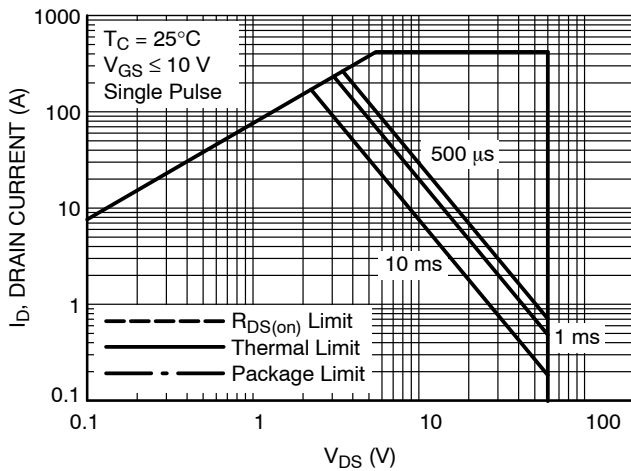


Figure 11. Maximum Rated Forward Biased Safe Operating Area

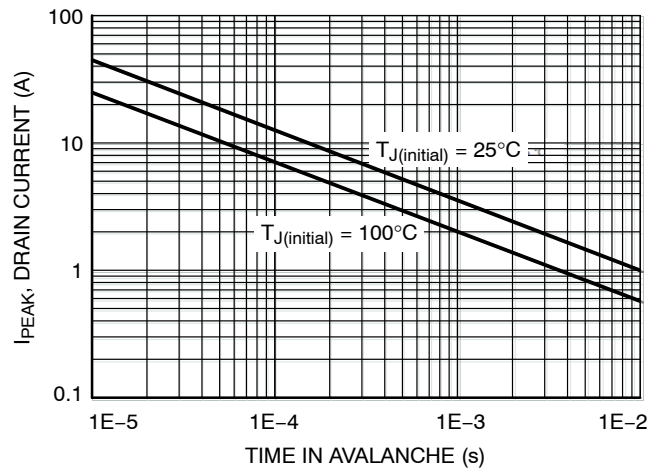


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVTFS5C670NL

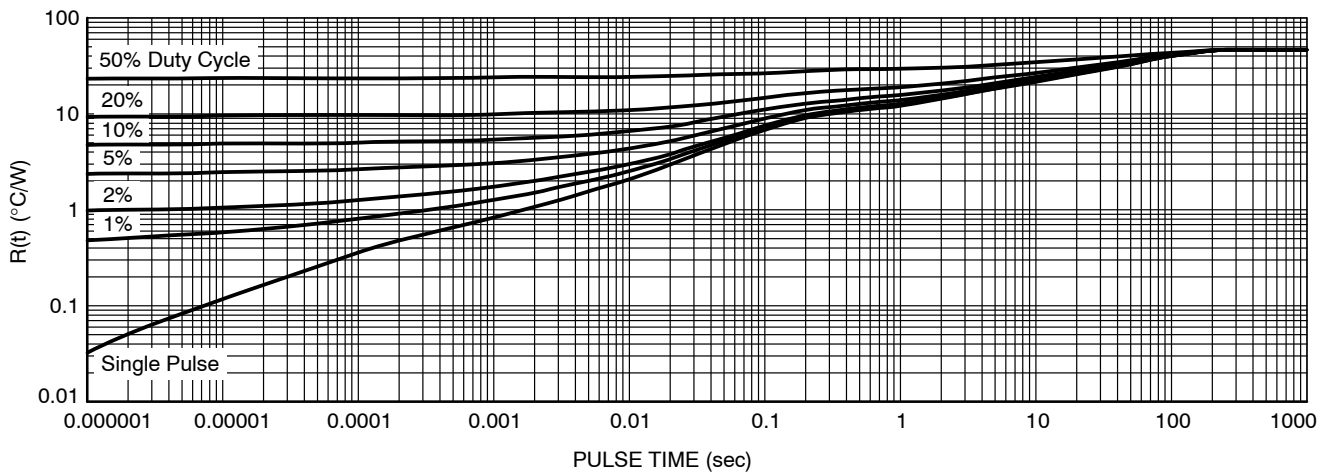


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] |
|-------------------|---------|--------------------------------------|-----------------------|
| NVTFS5C670NLTAG | 670L | WDFN8 (Pb-Free) | 1500 / Tape & Reel |
| NVTFS5C670NLWFTAG | 70LW | WDFNW8 (Pb-Free, Wettable Flanks) | 1500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

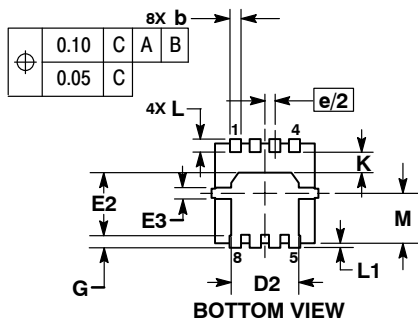
DATE 23 APR 2012



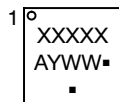
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | --- | 0.05 | 0.000 | --- | 0.002 |
| b | 0.23 | 0.30 | 0.40 | 0.009 | 0.012 | 0.016 |
| c | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 3.30 BSC | | | 0.130 BSC | | |
| D1 | 2.95 | 3.05 | 3.15 | 0.116 | 0.120 | 0.124 |
| D2 | 1.98 | 2.11 | 2.24 | 0.078 | 0.083 | 0.088 |
| E | 3.30 BSC | | | 0.130 BSC | | |
| E1 | 2.95 | 3.05 | 3.15 | 0.116 | 0.120 | 0.124 |
| E2 | 1.47 | 1.60 | 1.73 | 0.058 | 0.063 | 0.068 |
| E3 | 0.23 | 0.30 | 0.40 | 0.009 | 0.012 | 0.016 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| G | 0.30 | 0.41 | 0.51 | 0.012 | 0.016 | 0.020 |
| K | 0.65 | 0.80 | 0.95 | 0.026 | 0.032 | 0.037 |
| L | 0.30 | 0.43 | 0.56 | 0.012 | 0.017 | 0.022 |
| L1 | 0.06 | 0.13 | 0.20 | 0.002 | 0.005 | 0.008 |
| M | 1.40 | 1.50 | 1.60 | 0.055 | 0.059 | 0.063 |
| θ | 0° | --- | 12° | 0° | --- | 12° |



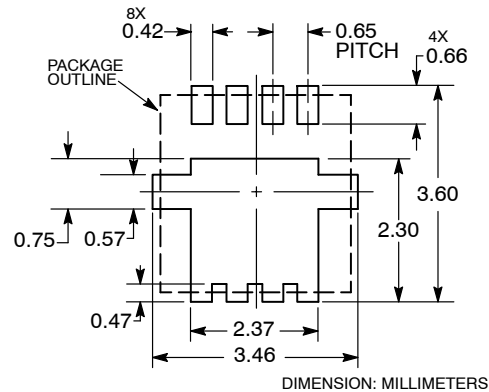
GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

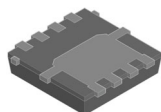
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| DESCRIPTION: | WDFN8 3.3X3.3, 0.65P | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

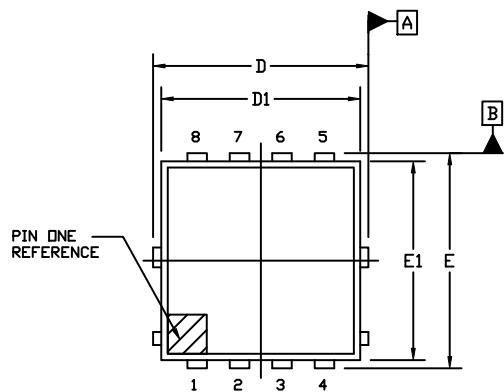
PACKAGE DIMENSIONS

ON Semiconductor®



WDFNW8 3.3x3.3, 0.65P (Full-Cut μ 8FL WF) CASE 515AN ISSUE O

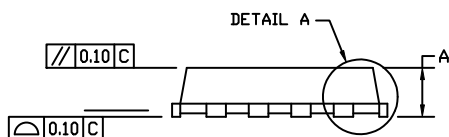
DATE 25 AUG 2020



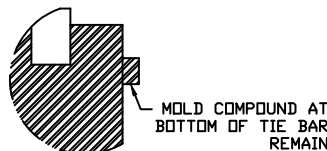
TOP VIEW



DETAIL A



SIDE VIEW



DETAIL B

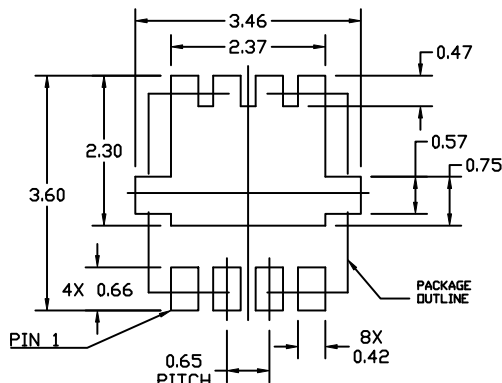
NOTES:

1. DIMENSIONING AND TOLERANCING PER: ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NDM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | ---- | 0.05 |
| b | 0.23 | 0.30 | 0.40 |
| c | 0.15 | 0.20 | 0.25 |
| D | 3.05 | 3.30 | 3.55 |
| D1 | 2.95 | 3.05 | 3.15 |
| D2 | 1.98 | 2.11 | 2.24 |
| E | 3.05 | 3.30 | 3.55 |
| E1 | 2.95 | 3.05 | 3.15 |
| E2 | 1.47 | 1.60 | 1.73 |
| E3 | 0.23 | 0.30 | 0.40 |
| e | 0.65 BSC | | |
| G | 0.30 | 0.41 | 0.51 |
| K | 0.65 | 0.80 | 0.95 |
| L | 0.30 | 0.43 | 0.59 |
| L1 | 0.06 | 0.13 | 0.20 |
| M | 1.40 | 1.50 | 1.60 |



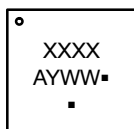
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

(Note: Microdot may be in either location)

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- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management