



# THE DATASHEET OF TRSF3223EIDB





Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low and EN is high, both drivers and receivers are shut off, and the supply current is reduced to 1 mA. Disconnecting the serial port or turning off the peripheral drivers causes auto-powerdown to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown enabled, the device is automatically activated when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μs. INVALID is low (invalid data) if the receiver input voltage is between -0.3 V and 0.3 V for more than 30 μs. Refer to Figure 4 for receiver input levels.

**Table 1. ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1) (2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 25	TRSF3223ECDW	TRSF3223EC
		Reel of 2000	TRSF3223ECDWR	
	SSOP – DB	Tube of 70	TRSF3223ECDB	RT23EC
		Reel of 2000	TRSF3223ECDBR	
	TSSOP – PW	Tube of 70	TRSF3223ECPW	RT23EC
		Reel of 2000	TRSF3223ECPWR	
-40°C to 85°C	SOIC – DW	Tube of 25	TRSF3223EIDW	TRSF3223EI
		Reel of 2000	TRSF3223EIDWR	
	SSOP – DB	Tube of 70	TRSF3223EIDB	RT23EI
		Reel of 2000	TRSF3223EIDBR	
	TSSOP – PW	Tube of 70	TRSF3223EIPW	RT23EI
		Reel of 2000	TRSF3223EIPWR	
	QFN – RGW	Reel of 3000	TRSF3223EIRGWR	RT23EI

- (1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**FUNCTION TABLES**

**Each Driver<sup>(1)</sup>**

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

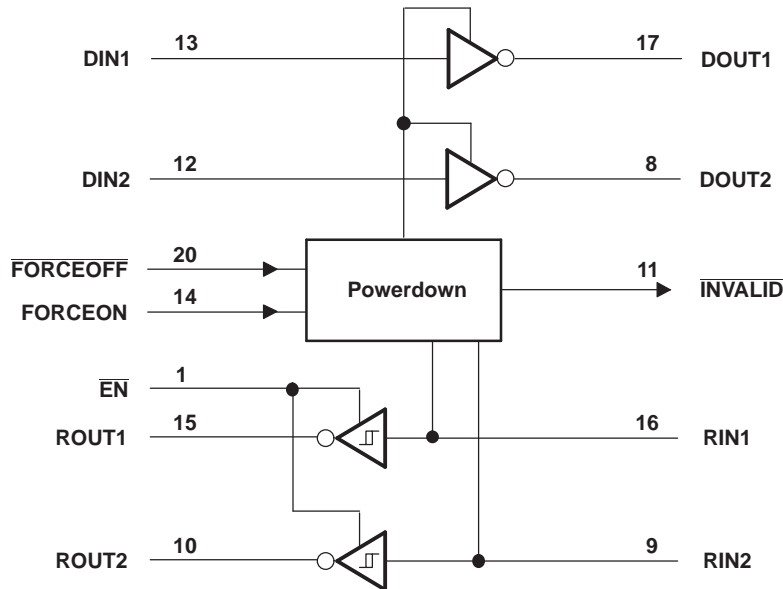
(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver<sup>(1)</sup>

INPUTS			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

- (1) H = high level, L = low level, X = irrelevant,  
Z = high impedance (off),  
Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers are for the DB, DW, and PW packages.

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.3	6	V
V+	Positive-output supply voltage range <sup>(2)</sup>	-0.3	7	V
V-	Negative-output supply voltage range <sup>(2)</sup>	0.3	-7	V
V+ – V-	Supply voltage difference <sup>(2)</sup>		13	V
V <sub>I</sub>	Input voltage range	Driver ( $\overline{\text{FORCEOFF}}$ , FORCEON, $\overline{\text{EN}}$ )		V
		Receiver		
V <sub>O</sub>	Output voltage range	Driver		V
		Receiver ( $\overline{\text{INVALID}}$ )		
$\theta_{JA}$	Package thermal impedance <sup>(3) (4)</sup>	DB package		°C/W
		DW package		
		PW package		
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of T<sub>J</sub>(max),  $\theta_{JA}$ , and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J</sub>(max) – T<sub>A</sub>)/ $\theta_{JA}$ . Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

See Figure 6

		MIN	NOM	MAX	UNIT	
Supply voltage		V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
		V <sub>CC</sub> = 5 V	4.5	5	5.5	
V <sub>IH</sub>	Driver and control high-level input voltage	DIN, $\overline{\text{EN}}$ , $\overline{\text{FORCEOFF}}$ , FORCEON		V		
		V <sub>CC</sub> = 3.3 V	2			
		V <sub>CC</sub> = 5 V	2.4			
V <sub>IL</sub>	Driver and control low-level input voltage	DIN, $\overline{\text{EN}}$ , $\overline{\text{FORCEOFF}}$ , FORCEON		0.8	V	
V <sub>I</sub>	Driver and control input voltage	DIN, $\overline{\text{EN}}$ , $\overline{\text{FORCEOFF}}$ , FORCEON		0	V	
	Receiver input voltage			5.5		
T <sub>A</sub>	Operating free-air temperature	TRSF3223EC	0	70	°C	
		TRSF3223EI	-40	85		

- (1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
I <sub>I</sub>	Input leakage current	$\overline{\text{EN}}$ , $\overline{\text{FORCEOFF}}$ , FORCEON		±0.01	±1	μA	
I <sub>CC</sub>	Supply current	Auto-powerdown disabled	V <sub>CC</sub> = 3.3 V or 5 V, T <sub>A</sub> = 25°C, No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V <sub>CC</sub>		0.3	1	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	
		Auto-powerdown enabled	No load, $\overline{\text{FORCEOFF}}$ at V <sub>CC</sub> , FORCEON at GND, All RIN are open or grounded		1	10	μA

- (1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.
- (2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## DRIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	DOOUT at R <sub>L</sub> = 3 kΩ to GND	5	5.4		V
V <sub>OL</sub>	Low-level output voltage	DOOUT at R <sub>L</sub> = 3 kΩ to GND	–5	–5.4		V
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = V <sub>CC</sub>		±0.01	±1	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> at GND		±0.01	±1	μA
I <sub>OS</sub>	Short-circuit output current <sup>(3)</sup>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V		±35	±60	mA
		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V				
r <sub>o</sub>	Output resistance	V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0 V, V <sub>O</sub> = ±2 V	300	10M		Ω
I <sub>OZ</sub>	Output leakage current	FORCEOFF = GND, V <sub>CC</sub> = 3 V to 3.6 V, V <sub>O</sub> = ±12 V			±25	μA
		FORCEOFF = GND, V <sub>CC</sub> = 4.5 V to 5.5 V, V <sub>O</sub> = ±12 V			±25	

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
Maximum data rate (see Figure 1)	R <sub>L</sub> = 3 kΩ, One DOOUT switching	C <sub>L</sub> = 1000 pF		250		kbit/s	
		C <sub>L</sub> = 250 pF,	V <sub>CC</sub> = 3 V to 4.5 V	1000			
		C <sub>L</sub> = 1000 pF,	V <sub>CC</sub> = 4.5 V to 5.5 V	1000			
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	C <sub>L</sub> = 150 pF to 2500 pF,	R <sub>L</sub> = 3 kΩ to 7 kΩ, See Figure 2	300		ns	
SR(tr)	Slew rate, transition region (see Figure 1)	R <sub>L</sub> = 7 kΩ,	C <sub>L</sub> = 150 pF to 1000 pF	8	90	V/μs	
		R <sub>L</sub> = 3 kΩ	C <sub>L</sub> = 1000 pF	12	60		
			C <sub>L</sub> = 150 pF to 250 pF	24	150		

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## RECEIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.1		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.6	2.4	V
		V <sub>CC</sub> = 5 V		1.9	2.4	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.1		V
		V <sub>CC</sub> = 5 V	0.6	1.4		
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.5		V
I <sub>OZ</sub>	Output leakage current	$\overline{EN} = V_{CC}$		±0.05		µA
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5		kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP <sup>(2)</sup>	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See Figure 3	150	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See Figure 3	150	ns
t <sub>en</sub>	Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See Figure 4	200	ns
t <sub>dis</sub>	Output disable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See Figure 4	200	ns
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	See Figure 3	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

## AUTO-POWERDOWN SECTION

### Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND,	$\overline{FORCEOFF} = V_{CC}$		2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND,	$\overline{FORCEOFF} = V_{CC}$	-2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND,	$\overline{FORCEOFF} = V_{CC}$	-0.3	0.3	V
$V_{OH}$	$\overline{INVALID}$ high-level output voltage	$I_{OH} = 1\text{ mA}$ , $\overline{FORCEOFF} = V_{CC}$	FORCEON = GND,	$V_{CC} - 0.6$		V
$V_{OL}$	$\overline{INVALID}$ low-level output voltage	$I_{OL} = 1.6\text{ mA}$ , $\overline{FORCEOFF} = V_{CC}$	FORCEON = GND,		0.4	V

### Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TYP <sup>(1)</sup>	UNIT
$t_{valid}$	Propagation delay time, low- to high-level output	1	$\mu\text{s}$
$t_{invalid}$	Propagation delay time, high- to low-level output	30	$\mu\text{s}$
$t_{en}$	Supply enable time	100	$\mu\text{s}$

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

### PARAMETER MEASUREMENT INFORMATION

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

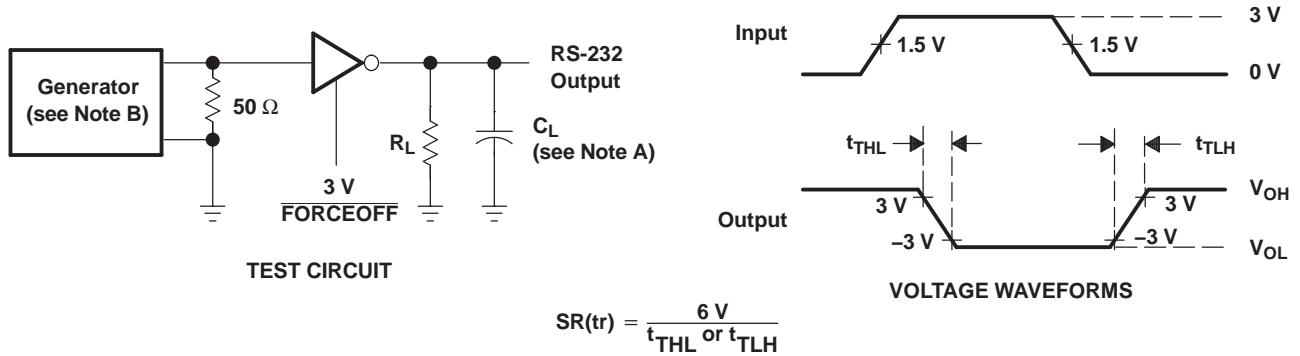


Figure 1. Driver Slew Rate

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

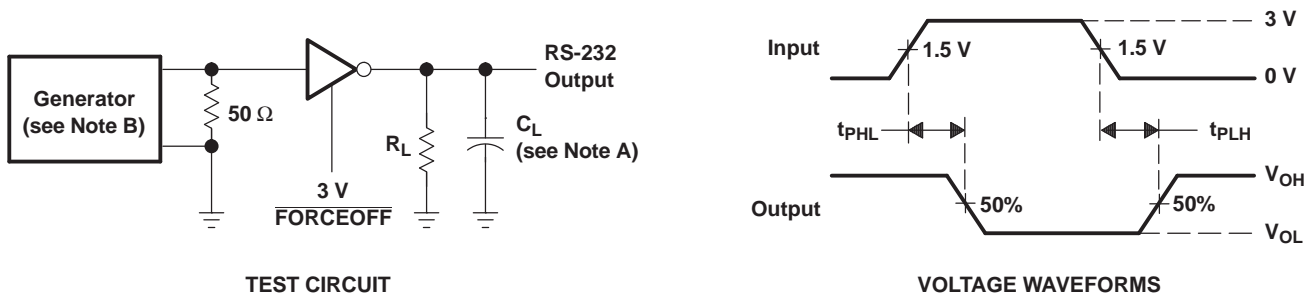


Figure 2. Driver Pulse Skew

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

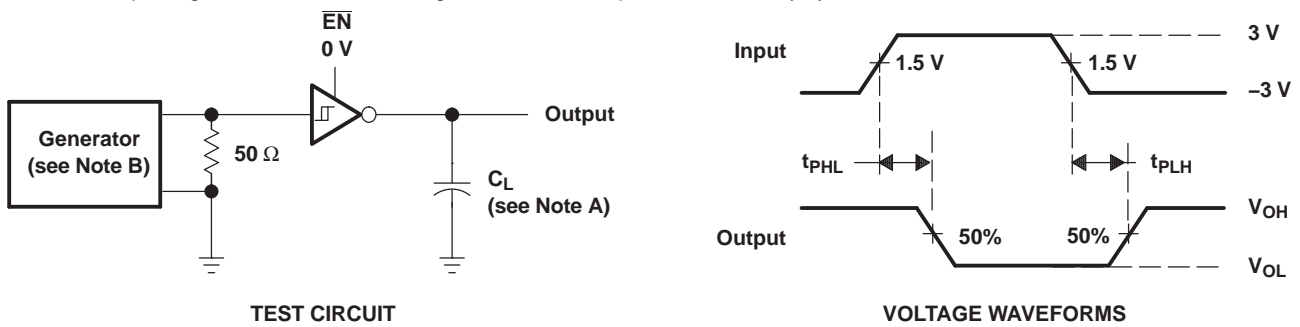


Figure 3. Receiver Propagation Delay Times

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

PARAMETER MEASUREMENT INFORMATION (continued)

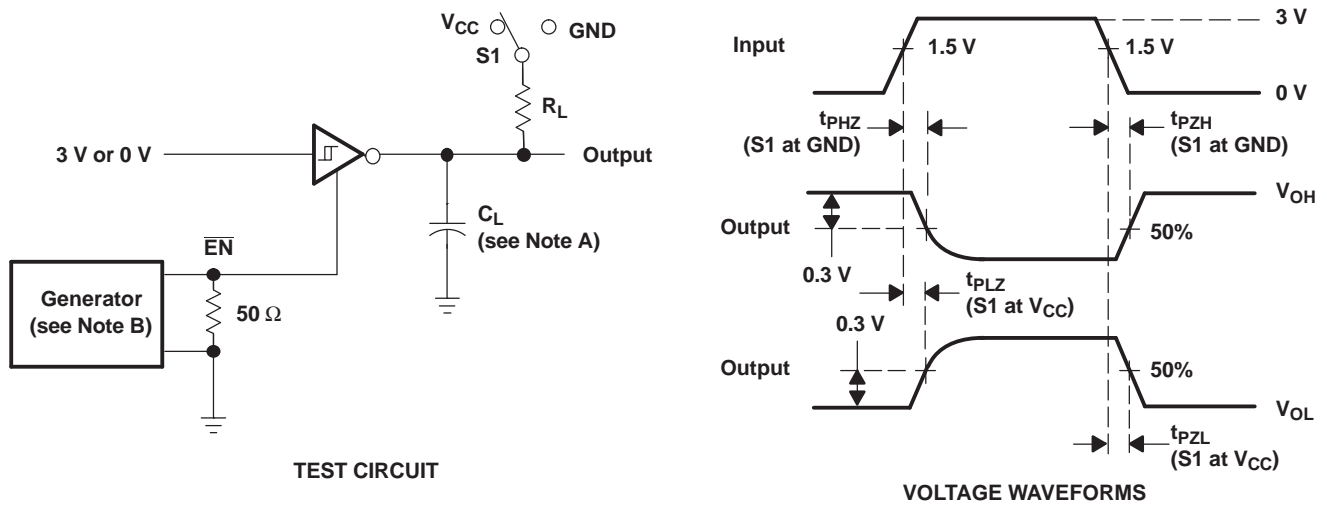
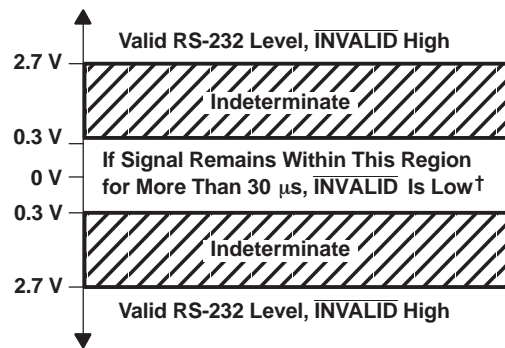
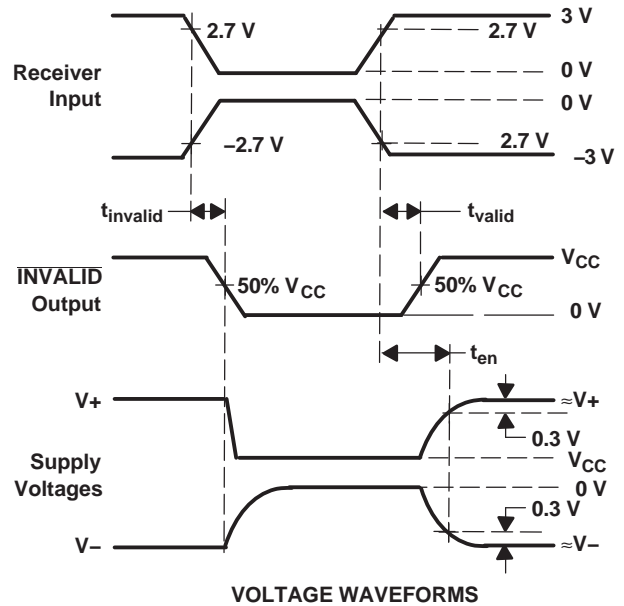
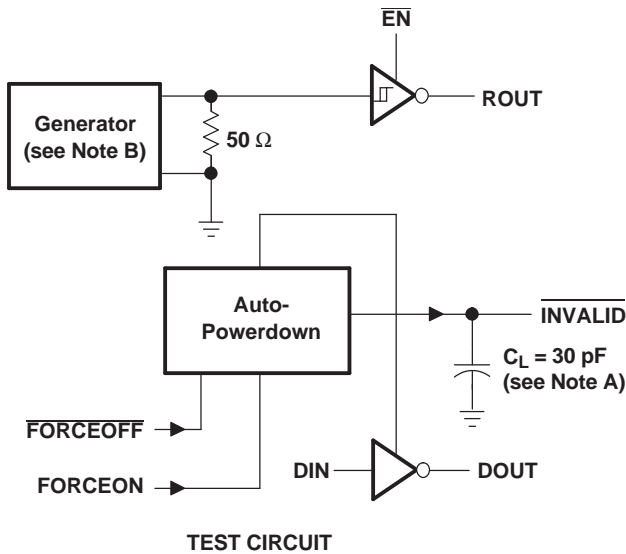


Figure 4. Receiver Enable and Disable Times

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

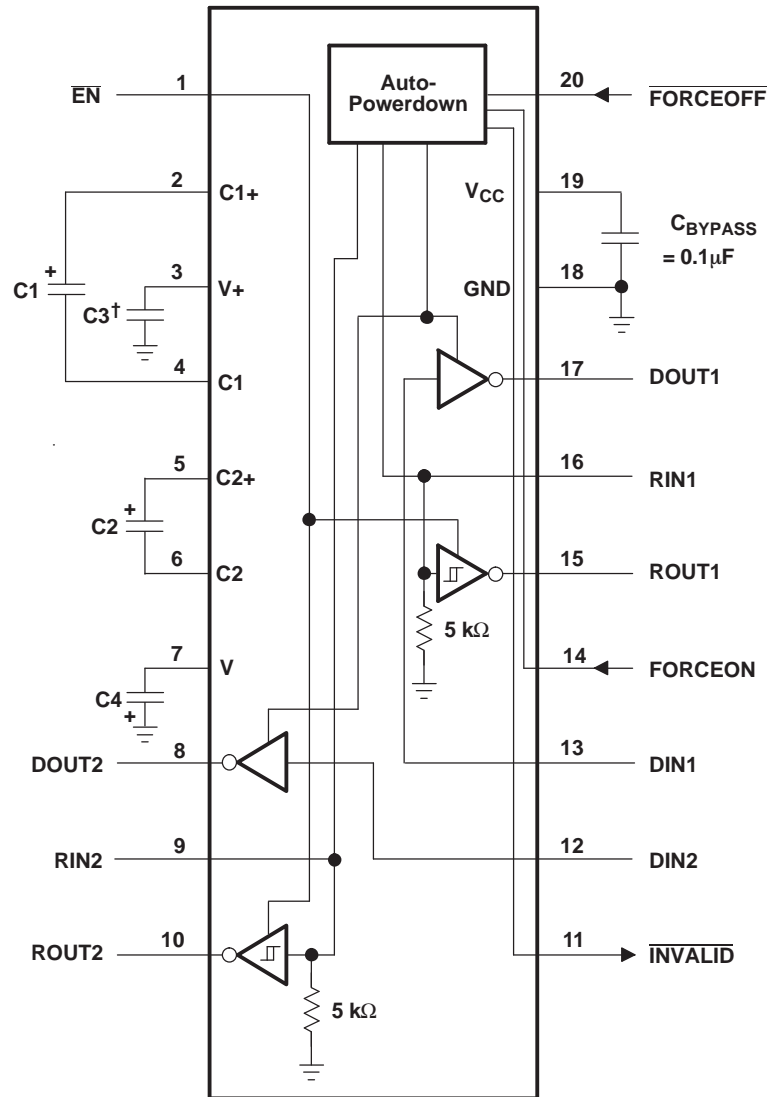
PARAMETER MEASUREMENT INFORMATION (continued)



† Auto-powerdown disables drivers and reduces supply current to 1  $\mu$ A

Figure 5.  $\overline{\text{INVALID}}$  Propagation Delay Times and Supply Enabling Time

APPLICATION INFORMATION



† C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V<sub>CC</sub> vs CAPACITOR VALUES

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 6. Typical Operating Circuit and Capacitor Values

### REVISION HISTORY

Changes from Original (August 2007) to Revision A	Page
• Added RGW package to datasheet. ....	1
• Deleted RHL package from datasheet. ....	1

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRSF3223ECDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RT23EC	<a href="#">Samples</a>
TRSF3223ECPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RT23EC	<a href="#">Samples</a>
TRSF3223EIDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI	<a href="#">Samples</a>
TRSF3223EIDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3223EI	<a href="#">Samples</a>
TRSF3223EIPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI	<a href="#">Samples</a>
TRSF3223EIPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI	<a href="#">Samples</a>
TRSF3223EIPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI	<a href="#">Samples</a>
TRSF3223EIRGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RT23EI	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3223ECDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRSF3223ECPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TRSF3223EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRSF3223EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TRSF3223EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TRSF3223EIRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3223ECDBR	SSOP	DB	20	2000	367.0	367.0	38.0
TRSF3223ECPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TRSF3223EIDBR	SSOP	DB	20	2000	367.0	367.0	38.0
TRSF3223EIDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TRSF3223EIPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TRSF3223EIRGWR	VQFN	RGW	20	3000	367.0	367.0	35.0

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

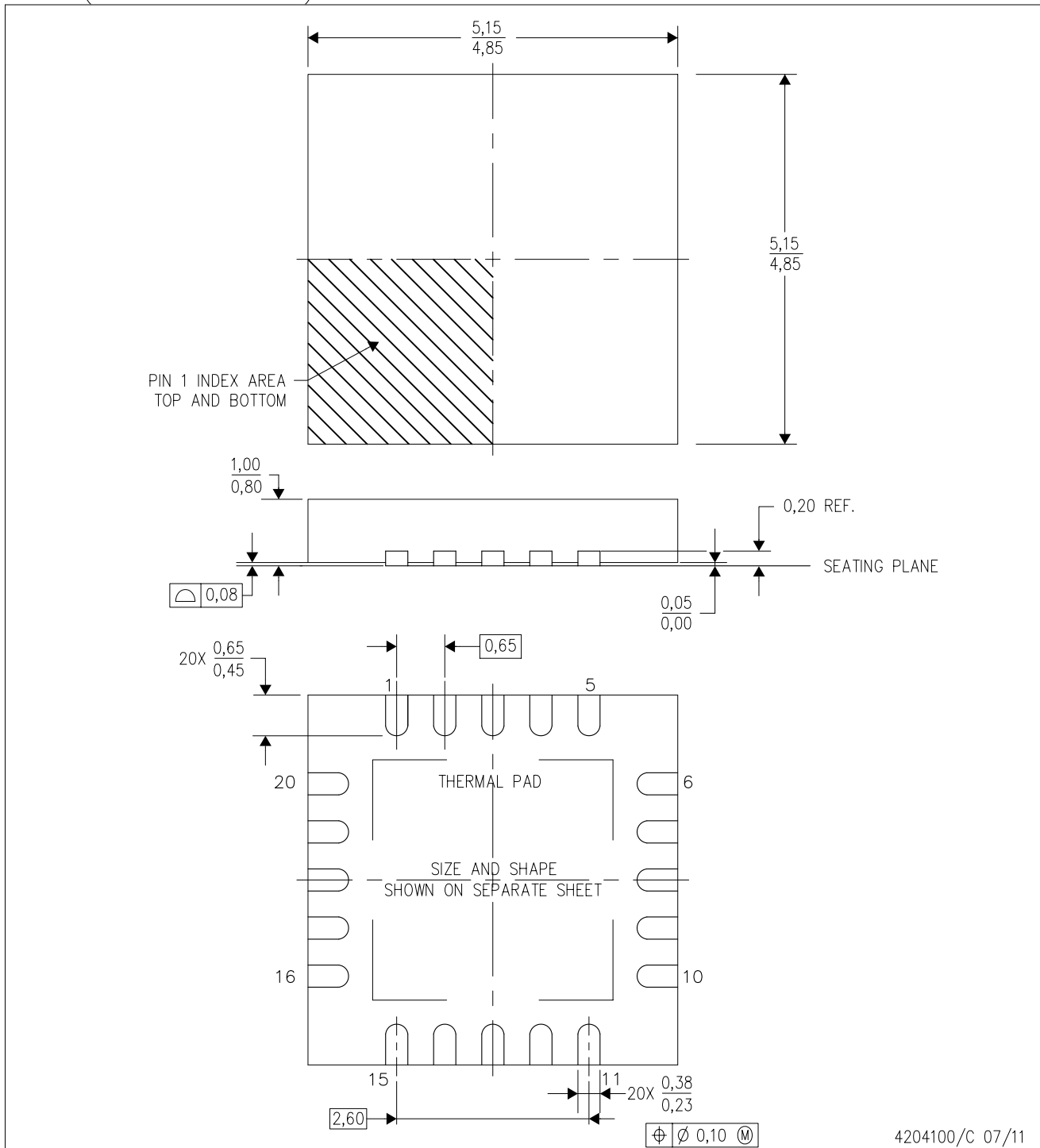
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

RGW (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD

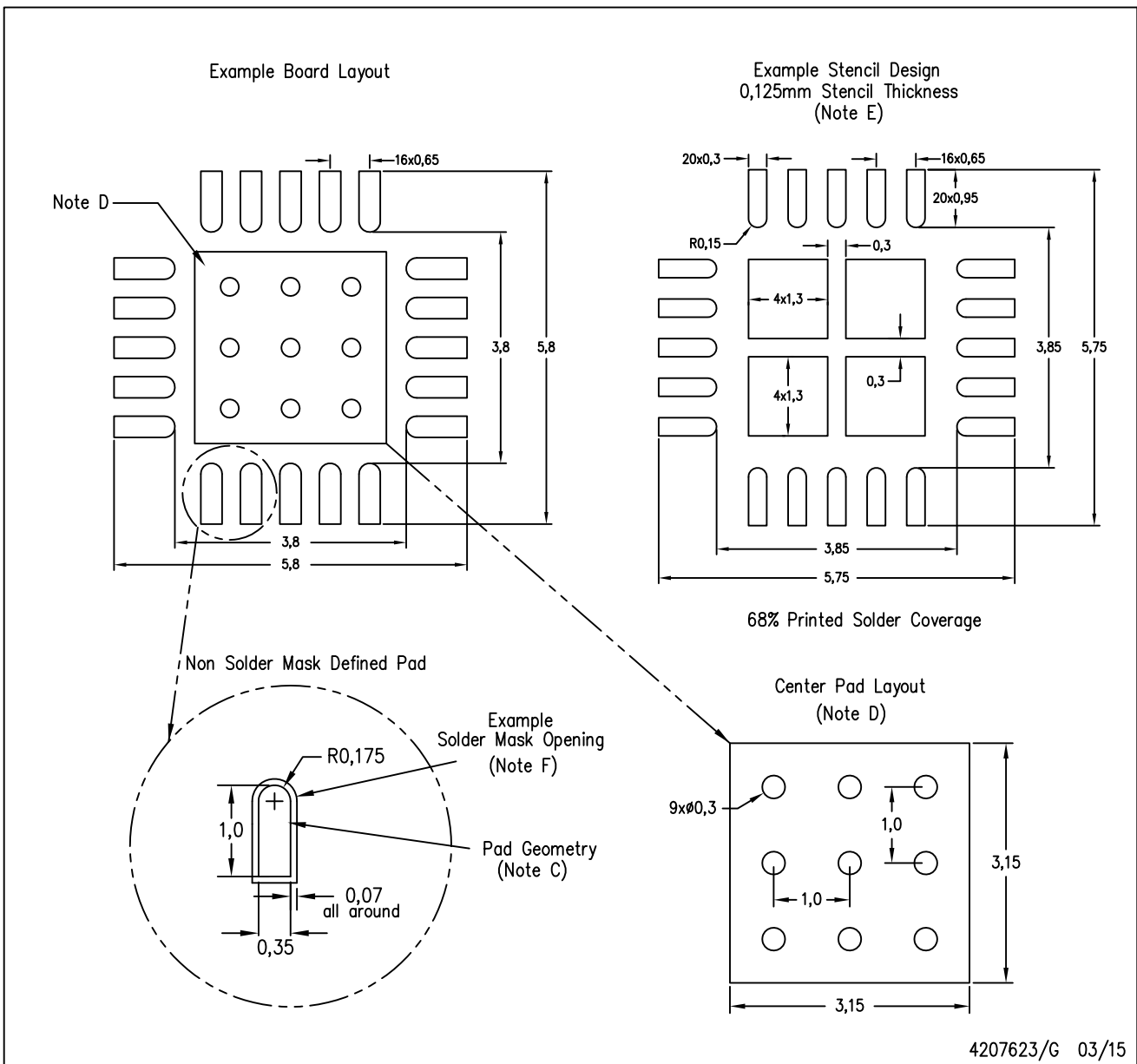


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flat pack, No-leads (QFN) package configuration
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.



RGW (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

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