



THE DATASHEET OF NLX2G66DMUTAG



NLX2G66

Dual Bilateral Analog Switch / Digital Multiplexer

The NLX2G66 is a dual single pole, single throw (SPST) analog switch / digital multiplexer. This single supply voltage IC is designed with a sub-micron CMOS technology to provide low propagation delays (t_{pd}) and ON resistance (R_{ON}), while maintaining low power dissipation. This bi-lateral switch can be used with either analog or digital signals that may vary across the full power supply range from V_{CC} to GND.

Features

- Wide V_{CC} Operating Range: 1.65 V to 5.5 V
- OVT up to +5.5 V for Control Pin
- R_{ON} : Typically 5.5 Ω at $V_{CC} = 4.5$ V and $I_S = 32$ mA
- Rail-to-Rail Input/Output
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- Ultra-Small Pb-Free, Halide-Free, RoHS-Compliant Packages
- ESD Performance: > 5000 V HBM, > 400 V MM

Typical Applications

- Cell Phones, PDAs, MP3 and other Portable Media Players

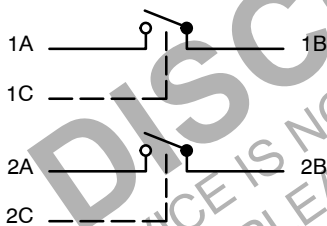


Figure 1. Analog Symbol

PIN ASSIGNMENTS

UDFN8	WLCSP8	Description
1	A1	1A
2	B1	1B
3	C1	2C
4	D1	GND
5	D2	2A
6	C2	2B
7	B2	1C
8	A2	V_{CC}



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MARKING DIAGRAMS

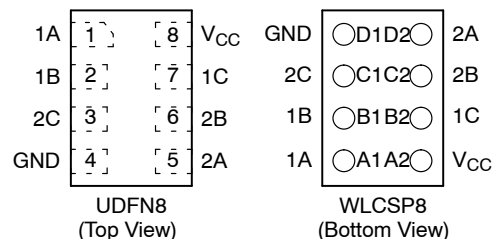


XX = Specific Device Code
M = Date Code
■ = Pb-Free Package



A = Assembly Location
Y = Year
WW = Work Week

PIN ASSIGNMENTS



FUNCTION TABLE

Control Input (C)	Switch
L	OFF
H	ON

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

NLX2G66

Table 1. MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CC}	Positive DC Supply Voltage	-0.5 to +7.0	V
V_S	Switch Input / Output Voltage (Pins 1A, 1B, 2A and 2B)	-0.5 to + V_{CC} + 0.5	V
V_I	Digital Control Input Voltage (Pins 1C and 2C)	-0.5 to +7.0	V
I_{OK}	I/O port diode current	± 50	mA
I_{IK}	Control input diode current	-50	mA
$I_{I/O}$	Continuous DC Current Through Analog Switch	± 100	mA
I_L	Latch-up Current, (Above V_{CC} and below GND at 125°C)	± 100	mA
T_s	Storage Temperature	-65 to +150	°C
V_{ESD}	ESD Withstand Voltage: Human Body Model (HBM) Machine Model (MM)	≥ 5000 > 400	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	1.65	5.5	V
V_S	Switch Input / Output Voltage (Pins 1A, 2A, 1B and 2B)	GND	V_{CC}	V
V_I	Digital Control Input Voltage (Pins 1C and 2C)	GND	5.5	V
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Transition Rise or Fall Time (ON/OFF Control Input)	$V_{CC} = < 3.0$ V 0	20	ns/V
		$V_{CC} = \geq 3.0$ V 0	10	

Table 3. ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit				Unit
				25°C		-55° to 125°C		
				Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage, Control Input		1.65 to 1.95			$V_{CC} \times 0.65$		V
			2.3 to 5.5			$V_{CC} \times 0.7$		
V_{IL}	Low-Level Input Voltage, Control Input		1.65 to 1.95			$V_{CC} \times 0.35$		V
			2.3 to 5.5			$V_{CC} \times 0.30$		
I_I	Input Leakage Current, Control Input	$V_I = V_{CC}$ or GND	5.5		± 0.1		± 1	μA
$I_{S(ON)}$	ON-State Switch Leakage Current	$V_{IS} = V_{CC}$ or GND, $V_I = V_{IH}$, $V_{OS} = \text{Open}$	5.5		± 0.1		± 1	μA
$I_{S(OFF)}$	OFF-State Switch Leakage Current	$V_{IS} = V_{CC}$ and $V_{OS} = \text{GND}$, or $V_{IS} = \text{GND}$ and $V_{OS} = V_{CC}$ GND, $V_I = V_{IL}$.	5.5		± 0.1		± 1	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	5.5		1.0		10	μA
ΔI_{CC}	Supply Current Change	$V_I = V_{CC} - 0.6$	5.5				500	μA
C_I	Control Input Capacitance		5				3.0	pF
$C_{I/O(OFF)}$	Switch OFF Input / Output Capacitance	See Figure 3	5				6.0	pF
$C_{I/O(ON)}$	Switch ON Input / Output Capacitance	See Figure 4	5				13	pF

NLX2G66

Table 4. SWITCHING CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC}	Guaranteed Limit		Unit
				-55° to 125°C		
				Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, A to B, B to A	C _L = 30 pF, R _L = 1 kΩ	1.8		6.5	ns
			2.5		3.3	
		C _L = 50 pF, R _L = 500 Ω	3.3		2.5	
			5.0		2.2	
t _{EN} (t _{PZL} , t _{PZH})	Enable Time, C to Analog Output (A or B)	C _L = 50 pF, R _L = 500 Ω See Figure 6	1.8		10	ns
			2.5		6.5	
			3.3		5.5	
			5.0		4.9	
t _{DIS} (t _{PLZ} , t _{PHZ})	Disable Time, C to Analog Output (A or B)	C _L = 50 pF, R _L = 500 Ω See Figure 6	1.8		9.0	ns
			2.5		7.2	
			3.3		6.5	
			5.0		6.0	

Table 5. ANALOG SWITCH CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC}	25°C	-55° to 125°C		Unit	
				Typ	Min	Max		
R _{ON}	On-Resistance	V _{IS} = V _{CC} or GND, V _I = V _{IH} , See Figure 2	I _S = 4 ma	1.65	12	30	Ω	
				I _S = 8 ma	2.3	9		20
				I _S = 24 ma	3.0	7.5		15
				I _S = 32 ma	4.5	5.5		13
R _{ON(peak)}	Peak On-Resistance	V _{IS} = GND to V _{CC} ; V _I = V _{IH} , See Figure 2	I _S = 4 ma	1.65	74.5	220	Ω	
				I _S = 8 ma	2.3	20		75
				I _S = 24 ma	3.0	11.5		25
				I _S = 32 ma	4.5	7.5		17
ΔR _{ON}	On-Resistance Mismatch between Switches	V _{IS} = GND to V _{CC} ; V _I = V _{IH} , See Figure 2	I _S = 4 ma	1.65		8.0	Ω	
				I _S = 8 ma	2.3			5.0
				I _S = 24 ma	3.0			3.0
				I _S = 32 ma	4.5			2.0
BW	Bandwidth (f _{-3dB})	R _L = 50 Ω, C _L = 5 pF, f _N = Sine Wave See Figure 8	1.65			> 270	MHz	
				2.3		> 270		
				3.0		> 270		
				4.5		> 270		

NLX2G66

Table 5. ANALOG SWITCH CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	V _{CC}	25°C	Unit
				Typ	
ISO _{Off}	Off-Channel Feedthrough Isolation	R _L = 600 Ω, C _L = 50 pF, f _{IN} = 1 MHz Sine Wave See Figure 9	1.65	-70	dB
			2.3	-70	
			3.0	-70	
			4.5	-70	
		R _L = 50 Ω, C _L = 5 pF, f _{IN} = 1 MHz Sine Wave See Figure 9	1.65	-60	
			2.3	-60	
			3.0	-60	
			4.5	-60	
XTalk	Crosstalk Between Switches	R _L = 600 Ω, C _L = 50 pF, f _{IN} = 1 MHz Sine Wave See Figure 10	1.65	-100	dB
			2.3	-100	
			3.0	-100	
			4.5	-100	
		R _L = 50 Ω, C _L = 5 pF, f _{IN} = 1 MHz Sine Wave See Figure 10	1.65	-90	
			2.3	-90	
			3.0	-90	
			4.5	-90	
	Feedthrough Noise, Control to Switch	R _L = 600 Ω, C _L = 50 pF, f _{IN} = 1 MHz Square Wave, t _r = t _f = 2 ns, See Figure 11	1.65	10	mV _{pp}
			2.3	10	
			3.0	10	
			4.5	15	
THD	Total Harmonic Distortion	C _L = 50 pF, R _L = 50 Ω, f _{IN} = 600 Hz to 20 KHz Sine Wave, See Figure 12	2.3	0.025	%
			3.0	0.015	
			4.5	0.01	

Table 6. POWER DISSIPATION CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC}	25°C	Unit
				Typ	
C _{PD}	Power Dissipation Capacitance	f = 10 MHz	1.65	8.0	pF
			2.3	8.9	
			3.0	9.6	
			4.5	10.9	

NLX2G66

Table 7. DEVICE ORDERING INFORMATION

Device Order Number	Package	Shipping†
NLX2G66DMUTAG	UDFN8-0.5P, 1.95 mm x 1.0 mm (Pb-Free)	3000 / Tape & Reel
NLX2G66DMUTCG	UDFN8-0.5P, 1.95 mm x 1.0 mm (Pb-Free)	3000 / Tape & Reel
NLX2G66MU3TCG (In Development)	UDFN8-0.35P, 1.45 mm x 1.0 mm (Pb-Free)	3000 / Tape & Reel
NLX2G66FCTAG	WLCSP8, 1.888 mm x 0.888 mm (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

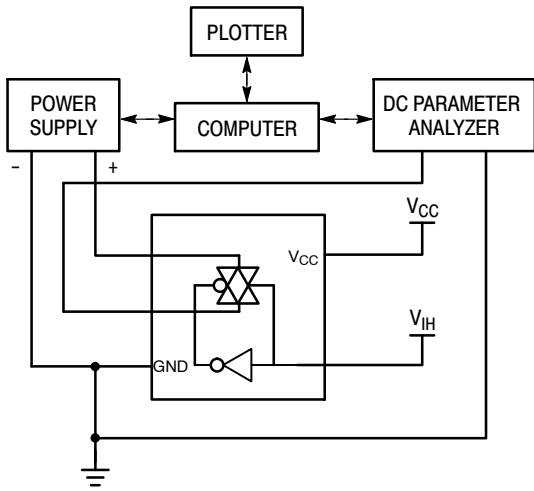


Figure 2. On Resistance Test Set-Up

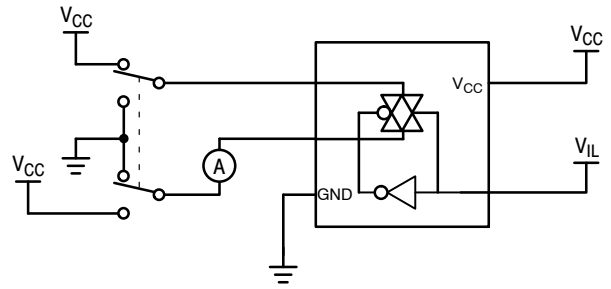


Figure 3. Maximum Off-Channel Leakage Current Test Set-Up

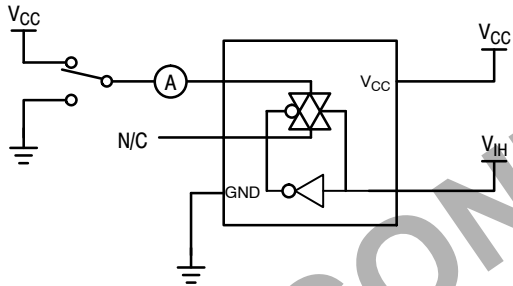


Figure 4. Maximum On-Channel Leakage Current Test Set-Up

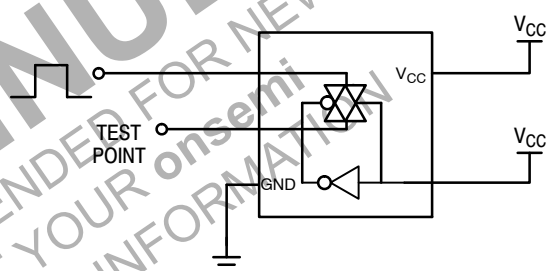
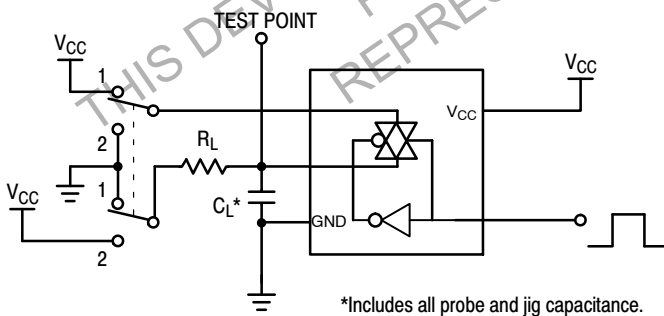


Figure 5. Propagation Delay Test Set-Up

Switch to Position 2 when testing t_{PLZ} and t_{PZL}
 Switch to Position 1 when testing t_{PHZ} and t_{PZH}



*Includes all probe and jig capacitance.

Figure 6. Propagation Delay Output Enable/Disable Test Set-Up

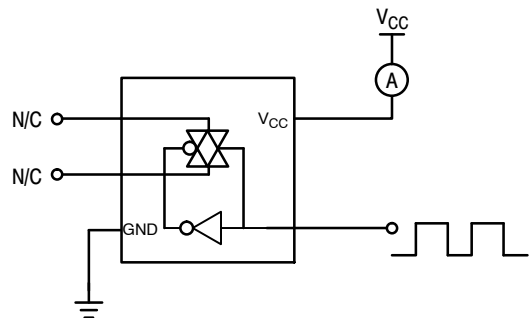


Figure 7. Power Dissipation Capacitance Test Set-Up

NLX2G66

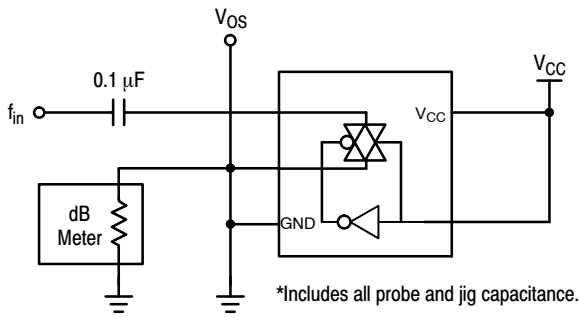


Figure 8. Maximum On-Channel Bandwidth Test Set-Up

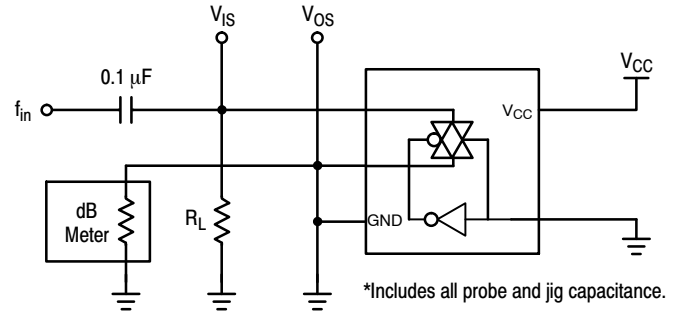


Figure 9. Off-Channel Feedthrough Isolation Test Set-Up

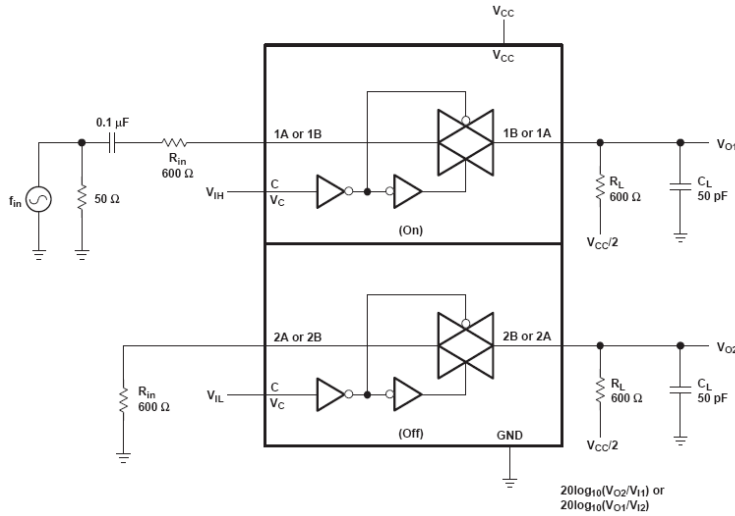


Figure 10. Crosstalk (between Switches)

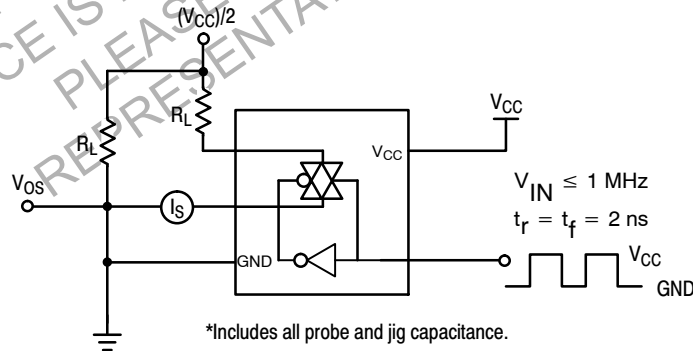


Figure 11. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

NLX2G66

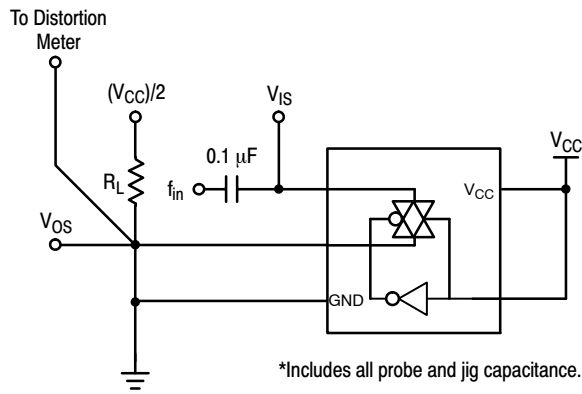


Figure 12. Total Harmonic Distortion Test Set-Up

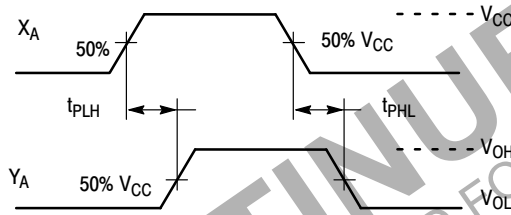


Figure 13. Propagation Delay, Analog In to Analog Out Waveforms

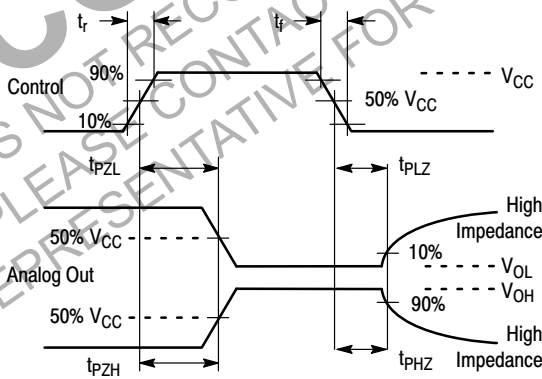


Figure 14. Propagation Delay, ON/OFF Control

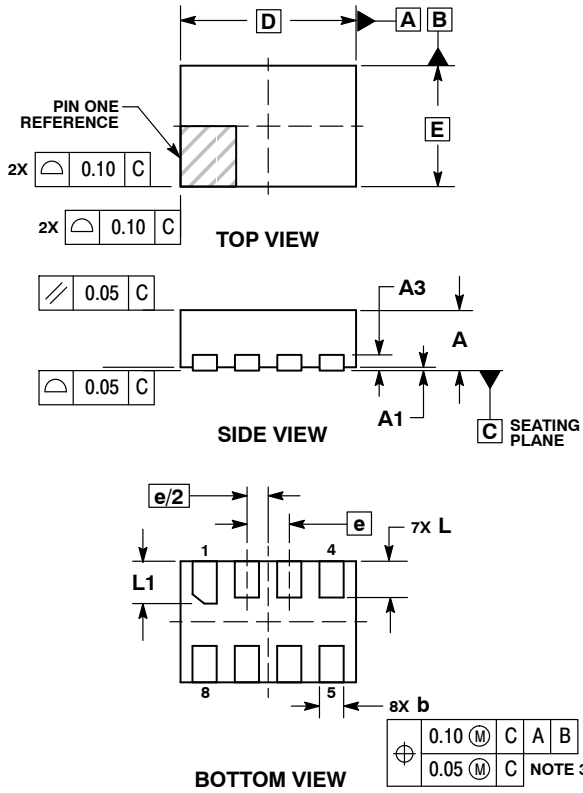
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



UDFN8, 1.45x1.00, 0.35P
CASE 517BZ
ISSUE O

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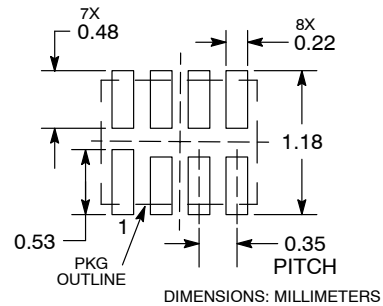
DATE 18 MAY 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
 4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

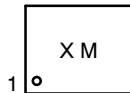
MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.45	BSC
E	1.00	BSC
e	0.35	BSC
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present. Some products may not follow the Generic Marking.

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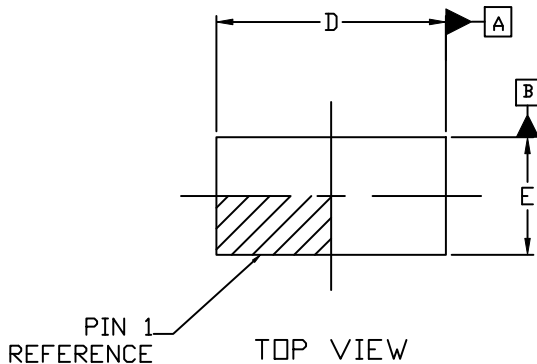
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



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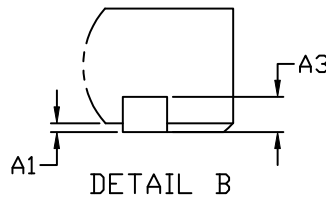
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CASE 517CA
ISSUE A

DATE 22 SEP 2020

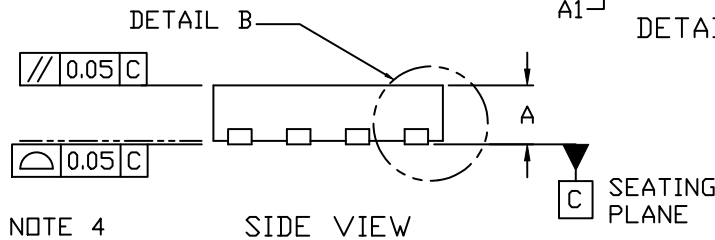


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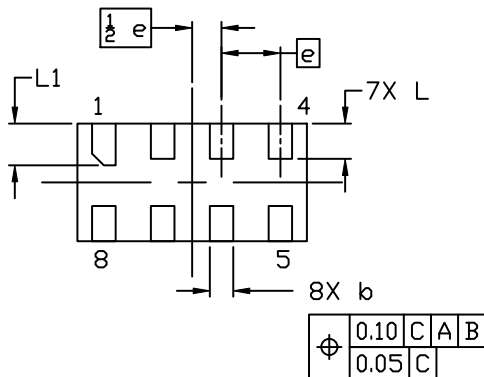
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
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3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO ALL THE TERMINALS.
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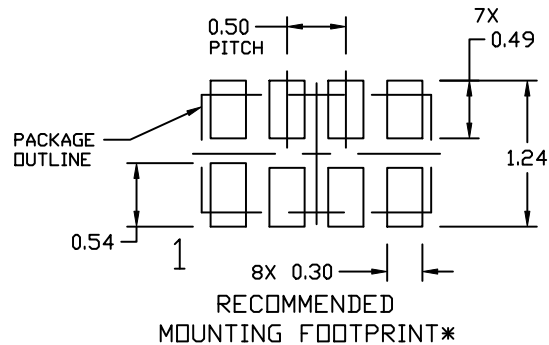
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3	0.13 REF		
b	0.15	0.20	0.25
D	1.85	1.95	2.05
E	0.90	1.00	1.10
e	0.50 BSC		
L	0.25	0.30	0.35
L1	0.30	0.35	0.40



NOTE 4

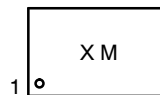


BOTTOM VIEW NOTE 3



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

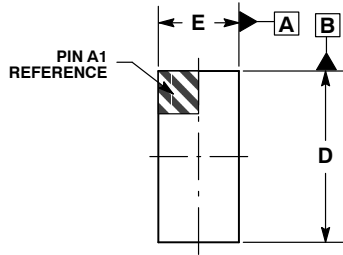
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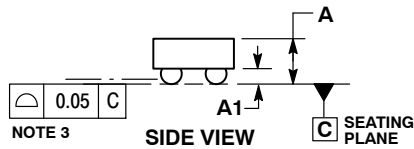
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CASE 567MR
ISSUE A

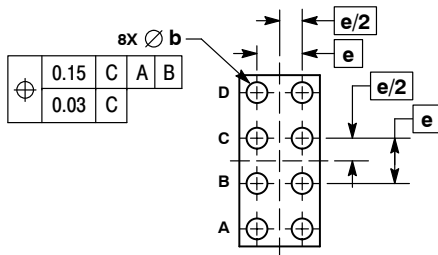
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TOP VIEW



SIDE VIEW



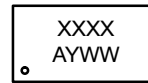
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.50
A1	0.15	0.19
b	0.21	0.25
D	1.858	1.918
E	0.858	0.918
e	0.50 BSC	

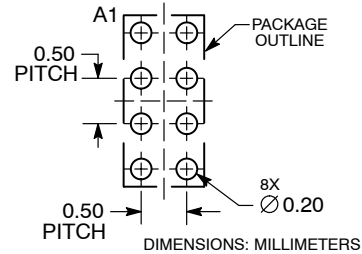
GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	WLCSP8, 1.888X0.888	PAGE 1 OF 6

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