



**THE DATASHEET OF
IPTG039N15NM5ATMA1**



MOSFET

OptiMOS™ 5 Power-Transistor, 150 V

Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

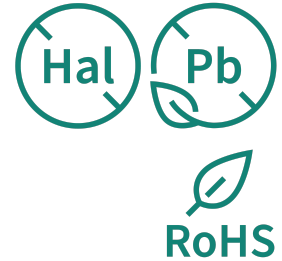
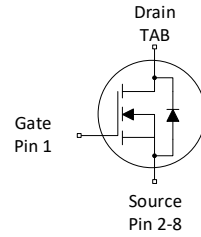
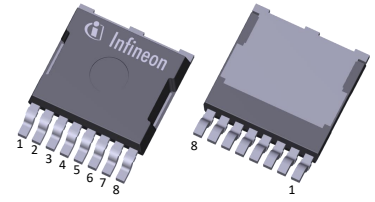
Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|------------------|-------|------------|
| V_{DS} | 150 | V |
| $R_{DS(on),max}$ | 3.9 | m Ω |
| I_D | 190 | A |
| Q_{oss} | 207 | nC |
| Q_G | 74 | nC |

PG-HSOG-8



| Type/Ordering Code | Package | Marking | Related Links |
|--------------------|-----------|----------|---------------|
| IPTG039N15NM5 | PG-HSOG-8 | 039N15N5 | - |



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1 Maximum ratings

unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|--|----------------|--------|------|-------------------------|------|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 190 134 128 21 | A | $V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=8\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=40\text{ °C/W}^2)$ |
| Pulsed drain current ³⁾ | $I_{D,pulse}$ | - | - | 760 | A | $T_A=25\text{ °C}$ |
| Avalanche energy, single pulse ⁴⁾ | E_{AS} | - | - | 344 | mJ | $I_D=100\text{ A}, R_{GS}=25\text{ }\Omega$ |
| Gate source voltage | V_{GS} | -20 | - | 20 | V | - |
| Power dissipation | P_{tot} | - | - | 319 3.8 | W | $T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=40\text{ °C/W}^2)$ |
| Operating and storage temperature | T_j, T_{stg} | -55 | - | 175 | °C | - |

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|------------|--------|------|------|------|----------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 0.47 | °C/W | - |
| Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾ | R_{thJA} | - | - | 40 | °C/W | - |
| Thermal resistance, junction - ambient, minimal footprint | R_{thJA} | - | - | 62 | °C/W | - |

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|----------------------------------|---------------|--------|------------|------------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 150 | - | - | V | $V_{GS}=0\text{ V}, I_D=1\text{ mA}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 3.0 | 3.8 | 4.6 | V | $V_{DS}=V_{GS}, I_D=243\text{ }\mu\text{A}$ |
| Zero gate voltage drain current | I_{DSS} | - | 0.1 10 | 1.0 100 | μA | $V_{DS}=120\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$ $V_{DS}=120\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}$ |
| Gate-source leakage current | I_{GSS} | - | 10 | 100 | nA | $V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 3.5 3.8 | 3.9 4.3 | m Ω | $V_{GS}=10\text{ V}, I_D=50\text{ A}$ $V_{GS}=8\text{ V}, I_D=25\text{ A}$ |
| Gate resistance ⁶⁾ | R_G | - | 1.1 | 1.6 | Ω | - |
| Transconductance | g_{fs} | - | 110 | - | S | $ V_{DS} \geq 2 I_D R_{DS(on)max}, I_D=50\text{ A}$ |

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|--|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance ⁷⁾ | C_{iss} | - | 5600 | 7300 | pF | $V_{GS}=0\text{ V}, V_{DS}=75\text{ V}, f=1\text{ MHz}$ |
| Output capacitance ⁷⁾ | C_{oss} | - | 1400 | 1930 | pF | $V_{GS}=0\text{ V}, V_{DS}=75\text{ V}, f=1\text{ MHz}$ |
| Reverse transfer capacitance ⁷⁾ | C_{rss} | - | 31 | 55 | pF | $V_{GS}=0\text{ V}, V_{DS}=75\text{ V}, f=1\text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | - | 19 | - | ns | $V_{DD}=75\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$ |
| Rise time | t_r | - | 4.5 | - | ns | $V_{DD}=75\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$ |
| Turn-off delay time | $t_{d(off)}$ | - | 23.5 | - | ns | $V_{DD}=75\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$ |
| Fall time | t_f | - | 5.5 | - | ns | $V_{DD}=75\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$ |

⁷⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁸⁾

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|------------------------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 30 | - | nC | $V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge at threshold | $Q_{g(th)}$ | - | 21 | - | nC | $V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$ |
| Gate to drain charge ⁹⁾ | Q_{gd} | - | 15 | 22 | nC | $V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$ |
| Switching charge | Q_{sw} | - | 23 | - | nC | $V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total ⁹⁾ | Q_g | - | 74 | 93 | nC | $V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$ |
| Gate plateau voltage | $V_{plateau}$ | - | 5.4 | - | V | $V_{DD}=75\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$ |
| Output charge ⁹⁾ | Q_{oss} | - | 207 | 275 | nC | $V_{DS}=75\text{ V}, V_{GS}=0\text{ V}$ |

⁸⁾ See "Gate charge waveforms" for parameter definition

⁹⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|--|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | I_S | - | - | 190 | A | $T_C=25\text{ °C}$ |
| Diode pulse current | $I_{S,pulse}$ | - | - | 760 | A | $T_C=25\text{ °C}$ |
| Diode forward voltage | V_{SD} | - | 0.81 | 1.0 | V | $V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$ |
| Reverse recovery time ¹⁰⁾ | t_{rr} | - | 53.5 | 107 | ns | $V_R=75\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$ |
| Reverse recovery charge ¹⁰⁾ | Q_{rr} | - | 77 | 155 | nC | $V_R=75\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$ |

¹⁰⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

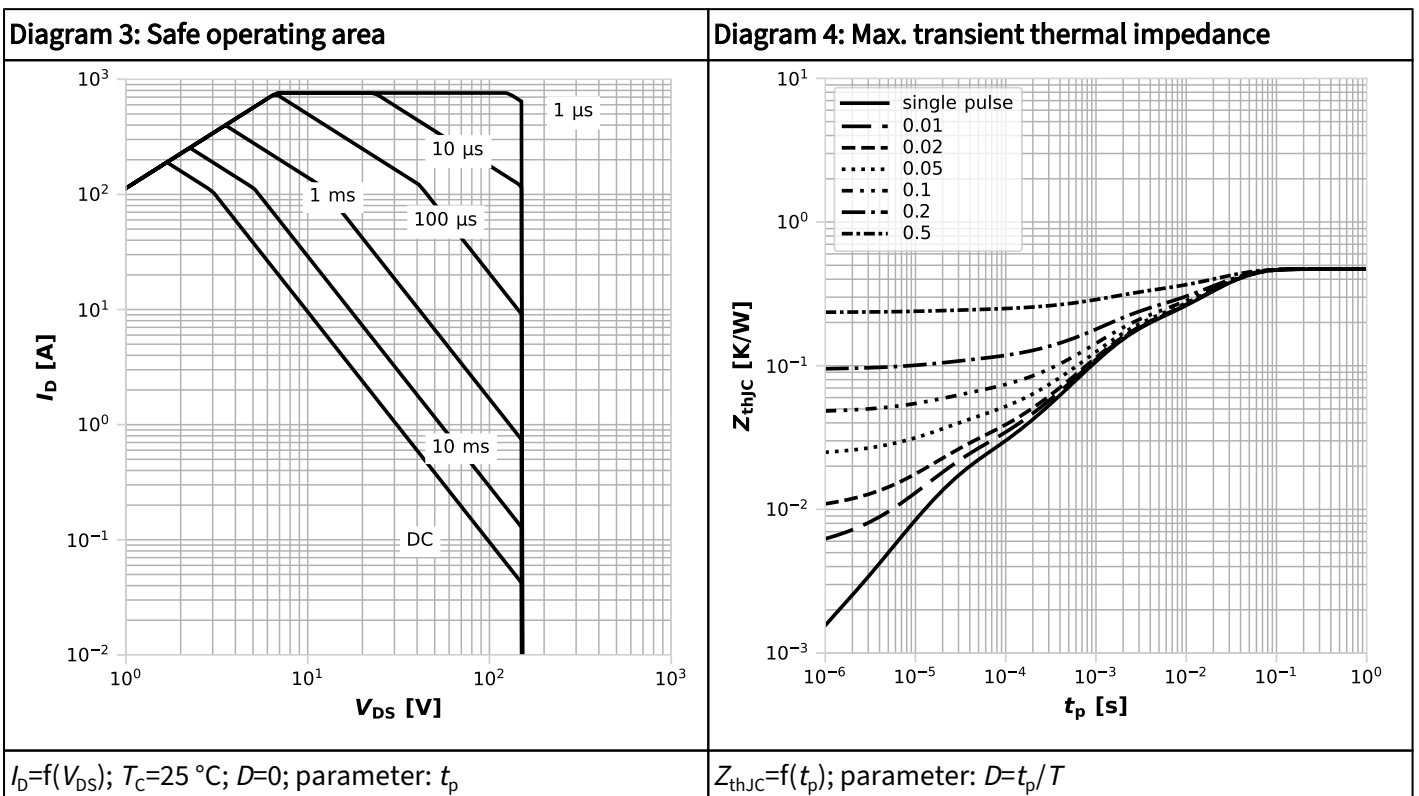
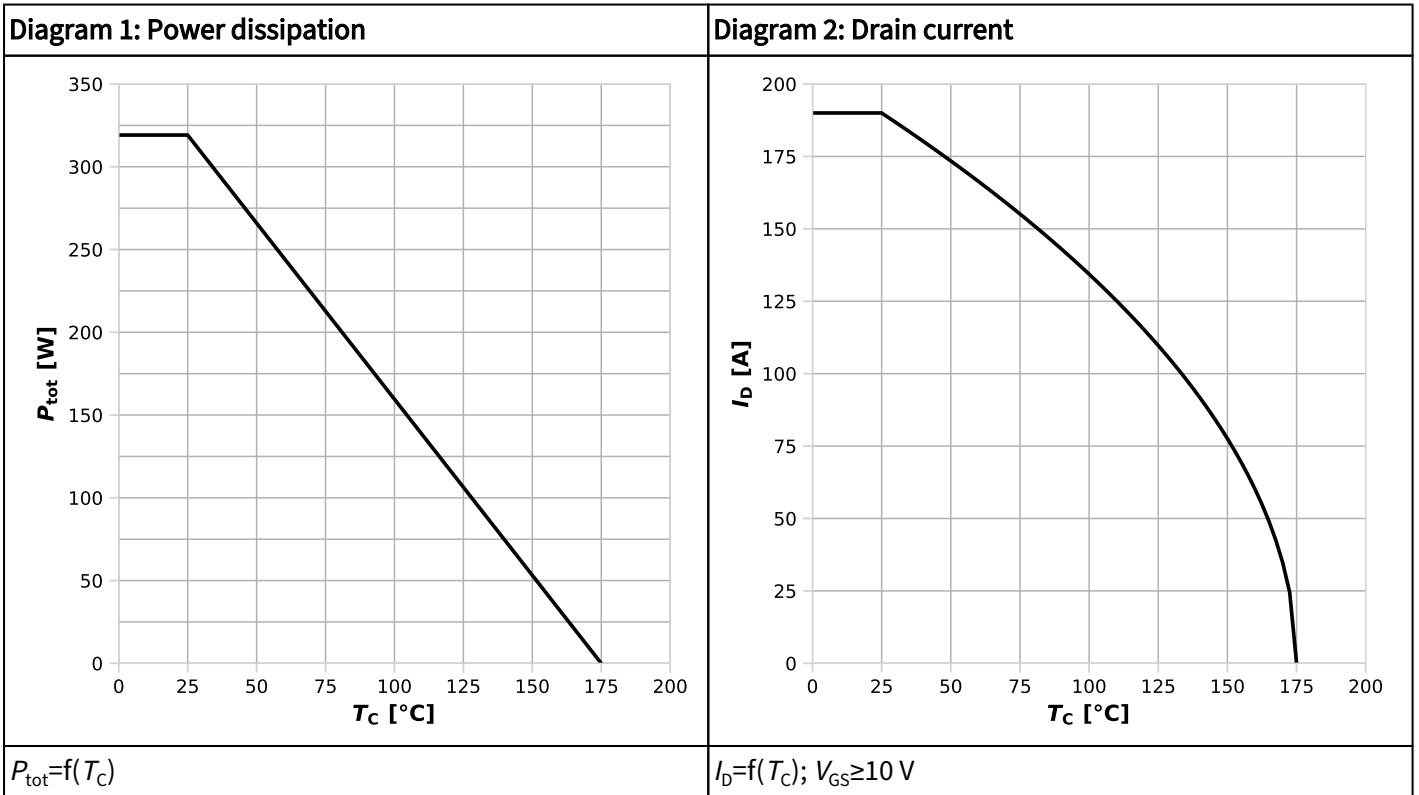
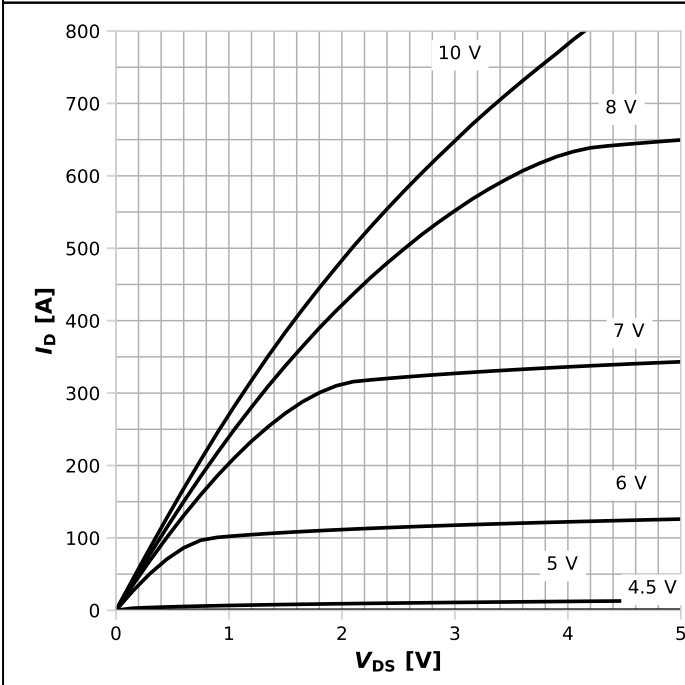
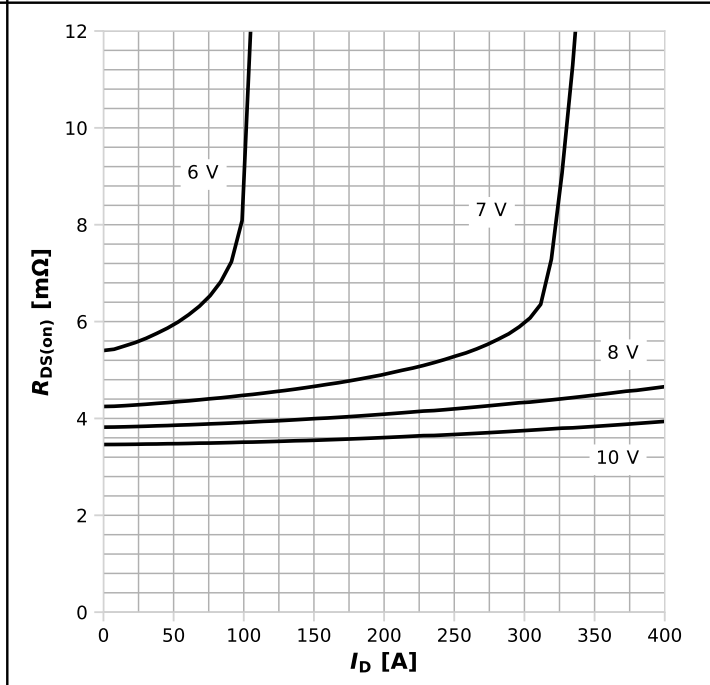


Diagram 5: Typ. output characteristics



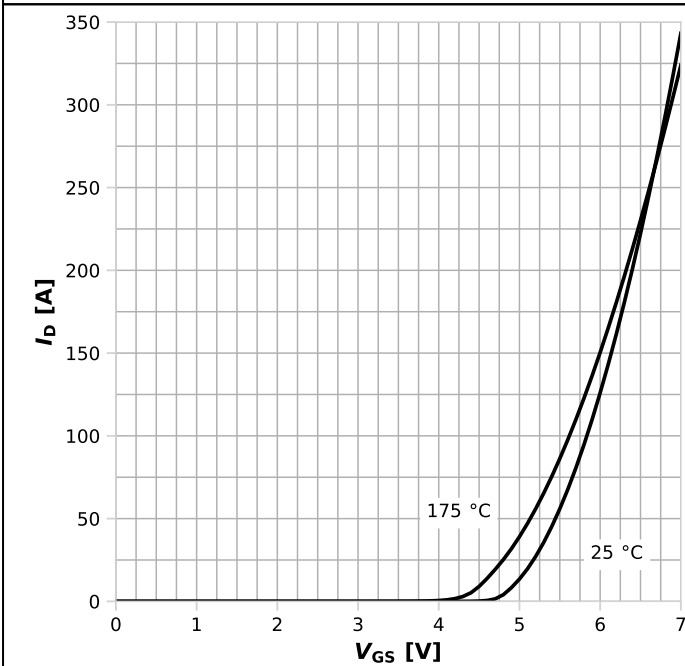
$I_D = f(V_{DS}), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



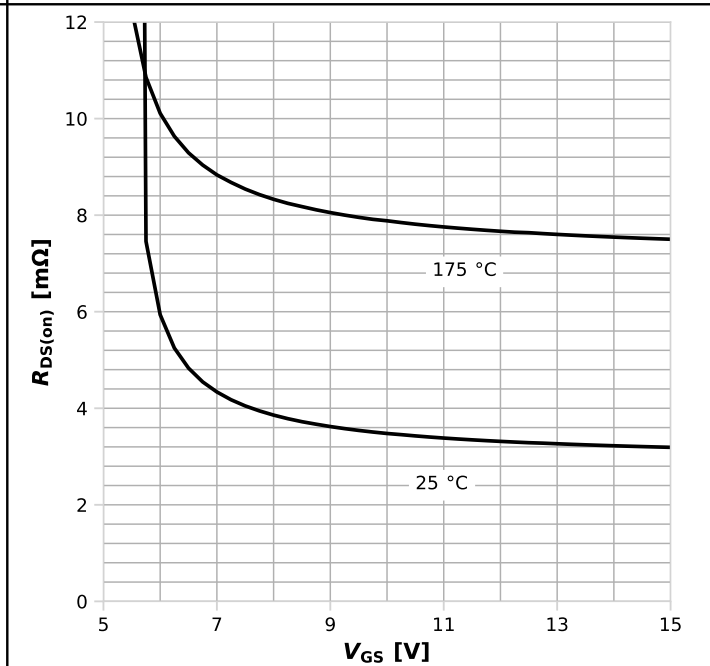
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



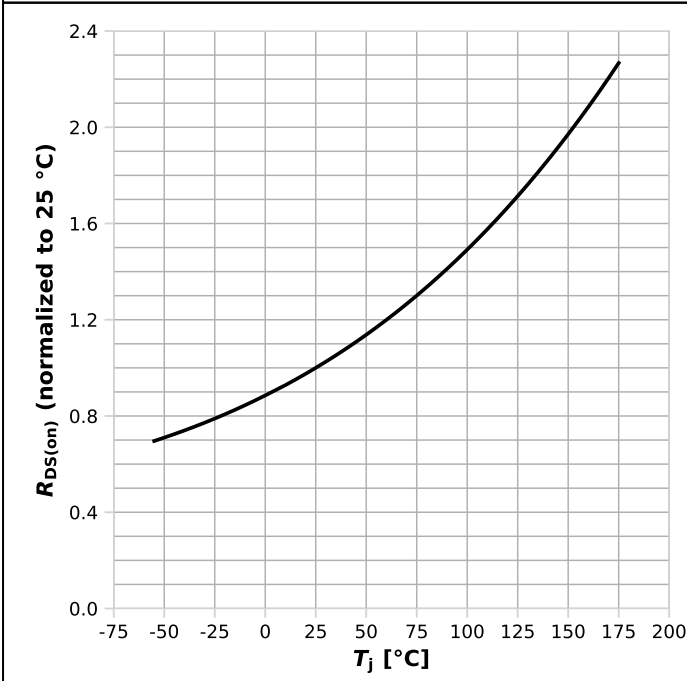
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. drain-source on resistance



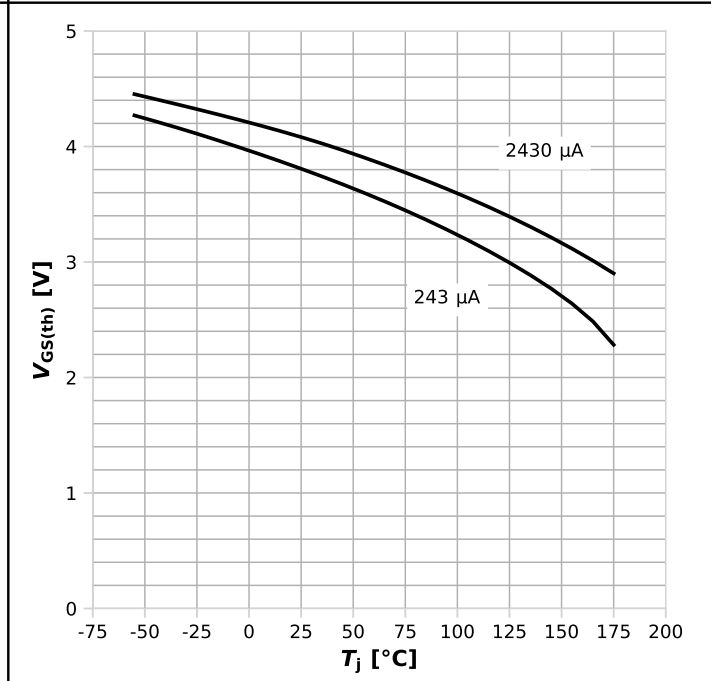
$R_{DS(on)} = f(V_{GS}), I_D = 50\text{ A};$ parameter: T_j

Diagram 9: Normalized drain-source on resistance



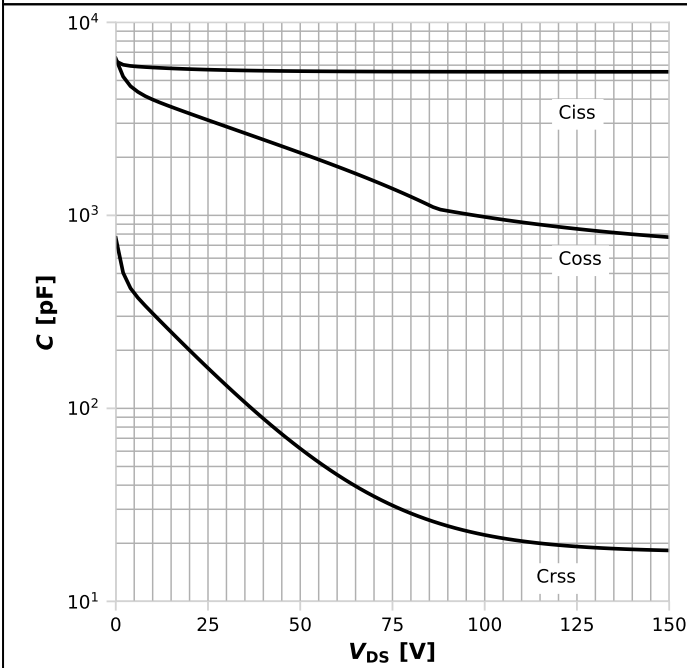
$R_{DS(on)}=f(T_j), I_D=50\text{ A}, V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



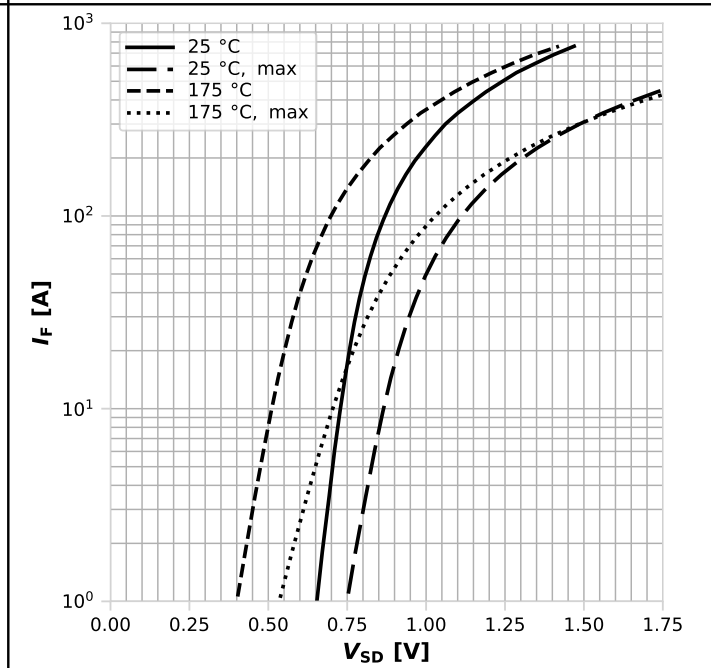
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS};$ parameter: I_D

Diagram 11: Typ. capacitances



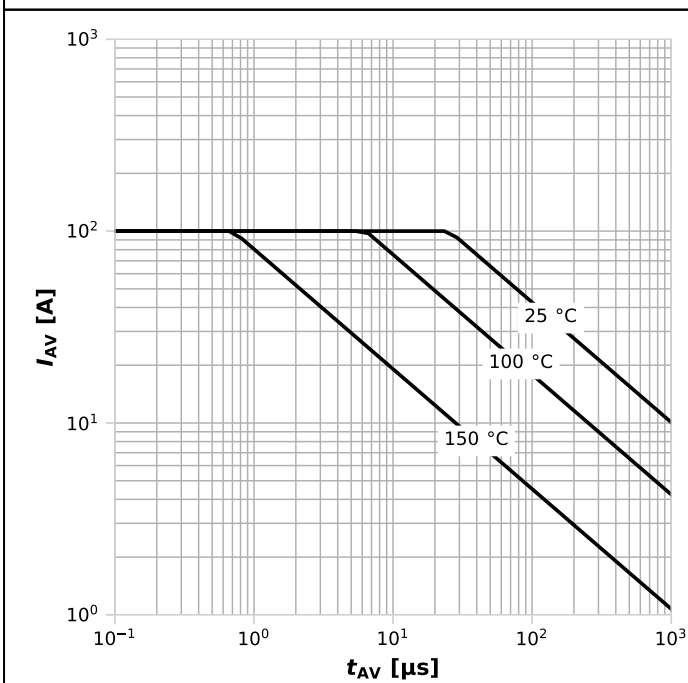
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



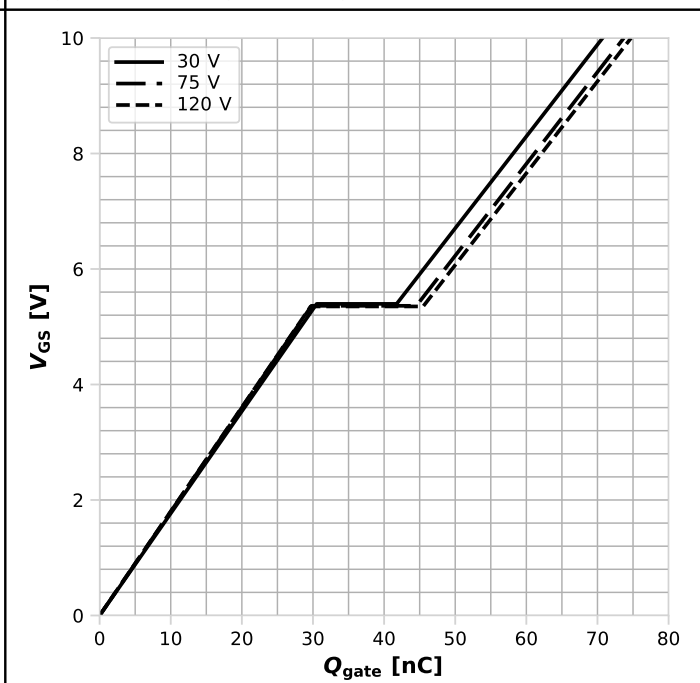
$I_F=f(V_{SD});$ parameter: T_j

Diagram 13: Avalanche characteristics



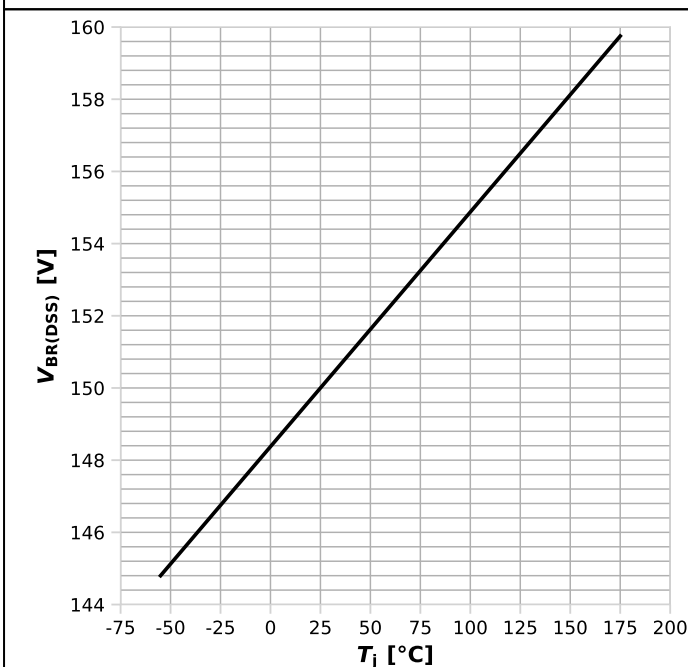
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



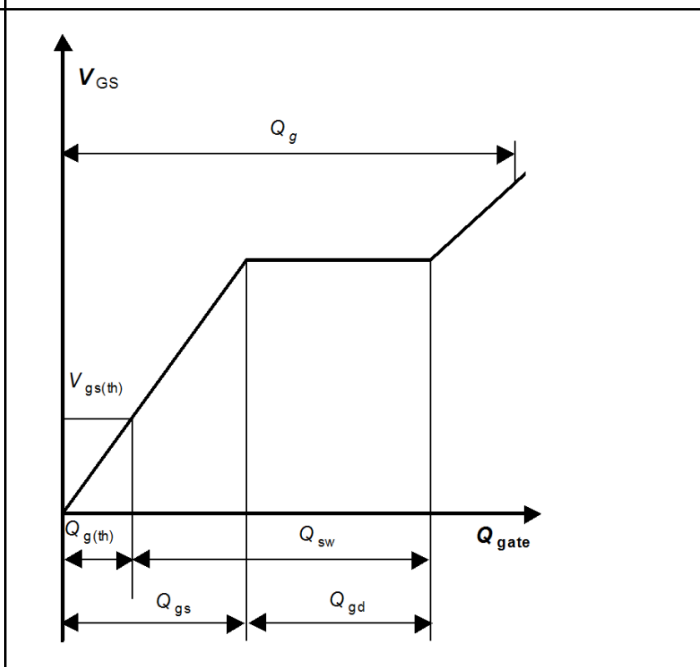
$V_{GS}=f(Q_{gate}), I_D=50$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



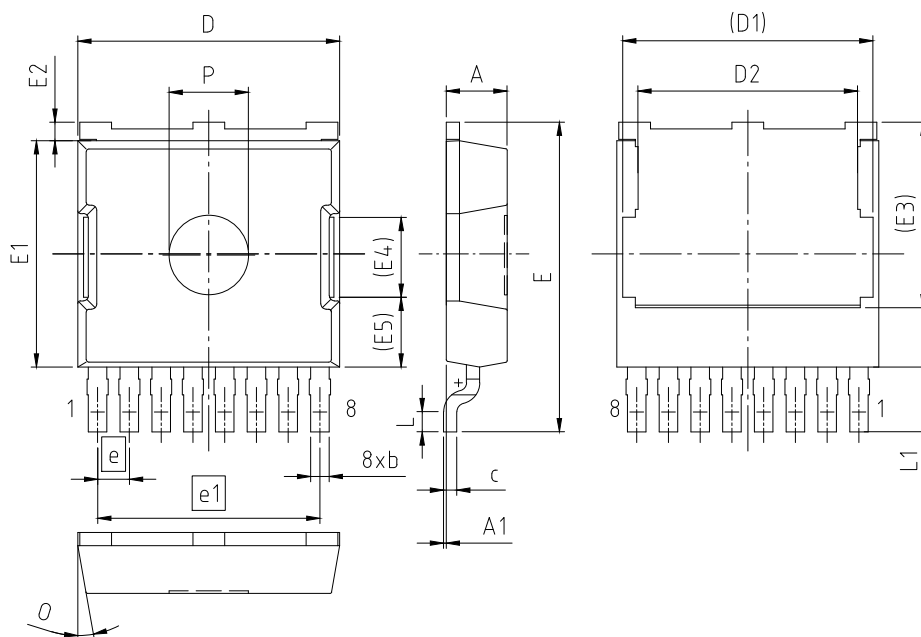
$V_{BR(DSS)}=f(T_j); I_D=1$ mA

Gate charge waveforms



-

5 Package Outlines



| PACKAGE - GROUP NUMBER: PG-HSOG-8-U01 | | | | | |
|--|-------------|-------|------------|-------------|------|
| DIMENSIONS | MILLIMETERS | | DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. | | MIN. | MAX. |
| A | 2.20 | 2.40 | e | 1.20 | |
| A1 | 0.00 | 0.10 | e1 | 8.40 | |
| b | 0.60 | 0.80 | L | 0.66 | 0.86 |
| c | 0.40 | 0.60 | L1 | 2.44 | 2.74 |
| D | 9.70 | 10.10 | O | 8° | 12° |
| D1 | 9.46 | | P | 2.90 | 3.10 |
| D2 | 8.20 | 8.40 | | | |
| E | 11.50 | 11.90 | | | |
| E1 | 8.45 | 8.75 | | | |
| E2 | 0.50 | 0.90 | | | |
| E3 | 7.01 | | | | |
| E4 | 3.02 | | | | |
| E5 | 2.64 | | | | |

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-HSOG-8, dimensions in mm

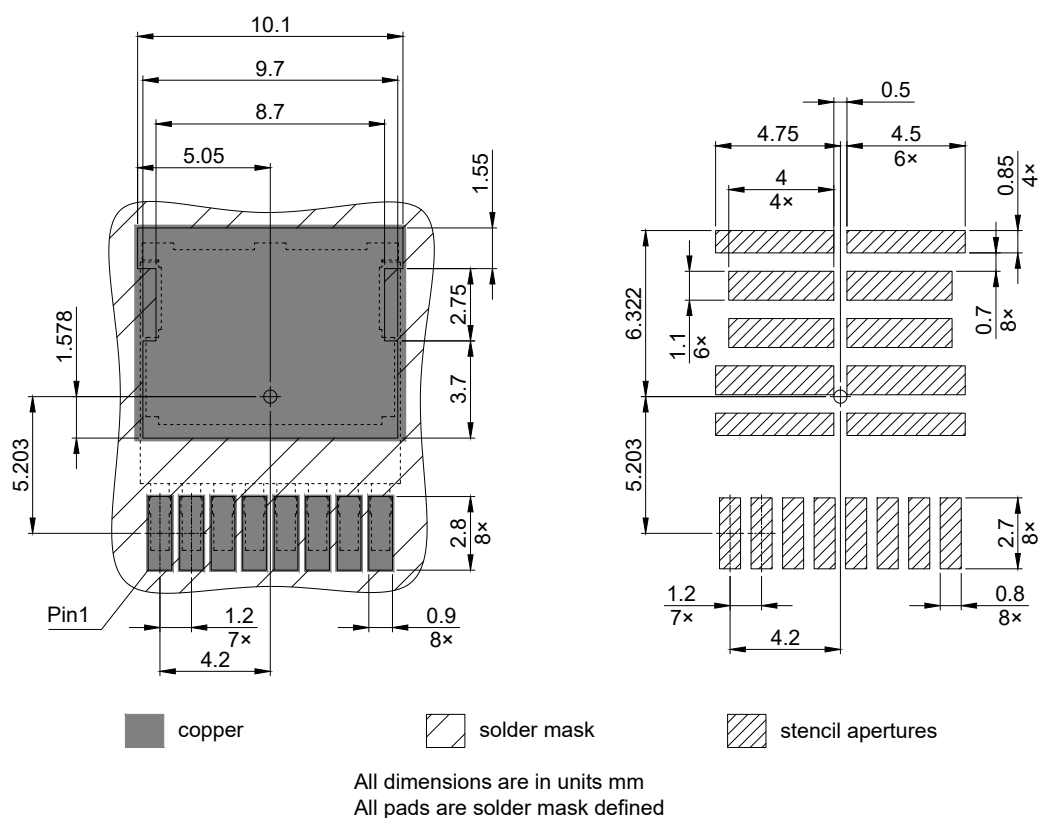
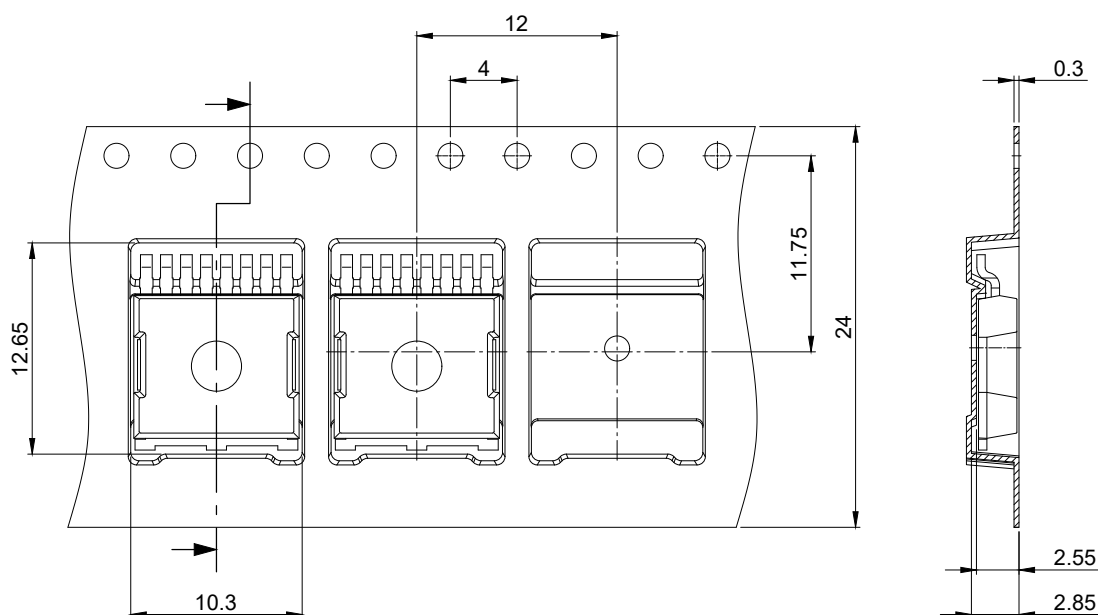


Figure 2 Outline PG-HSOG-8, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Outline PG-HSOG-8, dimensions in mm

Revision History

IPTG039N15NM5

Revision 2024-06-11, Rev. 2.2

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2022-05-05 | Release of final version |
| 2.1 | 2023-03-13 | Update Coss max |
| 2.2 | 2024-06-11 | Update Rg |

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