THE DATASHEET OF

NCP164AMT180TAG

LDO Regulator, 300 mA, Low Dropout Voltage, Ultra Low Noise, High PSRR with Power Good

NCP164

The NCP164 is a 300 mA LDO, next generation of high PSRR, ultra−low noise and low dropout regulators with Power Good open collector output. Designed to meet the requirements of RF and sensitive analog circuits, the NCP164 device provides ultra−low noise, high PSRR and low quiescent current. The device also offer excellent load/line transients. The NCP164 is designed to work with a 1 µF input and a 1 µF output ceramic capacitor. It is available in industry standard TSOP−5 and WDFN6 0.65P, 2 mm x 2 mm.

Features

- Operating Input Voltage Range: 1.6 V to 5.5 V
- Available in Fixed Voltage Option: 1.2 V to 5 V
- Adjustable Version Reference Voltage: 1.1 V
- ±2% Accuracy Over Load and Temperature
- Ultra Low Quiescent Current Typ. 30 µA
- Standby Current: Typ. 0.1 µA
- Very Low Dropout: 110 mV at 300 mA for 3.3 V Variant
- Ultra High PSRR: Typ. 85 dB at 10 mA, f = 1 kHz
- Ultra Low Noise: 9 μV_{RMS} (Fixed Version)
- Stable with a 1 µF Small Case Size Ceramic Capacitors
- Available in – TSOP−5 3 mm x 1.5 mm x 1 mm CASE 483
    - WDFN6 2 mm x 2 mm x 0.75 mm CASE 511BR
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Communication Systems
- In−Vehicle Networking
- Telematics, Infotainment and Clusters
- General Purpose Automotive

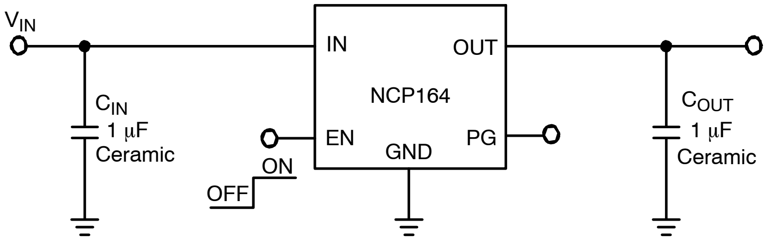

Figure 1. Typical Application Schematic

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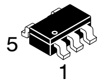
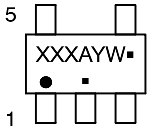
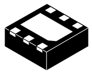
MARKING DIAGRAMS

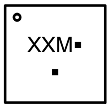


TSOP−5
CASE 483



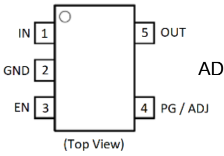


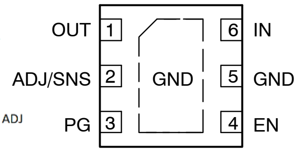
WDFN6 2x2, 0.65P
CASE 511BR



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
M = Month Code
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTONS





WDFN6 2x2 mm
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

Table 1. PIN FUNCTION DESCRIPTION

Pin No. TSOP−5	Pin No. WDFN6	Pin Name	Description
1	6	IN	Input voltage supply pin
5	1	OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor
3	4	EN	Chip enable: Applying V_{EN} < 0.2 V disables the regulator, Pulling V_{EN} > 0.7 V enables the LDO
4 / −	3	PG	Power Good, open collector. Use 10 kΩ to 100 kΩ pull−up resistor connected to output or input voltage
2	5	GND	Common ground connection
− / 4	2	ADJ	Adjustable output feedback pin (for adjustable version only)
−	2	SNS	Sense feedback pin. Must be connected to OUT pin on PCB (for fixed versions only)
−	−	N/C	Not connected, pin can be tied to ground plane for better power dissipation
−	EPAD	EPAD	Expose pad should be tied to ground plane for better power dissipation

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN}+0.3, max. 6	V
Chip Enable Input	V_{CE}	−0.3 to 6	V
Power Good Voltage	V_{PG}	−0.3 to 6	V
Power Good Current	I_{PG}	30	mA
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per EIA/JESD22−C101, Field Induced Charge Model

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
THERMAL CHARACTERISTICS, TSOP−5 PACKAGE			
Thermal Resistance, Junction−to−Ambient (Note 3)	$R_{\theta JA}$	158	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	155	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	102	°C/W
Thermal Resistance, Junction−to−Board	$R_{\theta JB}$	197	°C/W
Characterization Parameter, Junction−to−Top	Ψ_{JT}	40	°C/W
Characterization Parameter, Junction−to−Board	Ψ_{JB}	82	°C/W
THERMAL CHARACTERISTICS, WDFN6−2X2, 0.65 PITCH PACKAGE			
Thermal Resistance, Junction−to−Ambient (Note 3)	$R_{\theta JA}$	51	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	142	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	2.0	°C/W
Thermal Resistance, Junction−to−Board	$R_{\theta JB}$	117	°C/W
Characterization Parameter, Junction−to−Top	Ψ_{JT}	1.9	°C/W
Characterization Parameter, Junction−to−Board	Ψ_{JB}	7.7	°C/W

3. The junction−to−ambient thermal resistance under natural convection is obtained in a simulation on a high−K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51−2a.
4. The junction−to−case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30−88.

Table 4. ELECTRICAL CHARACTERISTICS (−40°C ≤ T_J ≤ 150°C; $V_{IN} = V_{OUT(NOM)} + 0.5$ V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1 μF, $V_{EN} = V_{IN}$, unless otherwise noted. Typical values are at T_J = +25°C (Note 5))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.6		5.5	V
Output Voltage Accuracy	$V_{IN} = V_{OUT(NOM)} + 0.5$ V to 5.0 V, 0.1 mA ≤ I_{OUT} ≤ 300 mA		V_{OUT}	−2		+2	%
Reference Voltage (Adjustable Ver. ADJ pin connected to OUT)	V_{IN} = 1.6 V to 5.0 V, 0.1 mA ≤ I_{OUT} ≤ 300 mA		V_{ADJ}	1.078	1.1	1.122	V
Line Regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.0 V		$Line_{Reg}$		0.5		mV/V
Load Regulation	I_{OUT} = 1 mA to 300 mA		$Load_{Reg}$		2		mV
Dropout Voltage (Note 6) TSOP−5, WDFN6	I_{OUT} = 300 mA	$V_{OUT(NOM)}$ = 1.5 V	V_{DO}		170	295	mV
		$V_{OUT(NOM)}$ = 1.8 V			155	255	
		$V_{OUT(NOM)}$ = 2.5 V			125	200	
		$V_{OUT(NOM)}$ = 2.8 V			115	185	
		$V_{OUT(NOM)}$ = 3.0 V			113	177	
		$V_{OUT(NOM)}$ = 3.3 V			110	170	
		$V_{OUT(NOM)}$ = 4.5 V			95	135	
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	350	560		mA
Short Circuit Current	V_{OUT} = 0 V		I_{SC}		580		
Quiescent Current	I_{OUT} = 0 mA		I_Q		30	40	μA
Shutdown Current	V_{EN} ≤ 0.4 V		I_{DIS}		0.01	1.5	μA
EN Pin Threshold Voltage	EN Input Voltage "H"		V_{ENH}	0.7			V
	EN Input Voltage "L"		V_{ENL}			0.2	
EN Pull Down Current	V_{EN} = 5.0 V		I_{EN}		0.2	0.6	μA
Power Good Threshold Voltage	Output Voltage Raising		V_{PGUP}		95		%
	Output Voltage Falling		V_{PGDW}		90		
Power Good Output Voltage Low	I_{PG} = 5 mA, Open drain		V_{PGLO}			0.3	V
Turn−On Time (Note 7)	C_{OUT} = 1 μF, From assertion of V_{EN} to V_{OUT} = 95% $V_{OUT(NOM)}$				120		μs
Power Supply Rejection Ratio (Note 7)	$V_{OUT(NOM)}$ = 3.3 V, I_{OUT} = 10 mA	f = 100 Hz	P_{SRR}		83		dB
		f = 1 kHz			85		
		f = 10 kHz			80		
		f = 100 kHz			61		
Output Voltage Noise (Fixed Ver.)	f = 10 Hz to 100 kHz	I_{OUT} = 10 mA	V_N		9		μV_{RMS}
Thermal Shutdown Threshold (Note 7)	Temperature rising		T_{SDH}		165		°C
	Temperature hysteresis		T_{HYST}		15		°C
Active output discharge resistance	V_{EN} < 0.2 V, Version A only		R_{DIS}		260		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A$ = 25°C.
6. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
7. Guaranteed by design and characterization.

TYPICAL CHARACTERISTICS

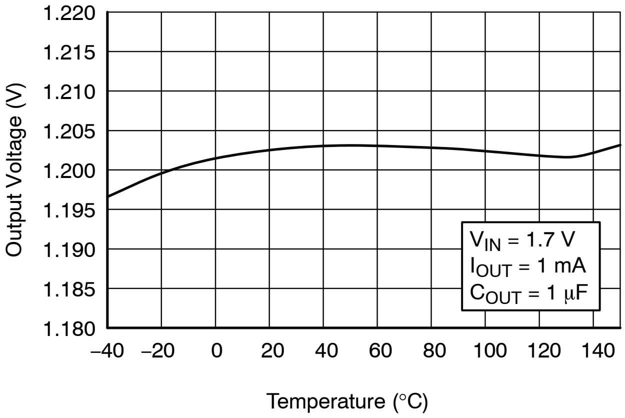


Figure 2. Output Voltage vs. Temperature – V_{OUT} = 1.2 V

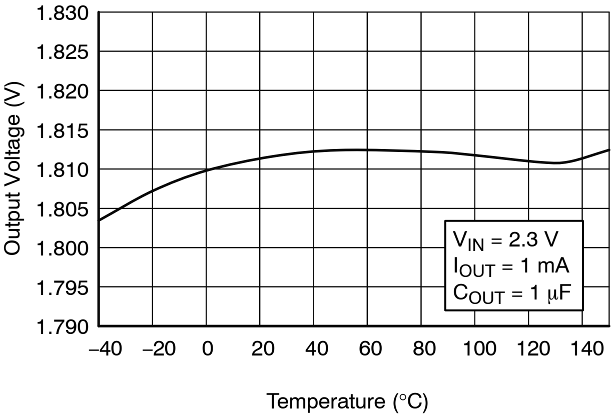


Figure 3. Output Voltage vs. Temperature – V_{OUT} = 1.8 V

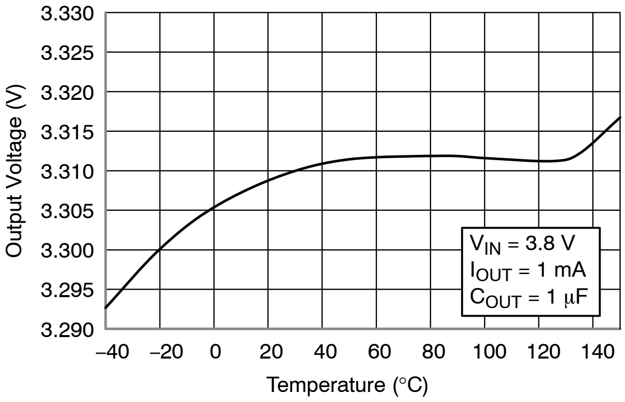


Figure 4. Output Voltage vs. Temperature – V_{OUT} = 3.3 V

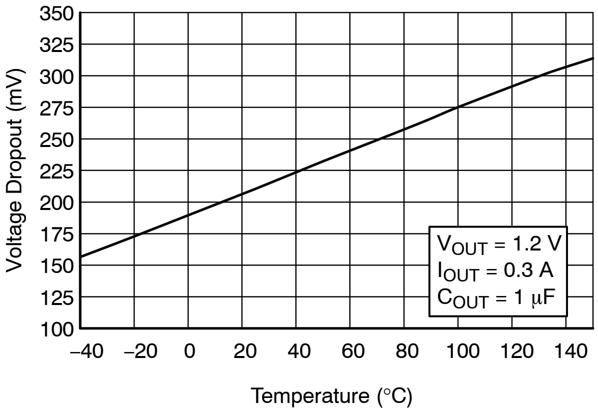


Figure 5. Dropout Voltage vs. Temperature – V_{OUT} = 1.2 V

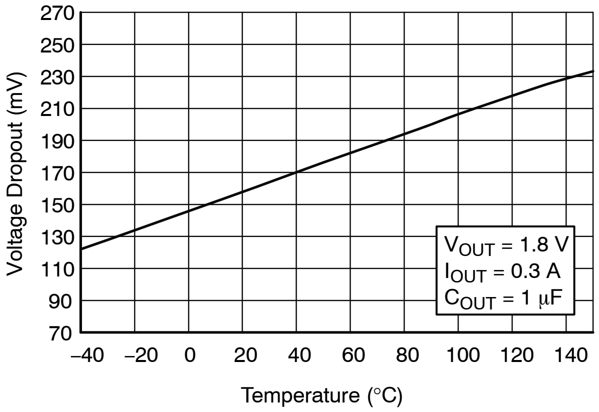


Figure 6. Dropout Voltage vs. Temperature – V_{OUT} = 1.8 V

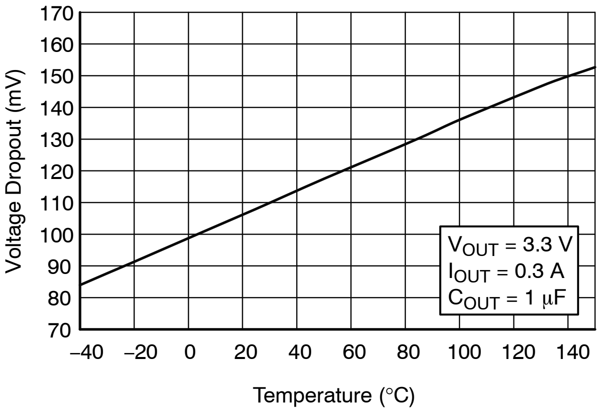


Figure 7. Dropout Voltage vs. Temperature – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS (continued)

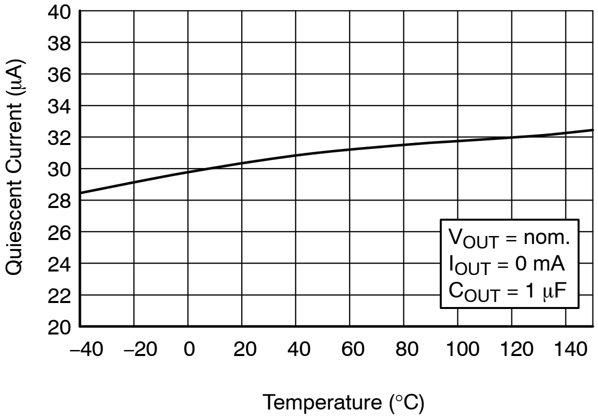


Figure 8. Quiescent Current va Temperature

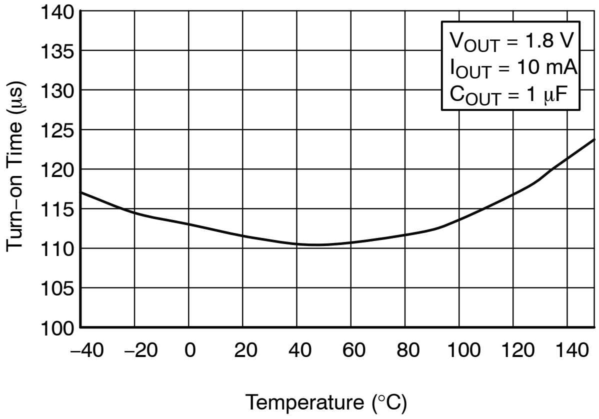


Figure 9. Turn−on Time vs. Temperature

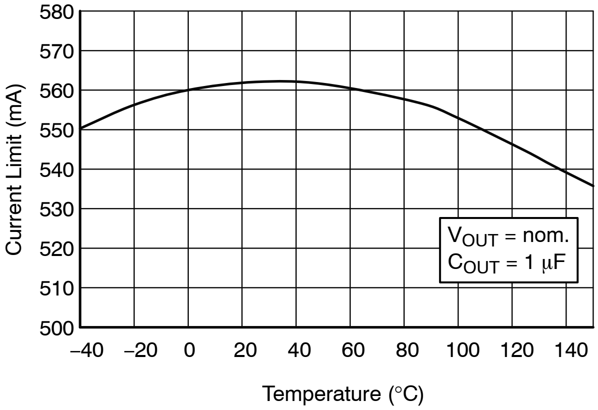


Figure 10. Current Limit vs. Temperature

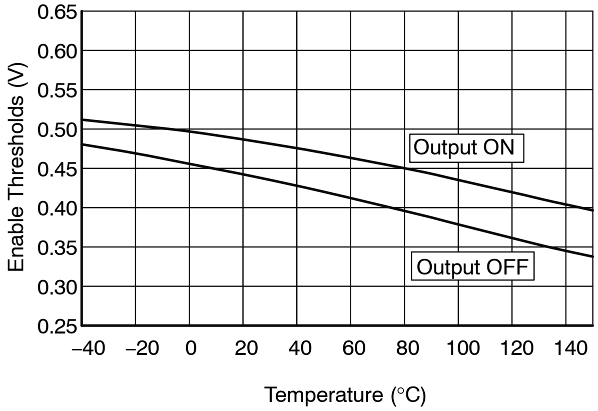


Figure 11. Enable Thresholds vs Temperature

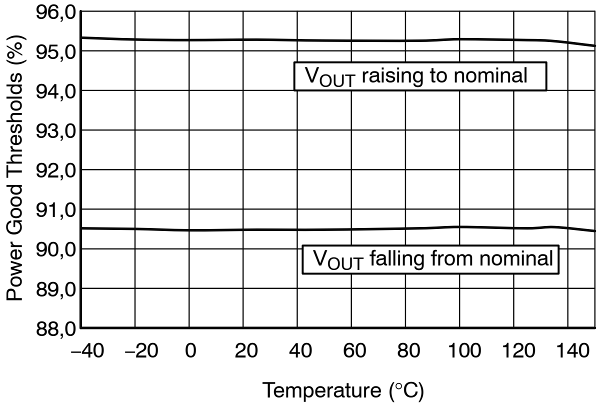


Figure 12. Power Good Threshold vs. Temperature

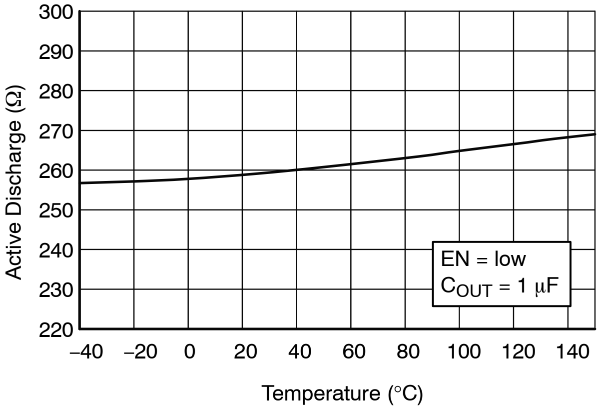


Figure 13. Active Discharge Resistance vs. Temperature

TYPICAL CHARACTERISTICS (continued)

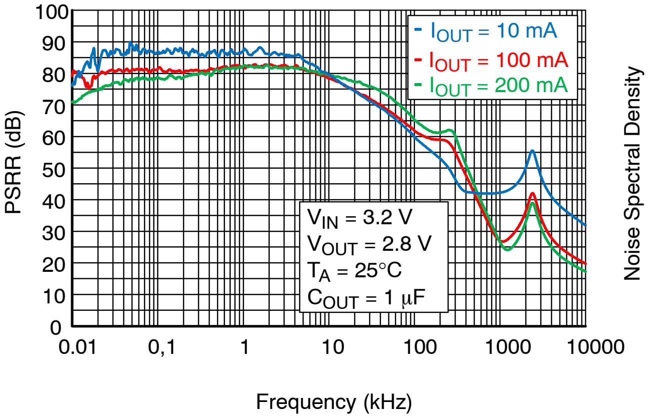


Figure 14. Power Supply Rejection Ration for V_{OUT} = 2.8 V, C_{OUT} = 1 μF

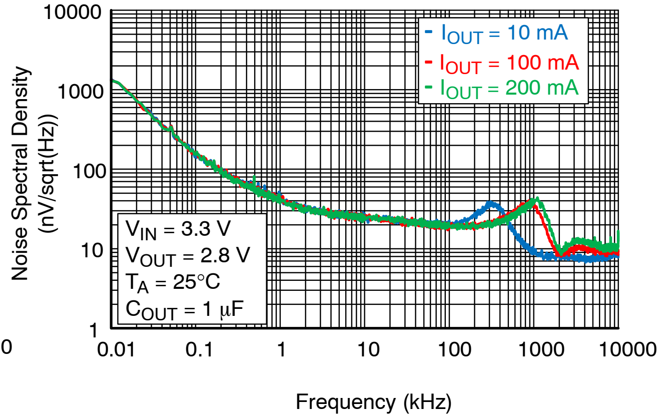


Figure 15. Output Voltage Noise Spectral Density for V_{OUT} = 2.8 V, C_{OUT} = 1 μF

APPLICATIONS INFORMATION

The NCP164 is the member of new family of high output current and low dropout regulators which delivers low quiescent and ground current consumption, good noise and power supply ripple rejection ratio performance. The NCP164 incorporates EN pin and power good output for simple controlling by MCU or logic. Standard features include current limiting, soft–start feature and thermal protection.

Input Decoupling (C_{IN})

It is recommended to connect at least 1 μF ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or noise superimposed onto constant input voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes. Higher capacitance and lower ESR capacitors will improve the overall line transient response.

Output Decoupling (C_{OUT})

The NCP164 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of 1 μF or greater. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended.

Power Good Output Connection

The NCP164 include Power Good functionality for better interfacing to MCU system. Power Good output is open collector type, capable to sink up to 10 mA. Recommended operating current is between 10 μA and 1 mA to obtain low saturation voltage. External pull–up resistor can be connected to any voltage up to 5.0 V (please see Absolute Maximum Ratings table).

Power Dissipation and Heat Sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C, however device is capable to work up to junction temperature +150°C. The maximum power dissipation the NCP164 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

The power dissipated by the NCP164 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND}(I_{OUT})) + I_{OUT}\,(V_{IN} - V_{OUT}) \qquad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{OUT} \times I_{OUT}\right)}{I_{OUT} + I_{GND}} \qquad \text{(eq. 3)}$$

Hints

VIN and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCP164, and make traces as short as possible.

Adjustable Version

Not only adjustable version, but also any fixed version can be used to create adjustable voltage, where original fixed voltage becomes reference voltage for resistor divider and feedback loop. Output voltage can be equal or higher than original fixed option, while possible range is from 1.1 V up to 5 V. Figure 16 shows how to add external resistors to increase output voltage above fixed value.

Output voltage is then given by equation

$$V_{OUT} = V_{FIX} \times (1 + R1/R2) \qquad \text{(eq. 4)}$$

where V_{FIX} is voltage of original fixed version (from 1.2 V up to 5 V) or adjustable version (1.1 V). Do not operate the device at output voltage about 5.2 V, as device can be damaged.

In order to avoid influence of current flowing into SNS pin to output voltage accuracy (SNS current varies with voltage option and temperature, typical value is 300 nA) it is recommended to use values of R1 and R2 below 500 kΩ.

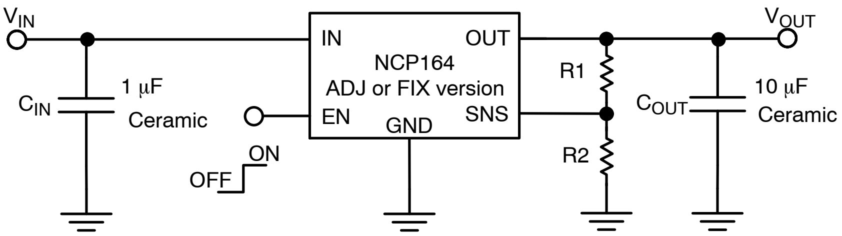


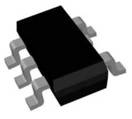
Figure 16. Adjustable Variant Application

Please note that output noise is amplified by V_{OUT} / V_{FIX} ratio. For example, if original 1.2 V fixed variant is used to create 3.6 V output voltage, output noise is increased 3.6 / 1.2 = 3 times and real value will be 3 × 9 µVrms = 27 µVrms. For noise sensitive applications it is recommended to use as high fixed variant as possible – for example in case above it is better to use 3.3 V fixed variant to create 3.6 V output voltage, as output noise will be amplified only 3.6 / 3.3 = 1.09 × (9.8 µVrms).

ORDERING INFORMATION

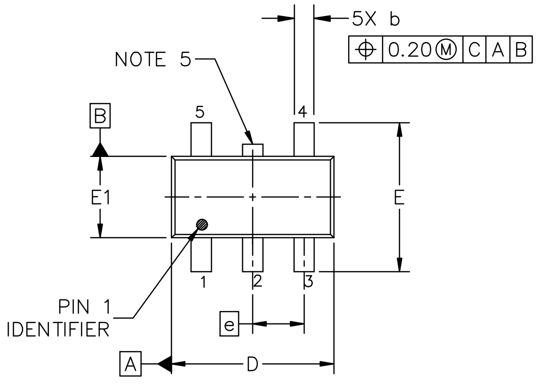
Device Part No.	Voltage Variant	Marking	Package Option	Package	Shipping †
NCP164ASN180T1G	1.8 V	AJ	N/A	TSOP5 (Pb−Free)	3000 / Tape & Reel
NCP164ASN280T1G	2.8 V	AK	N/A	TSOP5 (Pb−Free)	3000 / Tape & Reel
NCP164ASN330T1G	3.3 V	AL	N/A	TSOP5 (Pb−Free)	3000 / Tape & Reel
NCP164ASNADJT1G	ADJ	A6	N/A	TSOP5 (Pb−Free)	3000 / Tape & Reel
NCP164AMT120TAG	1.2 V	CA	Non−Wettable	WDFN6 2 x 2 (Pb−Free)	3000 / Tape & Reel
NCP164AMT180TAG	1.8 V	CJ	Non−Wettable	WDFN6 2 x 2 (Pb−Free)	3000 / Tape & Reel
NCP164AMT280TAG	2.8 V	CK	Non−Wettable	WDFN6 2 x 2 (Pb−Free)	3000 / Tape & Reel
NCP164AMT330TAG	3.3 V	CL	Non−Wettable	WDFN6 2 x 2 (Pb−Free)	3000 / Tape & Reel
NCP164AMTADJTAG	ADJ	C2	Non−Wettable	WDFN6 2 x 2 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

DATE 01 APR 2024

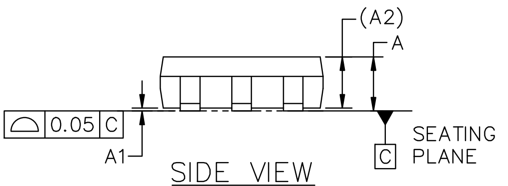


TOP VIEW

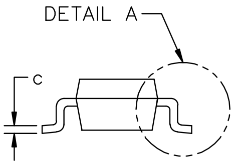
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

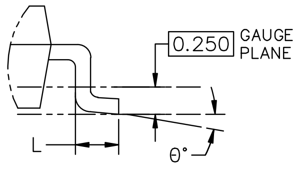
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°



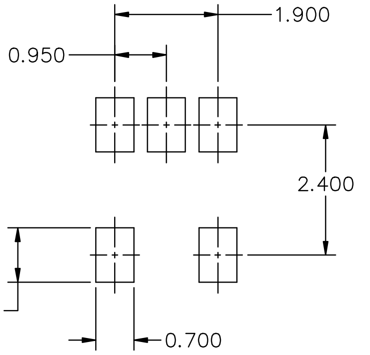
SIDE VIEW



END VIEW



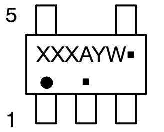
DETAIL "A"
SCALE 2:1



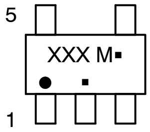
RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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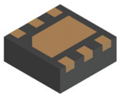
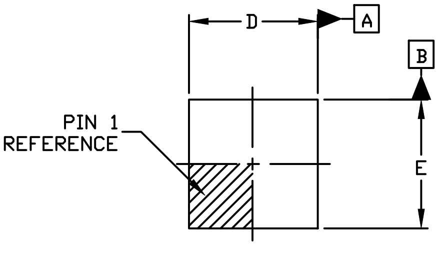
DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



WDFN6 2x2, 0.65P
CASE 511BR
ISSUE C

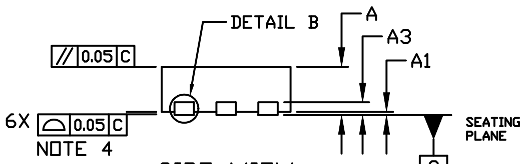
DATE 01 DEC 2021



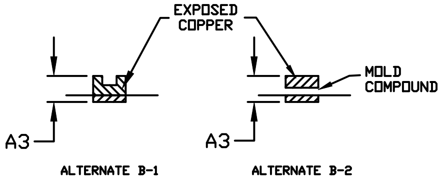
TOP VIEW

NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e	0.65 BSC		
K	0.20 REF		
L	0.20	0.30	0.40
L1	---	---	0.15

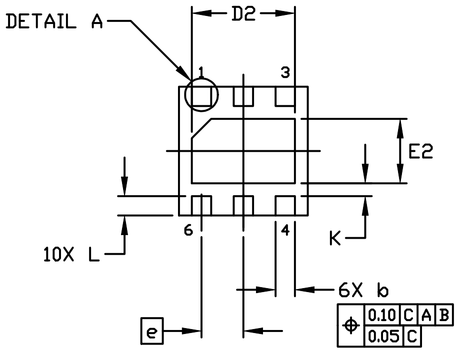


SIDE VIEW

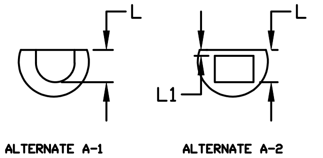


DETAIL B

ALTERNATE CONSTRUCTION

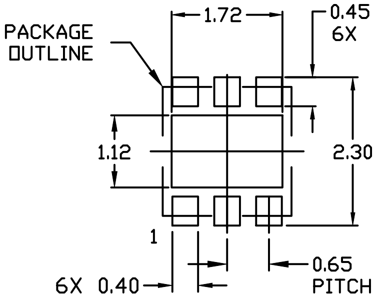


BOTTOM VIEW



DETAIL A

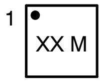
ALTERNATE CONSTRUCTIONS



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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