THE DATASHEET OF

LT3689IMSE-5#TRPBF

700mA Step-Down Regulator with Power-On Reset and Watchdog Timer

FEATURES

- **Wide Input Range:**
  Operation from 3.6V to 36V
  Overvoltage Lockout Protects Circuits through 60V Transients
- **85µA I_Q at 12V_{IN} to 3.3V_{OUT}**
- **Low Ripple Burst Mode® Operation Allows Output Ripple <15mV_{P-P}**
- **Programmable, Defeatable Watchdog Timer with Window or Timeout Control**
- **Programmable Power-On Reset Timer (POR)**
- **Synchronizable, Adjustable 350kHz to 2.2MHz Switching Frequency**
- 700mA Output Switching Regulator with Internal Power Switch
- Fixed 5V or Adjustable Output Voltage
- 800mV Feedback Voltage
- Programmable Input Undervoltage Lockout with Hysteresis
- 16-Pin 3mm × 3mm QFN and 16-Pin MSOP Packages

APPLICATIONS

- Automotive Electronic Control Units
- Industrial Power Supplies

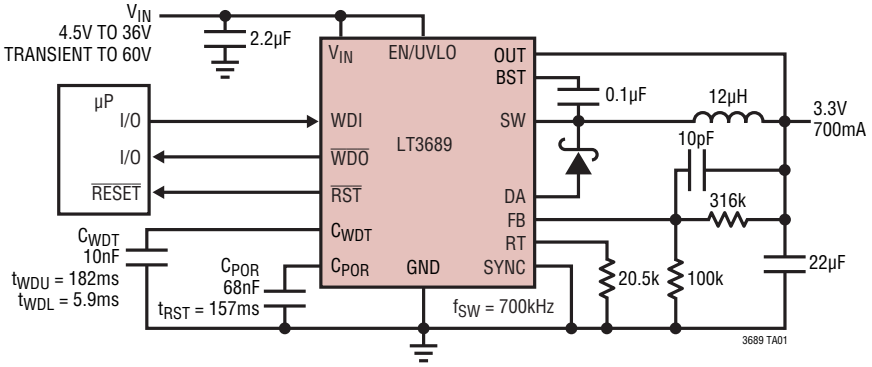
DESCRIPTION

The LT®3689 is an adjustable frequency (350kHz to 2.2MHz) monolithic step-down switching regulator with a power-on reset and watchdog timer. The regulator operates from inputs up to 36V and withstands transients up to 60V. Low ripple Burst Mode® operation maintains high efficiency at low output current while keeping output ripple below 15mV in a typical application, with input quiescent current of just 85µA. Shutdown circuitry reduces input supply current to less than 1µA while EN/UVLO is pulled low. Using a resistor divider on the EN/UVLO pin provides a programmable undervoltage lockout. Current limit, frequency foldback and thermal shutdown provide fault protection.

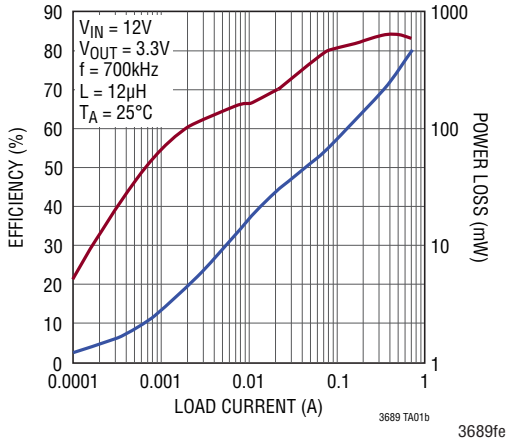
The reset and watchdog timeout periods are independently adjustable using external capacitors. Tight accuracy specifications and glitch immunity ensure reliable reset operation of a system without false triggering. The open collector $\overline{RST}$ will pull down if output voltage drops 10% below the programmed value. The watchdog timer is pin-selectable for window or timeout modes. In timeout mode, $\overline{WDO}$ pulls low if too long of a period passes before a watchdog transition is detected. In window mode, the LT3689 monitors for WDI falling edges grouped too close together or too far apart.

TYPICAL APPLICATION

3.3V Regulator with Power-On Reset Timer and Watchdog Timer



Efficiency

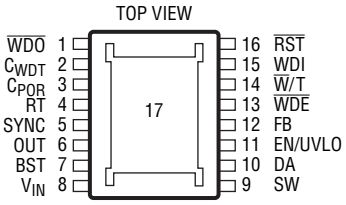


ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, EN/UVLO Voltage (Note 2) 60V
BST Voltage 60V
BST Above SW Voltage 30V
OUT, $\overline{WDE}$ Voltage 30V
FB, RT, SYNC, $\overline{W}$/T, WDI, $\overline{RST}$, $\overline{WDO}$ Voltage 6V
C_{WDT}, C_{POR} Voltage 3V

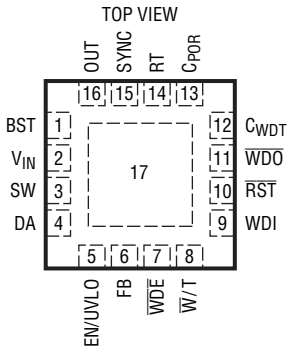
Operating Junction Temperature Range (Note 3)
LT3689E ..... –40°C to 125°C
LT3689I ..... –40°C to 125°C
LT3689H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP

θ_{JA} = 43°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3689EMSE#PBF	LT3689EMSE#TRPBF	3689	16-Lead Plastic MSOP with Exposed Pad	–40°C to 125°C
LT3689IMSE#PBF	LT3689IMSE#TRPBF	3689	16-Lead Plastic MSOP with Exposed Pad	–40°C to 125°C
LT3689HMSE#PBF	LT3689HMSE#TRPBF	3689	16-Lead Plastic MSOP with Exposed Pad	–40°C to 150°C
LT3689EMSE-5#PBF	LT3689EMSE-5#TRPBF	36895	16-Lead Plastic MSOP with Exposed Pad	–40°C to 125°C
LT3689IMSE-5#PBF	LT3689IMSE-5#TRPBF	36895	16-Lead Plastic MSOP with Exposed Pad	–40°C to 125°C
LT3689HMSE-5#PBF	LT3689HMSE-5#TRPBF	36895	16-Lead Plastic MSOP with Exposed Pad	–40°C to 150°C
LT3689EUD#PBF	LT3689EUD#TRPBF	LDND	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3689IUD#PBF	LT3689IUD#TRPBF	LDND	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3689EUD-5#PBF	LT3689EUD-5#TRPBF	LFFM	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3689IUD-5#PBF	LT3689IUD-5#TRPBF	LFFM	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{OUT} = 5V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{IN} Fixed Undervoltage Lockout		●		3.4	3.7	V
	V_{IN} Overvoltage Lockout		●	36	38	40	V
	Quiescent Current from V_{IN}	$V_{EN/UVLO}$ = 0.3V V_{OUT} = 3V, Not Switching V_{OUT} = 0V, Not Switching	 ● 		0.01 50 125	0.5 95 175	µA µA µA
	Quiescent Current from OUT	$V_{EN/UVLO}$ = 0.3V V_{OUT} = 3V, Not Switching (Note 7) V_{OUT} = 0V, Not Switching	 ● 		0.01 75 –5	0.5 150 –20	µA µA µA
	LT3689-5 Quiescent Current from V_{IN}	$V_{EN/UVLO}$ = 0.3V V_{OUT} = 5.5V (Note 8) V_{OUT} = 0V	 ● 		0.01 50 125	0.5 95 175	µA µA µA
	LT3689-5 Quiescent Current from OUT	$V_{EN/UVLO}$ = 0.3V V_{OUT} = 5.5V	 ●		8 95	16 150	µA µA
	LT3689 FB Voltage		 ●	0.790 0.780	0.800	0.812 0.812	V V
	LT3689-5 Output Voltage		 ●	4.950 4.900	5.000	5.050 5.100	V V
	LT3689 FB Pin Bias Current	V_{FB} = 0.800V	●		–30	–100	nA
	LT3689 FB Voltage Line Regulation	5V < V_{IN} < 36V			0.005		%/V
	LT3689-5 Output Voltage Line Regulation	5.5V < V_{IN} < 36V			0.005		%/V
f_{SW}	Switching Frequency	R_T = 4.02k R_T = 31.62k	● ●	1.8 420	2 500	2.2 540	MHz kHz
$t_{SW(OFF)}$	Switch Off-Time				120	160	ns
	Foldback Frequency	R_T = 4.02k, V_{FB} = 0V			250		kHz
	Switch Current Limit (Note 4)		●	1.15	1.55	1.95	A
	Switch V_{CESAT}	I_{SW} = 0.8A			450		mV
	Switch Leakage Current				0.01	1	µA
	DA Current Limit			0.85	1.2	1.5	A
	Boost Schottky Reverse Leakage	V_{BST} = 12V, V_{OUT} = 0V			0.1	5	µA
	Minimum BST Above SW Voltage				1.8	2.5	V
	BST Pin Current	I_{SW} = 0.8A			15	25	mA
	EN/UVLO Threshold Voltage			1.150	1.260	1.350	V
	EN/UVLO Pin Current	$V_{EN/UVLO}$ = 1.35V $V_{EN/UVLO}$ = 1.15V	 	 2.5	0. 01 4.1	1 5.5	µA µA
	EN/UVLO Pin Current Hysteresis	$I(V_{EN/UVLO}$ = 1.15V) – $I(V_{EN/UVLO}$ = 1.35V)		2.8	3.8	4.8	µA
	SYNC Threshold Voltage			0.4	0.8	1	V
V_{RST}	Reset Threshold as % of V_{FB}		●	88	90	92	%
t_{RST}	Reset Timeout Period	C_{POR} = 8200pF	●	17	19	21	ms
t_{WDU}	Watchdog Upper Boundary	C_{WDT} = 1000pF	●	17	19	21	ms
t_{WDL}	Watchdog Lower Boundary	C_{WDT} = 1000pF	●	610	675	785	µs
V_{OL}	$\overline{RST}$, $\overline{WDO}$ Output Voltage Low	I_{SINK} = 2.5mA I_{SINK} = 100µA	● ●		0.15 0.05	0.4 0.3	V V
V_{OH}	$\overline{RST}$, $\overline{WDO}$ Output Voltage High (Note 6)		●	V_{OUT} –1			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{OUT} = 5V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{UV}	UV Detect to $\overline{RST}$ Asserted	Step V_{FB} from 0.9V to 0.5V	●	10	30	65	µs
	WDI Input Threshold		●	0.4	0.95	1.15	V
	WDI Input Pull-Up Current				–2		µA
	WDI Input Pulse Width		●	300			ns
	$\overline{W}$/T Threshold Voltage		●	0.4	0.8	1	V
	$\overline{W}$/T Input Pull-Down Current				2.6		µA
	$\overline{WDE}$ Threshold Voltage		●	0.4	0.8	1	V
	$\overline{WDO}$ Pull-Up Current (Note 6)			–0.6	–0.85		µA
	$\overline{RST}$ Pull-Up Current (Note 6)			–0.6	–0.85		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute maximum voltage at V_{IN} and EN/UVLO pins is 60V for nonrepetitive 1 second transients, and 36V for continuous operation.

Note 3: The LT3689E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3689I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3689H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: Current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

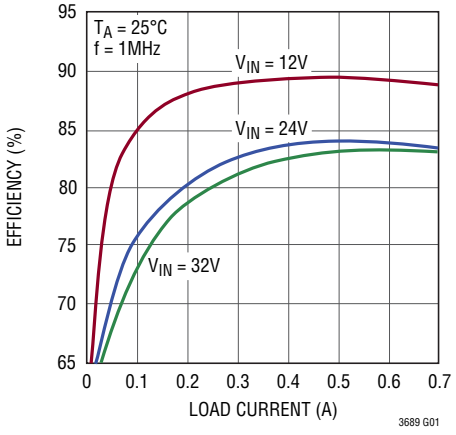
Note 6: The output of $\overline{RST}$ and $\overline{WDO}$ has a weak pull-up to V_{OUT} of typically 1µA. However, external pull-up resistors may be used when faster rise times are required or for V_{OH} higher than V_{OUT}.

Note 7: Polarity specification for all currents into pins is positive. All voltages are referenced to GND unless otherwise specified.

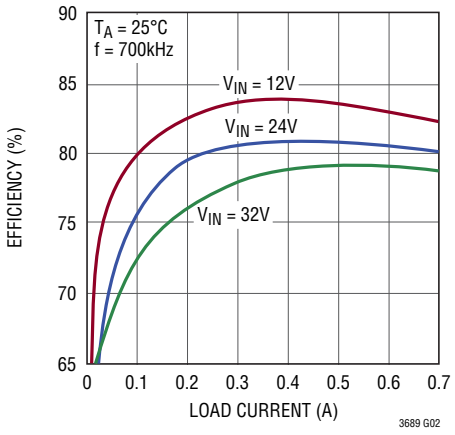
Note 8: For the LT3689-5, V_{OUT} is set to 5.5V to ensure the switching.

TYPICAL PERFORMANCE CHARACTERISTICS

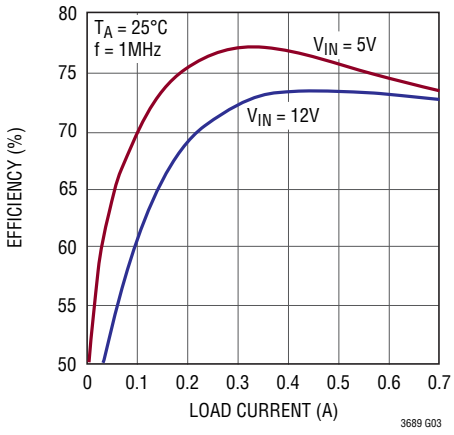
Efficiency, V_{OUT} = 5V



Efficiency, V_{OUT} = 3.3V

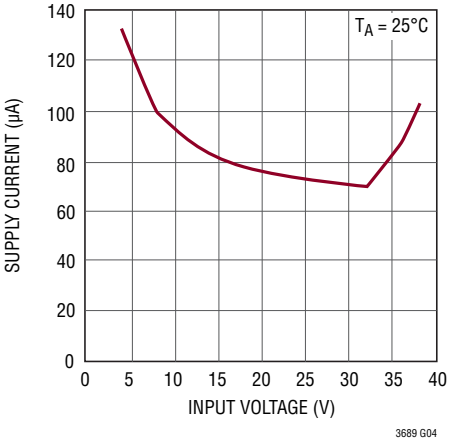


Efficiency, V_{OUT} = 1.8V

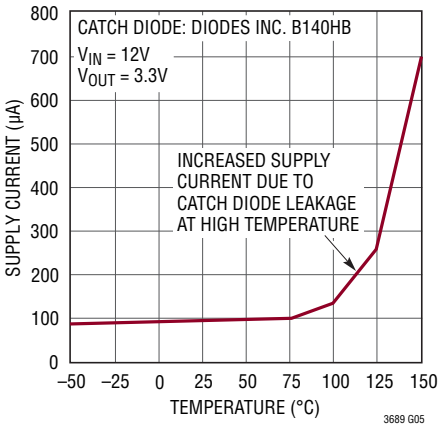


TYPICAL PERFORMANCE CHARACTERISTICS

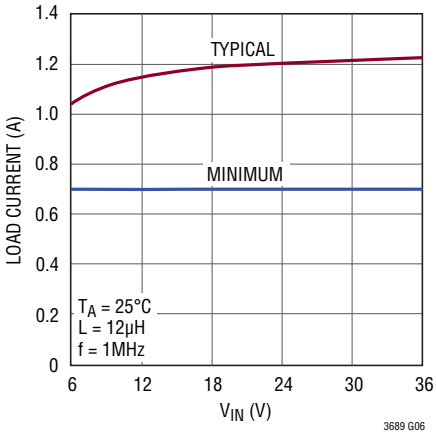
No-Load Supply Current vs V_{IN}



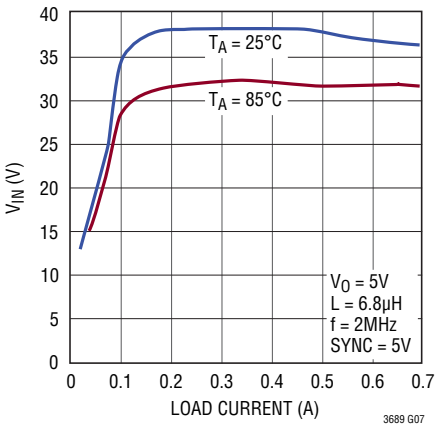
No-Load Supply Current



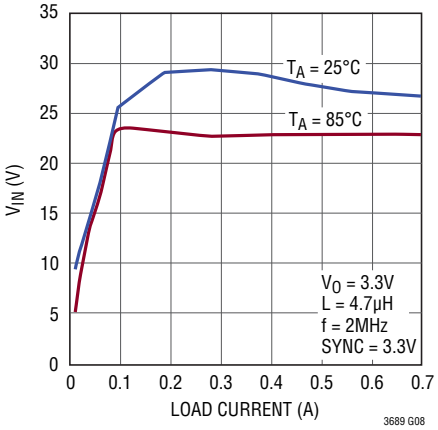
Maximum Load Current, $5V_{OUT}$



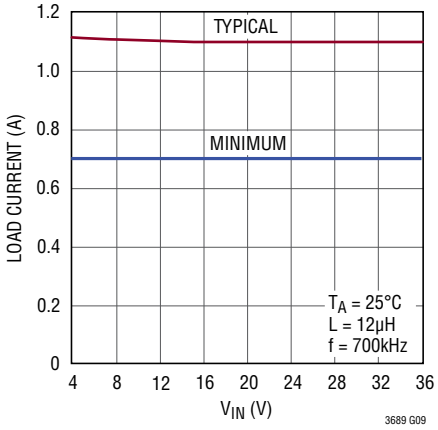
Maximum V_{IN} for Full Frequency



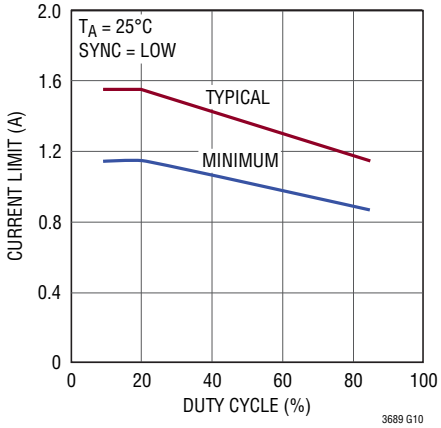
Maximum V_{IN} for Full Frequency



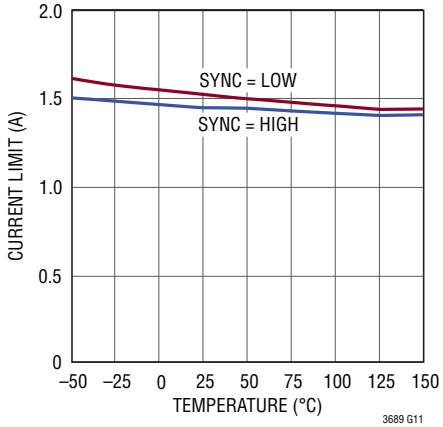
Maximum Output Current, $3.3V_{OUT}$



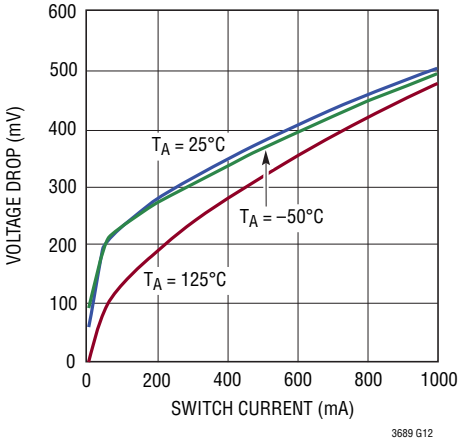
Switch Current Limit vs Duty Cycle



Switch Current Limit vs Temperature

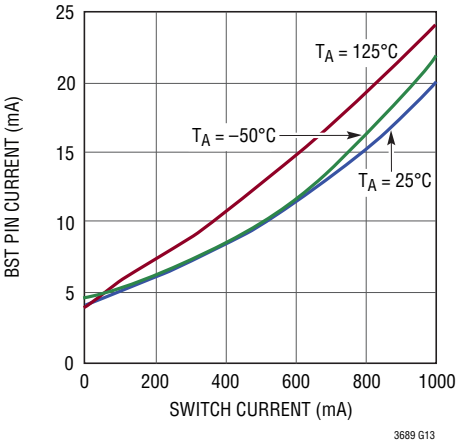


Switch Voltage Drop



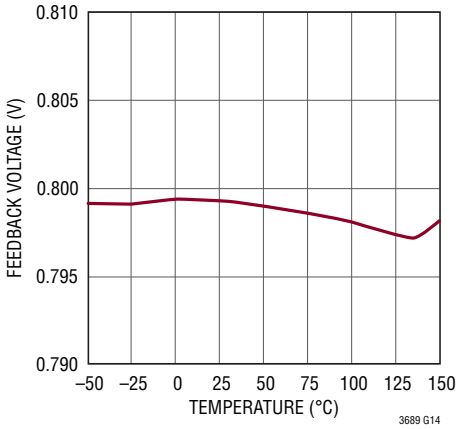
TYPICAL PERFORMANCE CHARACTERISTICS

BST Pin Current



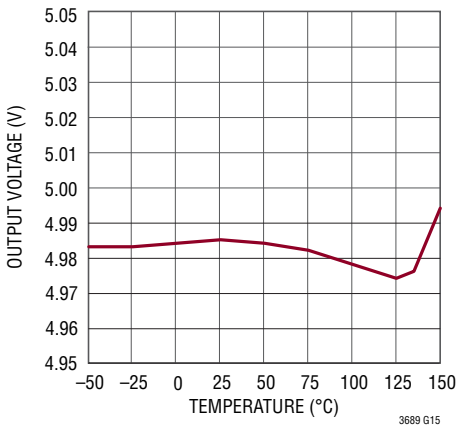
3689 G13

Feedback Voltage



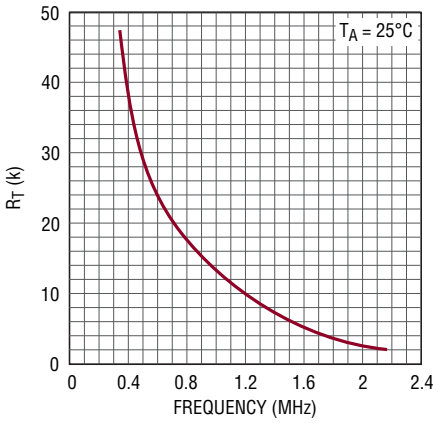
3689 G14

Output Voltage



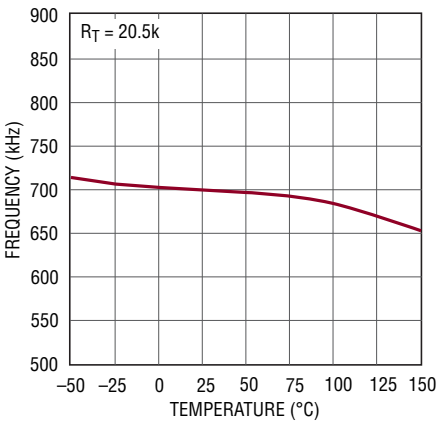
3689 G15

Switching Frequency vs R_T



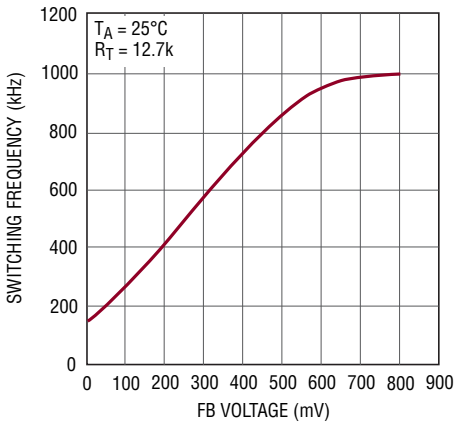
3689 G16

Switching Frequency



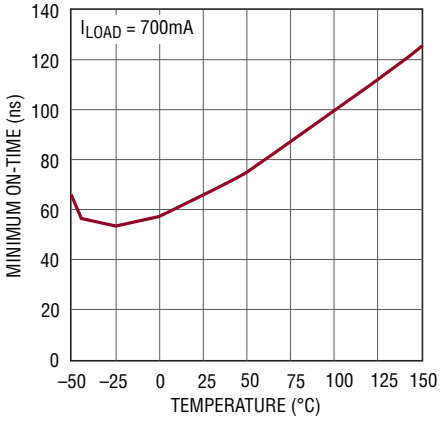
3689 G17

Frequency Foldback



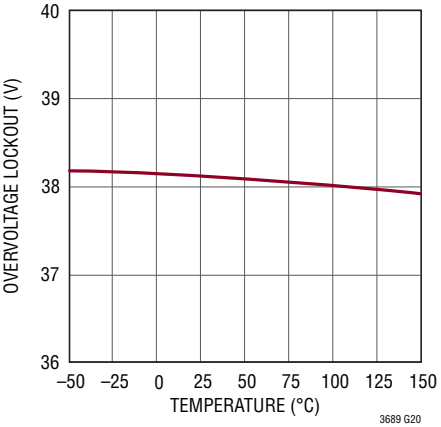
3689 G18

Minimum Switch On-Time



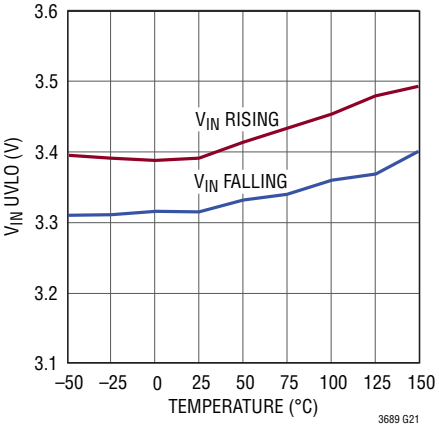
3689 G19

Overvoltage Lockout



3689 G20

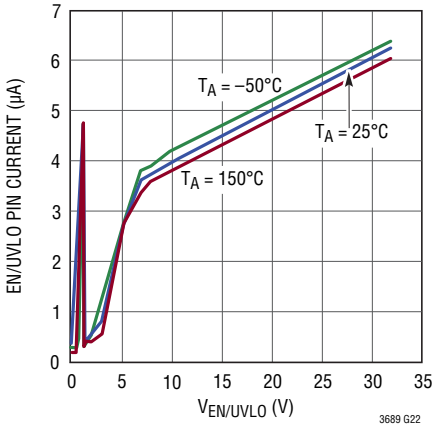
V_{IN} Fixed Undervoltage Lockout



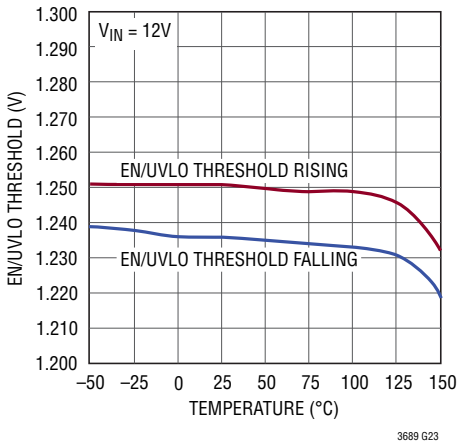
3689 G21

TYPICAL PERFORMANCE CHARACTERISTICS

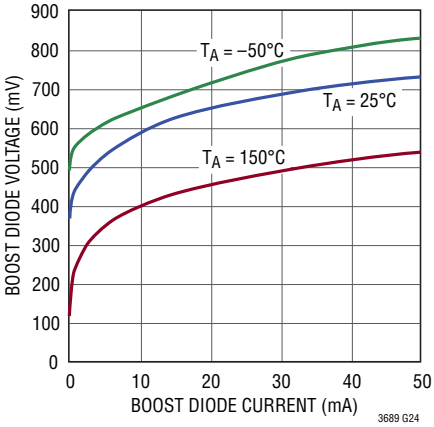
EN/UVLO Pin Current



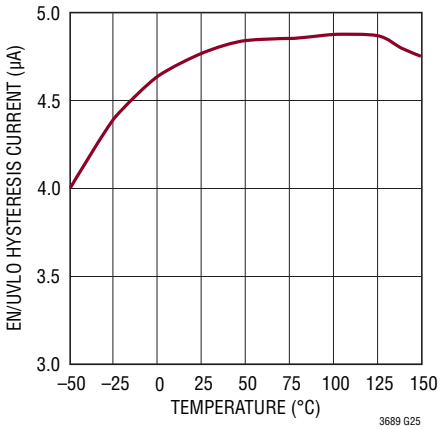
EN/UVLO Pin Threshold



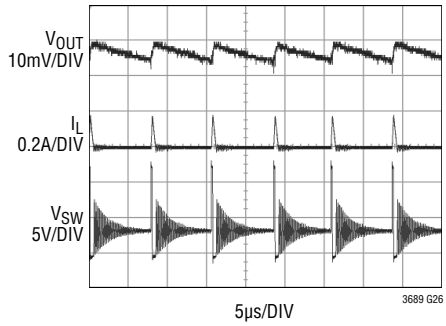
Boost Diode Forward Voltage



EN/UVLO Hysteresis Current



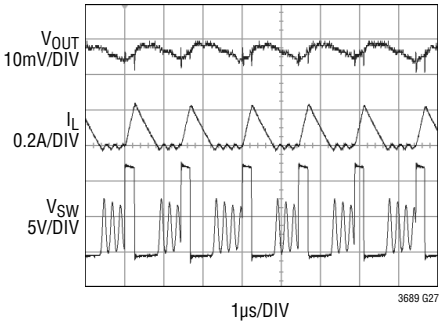
Switching Waveform: Burst Mode Operation



5µs/DIV

V_{IN} = 12V, FRONT PAGE APPLICATION
I_{LOAD} = 6mA

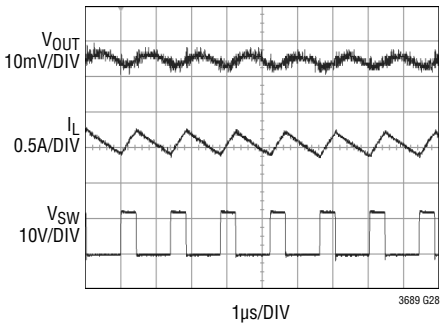
Switching Waveform: Transition from Burst Mode to Full Frequency



1µs/DIV

V_{IN} = 12V, FRONT PAGE APPLICATION
I_{LOAD} = 60mA

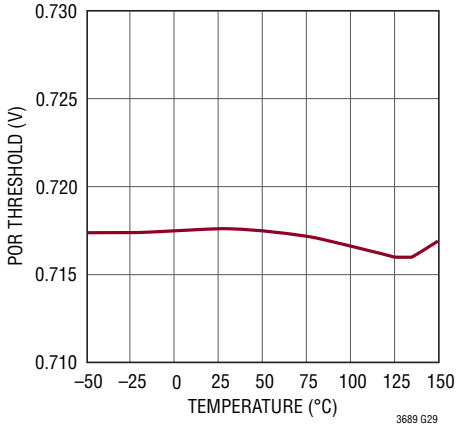
Switching Waveform: Full Frequency Continuous Operation



1µs/DIV

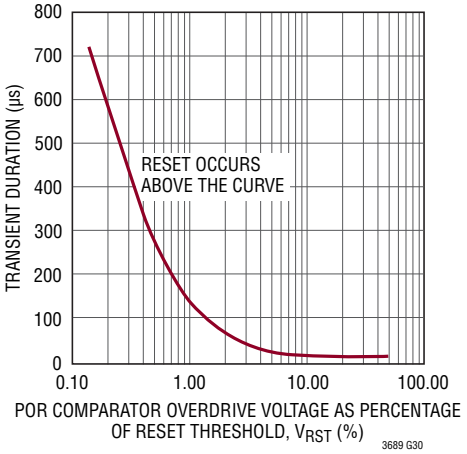
V_{IN} = 12V, FRONT PAGE APPLICATION
I_{LOAD} = 600mA

Power-On-Reset Threshold vs Temperature

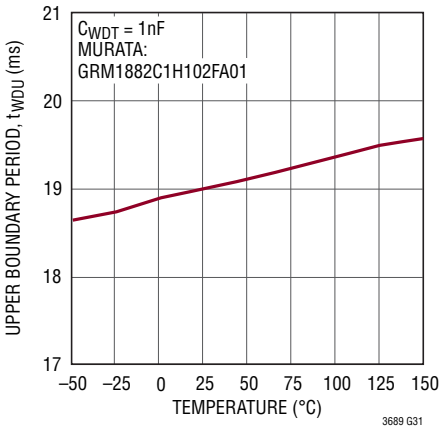


TYPICAL PERFORMANCE CHARACTERISTICS

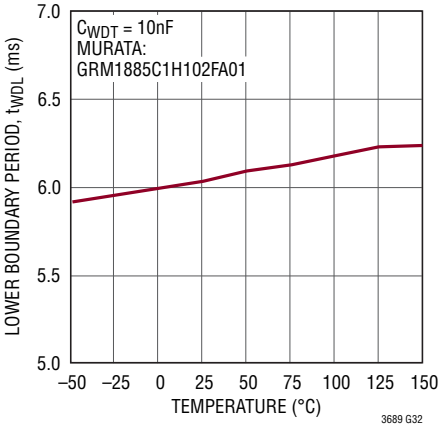
Transient Duration vs POR Comparator Overdrive



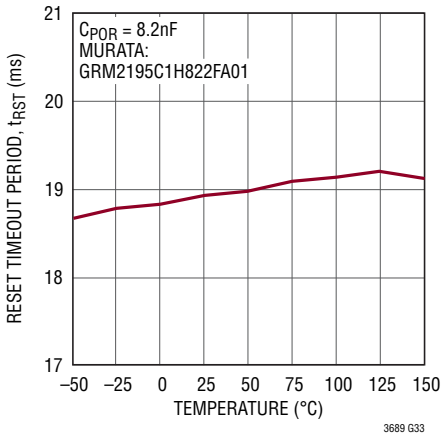
Watchdog Upper Boundary Period



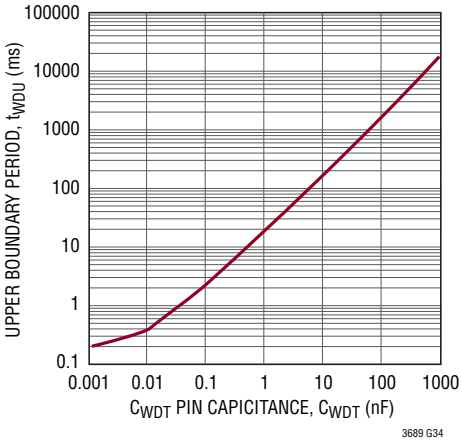
Watchdog Lower Boundary Period



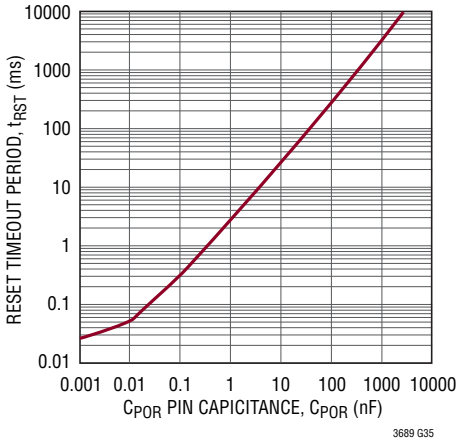
Reset Timeout Period



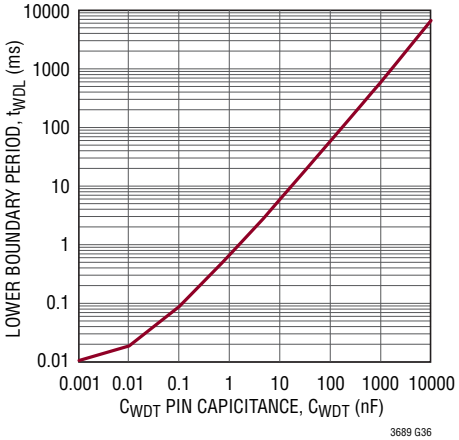
Watchdog Upper Boundary Period vs Capacitance



Reset Timeout Period vs Capacitance



Watchdog Lower Boundary Period vs Capacitance



PIN FUNCTIONS

BST: The BST pin is used to provide drive voltage higher than the input voltage to the internal NPN power switch.

V_{IN}: The V_{IN} pin supplies current to the LT3689's internal circuitry and to the internal power switch and must be locally bypassed.

SW: The SW pin is the output of the internal power switch. Connect this pin to the inductor, catch diode and boost capacitor.

DA: Tie the DA pin to the anode of the external catch Schottky diode. If the DA pin current exceeds 1.2A, which could occur in an overload or short-circuit condition, switching is disabled until the DA pin current falls below 1.2A.

EN/UVLO: The EN/UVLO pin is used to put the LT3689 in shutdown mode. Pull the pin below 0.3V to shut down the LT3689. The 1.26V threshold can function as an accurate undervoltage lockout (UVLO), preventing the regulator from operating until the input voltage has reached the programmed level.

FB: The LT3689 regulates the feedback pin to 0.800V. Connect the feedback resistor divider tap to this pin. For the fixed LT3689-5 output, this pin can be used to connect a phase lead capacitor between the OUT pin and FB pin to optimize transient response.

$\overline{WDE}$: Watchdog Timer Enable Pin. This pin disables the watchdog timer if the $\overline{WDE}$ voltage exceeds 1V. $\overline{WDO}$ is high in this condition.

$\overline{W}$/T: Setting $\overline{W}$/T low puts the LT3689 watchdog timer into window mode. If two or more negative edges occur on WDI before the watchdog lower boundary (t_{WDL}) period expires, or no negative edge occurs within the watchdog upper boundary (t_{WDU}) period, the part will set $\overline{WDO}$ low. If $\overline{W}$/T is set high, the part will only set $\overline{WDO}$ low if no transition occurs within the watchdog upper boundary period.

WDI: Watchdog Timer Input Pin. This pin receives the watchdog signal from a microprocessor. If the appropriate signal is not received, the part will pulse $\overline{WDO}$ low for a period equal to the reset timeout period. The watchdog timer is disabled until the $\overline{WDO}$ pin goes high again.

$\overline{RST}$: Active low, open collector logic output with a weak pull-up to V_{OUT}. After V_{OUT} rises above 90% of its programmed value, the reset remains asserted for the period set by the capacitor on the C_{POR} pin.

$\overline{WDO}$: Active low, open collector logic output with weak pull-up to V_{OUT}. $\overline{WDO}$ pulls low if the $\overline{WDE}$ is enabled and the microprocessor fails to drive the WDI pin of the LT3689 with an appropriate signal.

C_{WDT}: Watchdog Timer Programming Pin. Place a capacitor (C_{WDT}) between this pin and ground to adjust the watchdog upper and lower boundary period. To determine the watchdog upper boundary period, and the lower boundary period, use the following equations:

$t_{WDU} = 18.2 \bullet C_{WDT}$ (watchdog upper boundary period)

$t_{WDL} = 0.588 \bullet C_{WDT}$ (watchdog lower boundary period)

t_{WDU} and t_{WDL} are in ms and C_{WDT} is in nF. As an example, a 47nF capacitor will generate an 855ms watchdog upper boundary period and a 27.6ms watchdog lower boundary period.

C_{POR}: Reset Delay Timer Programming Pin. Attach an external capacitor (C_{POR}) to GND to set a reset delay time of 2.3ms/nF.

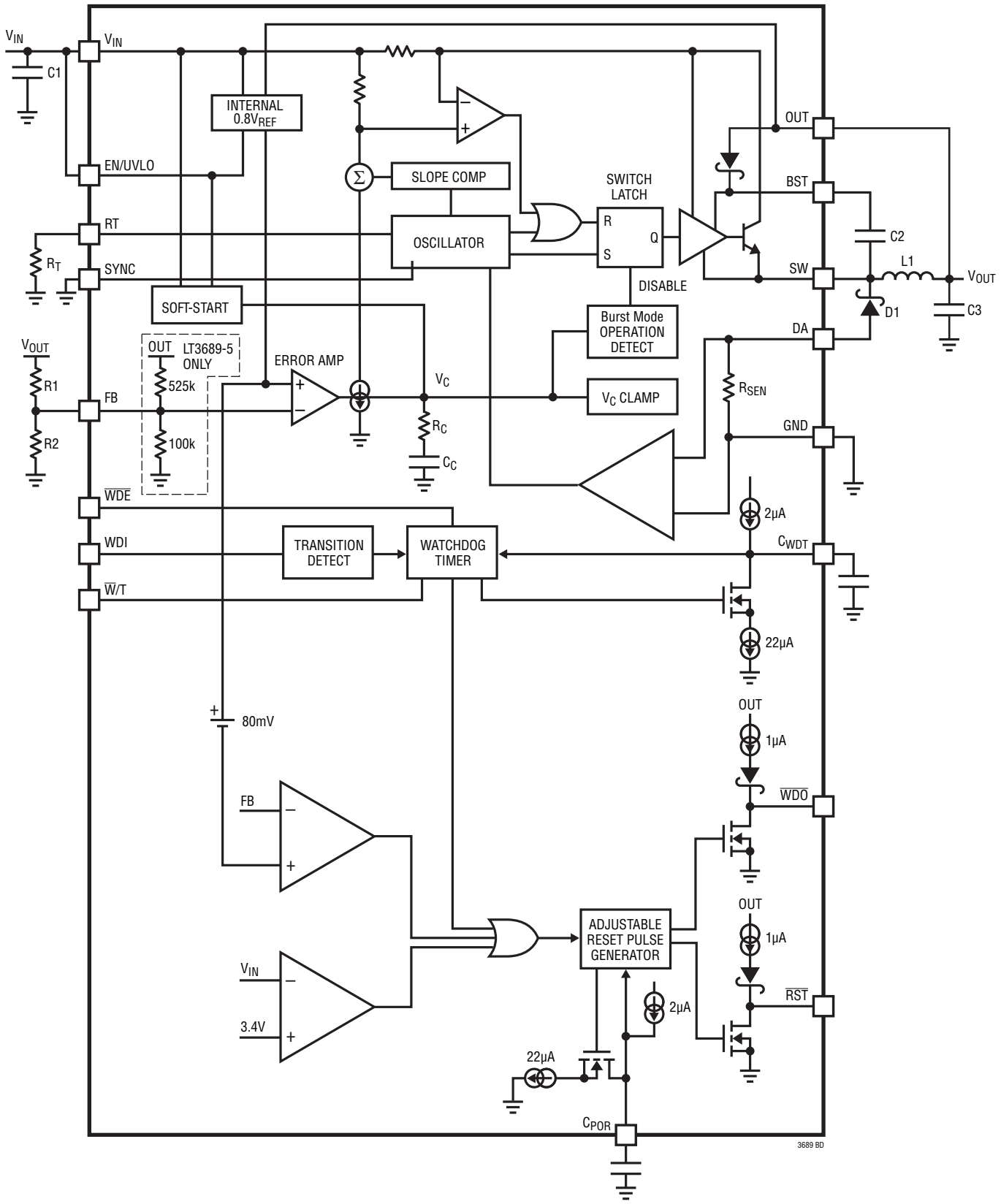
RT: Sets the Internal Oscillator Frequency. Tie a 31.6k resistor from RT to GND for a 500kHz switching frequency.

SYNC: Drive the SYNC pin with a logic level signal with positive and negative pulse widths of at least 80ns. The R_T resistor should be chosen to set the LT3689 switching frequency at least 20% below the lowest synchronization input frequency.

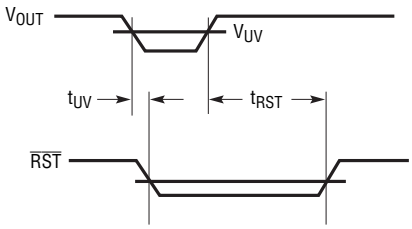
OUT: The OUT pin supplies current to the internal circuitry when OUT is above 3V, reducing input quiescent current. The internal Schottky diode is connected from OUT to BST, providing the charging path for the boost capacitor. For the LT3689-5, this pin connects to the internal feedback divider that programs the fixed 5V output.

GND: Ground. Tie the exposed pad directly to the ground plane. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board. The device must be soldered to the circuit board for proper operation.

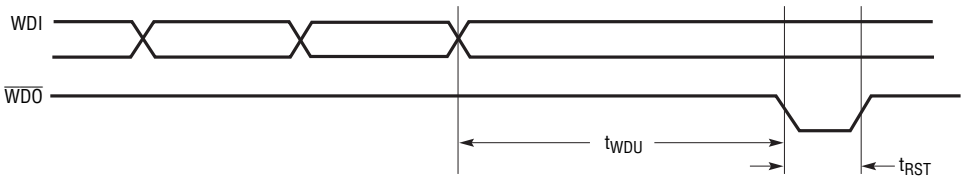
BLOCK DIAGRAM



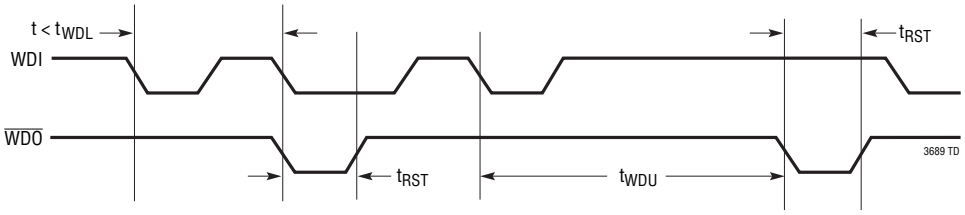
TIMING DIAGRAMS



POWER-ON RESET TIMING



WATCHDOG TIMING ($\overline{W}$/T = HIGH), TIMEOUT MODE



WATCHDOG TIMING ($\overline{W}$/T = LOW), WINDOW MODE

t_{UV} = TIME REQUIRED TO ASSERT $\overline{RST}$ LOW ONCE V_{OUT} GOES BELOW V_{UV}
t_{RST} = PROGRAMMED RESET PERIOD
t_{WDU} = WATCHDOG UPPER BOUNDARY PERIOD
t_{WDL} = WATCHDOG WINDOW MODE LOWER BOUNDARY PERIOD
V_{UV} = OUTPUT VOLTAGE RESET THRESHOLD

OPERATION

The LT3689 is a constant-frequency, current mode step-down regulator with a watchdog and a reset timer that allows microprocessor supervisory functions. Operation can be best understood by referring to the Block Diagram. Keeping the EN/UVLO pin at ground completely shuts off the part drawing minimal current from the V_{IN} source. To turn on the internal bandgap and the rest of the logic circuitry, raise the EN/UVLO pin above the accurate threshold of 1.26V. Also, V_{IN} needs to be higher than 3.7V for the part to start switching.

Switching Regulator Operation

An oscillator, with frequency set by R_T, enables an RS flip-flop, turning on the internal power switch. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at V_C. An error amplifier measures the output voltage through the resistor divider tied to the FB pin and servos the V_C voltage. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. An active clamp on the V_C voltage provides current limit.

An internal regulator provides power to the control circuitry. The bias regulator normally draws current from the V_{IN} pin, but if the OUT pin is connected to an external voltage higher than 3V, bias current will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The OUT pin also provides a current path to the internal boost diode that charges up the boost capacitor. The switch driver operates either from the V_{IN} or from the BST pin. An external capacitor is used to generate a voltage at the BST pin that is higher than the V_{IN} supply. This allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation. To further optimize efficiency, the LT3689 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 85µA in a typical application. The oscillator reduces the LT3689's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during start-up and overload conditions.

A comparator monitors the current flowing through the catch diode via the DA pin. This comparator delays switching if the diode current goes higher than 1.2A (typical) during a fault condition such as a shorted output with high input voltage. The switching will only resume once the diode current has fallen below the 1.2A limit. This way the DA comparator regulates the valley current of the inductor to 1.2A during a short-circuit.

The LT3689 has an overvoltage protection feature which disables switching when the V_{IN} goes above 38V (typical) during transients. When switching is disabled, the LT3689 can safely sustain transient input voltages up to 60V.

Power-On Reset and Watchdog Timer Operation

The LT3689 has a power-on reset (POR) comparator that monitors the regulated output voltage. If the output voltage is below 10% of the regulation value, the $\overline{RST}$ pin is pulled low. Once the output voltage crosses over 90% of the regulation value, a reset timer is started and $\overline{RST}$ is released after the programmed reset delay time. The reset delay is programmable through the C_{POR} pin.

The watchdog typically monitors a microprocessor's activity. The watchdog can be enabled or disabled by applying a logic signal to the $\overline{WDE}$ pin. The watchdog can be operated in either timeout or window mode by applying a logic signal to the $\overline{W}$/T pin. In timeout mode, the microprocessor is required to change the logic state of the WDI pin on a periodic basis in order to clear the watchdog timer and to prevent the $\overline{WDO}$ from going low. In window mode, the watchdog timer requires successive negative edges on the WDI pin to come within a programmed time window to keep $\overline{WDO}$ from going low. Therefore, in window mode, if the time between the two negative WDI edges is too short or too long, then the $\overline{WDO}$ pin will be pulled low. When the $\overline{WDO}$ pin goes low, either in timeout or in window mode, the reset timer turns on and keeps the $\overline{WDO}$ pin low. The $\overline{WDO}$ pin will go high again once the reset timer expires or the $\overline{RST}$ pin goes low when the output voltage falls 10% below the regulation value. Both the timeout and window periods can be set through the C_{WDT} pin.

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The output voltage is programmed with a resistor divider between the output and the FB pin. Choose 1% resistors according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$

For reference designators, refer to the Block Diagram.

Setting the Switching Frequency

The LT3689 uses a constant-frequency PWM architecture that can be programmed to switch from 350kHz to 2.2MHz by using a resistor tied from the RT pin to ground. Table 1 shows the R_T values for various switching frequencies.

Table 1. Switching Frequency vs R_T

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
0.35	48.7
0.5	31.6
0.6	24.9
0.7	20.5
0.8	16.9
0.9	14.7
1	12.7
1.2	9.53
1.4	7.5
1.6	6.04
1.8	4.87
2	4.02
2.2	3.16

Operating Frequency Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, and narrower input voltage range at constant-frequency. The highest constant-switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_D}{t_{ON(MIN)}\left(V_{IN} - V_{SW} + V_D\right)}$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.5V) and V_{SW} is the internal switch drop (~0.5V at maximum load). If the LT3689 is programmed to operate at a frequency higher than $f_{SW(MAX)}$ for a given V_{IN} input voltage, the LT3689 enters pulse-skipping mode, where it skips switching cycles to maintain regulation. At frequencies higher than $f_{SW(MAX)}$, the LT3689 no longer operates with constant-frequency. The LT3689 enters pulse-skipping mode at frequencies higher than $f_{SW(MAX)}$ because of the limitation on the LT3689's minimum on-time of 130ns. As the switching frequency is increased above $f_{SW(MAX)}$, the part is required to switch for shorter periods of time to maintain the same duty cycle. Delays associated with turning off the power switch dictate the minimum on-time of the part. When the required on-time decreases below the minimum on-time of 130ns, the switch pulse width remains fixed at 130ns (instead of becoming narrower to accommodate the duty cycle requirement). The inductor current ramps up to a value exceeding the load current and the output ripple increases. The part then remains off until the output voltage dips below the programmed value before it begins switching again.

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Maximum Operating Voltage

The maximum input voltage for LT3689 applications depends on switching frequency, the absolute maximum ratings of the V_{IN} and BST pins, and by the minimum duty cycle (DC_{MIN}). The LT3689 can operate from input voltages up to 36V, and safely withstand input transient voltages up to 60V. Note that while V_{IN} > 38V (typical), the LT3689 will stop switching, allowing the output to fall out of regulation.

$$DC_{MIN} = t_{ON(MIN)} \bullet f_{SW}$$

where $t_{ON(MIN)}$ is equal to 130ns (for T_J > 125°C $t_{ON(MIN)}$ is equal to 150ns) and f_{SW} is the switching frequency. Running at a lower switching frequency allows a lower minimum duty cycle. The maximum input voltage before pulse-skipping occurs depends on the output voltage and the minimum duty cycle:

$$V_{IN(PS)} = \frac{V_{OUT} + V_D}{DC_{MIN}} - V_D + V_{SW}$$

Example: f_{SW} = 790kHz, V_{OUT} = 3.3V,

DC_{MIN} = 130ns • 790kHz = 0.103

$$V_{IN(PS)} = \frac{3.3V + 0.4V}{0.103} - 0.4V + 0.4V = 36V$$

The LT3689 will regulate the output current at input voltages greater than $V_{IN(PS)}$. For example, an application with an output voltage of 1.8V and switching frequency of 1.5MHz has a $V_{IN(PS)}$ of 11.3V, as shown in Figure 1. Figure 2 shows operation at 24V. Output ripple and peak inductor current have significantly increased. A saturating inductor may further reduce performance. For input voltages over 30V, there are restrictions on the inductor size and saturation rating. See the Inductor Selection section for more details. In pulse-skipping mode, the LT3689 skips switching pulses to maintain output regulation. Above 38V (typical) switching will stop. Transients of up to 60V are acceptable, regardless of switching frequency.

Minimum Operating Voltage Range

The minimum input voltage is determined either by the LT3689's minimum operating voltage of ~3.4V or by its maximum duty cycle. The duty cycle is the fraction of time that the internal switch is on and is determined by the input and output voltages:

$$DC = \frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D}$$

Unlike many fixed frequency regulators, the LT3689 can extend its duty cycle by remaining on for multiple cycles. The LT3689 will not switch off at the end of each clock cycle if there is sufficient voltage across the boost capacitor (C3 in the Block Diagram). Eventually, the voltage on the boost capacitor falls and requires refreshing. Circuitry detects

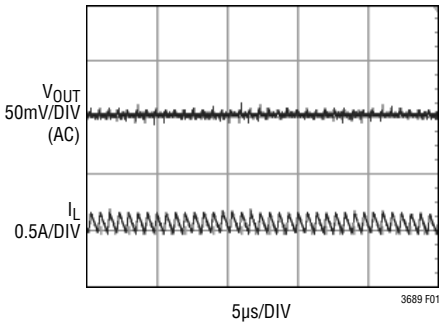

Figure 1. Operation Below $V_{IN(PS)}$. V_{IN} = 10V, V_{OUT} = 1.8V and f_{SW} = 1.5MHz

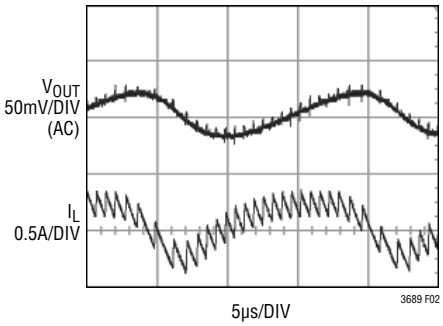

Figure 2. Operation Above $V_{IN(PS)}$. V_{IN} = 24V, V_{OUT} = 1.8V and f_{SW} = 1.5MHz. Output Ripple and Peak Inductor Current Increase

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this condition and forces the switch to turn off, allowing the inductor current to charge up the boost capacitor. This places a limitation on the maximum duty cycle. The maximum duty cycle that the LT3689 can sustain is 90%. From this DC_{MAX} number, the minimum operating voltage can be calculated using the following equation:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_D}{0.90} - V_D + V_{SW}$$

Example: V_{OUT} = 3.3V

$$V_{IN(MIN)} = \frac{3.3V + 0.4V}{0.90} - 0.4V + 0.4V = 4.1V$$

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = (V_{OUT} + V_F) \bullet \frac{2.2MHz}{f_{SW}}$$

where V_F is the voltage drop of the catch diode (~0.4V), f_{SW} is the switching frequency in MHz, and L is in µH. The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be at least 30% higher. For robust operation in fault conditions (start-up or short-circuit) and high input voltage (>30V), use an 8.2µH or greater inductor (for $T_J > 125°C$, use 10µH or larger) with a saturation rating of 2.5A, or higher. To keep the efficiency high, the series resistance (DCR) should be less than 0.15Ω and the core material should be intended for high frequency applications. Table 2 lists several vendors and suitable types.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT3689 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3689 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. Also, if the inductor current's bottom peak exceeds the DA current limit ($I_{LIM(DA)}$) at high output currents then the DA current comparator will regulate the bottom peak to $I_{LIM(DA)}$. This will result in higher inductor ripple current and will further limit the max output current. The DA current limit consists of a DC and an AC component. The nominal DC component is fixed at 1.2A. The AC component depends on the output voltage, inductor size and a fixed time delay between the DA comparator turning off and switch turning on. Therefore, the DA current limit $I_{LIM(DA)}$ will increase as the output voltage collapses under overload conditions.

$$I_{LIM(DA)} = 1.2A - \frac{(V_{OUT} + V_D)}{L} \bullet 0.25\mu s$$

Table 2. Inductor Vendors

VENDOR	URL	PART SERIES	INDUCTANCE RANGE (µH)	SIZE (mm)
Sumida	www.sumida.com	CDRH4D28 CDRH5D28	1.2 to 4.7 2.5 to 10	4.5 × 4.5 5.5 × 5.5
Toko	www.toko.com	A916CY D585LC	2 to 12 1.1 to 39	6.3 × 6.2 8.1 × 8
Würth Elektronik	www.we-online.com	WE-TPC(M) WE-PD2(M)	1 to 10 2.2 to 22	4.8 × 4.8 5.2 × 5.8

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Choose an inductor using the previous inductor selection equation to guarantee 700mA of output current. If using a smaller inductor, check the DA current limit equation to verify that the DA circuitry will not lower the switching frequency.

When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = \frac{(1-DC)(V_{OUT}+V_D)}{L \bullet f_{SW}}$$

where f_{SW} is the switching frequency of the LT3689 and L is the value of the inductor. The peak inductor and switch current is:

$$I_{SW(PK)} = I_{L(PK)} = I_{OUT} + \frac{\Delta I_L}{2}$$

To maintain output regulation, this peak current must be less than the LT3689's switch current limit I_{LIM}. I_{LIM} is at least 1.5A for at low duty cycles and decreases linearly to 0.87A at DC = 85%. The maximum output current is a function of the chosen inductor value.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

$$= 1.15A \bullet (1-0.28 \bullet DC) - \frac{\Delta I_L}{2}$$

Choosing an inductor value so that the ripple current is small will allow a maximum output current near the switch current limit.

One approach to choosing the inductor is to start with the preceding simple rule, determine the available inductors, and choose one to meet cost or space goals. Next, use these equations to check that the LT3689 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when I_{OUT} is less than $\Delta I_L/2$.

Of course, such a simple design guide will not always result in the optimum inductor for the application. A larger value inductor provides a slightly higher maximum load current and will reduce the output voltage ripple. If the load is lower than 0.7A, decrease the value of the inductor and operate with a higher ripple current. This allows the use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. There are graphs in the Typical Performance Characteristics section of this data sheet that show the maximum load current as a function of input voltage for several popular output voltages. Low inductance may result in discontinuous mode operation, which is okay but further reduces maximum load current. For details of maximum output current and discontinuous mode operation, see Linear Technology Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillations:

$$L_{MIN} = \frac{1.4\left(V_{OUT}+V_D\right)}{f_{SW}}$$

where L_{MIN} is in µH, V_{OUT} and V_D are in volts, and f_{SW} is in MHz.

Input Capacitor

Bypass the input of the LT3689 circuit with a ceramic capacitor of an X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. The minimum value of input capacitance depends on the switching frequency. Use an input capacitor of 1µF or more for switching frequencies between 1MHz to 2.2MHz, and 2.2µF or more for frequencies lower than 1MHz. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a lower performance electrolytic capacitor. Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3689 input and to force this very high frequency switching current into a tight local loop, minimizing EMI. A ceramic capacitor is capable of this task, but only if it is placed close to the LT3689 and the catch diode (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3689. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the

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LT3689 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3689's voltage rating. For a complete discussion, see Linear Technology's Application Note 88.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3689 to produce the DC output. In this role it determines the output ripple, and low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3689's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{50}{V_{OUT}\ f_{SW}}$$

where f_{SW} is in MHz, and C_{OUT} is the recommended output capacitance in µF. Use X5R or X7R types, which will provide low output ripple and good transient response. Transient performance can be improved with a high value capacitor, but a phase lead capacitor across the feedback resistor R1 may be required to get the full benefit (see the Frequency Compensation section).

High performance electrolytic capacitors can be used for the output capacitor. Low ESR is important, so choose one that is intended for use in switching regulators. The ESR should be specified by the supplier and should be 0.1Ω or less. Such a capacitor will be larger than a ceramic capacitor and will have a larger capacitance because the capacitor must be large to achieve low ESR. Table 3 lists several capacitor vendors.

Table 3. Capacitor Vendors

VENDOR	PHONE	URL
Panasonic	(714) 373-7366	www.panasonic.com
Kemet	(864) 963-6300	www.kemet.com
Sanyo	(408) 749-9714	www.sanyovideo.com
Murata	(408) 436-1300	www.murata.com
AVX		www.avxcorp.com
Taiyo Yuden	(864) 963-6300	www.taiyo-yuden.com

Catch Diode

The catch diode conducts current only during switch-off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT}\ (V_{IN} - V_{OUT})}{V_{IN}}$$

where I_{OUT} is the output load current. The only reason to consider a diode with a larger current rating than necessary for nominal operation is for the worst-case condition of shorted output. The diode current will then increase to the typical peak switch current limit. Peak reverse voltage is equal to the regulator input voltage. Use a Schottky diode with a reverse voltage rating greater than the input voltage. The overvoltage protection feature in the LT3689 will keep the switch off when V_{IN} > 38V (typical), which allows the use of a 40V rated Schottky even when V_{IN} ranges up to 60V. Table 4 lists several Schottky diodes and their manufacturers.

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Table 4. Diode Vendors

PART NUMBER	V_R (V)	I_{AVE} (A)	V_F AT I_{AVE} (mV)
On Semiconductor			
MBRM120E	20	1	530
MBRM140	40	1	550
Diodes Inc.			
B120	20	1	500
B130	30	1	500
B140	40	1	500
B0540W	40	0.5	510
B140HB	40	1	530

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT3689 due to their piezoelectric nature. When in Burst Mode operation, the LT3689's switching frequency depends on the load current, and at very light loads the LT3689 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT3689 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet. If this noise is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

Frequency Compensation

The LT3689 uses current mode control to regulate the output, which simplifies loop compensation. In particular, the LT3689 does not require the ESR of the output capacitor for stability, allowing the use of ceramic capacitors to achieve low output ripple and small circuit size. Figure 3 shows an equivalent circuit for the LT3689 control loop. The error amp is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C node. Note that the output capacitor, C1, integrates this current, and that the capacitor on the V_C node (C_C) integrates the error amplifier output current, resulting in two poles in the loop. R_C provides a zero. With the recommended output capacitor, the loop crossover occurs above the R_CC_C zero. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. With a larger ceramic capacitor (very low ESR), crossover may be lower and a phase lead capacitor (C_{PL}) across the feedback divider may improve the phase margin and transient response. Large electrolytic capacitors may have an ESR large enough to create an additional zero, and the phase lead may not be necessary.

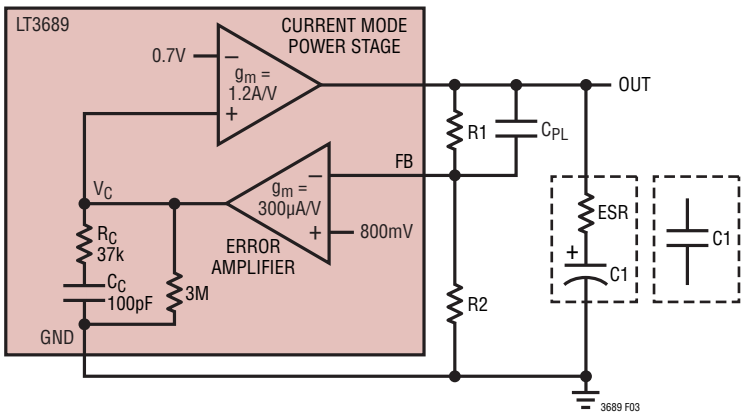

Figure 3. Model for the Loop Response

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Most applications running at V_{IN} greater than 20V will require a small phase lead capacitor, ranging from 2pF to about 30pF, between the FB pin and V_{OUT} for good transient response. The circuits in the Typical Applications section use the appropriate phase lead capacitors and are stable at all input voltages.

If the output capacitor is different than the recommended capacitor, stability should be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load. Figure 4 shows the transient response when the load current is stepped from 360mA to 720mA and back to 360mA.

Low Ripple Burst Mode Operation and Pulse-Skipping Mode

The LT3689 is capable of operating in either low ripple Burst Mode operation or pulse-skipping mode, which is selected using the SYNC pin. See the Synchronization section for details. To enhance efficiency at light loads, the LT3689 can be operated in low ripple Burst Mode operation that keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LT3689 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. Because the LT3689 delivers power to the output with single, low current pulses, the output ripple is kept below 15mV for a typical application. The LT3689-5 has a slightly higher output ripple of 25mV. This higher ripple can be reduced by using a larger output capacitor. In addition, V_{IN} and OUT quiescent currents are reduced to typically 50µA and 75µA, respectively, during the sleep time. As the load current decreases towards a no-load condition, the percentage of time that the LT3689 operates in sleep mode increases and the average input current is greatly reduced, resulting in high efficiency even at very low loads (see Figure 5).

At higher output loads (above approximately 60mA at V_{IN} = 12V for the front page application) the LT3689 will be running at the frequency programmed by the R_T resistor, and will be operating in standard PWM mode. The transition between PWM and low ripple Burst Mode operation is seamless, and will not disturb the output voltage. If low quiescent current is not required, the LT3689 can operate in pulse-skipping mode. The benefit of this mode is that the LT3689 will enter full frequency standard PWM operation at a lower output load current than when in Burst Mode operation. The front page application circuit will switch at full frequency at output loads higher than about 15mA at $12V_{IN}$.

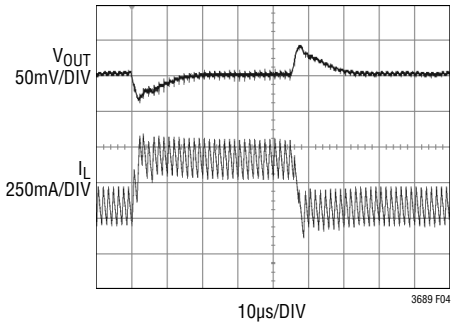

Figure 4. Transient Load Response of the LT3689 Front Page Application as the Load Current is Stepped from 360mA to 720mA. V_{OUT} = 3.3V, V_{IN} = 12V

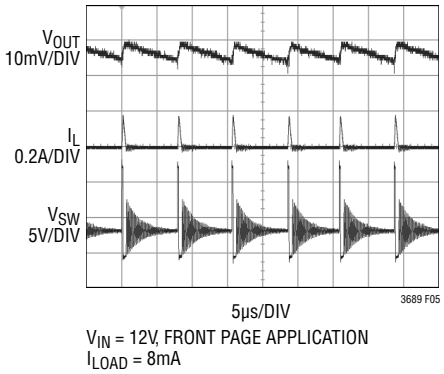

Figure 5. Burst Mode Operation

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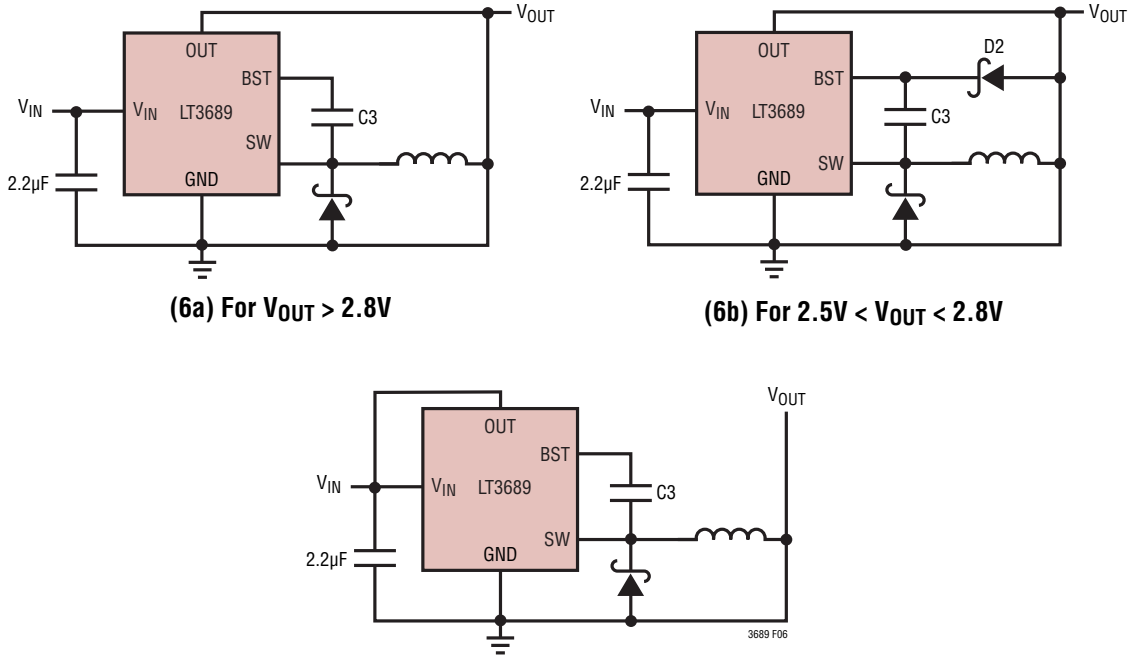
BST and OUT Pin Considerations

Capacitor C3 and the internal boost Schottky diode (see the Block Diagram) are used to generate a boost voltage that is higher than the input voltage. In most cases, a 0.1µF capacitor will work well. Figure 6 shows three ways to arrange the boost circuit. The BST pin must be more than 2.3V above the SW pin for best efficiency. For outputs of 3V and above, the standard circuit (Figure 6a) is best. For outputs between 2.8V and 3V, use a 0.47µF boost capacitor. A 2.5V output presents a special case because it is marginally adequate to support the boosted drive stage while using the internal boost diode. For reliable BST pin operation with 2.5V outputs, use a good external Schottky diode (such as ON Semiconductor's MBR0540), and a 0.47µF boost capacitor (see Figure 6b). For lower output voltages, the boost diode can be tied to the input (Figure 6c), or to another supply greater than 2.8V. The circuit in Figure 6a is more efficient because the BST pin current and OUT pin quiescent current comes from a lower voltage source. Ensure that the maximum voltage ratings of the BST and OUT pins are not exceeded.

The minimum operating voltage of an LT3689 application is limited by the minimum input voltage (3.7V) and by the maximum duty cycle, as outlined in the Minimum Operating Voltage Range section. For proper start-up, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or the LT3689 is turned on with its EN/UVLO pin when the output is already in regulation, then the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. For lower start-up voltage, the boost diode can be tied to V_{IN}; however, this restricts the input range to one-half of the absolute maximum rating of the BST pin.



(6a) For $V_{OUT} > 2.8V$

(6b) For $2.5V < V_{OUT} < 2.8V$

(6c) For $V_{OUT} < 2.5V$; $V_{IN(MAX)} = 30V$

Figure 6. Three Circuits for Generating the Boost Voltage

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Another way to lower the start-up voltage is by using a resistor divider on the EN/UVLO pin (see the Shutdown and Undervoltage Lockout section). A resistor divider on EN/UVLO pin programs the turn-on threshold to slightly higher than the minimum V_{IN} voltage required to run at full load. Below the EN/UVLO high voltage, the part will stay shut off and the output cap will remain discharged during the worse case slow V_{IN} ramp. When the EN/UVLO pin crosses the EN/UVLO high threshold, the part will turn on and the empty output capacitor will provide enough load to bring the output voltage in regulation. This technique significantly lowers the start-up voltage of the circuit. The plot in Figure 7 depicts the minimum load required to start and run (as a function of input voltage). It also depicts the benefit of programming the EN/UVLO threshold to lower the start-up voltage at low load currents. At light loads, the inductor current becomes discontinuous and the effective duty cycle can be very high. This reduces the minimum input voltage to approximately 300mV above V_{OUT}. At higher load currents, the inductor current is continuous and the duty cycle is limited by the maximum duty cycle of the LT3689, requiring a higher input voltage to maintain regulation.

Soft-Start

The LT3689 has an internal soft-start that gradually ramps up the switch current limit from about 100mA to the switch's maximum current limit in typical value of 150µs, as shown in Figure 8. This feature limits the inrush current during start-up and prevents the switch current from spiking when the EN/UVLO pin crosses the UVLO threshold. A soft-start sequence is also initiated right after a V_{IN} overvoltage/undervoltage lockout, or thermal shutdown fault in order to prevent the switch current from suddenly jumping to its maximum current limit.

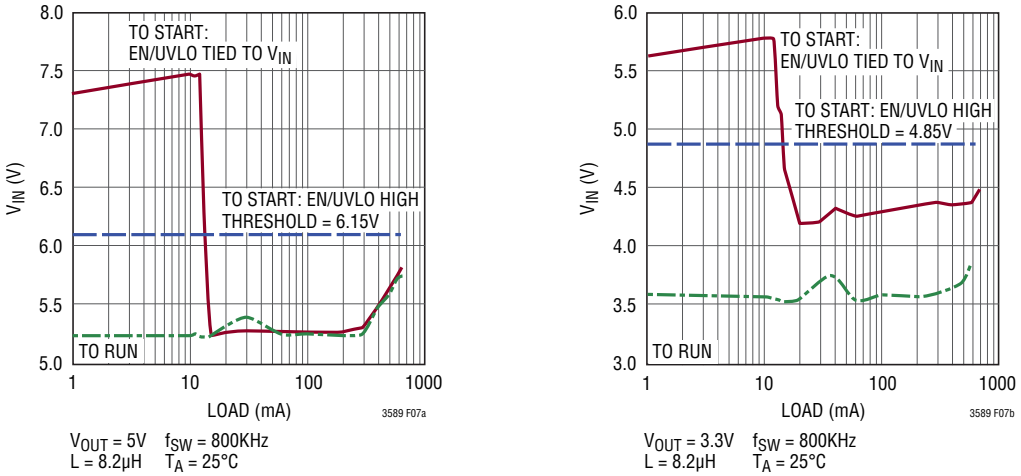

Figure 7. LT3689 Minimum V_{IN} to Start and Run vs Load

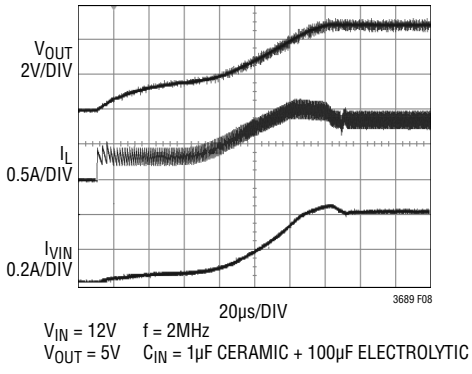

Figure 8. Internal Soft-Start

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Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.3V (this can be ground or a logic output). Synchronizing the LT3689 oscillator to an external frequency can be done by connecting a square wave (with positive and negative pulse width >80ns) to the SYNC pin. The square wave amplitude should have valleys that are below 0.3V and peaks that are above 1V (up to 6V).

The LT3689 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will skip pulses to maintain regulation.

The LT3689 may be synchronized over a 350kHz to 2.5MHz range. The R_T resistor should be chosen to set the LT3689 switching frequency 20% below the lowest synchronization input. For example, if the synchronization signal will be 350kHz and higher, the R_T should be chosen for 280kHz. To assure reliable and safe operation, the LT3689 will only synchronize when the output voltage is above 90% of its regulated voltage. It is therefore necessary to choose a large enough inductor value to supply the required output current at the frequency set by the R_T resistor (see the Inductor Selection section). It is also important to note that the slope compensation is set by the R_T value. When the sync frequency is much higher than the one set by R_T, the slope compensation will be significantly reduced, which may require a larger inductor value to prevent subharmonic oscillation. The minimum inductor value should be calculated using the RT programmed frequency to avoid subharmonic oscillation.

Shutdown and Undervoltage Lockout

Figure 9 shows how to add undervoltage lockout (UVLO) to the LT3689. Typically, UVLO is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where the problems might occur. An internal comparator will force the part into shutdown below the minimum V_{IN} of 3.4V. This feature can be used to prevent excessive discharge of battery-operated systems. If an adjustable UVLO threshold is required, the EN/UVLO pin can be used. The threshold voltage of the EN/UVLO pin comparator is 1.26V. Current hysteresis is added above the EN threshold. This can be used to set voltage hysteresis of the UVLO using the following:

$$R3 = \frac{V_H - V_L}{4\mu A} - 4k$$

$$R4 = \frac{1.26V}{\left(\frac{V_H - 1.26V}{R3}\right) - 4\mu A}$$

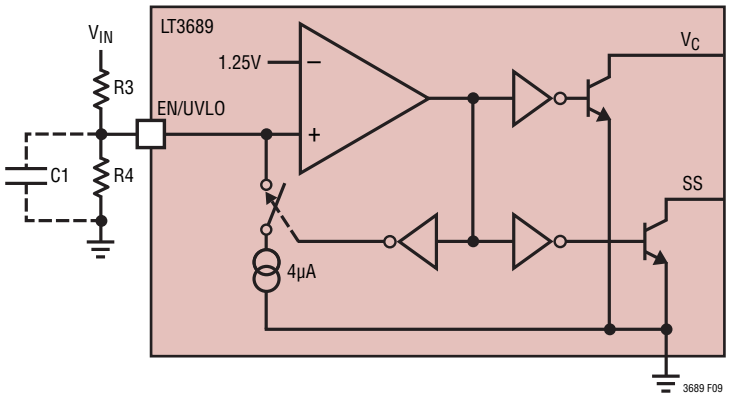

Figure 9. Undervoltage Lockout

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Example: switching should not start until the input is above 4.40V, and is to stop if the input falls below 4V.

$$V_H = 4.40V, V_L = 4V$$

$$R3 = \frac{4.40V - 4V}{4\mu A} - 4k = 95.3k$$

$$R4 = \frac{1.26V}{\frac{4.40V - 1.26V}{95.3k} - 4\mu A} = 43.2k \quad \text{(Nearest 1\% Resistor)}$$

Keep the connection from the resistor to the EN/UVLO pin short and make sure the interplane or surface capacitance to switching nodes is minimized. If high resistor values are used, the EN/UVLO pin should be bypassed with a 1nF capacitor to prevent coupling problems from the switch node.

Output Voltage Monitoring

The LT3689 provides power supply monitoring for microprocessor-based systems. The features include power-on reset (POR) and watchdog timing.

A precise internal voltage reference and glitch immune precision POR comparator circuit monitor the LT3689 output voltage. The switcher's output voltage must be above 90% of programmed value for $\overline{RST}$ not to be asserted (refer to the Timing Diagram). The LT3689 will assert $\overline{RST}$ during power-up, power-down and brownout conditions. Once the output voltage rises above the $\overline{RST}$ threshold, the adjustable reset timer is started and $\overline{RST}$ is released after the reset timeout period. On power-down, once the output voltage drops below $\overline{RST}$ threshold, $\overline{RST}$ is held at a logic low. The reset timer is adjustable using external capacitors. The $\overline{RST}$ pin has a weak pull-up to the OUT pin.

The POR comparator is designed to be robust against FB pin noise, which could potentially false trigger the $\overline{RST}$ pin. The POR comparator lowpass filters the first stage of the comparator. This filter integrates the output of the comparator before asserting the $\overline{RST}$. The benefit of adding this filter is that any transients at the buck regulator's output must be of sufficient magnitude and duration before it triggers a logic change in the output (see the Typical Transient vs POR Comparator Overdrive in the Typical Performance Characteristics section). This prevents spurious resets caused by output voltage transients such as load steps or short brownout conditions without sacrificing the DC reset threshold accuracy.

Watchdog

The LT3689 includes an adjustable watchdog timer that monitors a µP's activity. If a code execution error occurs in a µP, the watchdog will detect this error and will set the $\overline{WDO}$ low. This signal can be used to interrupt a routine or to reset a microprocessor.

The watchdog is operated either in timeout or window mode. In timeout mode, the microprocessor needs to toggle the WDI pin before the watchdog timer expires, to keep the $\overline{WDO}$ pin high. If no WDI pulse (either positive or negative) appears during the programmed timeout period, then the circuitry will pull $\overline{WDO}$ low. During normal operation, the WDI input signal's high to low, and low to high transition periods should be set lower than the watchdog's programmed time to keep $\overline{WDO}$ inactive.

In window mode, the watchdog circuitry is triggered by negative edges on the WDI pin. The window mode restricts the WDI pin's negative going pulses to appear inside a programmed time window (see the Timing Diagram) to prevent $\overline{WDO}$ from going low. If more than two pulses are registered in the watchdog lower boundary period, the $\overline{WDO}$ is forced to go low. The WDI edges are ignored while the C_{WDT} capacitor charges from 0V to 200mV right after a low to high transition on the $\overline{WDO}$ or $\overline{RST}$ pin. The $\overline{WDO}$ also goes low if no negative edge is supplied to the WDI pin in the watchdog upper boundary period. During a code execution error, the microprocessor will output WDI pulses that would be either too fast or too slow. This condition will assert $\overline{WDO}$ and force the microprocessor to reset the program. In window mode, the WDI signal frequency is bounded by an upper and lower limit for normal operation. The WDI input frequency period should be higher than the t_{WDL} period, and lower than the t_{WDU} period, to keep $\overline{WDO}$ high under normal conditions. The window mode's t_{WDL} and t_{WDU} times have a fixed ratio of 31 between them. These times can be increased or decreased by adjusting an external capacitor on the C_{WDT} pin.

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In both watchdog modes, when $\overline{WDO}$ is asserted, the reset timer is enabled. Any WDI pulses that appear while the reset timer is running are ignored. When the reset timer expires, the $\overline{WDO}$ is allowed to go high again. Therefore, if no input is applied to the WDI pin, then the watchdog circuitry produces a train of pulses on the $\overline{WDO}$ pin. The high time of this pulse train is equal to the timeout period, and low time is equal to the reset period. Also, $\overline{WDO}$ and $\overline{RST}$ cannot be logic low simultaneously. If $\overline{WDO}$ is low and $\overline{RST}$ goes low, then $\overline{WDO}$ will go high.

The $\overline{WDE}$ pin allows the user to turn on and off the watchdog function. Do not leave this pin open. Tie it high or low to turn watchdog off or on, respectively. The $\overline{W}$/T pin enables/disables the window/timeout mode. Leaving this pin open is fine and will put the watchdog in window mode. It has a weak pull-down to ground. The WDI pin has an internal 2µA weak pull-up that keeps the WDI pin high. If watchdog is disabled, leaving this pin open is acceptable.

Selecting the Reset Timing Capacitors

The reset timeout period is adjustable in order to accommodate a variety of microprocessor applications. The reset timeout period, (t_{RST}), is adjusted by connecting a capacitor, C_{POR}, between the C_{POR} pin and ground. The value of this capacitor is determined by:

$$C_{POR} = t_{RST} \bullet 432\left(\frac{pF}{ms}\right)$$

This equation is accurate for reset timeout periods of 5ms, or greater. To program faster timeout periods, see the Reset Timeout Period vs Capacitance graph in the Typical Performance Characteristics section. Leaving the C_{POR} pin unconnected will generate a minimum reset timeout of approximately 25µs. Maximum reset timeout is limited by the largest available low leakage capacitor. The accuracy of the timeout period will be affected by

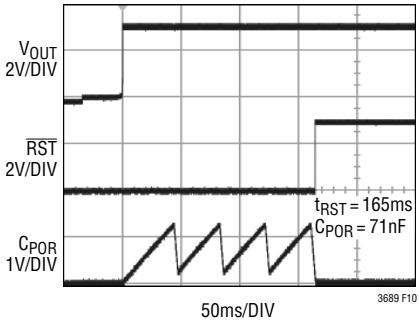

Figure 10. Reset Timer Waveforms

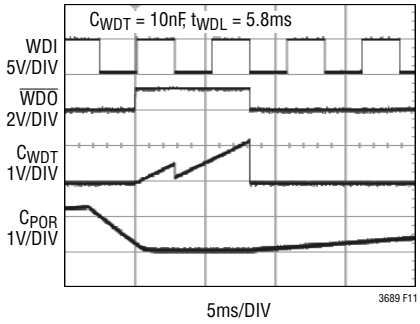

Figure 11. Window Watchdog Waveforms ($\overline{W}$/T = Low)

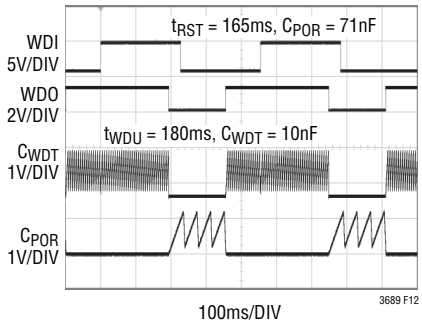

Figure 12. Timeout Watchdog Waveforms ($\overline{W}$/T = High)

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capacitor leakage (the nominal charging current is 2µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

Selecting the Watchdog Timing Capacitor

The watchdog timeout period is adjustable and can be optimized for software execution. The watchdog upper boundary timeout period, t_{WDU} is adjusted by connecting a capacitor, C_{WDT}, between the C_{WDT} pin and ground. Given a specified watchdog timeout period, the capacitor is determined by:

$$C_{WDT} = t_{WDU} \bullet 55\left(\frac{pF}{ms}\right)$$

This equation is accurate for upper boundary periods of 20ms, or greater. The watchdog lower boundary period (t_{WDL}) has a fixed relationship to t_{WDU} for a given capacitor. The t_{WDL} period is related to t_{WDU} by the following:

$$t_{WDL} = \frac{1}{31} \bullet t_{WDU}$$

In addition, the following equation can be used to calculate the watchdog lower boundary period for a given C_{WDT} capacitor value.

$$C_{WDT} = t_{WDL} \bullet \frac{1.7nF}{ms}$$

These lower boundary period equations are accurate for a t_{WDL} of 3ms, or greater. To program faster t_{WDU} and t_{WDL} periods, see the Watchdog Upper and Lower Boundary Periods vs Capacitance graphs in the Typical Performance Characteristics section.

Leaving the C_{WDT} pin unconnected will generate a minimum watchdog timeout of approximately 200µs. Maximum timeout is limited by the largest available low leakage capacitor. The accuracy of the timeout period will be affected by capacitor leakage (the nominal charging current is 2µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

Time Charts for the Power-On-Reset and Watch Dog Timers

The watchdog timer monitors proper operation of the microprocessor. During the start-up sequence of the microprocessor, there are fixed requirements for the watch dog input (WDI) in order to keep the $\overline{WDO}$ pin from flagging a fault.

Requirements for the watch dog input in window mode (W/T = Low) are best understood by looking at Figure 13. In window mode, the WDI pin detects falling edges. These edges are ignored until the power-on-reset timer expires, and the CWDT pin has risen above 0.2V for the first time, as shown in Figure 13a. After that time, there must be a falling edge on the WDI pin before the watchdog timer expires, which will happen within t_{WDU} (a minimum of 17ms while using 1000pF for CWDT). After this first valid falling edge, subsequent edges must follow the timing sequence outlined in Figure 13b. Each subsequent edge must occur after t_{WDL} (a maximum of 785µs while using 1000pF for CWDT) and before t_{WDU}.

If there is a timing fault, the $\overline{WDO}$ pin will flag low, and will initiate a restart sequence using the power-on-reset timer, as shown in Figure 13c. The $\overline{RST}$ pin will remain high, however. WDI edges are ignored until the power-on-reset timer expires, and the CWDT pin has risen above 0.2V. After that time, there must be a falling edge on the WDI pin before the watchdog timer expires, which will happen within t_{WDU}. After this first valid falling edge, subsequent edges must follow the timing sequence outlined in Figure 13b.

Requirements for the watch dog input in timer mode (W/T = High) are best understood by looking at Figure 14. In timer mode, the WDI pin detects rising and falling edges. These edges are ignored until the power-on-reset timer expires, and the CWDT pin has risen above 0.2V for the first time, as shown in Figure 14a. After that time, there must be an edge on the WDI pin before the watchdog timer expires, which will happen within t_{WDU} (a minimum of 17ms while using 1000pF for CWDT). After this first edge, subsequent edges must follow the timing sequence outlined in Figure 14b. Each subsequent edge must occur before t_{WDU}.

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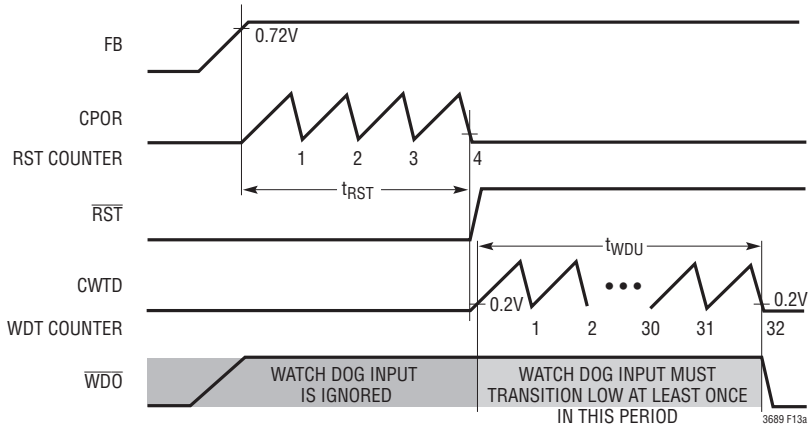
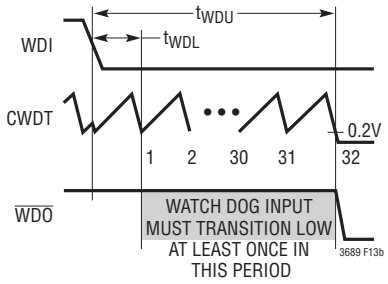
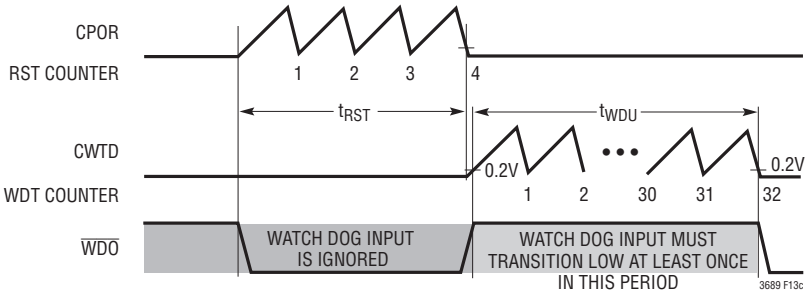


(13a) $\overline{W}$/T = Low. The First Valid Negative Edge on WDI Must Occur Before the Watchdog Timer Expires



(13b) $\overline{W}$/T = Low. Subsequent Negative Edges Must Occur Within a Fixed Time Window



(13c) $\overline{W}$/T = Low. Restart Sequence After a Timing Fault

Figure 13. $\overline{W}$/T = Low. Time Charts for the Power-On-Reset and Watchdog Timer in Window Mode

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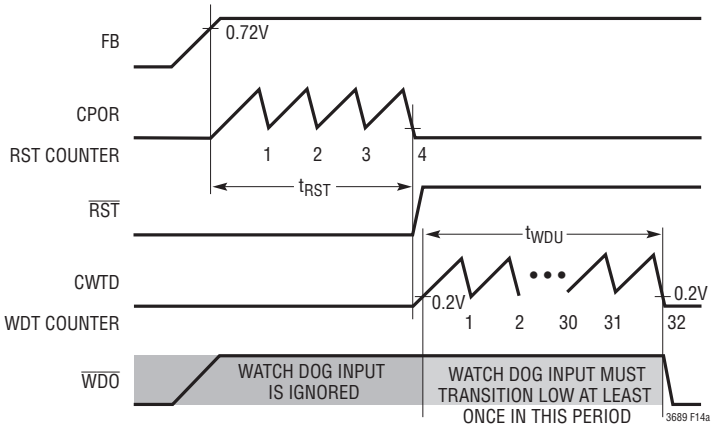
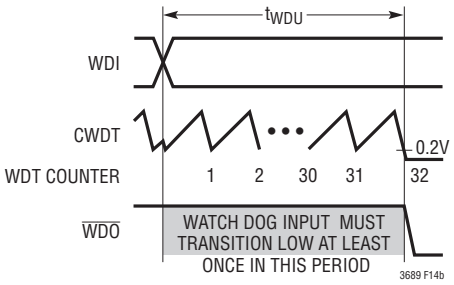
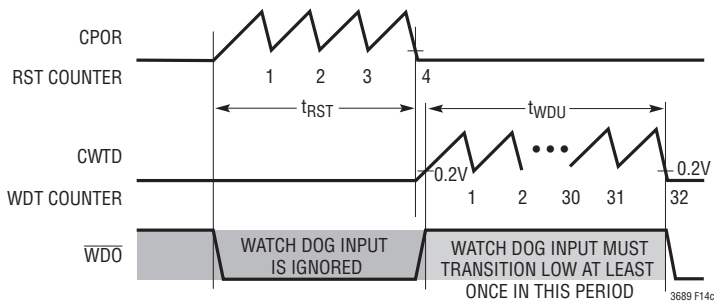


(14a) $\overline{W}$/T = High. The First Valid Negative Edge on WDI Must Occur Before the Watchdog Timer Expires



(14b) $\overline{W}$/T = High. Subsequent Edges Must Occur Before the Timer Expires



(14c) $\overline{W}$/T = Low. Restart Sequence After a Timing Fault

Figure 14. $\overline{W}$/T = High. Time Charts for the Power-On-Reset and Watchdog Timer in Timer Mode

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If there is a timing fault, the WDO pin will flag, low, and will initiate a restart sequence using the power-on-reset timer, as shown in Figure 14c. The $\overline{RST}$ pin will remain high, however. WDI edges are ignored until the power-on-reset timer expires, and the CWDT pin has risen above 0.2V for the first time. After that time, there must be an edge on the WDI pin before the watchdog timer expires, which will happen within t_{WDU}. After this first falling edge, subsequent edges must follow the timing sequence outlined in Figure 14b.

Shorted and Reversed Input Protection

If an inductor is chosen to prevent excessive saturation, the LT3689 will tolerate a shorted output. When operating in short-circuit condition, the LT3689 will reduce its frequency until the valley current is at a typical value of 1.2A (see Figure 15). There is another situation to consider in systems where the output will be held high when the input to the LT3689 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LT3689's output. If the V_{IN} pin is allowed to float and the EN/UVLO pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT3689's internal circuitry will pull its quiescent current through its SW pin. This is fine if the system can tolerate a few mA in this state. If the EN/UVLO pin is grounded, the SW pin current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LT3689 can pull large currents from the output through the SW pin and the V_{IN} pin. Figure 16 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

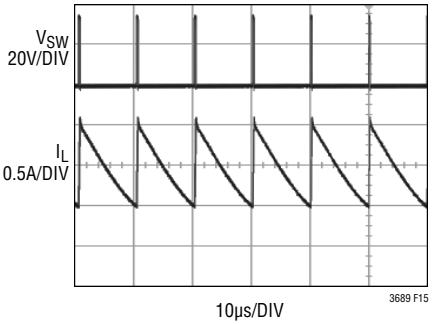


Figure 15. The LT3689 Reduces its Frequency to Below 100kHz to Protect Against Shorted Output with 36V Input

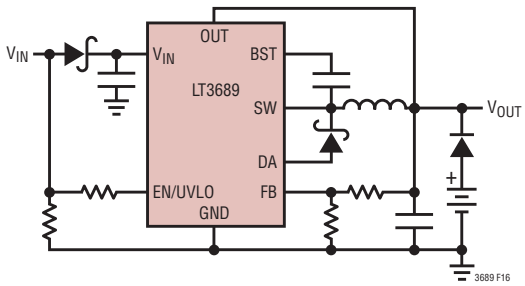


Figure 16. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output; It Also Protects the Circuit from a Reversed Input. The LT3689 Runs Only When the Input Is Present

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 17 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT3689's V_{IN} and SW pins, the catch diode (D1) and the input capacitor (C1). The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board. Place a local, unbroken ground plane below these components. The SW and BST nodes should be as small as possible. Finally, keep the FB node small so that the

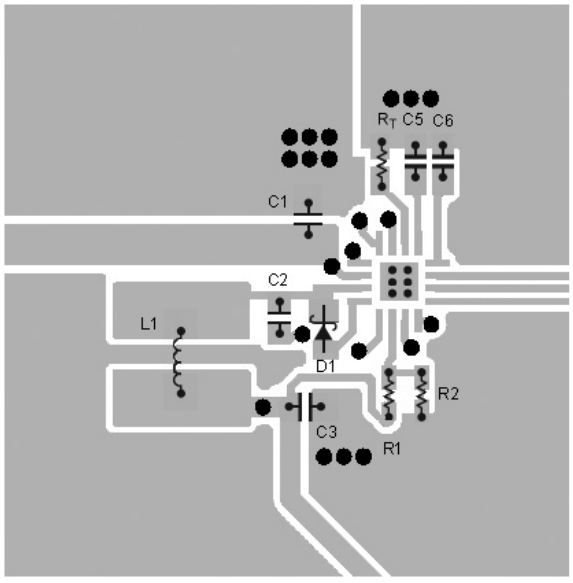


Figure 17. Example Layout for QFN Package. A Good PCB Layout Ensures Proper Low EMI Operation

APPLICATIONS INFORMATION

ground traces will shield them from the SW and BOOST nodes. The Exposed Pad on the bottom of the package must be soldered to ground so that the pad acts as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT3689 to additional ground planes within the circuit board and on the bottom side.

High Temperature Considerations

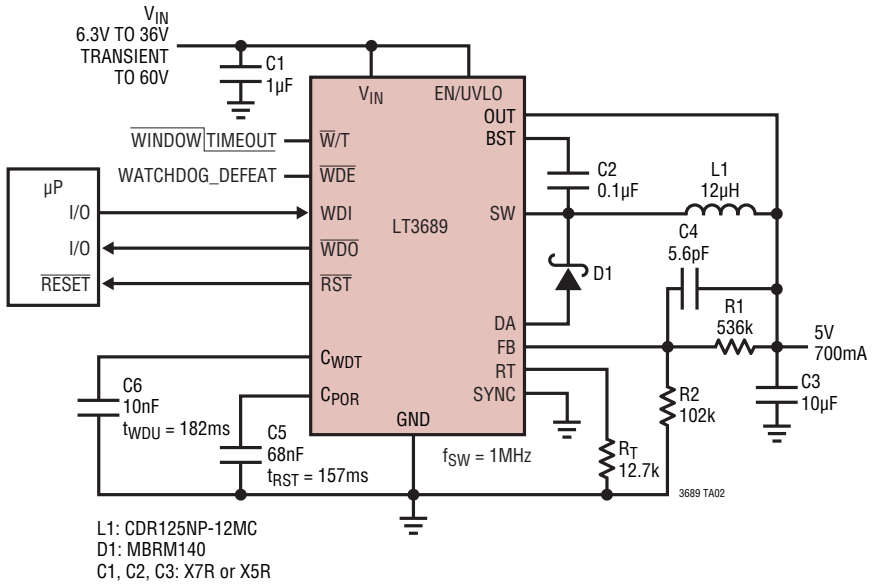
The PCB must provide heat sinking to keep the LT3689 cool. The Exposed Pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread the heat dissipated by the LT3689. Placing additional vias can reduce thermal resistance further. Because of the large output current capability of the LT3689, it is possible to dissipate enough heat to raise the junction temperature beyond the absolute maximum of 125°C (150°C for H-grade). When operating at high ambient temperatures, the maximum load current should be derated as the ambient temperature approaches 125°C (150°C for H-grade). A board measuring 5cm × 7.5cm with a top layer layout similar to Figure 15 was evaluated in still air at $3.3V_{OUT}$, 700kHz switching frequency. At 700mA load, the temperature reached approximately 12°C above ambient for input voltages equal to 12V and 24V. Power dissipation within the LT3689 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the catch diode loss. The die temperature is calculated by multiplying the LT3689 power dissipation by the thermal resistance from junction-to-ambient.

Other Linear Technology Publications

Application Notes 19, 35 and 44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note 318 shows how to generate a bipolar output supply using a buck regulator.

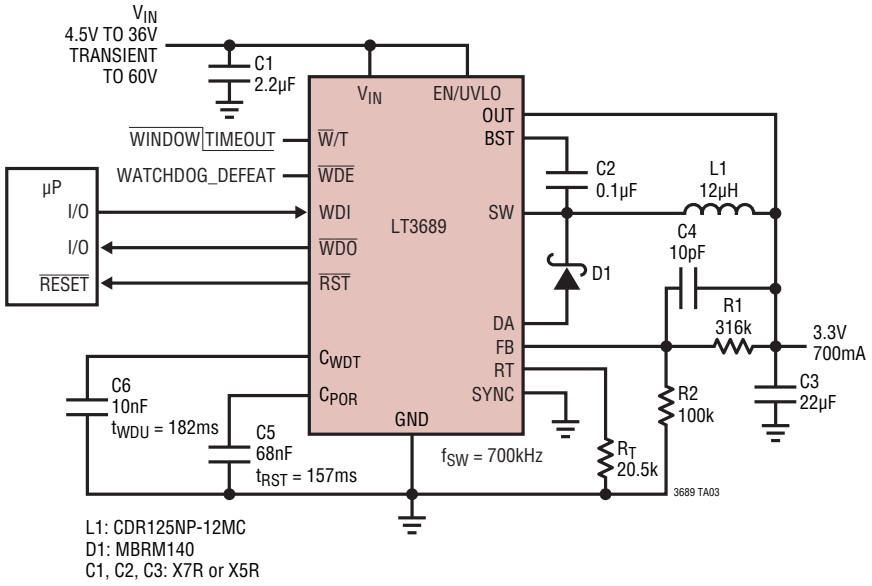
TYPICAL APPLICATIONS

5V Step-Down Converter

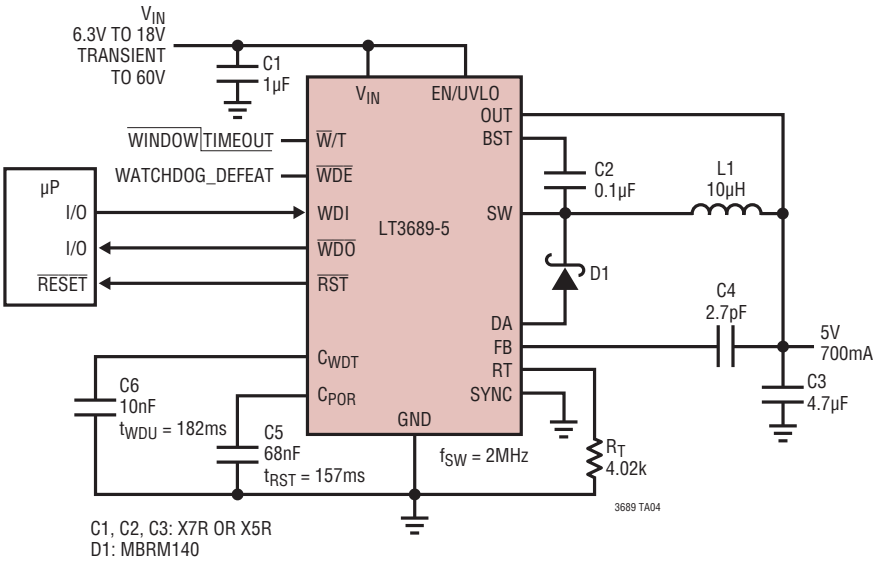


TYPICAL APPLICATIONS

3.3V Step-Down Converter

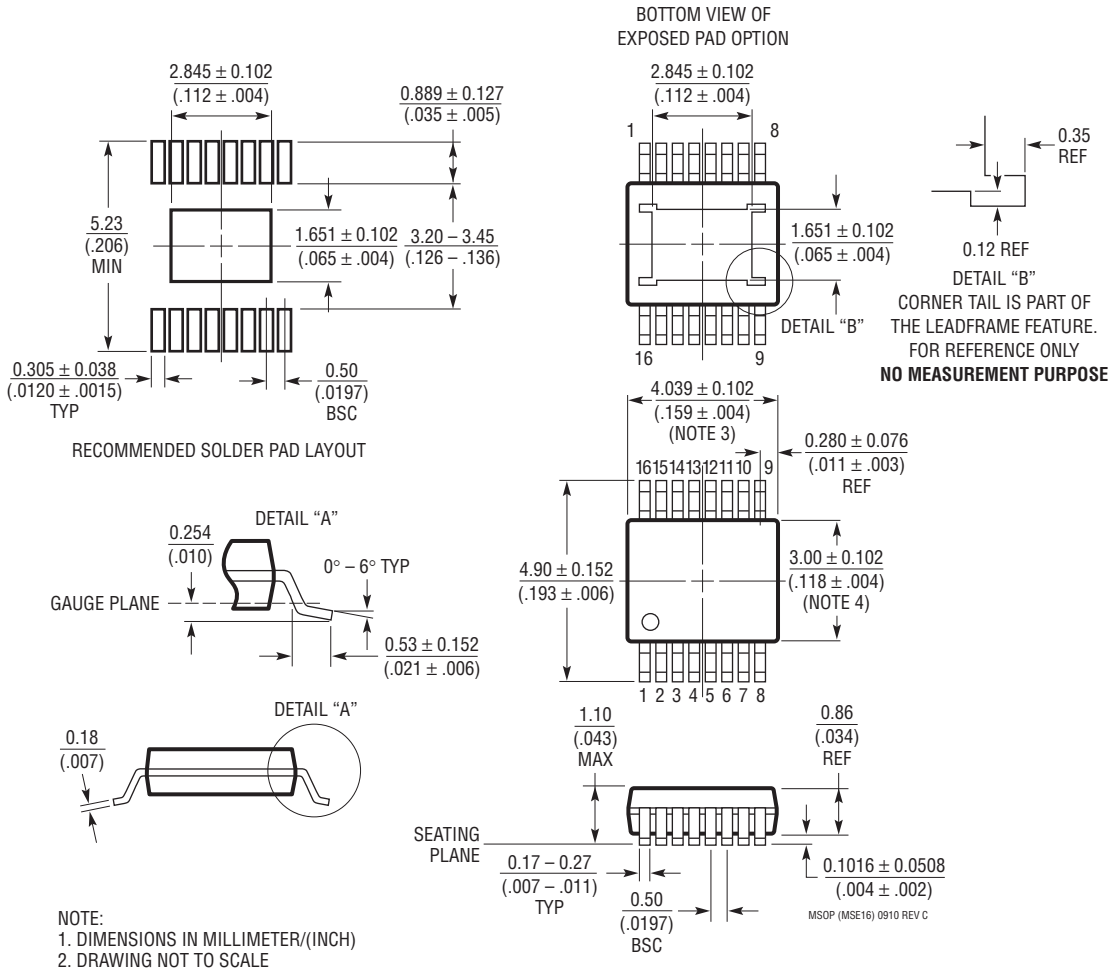


5V, 2MHz Step-Down Converter



PACKAGE DESCRIPTION

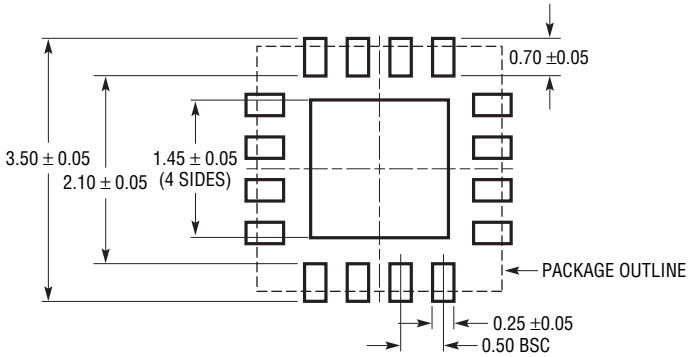
MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev C)



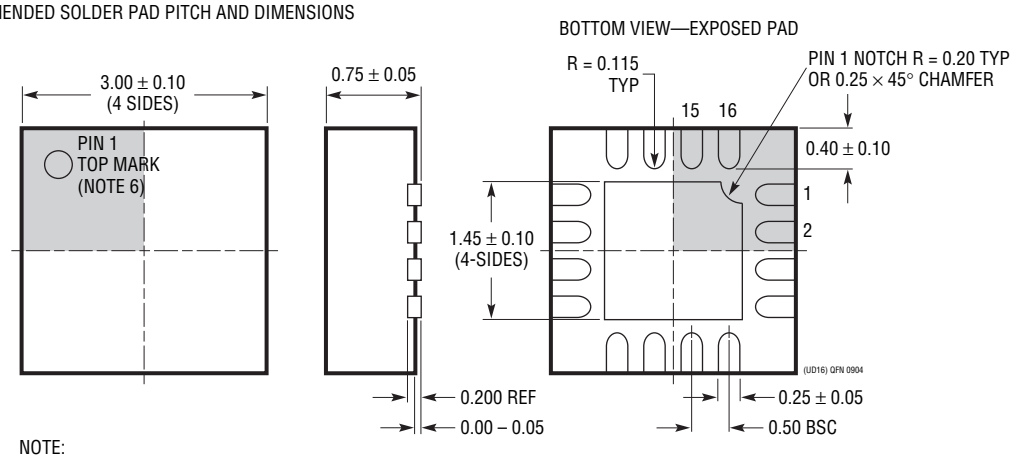
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



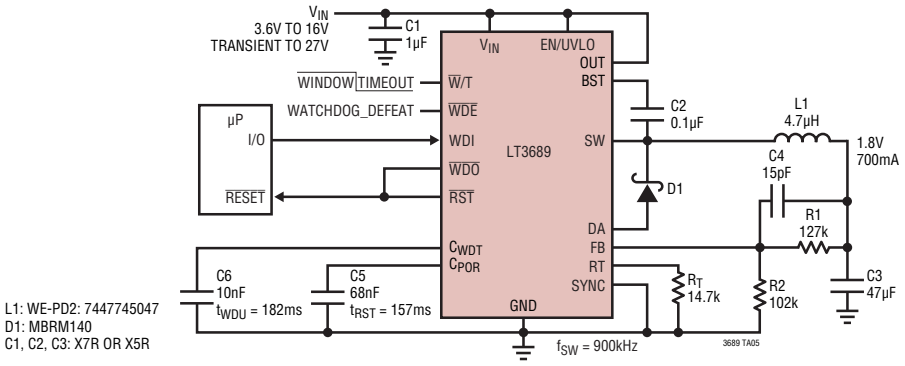
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/10	Added LT3689-5 Fixed Output Voltage Option	1–32
B	9/10	Revised conditions for $t_{SW(OFF)}$ and V_{OL} in Electrical Characteristics section.	3
C	10/10	Removed connection from OUT to GND in 5V, 2MHz Step-Down Converter drawing in Typical Applications section.	28
D	2/11	Replaced Figure 12 in the Applications Information section.	24
E	3/13	Clarified Switching Frequency limits, Foldback Resistor values Clarified Watchdog Timing graphs	3 25-28

TYPICAL APPLICATION

1.8V Step-Down Converter with System Reset Generated by Watchdog Timing or Output Voltage Failure



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1766	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} = 25µA, TSSOP-16 and TSSOP-16E Packages
LT1936	36V, 1.4A (I_{OUT}), 500kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 1.9mA, I_{SD} <1µA, MS8E Package
LT1976/LT1977	60V, 1.2A (I_{OUT}), 200kHz/500kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 100µA, I_{SD} <1µA, TSSOP-16E Package
LT3434/LT3435	60V, 2.4A (I_{OUT}), 200kHz/500kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 100mA, I_{SD} <1µA, TSSOP-16E Package
LT3437	60V, 400mA (I_{OUT}), Micropower Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 100µA, I_{SD} <1µA, 3mm × 3mm DFN-10 and TSSOP-16E Packages
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.6V to 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} <1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3481	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.6V to 34V, $V_{OUT(MIN)}$ = 1.26V, I_Q = 50mA, I_{SD} <1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3493	36V, 1.4A (I_{OUT}), 750kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.9mA, I_{SD} <1µA, 2mm × 3mm DFN-6 Package
LT3500	36V, 40V_{MAX}, 2A, 2.5MHz High Efficiency Step-Down DC/DC Converter and LDO Controller	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5mA, I_{SD} <10µA, 3mm × 3mm DFN-10 Package
LT3505	36V with Transient Protection to 40V, 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 34V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 2mA, I_{SD} = 2µA, 3mm × 3mm DFN-8 and MSOP-8E Packages
LT3507	36V 2.5MHz, Triple (2.4A + 1.5A + 1.5A (I_{OUT})) with LDO Controller High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5mA, I_{SD} = 10µA, TSSOP-16 and TSSOP-16E Packages
LT3508	36V with Transient Protection to 40V, Dual 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.7V to 37V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 4.6mA, I_{SD} = 1µA, 4mm × 4mm QFN-24 and TSSOP-16E Packages
LT3682	36V, 60V_{MAX}, 1A, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75mA, I_{SD} <1µA, 3mm × 3mm DFN-12 Package
LT3684	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 34V, $V_{OUT(MIN)}$ = 1.26V, I_Q = 850µA, I_{SD} <1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3685	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} <1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages

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