THE DATASHEET OF

DS80PCI102SQE/NOPB

www.win-source.net 0086-755-83957316

DS80PCI102 2.5-Gbps / 5.0-Gbps / 8.0-Gbps 1-Lane PCI-Express™ Repeater With Equalization and De-Emphasis

1 Features

- Comprehensive Family, Proven System Interoperability
  - **DS80PCI102:** x1 PCIe Gen-1, Gen-2, and Gen-3
  - DS80PCI402: x4 PCIe Gen-1, Gen-2, and Gen-3
  - DS80PCI800: x8/x16 PCIe Gen-1, Gen-2, and Gen-3
- Automatic Rate-Detect and Adaptation to Gen-1, Gen-2, and Gen-3 Speeds
- Seamless Support for Gen-3 Transmit FIR Handshake
- Receiver EQ (up to 36 dB), Transmit De-Emphasis (up to -12 dB)
- Adjustable Transmit VOD: 0.7 to 1.3 Vp-p (Pin Mode)
- 0.2 UI of Residual Deterministic Jitter at 8 Gbps After 40 Inches of FR4 or 10 m 30-awg PCIe Cable
- Low Power Dissipation With Ability to Turn Off Unused Channels: 65 mW/Channel
- Automatic Receiver Detect (Hot-Plug)
- Multiple Configuration Modes: Pins/SMBus/Direct-EEPROM Load
- Flow-Thru Pinout in 4-mm × 4-mm 24-Pin Leadless WQFN Package
- Single Supply Voltage: 2.5 V or 3.3 V (Selectable)
- ±5-kV HBM ESD Rating
- −40°C to 85°C Operating Temperature Range

2 Applications

PCI Express Gen-1, Gen-2, and Gen-3

3 Description

The DS80PCI102 is a low-power, 1-lane repeater with 4-stage input equalization, and an output de-emphasis driver to enhance the reach of PCI-Express serial links in board-to-board or cable interconnects. The device is ideal for x1 PCI-Express configuration, and it automatically detects and adapts to Gen-1, Gen-2, and Gen-3 data rates for easy system upgrade.

DS80PCI102 offers programmable transmit de-emphasis (up to 12 dB), transmit VOD (up to 1300 mVp-p), and receive equalization (up to 36 dB) to enable longer distance transmission in lossy copper cables (10 meters or more), or backplanes (40 inches or more) with multiple connectors. The receiver can open an input eye that is completely closed due to inter-symbol interference (ISI) introduced by the interconnect medium.

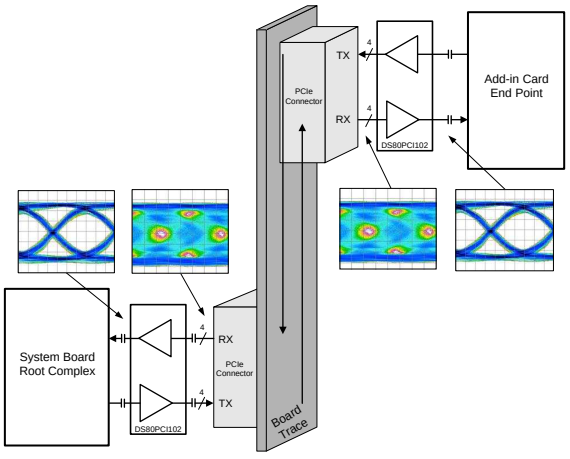
The programmable settings can be applied easily through pins or software (SMBus/I^{2}C), or can be loaded through an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up, which eliminates the need for an external microprocessor or software driver.

Device Information(1)

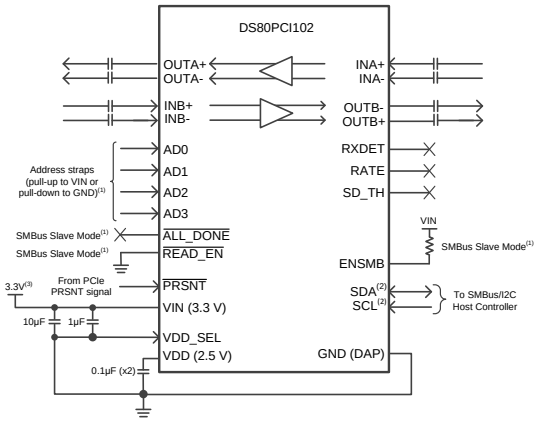
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS80PCI102	WQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Block Diagram



Simplified Schematic Diagram



(1) Schematic shows connection for SMBus Slave Mode (ENSMB=1kΩ to VDD)
For SMBus Master Mode or Pin Mode configuration, the connections are different.
(2) SMBus signals need to be pulled up elsewhere in the system.
(3) Schematic requires different connections for 2.5 V mode.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision F (October 2014) to Revision G — **Page**

- Changed pin mapping for VIN and VDD to correct typo ... 5
- Added full SMBus-to-EEPROM table mapping ... 20
- Changed description of EEPROM bits to match corresponding SMBus register map description ... 20
- Changed location of CHB VOD in Table 7 to match correct location in EEPROM map ... 23
- Changed address start and end numbers for Devices 0-3 to reflect correct bytes per device ... 25
- Changed EEPROM bit description to match the description in the corresponding SMBus register map ... 25
- Changed location of CHA VOD in Table 9 to match correct location in EEPROM map ... 27
- Added information in Register Map about register bits saved to EEPROM ... 29

Changes from Revision E (February 2013) to Revision F — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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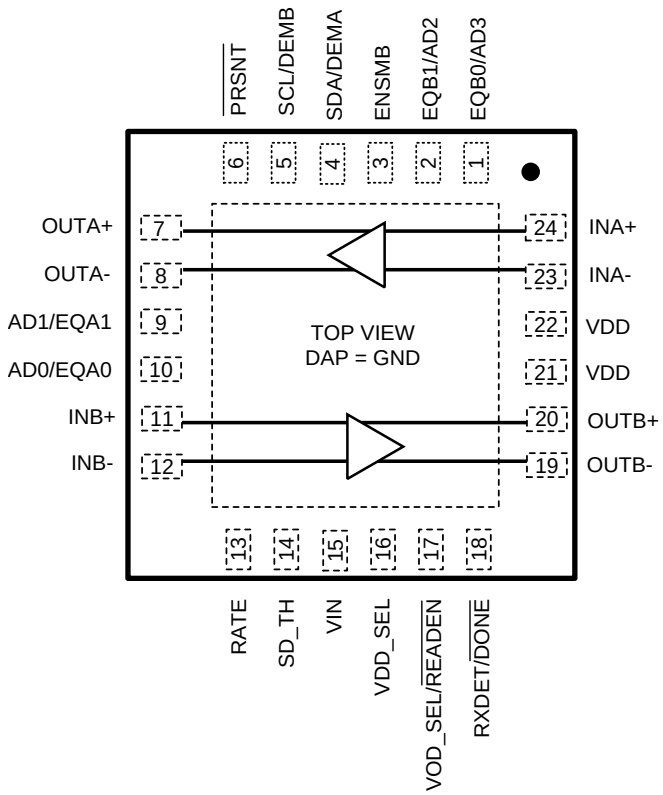
5 Pin Configuration and Functions

RTW Package
24 Pins
Top View



Pin Functions (1) (2) (3) (4)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
DIFFERENTIAL HIGH SPEED I/O'S			
INA+, INA-, INB+, INB-	24, 23 11, 12	I, CML	Inverting and noninverting differential inputs to the equalizer. A gated on-chip 50-Ω termination resistor connects INn+ to VDD and INn- to VDD depending on the state of RXDET. See Table 4 AC coupling required on high-speed I/O
OUTA+, OUTA-, OUTB+, OUTB-	7, 8 20, 19	O, CML	Inverting and noninverting 50-Ω driver outputs with de-emphasis. Compatible with AC-coupled CML inputs.
CONTROL PINS — SHARED (LVCMOS)			
ENSMB	3	I, 4-LEVEL, LVCMOS	System management bus (SMBus) enable pin Tie 1 kΩ to VDD (2.5-V mode) or VIN (3.3-V mode) = Register access SMBus slave mode FLOAT = Read external EEPROM (master SMBUS mode) Tie 1 kΩ to GND = Pin mode

(1) LVCMOS inputs without the “FLOAT” conditions must be driven to a logic low or high at all times or operation is not verified.
(2) Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10% to 90%.
(3) For 3.3-V mode operation, VIN pin = 3.3 V and the VDD for the 4-level input is 3.3 V.
(4) For 2.5-V mode operation, VDD pin = 2.5 V and the VDD for the 4-level input is 2.5 V.

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Pin Functions[1][2][3][4] (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
ENSMB = 1 (SMBus SLAVE MODE)			
SCL	5	I, 2-LEVEL, LVCMOS, O, open drain	In SMBus Slave Mode, this pin is the SMBus clock I/O. Clock input or open drain output. External 2-kΩ to 5-kΩ pullup resistor to VDD or VIN recommended as per SMBus interface standards.[5]
SDA	4	I, 2-LEVEL, LVCMOS, O, open drain	In both SMBus Modes, this pin is the SMBus data I/O. Data input or open drain output. External 2-kΩ to 5-kΩ pullup resistor to VDD or VIN recommended as per SMBus interface standards.[5]
AD0-AD3	10, 9, 2, 1	I, 4-LEVEL, LVCMOS	SMBus Slave Address Inputs. In both SMBus Modes, these pins are the user set SMBus slave address inputs. External 1-kΩ pullup or pulldown recommended.
$\overline{\text{READEN}}$	17	I, 2-LEVEL, LVCMOS	When in SMBus Slave Mode the $\overline{\text{READEN}}$ pin must be tied LOW for the AD[3:0] to be active. If this pin is tied HIGH or FLOAT, the device slave address is 0xB0.
ENSMB = FLOAT (SMBus MASTER MODE)			
SCL	5	I, 2-LEVEL, LVCMOS, O, open drain	Clock output when loading EEPROM configuration, reverting to SMBus clock input when EEPROM load is complete ($\overline{\text{DONE}}$ = 0). External 2-kΩ to 5-kΩ pullup resistor to VDD or VIN recommended as per SMBus interface standards.[5]
SDA	4	I, 2-LEVEL, LVCMOS, O, open drain	In both SMBus Modes, this pin is the SMBus data I/O. Data input or open drain output. External 2-kΩ to 5-kΩ pullup resistor to VDD or VIN recommended as per SMBus interface standards.[5]
AD0-AD3	10, 9, 2, 1	I, 4-LEVEL, LVCMOS	SMBus Slave Address Inputs. In both SMBus Modes, these pins are the user set SMBus slave address inputs. External 1-kΩ pullup or pulldown recommended.
$\overline{\text{READEN}}$	17	I, 2-LEVEL, LVCMOS	A logic low on this pin starts the load from the external EEPROM.[6] Once EEPROM load is complete ($\overline{\text{DONE}}$ = 0), this pin functionality remains as $\overline{\text{READEN}}$. It does not revert to an SD_TH input.
$\overline{\text{DONE}}$	18	O, 2-LEVEL, LVCMOS	Valid register load status output HIGH = External EEPROM load failed or incomplete LOW = External EEPROM load passed
ENSMB = 0 (PIN MODE)			
EQA0, EQA1 EQB0, EQB1	10, 9 1, 2	I, 4-LEVEL, LVCMOS	EQA[1:0] and EQB[1:0] control the level of equalization on the input pins. The pins are active only when ENSMB is deasserted (LOW). When ENSMB goes high the SMBus registers provide independent control of each lane, and the EQA[1:0] and EQB[1:0] pins are converted to SMBUS AD[3:0] inputs. See Table 2.
DEMA, DEMB	4, 5	I, 4-LEVEL, LVCMOS	DEMA DEMB controls the level of de-emphasis. The DEMA/B pins are only active when ENSMB is deasserted (LOW). DEMA controls the A channel and DEMB controls the B channel. When ENSMB goes high the SMBus registers provide independent control of each channel and the DEM pins are converted to SMBUS SDA and SCL pins. See Table 3.
CONTROL PINS — BOTH PIN AND SMBUS MODES (LVCMOS)			
$\overline{\text{PRSNT}}$	6	I, 2-LEVEL, LVCMOS	Cable Present Detect input. High when a cable is not present per PCIe Cabling Spec. 1.0. Puts part into low power mode. When LOW (normal operation) part is enabled. See Table 4.
VOD_SEL	17	I, 4-LEVEL, LVCMOS	VOD Select pin. See Table 3.
VDD_SEL	16	I, LVCMOS	Controls the internal regulator. FLOAT = 2.5-V mode Tie GND = 3.3-V mode See Figure 16.
RXDET	18	I, 4-LEVEL, LVCMOS	The RXDET pin controls the receiver detect function. Depending on the input level, a 50-Ω or > 50-kΩ termination to the power rail is enabled. See Table 4.

(5) SCL and SDA pins can be tied either to 3.3 V or 2.5 V, regardless of whether the device is operating in 2.5-V mode or 3.3-V mode.
(6) When $\overline{\text{READEN}}$ is asserted low, the device attempts to load EEPROM. If EEPROM cannot be loaded successfully, for example due to an invalid or blank hex file, the DS80PCI102 waits indefinitely in an unknown state where SMBus access is not possible. $\overline{\text{DONE}}$ pin remains high in this situation.

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Pin Functions[(1)(2)(3)(4)] (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
RATE	13	I, 4-LEVEL, LVCMOS	RATE control pin selects GEN 1,2 and GEN 3 operating modes. Tie 1 kΩ to GND = GEN 1,2 FLOAT = AUTO Rate Select of Gen1/2 and Gen3 with de-emphasis Tie 20 kΩ to GND = GEN 3 without de-emphasis Tied 1 kΩ to VDD = RESERVED
SD_TH	14	I, 4-LEVEL, LVCMOS	Controls the internal Signal Detect Threshold. See Table 5.
POWER			
VIN	15	Power	In 3.3-V mode, feed 3.3 V to VIN In 2.5-V mode, leave floating
VDD	21, 22	Power	Power supply pins 2.5-V mode, connect to 2.5-V supply 3.3-V mode, connect 0.1-µF capacitor to each VDD pin (output of LDO)
GND	DAP	Power	Ground pad (DAP - die attach pad).

6 Specifications

6.1 Absolute Maximum Ratings [(1)(2)]

	MIN	MAX	UNIT
Supply voltage (VDD - 2.5 V)	–0.5	2.75	V
Supply voltage (VIN - 3.3 V)	–0.5	4.0	V
LVCMOS Input/Output Voltage	–0.5	4.0	V
CML Input Voltage	–0.5	VDD + 0.5	V
CML Input Current	–30	30	mA
Junction Temperature		125	°C
Lead temperature soldering (4 s)[(3)]		260	°C
Storage temperature, T_{stg}	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute Maximum Numbers are specified for a junction temperature range of –40° C to 125° C. Models are validated to Maximum Operating Voltages only.
(3) For soldering specifications: See application note SNOA549.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±5000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±1250	
	MM, STD - JESD22-A115-A	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage (2.5-V mode)	2.375	2.5	2.625	V
Supply Voltage (3.3-V mode)	3.0	3.3	3.6	V
Ambient Temperature	-40	25	85	°C
SMBus (SDA, SCL)			3.6	V

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6.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
IDD	Supply Current	VIN = 3.3-V supply, EQ = Enabled, RXDET = 1, VOD = 1.0 Vp-p, $\overline{\text{PRSNT}}$ = LOW		50	63	mA
		VIN = 3.3-V supply, $\overline{\text{PRSNT}}$ = HIGH		9	12	mA
		VDD = 2.5 V, $\overline{\text{PRSNT}}$ = HIGH		6	9	mA
LVCMOS / LVTTL DC SPECIFICATIONS						
V_{IH25}	High-level input voltage ($\overline{\text{READ_EN}}$ pin)	2.5-V Mode	2.0		VDD	V
V_{IH33}	High-level input voltage ($\overline{\text{READ_EN}}$ pin)	3.3-V Mode	2.0		VIN	V
V_{IH}	High Level Input Voltage ($\overline{\text{PRSNT}}$ pin)	2.5-V Mode	0.9 × VDD		VDD	V
		3.3-V Mode	0.9 × VIN		VIN	
V_{IL}	Low Level Input Voltage		0		0.7	V
V_{OH}	High Level Output Voltage ($\overline{\text{DONE}}$ pin)	I_{OH} = −4 mA	2.0			V
V_{OL}	Low Level Output Voltage ($\overline{\text{DONE}}$ pin)	I_{OL} = 4 mA			0.4	V
I_{IH}	Input High Current ($\overline{\text{PRSNT}}$ pin)	VIN Supply = 3.6 V, Input = 3.6 V	–15		15	µA
	Input High Current with internal resistors (4–level input pin)		+20		80	µA
I_{IL}	Input Low Current ($\overline{\text{PRSNT}}$ pin)	VIN = 3.6 V, Input = 0 V	–15		15	µA
	Input Low Current with internal resistors (4–level input pin)		–160		-40	µA
CML RECEIVER INPUTS (IN_N+, IN_N-)						
$RL_{RX-DIFF}$	RX Differential return loss	0.05 to 1.25 GHz		–16		dB
		1.25 to 2.5 GHz		–16		dB
		2.5 to 4.0 GHz		–14		dB
RL_{RX-CM}	RX Common mode return loss	0.05 to 2.5 GHz		–12		dB
		2.5 to 4.0 GHz		–8		dB
Z_{RX-DC}	RX DC single-ended impedance	VDD = 2.5 V	40	50	60	Ω
$Z_{RX-DIFF-DC}$	RX DC differential mode impedance	VDD = 2.5 V	80	100	120	Ω
$V_{RX-DIFF-DC}$	VID - Differential RX peak to peak input voltage				1.2	V
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input common mode impedance for V > 0	VID = 0 to 200 mV, ENSMB = 0, RXDET = 0, VDD = 2.5 V		50		kΩ
$V_{RX-SIGNAL-DET-DIFF-PP}$	Signal detect assert level for active data signal	SD_TH = Float, 0101 pattern at 8 Gbps Measured at pins		180		mVp-p
$V_{RX-IDLE-DET-DIFF-PP}$	Signal detect deassert level for electrical idle	SD_TH = Float, 0101 pattern at 8 Gbps Measured at pins		110		mVp-p

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Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH SPEED OUTPUTS						
$V_{TX-DIFF-PP}$	Output voltage differential swing	Differential measurement with OUT_n+ and OUT_n-, terminated by 50 Ω to GND, AC-Coupled, VID = 1.0 Vp-p, DEMA/B = 0, VOD_SEL = Float, (1)	0.8	1.0	1.1	Vp-p
$V_{TX-DE-RATIO_3.5}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEMA/B = Float, VOD_SEL = Float, (GEN 1, 2 only)		–3.5		dB
$V_{TX-DE-RATIO_6}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEMA/B = 20 kΩ to GND, VOD_SEL = Float, (GEN 1, 2 only)		–6		dB
T_{TX-RJ}	Random Ritter	VID = 800 mV, 0101 pattern, 8.0 Gbps, VOD = 1.0 V, EQ = 0x00, DE = 0 dB		0.3		ps RMS
T_{TX-DJ}	Deterministic Jitter	VID = 800 mV, PRBS15, 8.0 Gbps VOD = 1.0 V, EQ = 0x00, DE = 0 dB		0.05		UIpp
$T_{TX-RISE-FALL}$	TX rise/fall time	20% to 80% of differential output voltage, (2)	34	45		ps
$T_{RF-MISMATCH}$	TX rise/fall mismatch	20% to 80% of differential output voltage, (2)		0.01		UI
$RL_{TX-DIFF}$	TX Differential return loss	0.05 to 1.25 GHz		–16		dB
		1.25 to 2.5 GHz		–12		dB
		2.5 to 4 GHz		–11		dB
RL_{TX-CM}	TX Common mode return loss	0.05 to 2.5 GHz		–12		dB
		2.5 to 4 GHz		–8		dB
$Z_{TX-DIFF-DC}$	DC differential TX impedance			100		Ω
$V_{TX-CM-AC-PP}$	TX AC common mode voltage	VOD = 1.0 Vp-p, DEMA/B = 0, VOD_SEL = Float, (2)			100	mVp-p
$I_{TX-SHORT}$	TX short circuit current limit	Total current the transmitter can supply when shorted to VDD or GND		20		mA
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	(2)			100	mV
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode voltgae between TX+ and TX-	(2)			25	mV
$T_{TX-IDLE-DATA}$	Max time to transition to differential DATA signal after IDLE	VID = 1.0 Vp-p, 8 Gbps		3.5		ns
$T_{TX-DATA-IDLE}$	Max time to transition to IDLE after differential DATA signal	VID = 1.0 Vp-p, 8 Gbps		6.5		ns
$T_{PLHD/PHLD}$	High-to-Low and Low-to-High Differential Propagation Delay	DE = 0, EQ = 0x00, (3)		200		ps
T_{LSK}	Lane-to-lane skew	T = 25ºC, VDD = 2.5 V		25		ps
T_{PPSK}	Part-to-part propagation delay skew	T = 25ºC, VDD = 2.5 V		40		ps

(1) In GEN3 mode, the output VOD level is not fixed. It will be adjusted automatically based on the VID input amplitude level. The output VOD level set by DEMA/B[1:0] in GEN3 mode is dependent on the VID level and the frequency content. The DS80PCI102 repeater in GEN3 mode is designed to be transparent, so the TX-FIR (de-emphasis) is passed to the RX to support the PCIe GEN3 handshake negotiation link training.
(2) Parameter is characterized but not tested in production.
(3) Propagation Delay measurements will change slightly based on the level of EQ selected. EQ = 0x00 will result in the shortest propagation delays.

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Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EQUALIZATION						
DJE1	Residual deterministic jitter at 8 Gbps	35” 4mils FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 0x1F,** DEM = 0 dB		0.14		UIpp
DJE2	Residual deterministic jitter at 5 Gbps	35” 4mils FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 0x1F,** DEM = 0 dB		0.1		UIpp
DJE3	Residual deterministic jitter at 2.5 Gbps	35” 4mils FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 0x1F,** DEM = 0 dB		0.05		UIpp
DJE4	Residual deterministic jitter at 8 Gbps	10 meters 30-awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 0x2F,** DEM = 0 dB		0.16		UIpp
DJE5	Residual deterministic jitter at 5 Gbps	10 meters 30-awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 0x2F,** DEM = 0 dB		0.1		UIpp
DJE6	Residual deterministic jitter at 2.5 Gbps	10 meters 30-awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 0x2F,** DEM = 0 dB		0.05		UIpp
DE-EMPHASIS (GEN 1&2 MODE ONLY)						
DJD1	Residual deterministic jitter at 2.5 Gbps and 5.0 Gbps	10” 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 0x00, VOD = 1.0 Vp-p, **DEM = −3.5 dB**		0.1		UIpp
DJD2	Residual deterministic jitter at 2.5 Gbps and 5.0 Gbps	20” 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 0x00, VOD = 1.0 Vp-p, **DEM = −9 dB**		0.1		UIpp

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6.5 Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pullup Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	(1)	-200		200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SCL	(1) (2)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5 V ± 5% OR 3.3 V ± 10%	Pullup V_{DD} = 3.3 V (1) (2) (3)		2000		Ω
		Pullup V_{DD} = 2.5 V (1) (2) (3)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS						
FSMB	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = FLOAT (Master Mode)	280	400	520	kHz
T_{BUF}	Bus Free Time Between Stop and Start Condition		1.3			µs
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	0.6			µs
$T_{SU:STA}$	Repeated Start Condition Setup Time		0.6			µs
$T_{SU:STO}$	Stop Condition Setup Time		0.6			µs
$T_{HD:DAT}$	Data Hold Time		0			ns
$T_{SU:DAT}$	Data Setup Time		100			ns
T_{LOW}	Clock Low Period		1.3			µs
T_{HIGH}	Clock High Period	(4)	0.6		50	µs
t_F	Clock/Data Fall Time	(4)			300	ns
t_R	Clock/Data Rise Time	(4)			300	ns
t_{POR}	Time in which a device must be operational after power-on reset	(4) (5)			500	ms

(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400 pF.
(3) Maximum termination voltage should be identical to the device supply voltage.
(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.
(5) Specified by Design. Parameter not tested in production.

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6.6 Timing Diagrams

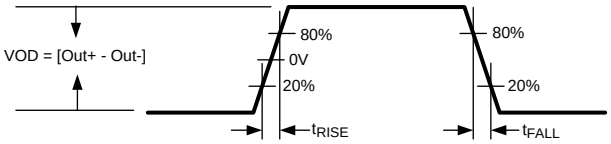

Figure 1. CML Output and Rise and Fall Times

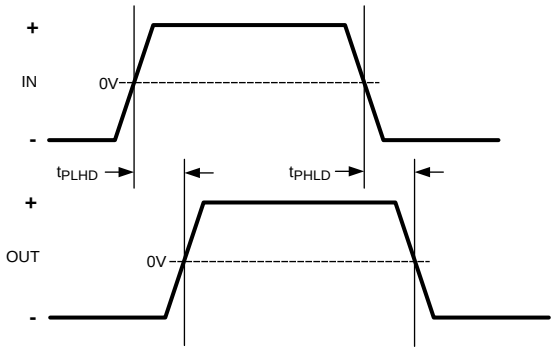

Figure 2. Propagation Delay Timing Diagram

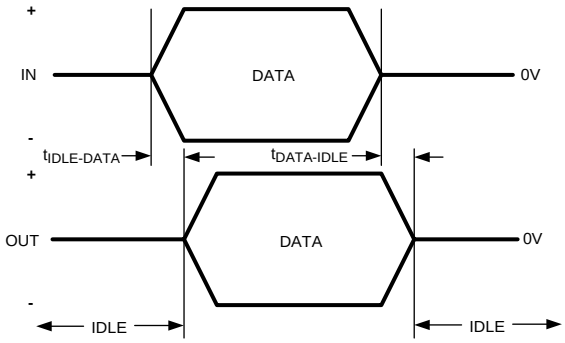

Figure 3. Transmit IDLE-DATA and DATA-IDLE Response Time

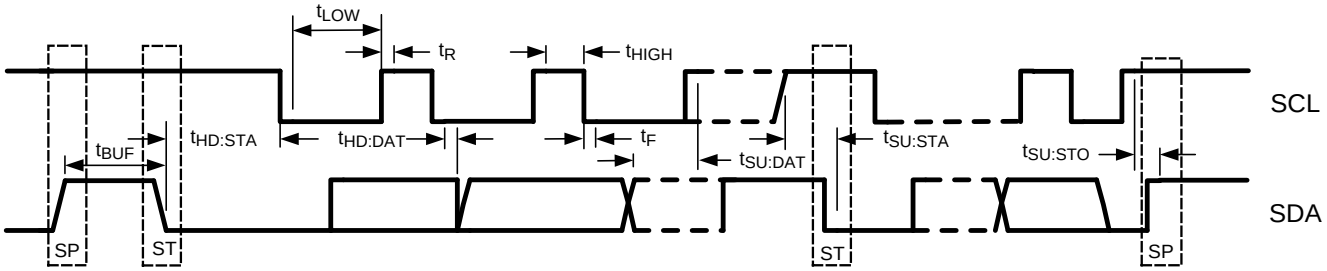

Figure 4. SMBus Timing Parameters

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6.7 Typical Characteristics

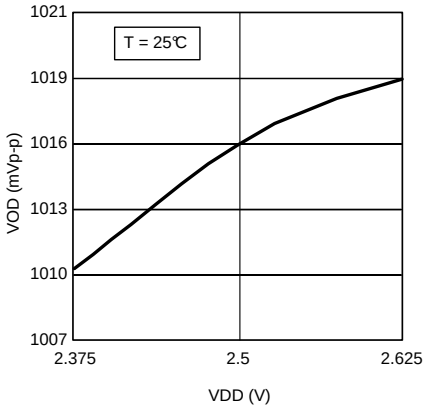


Figure 5. Output Differential Voltage (VOD = 1.0 Vp-p) vs Supply Voltage (VDD)

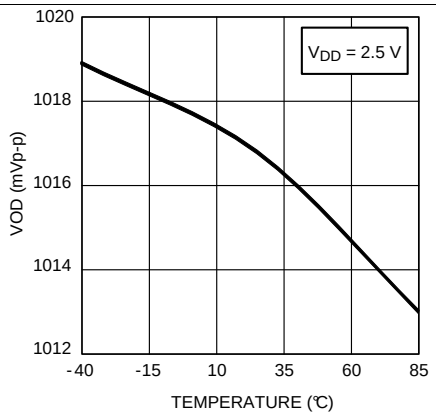


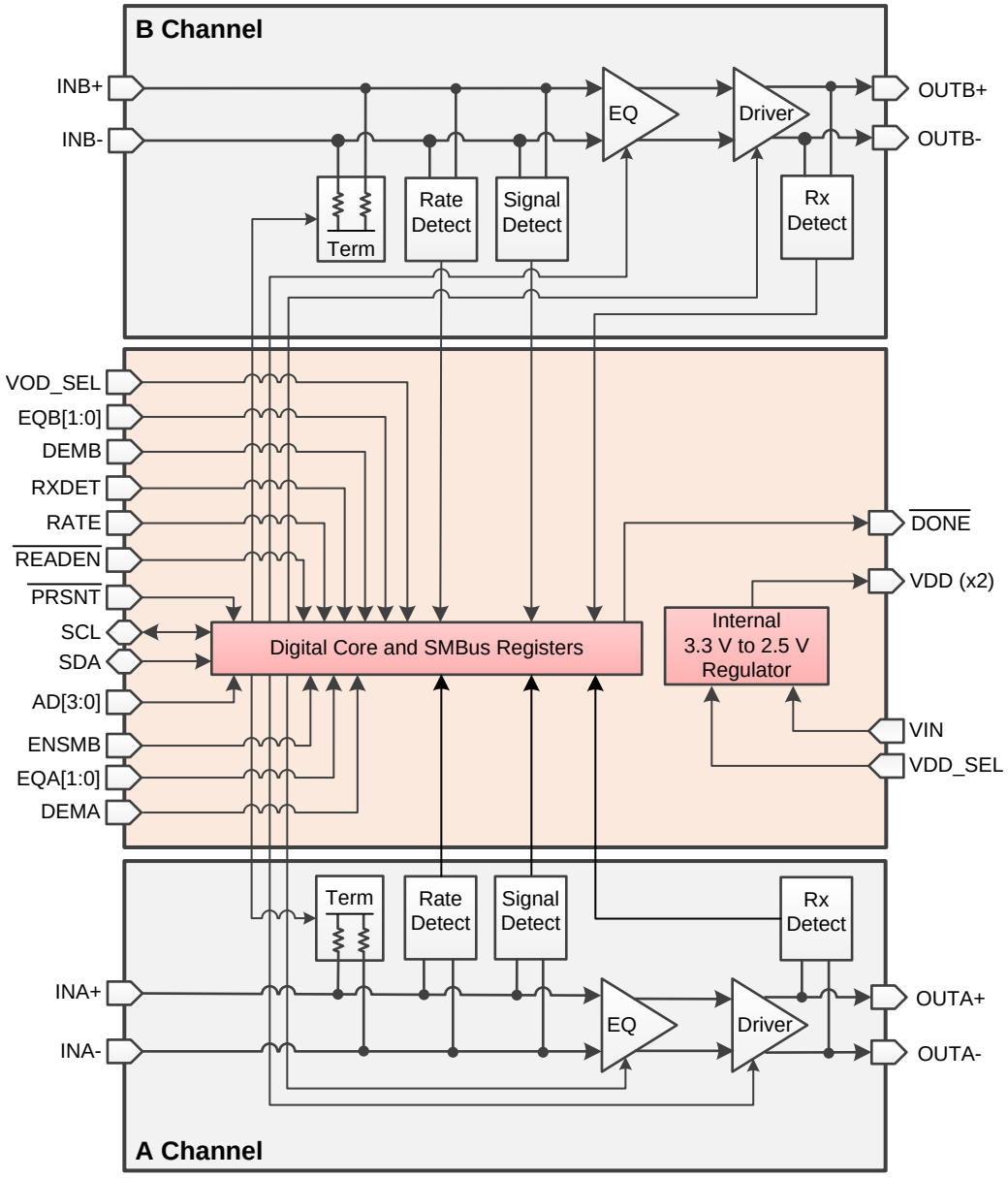
Figure 6. Output Differential Voltage (VOD = 1.0 Vp-p) vs Temperature

7 Detailed Description

7.1 Overview

The DS80PCI102 provides input CTLE and output De-emphasis equalization for lossy printed circuit board trace and cables. The DS80PCI102 operates in three modes: Pin Control Mode configuration (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) for register configurations from host controller or SMBus Master Mode (ENSMB = Float) for loading the register configurations from an external EEPROM.

7.2 Functional Block Diagram



Note: This diagram is representative of device signal flow only; Channels A and B are bi-directional channels.

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7.3 Feature Description

7.3.1 4-Level Input Configuration Guidelines

The 4-level input pins use a resistor divider to help set the four valid levels. There is an internal 30-kΩ pullup and a 60-kΩ pulldown connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1-kΩ pullup, 1-kΩ pulldown, no connect, or 20-kΩ pulldown provide the optimal voltage levels for each of the four input states.

Table 1. 4-Level Input Voltage

LEVEL	SETTING	3.3-V MODE	2.5-V MODE
0	1 kΩ to GND	0.1 V	0.08 V
R	20 kΩ to GND	0.33 × V_{IN}	0.33 × V_{DD}
F	FLOAT	0.67 × V_{IN}	0.67 × V_{DD}
1	1 kΩ to V_{DD}/V_{IN}	V_{IN} – 0.05 V	V_{DD} – 0.04 V

Typical 4-level input thresholds:

- Level 1 to 2 = 0.2 V_{IN} or V_{DD}
- Level 2 to 3 = 0.5 V_{IN} or V_{DD}
- Level 3 to 4 = 0.8 V_{IN} or V_{DD}

To minimize the start-up current associated with the integrated 2.5-V regulator, the 1-kΩ pullup and pulldown resistors are recommended. If several 4-level inputs require the same setting, it is possible to combine two or more 1-kΩ resistors into a single lower value resistor. As an example; combining two inputs with a single 500-Ω resistor is a good way to save board space. For the 20 kΩ to GND, this should also scale to 10 kΩ.

Table 2. Equalizer Settings(1)

LEVEL	EQA1 EQB1	EQA0 EQB0	EQ – 8 BITS [7:0]	dB at 1.25 GHz	dB at 2.5 GHz	dB at 4 GHz	SUGGESTED USE
1	0	0	0000 0000 = 0x00	2.1	3.7	4.9	FR4 < 5 inch trace
2	0	R	0000 0001 = 0x01	3.4	5.8	7.9	FR4 5 inch 5–mil trace
3	0	Float	0000 0010 = 0x02	4.8	7.7	9.9	FR4 5 inch 4–mil trace
4	0	1	0000 0011 = 0x03	5.9	8.9	11.0	FR4 10 inch 5–mil trace
5	R	0	0000 0111 = 0x07	7.2	11.2	14.3	FR4 10 inch 4–mil trace
6	R	R	0001 0101 = 0x15	6.1	11.4	14.6	FR4 15 inch 4–mil trace
7	R	Float	0000 1011 = 0x0B	8.8	13.5	17.0	FR4 20 inch 4–mil trace
8	R	1	0000 1111 = 0x0F	10.2	15.0	18.5	FR4 25 to 30 inch 4–mil trace
9	Float	0	0101 0101 = 0x55	7.5	12.8	18.0	FR4 30 inch 4–mil trace
10	Float	R	0001 1111 = 0x1F	11.4	17.4	22.0	FR4 35 inch 4–mil trace
11	Float	Float	0010 1111 = 0x2F	13.0	19.7	24.4	10 m, 30-awg cable
12	Float	1	0011 1111 = 0x3F	14.2	21.1	25.8	10 m – 12 m cable
13	1	0	1010 1010 = 0xAA	13.8	21.7	27.4	
14	1	R	0111 1111 = 0x7F	15.6	23.5	29.0	
15	1	Float	1011 1111 = 0xBF	17.2	25.8	31.4	
16	1	1	1111 1111 = 0xFF	18.4	27.3	32.7	

(1) The suggested equalizer CTLE settings are based on 0 dB of TX preshoot/de-emphasis. In PCIe Gen 3 applications which use TX preshoot/de-emphasis, the CTLE should be set to a lower boost setting to optimize the RX eye opening.

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Table 3. Output Voltage and De-Emphasis Settings

LEVEL	VOD_SEL	DEMA DEMB	VOD (Vp-p)	DEM (dB)(1)	SUGGESTED USE
1	0	0	0.7	0	FR4 < 5 inch 4–mil trace
2	0	R	0.7	- 6	FR4 12 inch 4–mil trace
3	0	Float	0.7	- 3.5	FR4 10 inch 4–mil trace
4	0	1	0.7	- 9	FR4 15 inch 4–mil trace
5	R	0	1.2	0	FR4 < 5 inch 4–mil trace
6	R	R	1.2	- 6	FR4 12 inch 4–mil trace
7	R	Float	1.2	- 3.5	FR4 10 inch 4–mil trace
8	R	1	1.2	- 9	FR4 15 inch 4–mil trace
9	Float	0	1.0	0	FR4 < 5 inch 4–mil trace
10	Float	R	1.0	- 6	FR4 15 inch 4–mil trace
11	Float	Float	1.0	- 3.5	FR4 10 inch 4–mil trace
12	Float	1	1.0	- 9	FR4 20 inch 4–mil trace
13	1	0	1.1	0	FR4 < 5 inch 4–mil trace
14	1	R	1.1	- 1.5	FR4 5 inch 4–mil trace
15	1	Float	1.3	- 1.5	FR4 5 inch 4–mil trace
16	1	1	1.3	- 3.5	FR4 10 inch 4–mil trace

(1) The VOD output amplitude and DEM de-emphasis levels are set with the DEMA/B[1:0] pins. The de-emphasis levels are available in GEN1, GEN2, and GEN 3 modes when RATE = Float.

Table 4. RX-Detect Settings

$\overline{\text{PRSNT}}$(1) (PIN 52)	RXDET (PIN 22)	SMBus REG BIT[3:2]	INPUT TERMINATION	COMMENTS
0	0	00	Hi-Z	Manual RX-Detect, input is high-impedance mode
0	Tie 20 kΩ to GND	01	Pre Detect: Hi-Z Post Detect: 50 Ω	Auto RX-Detect, outputs test every 12 ms for 600 ms then stops; termination is hi-Z until detection; once detected input termination is 50 Ω Reset function by pulsing $\overline{\text{PRSNT}}$ high for 5 µs then low again
0	Float (Default)	10	Pre Detect: Hi-Z Post Detect: 50 Ω	Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω Reset function by pulsing $\overline{\text{PRSNT}}$ high for 5 µs then low again
0	1	11	50 Ω	Manual RX-Detect, input is 50 Ω
1	X		Hi-Z	Power-down mode, input is high impedance, output drivers are disabled Used to reset RX-Detect State Machine when held high for 5 µs

(1) In SMBus Slave Mode, the Rx Detect State Machine can be manually reset in software by overriding the device $\overline{\text{PRSNT}}$ function. This is accomplished by setting the Override RXDET bit (Reg 0x02[7]) and then toggling the RXDET Value bit (Reg 0x02[6]). See Table 10 for more information about resetting the Rx Detect State Machine.

Table 5. Signal Detect Threshold Level(1)

SD_TH	SMBus REG BIT [3:2] AND [1:0]	ASSERT LEVEL (TYP)	DEASSERT LEVEL (TYP)
0	10	210 mVp-p	150 mVp-p
R	01	160 mVp-p	100 mVp-p
F (default)	00	180 mVp-p	110 mVp-p
1	11	190 mVp-p	130 mVp-p

(1) VDD = 2.5 V, 25°C, and 0101 pattern at 8 Gbps.

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7.4 Device Functional Modes

The DS80PCI102 is a low power media compensation 1 lane repeater optimized for PCI Express Gen 1/2 and 3. The DS80PCI102 compensates for lossy FR-4 printed circuit board backplanes and balanced cables. The DS80PCI102 operates in 3 modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register information from external EEPROM; refer to Table 8 for additional information.

7.4.1 Pin Control Mode

When in pin mode (ENSMB = 0), equalization and de-emphasis can be selected through pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per the De- Emphasis table below. The RXDET pins provides automatic and manual control for input termination (50 Ω or > 50 kΩ). RATE setting is also pin controllable with pin selections (Gen 1/2, auto detect and Gen 3). The receiver electrical idle detect threshold is also adjustable through the SD_TH pin.

7.4.2 SMBUS Mode

When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by A or B as in the pin mode case. Upon assertion of ENSMB, the EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins (RATE, RXDET and SD_TH) remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low (pin mode). On power-up and when ENSMB is driven low all registers are reset to their default state. If PRSNT is asserted while ENSMB is high, the registers retain their current state.

Equalization settings accessible through the pin controls were chosen to meet the needs of most PCIe applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed through the SMBus registers. Each input has a total of 256 possible equalization settings. The *4-Level Input Configuration Guidelines* show the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and de-emphasis levels are set by registers.

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7.5 Programming

7.5.1 System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB = 1 kΩ to VDD to enable SMBus slave mode and allow access to the configuration registers.

The DS80PCI102 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBUS slave address inputs. The AD[3:0] pins have internal pulldown. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is 0xB0. Based on the SMBus 2.0 specification, the DS80PCI102 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). The device supports up to 16 address byte, which can be set with the AD[3:0] inputs. Below are the 16 addresses.

Table 6. Device Slave Address Bytes

AD[3:0] SETTINGS	ADDRESS BYTES (HEX)	7-BIT SLAVE ADDRESS (HEX)
0000	B0	58
0001	B2	59
0010	B4	5A
0011	B6	5B
0100	B8	5C
0101	BA	5D
0110	BC	5E
0111	BE	5F
1000	C0	60
1001	C2	61
1010	C4	62
1011	C6	63
1100	C8	64
1101	CA	65
1110	CC	66
1111	CE	67

The SDA/SCL pins are 3.3-V tolerant, but are not 5-V tolerant. An external pullup resistor is required on the SDA and SCL line. The resistor value can be from 2 kΩ to 5 kΩ depending on the voltage, loading, and speed.

7.5.2 Transfer of Data Through the SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A high-to-low transition on SDA while SCL is High indicates a message START condition.

STOP: A low-to-high transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

7.5.3 SMBus Transactions

The device supports WRITE and READ transactions. See Table 10 for register address, type (Read/Write, Read Only), default value and function information.

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7.5.4 Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a 0 indicating a WRITE.
2. The Device (Slave) drives the ACK bit (0).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (0).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (0).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

7.5.5 Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a 0 indicating a WRITE.
2. The Device (Slave) drives the ACK bit (0).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (0).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a 1 indicating a READ.
7. The Device drives an ACK bit 0.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit 1 indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

See *Table 10* for more information.

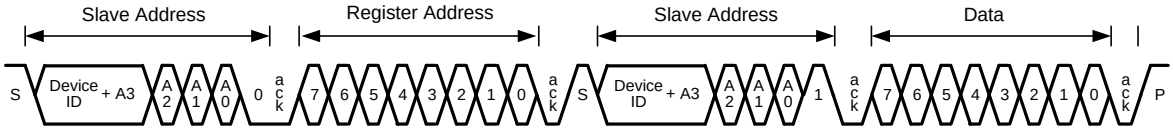

Figure 7. Typical SMBus Write Operation

7.5.6 EEPROM Programming

The DS80PCI102 supports reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS80PCI102 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the following guidelines should be followed:

- Set the DS80PCI102 into SMBus Master Mode.
  - ENSMB (PIN 3) = Float
- The external EEPROM device must support 1-MHz operation.
- The external EEPROM device address byte must be 0xA0.
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is 0xB0.
- The device address can be set with the use of the AD[3:0] input up to 16 different addresses. Use the example below to set each of the SMBus addresses.
  - AD[3:0] = 0001'b, the device address byte is 0xB2
  - AD[3:0] = 0010'b, the device address byte is 0xB4
  - AD[3:0] = 0011'b, the device address byte is 0xB6

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  - AD[3:0] = 0100'b, the device address byte is 0xB8
- The master implementation in the DS80PCI102 supports multiple devices reading from one EEPROM. When tying multiple devices to the SDA and SCL pins, use these guidelines:
  - Use adjacent SMBus addresses for the 4 devices
  - Use a pullup resistor on SDA; value = 4.7 kΩ
  - Use a pullup resistor on SCL; value = 4.7 kΩ
  - Daisy-chain $\overline{\text{READEN}}$ (Pin 17) and $\overline{\text{DONE}}$ (Pin18) from one device to the next device in the sequence.
    1. Tie $\overline{\text{READEN}}$ of the first device in the chain (U1) to GND
    2. Tie $\overline{\text{DONE}}$ of U1 to $\overline{\text{READEN}}$ of U2
    3. Tie $\overline{\text{DONE}}$ of U2 to $\overline{\text{READEN}}$ of U3
    4. Tie $\overline{\text{DONE}}$ of U3 to $\overline{\text{READEN}}$ of U4
    5. Optional: Tie $\overline{\text{DONE}}$ of U4 to a LED to show each of the devices have been loaded successfully

7.5.6.1 Master EEPROM Programming

The following example represents a 2 kbits (256 × 8-bit) EEPROM in hex format for the DS80PCI102 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the same SMBus line. There is a CRC enable flag to enable or disable CRC checking. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present, the configuration data start address immediately follows the 3-byte base header. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS80PCI102 device. For more details about EEPROM programming and Master mode, refer to SNLA228.

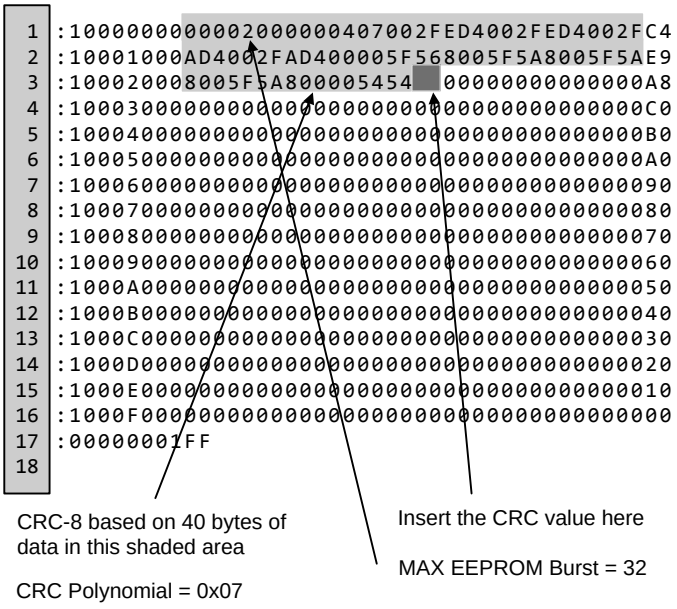

Figure 8. Typical EEPROM Data Set

NOTE

The maximum EEPROM size supported is 8kbits (1024 × 8 bits).

The CRC-8 calculation is performed on the first 3 bytes of header information plus the 37 bytes of data for the DS80PCI102, or 40 bytes in total. The result of this calculation is placed immediately after the DS80PCI102 data in the EEPROM, which ends with "5454". The CRC-8 in the DS80PCI102 uses a polynomial = $x^8 + x^2 + x + 1$.

There are two pins that provide unique functions in SMBus Master mode:

- $\overline{\text{DONE}}$
- $\overline{\text{READEN}}$

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When the DS80PCI102 is powered up in SMBus master mode, it reads its configuration from the external EEPROM when the READEN pin goes low. When the DS80PCI102 is finished reading its configuration from the external EEPROM, it drives the DONE pin low. In applications where there is more than one DS80PCI102 on the same SMBus, bus contention can result if more than one DS80PCI102 tries to take control of the SMBus at the same time. The READEN and DONE pins prevent this bus contention. The system should be designed so that the READEN pin from one DS80PCI102 in the system is driven low on power-up. This DS80PCI102 will take command of the SMBus on power-up and will read its initial configuration from the external EEPROM. When it is finished reading its configuration, it will drive the DONE pin low. This pin should be connected to the READEN pin of another DS80PCI102. When this second DS80PCI102 senses its READEN pin driven low, it will take command of the SMBus and read its initial configuration from the external EEPROM, after which it will set its DONE pin low. By connecting the DONE pin of each DS80PCI102 to the READEN pin of the next DS80PCI102, each DS80PCI102 can read its initial configuration from the EEPROM without causing bus contention.

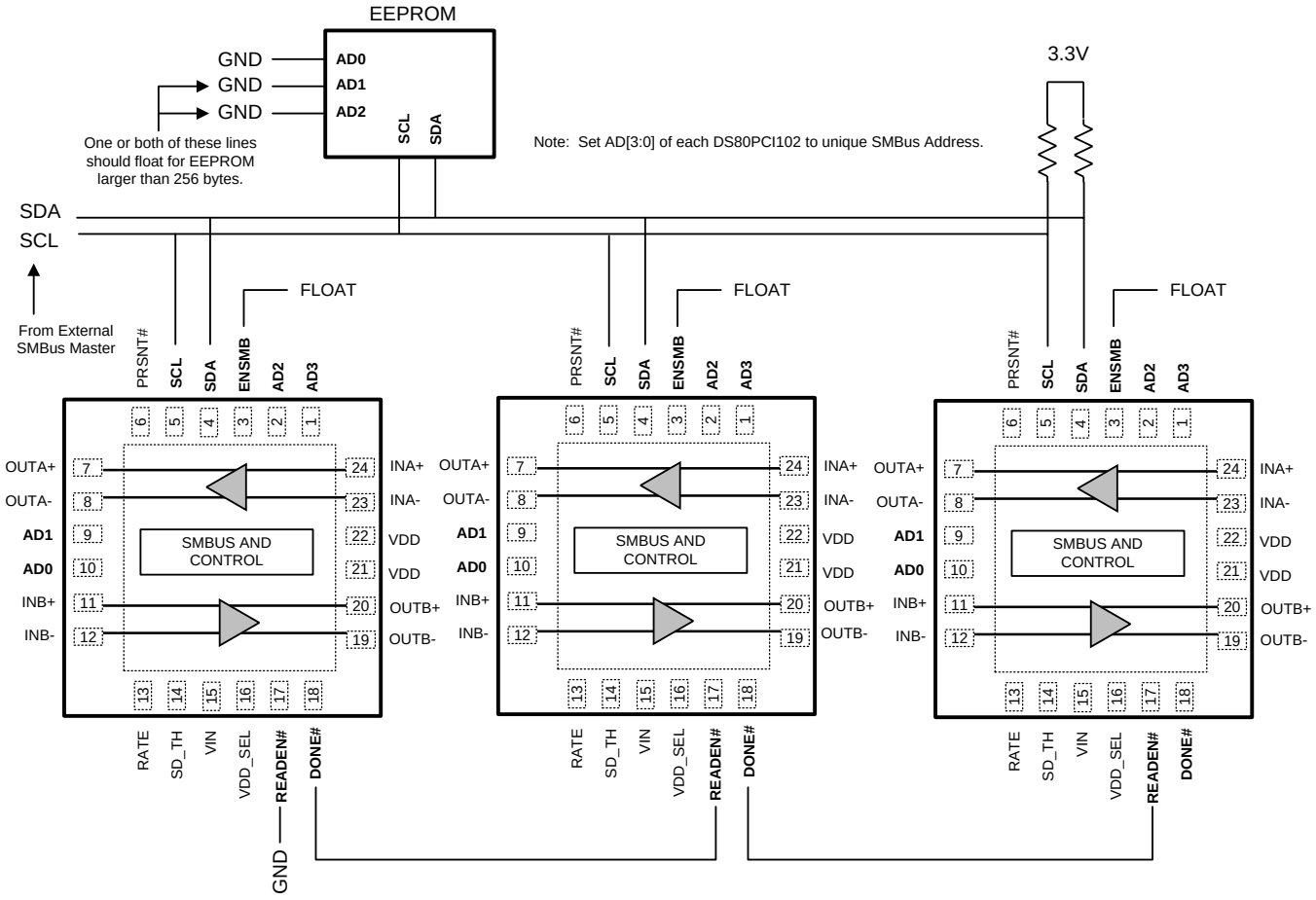

Figure 9. Typical Multi-Device EEPROM Connection Diagram

7.5.6.2 EEPROM Address Mapping

A detailed EEPROM Address Mapping for a single device is shown in Table 7. For instances where multiple devices are written to EEPROM, the device starting address definitions align starting with Byte 0x03. A register map overview for a multi-device EEPROM address map is shown in Table 8.

7.6 Register Maps

Table 7. Single Device with Default Value

EEPROM Address Byte			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Description		0x00	CRC_EN	Address Map Present	EEPROM > 256 Bytes	Reserved	DEVICE COUNT[3]	DEVICE COUNT[2]	DEVICE COUNT[1]	DEVICE COUNT[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x01	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x02	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x03	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PWDN CH B	PWDN CH A
SMBus Register			0x01[7]	0x01[6]	0x01[5]	0x01[4]	0x01[3]	0x01[2]	0x01[1]	0x01[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x04	Reserved	Reserved	PWDN_Inputs	PWDN_Osc	Override PRST	Reserved	Reserved	Reserved
SMBus Register			0x02[5]	0x02[4]	0x02[3]	0x02[2]	0x02[0]	0x04[7]	0x04[6]	0x04[5]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x05	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Ovrd IDLE_TH	Reserved
SMBus Register			0x04[4]	0x04[3]	0x04[2]	0x04[1]	0x04[0]	0x06[4]	0x08[6]	0x08[5]
Default Value	0x04		0	0	0	0	0	1	0	0
Description		0x06	Reserved	Ovrd RXDET	Ovrd RATE	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x08[4]	0x08[3]	0x08[2]	0x08[1]	0x08[0]	0x0B[6]	0x0B[5]	0x0B[4]
Default Value	0x07		0	0	0	0	0	1	1	1
Description		0x07	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RXDET_A_1	RXDET_A_0
SMBus Register			0x0B[3]	0x0B[2]	0x0B[1]	0x0B[0]	0x0E[5]	0x0E[4]	0x0E[3]	0x0E[2]
Default Value	0x00		0	0	0	0	0	0	0	0

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Table 7. Single Device with Default Value (continued)

EEPROM Address Byte			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Description		0x08	CHA_EQ[7]	CHA_EQ[6]	CHA_EQ[5]	CHA_EQ[4]	CHA_EQ[3]	CHA_EQ[2]	CH0_EQ[1]	CH0_EQ[0]
SMBus Register			0x0F[7]	0x0F[6]	0x0F[5]	0x0F[4]	0x0F[3]	0x0F[2]	0x0F[1]	0x0F[0]
Default Value	0x2F		0	0	1	0	1	1	1	1
Description		0x09	CHA_Sel SCP	CHA_Sel RATE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x10[7]	0x10[6]	0x10[5]	0x10[4]	0x10[3]	0x10[2]	0x10[1]	0x10[0]
Default Value	0xED		1	1	1	0	1	1	0	1
Description		0x0A	CHA_DEM[2]	CHA_DEM[1]	CHA_DEM[0]	Reserved	CHA_Idle_ThA[1]	CHA_Idle_ThA[0]	CHA_Idle_ThD[1]	CHA_Idle_ThD[0]
SMBus Register			0x11[2]	0x11[1]	0x11[0]	0x12[7]	0x12[3]	0x12[2]	0x12[1]	0x12[0]
Default Value	0x40		0	1	0	0	0	0	0	0
Description		0x0B	Reserved	Reserved	RXDET_B_1	RXDET_B_0	CHB_EQ[7]	CHB_EQ[6]	CHB_EQ[5]	CHB_EQ[4]
SMBus Register			0x15[5]	0x15[4]	0x15[3]	0x15[2]	0x16[7]	0x16[6]	0x16[5]	0x16[4]
Default Value	0x02		0	0	0	0	0	0	1	0
Description		0x0C	CHB_EQ[3]	CHB_EQ[2]	CHB_EQ[1]	CHB_EQ[0]	CHB_Sel SCP	CHB_Sel RATE	Reserved	Reserved
SMBus Register			0x16[3]	0x16[2]	0x16[1]	0x16[0]	0x17[7]	0x17[6]	0x17[5]	0x17[4]
Default Value	0xFE		1	1	1	1	1	1	1	0
Description		0x0D	Reserved	Reserved	Reserved	Reserved	CHB_DEM[2]	CHB_DEM[1]	CHB_DEM[0]	Reserved
SMBus Register			0x17[3]	0x17[2]	0x17[1]	0x17[0]	0x18[2]	0x18[1]	0x18[0]	0x19[7]
Default Value	0xD4		1	1	0	1	0	1	0	0
Description		0x0E	CHB_Idle_ThA[1]	CHB_Idle_ThA[0]	CHB_Idle_ThD[1]	CHB_Idle_ThD[0]	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x19[3]	0x19[2]	0x19[1]	0x19[0]	0x1C[5]	0x1C[4]	0x1C[3]	0x1C[2]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x0F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x1D[7]	0x1D[6]	0x1D[5]	0x1D[4]	0x1D[3]	0x1D[2]	0x1D[1]	0x1D[0]
Default Value	0x2F		0	0	1	0	1	1	1	1

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Table 7. Single Device with Default Value (continued)

EEPROM Address Byte			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Description		0x10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x1E[7]	0x1E[6]	0x1E[5]	0x1E[4]	0x1E[3]	0x1E[2]	0x1E[1]	0x1E[0]
Default Value	0xAD		1	0	1	0	1	1	0	1
Description		0x11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x1F[2]	0x1F[1]	0x1F[0]	0x20[7]	0x20[3]	0x20[2]	0x20[1]	0x20[0]
Default Value	0x40		0	1	0	0	0	0	0	0
Description		0x12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x23[5]	0x23[4]	0x23[3]	0x23[2]	0x24[7]	0x24[6]	0x24[5]	0x24[4]
Default Value	0x02		0	0	0	0	0	0	1	0
Description		0x13	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHA_VOD[2]
SMBus Register			0x24[3]	0x24[2]	0x24[1]	0x24[0]	0x25[7]	0x25[6]	0x25[5]	0x25[4]
Default Value	0xFA		1	1	1	1	1	0	1	0
Description		0x14	CHA_VOD[1]	CHA_VOD[0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x25[3]	0x25[2]	0x25[1]	0x25[0]	0x26[2]	0x26[1]	0x26[0]	0x27[7]
Default Value	0xD4		1	1	0	1	0	1	0	0
Description		0x15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x27[3]	0x27[2]	0x27[1]	0x27[0]	0x28[6]	0x28[5]	0x28[4]	0x28[3]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x16	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x28[2]	0x28[1]	0x28[0]	0x2B[5]	0x2B[4]	0x2B[3]	0x2B[2]	0x2C[7]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x2C[6]	0x2C[5]	0x2C[4]	0x2C[3]	0x2C[2]	0x2C[1]	0x2C[0]	0x2D[7]
Default Value	0x5F		0	1	0	1	1	1	1	1

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Table 7. Single Device with Default Value (continued)

EEPROM Address Byte			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Description		0x18	Reserved	Reserved	CHB_VOD[2]	CHB_VOD[1]	CHB_VOD[0]	Reserved	Reserved	Reserved
SMBus Register			0x2D[6]	0x2D[5]	0x2D[4]	0x2D[3]	0x2D[2]	0x2D[1]	0x2D[0]	0x2E[2]
Default Value	0x5A		0	1	0	1	1	0	1	0
Description		0x19	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x2E[1]	0x2E[0]	0x2F[7]	0x2F[3]	0x2F[2]	0x2F[1]	0x2F[0]	0x32[5]
Default Value	0x80		1	0	0	0	0	0	0	0
Description		0x1A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x32[4]	0x32[3]	0x32[2]	0x33[7]	0x33[6]	0x33[5]	0x33[4]	0x33[3]
Default Value	0x05		0	0	0	0	0	1	0	1
Description		0x1B	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x33[2]	0x33[1]	0x33[0]	0x34[7]	0x34[6]	0x34[5]	0x34[4]	0x34[3]
Default Value	0xF5		1	1	1	1	0	1	0	1
Description		0x1C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x34[2]	0x34[1]	0x34[0]	0x35[2]	0x35[1]	0x35[0]	0x36[7]	0x36[3]
Default Value	0xA8		1	0	1	0	1	0	0	0
Description		0x1D	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x36[2]	0x36[1]	0x36[0]	0x39[5]	0x39[4]	0x39[3]	0x39[2]	0x3A[7]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x1E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x3A[6]	0x3A[5]	0x3A[4]	0x3A[3]	0x3A[2]	0x3A[1]	0x3A[0]	0x3B[7]
Default Value	0x5F		0	1	0	1	1	1	1	1
Description		0x1F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x3B[6]	0x3B[5]	0x3B[4]	0x3B[3]	0x3B[2]	0x3B[1]	0x3B[0]	0x3C[2]
Default Value	0x5A		0	1	0	1	1	0	1	0

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Table 7. Single Device with Default Value (continued)

EEPROM Address Byte			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Description		0x20	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x3C[1]	0x3C[0]	0x3D[7]	0x3D[3]	0x3D[2]	0x3D[1]	0x3D[0]	0x40[5]
Default Value	0x80		1	0	0	0	0	0	0	0
Description		0x21	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x40[4]	0x40[3]	0x40[2]	0x41[7]	0x41[6]	0x41[5]	0x41[4]	0x41[3]
Default Value	0x05		0	0	0	0	0	1	0	1
Description		0x22	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x41[2]	0x41[1]	0x41[0]	0x42[7]	0x42[6]	0x42[5]	0x42[4]	0x42[3]
Default Value	0xF5		1	1	1	1	0	1	0	1
Description		0x23	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x42[2]	0x42[1]	0x42[0]	0x43[2]	0x43[1]	0x43[0]	0x44[7]	0x44[3]
Default Value	0xA8		1	0	1	0	1	0	0	0
Description		0x24	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x44[2]	0x44[1]	0x44[0]	0x47[3]	0x47[2]	0x47[1]	0x47[0]	0x48[7]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x25	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x48[6]	0x4C[7]	0x4C[6]	0x4C[5]	0x4C[4]	0x4C[3]	0x4C[0]	0x59[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x26	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x5A[7]	0x5A[6]	0x5A[5]	0x5A[4]	0x5A[3]	0x5A[2]	0x5A[1]	0x5A[0]
Default Value	0x54		0	1	0	1	0	1	0	0
Description		0x27	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x5B[7]	0x5B[6]	0x5B[5]	0x5B[4]	0x5B[3]	0x5B[2]	0x5B[1]	0x5B[0]
Default Value	0x54		0	1	0	1	0	1	0	0

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Table 8. Multi-Device EEPROM Register Map Overview(1)(2)(3)(4)

	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Header	0	CRC EN	Address Map	EEPROM > 256 Bytes	Reserved	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	2	EE Burst[7]	EE Burst[6]	EE Burst[5]	EE Burst[4]	EE Burst[3]	EE Burst[2]	EE Burst[1]	EE Burst[0]
Device 0 Info	3	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	4	EE AD0 [7]	EE AD0 [6]	EE AD0 [5]	EE AD0 [4]	EE AD0 [3]	EE AD0 [2]	EE AD0 [1]	EE AD0 [0]
Device 1 Info	5	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	6	EE AD1 [7]	EE AD1 [6]	EE AD1 [5]	EE AD1 [4]	EE AD1 [3]	EE AD1 [2]	EE AD1 [1]	EE AD1 [0]
Device 2 Info	7	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	8	EE AD2 [7]	EE AD2 [6]	EE AD2 [5]	EE AD2 [4]	EE AD2 [3]	EE AD2 [2]	EE AD2 [1]	EE AD2 [0]
Device 3 Info	9	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	10	EE AD3 [7]	EE AD3 [6]	EE AD3 [5]	EE AD3 [4]	EE AD3 [3]	EE AD3 [2]	EE AD3 [1]	EE AD3 [0]
Device 0 Addr 3	11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PWDN CH B	PWDN CH A
Device 0 Addr 4	12	Reserved	Reserved	PDWN Inp	PDWN OSC	Ovrd PRST	Reserved	Reserved	Reserved
Device 0 Addr 38	46	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Device 0 Addr 39	47	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Device 1 Addr 3	48	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PWDN CH B	PWDN CH A
Device 1 Addr 4	49	Reserved	Reserved	PDWN Inp	PDWN OSC	Ovrd PRST	Reserved	Reserved	Reserved
Device 1 Addr 38	83	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Device 1 Addr 39	84	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Device 2 Addr 3	85	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PWDN CH B	PWDN CH A
Device 2 Addr 4	86	Reserved	Reserved	PDWN Inp	PDWN OSC	Ovrd PRST	Reserved	Reserved	Reserved

(1) CRC EN = 1; Address Map = 1
(2) EEPROM > 256 Bytes = 0
(3) COUNT[3:0] = 0011'b
(4) Multiple DS80PCI102 devices may point at the same address space if they have identical programming values.

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Table 8. Multi-Device EEPROM Register Map Overview[(1)(2)(3)(4)] (continued)

	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Device 2 Addr 38	120	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Device 2 Addr 39	121	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Device 3 Addr 3	122	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PWDN CH B	PWDN CH A
Device 3 Addr 4	123	Reserved	Reserved	PDWN Inp	PDWN OSC	Ovrd PRST	Reserved	Reserved	Reserved
Device 3 Addr 38	157	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Device 3 Addr 39	158	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Table 9. Multi DS80PCI102 EEPROM Data

EEPROM Address	Address (Hex)	EEPROM Data	Comments
0	00	0x43	CRC_EN = 0, Address Map = 1, Device Count = 3 (Devices 0, 1, 2, and 3)
1	01	0x00	
2	02	0x08	EEPROM Burst Size
3	03	0x00	CRC not used
4	04	0x0B	Device 0 Address Location
5	05	0x00	CRC not used
6	06	0x30	Device 1 Address Location
7	07	0x00	CRC not used
8	08	0x30	Device 2 Address Location
9	09	0x00	CRC not used
10	0A	0x0B	Device 3 Address Location
11	0B	0x00	Begin Device 0 and Device 3 - Address Offset 3
12	0C	0x00	
13	0D	0x04	
14	0E	0x07	
15	0F	0x00	
16	10	0x2F	Default EQ CHA
17	11	0xED	
18	12	0x40	
19	13	0x02	Default EQ CHB
20	14	0xFE	Default EQ CHB
21	15	0xD4	
22	16	0x00	
23	17	0x2F	
24	18	0xAD	
25	19	0x40	
26	1A	0x02	
27	1B	0xFA	PCI102 CHA VOD = 1000 mVpp
28	1C	0xD4	PCI102 CHA VOD = 1000 mVpp
29	1D	0x01	
30	1E	0x80	
31	1F	0x5F	
32	20	0x56	PCI102 CHB VOD = 1000 mVpp
33	21	0x80	
34	22	0x05	
35	23	0xF5	
36	24	0xA8	
37	25	0x00	
38	26	0x5F	
39	27	0x5A	
40	28	0x80	
41	29	0x05	
42	2A	0xF5	
43	2B	0xA8	
44	2C	0x00	
45	2D	0x00	
46	2E	0x54	

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Table 9. Multi DS80PCI102 EEPROM Data (continued)

EEPROM Address	Address (Hex)	EEPROM Data	Comments
47	2F	0x54	End Device 0 and Device 3 - Address Offset 39
48	30	0x00	Begin Device 1 and Device 2 - Address Offset 3
49	31	0x00	
50	32	0x04	
51	33	0x07	
52	34	0x00	
53	35	0x2F	Default EQ CHA
54	36	0xED	
55	37	0x40	
56	38	0x02	Default EQ CHB
57	39	0xFE	Default EQ CHB
58	3A	0xD4	
59	3B	0x00	
60	3C	0x2F	
61	3D	0xAD	
62	3E	0x40	
63	3F	0x02	
64	40	0xFA	PCI102 CHA VOD = 1000 mVpp
65	41	0xD4	PCI102 CHA VOD = 1000 mVpp
66	42	0x01	
67	43	0x80	
68	44	0x5F	
69	45	0x56	PCI102 CHB VOD = 1000 mVpp
70	46	0x80	
71	47	0x05	
72	48	0xF5	
73	49	0xA8	
74	4A	0x00	
75	4B	0x5F	
76	4C	0x5A	
77	4D	0x80	
78	4E	0x05	
79	4F	0xF5	
80	50	0xA8	
81	51	0x00	
82	52	0x00	
83	53	0x54	
84	54	0x54	End Device 1 and Device 2 - Address Offset 39

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Table 10. SMBus Register Map

Address	Register Name	Bit	Field	Type	Default	EEPROM Bit	Description
0x00	Device Address Observation	7	Reserved	R/W	0x00		Reserved
		6:3	I2C Address [3:0]	R			SMBus strap observation
		2	EEPROM reading done	R			1: Device completed the read from external EEPROM
		1	Reserved	RWSC			Reserved
		0	Reserved	RWSC			Reserved
0x01	Control 1	7:2	Reserved	R/W	0x00	Yes	Reserved
		1:0	PWDN A/B				[1]: Powerdown Channel B (1); Normal Operation (0) [0]: Powerdown Channel A (1); Normal Operation (0)
0x02	Control 2	7	Override RXDET	R/W	0x00		1 = Override Automatic Rx Detect State Machine Reset
		6	RXDET Value				1 = Set Rx Detect State Machine Reset 0 = Clear Rx Detect State Machine Reset
		5:4	Reserved			Yes	Reserved
		3	PWDN Inputs			Yes	Reserved
		2	PWDN Oscillator			Yes	Reserved
		1	Reserved				Reserved
		0	Override PRSNT			Yes	1: Enables Reg 0x01[1:0] 0: Normal Operation
0x03	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x04	Reserved	7:0	Reserved	R/W	0x00	Yes	Reserved
0x05	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x06	Slave Register Control	7:5	Reserved	R/W	0x10		Reserved
		4	Reserved			Yes	Reserved
		3	Register Enable				1 = Enables SMBus Slave Mode Register Control **Note: To change VOD, DEM, and EQ of the channels in slave mode, this bit must be set to 1.**
		2:0	Reserved				Reserved
0x07	Digital Reset and Control	7	Reserved	R/W	0x01		Reserved
		6	Reset Regs				Self clearing reset for registers. Writing a [1] will return register settings to default values.
		5	Reset SMBus Master				Self clearing reset to SMBus master state machine
		4:0	Reserved				Reserved
0x08	Pin Override	7	Reserved	R/W	0x00		Reserved
		6	Override Idle Threshold			Yes	[1]: Override by Channel - see Reg 0x12 and 0x19 [0]: SD_TH pin control
		5:4	Reserved			Yes	Set bits to 0
		3	Override RXDET			Yes	[1]: Force RXDET by Channel - see Reg 0x0E and 0x15 [0]: Normal Operation
		2	Override RATE			Yes	[1]: Override by Channel - see Reg 0x10 and 0x17 [0]: Normal Operation
		1:0	Reserved			Yes	Reserved
0x09	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x0A	Reserved	7:0	Reserved	R	0x00		Reserved

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Table 10. SMBus Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Bit	Description
0x0B	Reserved	7	Reserved	R/W	0x70		Reserved
		6:0	Reserved	R/W		Yes	Reserved
0x0C	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x0D	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x0E	CH A RXDET Control	7:6	Reserved	R/W	0x00		Reserved
		5:4	Reserved			Yes	Reserved
		3:2	RXDET			Yes	00: Input is hi-Z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is hi-Z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved				Reserved
0x0F	CH A EQ Control	7:0	BOOST [7:0]	R/W	0x2F	Yes	EQ Control - total of 256 levels See Table 2
0x10	CH A RATE Control	7	Sel_scp	R/W	0xED	Yes	1 = Short Circuit Protection ON 0 = Short Circuit Protection OFF
		6	Sel_RATE			Yes	1 = Select GEN1/2 Mode 0 = Select GEN3 Mode
		5:3	Reserved			Yes	Reserved
		2:0	Reserved			Yes	Reserved
0x11	CH A DEM Control	7	Reserved	R	0x82		Reserved
		6:5	Rate Information				Signal Rate Detected 00 = GEN1 (2.5G) 01 = GEN2 (5.0G) 11 = GEN3 (8.0G)
		4:3	Reserved	R/W			Reserved
		2:0	DEM [2:0]			Yes	DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x12	CH A Idle Threshold	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:2	idle_thA[1:0]			Yes	Assert Thresholds Use only if register 0x08 [6] = 1 00 = 180 mV (Default) 01 = 160 mV 10 = 210 mV 11= 190 mV
		1:0	idle_thD[1:0]			Yes	Deassert Thresholds Use only if register 0x08 [6] = 1 00 = 110 mV (Default) 01 = 100 mV 10 = 150 mV 11= 130 mV
0x13	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x14	Reserved	7:0	Reserved	R/W	0x00		Reserved

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Table 10. SMBus Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Bit	Description
0x15	CH B RXDET Control	7:6	Reserved	R/W	0x00		Reserved
		5:4	Reserved			Yes	Reserved
		3:2	RXDET			Yes	00: Input is hi-Z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is hi-Z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is hi-Z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved				Reserved
0x16	CH B EQ Control	7:0	BOOST [7:0]	R/W	0x2F	Yes	EQ Control - total of 256 levels See Table 2
0x17	CH B RATE Control	7	Sel_scp	R/W	0xED	Yes	1 = Short Circuit Protection ON 0 = Short Circuit Protection OFF
		6	Sel_RATE			Yes	1 = Select GEN1/2 Mode 0 = Select GEN3 Mode
		5:3	Reserved			Yes	Reserved
		2:0	Reserved			Yes	Reserved
0x18	CH B DEM Control	7	Reserved	R	0x02		Reserved
		6:5	Rate Information				Signal Rate Detected 00 = GEN1 (2.5G) 01 = GEN2 (5.0G) 11 = GEN3 (8.0G)
		4:3	Reserved	R/W			Reserved
		2:0	DEM [2:0]			Yes	DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x19	CH B Idle Threshold	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:2	idle_thA[1:0]			Yes	Assert Thresholds Use only if register 0x08 [6] = 1 00 = 180 mV (Default) 01 = 160 mV 10 = 210 mV 11= 190 mV
		1:0	idle_thD[1:0]			Yes	Deassert Thresholds Use only if register 0x08 [6] = 1 00 = 110 mV (Default) 01 = 100 mV 10 = 150 mV 11= 130 mV
0x1A-0x1B	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x1C	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x1D	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x1E	Reserved	7:0	Reserved	R/W	0xAD	Yes	Reserved

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Table 10. SMBus Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Bit	Description
0x1F	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved
0x20	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x21-0x22	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x23	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x24	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x25	CH A VOD	7:5	Reserved	R/W	0xAD	Yes	Reserved
		4:2	VOD CHA Control			Yes	VOD Control CHA 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V (default) 100: 1.1 V 101: 1.2 V 110: 1.3 V 111: 1.4 V
		1:0	Reserved			Yes	Reserved
0x26	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved
0x27	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x28	Idle Control	7	Reserved	R/W	0x00		Reserved
		6:0	Reserved			Yes	Reserved
0x29-0x2A	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x2B	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x2C	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x2D	CH B VOD	7:5	Reserved	R/W	0xAD	Yes	Reserved
		4:2	VOD CHB Control			Yes	VOD Control CHB 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V (default) 100: 1.1 V 101: 1.2 V 110: 1.3 V 111: 1.4 V
		1:0	Reserved			Yes	Reserved
0x2E	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved
0x2F	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x30-0x31	Reserved	7:0	Reserved	R/W	0x00		Reserved

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Table 10. SMBus Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Bit	Description
0x32	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x33	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x34	Reserved	7:0	Reserved	R/W	0xAD	Yes	Reserved
0x35	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved
0x36	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x37-0x38	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x39	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x3A	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x3B	Reserved	7:0	Reserved	R/W	0xAD	Yes	Reserved
0x3C	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved
0x3D	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x3E-0x3F	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x40	Reserved	7:6	Reserved	R/W	0x00		Reserved
		5:2	Reserved			Yes	Reserved
		1:0	Reserved				Reserved
0x41	Reserved	7:0	Reserved	R/W	0x2F	Yes	Reserved
0x42	Reserved	7:0	Reserved	R/W	0xAD	Yes	Reserved
0x43	Reserved	7:3	Reserved	R/W	0x02		Reserved
		2:0	Reserved			Yes	Reserved
0x44	Reserved	7	Reserved	R/W	0x00	Yes	Reserved
		6:4	Reserved				Reserved
		3:0	Reserved			Yes	Reserved
0x45	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x46	Reserved	7:0	Reserved	R/W	0x38		Reserved
0x47	Reserved	7:4	Reserved	R/W	0x00		Reserved
		3:0	Reserved			Yes	Reserved
0x48	Reserved	7:6	Reserved	R/W	0x05	Yes	Reserved
		5:0	Reserved				Reserved
0x49-0x4B	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x4C	Reserved	7:3	Reserved	R/W	0x00	Yes	Reserved
		2:1	Reserved				Reserved
		0	Reserved			Yes	Reserved
0x4D-0x50	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x51	Device Information	7:5	Version[2:0]	R	0x77		011'b
		4:0	Device ID[4:0]				1 0111'b
0x52	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x53	Reserved	7:0	Reserved	R/W	0x00		Reserved

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Table 10. SMBus Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Bit	Description
0x54	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x55	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x56	Reserved	7:0	Reserved	R/W	0x10		Reserved
0x57	Reserved	7:0	Reserved	R/W	0x64		Reserved
0x58	Reserved	7:0	Reserved	R/W	0x21		Reserved
0x59	Reserved	7:1	Reserved	R/W	0x00		Reserved
		0	Reserved			Yes	Reserved
0x5A	Reserved	7:0	Reserved	R/W	0x54	Yes	Reserved
0x5B	Reserved	7:0	Reserved	R/W	0x54	Yes	Reserved
0x5C	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x5D	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x5E	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x5F	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x60	Reserved	7:0	Reserved	R/W	0x00		Reserved
0x61	Reserved	7:0	Reserved	R/W	0x00		Reserved

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In PCIe Gen-3 applications, the specification requires Rx-Tx link training to establish and optimize signal conditioning settings at 8 Gbps. In link training, the Rx partner requests a series of FIR - preshoot and de-emphasis coefficients (10 Presets) from the Tx partner. The Rx partner includes 7-levels (6 dB to 12 dB) of CTLE followed by a single tap DFE. The link training would pre-condition the signal with an equalized link between the root-complex and endpoint. Note that there is no link training in PCIe Gen-1 (2.5 Gbps) or PCIe Gen-2 (5.0 Gbps) applications. The DS80PCI102 is placed in between the Tx and Rx. It would help extend the PCB trace reach distance by boosting the attenuated signals with it's equalization, so that the signal can be more easily recovered by the downstream Rx. In Gen 3 mode, DS80PCI102 transmit outputs are designed to pass the Tx Preset signaling onto the Rx for the PCIe Gen 3 link to train and optimize the equalization settings. The suggested setting for the DS80PCI102 are EQ = 0x00, VOD = 1.2 Vp-p and DEM = 0 dB. Additional adjustments to increase the EQ or DEM setting should be performed to optimize the eye opening in the Rx partner. See the tables below for Pin Mode and SMBus Mode configurations.

Table 11. Suggested Device Settings in Pin Mode

Channel	Pin Mode Settings
EQx[1:0]	0, 0 (Level 1)
DEMx	Float, R (Level 10)

Table 12. Suggested Device Settings in SMBus Slave Mode

Register	Write Value	Comments
0x06	0x18	Enables SMBus Slave Mode Register Control
0x0F	0x00	Set CHA EQ to 0x00.
0x25	0xAD	Set CHA VOD to 101'b (1.2 Vp-p).
0x11	0x00	Set CHA DEM to 000'b (0 dB).
0x16	0x00	Set CHB EQ to 0x00.
0x2D	0xAD	Set CHB VOD to 101'b (1.2 Vp-p).
0x18	0x00	Set CHB DEM to 000'b (0 dB).

8.2 Typical Application

The DS80PCI102 extends PCB trace and cable reach in PCIe Gen1, 2 and 3 applications by applying equalization to compensate for the insertion loss of the trace or cable. In Gen 3 mode, the device aids specifically in the equalization link training to improve the margin and overall eye inside the Rx. The DS80PCI102 can be used on the motherboard, mid plane (riser card), end-point target cards, and active cable assemblies. The capability of the DS80PCI102 performance is shown in the following two test setup connections.

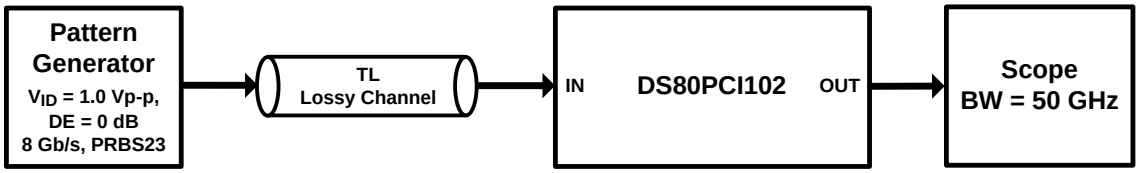


Figure 10. Test Setup Connections Diagram

Typical Application (continued)

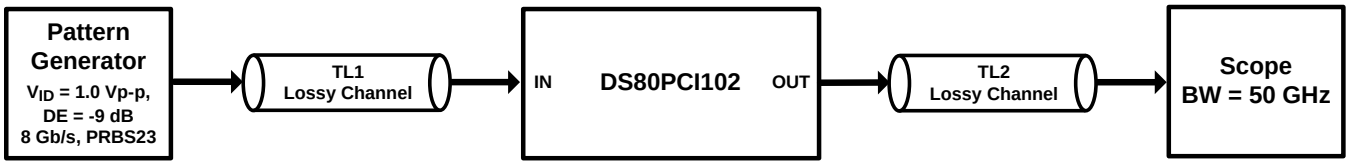


Figure 11. Test Setup Connections Diagram

8.2.1 Design Requirements

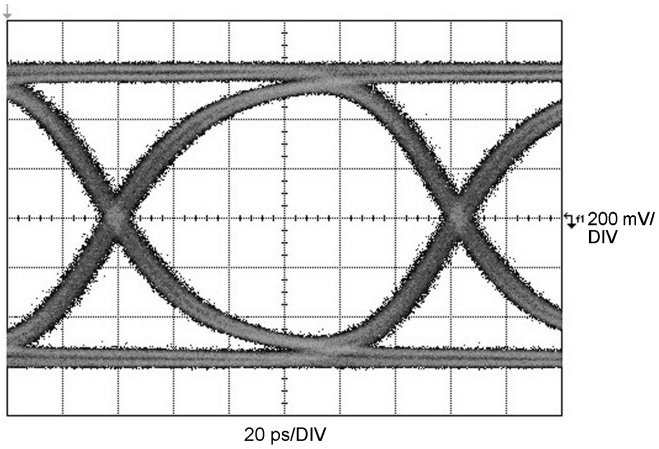
As with any high speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Use 100-Ω impedance traces. Length matching on the P and N traces should be done on the single-end segments of the differential pair.
- Use uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- For Gen3, AC-coupling capacitors of 220 nF are recommended, maximum body size is 0402, and add cutout void on GND plane below the landing pad of the capacitor in order to reduce parasitic capacitance to GND.
- Back-drill connector vias and signal vias to minimize stub length.
- Use Reference plane vias to ensure a low inductance path for the return current.

8.2.2 Detailed Design Procedure

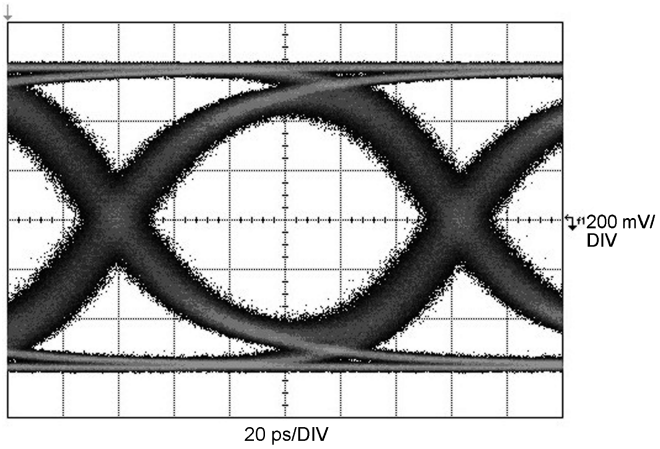
The DS80PCI102 should be placed at an offset location and close to the Rx with respect to the overall channel attenuation. The suggested settings are recommended as a starting point for most applications. Once these settings are configured, additional adjustments of the DS80PCI102 EQ or DE may be required to optimize the repeater performance. The CTLE and DFE coefficient in the Rx can also be adjusted to further improve the eye opening.

8.2.3 Application Curves



DS80PCI102 Settings:
EQ[1:0] = [R, R] or 0x15, Dem[1:0] = [Float, Float]

Figure 12. TL = 20-Inch 4–Mil FR4 Trace



DS80PCI102 Settings:
EQ[1:0] = [Float, R] or 0x1F, DEM[1:0] = [Float, Float]

Figure 13. TL = 35-Inch 4–Mil FR4 Trace

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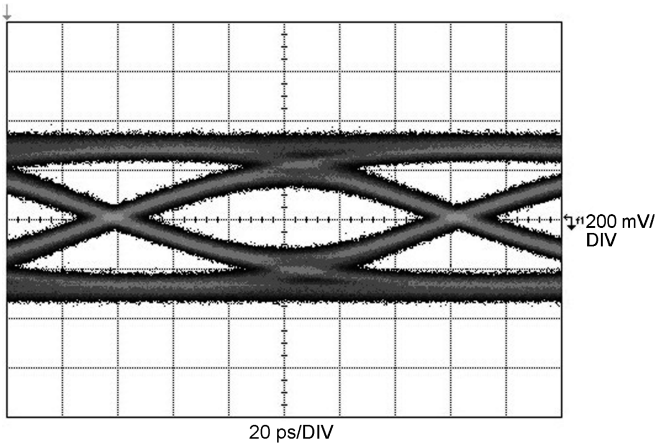
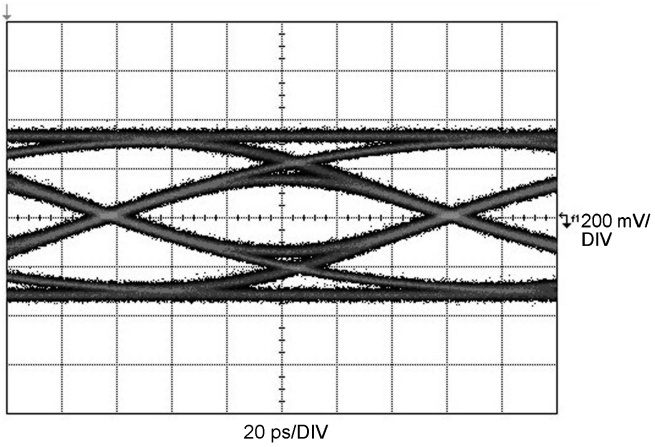
Typical Application (continued)



DS80PCI102 Settings:
EQ[1:0] = [R, R] or 0x15, DEM[1:0] = [Float, Float]

Figure 14. TL1 = 20-Inch 4–Mil FR4 Trace, TL2 = 15-Inch 4–Mil FR4 Trace



DS80PCI102 Settings:
EQ[1:0] = [R, 1] or 0x0F, DEM[1:0] = [Float, Float]

Figure 15. TL1 = 30-Inch 4–Mil FR4 Trace, TL2 = 15-Inch 4–Mil FR4 Trace

9 Power Supply Recommendations

9.1 3.3-V or 2.5-V Supply Mode Operation

The DS80PCI102 has an optional internal voltage regulator to provide the 2.5-V supply to the device. In 3.3-V mode, the VIN pin = 3.3 V is used to supply power to the device and the VDD pins should be left open. The internal regulator will provide the 2.5 V to the VDD pins of the device and a 0.1-µF capacitor is needed at each of the five VDD pins for power supply de-coupling (total capacitance should be ≤ 0.5 µF), and the VDD pins should be left open. The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5-V mode, the VIN pin should be left open and 2.5-V supply must be applied to the VDD pins. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

The DS80PCI102 can be configured for 2.5-V operation or 3.3-V operation. The lists below outline required connections for each supply selection.

3.3-V Mode of Operation

1. Tie VDD_SEL = 0 with 1-kΩ resistor to GND.
2. Feed 3.3-V supply into VIN pin. Local 1.0-µF decoupling at VIN is recommended.
3. See information on VDD bypass below.
4. SDA and SCL pins should connect pullup resistor to VIN
5. Any 4-Level input which requires a connection to "Logic 1" should use a 1-kΩ resistor to VIN

2.5-V Mode of Operation

6. VDD_SEL = Float
7. VIN = Float
8. Feed 2.5-V supply into VDD pins.
9. See information on VDD bypass below.
10. SDA and SCL pins connect pullup resistor to VDD for 2.5-V uC SMBus IO
11. SDA and SCL pins connect pullup resistor to VDD for 3.3-V uC SMBus IO
12. Any 4-Level input which requires a connection to "Logic 1" should use a 1-kΩ resistor to VIN

NOTE

Note: The DAP (bottom solder pad) is the GND connection.

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3.3-V or 2.5-V Supply Mode Operation (continued)

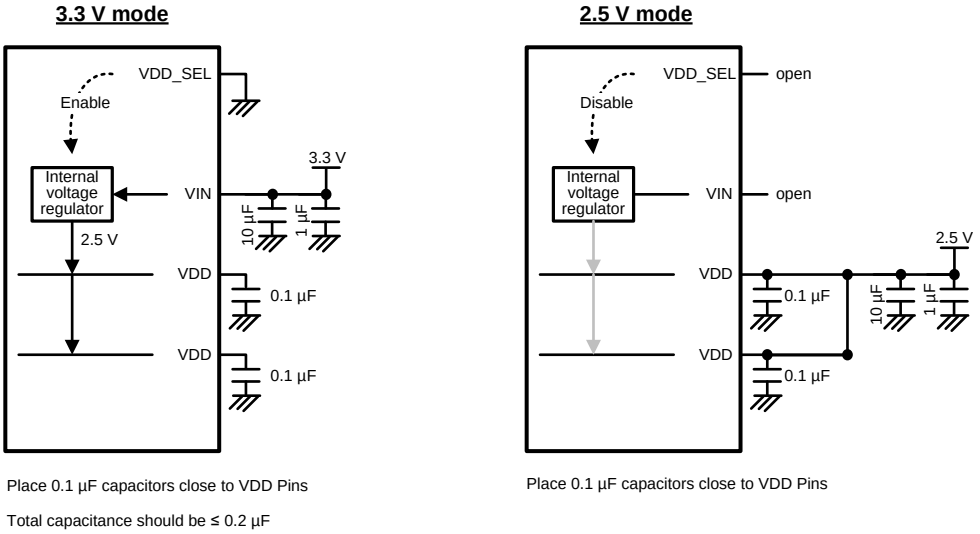

Figure 16. 3.3 V or 2.5 V Supply Connection Diagram

9.2 Power Supply Bypass

Two approaches are recommended to ensure that the DS80PCI102 is provided with an adequate power supply bypass. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to the device. Small body size capacitors (such as 0402) reduce the parasitic inductance of the capacitor and also help in placement close to the VDD pin. If possible, the layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.

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10 Layout

10.1 Layout Guidelines

The differential inputs and outputs are designed with 100-Ω differential terminations. Therefore, they should be connected to interconnects with controlled differential impedance of approximately 85-110 Ω. It is preferable to route differential lines primarily on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used, the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. To minimize the effects of crosstalk, a 5:1 ratio or greater should be maintained between inter-pair spacing and trace width. See AN-1187 *Leadless Leadframe Package (LLP) Application Report* (SNOA401) for additional information on QFN (WQFN) packages.

The DS80PCI102 pinout promotes easy high speed routing and layout. To optimize DS80PCI102 performance refer to the following guidelines:

1. Place local VIN and VDD capacitors as close as possible to the device supply pins. Often the best location is directly under the DS80PCI102 pins to reduce the inductance path to the capacitor. In addition, bypass capacitors may share a via with the DAP GND to minimize ground loop inductance.
2. Differential pairs going into or out of the DS80PCI102 should have adequate pair-to-pair spacing to minimize crosstalk.
3. Use return current via connections to link reference planes locally. This ensures a low inductance return current path when the differential signal changes layers.
4. Optimize the via structure to minimize trace impedance mismatch.
5. Place GND vias around the DAP perimeter to ensure optimal electrical and thermal performance.
6. Use small body size AC coupling capacitors when possible — 0402 or smaller size is preferred. The AC coupling capacitors should be placed closer to the Rx on the channel.

Figure 17 depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the detrimental high-frequency effects of stubs on the signal path.

10.2 Layout Example

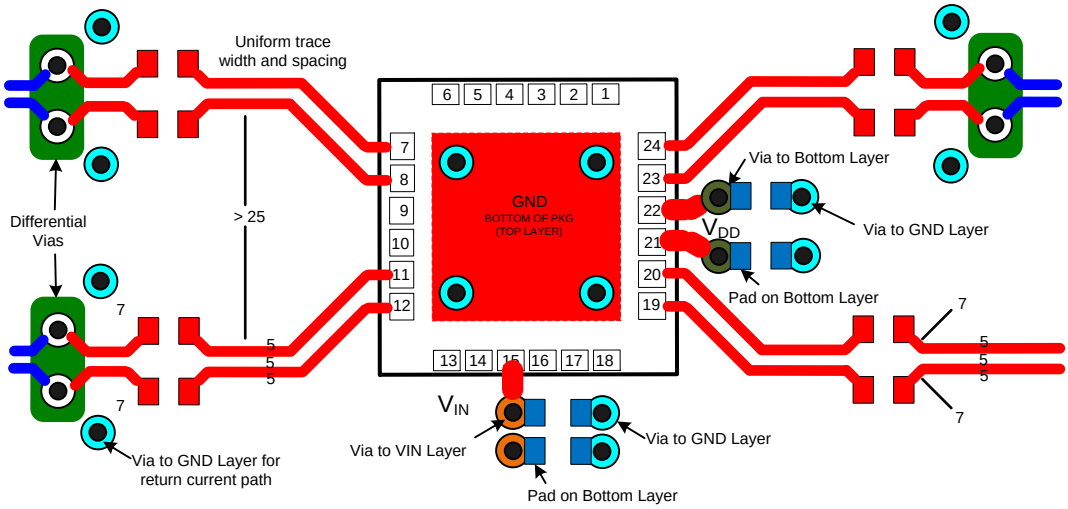

Figure 17. Typical Routing Options

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Absolute Maximum Ratings for Soldering*, SNOA549

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
PCI-Express is a trademark of PCI-SIG.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS80PCI102SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	PCI102	Samples
DS80PCI102SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	PCI102	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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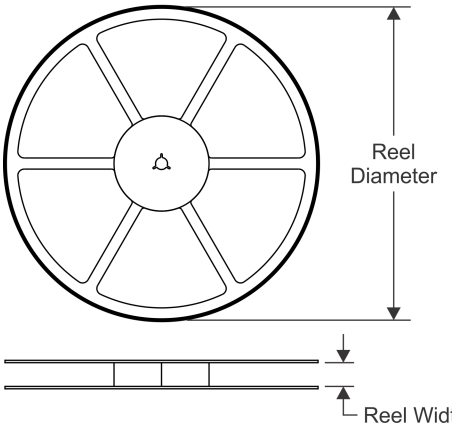
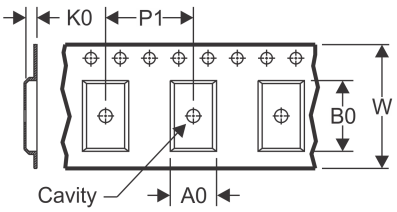
TAPE AND REEL INFORMATION

REEL DIMENSIONS

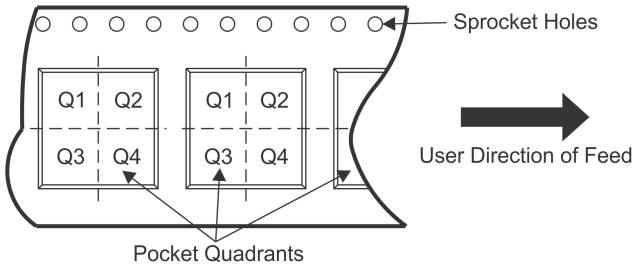


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

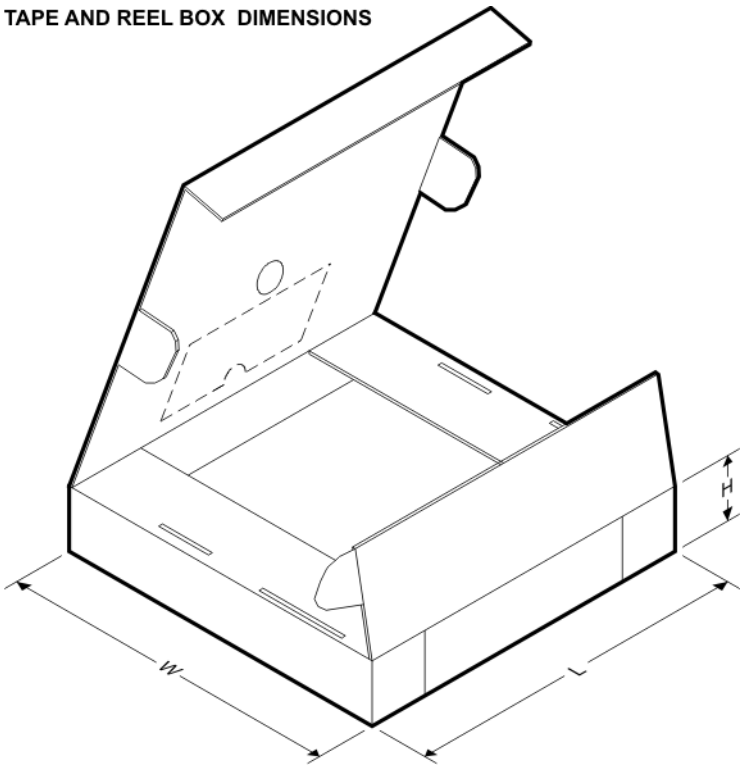
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS80PCI102SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS80PCI102SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

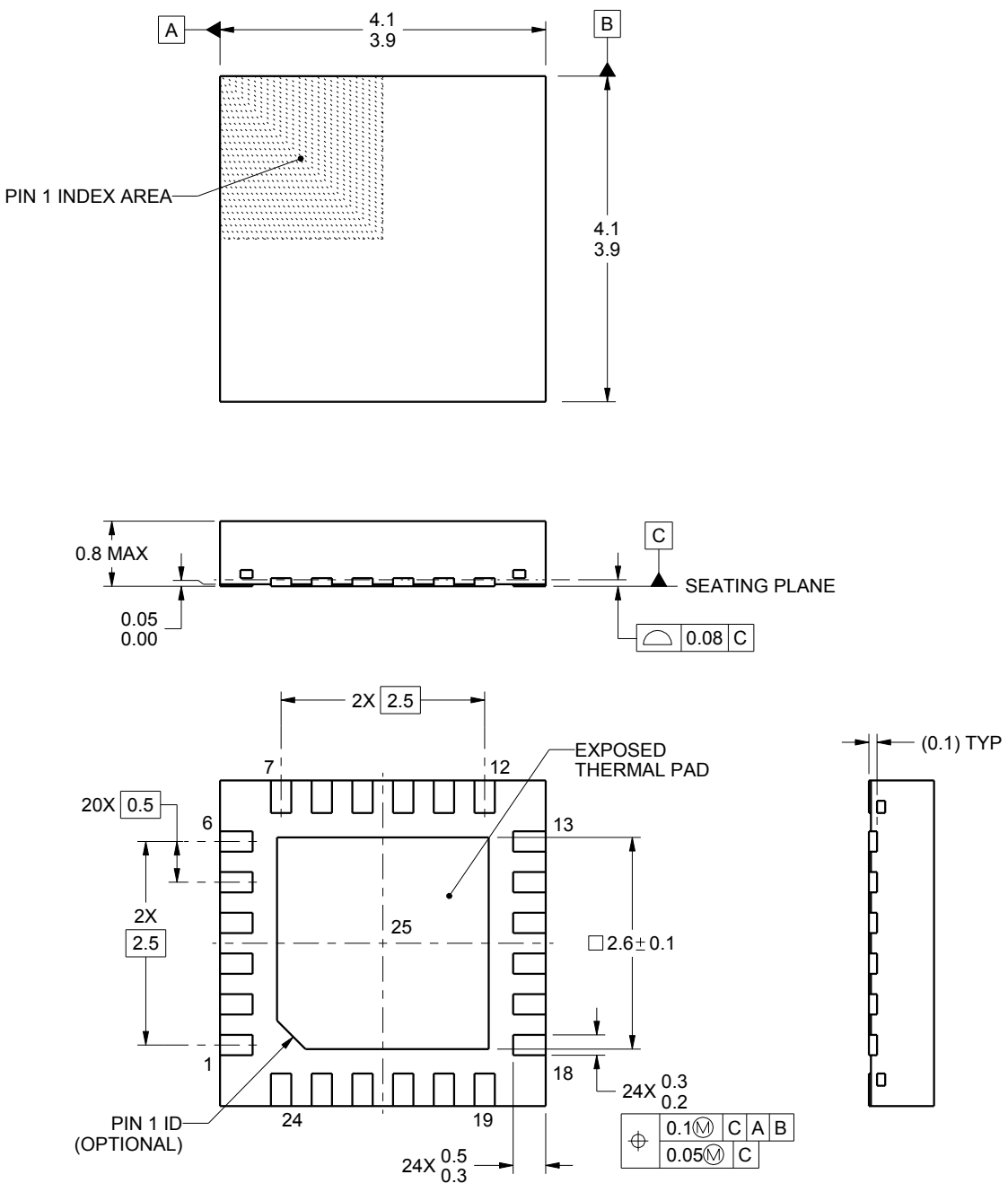
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS80PCI102SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
DS80PCI102SQE/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0

PACKAGE OUTLINE

RTW0024A

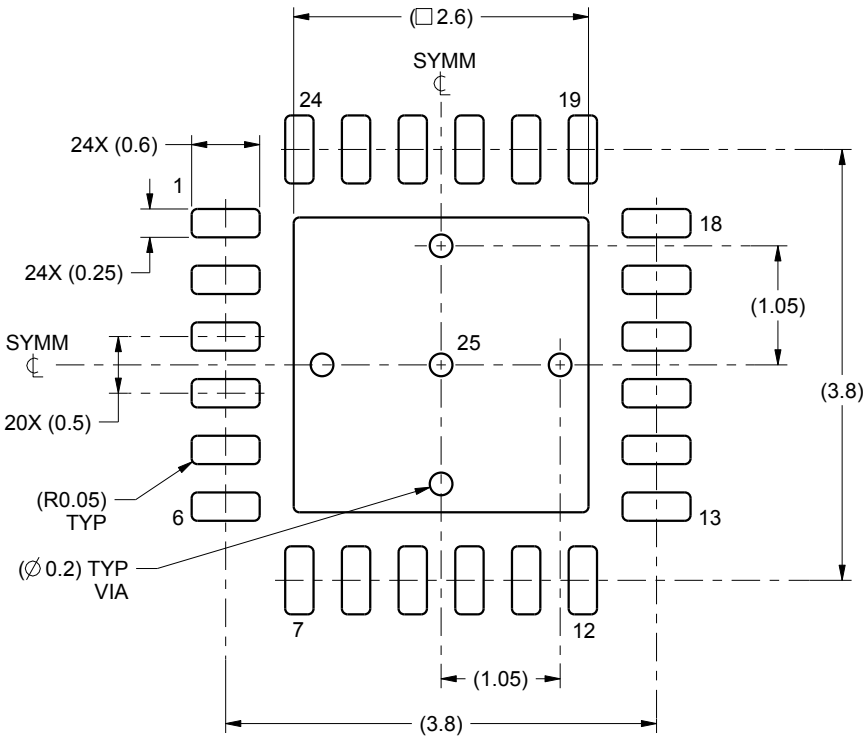
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

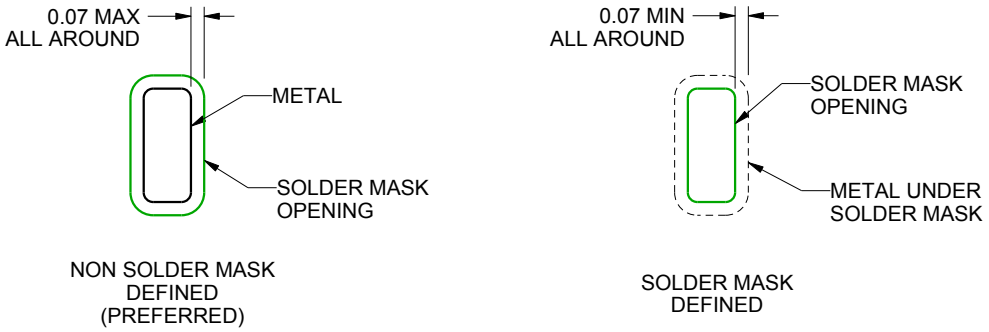


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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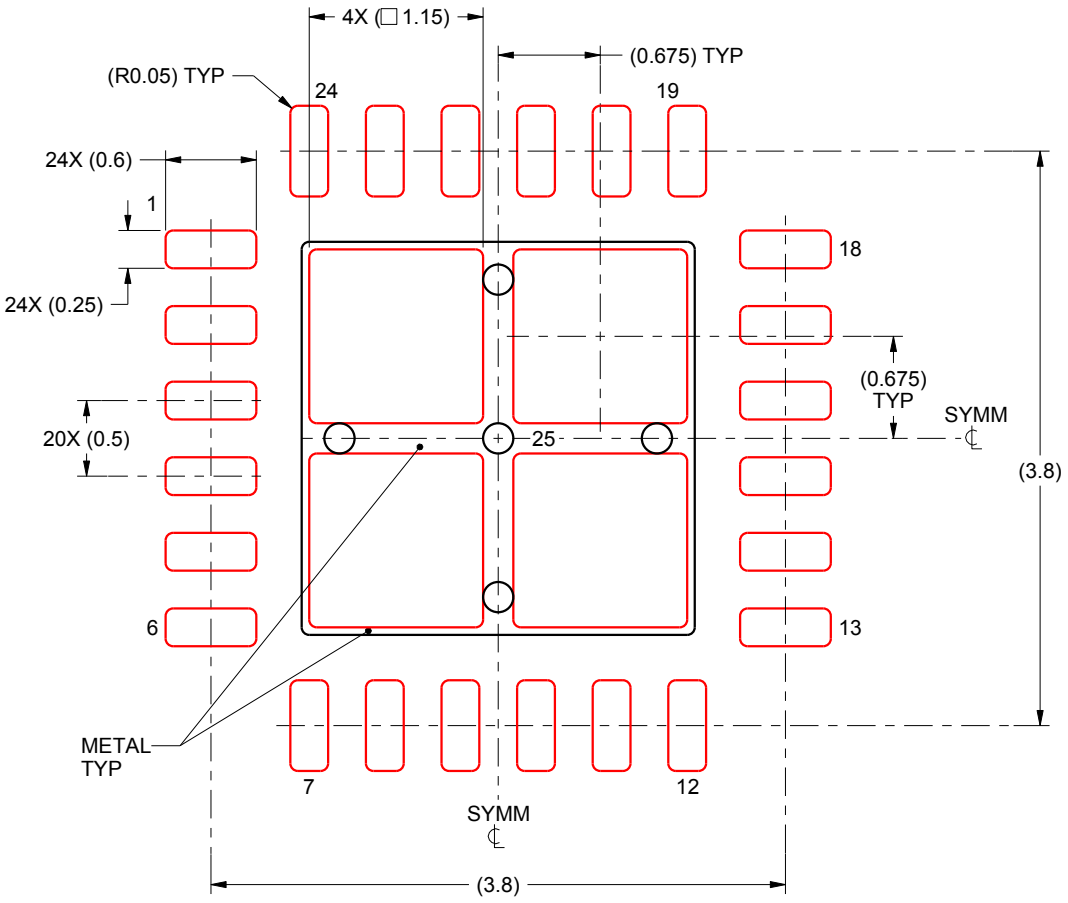
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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