THE DATASHEET OF

STM32H753ZIT6TR

www.win-source.net 0086-755-83957316

STM32H753xI

32-bit Arm® Cortex®-M7 480MHz MCUs, 2MB Flash, 1MB RAM, 46 com. and analog interfaces, crypto

Datasheet - production data

Features

Includes ST state-of-the-art patented technology

Core

- 32-bit Arm® Cortex®-M7 core with double-precision FPU and L1 cache: 16 Kbytes of data and 16 Kbytes of instruction cache; frequency up to 480 MHz, MPU, 1027 DMIPS/ 2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

Memories

- 2 Mbytes of Flash memory with read-while-write support
- 1 Mbyte of RAM: 192 Kbytes of TCM RAM (inc. 64 Kbytes of ITCM RAM + 128 Kbytes of DTCM RAM for time critical routines), 864 Kbytes of user SRAM, and 4 Kbytes of SRAM in Backup domain
- Dual mode Quad-SPI memory interface running up to 133 MHz
- Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND Flash memory clocked up to 100 MHz in Synchronous mode
- CRC calculation unit

Security

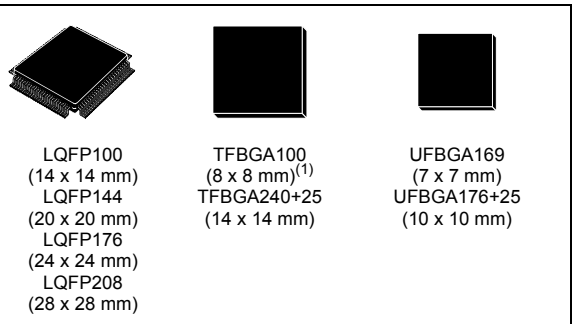
- ROP, PC-ROP, active tamper, secure firmware upgrade support, Secure access mode

General-purpose input/outputs

- Up to 168 I/O ports with interrupt capability

Reset and power management

- 3 separate power domains which can be independently clock-gated or switched off:



LQFP100 (14 x 14 mm)
LQFP144 (20 x 20 mm)
LQFP176 (24 x 24 mm)
LQFP208 (28 x 28 mm)

TFBGA100 (8 x 8 mm)(1)
TFBGA240+25 (14 x 14 mm)

UFBGA169 (7 x 7 mm)
UFBGA176+25 (10 x 10 mm)

  - D1: high-performance capabilities
  - D2: communication peripherals and timers
  - D3: reset/clock control/power management
- 1.62 to 3.6 V application supply and I/Os
- POR, PDR, PVD and BOR
- Dedicated USB power embedding a 3.3 V internal regulator to supply the internal PHYs
- Embedded regulator (LDO) with configurable scalable output to supply the digital circuitry
- Voltage scaling in Run and Stop mode (6 configurable ranges)
- Backup regulator (~0.9 V)
- Voltage reference for analog peripheral/V_{REF+}
- Low-power modes: Sleep, Stop, Standby and V_{BAT} supporting battery charging

Low-power consumption

- V_{BAT} battery operating mode with charging capability
- CPU and domain power state monitoring pins
- 2.95 µA in Standby mode (Backup SRAM OFF, RTC/LSE ON)

Clock management

- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI

This is information on a product in full production. www.st.com

- External oscillators: 4-48 MHz HSE, 32.768 kHz LSE
- 3× PLLs (1 for the system clock, 2 for kernel clocks) with Fractional mode

Interconnect matrix

- 3 bus matrices (1 AXI and 2 AHB)
- Bridges (5× AHB2-APB, 2× AXI2-AHB)

4 DMA controllers to unload the CPU

- 1× high-speed master direct memory access controller (MDMA) with linked list support
- 2× dual-port DMAs with FIFO
- 1× basic DMA with request router capabilities

Up to 35 communication peripherals

- 4× I2Cs FM+ interfaces (SMBus/PMBus)
- 4× USARTs/4x UARTs (ISO7816 interface, LIN, IrDA, up to 12.5 Mbit/s) and 1x LPUART
- 6× SPIs, 3 with muxed duplex I2S audio class accuracy via internal audio PLL or external clock, 1x I2S in LP domain (up to 150 MHz)
- 4x SAIs (serial audio interface)
- SPDIFRX interface
- SWPMI single-wire protocol master I/F
- MDIO Slave interface
- 2× SD/SDIO/MMC interfaces (up to 125 MHz)
- 2× CAN controllers: 2 with CAN FD, 1 with time-triggered CAN (TT-CAN)
- 2× USB OTG interfaces (1FS, 1HS/FS) crystal-less solution with LPM and BCD
- Ethernet MAC interface with DMA controller
- HDMI-CEC
- 8- to 14-bit camera interface (up to 80 MHz)

11 analog peripherals

- 3× ADCs with 16-bit max. resolution (up to 36 channels, up to 3.6 MSPS)
- 1× temperature sensor
- 2× 12-bit D/A converters (1 MHz)
- 2× ultra-low-power comparators
- 2× operational amplifiers (7.3 MHz bandwidth)
- 1× digital filters for sigma delta modulator (DFSDM) with 8 channels/4 filters

Graphics

- LCD-TFT controller up to XGA resolution
- Chrom-ART graphical hardware Accelerator (DMA2D) to reduce CPU load
- Hardware JPEG Codec

Up to 22 timers and watchdogs

- 1× high-resolution timer (2.1 ns max resolution)
- 2× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input (up to 240 MHz)
- 2× 16-bit advanced motor control timers (up to 240 MHz)
- 10× 16-bit general-purpose timers (up to 240 MHz)
- 5× 16-bit low-power timers (up to 240 MHz)
- 2× watchdogs (independent and window)
- 1× SysTick timer
- RTC with sub-second accuracy and hardware calendar

Cryptographic acceleration

- AES 128, 192, 256, TDES,
- HASH (MD5, SHA-1, SHA-2), HMAC
- True random number generators

Debug mode

- SWD & JTAG interfaces
- 4-Kbyte Embedded Trace Buffer

96-bit unique ID

All packages are ECOPACK2 compliant

Table 1. Device summary

Reference	Part number
STM32H753xI	STM32H753VI, STM32H753ZI, STM32H753II, STM32H753BI, STM32H753XI, STM32H753AI

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1 Introduction

This document provides information on STM32H53xI microcontrollers, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging, and ordering information.

This document should be read in conjunction with the STM32H53xI reference manual (RM0433), available from the STMicroelectronics website *www.st.com*.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32H53xI errata sheet (ES0396), available on the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-M7 core, please refer to the Cortex®-M7 Technical Reference Manual, available from the http://www.arm.com website.

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2 Description

STM32H753xI devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 480 MHz. The Cortex® -M7 core features a floating point unit (FPU) which supports Arm® double-precision (IEEE 754 compliant) and single-precision data-processing instructions and data types. STM32H753xI devices support a full set of DSP instructions and a memory protection unit (MPU) to enhance application security.

STM32H753xI devices incorporate high-speed embedded memories with a dual-bank Flash memory of 2 Mbytes, up to 1 Mbyte of RAM (including 192 Kbytes of TCM RAM, up to 864 Kbytes of user SRAM and 4 Kbytes of backup SRAM), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, 2x32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memory access.

All the devices offer three ADCs, two DACs, two ultra-low power comparators, a low-power RTC, a high-resolution timer, 12 general-purpose 16-bit timers, two PWM timers for motor control, five low-power timers, a true random number generator (RNG), and a cryptographic acceleration cell. The devices support four digital filters for external sigma-delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals
  - Four I^2Cs
  - Four USARTs, four UARTs and one LPUART
  - Six SPIs, three I2Ss in Half-duplex mode. To achieve audio class accuracy, the I2S peripherals can be clocked by a dedicated internal audio PLL or by an external clock to allow synchronization.
  - Four SAI serial audio interfaces
  - One SPDIFRX interface
  - One SWPMI (Single Wire Protocol Master Interface)
  - Management Data Input/Output (MDIO) slaves
  - Two SDMMC interfaces
  - A USB OTG full-speed and a USB OTG high-speed interface with full-speed capability (with the ULPI)
  - One FDCAN plus one TT-FDCAN interface
  - An Ethernet interface
  - Chrom-ART Accelerator
  - HDMI-CEC
- Advanced peripherals including
  - A flexible memory control (FMC) interface
  - A Quad-SPI Flash memory interface
  - A camera interface for CMOS sensors
  - An LCD-TFT display controller
  - A JPEG hardware compressor/decompressor

Refer to *Table 2: STM32H753xI features and peripheral counts* for the list of peripherals available on each part number.

STM32H753xI devices operate in the –40 to +85 °C temperature range from a 1.62 to 3.6 V power supply. The supply voltage can drop down to 1.62 V by using an external power supervisor (see *Section 3.5.2: Power supply supervisor)* and connecting the PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

Dedicated supply inputs for USB (OTG_FS and OTG_HS) are available on all packages except LQFP100 to allow a greater power supply choice.

A comprehensive set of power-saving modes allows the design of low-power applications.

STM32H753xI devices are offered in 8 packages ranging from 100 pins to 240 pins/balls. The set of included peripherals changes with the device chosen.

These features make STM32H753xI microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smart watches.

Figure 1 shows the device block diagram.

Table 2. STM32H753xI features and peripheral counts

Peripherals		STM32H753 VI	STM32H753 ZI	STM32H753 AI	STM32H753 II	STM32H753 BI	STM32H753 XI
Flash memory in Kbytes		2 x 1 Mbyte					
SRAM in Kbytes	SRAM mapped onto AXI bus	512					
	SRAM1 (D2 domain)	128					
	SRAM2 (D2 domain)	128					
	SRAM3 (D2 domain)	32					
	SRAM4 (D3 domain)	64					
TCM RAM in Kbytes	ITCM RAM (instruction)	64					
	DTCM RAM (data)	128					
Backup SRAM (Kbytes)		4					
FMC		Yes(1)					
GPIOs		82	114	131	140	168	
Quad-SPI interface		Yes					
Ethernet		Yes					
Timers	High-resolution	1					
	General-purpose	10					
	Advanced-control (PWM)	2					
	Basic	2					
	Low-power	5					
Wakeup pins Tamper pins		4 2		5 2	6 3		
Random number generator		Yes					
Cryptographic accelerator		Yes					

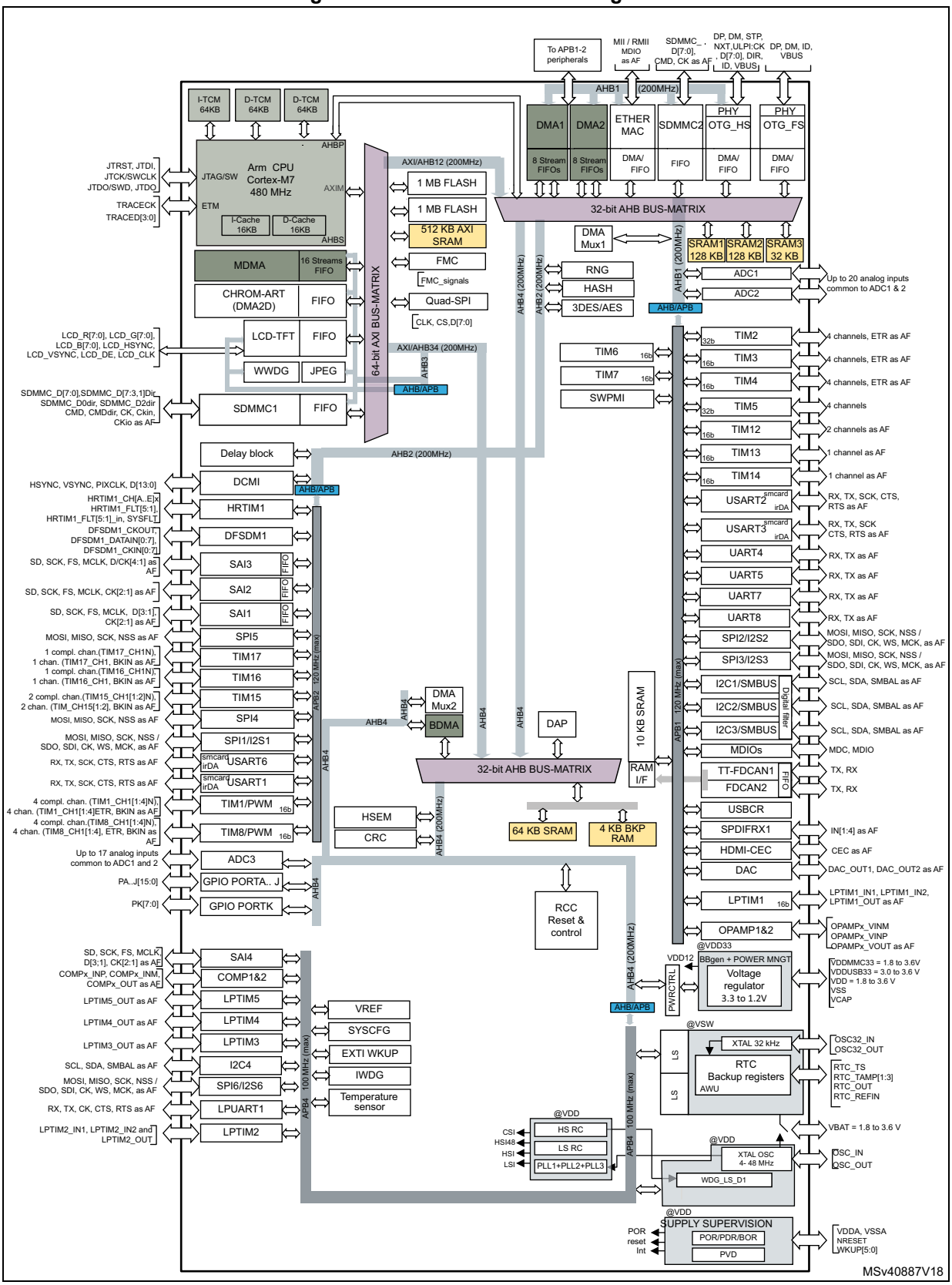
Table 2. STM32H753xI features and peripheral counts (continued)

Peripherals		STM32H753 VI	STM32H753 ZI	STM32H753 AI	STM32H753 II	STM32H753 BI	STM32H753 XI
Communication interfaces	SPI / I2S	6/3[2]					
	I2C	4					
	USART/UART/ LPUART	4/4 /1					
	SAI	4					
	SPDIFRX	4 inputs					
	SWPMI	Yes					
	MDIO	Yes					
	SDMMC	2					
	FDCAN/TT-FDCAN	1/1					
	USB OTG_FS	Yes					
	USB OTG_HS	Yes					
Ethernet and camera interface		Yes					
LCD-TFT		Yes					
JPEG Codec		Yes					
Chrom-ART Accelerator (DMA2D)		Yes					
16-bit ADCs		3					
Number of Direct channels Number of Fast channels Number of Slow channels		2 3 11	2 9 17	2 9 21			4 9 23
12-bit DAC Number of channels		Yes 2					
Comparators		2					
Operational amplifiers		2					
DFSDM		Yes					
Maximum CPU frequency		480MHz[3][4]/400 MHz					
Operating voltage		1.71 to 3.6 V[5]	1.62 to 3.6 V[6]				
Operating temperatures		Ambient temperatures: –40 up to +85 °C[7]					
		Junction temperature: –40 to + 125 °C					
Package		LQFP100 TFBGA100	LQFP144	UFBGA169	LQFP176 UFBGA176+ 25	LQFP208	TFBGA240+ 25

1. SDRAM is not available on LQFP144 package.
2. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. The maximum CPU frequency of 480 MHz can be obtained on devices revision V.

4. The product junction temperature must be kept within the –40 to +105 °C temperature range.
5. Since the LQFP100 package does not feature the PDR_ON pin (tied internally to V_{DD}), the minimum V_{DD} value for this package is 1.71 V.
6. V_{DD}/V_{DDA} can drop down to 1.62 V by using an external power supervisor (see *Section 3.5.2: Power supply supervisor*) and connecting PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.
7. The product junction temperature must be kept within the –40 to +125 °C temperature range.

Figure 1. STM32H753xI block diagram



3 Functional overview

3.1 Arm® Cortex®-M7 with FPU

The Arm® Cortex®-M7 with double-precision FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 1 shows the general block diagram of the STM32H753xI family.

Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to 8 independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

3.3 Memories

3.3.1 Embedded Flash memory

The STM32H753xI devices embed 2 Mbytes of Flash memory that can be used for storing programs and data.

The Flash memory is organized as 266-bit Flash words memory that can be used for storing both code and data constants. Each word consists of:

- One Flash word (8 words, 32 bytes or 256 bits)
- 10 ECC bits.

The Flash memory is divided into two independent banks. Each bank is organized as follows:

- 1 Mbyte of user Flash memory block containing eight user sectors of 128 Kbytes (4 K Flash memory words)
- 128 Kbytes of System Flash memory from which the device can boot
- 2 Kbytes (64 Flash words) of user option bytes for user configuration

3.3.2 Secure access mode

In addition to other typical memory protection mechanism (RDP, PCROP), STM32H753xI devices introduce the Secure access mode, a new enhanced security feature. This mode allows developing user-defined secure services by ensuring, on the one hand code and data protection and on the other hand code safe execution.

Two types of secure services are available:

- STMicroelectronics Root Secure Services:

  These services are embedded in System memory. They provide a secure solution for firmware and third-party modules installation. These services rely on cryptographic algorithms based on a device unique private key.
- User-defined secure services:

  These services are embedded in user Flash memory. Examples of user secure services are proprietary user firmware update solution, secure Flash integrity check or any other sensitive applications that require a high level of protection.

  The secure firmware is embedded in specific user Flash memory areas configured through option bytes.

Secure services are executed just after a reset and preempt all other applications to guarantee protected and safe execution. Once executed, the corresponding code and data are no more accessible.

The above secure services are available only for Cortex®-M7 core operating in Secure access mode. The other masters cannot access the option bytes involved in Secure access mode settings or the Flash secured areas.

3.3.3 Embedded SRAM

All devices feature:

- 512 Kbytes of AXI-SRAM mapped onto AXI bus on D1 domain.
- SRAM1 mapped on D2 domain: 128 Kbytes
- SRAM2 mapped on D2 domain: 128 Kbytes
- SRAM3 mapped on D2 domain: 32 Kbytes
- SRAM4 mapped on D3 domain: 64 Kbytes
- 4 Kbytes of backup SRAM

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.
- RAM mapped to TCM interface (ITCM and DTCM):

  Both ITCM and DTCM RAMs are 0 wait state memories. either They can be accessed either from the CPU or the MDMA (even in Sleep mode) through a specific AHB slave of the CPU(AHBP):
  - 64 Kbytes of ITCM-RAM (instruction RAM)

    This RAM is connected to ITCM 64-bit interface designed for execution of critical real-times routines by the CPU.
  - 128 Kbytes of DTCM-RAM (2x 64-Kbyte DTCM-RAMs on 2x32-bit DTCM ports)

    The DTCM-RAM could be used for critical real-time data, such as interrupt service routines or stack/heap memory. Both DTCM-RAMs can be used in parallel (for load/store operations) thanks to the Cortex®-M7 dual issue capability.

  The MDMA can be used to load code or data in ITCM or DTCM RAMs.

Error code correction (ECC)

Over the product lifetime, and/or due to external events such as radiations, invalid bits in memories may occur. They can be detected and corrected by ECC. This is an expected behavior that has to be managed at final-application software level in order to ensure data integrity through ECC algorithms implementation.

SRAM data are protected by ECC:

- 7 ECC bits are added per 32-bit word.
- 8 ECC bits are added per 64-bit word for AXI-SRAM and ITCM-RAM.

The ECC mechanism is based on the SECDED algorithm. It supports single-error correction and double-error detection.

3.4 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space
- All RAM address space: ITCM, DTCM RAMs and SRAMs
- The System memory bootloader

The boot loader is located in non-user System memory. It is used to reprogram the Flash memory through a serial interface (USART, I2C, SPI, USB-DFU). Refer to *STM32 microcontroller System memory Boot mode* application note (AN2606) for details.

3.5 Power supply management

3.5.1 Power supply scheme

STM32H53xI power supply voltages are the following:

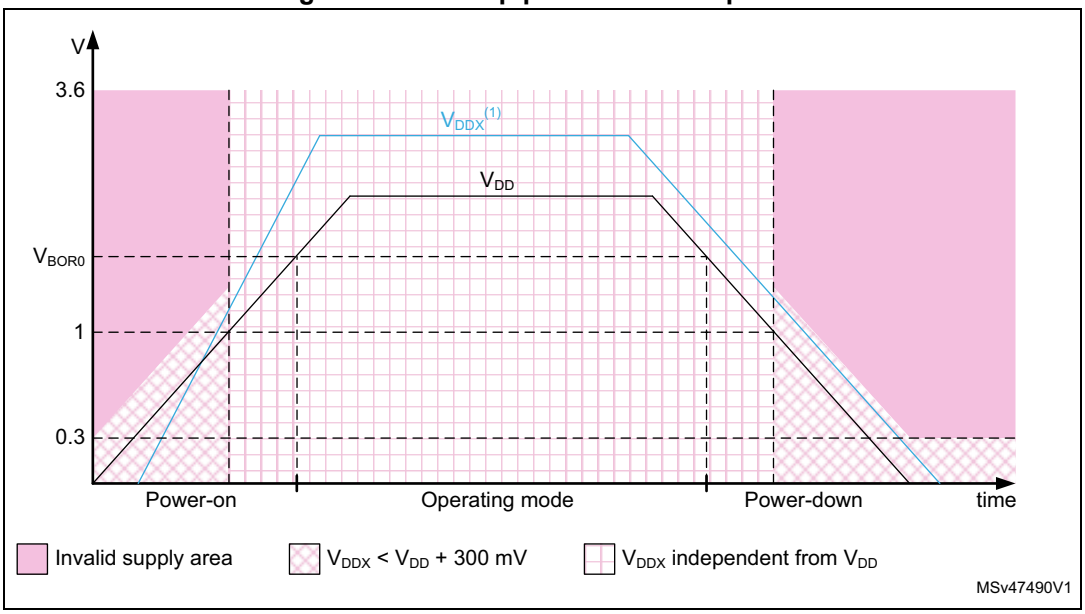
- V_{DD} = 1.62 to 3.6 V: external power supply for I/Os, provided externally through V_{DD} pins.
- V_{DDLDO} = 1.62 to 3.6 V: supply voltage for the internal regulator supplying V_{CORE}
- V_{DDA} = 1.62 to 3.6 V: external analog power supplies for ADC, DAC, COMP and OPAMP.
- $V_{DD33USB}$ and $V_{DD50USB}$:
  $V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via the USB internal regulator. This allows supporting a V_{DD} supply different from 3.3 V.
  The USB regulator can be bypassed to supply directly $V_{DD33USB}$ if V_{DD} = 3.3 V.
- V_{BAT} = 1.2 to 3.6 V: power supply for the V_{SW} domain when V_{DD} is not present.
- V_{CAP}: V_{CORE} supply voltage, which values depend on voltage scaling (1.0 V, 1.1 V, 1.2 V or 1.35 V). They are configured through VOS bits in PWR_D3CR register and ODEN bit in the SYSCFG_PWRCR register. The V_{CORE} domain is split into the following power domains that can be independently switch off.
  - D1 domain containing some peripherals and the Cortex®-M7 core.
  - D2 domain containing a large part of the peripherals.
  - D3 domain containing some peripherals and the system control.

During power-up and power-down phases, the following power sequence requirements must be respected (see *Figure 2*):

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, $V_{DD33USB}$, $V_{DD50USB}$) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the microcontroller remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 2. Power-up/power-down sequence



1. V_{DDx} refers to any power supply among V_{DDA}, $V_{DD33USB}$, $V_{DD50USB}$.

3.5.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in Reset mode when V_{DD} is below this threshold,

- Power-down reset (PDR)

  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.

  The PDR supervisor can be enabled/disabled through PDR_ON pin.

- Brownout reset (BOR)

  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.

3.5.3 Voltage regulator

The same voltage regulator supplies the 3 power domains (D1, D2 and D3). D1 and D2 can be independently switched off.

Voltage regulator output can be adjusted according to application needs through 6 power supply levels:

- Run mode (VOS0 to VOS3)
  - Scale 0: boosted performance (available only with LDO regulator)
  - Scale 1: high performance
  - Scale 2: medium performance and consumption
  - Scale 3: optimized performance and low-power consumption
- Stop mode (SVOS3 to SVOS5)
  - Scale 3: peripheral with wakeup from Stop mode capabilities (UART, SPI, I2C, LPTIM) are operational
  - Scale 4 and 5 where the peripheral with wakeup from Stop mode is disabled

    The peripheral functionality is disabled but wakeup from Stop mode is possible through GPIO or asynchronous interrupt.

3.6 Low-power strategy

There are several ways to reduce power consumption on STM32H753xI:

- Decrease the dynamic power consumption by slowing down the system clocks even in Run mode and by individually clock gating the peripherals that are not used.
- Save power consumption when the CPU is idle, by selecting among the available low-power mode according to the user application needs. This allows achieving the best compromise between short startup time, low-power consumption, as well as available wakeup sources.

The devices feature several low-power modes:

- CSleep (CPU clock stopped)
- CStop (CPU sub-system clock stopped)
- DStop (Domain bus matrix clock stopped)
- Stop (System clock stopped)
- DStandby (Domain powered down)
- Standby (System powered down)

CSleep and CStop low-power modes are entered by the MCU when executing the WFI (Wait for Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex®-Mx core is set after returning from an interrupt service routine.

A domain can enter low-power mode (DStop or DStandby) when the processor, its subsystem and the peripherals allocated in the domain enter low-power mode.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally the system can enter Stop or Standby when all EXTI wakeup sources are cleared and the power domains are in DStop or DStandby mode.

Table 3. System vs domain low-power mode

System power mode	D1 domain power mode	D2 domain power mode	D3 domain power mode
Run	DRun/DStop/DStandby	DRun/DStop/DStandby	DRun
Stop	DStop/DStandby	DStop/DStandby	DStop
Standby	DStandby	DStandby	DStandby

3.7 Reset and clock controller (RCC)

The clock and reset controller is located in D3 domain. The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows to apply clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baudrate.

3.7.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - HSE clock: 4-50 MHz (generated from an external source) or 4-48 MHz(generated from a crystal/ceramic resonator)
  - LSE clock: 32.768 kHz

The RCC provides three PLLs: one for system clock, two for kernel clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

3.7.2 System reset sources

Power-on reset initializes all registers while system reset reinitializes the system except for the debug, part of the RCC and power controller status registers, as well as the backup power domain.

A system reset is generated in the following cases:

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Window watchdog
- Independent watchdog
- Software reset
- Low-power mode security reset
- Exit from Standby

3.8 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

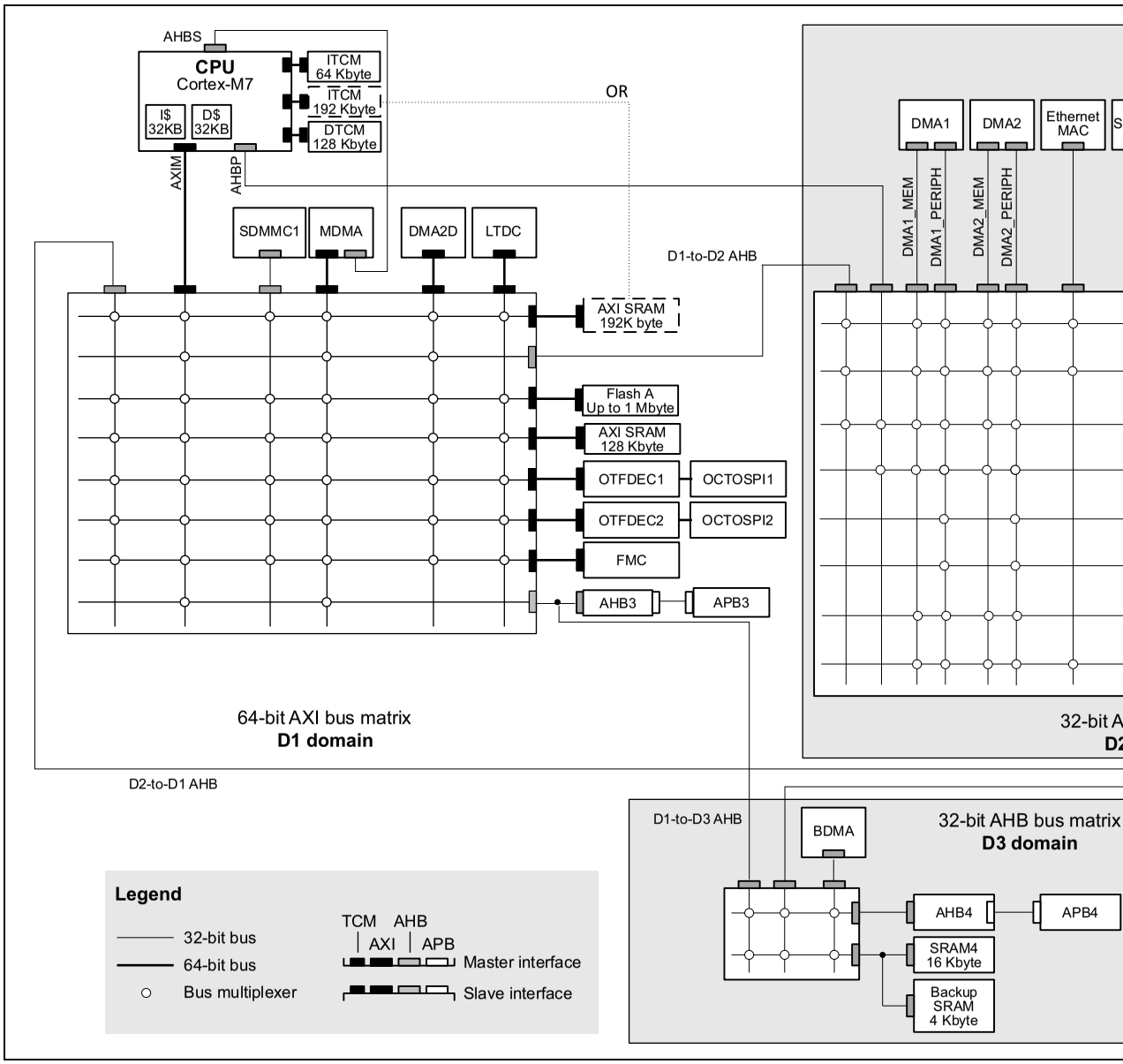
After reset, all GPIOs (except debug pins) are in Analog mode to reduce power consumption (refer to GPIOs register reset values in the device reference manual).

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.9 Bus-interconnect matrix

The devices feature an AXI bus matrix, two AHB bus matrices and bus bridges that allow interconnecting bus masters with bus slaves (see *Figure 3*).

Figure 3. STM32H753xI bus matrix



3.10 DMA controllers

The devices feature four DMA instances to unload CPU activity:

- A master direct memory access (MDMA)

  The MDMA is a high-speed DMA controller, which is in charge of all types of memory transfers (peripheral to memory, memory to memory, memory to peripheral), without any CPU action. It features a master AXI interface and a dedicated AHB interface to access Cortex®-M7 TCM memories.

  The MDMA is located in D1 domain. It is able to interface with the other DMA controllers located in D2 domain to extend the standard DMA capabilities, or can manage peripheral DMA requests directly.

  Each of the 16 channels can perform single block transfers, repeated block transfers and linked list transfers.
- Two dual-port DMAs (DMA1, DMA2) located in D2 domain, with FIFO and request router capabilities.
- One basic DMA (BDMA) located in D3 domain, with request router capabilities.

The DMA request router could be considered as an extension of the DMA controller. It routes the DMA peripheral requests to the DMA controller itself. This allowing managing the DMA requests with a high flexibility, maximizing the number of DMA requests that run concurrently, as well as generating DMA requests from peripheral output trigger or DMA event.

3.11 Chrom-ART Accelerator (DMA2D)

The Chrom-Art Accelerator (DMA2D) is a graphical accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables. The DMA2D also supports block based YCbCr to handle JPEG decoder output.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and handle up to 150 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved on interrupt entry, and restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.13 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processor, power domains and/or D3 domain from Stop mode.

The EXTI handles up to 89 independent event/interrupt lines split as 28 configurable events and 61 direct events .

Configurable events have dedicated pending flags, active edge selection, and software trigger capable.

Direct events provide interrupts or events from peripherals having a status flag.

3.14 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.15 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by 2.

3.16 Quad-SPI memory interface (QUADSPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual or Quad-SPI Flash memories. It supports both single and double datarate operations.

It can operate in any of the following modes:

- Direct mode through registers
- External Flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes of external Flash memory can be mapped, and 8-, 16- and 32-bit data accesses are supported as well as code execution.

The opcode and the frame format are fully programmable.

3.17 Analog-to-digital converters (ADCs)

The STM32H753xI devices embed three analog-to-digital converters, which resolution can be configured to 16, 14, 12, 10 or 8 bits.

Each ADC shares up to 20 external channels, performing conversions in the Single-shot or Scan mode. In Scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller, thus allowing to automatically transfer ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15, HRTIM1 and LPTIM1 timer.

3.18 Temperature sensor

STM32H753xI devices embed a temperature sensor that generates a voltage (V_{TS}) that varies linearly with the temperature. This temperature sensor is internally connected to ADC3_IN18. The conversion range is between 1.7 V and 3.6 V. It can measure the device junction temperature ranging from − 40 up to +125 °C.

The temperature sensor have a good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the System memory area, which is accessible in Read-only mode.

3.19 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers and the backup SRAM.

To optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} dropped below the PDR level.

The voltage on the VBAT pin could be provided by an external battery, a supercapacitor or directly by V_{DD}, in which case, the V_{BAT} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

3.20 Digital-to-analog converters (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- external triggers for conversion
- input voltage reference V_{REF+} or internal VREFBUF reference.

The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.21 Ultra-low-power comparators (COMP)

STM32H753xI devices embed two rail-to-rail comparators (COMP1 and COMP2). They feature programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) as well as selectable output polarity.

The reference voltage can be one of the following:

- An external I/O
- A DAC output channel
- An internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers, and be combined into a window comparator.

3.22 Operational amplifiers (OPAMP)

STM32H753xI devices embed two rail-to-rail operational amplifiers (OPAMP1 and OPAMP2) with external or internal follower routing and PGA capability.

The operational amplifier main features are:

- PGA with a non-inverting gain ranging of 2, 4, 8 or 16 or inverting gain ranging of -1, -3, -7 or -15
- One positive input connected to DAC
- Output connected to internal ADC
- Low input bias current down to 1 nA
- Low input offset voltage down to 1.5 mV
- Gain bandwidth up to 7.3 MHz

The devices embeds two operational amplifiers (OPAMP1 and OPAMP2) with two inputs and one output each. These three I/Os can be connected to the external pins, thus enabling any type of external interconnections. The operational amplifiers can be configured internally as a follower, as an amplifier with a non-inverting gain ranging from 2 to 16 or with inverting gain ranging from -1 to -15.

3.23 Digital filter for sigma-delta modulators (DFSDM)

The devices embed one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from internal ADC peripherals or microcontroller memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0..20 MHz
- alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: ADC data or memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM0)
- analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion

- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- "regular" or "injected" conversions:
  - "regular" conversions can be requested at any time or even in Continuous mode without having any impact on the timing of "injected" conversions
  - "injected" conversions for precise timing and with high conversion priority

Table 4. DFSDM implementation

DFSDM features	DFSDM1
Number of filters	4
Number of input transceivers/channels	8
Internal ADC parallel input	X
Number of external triggers	16
Regular channel information in identification register	X

3.24 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can achieve a data transfer rate up to 140 Mbyte/s using a 80 MHz pixel clock. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports Continuous mode or Snapshot (a single frame) mode
- Capability to automatically crop the image

3.25 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x64-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

3.26 JPEG Codec (JPEG)

The JPEG Codec can encode and decode a JPEG stream as defined in the ***ISO/IEC 10918-1*** specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Support for single greyscale component
- Ability to enable/disable header processing
- Fully synchronous design
- Configuration for High-speed decode mode

3.27 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

3.28 Cryptographic acceleration (CRYP and HASH)

The devices embed a cryptographic processor that supports the advanced cryptographic algorithms usually required to ensure confidentiality, authentication, data integrity and non-repudiation when exchanging messages with a peer:

- Encryption/Decryption
  - DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key
  - AES (advanced encryption standard): ECB, CBC, GCM, CCM, and CTR (Counter mode) chaining algorithms, 128, 192 or 256-bit key
- Universal HASH
  - SHA-1 and SHA-2 (secure HASH algorithms)
  - MD5
  - HMAC

The cryptographic accelerator supports DMA request generation.

3.29 Timers and watchdogs

The devices include one high-resolution timer, two advanced-control timers, ten general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

All timer counters can be frozen in Debug mode.

Table 5 compares the features of the advanced-control, general-purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz) (1)
High-resolution timer	HRTIM1	16-bit	Up	/1 /2 /4 (x2 x4 x8 x16 x32, with DLL)	Yes	10	Yes	480	480
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	120	240

Table 5. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz) (1)
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	120	240
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	120	240
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	120	240
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	120	240
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	120	240
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	120	240
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	120	240
Low-power timer	LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No	120	240

1. The maximum timer clock is up to 480 MHz depending on TIMPRE bit in the RCC_CFGR register and D2PRE1/2 bits in RCC_D2CFGR register.

3.29.1 High-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

The HRTIM1 timer is made of a digital kernel clocked at 480 MHz The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, Burst mode controller, Push-pull and Resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

3.29.2 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (Edge- or Center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.29.3 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32H753xI devices (see *Table 5* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The devices include 4 full-featured general-purpose timers: TIM2, TIM3, TIM4 and TIM5. TIM2 and TIM5 are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. All timers feature 4 independent channels for input capture/output compare, PWM or One-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  TIM2, TIM3, TIM4 and TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or One-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

3.29.4 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

3.29.5 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5)

The low-power timers have an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / One-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.29.6 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.29.7 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

3.29.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.30 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, Wakeup Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.31 Inter-integrated circuit interface (I2C)

STM32H753xI devices embed four I^2C interfaces.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and Master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

3.32 Universal synchronous/asynchronous receiver transmitter (USART)

STM32H753xI devices have four embedded universal synchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7 and UART8). Refer to *Table 6* for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire Half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 12.5 Mbit/s.

USART1, USART2, USART3 and USART6 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

The USARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the MCU from Stop mode.The wakeup from Stop mode is programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

All USART interfaces can be served by the DMA controller.

Table 6. USART features

USART modes/features(1)	USART1/2/3/6	UART4/5/7/8
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (Master/Slave)	X	-
Smartcard mode	X	-
Single-wire Half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wakeup from low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X
USART data length	7, 8 and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	16	

1. X = supported.

3.33 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART (LPUART1). The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wakeup from Stop mode are programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.34 Serial peripheral interfaces (SPI)/integrated interchip sound interfaces (I2S)

The devices feature up to six SPIs (SPI2S1, SPI2S2, SPI2S3, SPI4, SPI5 and SPI6) that allow communicating up to 150 Mbits/s in Master and Slave modes, in Half-duplex, Full-duplex and Simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. All SPI interfaces support NSS pulse mode, TI mode, Hardware CRC calculation and 8x 8-bit embedded Rx and Tx FIFOs with DMA capability.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in Master or Slave mode, in Simplex or Full-duplex communication mode, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in Master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I^2S interfaces support 16x 8-bit embedded Rx and Tx FIFOs with DMA capability.

3.35 Serial audio interfaces (SAI)

The devices embed 4 SAIs (SAI1, SAI2, SAI3 and SAI4) that allow designing many stereo or mono audio protocols such as I2S, LSB or MSB-justified, PCM/DSP, TDM or AC’97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio sub-blocks. Each block has it own clock generator and I/O line controller.
Audio sampling frequencies up to 192 kHz are supported.
In addition, up to 6 microphones can be supported thanks to an embedded PDM interface.
The SAI can work in master or slave configuration. The audio sub-blocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

3.36 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main SPDIFRX features are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

3.37 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- Full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.38 Management Data Input/Output (MDIO) slaves

The devices embed an MDIO slave interface it includes the following features:

- 32 MDIO Registers addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO Register write
  - MDIO Register read
  - MDIO protocol error
- Able to operate in and wake up from Stop mode

3.39 SD/SDIO/MMC card host interfaces (SDMMC)

Two SDMMC host interfaces are available. They support *MultiMediaCard System Specification Version 4.51* in three different databus modes: 1 bit (default), 4 bits and 8 bits.

Both interfaces support the *SD memory card specifications version 4.1.* and the *SDIO card specification version 4.0.* in two different databus modes: 1 bit (default) and 4 bits.

Each SDMMC host interface supports only one SD/SDIO/MMC card at any one time and a stack of MMC Version 4.51 or previous.

The SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the SRAM.

3.40 Controller area network (FDCAN1, FDCAN2)

The controller area network (CAN) subsystem consists of two CAN modules, a shared message RAM memory and a clock calibration unit.

Both CAN modules (FDCAN1 and FDCAN2) are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TT-FDCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10-Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TT-FDCAN). This message RAM is shared between the two FDCAN1 and FDCAN2 modules.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for both FDCAN1 and FDCAN2 from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

3.41 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed two USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. OTG-HS1 supports both full-speed and high-speed operations, while OTG-HS2 supports only full-speed operations. They both integrate the transceivers for full-speed operation (12 Mbit/s) and are able to operate from the internal HSI48 oscillator. OTG-HS1 features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG-HS1 in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripherals are compliant with the USB 2.0 specification and with the OTG 2.0 specification. They have software-configurable endpoint setting and supports suspend/resume. The USB OTG controllers require a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The main features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 9 bidirectional endpoints (including EP0)
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode (OTG_HS1 only)

  The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.42 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3.43 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The devices embed a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

3.44 Debug infrastructure

The devices offer a comprehensive set of debug and trace features to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- Arm® CoreSight™ debug and trace components

The debug can be controlled via a JTAG/Serial-wire debug access port, using industry standard debugging tools.

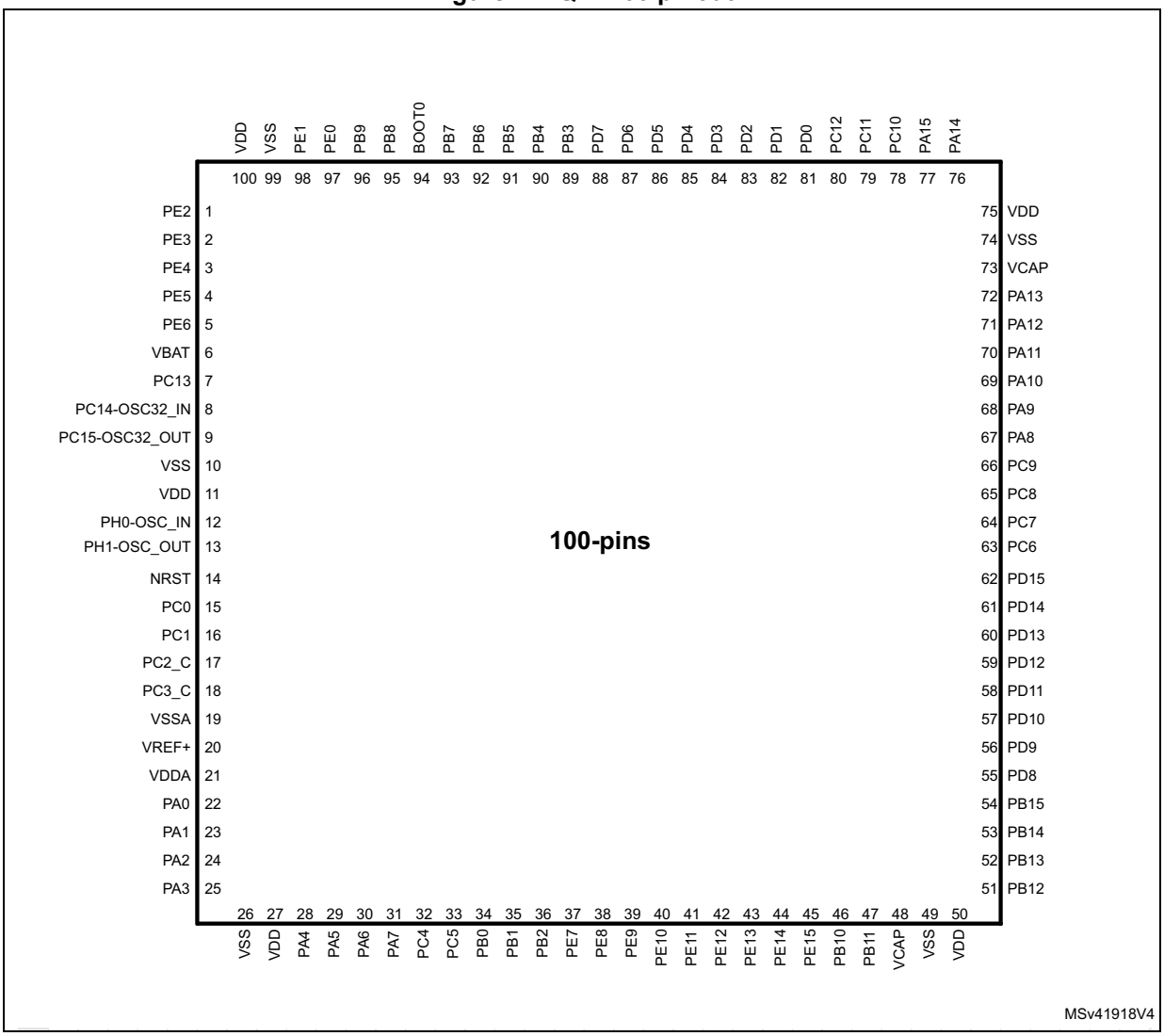
The trace port performs data capture for logging and analysis.

4 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

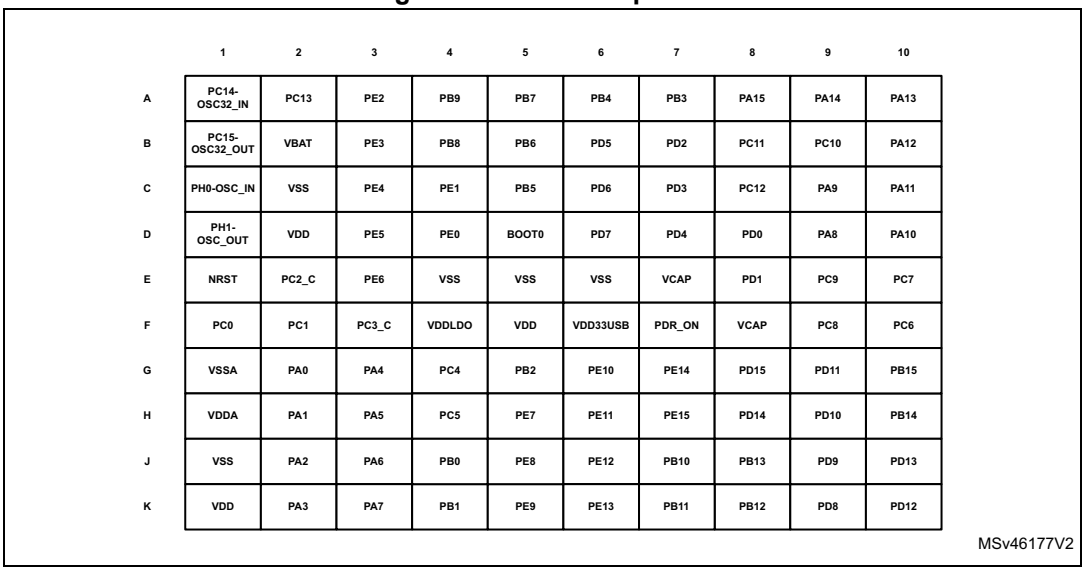
5 Pin descriptions

Figure 4. LQFP100 pinout



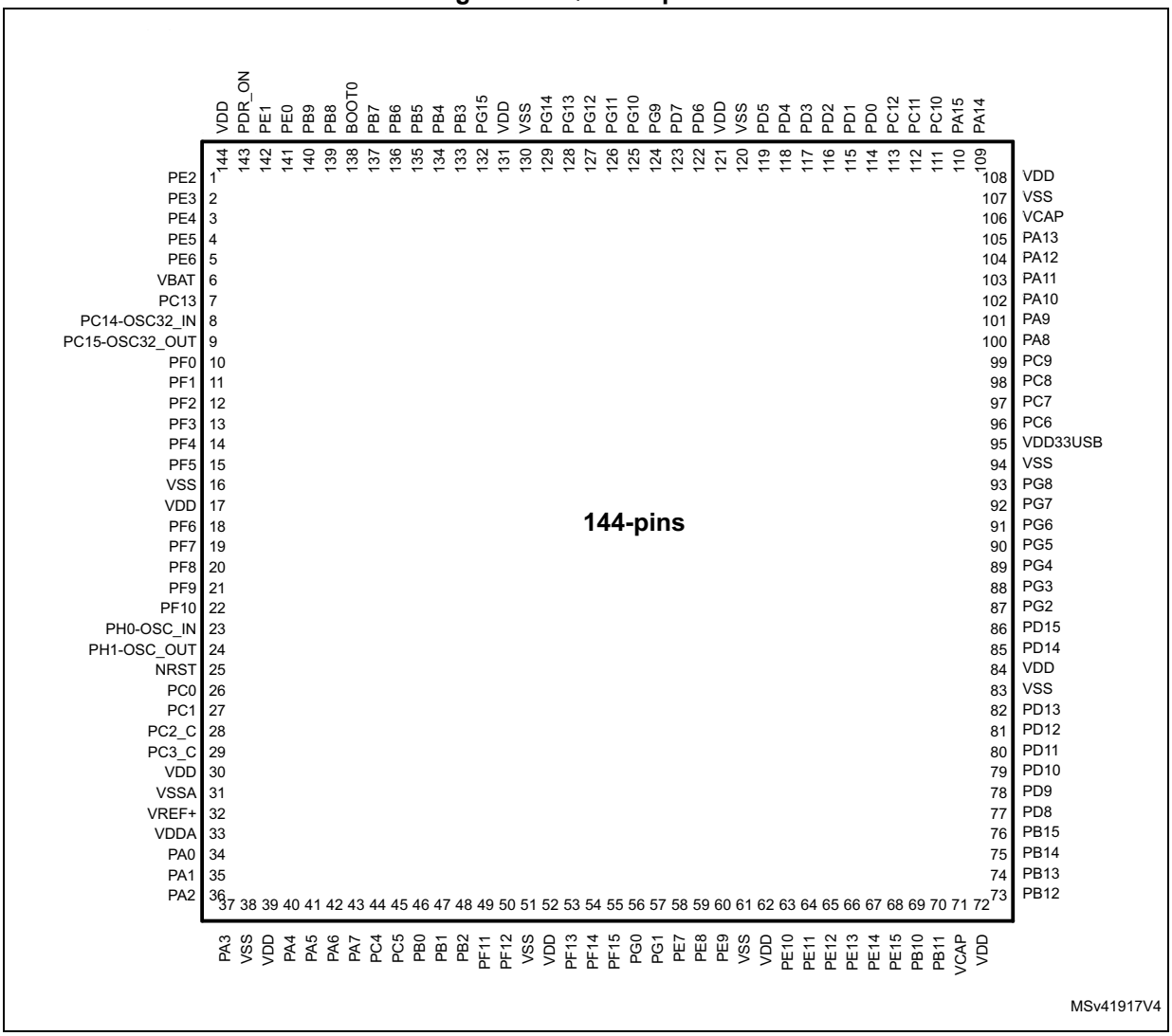
1. The above figure shows the package top view.

Figure 5. TFBGA100 pinout



1. The above figure shows the package top view.

Figure 6. LQFP144 pinout



1. The above figure shows the package top view.

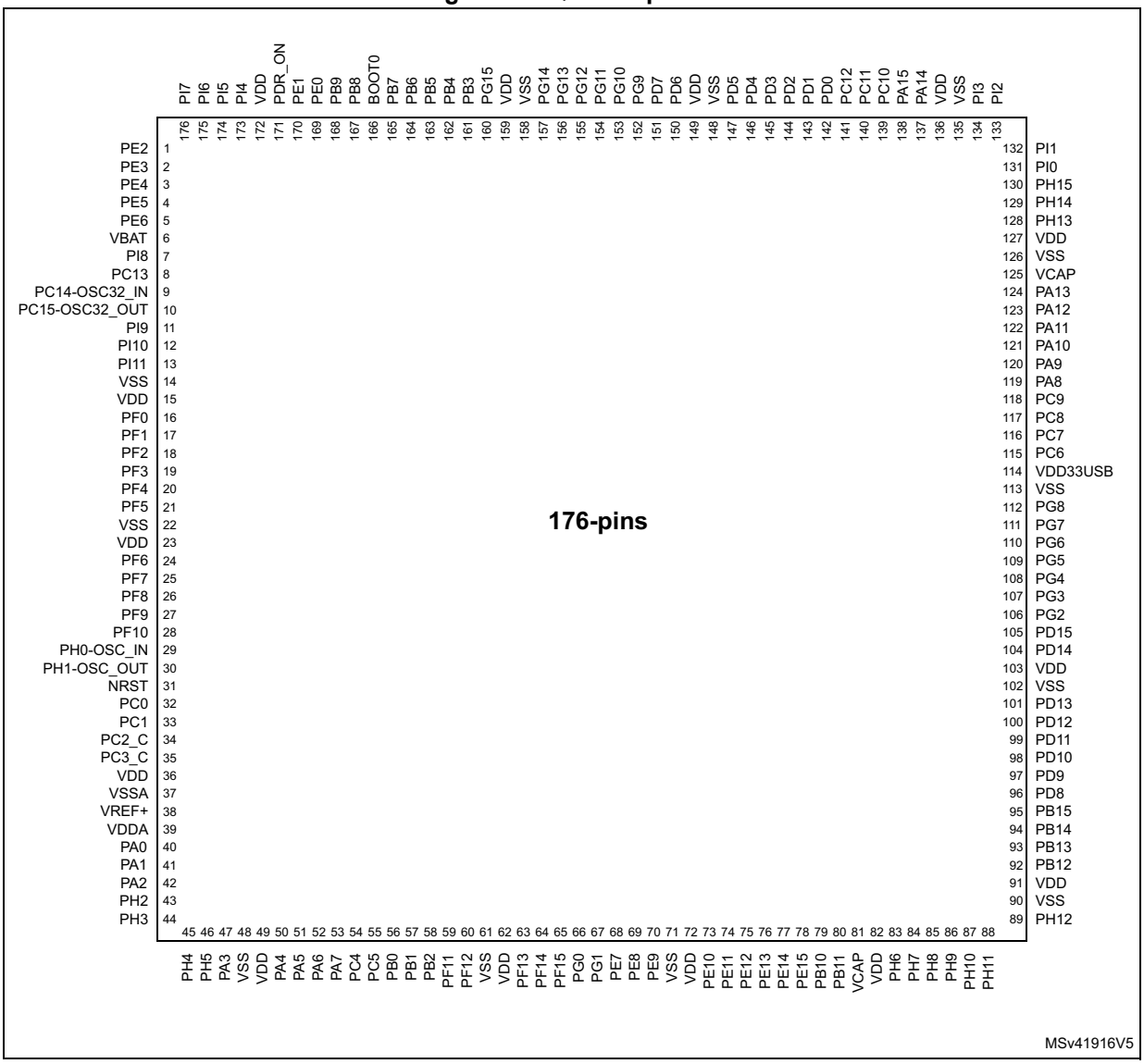
Figure 7. UFBGA169 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PE4	PE2	VDD	PI6	PB6	PI2	VDD	PG10	PD5	VDD	PC12	PC10	PI0
B	PC15-OSC32_OUT	PE3	VSS	VDDLDO	PB8	PB4	PI3	PG11	PD6	VSS	PC11	PA14	PI1
C	PC14-OSC32_IN	PE6	PE5	PDR_ON	PB9	PB5	PG14	PG9	PD4	PD1	PA15	VSS	VDD
D	VDD	VSS	PC13	PE1	PE0	PB7	PG13	PD7	PD3	PD0	PA13	VDDLDO	VCAP
E	PI11	PI7	VBAT	PF1	PF3	BOOT0	PG15	PG12	PD2	PA10	PA9	PA8	PA12
F	PI13	PI12	PF0	PF2	PF5	PF7	PB3	PG4	PC6	PC7	PC9	PC8	PA11
G	VDD	VSS	PF4	PF6	PF9	NRST	PF13	PE7	PG6	PG7	PG8	VDD50_USB	VDD33_USB
H	PH0-OSC_IN	PH1-OSC_OUT	PF10	PF8	PJ1	PA4	PF14	PE8	PG2	PG3	PG5	VSS	VDD
J	PC0	PC1	VSSA	PJ0	PA0	PA7	PF15	PE9	PE14	PD11	PD13	PD15	PD14
K	PC3_C	PC2_C	PH4	PA1	PA6	PC4	PG0	PE13	PH10	PH12	PD9	PD10	PD12
L	VDDA	VREF+	PH5	PA5	PB1	PB2	PG1	PE12	PB10	PH11	PB13	VSS	VDD
M	VDD	VSS	PH3	VSS	PB0	PF11	VSS	PE10	PB11	VDDLDO	VSS	PD8	PB15
N	PA2	PH2	PA3	VDD	PC5	PF12	VDD	PE11	PE15	VCAP	VDD	PB12	PB14

MSv45339V4

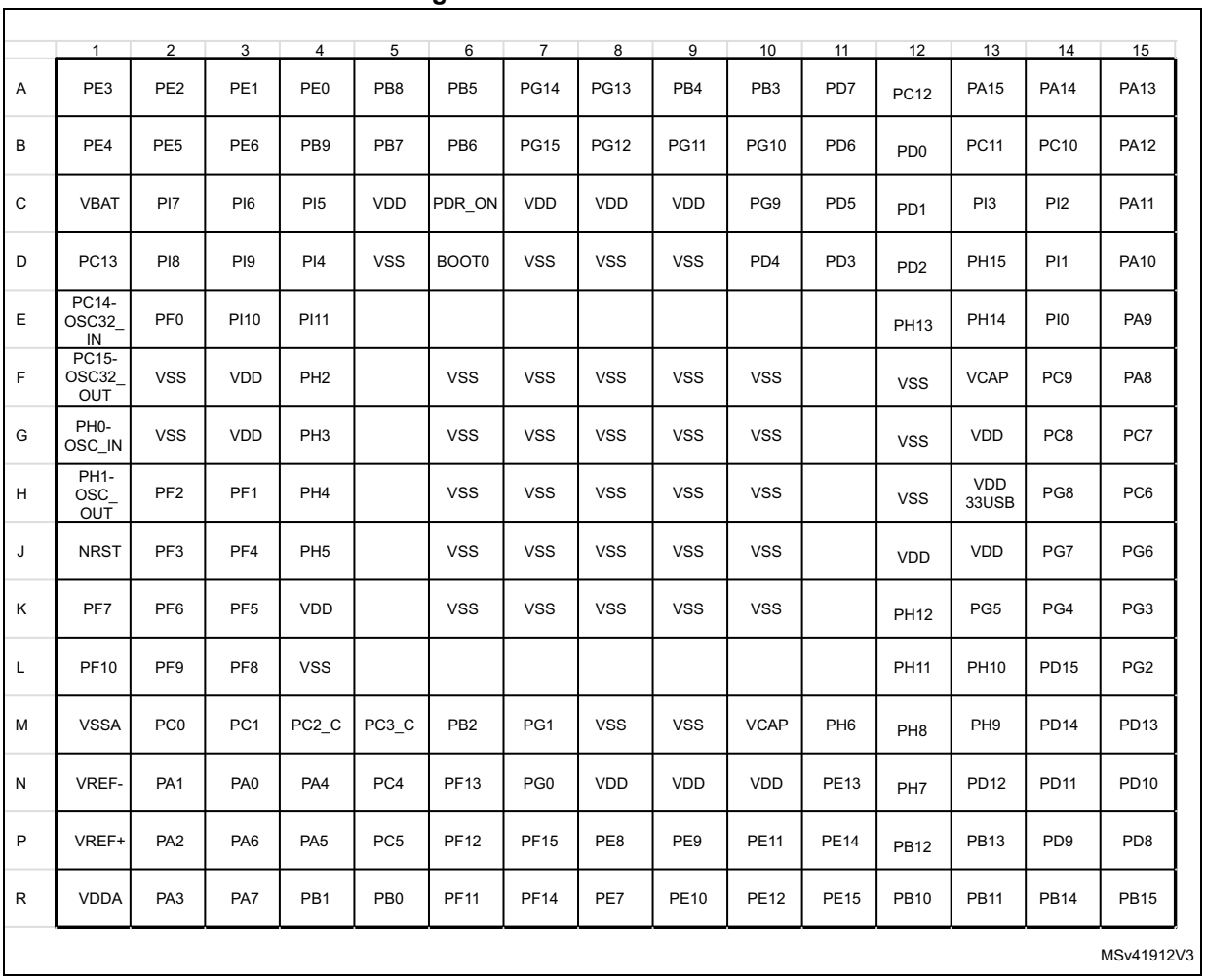
1. The above figure shows the package top view.

Figure 8. LQFP176 pinout



1. The above figure shows the package top view.

Figure 9. UFBGA176+25 ballout

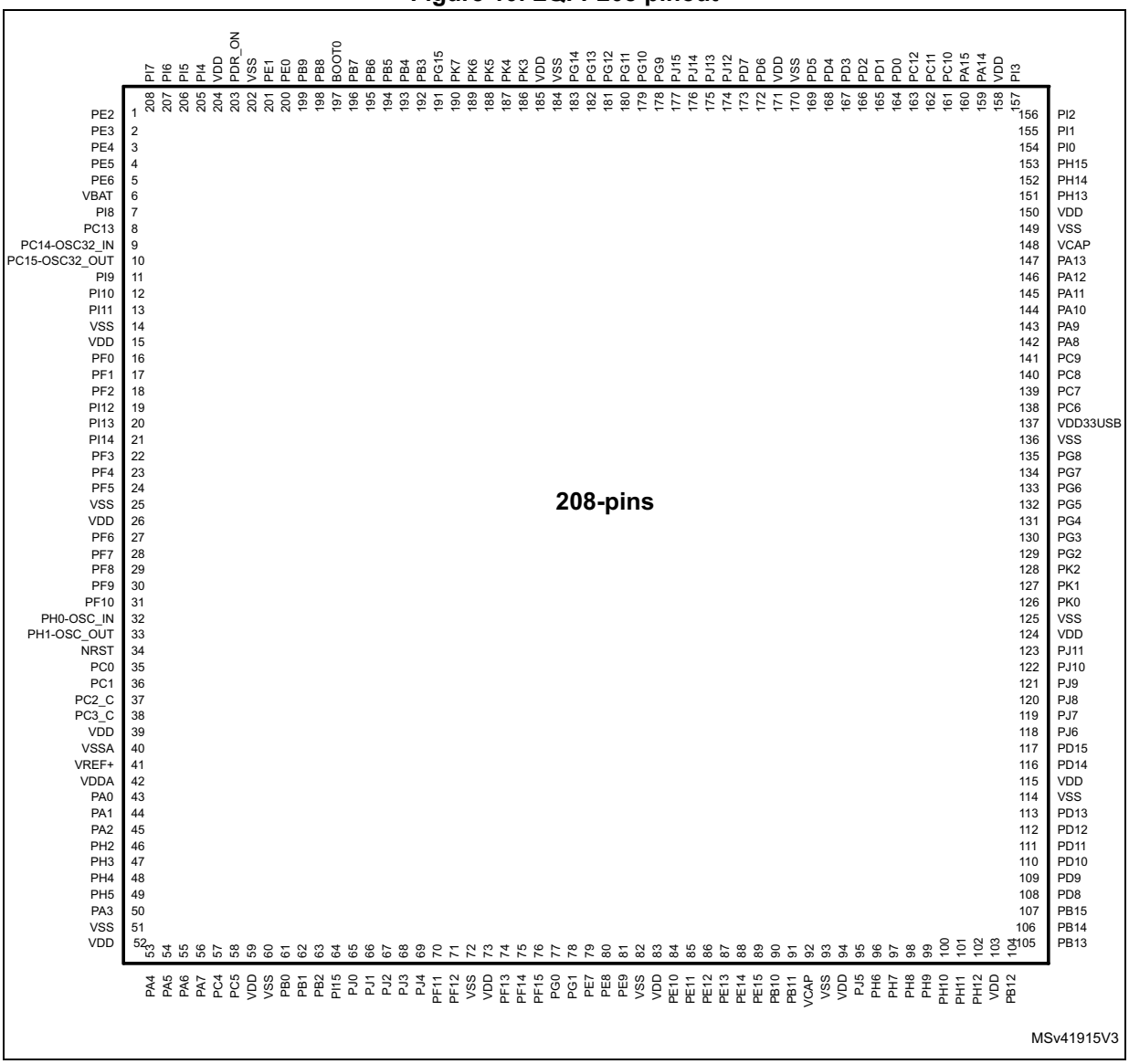


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	PDR_ON	VDD	VDD	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13	PI8	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14-OSC32_IN	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15-OSC32_OUT	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP	PC9	PA8
G	PH0-OSC_IN	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1-OSC_OUT	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD 33USB	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	VSS								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2_C	PC3_C	PB2	PG1	VSS	VSS	VCAP	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

MSv41912V3

1. The above figure shows the package top view.

Figure 10. LQFP208 pinout



1. The above figure shows the package top view.

Figure 11. TFBGA240+25 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	PI6	PI5	PI4	PB5	VDD LDO	VCAP	PK5	PG10	PG9	PD5	PD4	PC10	PA15	PI1	PI0	VSS
B	VBAT	VSS	PI7	PE1	PB6	VSS	PB4	PK4	PG11	PJ15	PD6	PD3	PC11	PA14	PI2	PH15	PH14
C	PC15-OSC32_OUT	PC14-OSC32_IN	PE2	PE0	PB7	PB3	PK6	PK3	PG12	VSS	PD7	PC12	VSS	PI3	PA13	VSS	VDD LDO
D	PE5	PE4	PE3	PB9	PB8	PG15	PK7	PG14	PG13	PJ14	PJ12	PD2	PD0	PA10	PA9	PH13	VCAP
E	NC(2)	PI9	PC13	PI8	PE6	VDD	PDR_ON	BOOT0	VDD	PJ13	VDD	PD1	PC8	PC9	PA8	PA12	PA11
F	VSS(3)	VSS(4)	PI10	PI11	VDD								PC7	PC6	PG8	PG7	VDD33 USB
G	PF2	VSS(4)	PF1	PF0	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG5	PG6	VSS	VDD50 USB
H	PI12	PI13	PI14	PF3	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG4	PG3	PG2	PK2
J	PH1-OSC_OUT	PH0-OSC_IN	VSS	PF5	PF4		VSS	VSS	VSS	VSS	VSS		VDD	PK0	PK1	VSS	VSS
K	NRST	PF6	PF7	PF8	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ11	VSS	NC	NC
L	VDDA	PC0	PF10	PF9	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ10	VSS	NC	NC
M	VREF+	PC1	PC2	PC3	VDD								VDD	PJ9	VSS	NC	NC
N	VREF-	PH2	PA2	PA1	PA0	PJ0	VDD	VDD	PE10	VDD	VDD	VDD	PJ8	PJ7	PJ6	VSS	NC
P	VSSA	PH3	PH4	PH5	PI15	PJ1	PF13	PF14	PE9	PE11	PB10	PB11	PH10	PH11	PD15	PD14	VDD
R	PC2_C	PC3_C	PA6	VSS	PA7	PB2	PF12	VSS	PF15	PE12	PE15	PJ5	PH9	PH12	PD11	PD12	PD13
T	PA0_C	PA1_C	PA5	PC4	PB1	PJ2	PF11	PG0	PE8	PE13	PH6	VSS	PH8	PB12	PB15	PD10	PD9
U	VSS	PA3	PA4	PC5	PB0	PJ3	PJ4	PG1	PE7	PE14	VCAP	VDD LDO	PH7	PB13	PB14	PD8	VSS

MSv41911V5

1. The above figure shows the package top view.
2. This ball should remain floating.
3. This ball should not remain floating. It can be connected to VSS or VDD. It is reserved for future use.
4. This ball should be connected to VSS.

Table 7. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
		ANA	Analog-only Input
I/O structure		FT	5 V tolerant I/O
		TT	3.3 V tolerant I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT and FT I/Os	
		_f	I2C FM+ option
		_a	analog option (supplied by V_{DDA})
		_u	USB option (supplied by $V_{DD33USB}$)
		_h	High-speed low-voltage I/O
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 8. Pin/ball definition

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
1	A3	1	A2	A2	1	1	C3	PE2	I/O	FT_h	-	TRACECLK, SAI1_CK1, SPI4_SCK, SAI1_MCLK_A, SAI4_MCLK_A, QUADSPI_BK1_IO2, SAI4_CK1, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	B3	2	B2	A1	2	2	D3	PE3	I/O	FT_h	-	TRACED0, TIM15_BKIN, SAI1_SD_B, SAI4_SD_B, FMC_A19, EVENTOUT	-
3	C3	3	A1	B1	3	3	D2	PE4	I/O	FT_h	-	TRACED1, SAI1_D2, DFSDM1_DATIN3, TIM15_CH1N, SPI4_NSS, SAI1_FS_A, SAI4_FS_A, SAI4_D2, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-
4	D3	4	C3	B2	4	4	D1	PE5	I/O	FT_h	-	TRACED2, SAI1_CK2, DFSDM1_CKIN3, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, SAI4_SCK_A, SAI4_CK2, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	E3	5	C2	B3	5	5	E5	PE6	I/O	FT_h	-	TRACED3, TIM1_BKIN2, SAI1_D1, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, SAI4_SD_A, SAI4_D1, SAI2_MCLK_B, TIM1_BKIN2_COMP12, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	M4	H10	-	-	A1	VSS	S	-	-	-	-
-	-	-	A3	-	-	-	-	VDD	S	-	-	-	-
6	B2	6	E3	C1	6	6	B1	VBAT	S	-	-	-	-
-	-	-	-	J6	-	-	B2	VSS	S	-	-	-	-
-	-	-	-	D2	7	7	E4	PI8	I/O	FT	-	EVENTOUT	RTC_TAMP2/ WKUP2
7	A2	7	D3	D1	8	8	E3	PC13	I/O	FT	-	EVENTOUT	RTC_TAMP1/ RTC_TS/ WKUP3
-	-	-	-	J7	-	-	B6	VSS	S	-	-	-	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
8	A1	8	C1	E1	9	9	C2	PC14-OSC32_IN (OSC32_IN)(1)	I/O	FT	-	EVENTOUT	OSC32_IN
9	B1	9	B1	F1	10	10	C1	PC15-OSC32_OUT (OSC32_OUT)(1)	I/O	FT	-	EVENTOUT	OSC32_OUT
-	-	-	-	D3	11	11	E2	PI9	I/O	FT_h	-	UART4_RX, FDCAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	-	-	E3	12	12	F3	PI10	I/O	FT_h	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	
-	-	-	E1	E4	13	13	F4	PI11	I/O	FT	-	LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT	WKUP4
-	C2	-	D2	F2	14	14	A17	VSS	S	-	-	-	-
-	D2	-	D1	F3	15	15	E6	VDD	S	-	-	-	-
-	-	-	-	-	-	-	E1(2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	F1(3)	VSS	S	-	-	-	-
-	-	-	-	-	-	-	G2(4)	VSS	S	-	-	-	-
-	-	10	F3	E2	16	16	G4	PF0	I/O	FT_f	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	11	E4	H3	17	17	G3	PF1	I/O	FT_f	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	12	F4	H2	18	18	G1	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	F2	-	-	19	H1	PI12	I/O	FT	-	LCD_HSYNC, EVENTOUT	-
-	-	-	F1	-	-	20	H2	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	-	-	21	H3	PI14	I/O	FT_h	-	LCD_CLK, EVENTOUT	-
-	-	13	E5	J2	19	22	H4	PF3	I/O	FT_ha	-	FMC_A3, EVENTOUT	ADC3_INP5
-	-	14	G3	J3	20	23	J5	PF4	I/O	FT_ha	-	FMC_A4, EVENTOUT	ADC3_INN5, ADC3_INP9

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	15	F5	K3	21	24	J4	PF5	I/O	FT_ha	-	FMC_A5, EVENTOUT	ADC3_INP4
10	-	16	B10	G2	22	25	C10	VSS	S	-	-	-	-
11	-	17	G1	G3	23	26	E9	VDD	S	-	-	-	-
-	-	18	G4	K2	24	27	K2	PF6	I/O	FT_ha	-	TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, SAI4_SD_B, QUADSPI_BK1_IO3, EVENTOUT	ADC3_INN4, ADC3_INP8
-	-	19	F6	K1	25	28	K3	PF7	I/O	FT_ha	-	TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, SAI4_MCLK_B, QUADSPI_BK1_IO2, EVENTOUT	ADC3_INP3
-	-	20	H4	L3	26	29	K4	PF8	I/O	FT_ha	-	TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS/UART7_DE, SAI4_SCK_B, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_INN3, ADC3_INP7
-	-	21	G5	L2	27	30	L4	PF9	I/O	FT_ha	-	TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, SAI4_FS_B, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_INP2
-	-	22	H3	L1	28	31	L3	PF10	I/O	FT_ha	-	TIM16_BKIN, SAI1_D3, QUADSPI_CLK, SAI4_D3, DCMI_D11, LCD_DE, EVENTOUT	ADC3_INN2, ADC3_INP6
12	C1	23	H1	G1	29	32	J2	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
13	D1	24	H2	H1	30	33	J1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
14	E1	25	G6	J1	31	34	K1	NRST	I/O	RST	-	-	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
15	F1	26	J1	M2	32	35	L2	PC0	I/O	FT_a	-	DFSDM1_CKIN0, DFSDM1_DATIN4, SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC123_ INP10
16	F2	27	J2	M3	33	36	M2	PC1	I/O	FT_ ha	-	TRACED0, SAI1_D1, DFSDM1_DATIN0, DFSDM1_CKIN4, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, SAI4_SD_A, SDMMC2_CK, SAI4_D1, ETH_MDC, MDIOS_MDC, EVENTOUT	ADC123_ INN10, ADC123_ INP11, RTC_TAMP3/W KUP5
-	-	-	-	-	-	-	M3(5)	PC2	I/O	FT_a	-	CDSLEEP, DFSDM1_CKIN1, SPI2_MISO/I2S2_SDI, DFSDM1_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_ INN11, ADC123_ INP12
17 (6)	E2(6)	28(6)	K2(6)	M4(6)	34(6)	37(6)	R1(5)	PC2_C	ANA	TT_a	-		ADC3_INN1, ADC3_INP0
-	-	-	-	-	-	-	M4(5)	PC3	I/O	FT_a	-	CSLEEP, DFSDM1_DATIN1, SPI2_MOSI/I2S2_SDO, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC12_INN12, ADC12_INP13
18 (6)	F3(6)	29(6)	K1(6)	M5(6)	35(6)	38(6)	R2(5)	PC3_C	ANA	TT_a	-		ADC3_INP1
-	F5	30	-	G3	36	39	E11	VDD	S	-	-	-	-
-	E6	-	B3	J10	-	-	C13	VSS	S	-	-	-	-
19	G1	31	J3	M1	37	40	P1	VSSA	S	-	-	-	-
-	-	-	-	N1	-	-	N1	VREF-	S	-	-	-	-
20	-(7)	32	L2	P1	38	41	M1	VREF+	S	-	-	-	-
21	H1	33	L1	R1	39	42	L1	VDDA	S	-	-	-	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
22	G2	34	J5	N3	40	43	N5(5)	PA0	I/O	FT_a	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, TIM15_BKIN, USART2_CTS/USART2_NSS, UART4_TX, SDMMC2_CMD, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC1_INP16, WKUP0
-	-	-	-	-	-	-	T1(5)	PA0_C	ANA	TT_a	-		ADC12_INN1, ADC12_INP0
23	H2	35	K4	N2	41	44	N4(5)	PA1	I/O	FT_ha	-	TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, USART2_RTS/USART2_DE, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_INN16, ADC1_INP17
-	-	-	-	-	-	-	T2(5)	PA1_C	ANA	TT_a	-		ADC12_INP1
24	J2	36	N1	P2	42	45	N3	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, LPTIM4_OUT, TIM15_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC12_INP14, WKUP1
-	-	-	N2	F4	43	46	N2	PH2	I/O	FT_ha	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	ADC3_INP13
-	K1	-	M1	-	-	-	F5	VDD	S	-	-	-	-
-	J1	-	M7	J8	-	-	C16	VSS	S	-	-	-	-
-	-	-	M3	G4	44	47	P2	PH3	I/O	FT_ha	-	QUADSPI_BK2_IO1, SAI2_MCLK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	ADC3_INN13, ADC3_INP14
-	-	-	K3	H4	45	48	P3	PH4	I/O	FT_fa	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	ADC3_INN14, ADC3_INP15
-	-	-	L3	J4	46	49	P4	PH5	I/O	FT_fa	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	ADC3_INN15, ADC3_INP16

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
25	K2	37	N3	R2	47	50	U2	PA3	I/O	FT_ha	-	TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC12_INP15
26	-	38	G2	K6	-	51	F2(4)	VSS	S	-	-	-	-
-	-	-	-	L4	48	-	-	VSS	S	-	-	-	-
27	-	39	-	K4	49	52	G5	VDD	S	-	-	-	-
28	G3	40	H6	N4	50	53	U3	PA4	I/O	TT_a	-	D1PWREN, TIM5_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_INP18, DAC1_OUT1
29	H3	41	L4	P4	51	54	T3	PA5	I/O	TT_ha	-	D2PWREN, TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_INN18, ADC12_INP19, DAC1_OUT2
30	J3	42	K5	P3	52	55	R3	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO/I2S1_SDI, SPI6_MISO, TIM13_CH1, TIM8_BKIN_COMP12, MDIOS_MDC, TIM1_BKIN_COMP12, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_INP3
31	K3	43	J6	R3	53	56	R5	PA7	I/O	TT_a	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SDO, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_INN3, ADC12_INP7, OPAMP1_VINM

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
32	G4	44	K6	N5	54	57	T4	PC4	I/O	TT_a	-	DFSDM1_CKIN2, I2S1_MCK, SPDIFRX1_IN3, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC12_INP4, OPAMP1_VOUT, COMP1_INM
33	H4	45	N5	P5	55	58	U4	PC5	I/O	TT_a	-	SAI1_D3, DFSDM1_DATIN2, SPDIFRX1_IN4, SAI4_D3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, COMP1_OUT, EVENTOUT	ADC12_INN4, ADC12_INP8, OPAMP1_VINM
-	-	-	N4	-	-	59	G13	VDD	S	-	-	-	-
-	-	-	H12	J9	-	60	R4	VSS	S	-	-	-	-
34	J4	46	M5	R5	56	61	U5	PB0	I/O	FT_a	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC12_INN5, ADC12_INP9, OPAMP1_VINP, COMP1_INP
35	K4	47	L5	R4	57	62	T5	PB1	I/O	TT_a	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC12_INP5, COMP1_INM
36	G5	48	L6	M6	58	63	R6	PB2	I/O	FT_ha	-	RTC_OUT, SAI1_D1, DFSDM1_CKIN1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, SAI4_SD_A, QUADSPI_CLK, SAI4_D1, EVENTOUT	COMP1_INP
-	-	-	-	-	-	64	P5	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	J4	-	-	65	N6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	H5	-	-	66	P6	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	-	-	67	T6	PJ2	I/O	FT	-	LCD_R3, EVENTOUT	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	-	-	68	U6	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	-	-	69	U7	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	-	49	M6	R6	59	70	T7	PF11	I/O	FT_a	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	ADC1_INP2
-	-	50	N6	P6	60	71	R7	PF12	I/O	FT_ha	-	FMC_A6, EVENTOUT	ADC1_INN2, ADC1_INP6
-	-	51	M11	M8	61	72	J3	VSS	S	-	-	-	-
-	-	52	-	N8	62	73	H5	VDD	S	-	-	-	-
-	-	53	G7	N6	63	74	P7	PF13	I/O	FT_ha	-	DFSDM1_DATIN6, I2C4_SMBA, FMC_A7, EVENTOUT	ADC2_INP2
-	-	54	H7	R7	64	75	P8	PF14	I/O	FT_fha	-	DFSDM1_CKIN6, I2C4_SCL, FMC_A8, EVENTOUT	ADC2_INN2, ADC2_INP6
-	-	55	J7	P7	65	76	R9	PF15	I/O	FT_fh	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	-	56	K7	N7	66	77	T8	PG0	I/O	FT_h	-	FMC_A10, EVENTOUT	-
-	-	-	M2	F6	-	-	J16	VSS	S	-	-	-	-
-	-	-	A10	-	-	-	H13	VDD	S	-	-	-	-
-	-	57	L7	M7	67	78	U8	PG1	I/O	TT_h	-	FMC_A11, EVENTOUT	OPAMP2_VINM
37	H5	58	G8	R8	68	79	U9	PE7	I/O	TT_ha	-	TIM1_ETR, DFSDM1_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4/FMC_DA4, EVENTOUT	OPAMP2_VOUT, COMP2_INM
38	J5	59	H8	P8	69	80	T9	PE8	I/O	TT_ha	-	TIM1_CH1N, DFSDM1_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5/FMC_DA5, COMP2_OUT, EVENTOUT	OPAMP2_VINM
39	K5	60	J8	P9	70	81	P9	PE9	I/O	TT_ha	-	TIM1_CH1, DFSDM1_CKOUT, UART7_RTS/UART7_DE, QUADSPI_BK2_IO2, FMC_D6/FMC_DA6, EVENTOUT	OPAMP2_VINP, COMP2_INP

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	61	C12	M9	71	82	J17	VSS	S	-	-	-	-
-	-	62	C13	N9	72	83	J13	VDD	S	-	-	-	-
40	G6	63	M8	R9	73	84	N9	PE10	I/O	FT_ha	-	TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7/FMC_DA7, EVENTOUT	COMP2_INM
41	H6	64	N8	P10	74	85	P10	PE11	I/O	FT_ha	-	TIM1_CH2, DFSDM1_CKIN4, SPI4_NSS, SAI2_SD_B, FMC_D8/FMC_DA8, LCD_G3, EVENTOUT	COMP2_INP
42	J6	65	L8	R10	75	86	R10	PE12	I/O	FT_h	-	TIM1_CH3N, DFSDM1_DATIN5, SPI4_SCK, SAI2_SCK_B, FMC_D9/FMC_DA9, COMP1_OUT, LCD_B4, EVENTOUT	-
43	K6	66	K8	N11	76	87	T10	PE13	I/O	FT_h	-	TIM1_CH3, DFSDM1_CKIN5, SPI4_MISO, SAI2_FS_B, FMC_D10/FMC_DA10, COMP2_OUT, LCD_DE, EVENTOUT	-
-	-	-	L12	F7	-	-	T12	VSS	S	-	-	-	-
-	-	-	H13	-	-	-	K13	VDD	S	-	-	-	-
44	G7	67	J9	P11	77	88	U10	PE14	I/O	FT_h	-	TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11/FMC_DA11, LCD_CLK, EVENTOUT	-
45	H7	68	N9	R11	78	89	R11	PE15	I/O	FT_h	-	TIM1_BKIN, FMC_D12/FMC_DA12, TIM1_BKIN_COMP12/ COMP_TIM1_BKIN, LCD_R7, EVENTOUT	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
46	J7	69	L9	R12	79	90	P11	PB10	I/O	FT_f	-	TIM2_CH3, HRTIM_SCOUT, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM1_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
47	K7	70	M9	R13	80	91	P12	PB11	I/O	FT_f	-	TIM2_CH4, HRTIM_SCIN, LPTIM2_ETR, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT	-
48	F8	71	N10	M10	81	92	U11	VCAP	S	-	-	-	-
49	E4	-	-	K7	-	93	-	VSS	S	-	-	-	-
-	-	-	M10	-	-	-	U12	VDDLDO (8)	S	-	-	-	-
50	-	72	M1	N10	82	94	L13	VDD	S	-	-	-	-
-	-	-	-	-	-	95	R12	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	-	-	M11	83	96	T11	PH6	I/O	FT	-	TIM12_CH1, I2C2_SMBA, SPI5_SCK, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	-	-	N12	84	97	U13	PH7	I/O	FT_fa	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-
-	-	-	-	M12	85	98	T13	PH8	I/O	FT_fha	-	TIM5_ETR, I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	-	-	F8	-	-	-	VSS	S	-	-	-	-
-	-	-	L13	-	-	-	M13	VDD	S	-	-	-	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	M13	86	99	R13	PH9	I/O	FT_h	-	TIM12_CH2, I2C3_SMBA, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	-	K9	L13	87	100	P13	PH10	I/O	FT_h	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	-	L10	L12	88	101	P14	PH11	I/O	FT_fh	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	-	K10	K12	89	102	R14	PH12	I/O	FT_fh	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	-	-	H12	90	-	N16	VSS	S	-	-	-	-
-	-	-	N11	J12	91	103	P17	VDD	S	-	-	-	-
51	K8	73	N12	P12	92	104	T14	PB12[9]	I/O	FT_u	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, FDCAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, TIM1_BKIN_COMP12, UART5_RX, EVENTOUT	
52	J8	74	L11	P13	93	105	U14	PB13[9]	I/O	FT_u	-	TIM1_CH1N, LPTIM2_OUT, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS/USART3_NSS, FDCAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, UART5_TX, EVENTOUT	OTG_HS_VBUS

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
53	H10	75	N13	R14	94	106	U15	PB14	I/O	FT_u	-	TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, DFSDM1_DATIN2, USART3_RTS/ USART3_DE, UART4_RTS/UART4_DE, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
54	G10	76	M13	R15	95	107	T15	PB15	I/O	FT_u	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SDO, DFSDM1_CKIN2, UART4_CTS, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-
55	K9	77	M12	P15	96	108	U16	PD8	I/O	FT_h	-	DFSDM1_CKIN3, SAI3_SCK_B, USART3_TX, SPDIFRX1_IN2, FMC_D13/FMC_DA13, EVENTOUT	-
56	J9	78	K11	P14	97	109	T17	PD9	I/O	FT_h	-	DFSDM1_DATIN3, SAI3_SD_B, USART3_RX, FMC_D14/FMC_DA14, EVENTOUT	-
57	H9	79	K12	N15	98	110	T16	PD10	I/O	FT_h	-	DFSDM1_CKOUT, SAI3_FS_B, USART3_CK, FMC_D15/FMC_DA15, LCD_B3, EVENTOUT	-
-	-	-	N7	-	-	-	N12	VDD	S	-	-	-	-
-	-	-	-	F9	-	-	U17	VSS	S	-	-	-	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
58	G9	80	J10	N14	99	111	R15	PD11	I/O	FT_h	-	LPTIM2_IN2, I2C4_SMBA, USART3_CTS/USART3_NSS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16, EVENTOUT	-
59	K10	81	K13	N13	100	112	R16	PD12	I/O	FT_fh	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I2C4_SCL, USART3_RTS/USART3_DE, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17, EVENTOUT	-
60	J10	82	J11	M15	101	113	R17	PD13	I/O	FT_fh	-	LPTIM1_OUT, TIM4_CH2, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	-	83	-	K8	102	114	-	VSS	S	-	-	-	-
-	-	84	-	J13	103	115	N11	VDD	S	-	-	-	-
61	H8	85	J13	M14	104	116	P16	PD14	I/O	FT_h	-	TIM4_CH3, SAI3_MCLK_B, UART8_CTS, FMC_D0/FMC_DA0, EVENTOUT	-
62	G8	86	J12	L14	105	117	P15	PD15	I/O	FT_h	-	TIM4_CH4, SAI3_MCLK_A, UART8_RTS/UART8_DE, FMC_D1/FMC_DA1, EVENTOUT	-
-	-	-	-	-	-	118	N15	PJ6	I/O	FT	-	TIM8_CH2, LCD_R7, EVENTOUT	-
-	-	-	-	-	-	119	N14	PJ7	I/O	FT	-	TRGIN, TIM8_CH2N, LCD_G0, EVENTOUT	-
-	-	-	-	-	-	-	N10	VDD	S		-		-
-	-	-	-	F10	-	-	R8	VSS	S		-		-
-	-	-	-	-	-	120	N13	PJ8	I/O	FT	-	TIM1_CH3N, TIM8_CH1, UART8_TX, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	121	M14	PJ9	I/O	FT	-	TIM1_CH3, TIM8_CH1N, UART8_RX, LCD_G2, EVENTOUT	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	-	-	122	L14	PJ10	I/O	FT	-	TIM1_CH2N, TIM8_CH2, SPI5_MOSI, LCD_G3, EVENTOUT	-
-	-	-	-	-	-	123	K14	PJ11	I/O	FT	-	TIM1_CH2, TIM8_CH2N, SPI5_MISO, LCD_G4, EVENTOUT	-
-	-	-	-	-	-	124	N8	VDD	S		-		-
-	-	-	-	G6	-	125	U1	VSS	S	-	-	-	-
-	-	-	-	-	-	-	N17 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	M16 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	M17 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	K15	VSS	S	-	-	-	-
-	-	-	-	-	-	-	L16(2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	L17(2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	K16 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	K17 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	L15	VSS	S	-	-	-	-
-	-	-	-	-	-	126	J14	PK0	I/O	FT	-	TIM1_CH1N, TIM8_CH3, SPI5_SCK, LCD_G5, EVENTOUT	-
-	-	-	-	-	-	127	J15	PK1	I/O	FT	-	TIM1_CH1, TIM8_CH3N, SPI5_NSS, LCD_G6, EVENTOUT	-
-	-	-	-	-	-	128	H17	PK2	I/O	FT	-	TIM1_BKIN, TIM8_BKIN, TIM8_BKIN_COMP12, TIM1_BKIN_COMP12, LCD_G7, EVENTOUT	-
-	-	87	H9	L15	106	129	H16	PG2	I/O	FT_h	-	TIM8_BKIN, TIM8_BKIN_COMP12, FMC_A12, EVENTOUT	-
-	-	88	H10	K15	107	130	H15	PG3	I/O	FT_h	-	TIM8_BKIN2, TIM8_BKIN2_COMP12, FMC_A13, EVENTOUT	-
-	-	-	-	G7	-	-	-	VSS	S	-	-	-	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	-	-	-	N7	VDD	S	-	-	-	-
-	-	89	F8	K14	108	131	H14	PG4	I/O	FT_h	-	TIM1_BKIN2, TIM1_BKIN2_COMP12, FMC_A14/FMC_BA0, EVENTOUT	-
-	-	90	H11	K13	109	132	G14	PG5	I/O	FT_h	-	TIM1_ETR, FMC_A15/FMC_BA1, EVENTOUT	-
-	-	91	G9	J15	110	133	G15	PG6	I/O	FT_h	-	TIM17_BKIN, HRTIM_CHE1, QUADSPI_BK1_NCS, FMC_NE3, DCMI_D12, LCD_R7, EVENTOUT	-
-	-	92	G10	J14	111	134	F16	PG7	I/O	FT_h	-	HRTIM_CHE2, SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-
-	-	93	G11	H14	112	135	F15	PG8	I/O	FT_h	-	TIM8_ETR, SPI6_NSS, USART6_RTS/USART6_DE, SPDIFRX1_IN3, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	-	94	-	G12	113	136	G16	VSS	S	-	-	-	-
-	-	-	G12	-	-	-	G17	VDD50 USB(10)	S	-	-	-	-
-	F6	95	G13	H13	114	137	F17	VDD33 USB	S	-	-	-	-
-	-	-	-	-	-	-	M5	VDD	S	-	-	-	-
63	F10	96	F9	H15	115	138	F14	PC6	I/O	FT_h	-	HRTIM_CHA1, TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, I2S2_MCK, USART6_TX, SDMMC1_D0DIR, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	SWPMI_IO

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
64	E10	97	F10	G15	116	139	F13	PC7	I/O	FT_h	-	TRGIO, HRTIM_CHA2, TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, I2S3_MCK, USART6_RX, SDMMC1_D123DIR, FMC_NE1, SDMMC2_D7, SWPMI_TX, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-
65	F9	98	F12	G14	117	140	E13	PC8	I/O	FT_h	-	TRACED1, HRTIM_CHB1, TIM3_CH3, TIM8_CH3, USART6_CK, UART5_RTS/UART5_DE, FMC_NE2/FMC_NCE, SWPMI_RX, SDMMC1_D0, DCMI_D2, EVENTOUT	-
66	E9	99	F11	F14	118	141	E14	PC9	I/O	FT_fh	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, LCD_G3, SWPMI_SUSPEND, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT	-
-	-	-	-	G8	-	-	-	VSS	S	-	-		-
-	-	-	-	-	-	-	L5	VDD	S	-	-		-
67	D9	100	E12	F15	119	142	E15	PA8	I/O	FT_fha	-	MCO1, TIM1_CH1, HRTIM_CHB2, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, UART7_RX, TIM8_BKIN2_COMP12, LCD_B3, LCD_R6, EVENTOUT	-
68	C9	101	E11	E15	120	143	D15	PA9	I/O	FT_u	-	TIM1_CH2, HRTIM_CHC1, LPUART1_TX, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, LCD_R5, EVENTOUT	OTG_FS_VBUS

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
69	D10	102	E10	D15	121	144	D14	PA10	I/O	FT_u	-	TIM1_CH3, HRTIM_CHC2, LPUART1_RX, USART1_RX, OTG_FS_ID, MDIOS_MDIO, LCD_B4, DCMI_D1, LCD_B1, EVENTOUT	-
70	C10	103	F13	C15	122	145	E17	PA11	I/O	FT_u	-	TIM1_CH4, HRTIM_CHD1, LPUART1_CTS, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS/USART1_NSS, FDCAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-
71	B10	104	E13	B15	123	146	E16	PA12	I/O	FT_u	-	TIM1_ETR, HRTIM_CHD2, LPUART1_RTS/LPUART1_DE, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS/USART1_DE, SAI2_FS_B, FDCAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	A10	105	D11	A15	124	147	C15	PA13 (JTMS/SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	E7	106	D13	F13	125	148	D17	VCAP	S	-	-	-	-
74	E5	107	-	F12	126	149	-	VSS	S	-	-	-	-
-	-	-	D12	-	-	-	C17	VDDLDO (8)		-	-	-	-
75	-	108	-	G13	127	150	K5	VDD	S	-	-	-	-
-	-	-	-	E12	128	151	D16	PH13	I/O	FT_h	-	TIM8_CH1N, UART4_TX, FDCAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	-	-	E13	129	152	B17	PH14	I/O	FT_h	-	TIM8_CH2N, UART4_RX, FDCAN1_RX, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	D13	130	153	B16	PH15	I/O	FT_h	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	-	A13	E14	131	154	A16	PI0	I/O	FT_h	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	-	-	G9	-	-	-	VSS	S	-	-	-	-
-	-	-	B13	D14	132	155	A15	PI1	I/O	FT_h	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, TIM8_BKIN2_COMP12, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	-	A6	C14	133	156	B15	PI2	I/O	FT_h	-	TIM8_CH4, SPI2_MISO/I2S2_SDI, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	-	B7	C13	134	157	C14	PI3	I/O	FT_h	-	TIM8_ETR, SPI2_MOSI/I2S2_SDO, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	-	-	D9	135	-	-	VSS	S	-	-	-	-
-	-	-	-	C9	136	158	-	VDD	S	-	-	-	-
76	A9	109	B12	A14	137	159	B14	PA14 (JTCK/SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
77	A8	110	C11	A13	138	160	A14	PA15 (JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HRTIM_FLT1, CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS/UART4_DE, UART7_TX, EVENTOUT	-
78	B9	111	A12	B14	139	161	A13	PC10	I/O	FT_ha	-	HRTIM_EEV1, DFSDM1_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
79	B8	112	B11	B13	140	162	B13	PC11	I/O	FT_h	-	HRTIM_FLT2, DFSDM1_DATIN5, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT	-
80	C8	113	A11	A12	141	163	C12	PC12	I/O	FT_h	-	TRACED3, HRTIM_EEV2, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT	-
-	-	-	-	G10	-	-	-	VSS	S	-	-	-	-
81	D8	114	D10	B12	142	164	D13	PD0	I/O	FT_h	-	DFSDM1_CKIN6, SAI3_SCK_A, UART4_RX, FDCAN1_RX, FMC_D2/FMC_DA2, EVENTOUT	-
82	E8	115	C10	C12	143	165	E12	PD1	I/O	FT_h	-	DFSDM1_DATIN6, SAI3_SD_A, UART4_TX, FDCAN1_TX, FMC_D3/FMC_DA3, EVENTOUT	-
83	B7	116	E9	D12	144	166	D12	PD2	I/O	FT_h	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT	-
84	C7	117	D9	D11	145	167	B12	PD3	I/O	FT_h	-	DFSDM1_CKOUT, SPI2_SCK/I2S2_CK, USART2_CTS/USART2_NSS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
85	D7	118	C9	D10	146	168	A12	PD4	I/O	FT_h	-	HRTIM_FLT3, SAI3_FS_A, USART2_RTS/USART2_DE, FMC_NOE, EVENTOUT	-
86	B6	119	A9	C11	147	169	A11	PD5	I/O	FT_h	-	HRTIM_EEV3, USART2_TX, FMC_NWE, EVENTOUT	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	120	-	D8	148	170	-	VSS	S	-	-	-	-
-	-	121	-	C8	149	171	-	VDD	S	-	-	-	-
87	C6	122	B9	B11	150	172	B11	PD6	I/O	FT_h	-	SAI1_D1, DFSDM1_CKIN4, DFSDM1_DATIN1, SPI3_MOSI/I2S3_SDO, SAI1_SD_A, USART2_RX, SAI4_SD_A, SAI4_D1, SDMMC2_CK, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-
88	D6	123	D8	A11	151	173	C11	PD7	I/O	FT_h	-	DFSDM1_DATIN4, SPI1_MOSI/I2S1_SDO, DFSDM1_CKIN1, USART2_CK, SPDIFRX1_IN1, SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	-	-	-	-	174	D11	PJ12	I/O	FT	-	TRGOUT, LCD_G3, LCD_B0, EVENTOUT	-
-	-	-	-	-	-	175	E10	PJ13	I/O	FT	-	LCD_B4, LCD_B1, EVENTOUT	-
-	-	-	-	-	-	176	D10	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
-	-	-	-	-	-	177	B10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	-	-	-	H6	-	-	-	VSS	S	-	-	-	-
-	-	-	A7	-	-	-	-	VDD	S	-	-	-	-
-	-	124	C8	C10	152	178	A10	PG9	I/O	FT_h	-	SPI1_MISO/I2S1_SDI, USART6_RX, SPDIFRX1_IN4, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
-	-	125	A8	B10	153	179	A9	PG10	I/O	FT_h	-	HRTIM_FLT5, SPI1_NSS/I2S1_WS, LCD_G3, SAI2_SD_B, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	126	B8	B9	154	180	B9	PG11	I/O	FT_h	-	LPTIM1_IN2, HRTIM_EEV4, SPI1_SCK/I2S1_CK, SPDIFRX1_IN1, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-
-	-	127	E8	B8	155	181	C9	PG12	I/O	FT_h	-	LPTIM1_IN1, HRTIM_EEV5, SPI6_MISO, USART6_RTS/USART6_DE, SPDIFRX1_IN2, LCD_B4, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_NE4, LCD_B1, EVENTOUT	-
-	-	128	D7	A8	156	182	D9	PG13	I/O	FT_h	-	TRACED0, LPTIM1_OUT, HRTIM_EEV10, SPI6_SCK, USART6_CTS/USART6_NSS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, LCD_R0, EVENTOUT	-
-	-	129	C7	A7	157	183	D8	PG14	I/O	FT_h	-	TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, LCD_B0, EVENTOUT	-
-	-	130	-	D7	158	184	-	VSS	S	-	-	-	-
-	-	131	-	C7	159	185	-	VDD	S	-	-	-	-
-	-	-	-	-	-	186	C8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	-	-	-	187	B8	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	-	-	-	188	A8	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-
-	-	-	-	-	-	189	C7	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-
-	-	-	-	-	-	190	D7	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
-	-	-	-	H7	-	-	-	VSS	S	-	-	-	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	132	E7	B7	160	191	D6	PG15	I/O	FT_h	-	USART6_CTS/USART6_NSS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
89	A7	133	F7	A10	161	192	C6	PB3(JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, HRTIM_FLT4, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK, SDMMC2_D2, CRS_SYNC, UART7_RX, EVENTOUT	-
90	A6	134	B6	A9	162	193	B7	PB4(NJTRST)	I/O	FT	-	NJTRST, TIM16_BKIN, TIM3_CH1, HRTIM_EEV6, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, UART7_TX, EVENTOUT	-
91	C5	135	C6	A6	163	194	A5	PB5	I/O	FT	-	TIM17_BKIN, TIM3_CH2, HRTIM_EEV7, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, I2C4_SMBA, SPI3_MOSI/I2S3_SDO, SPI6_MOSI, FDCAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, UART5_RX, EVENTOUT	-
-	-	-	-	H8	-	-	-	VSS	S	-	-	-	-
92	B5	136	A5	B6	164	195	B5	PB6	I/O	FT_f	-	TIM16_CH1N, TIM4_CH1, HRTIM_EEV8, I2C1_SCL, CEC, I2C4_SCL, USART1_TX, LPUART1_TX, FDCAN2_TX, QUADSPI_BK1_NCS, DFSDM1_DATIN5, FMC_SDNE1, DCMI_D5, UART5_TX, EVENTOUT	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
93	A5	137	D6	B5	165	196	C5	PB7	I/O	FT_fa	-	TIM17_CH1N, TIM4_CH2, HRTIM_EEV9, I2C1_SDA, I2C4_SDA, USART1_RX, LPUART1_RX, DFSDM1_CKIN5, FMC_NL, DCMI_VSYNC, EVENTOUT	PVD_IN
94	D5	138	E6	D6	166	197	E8	BOOT0	I	B	-	-	VPP
95	B4	139	B5	A5	167	198	D5	PB8	I/O	FT_fh	-	TIM16_CH1, TIM4_CH3, DFSDM1_CKIN7, I2C1_SCL, I2C4_SCL, SDMMC1_CKIN, UART4_RX, FDCAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-
96	A4	140	C5	B4	168	199	D4	PB9	I/O	FT_fh	-	TIM17_CH1, TIM4_CH4, DFSDM1_DATIN7, I2C1_SDA, SPI2_NSS/I2S2_WS, I2C4_SDA, SDMMC1_CDIR, UART4_TX, FDCAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	D4	141	D5	A4	169	200	C4	PE0	I/O	FT_h	-	LPTIM1_ETR, TIM4_ETR, HRTIM_SCIN, LPTIM2_ETR, UART8_RX, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	C4	142	D4	A3	170	201	B4	PE1	I/O	FT_h	-	LPTIM1_IN2, HRTIM_SCOUT, UART8_TX, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	-	-	-	A7	VCAP	S	-	-	-	-
99	-	-	-	D5	-	202	-	VSS	S	-	-	-	-

Table 8. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	F7	143	C4	C6	171	203	E7	PDR_ON	I	FT	-	-	-
-	F4	-	B4	-	-	-	A6	VDDLDO (8)	S	-	-	-	-
100	-	144	-	C5	172	204	-	VDD	S	-	-	-	-
-	-	-	-	D4	173	205	A4	PI4	I/O	FT_h	-	TIM8_BKIN, SAI2_MCLK_A, TIM8_BKIN_COMP12, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	-	-	C4	174	206	A3	PI5	I/O	FT_h	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	-	A4	C3	175	207	A2	PI6	I/O	FT_h	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	-	E2	C2	176	208	B3	PI7	I/O	FT_h	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-
-	-	-	-	H9	-	-	-	VSS	S	-	-	-	-
-	-	-	-	K9	-	-	-	VSS	S	-	-	-	-
-	-	-	-	K10	-	-	M15	VSS	S	-	-	-	-

1. When this pin/ball was previously configured as an oscillator, the oscillator function is kept during and after a reset. This is valid for all resets except for power-on reset.
2. This ball should remain floating.
3. This ball should not remain floating. It can be connected to VSS or VDD. It is reserved for future use.
4. This ball should be connected to V_{SS}.
5. Pxy_C and Pxy pins/balls are two separate pads (analog switch open). The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.
6. There is a direct path between Pxy_C and Pxy pins/balls, through an analog switch. Pxy alternate functions are available on Pxy_C when the analog switch is closed. The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.
7. VREF+ pin, and consequently the internal voltage reference, are not available on the TFBGA100 package. On this package, this pin is double-bonded to VDDA which can be connected to an external reference. The internal voltage reference buffer is not available and must be kept disabled
8. When it is not available on a package, the VDDLDO pin is internally tied to VDD.
9. When the pin is used in USB configuration (OTG_HS_ID/OTG_HS_VBUS), the I/O is supplied by $V_{DD33USB}$, otherwise it is supplied by V_{DD}.
10. When it is not available on a package, the VDD50USB pin is internally tied to VDD33USB.

Table 9. Port A alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF1
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4 UART SWPM TIM1/ DFSDM SDMM MDIO ETH
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	TIM15_BKIN	-	-	USART2_CTS/USART2_NSS	UART4_TX	SDMMC2_CMD	SAI2_SD_B	ETH_M CRS
	PA1	-	TIM2_CH2	TIM5_CH2	LPTIM3_OUT	TIM15_CH1N	-	-	USART2_RTS/USART2_DE	UART4_RX	QUADSPI_BK1_IO3	SAI2_MCLK_B	ETH_M RX_CL ETH_R REF_C
	PA2	-	TIM2_CH3	TIM5_CH3	LPTIM4_OUT	TIM15_CH1	-	-	USART2_TX	SAI2_SCK_B	-	-	ETH_M
	PA3	-	TIM2_CH4	TIM5_CH4	LPTIM5_OUT	TIM15_CH2	-	-	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	ETH_M COL
	PA4	D1PWREN	-	TIM5_ETR	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	SPI6_NSS	-	-	-
	PA5	D2PWREN	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	SPI6_SCK	-	OTG_HS_ULPI_CK	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO/I2S1_SDI	-	-	SPI6_MISO	TIM13_CH1	TIM8_BKIN_COMP12	MDIO MDC
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SDO	-	-	SPI6_MOSI	TIM14_CH1	-	ETH_M RX_D ETH_R CRS_I
	PA8	MCO1	TIM1_CH1	HRTIM_CHB2	TIM8_BKIN2	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	UART7
	PA9	-	TIM1_CH2	HRTIM_CHC1	LPUART1_TX	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-
	PA10	-	TIM1_CH3	HRTIM_CHC2	LPUART1_RX	-	-	-	USART1_RX	-	-	OTG_FS_ID	MDIO MDIC
	PA11	-	TIM1_CH4	HRTIM_CHD1	LPUART1_CTS	-	SPI2_NSS/I2S2_WS	UART4_RX	USART1_CTS/USART1_NSS	-	FDCAN1_RX	OTG_FS_DM	-
	PA12	-	TIM1_ETR	HRTIM_CHD2	LPUART1_RTS/LPUART1_DE	-	SPI2_SCK/I2S2_CK	UART4_TX	USART1_RTS/USART1_DE	SAI2_FS_B	FDCAN1_TX	OTG_FS_DP	-

Table 9. Port A alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF1
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4 UART SWPM TIM1/ DFSDM SDMM MDIO ETH
Port A	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-
	PA15	JTDI	TIM2_CH1/TIM2_ETR	HRTIM_FLT1	-	CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SPI6_NSS	UART4_RTS/UART4_DE	-	-	UART7

Table 10. Port B alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C UA SWP TIM DFS SDM MD E
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	DFSDM1_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH RX
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH RX
	PB2	RTC_OUT	-	SAI1_D1	-	DFSDM1_CKIN1	-	SAI1_SD_A	SPI3_MOSI/I2S3_SDO	SAI4_SD_A	QUADSPI_CLK	SAI4_D1	
	PB3	JTDO/TRACESWO	TIM2_CH2	HRTIM_FLT4	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK	SDMMC2_D2	CRS_SYNC	UART
	PB4	NJTRST	TIM16_BKIN	TIM3_CH1	HRTIM_EEV6	-	SPI1_MISO/I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_NSS/I2S2_WS	SPI6_MISO	SDMMC2_D3	-	UART
	PB5	-	TIM17_BKIN	TIM3_CH2	HRTIM_EEV7	I2C1_SMBA	SPI1_MOSI/I2S1_SDO	I2C4_SMBA	SPI3_MOSI/I2S3_SDO	SPI6_MOSI	FDCAN2_RX	OTG_HS_ULPI_D7	ETH_ O
	PB6	-	TIM16_CH1N	TIM4_CH1	HRTIM_EEV8	I2C1_SCL	CEC	I2C4_SCL	USART1_TX	LPUART1_TX	FDCAN2_TX	QUADSPI_BK1_NCS	DFS DA
	PB7	-	TIM17_CH1N	TIM4_CH2	HRTIM_EEV9	I2C1_SDA	-	I2C4_SDA	USART1_RX	LPUART1_RX	-	-	DFS CK

Table 10. Port B alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C UA SWP TIM DFS SDM MD ET
Port B	PB8	-	TIM16_CH1	TIM4_CH3	DFSDM1_CKIN7	I2C1_SCL	-	I2C4_SCL	SDMMC1_CKIN	UART4_RX	FDCAN1_RX	SDMMC2_D4	ETH TX
	PB9	-	TIM17_CH1	TIM4_CH4	DFSDM1_DATIN7	I2C1_SDA	SPI2_NSS/I2S2_WS	I2C4_SDA	SDMMC1_CDIR	UART4_TX	FDCAN1_TX	SDMMC2_D5	I2C SM
	PB10	-	TIM2_CH3	HRTIM_SCOUT	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	DFSDM1_DATIN7	USART3_TX	-	QUADSPI_BK1_NCS	OTG_HS_ULPI_D3	ETH RX
	PB11	-	TIM2_CH4	HRTIM_SCIN	LPTIM2_ETR	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH TX ETH_ TX
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	DFSDM1_DATIN1	USART3_CK	-	FDCAN2_RX	OTG_HS_ULPI_D5	ETH TXD0 RMII
	PB13	-	TIM1_CH1N	-	LPTIM2_OUT	-	SPI2_SCK/I2S2_CK	DFSDM1_CKIN1	USART3_CTS/USART3_NSS	-	FDCAN2_TX	OTG_HS_ULPI_D6	ETH TXD1 RMII
	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/I2S2_SDI	DFSDM1_DATIN2	USART3_RTS/USART3_DE	UART4_RTS/UART4_DE	SDMMC2_D0	-	
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SDO	DFSDM1_CKIN2	-	UART4_CTS	SDMMC2_D1	-	

Table 11. Port C alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF1
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4 UART SWPM TIM1 DFSD SDMM MDIO ETH
Port C	PC0	-	-	-	DFSDM1_CKIN0	-	-	DFSDM1_DATIN4	-	SAI2_FS_B	-	OTG_HS_ULPI_STP	-
	PC1	TRACED0	-	SAI1_D1	DFSDM1_DATIN0	DFSDM1_CKIN4	SPI2_MOSI/I2S2_SDO	SAI1_SD_A	-	SAI4_SD_A	SDMMC2_CK	SAI4_D1	ETH_M
	PC2	CDSLEEP	-	-	DFSDM1_CKIN1	-	SPI2_MISO/I2S2_SDI	DFSDM1_CKOUT	-	-	-	OTG_HS_ULPI_DIR	ETH_ TXD
	PC3	CSLEEP	-	-	DFSDM1_DATIN1	-	SPI2_MOSI/I2S2_SDO	-	-	-	-	OTG_HS_ULPI_NXT	ETH_ TX_C
	PC4	-	-	-	DFSDM1_CKIN2	-	I2S1_MCK	-	-	-	SPDIFRX1_IN3	-	ETH_ RXD0/E RMII_R
	PC5	-	-	SAI1_D3	DFSDM1_DATIN2	-	-	-	-		SPDIFRX1_IN4	SAI4_D3	ETH_ RXD1/E RMII_R
	PC6	-	HRTIM_CHA1	TIM3_CH1	TIM8_CH1	DFSDM1_CKIN3	I2S2_MCK	-	USART6_TX	SDMMC1_D0DIR	FMC_NWAIT	SDMMC2_D6	-
	PC7	TRGIO	HRTIM_CHA2	TIM3_CH2	TIM8_CH2	DFSDM1_DATIN3	-	I2S3_MCK	USART6_RX	SDMMC1_D123DIR	FMC_NE1	SDMMC2_D7	SWPM
	PC8	TRACED1	HRTIM_CHB1	TIM3_CH3	TIM8_CH3	-	-	-	USART6_CK	UART5_RTS/UART5_DE	FMC_NE2/FMC_NCE	-	SWPM
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-	UART5_CTS	QUADSPI_BK1_IO0	LCD_G3	SWPI SUSPI
	PC10	-	-	HRTIM_EEV1	DFSDM1_CKIN5	-	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	QUADSPI_BK1_IO1	-	-
	PC11	-	-	HRTIM_FLT2	DFSDM1_DATIN5	-	-	SPI3_MISO/I2S3_SDI	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	-	-
	PC12	TRACED3	-	HRTIM_EEV2	-	-	-	SPI3_MOSI/I2S3_SDO	USART3_CK	UART5_TX	-	-	-
	PC13	-	-	-	-	-	-	-	-	-	-	-	-

Table 11. Port C alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF1
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4 UART SWPM TIM1 DFSD SDMM MDIO ETH
Port C	PC14	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-	-	-	-	-

Table 12. Port D alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C UAR SWP TIM DFSD SDMI MDI ET
Port D	PD0	-	-	-	DFSDM1_CKIN6	-	-	SAI3_SCK_A	-	UART4_RX	FDCAN1_RX	-	
	PD1	-	-	-	DFSDM1_DATIN6	-	-	SAI3_SD_A	-	UART4_TX	FDCAN1_TX	-	
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	
	PD3	-	-	-	DFSDM1_CKOUT	-	SPI2_SCK/I2S2_CK	-	USART2_CTS/USART2_NSS	-	-	-	
	PD4	-	-	HRTIM_FLT3	-	-	-	SAI3_FS_A	USART2_RTS/USART2_DE	-	-	-	
	PD5	-	-	HRTIM_EEV3	-	-	-	-	USART2_TX	-	-	-	
	PD6	-	-	SAI1_D1	DFSDM1_CKIN4	DFSDM1_DATIN1	SPI3_MOSI/I2S3_SDO	SAI1_SD_A	USART2_RX	SAI4_SD_A	-	SAI4_D1	SDMM C
	PD7	-	-	-	DFSDM1_DATIN4	-	SPI1_MOSI/I2S1_SDO	DFSDM1_CKIN1	USART2_CK	-	SPDIFRX1_IN1	-	SDMM CM

Table 12. Port D alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C UAR SWP TIM DFSD SDMI MDI ET
Port D	PD8	-	-	-	DFSDM1_CKIN3	-	-	SAI3_SCK_B	USART3_TX	-	SPDIFRX1_IN2	-	-
	PD9	-	-	-	DFSDM1_DATIN3	-	-	SAI3_SD_B	USART3_RX	-	-	-	-
	PD10	-	-	-	DFSDM1_CKOUT	-	-	SAI3_FS_B	USART3_CK	-	-	-	-
	PD11	-	-	-	LPTIM2_IN2	I2C4_SMBA	-	-	USART3_CTS/USART3_NSS	-	QUADSPI_BK1_IO0	SAI2_SD_A	-
	PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	I2C4_SCL	-	-	USART3_RTS/USART3_DE	-	QUADSPI_BK1_IO1	SAI2_FS_A	-
	PD13	-	LPTIM1_OUT	TIM4_CH2	-	I2C4_SDA	-	-		-	QUADSPI_BK1_IO3	SAI2_SCK_A	-
	PD14	-	-	TIM4_CH3	-	-	-	SAI3_MCLK_B	-	UART8_CTS	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	SAI3_MCLK_A	-	UART8_RTS/UART8_DE	-	-	-

Table 13. Port E alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C UAR SWPI TIM1 DFSD SDMM MDIO ET
Port E	PE0	-	LPTIM1_ETR	TIM4_ETR	HRTIM_SCIN	LPTIM2_ETR	-	-	-	UART8_RX	-	SAI2_MCLK_A	-
	PE1	-	LPTIM1_IN2	-	HRTIM_SCOUT	-	-	-	-	UART8_TX	-	-	-
	PE2	TRACECLK	-	SAI1_CK1	-	-	SPI4_SCK	SAI1_MCLK_A	-	SAI4_MCLK_A	QUADSPI_BK1_IO2	SAI4_CK1	ETH_TXD
	PE3	TRACED0	-	-	-	TIM15_BKIN	-	SAI1_SD_B	-	SAI4_SD_B	-	-	-
	PE4	TRACED1	-	SAI1_D2	DFSDM1_DATIN3	TIM15_CH1N	SPI4_NSS	SAI1_FS_A	-	SAI4_FS_A	-	SAI4_D2	-
	PE5	TRACED2	-	SAI1_CK2	DFSDM1_CKIN3	TIM15_CH1	SPI4_MISO	SAI1_SCK_A	-	SAI4_SCK_A	-	SAI4_CK2	-
	PE6	TRACED3	TIM1_BKIN2	SAI1_D1	-	TIM15_CH2	SPI4_MOSI	SAI1_SD_A	-	SAI4_SD_A	SAI4_D1	SAI2_MCLK_B	TIM1_2_COM
	PE7	-	TIM1_ETR	-	DFSDM1_DATIN2	-	-	-	UART7_RX	-	-	QUADSPI_BK2_IO0	-
	PE8	-	TIM1_CH1N	-	DFSDM1_CKIN2	-	-	-	UART7_TX	-	-	QUADSPI_BK2_IO1	-
	PE9	-	TIM1_CH1	-	DFSDM1_CKOUT	-	-	-	UART7_RTS/UART7_DE	-	-	QUADSPI_BK2_IO2	-
	PE10	-	TIM1_CH2N	-	DFSDM1_DATIN4	-	-	-	UART7_CTS	-	-	QUADSPI_BK2_IO3	-
	PE11	-	TIM1_CH2	-	DFSDM1_CKIN4	-	SPI4_NSS	-	-	-	-	SAI2_SD_B	-
	PE12	-	TIM1_CH3N	-	DFSDM1_DATIN5	-	SPI4_SCK	-	-	-	-	SAI2_SCK_B	-
	PE13	-	TIM1_CH3	-	DFSDM1_CKIN5	-	SPI4_MISO	-	-	-	-	SAI2_FS_B	-
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	SAI2_MCLK_B	-
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-		-

Table 14. Port F alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF1
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C UAR SWPM TIM1 DFSD SDMM MDIO ETI
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-
	PF3	-	-	-	-	-	-	-	-	-	-	-	-
	PF4	-	-	-	-	-	-	-	-	-	-	-	-
	PF5	-	-	-	-	-	-	-	-	-	-	-	-
	PF6	-	TIM16_CH1	-	-	-	SPI5_NSS	SAI1_SD_B	UART7_RX	SAI4_SD_B	QUADSPI_BK1_IO3	-	-
	PF7	-	TIM17_CH1	-	-	-	SPI5_SCK	SAI1_MCLK_B	UART7_TX	SAI4_MCLK_B	QUADSPI_BK1_IO2	-	-
	PF8	-	TIM16_CH1N	-	-	-	SPI5_MISO	SAI1_SCK_B	UART7_RTS/UART7_DE	SAI4_SCK_B	TIM13_CH1	QUADSPI_BK1_IO0	-
	PF9	-	TIM17_CH1N	-	-	-	SPI5_MOSI	SAI1_FS_B	UART7_CTS	SAI4_FS_B	TIM14_CH1	QUADSPI_BK1_IO1	-
	PF10	-	TIM16_BKIN	SAI1_D3	-	-	-	-	-	-	QUADSPI_CLK	SAI4_D3	-
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	SAI2_SD_B	-
	PF12	-	-	-	-	-	-	-	-	-	-	-	-
	PF13	-	-	-	DFSDM1_DATIN6	I2C4_SMBA	-	-	-	-	-	-	-
	PF14	-	-	-	DFSDM1_CKIN6	I2C4_SCL	-	-	-	-	-	-	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-	-	-	-	-

Table 15. Port G alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C /S T DF SD MD
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	
	PG1	-	-	-	-	-	-	-	-	-	-	-	
	PG2	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	TIM C
	PG3	-	-	-	TIM8_BKIN2	-	-	-	-	-	-	-	TIM _C
	PG4	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-	TIM _C
	PG5	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	
	PG6	-	TIM17_BKIN	HRTIM_CHE1	-	-	-	-	-	-	-	QUADSPI_BK1_NCS	
	PG7	-	-	HRTIM_CHE2	-	-	-	SAI1_MCLK_A	USART6_CK	-	-	-	
	PG8	-	-	-	TIM8_ETR	-	SPI6_NSS	-	USART6_RTS/USART6_DE	SPDIFRX1_IN3	-	-	ET
	PG9	-	-	-	-	-	SPI1_MISO/I2S1_SDI	-	USART6_RX	SPDIFRX1_IN4	QUADSPI_BK2_IO2	SAI2_FS_B	
	PG10	-	-	HRTIM_FLT5	-	-	SPI1_NSS/I2S1_WS	-	-	-	LCD_G3	SAI2_SD_B	
	PG11	-	LPTIM1_IN2	HRTIM_EEV4	-	-	SPI1_SCK/I2S1_CK	-	-	SPDIFRX1_IN1	-	SDMMC2_D2	ET T ETI T
	PG12	-	LPTIM1_IN1	HRTIM_EEV5	-	-	SPI6_MISO		USART6_RTS/USART6_DE	SPDIFRX1_IN2	LCD_B4	-	ET TXI RM
	PG13	TRACED0	LPTIM1_OUT	HRTIM_EEV10	-	-	SPI6_SCK	-	USART6_CTS/USART6_NSS	-	-	-	ET TXI RM

Table 15. Port G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C
Port G	PG14	TRACED1	LPTIM1_ETR	-	-	-	SPI6_MOSI	-	USART6_TX		QUADSPI_BK2_IO3	-	ET TXI RM
	PG15	-	-	-	-	-	-	-	USART6_CTS/USART6_NSS	-	-	-	

Table 16. Port H alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C UAR SWPI TIM1 DFSD SDMM MDIO ET
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-	-	-	-	-
	PH2	-	LPTIM1_IN2	-	-	-	-	-	-	-	QUADSPI_BK2_IO0	SAI2_SCK_B	ETH_CR
	PH3	-	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO1	SAI2_MCLK_B	ETH_CC
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	LCD_G5	OTG_HS_ULPI_NXT	-
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-
	PH6	-	-	TIM12_CH1	-	I2C2_SMBA	SPI5_SCK	-	-	-	-	-	ETH_RXD
	PH7	-	-	-	-	I2C3_SCL	SPI5_MISO	-	-	-	-	-	ETH_RXD
	PH8	-	-	TIM5_ETR	-	I2C3_SDA	-	-	-	-	-	-	-
	PH9	-	-	TIM12_CH2	-	I2C3_SMBA	-	-	-	-	-	-	-
	PH10	-	-	TIM5_CH1	-	I2C4_SMBA	-	-	-	-	-	-	-
	PH11	-	-	TIM5_CH2	-	I2C4_SCL	-	-	-	-	-	-	-
	PH12	-	-	TIM5_CH3	-	I2C4_SDA	-	-	-	-	-	-	-
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	UART4_TX	FDCAN1_TX	-	-
	PH14	-	-	-	TIM8_CH2N	-	-	-	-	UART4_RX	FDCAN1_RX	-	-
	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-

Table 17. Port I alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF1
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4 UART SWPM TIM1 DFSD SDMM MDIO ETI
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	-
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	TIM8_B 2_COM
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO/I2S2_SDI	-	-	-	-	-	-
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SDO	-	-	-	-	-	-
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCLK_A	TIM8_B _COM
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-
	PI8	-	-	-	-	-	-	-	-	-	-	-	-
	PI9	-	-	-	-	-	-	-	-	UART4_RX	FDCAN1_RX	-	-
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_ RX_
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-
	PI12	-	-	-	-	-	-	-	-	-	-	-	-
	PI13	-	-	-	-	-	-	-	-	-	-	-	-
	PI14	-	-	-	-	-	-	-	-	-	-	-	-
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-

Table 18. Port J alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF1
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4 UART SWPM TIM1 DFSD SDMM MDIO ETI
Port J	PJ0	-	-	-	-	-	-	-	-	-	LCD_R7	-	-
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-
	PJ6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-
	PJ7	TRGIN	-	-	TIM8_CH2N	-	-	-	-	-	-	-	-
	PJ8	-	TIM1_CH3N	-	TIM8_CH1	-	-	-	-	UART8_TX	-	-	-
	PJ9	-	TIM1_CH3	-	TIM8_CH1N	-	-	-	-	UART8_RX	-	-	-
	PJ10	-	TIM1_CH2N	-	TIM8_CH2	-	SPI5_MOSI	-	-	-	-	-	-
	PJ11	-	TIM1_CH2	-	TIM8_CH2N	-	SPI5_MISO	-	-	-	-	-	-
	PJ12	TRGOUT	-	-	-	-	-	-	-	-	LCD_G3	-	-
	PJ13	-	-	-	-	-	-	-	-	-	LCD_B4	-	-
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-

Table 19. Port K alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF1
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM1	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4 UART SWPM TIM1 DFSD SDMM MDIO ETI
Port K	PK0	-	TIM1_CH1N	-	TIM8_CH3	-	SPI5_SCK	-	-	-	-	-	-
	PK1	-	TIM1_CH1	-	TIM8_CH3N	-	SPI5_NSS	-	-	-	-	-	-
	PK2	-	TIM1_BKIN	-	TIM8_BKIN	-	-	-	-	-	-	TIM8_BKIN_COMP12	TIM1_E _COM
	PK3	-	-	-	-	-	-	-	-	-	-	-	-
	PK4	-	-	-	-	-	-	-	-	-	-	-	-
	PK5	-	-	-	-	-	-	-	-	-	-	-	-
	PK6	-	-	-	-	-	-	-	-	-	-	-	-
	PK7	-	-	-	-	-	-	-	-	-	-	-	-

6 Electrical characteristics (rev Y)

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at T_J = 25 °C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 12*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 13*.

Figure 12. Pin loading conditions

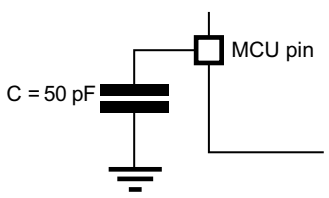
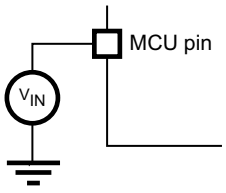
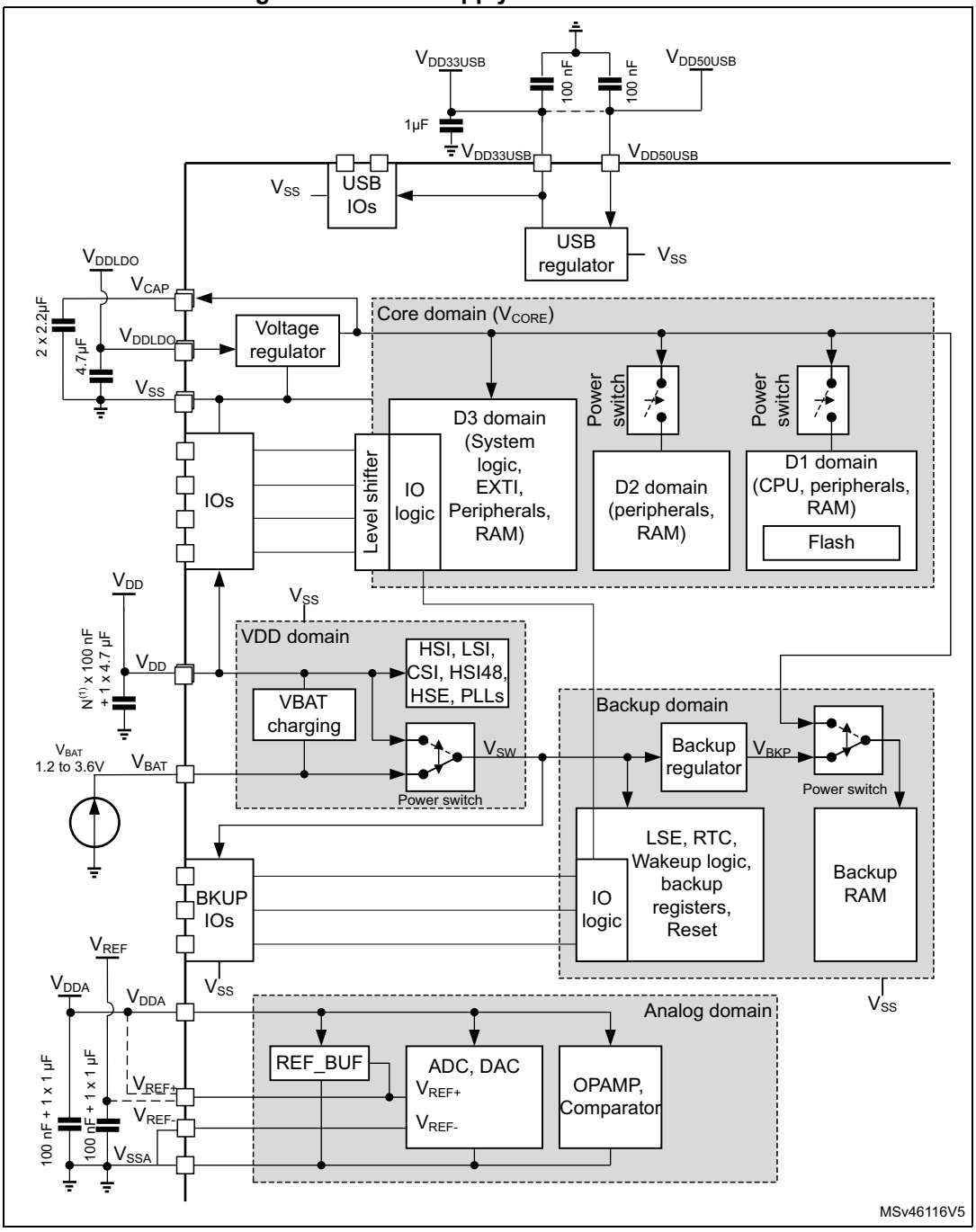


Figure 13. Pin input voltage



6.1.6 Power supply scheme

Figure 14. Power supply scheme



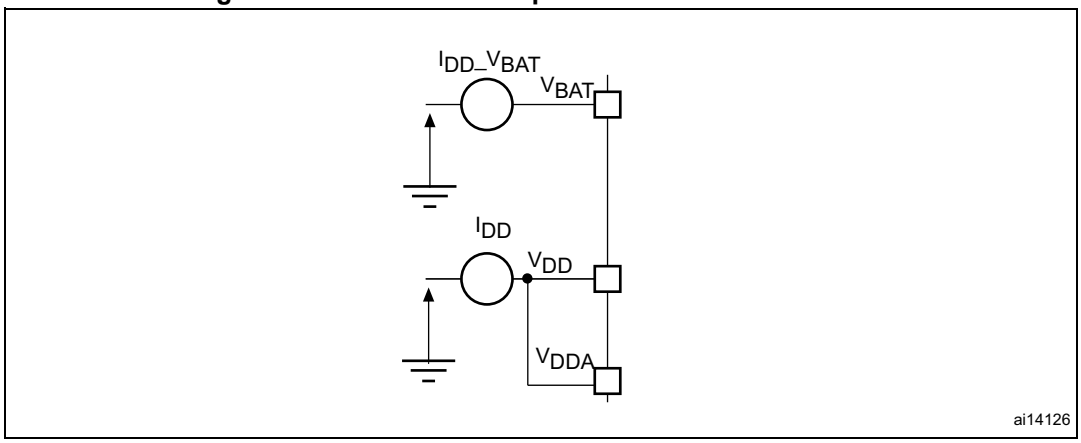
1. N corresponds to the number of VDD pins available on the package.
2. A tolerance of +/- 20% is acceptable on decoupling capacitors.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the

device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 15. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 20: Voltage characteristics*, *Table 21: Current characteristics*, and *Table 22: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 20. Voltage characteristics (1)

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDLDO}, V_{DDA}, $V_{DD33USB}$, V_{BAT})	−0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}−0.3	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) +4.0(3)(4)	V
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	V
	Input voltage on BOOT0 pin	V_{SS}	9.0	V
	Input voltage on any other pins	V_{SS}-0.3	4.0	V
$\lvert\Delta V_{DDX}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 58* for the maximum allowed injected current values.

3. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
4. To sustain a voltage higher than 4V the internal pull-up/pull-down resistors must be disabled.

Table 21. Current characteristics

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	620	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	620	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST and B pins except PA4, PA5	−5/+0	
	Injected current on PA4, PA5	−0/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 20: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 22. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	− 65 to +150	°C
T_J	Maximum junction temperature	125	

6.3 Operating conditions

6.3.1 General operating conditions

Table 23. General operating conditions

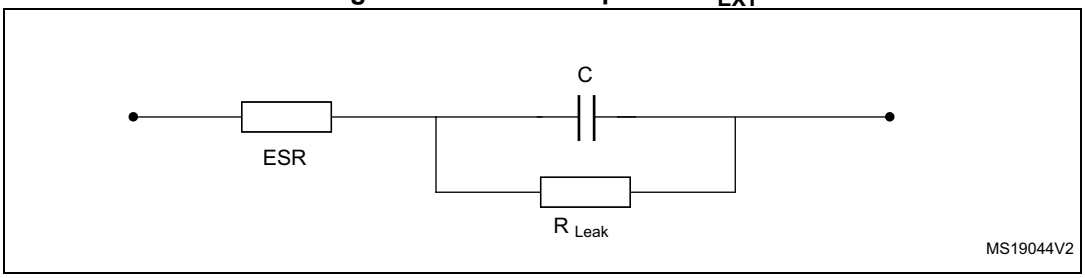
Symbol	Parameter	Operating conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.62(1)	3.6	V
V_{DDLDO}	Supply voltage for the internal regulator	$V_{DDLDO} \le V_{DD}$	1.62(1)	3.6	
$V_{DD33USB}$	Standard operating voltage, USB domain	USB used	3.0	3.6	
		USB not used	0	3.6	
V_{DDA}	Analog operating voltage	ADC or COMP used	1.62	3.6	
		DAC used	1.8		
		OPAMP used	2.0		
		VREFBUF used	1.8		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{IN}	I/O Input voltage	TT_xx I/O	−0.3	V_{DD}+0.3	
		BOOT0	0	9	
		All I/O except BOOT0 and TT_xx	−0.3	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$)+3.6V < 5.5V(2)(3)	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(4)	–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation	–40	125	
		Low-power dissipation(4)	–40	130	
T_J	Junction temperature range	Suffix 6 version	–40	125	°C

1. When RESET is released functionality is guaranteed down to V_{BOR0} min
2. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, $V_{DD33USB}$) +0.3V, the internal Pull-up and Pull-Down resistors must be disabled.
4. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 8.9: Thermal characteristics*).

6.3.2 VCAP external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP pin. C_{EXT} is specified in *Table 24*. Two external capacitors can be connected to VCAP pins.

Figure 16. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 24. VCAP operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF(2)
ESR	ESR of external capacitor	< 100 mΩ

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.
2. This value corresponds to CEXT typical value. A variation of +/-20% is tolerated.

6.3.3 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 25. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	
t_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	0	∞	
	V_{DDUSB} fall time rate	10	∞	

6.3.4 Embedded reset and power control block characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 26. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after BOR0 released	-	-	377	-	µs
$V_{BOR0/POR/PDR}$	Brown-out reset threshold 0 (V_{POR}/V_{PDR} thresholds)	Rising edge(1)	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable Voltage Detector threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge in Run mode	2.69	2.76	2.83	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BOR (unless BOR0) and PVD	Hysteresis in Run mode	-	100	-	mV
$I_{DD_BOR_PVD}$(1)	BOR(2) (unless BOR0) and PVD consumption from V_{DD}	-	-		0.630	µA

Table 26. Reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVM_0}	Analog voltage detector for V_{DDA} threshold 0	Rising edge	1.66	1.71	1.76	V
		Falling edge	1.56	1.61	1.66	
V_{AVM_1}	Analog voltage detector for V_{DDA} threshold 1	Rising edge	2.06	2.12	2.19	
		Falling edge	1.96	2.02	2.08	
V_{AVM_2}	Analog voltage detector for V_{DDA} threshold 2	Rising edge	2.42	2.50	2.58	
		Falling edge	2.35	2.42	2.49	
V_{AVM_3}	Analog voltage detector for V_{DDA} threshold 3	Rising edge	2.74	2.83	2.91	
		Falling edge	2.64	2.72	2.80	
V_{hyst_VDDA}	Hysteresis of V_{DDA} voltage detector	-	-	100	-	mV
I_{DD_PVM}	PVM consumption from $V_{DD(1)}$	-	-	-	0.25	µA
I_{DD_VDDA}	Voltage detector consumption on V_{DDA}(1)	Resistor bridge	-	-	2.5	µA

1. Guaranteed by design.
2. BOR0 is enabled in all modes and its consumption is therefore included in the supply current characteristics tables (refer to *Section 6.3.6: Supply current characteristics*).

6.3.5 Embedded reference voltage

The parameters given in *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 27. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltages	-40°C < TJ < 105°C, V_{DD} = 3.3 V	1.180	1.216	1.255	V
$t_{S_vrefint}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}(1)(2)	VBAT sampling time when reading the internal VBAT reference voltage	-	9	-	-	
I_{refbuf}(2)	Reference Buffer consumption for ADC	V_{DDA}=3.3 V	9	13.5	23	µA
ΔV_{REFINT}(2)	Internal reference voltage spread over the temperature range	-40°C < T_J < 105°C	-	5	15	mV
T_{coeff}(2)	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$(2)	Average Voltage coefficient	3.0V < V_{DD} < 3.6V	-	10	1370	ppm/V

Table 27. Embedded reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT_DIV1}	1/4 reference voltage	-	-	25	-	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage	-	-	50	-	
V_{REFINT_DIV3}	3/4 reference voltage	-	-	75	-	

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Guaranteed by design.

Table 28. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA} = 3.3 V	1FF1E860 - 1FF1E861

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 15: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{ACLK} frequency (refer to the table “Number of wait states according to CPU clock ($f_{rcc_c_ck}$) frequency and V_{CORE} range” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency divided by 2 and the APB clock frequency is AHB clock frequency divided by 2.

The parameters given in *Table 29* to *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 29. Typical and maximum current consumption in Run mode, code with data processing running from ITCM, regulator ON(1)

Symbol	Parameter	Conditions		$f_{rcc_c_ck}$ (MHz)	Typ	Max(2)				unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS1	400	71	110	210	290	540	mA
				300	56	-	-	-	-	
			VOS2	300	50	72	170	230	370	
				216	37	58	150	210	380	
				200	35.5	-	-	-	-	
			VOS3	200	33	50	130	190	300	
				180	30	47	130	180	290	
				168	28	45	130	180	290	
				144	25	41	120	180	290	
				60	13	28	110	160	280	
				25	10	24	99	160	270	
		All peripherals enabled	VOS1	400	165	220(3)	400	500(3)	840	
				300	130	-	-	-	-	
			VOS2	300	120	170	300	390	570	
				200	83	-	-	-	-	
			VOS3	200	78	110	220	300	470	

1. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
2. Guaranteed by characterization results unless otherwise specified.
3. Guaranteed by test in production.

Table 30. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, cache ON, regulator ON

Symbol	Parameter	Conditions		$f_{rcc_c_ck}$ (MHz)	Typ	Max(1)				unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS1	400	105	160	310	420	750	mA
				300	55	-	-	-	-	
			VOS2	300	50	72	160	230	370	
				216	38	-	-	-	-	
				200	36	-	-	-	-	
			VOS3	200	33	50	130	190	300	
				180	30	-	-	-	-	
				168	29	-	-	-	-	
				144	26	-	-	-	-	
				60	14	-	-	-	-	
				25	14	-	-	-	-	
		All peripherals enabled	VOS1	400	160	220	400	500	750	
				300	130	-	-	-	-	
			VOS2	300	120	160	300	390	560	
				200	81	-	-	-	-	
			VOS3	200	77	110	220	300	460	

1. Guaranteed by characterization results unless otherwise specified.

Table 31. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, cache OFF, regulator ON

Symbol	Parameter	Conditions		$f_{rcc_c_ck}$ (MHz)	Typ	Max(1)				unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS1	400	73	110	220	290	540	mA
			VOS2	300	52	75	170	230	370	
			VOS3	200	34	52	130	190	300	
		All peripherals enabled	VOS1	400	135	190	360	470	730	
			VOS2	300	100	150	270	370	550	
			VOS3	200	70	100	210	300	460	

1. Guaranteed by characterization results.

Table 32. Typical consumption in Run mode and corresponding performance versus code position

Symbol	Parameter	Conditions		$f_{rcc_c_ck}$ (MHz)	CoreMark	Typ	Unit	IDD/ CoreMark	Unit
		Peripheral	Code						
I_{DD}	Supply current in Run mode	All peripherals disabled, cache ON	ITCM	400	2012	71	mA	35	µA/ CoreMark
			FLASH A	400	2012	105		52	
			AXI SRAM	400	2012	105		52	
			SRAM1	400	2012	105		52	
			SRAM4	400	2012	105		52	
		All peripherals disabled cache OFF	ITCM	400	2012	71		35	
			FLASH A	400	593	70.5		119	
			AXI SRAM	400	344	70.5		205	
			SRAM1	400	472	74.5		158	
			SRAM4	400	432	72		167	

Table 33. Typical current consumption batch acquisition mode

Symbol	Parameter	Conditions		$f_{rcc_ahb_ck(AHB4)}$ (MHz)	Typ	unit
I_{DD}	Supply current in batch acquisition mode	D1Standby, D2Standby, D3Run	VOS3	64	6.5	mA
		D1Stop, D2Stop, D3Run	VOS3	64	12	

Table 34. Typical and maximum current consumption in Sleep mode, regulator ON

Symbol	Parameter	Conditions		$f_{rcc_c_ck}$ (MHz)	Typ	Max(1)				unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	All peripherals disabled	VOS1	400	31.0	64	220	330	660	mA
				300	24.5	57	210	330	650	
			VOS2	300	22.0	48	180	270	500	
				200	17.0	42	170	270	490	
			VOS3	200	15.5	37	150	230	400	

1. Guaranteed by characterization results.

Table 35. Typical and maximum current consumption in Stop mode, regulator ON

Symbol	Parameter	Conditions		Typ	Max(1)				unit
					T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	
$I_{DD(Stop)}$	D1Stop, D2Stop, D3Stop	Flash memory in low-power mode, no IWDG	SVOS5	1.4	7.2(2)	49	75(2)	140	mA
			SVOS4	1.95	11	66	110	200	
			SVOS3	2.85	16(2)	91	150(2)	240	
		Flash memory ON, no IWDG	SVOS5	1.65	7.2	49	75	140	
			SVOS4	2.2	11	66	110	180	
			SVOS3	3.15	16	91	150	300	
	D1Stop, D2Standby, D3Stop	Flash memory OFF, no IWDG	SVOS5	0.99	5.1	35	60	97	
			SVOS4	1.4	7.5	47	79	130	
			SVOS3	2.05	12	64	110	170	
		Flash memory ON, no IWDG	SVOS5	1.25	5.5	35	61	98	
			SVOS4	1.65	7.8	47	80	130	
			SVOS3	2.3	12	65	110	170	
	D1Standby, D2Stop, D3Stop	Flash OFF, no IWDG	SVOS5	0.57	3	21	36	57	
			SVOS4	0.805	4.5	27	47	74	
			SVOS3	1.2	6.7	37	63	99	
	D1Standby, D2Standby, D3Stop		SVOS5	0.17	1.1(2)	8	13(2)	20	
			SVOS4	0.245	1.5	11	17	26	
			SVOS3	0.405	2.4(2)	15	23(2)	35	

1. Guaranteed by characterization results.
2. Guaranteed by test in production.

Table 36. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions		Typ(3)				Max (3 V)(1)				Unit
		Backup SRAM	RTC & LSE	1.62 V	2.4 V	3 V	3.3 V	T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	
I_{DD} (Standby)	Supply current in Standby mode	OFF	OFF	1.8	1.9	1.95	2.05	4(2)	18(3)	40(2)	90(3)	µA
		ON	OFF	3.4	3.4	3.5	3.7	8.2(3)	47(3)	83(3)	141(3)	
		OFF	ON	2.4	3.5	3.86	4.12	-	-	-	-	
		ON	ON	3.95	5.1	5.46	5.97	-	-	-	-	

1. The maximum current consumption values are given for PDR OFF (internal reset OFF). When the PDR is OFF (internal reset OFF), the current consumption is reduced by 1.2 µA compared to PDR ON.
2. Guaranteed by test in production.
3. Guaranteed by characterization results.

Table 37. Typical and maximum current consumption in VBAT mode

Symbol	Parameter	Conditions		Typ(1)				Max (3 V)				Unit
		Backup SRAM	RTC & LSE	1.2 V	2 V	3 V	3.4 V	T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	
I_{DD} (VBAT)	Supply current in standby mode	OFF	OFF	0.024	0.035	0.062	0.096	0.5(1)	4.1(1)	10(1)	24(1)	µA
		ON	OFF	1.4	1.6	1.8	1.8	4.4(1)	22(1)	48(1)	87(1)	
		OFF	ON	0.24	0.45	0.62	0.73	-	-	-	-	
		ON	ON	1.97	2.37	2.57	2.77	-	-	-	-	

1. Guaranteed by characterization results.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 59: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 38: Peripheral current consumption in Run mode*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- $f_{rcc_c_ck}$ is the CPU clock. $f_{PCLK} = f_{rcc_c_ck}/4$, and $f_{HCLK} = f_{rcc_c_ck}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{rcc_c_ck}$ = 400 MHz (Scale 1), $f_{rcc_c_ck}$ = 300 MHz (Scale 2), $f_{rcc_c_ck}$ = 200 MHz (Scale 3)
- The ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 38. Peripheral current consumption in Run mode

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
AHB3	MDMA	8.3	7.6	7	µA/MHz
	DMA2D	21	20	18	
	JPEG	24	23	21	
	FLASH	9.9	9	8.3	
	FMC registers	0.9	0.9	0.8	
	FMC kernel	6.1	5.5	5.3	
	QUADSPI registers	1.5	1.4	1.3	
	QUADSPI kernel	0.9	0.8	0.7	
	SDMMC1 registers	8	7.2	6.8	
	SDMMC1 kernel	2.4	2	1.8	
	DTCM1	5.7	5	4.5	
	DTCM2	5.5	4.8	4.3	
	ITCM	3.2	2.9	2.6	
	D1SRAM1	7.6	6.8	6.1	
	AHB3 bridge	7.5	6.8	6.3	
AHB1	DMA1	1.1	1	1	
	DMA2	1.7	1.4	1.1	
	ADC1/2 registers	3.9	3.2	3.1	
	ADC1/2 kernel	0.9	0.8	0.7	
	ART accelerator	5.5	4.5	4.2	
	ETH1MAC	16	14	13	
	ETH1TX				
	ETH1RX				
	USB1 OTG registers	15	14	13	
	USB1 OTG kernel	-	8.5	8.5	
	USB1 ULPI	0.3	0.3	0.1	
	USB2 OTG registers	15	13	12	
	USB2 OTG kernel	-	8.6	8.6	
	USB2 ULPI	16	16	16	
	AHB1 Bridge	10	9.6	8.6	

Table 38. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
AHB2	DCMI	1.7	1.7	1.7	µA/MHz
	CRYP	0.1	0.1	0.1	
	HASH	0.1	0.1	0.1	
	RNG registers	1.8	1.4	1.2	
	RNG kernel	-	9.6	9.6	
	SDMMC2 registers	13	12	11	
	SDMMC2 kernel	2.7	2.5	2.4	
	D2SRAM1	3.3	3.1	2.8	
	D2SRAM2	2.9	2.7	2.5	
	D2SRAM3	1.9	1.8	1.7	
	AHB2 bridge	0.1	0.1	0.1	
AHB4	GPIOA	1.1	1	0.9	
	GPIOB	1	0.9	0.9	
	GPIOC	1.4	1.3	1.3	
	GPIOD	1.1	1	0.9	
	GPIOE	1	0.9	0.8	
	GPIOF	0.9	0.8	0.8	
	GPIOG	0.9	0.7	0.7	
	GPIOH	1	0.9	0.9	
	GPIOI	0.9	0.9	0.8	
	GPIOJ	0.9	0.8	0.8	
	GPIOK	0.9	0.8	0.7	
	CRC	0.5	0.4	0.4	
	BDMA	6.2	5.8	5.5	
	ADC3 registers	1.8	1.7	1.7	
	ADC3 kernel	0.1	0.1	0.1	
	Backup SRAM	1.9	1.8	1.8	
	Bridge AHB4	0.1	0.1	0.1	
APB3	LCD-TFT	12	11	10	µA/MHz
	WWDG1	0.5	0.4	0.3	
	APB3 bridge	0.5	0.2	0.1	

Table 38. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB1	TIM2	3.5	3.2	2.9	µA/MHz
	TIM3	3.4	3.1	2.7	
	TIM4	2.7	2.5	1.9	
	TIM5	3.2	2.9	2.5	
	TIM6	1	0.8	0.7	
	TIM7	1	0.9	0.7	
	TIM12	1.7	1.5	1.2	
	TIM13	1.5	1.3	1	
	TIM14	1.4	1.3	0.9	
	LPTIM1 registers	0.7	0.6	0.5	
	LPTIM1 kernel	2.3	2.1	1.9	
	WWDG2	0.6	0.4	0.4	
	SPI2 registers	1.8	1.5	1.2	
	SPI2 kernel	0.6	0.5	0.5	
	SPI3 registers	1.5	1.3	1.1	
	SPI3 kernel	0.6	0.5	0.5	
	SPDIFRX1 registers	0.6	0.5	0.3	
	SPDIFRX1 kernel	2.9	2.4	2.4	
	USART2 registers	1.4	1.3	1	
	USART2 kernel	4.7	4.1	4	
	USART3 registers	1.4	1.3	1	
	USART3 kernel	4.2	3.8	3.5	
	UART4 registers	1.5	1.1	1	
	UART4 kernel	3.7	3.6	3.2	

Table 38. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB1 (continued)	UART5 registers	1.4	1.4	1	µA/MHz
	UART5 kernel	3.6	3.2	3.1	
	I2C1 registers	0.8	0.8	0.6	
	I2C1 kernel	2	1.8	1.7	
	I2C2 registers	0.7	0.7	0.4	
	I2C2 kernel	1.9	1.7	1.6	
	I2C3 registers	0.9	0.7	0.6	
	I2C3 kernel	2.1	1.9	1.9	
	HDMI-CEC registers	0.5	0.3	0.3	
	DAC1/2	1.4	1.1	0.9	
	USART7 registers	1.9	1.8	1.3	
	USART7 kernel	4	3.5	3.3	
	USART8 registers	1.6	1.5	1.2	
	USART8 kernel	4	3.6	3.3	
	CRS	3.4	3.1	2.9	
	SWPMI registers	2.3	2	2	
	SWPMI kernel	0.1	0.1	0.1	
	OPAMP	0.5	0.4	0.4	
	MDIO	2.7	2.4	2.3	
	FDCAN registers	16	15	14	
	FDCAN kernel	7.8	7.6	7.1	
	Bridge APB1	0.1	0.1	0.1	

Table 38. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB2	TIM1	5.1	4.8	4.3	µA/MHz
	TIM8	5.4	4.9	4.6	
	USART1 registers	2.7	2.6	2.5	
	USART1 kernel	0.1	0.1	0.1	
	USART6 registers	2.6	2.5	2.5	
	USART6 kernel	0.1	0.1	0.1	
	SPI1 registers	1.8	1.6	1.6	
	SPI1 kernel	1	0.8	0.6	
	SPI4 registers	1.6	1.5	1.5	
	SPI4 kernel	0.5	0.4	0.4	
	TIM15	3.1	2.8	2.7	
	TIM16	2.4	2.1	2.1	
	TIM17	2.2	2	1.9	
	SPI5 registers	1.8	1.7	1.7	
	SPI5 kernel	0.6	0.5	0.3	
	SAI1 registers	1.5	1.4	1.4	
	SAI1 kernel	2	1.7	1.5	
	SAI2 registers	1.5	1.5	1.3	
	SAI2 kernel	2.2	1.9	1.8	
	SAI3 registers	1.8	1.6	1.6	
	SAI3 kernel	2.5	2.3	2.1	
	DFSDM1 registers	6	5.4	5.2	
	DFSDM1 kernel	0.9	0.8	0.7	
	HRTIM	40	37	35	
	Bridge APB2	0.1	0.1	0.1	

Table 38. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB4	SYSCFG	1	0.7	0.7	µA/MHz
	LPUART1 registers	1.1	1.1	1.1	
	LPUART1 kernel	2.6	2.4	2.1	
	SPI6 registers	1.6	1.5	1.4	
	SPI6 kernel	0.2	0.2	0.2	
	I2C4 registers	0.1	0.1	0.1	
	I2C4 kernel	2.4	2.1	2	
	LPTIM2 registers	0.5	0.5	0.5	
	LPTIM2 kernel	2.3	2.1	1.8	
	LPTIM3 registers	0.5	0.5	0.5	
	LPTIM3 kernel	2	2.1	1.5	
	LPTIM4 registers	0.5	0.5	0.5	
	LPTIM4 kernel	2	2	1.9	
	LPTIM5 registers	0.5	0.5	0.5	
	LPTIM5 kernel	2	1.8	1.5	
	COMP1/2	0.7	0.5	0.5	
	VREFBUF	0.6	0.4	0.4	
	RTC	1.2	1.1	1.1	
	SAI4 registers	1.6	1.5	1.4	
	SAI4 kernel	1.3	1.3	1.2	
	Bridge APB4	0.1	0.1	0.1	

Table 39. Peripheral current consumption in Stop, Standby and VBAT mode

Symbol	Parameter	Conditions	Typ	Unit
			3 V	
I_{DD}	RTC+LSE low drive	-	2.32	µA
	RTC+LSE medium-low drive	-	2.4	
	RTC+LSE medium-high drive	-	2.7	
	RTC+LSE High drive	-	3	

6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 40* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PC1) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 40. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep	-	9	10	CPU clock cycles
t_{WUSTOP}(2)	Wakeup from Stop	VOS3, HSI, Flash memory in normal mode	4.4	5.6	µs
		VOS3, HSI, Flash memory in low-power mode	12	15	
		VOS4, HSI, Flash memory in normal mode	15	20	
		VOS4, HSI, Flash memory in low-power mode	23	28	
		VOS5, HSI, Flash memory in normal mode	30	71	
		VOS5, HSI, Flash memory in low-power mode	38	47	
		VOS3, CSI, Flash memory in normal mode	27	37	
		VOS3, CSI, Flash memory in low power mode	36	50	
		VOS4, CSI, Flash memory in normal mode	38	48	
		VOS4, CSI, Flash memory in low-power mode	47	61	
		VOS5, CSI, Flash memory in normal mode	52	64	
		VOS5, CSI, Flash memory in low-power mode	62	77	
$t_{WUSTOP2}$(2)	Wakeup from Stop, clock kept running	VOS3, HSI, Flash memory in normal mode	2.6	3.4	
		VOS3, CSI, Flash memory in normal mode	26	36	
$t_{WUSTDBY}$(2)	Wakeup from Standby mode	-	390	500	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

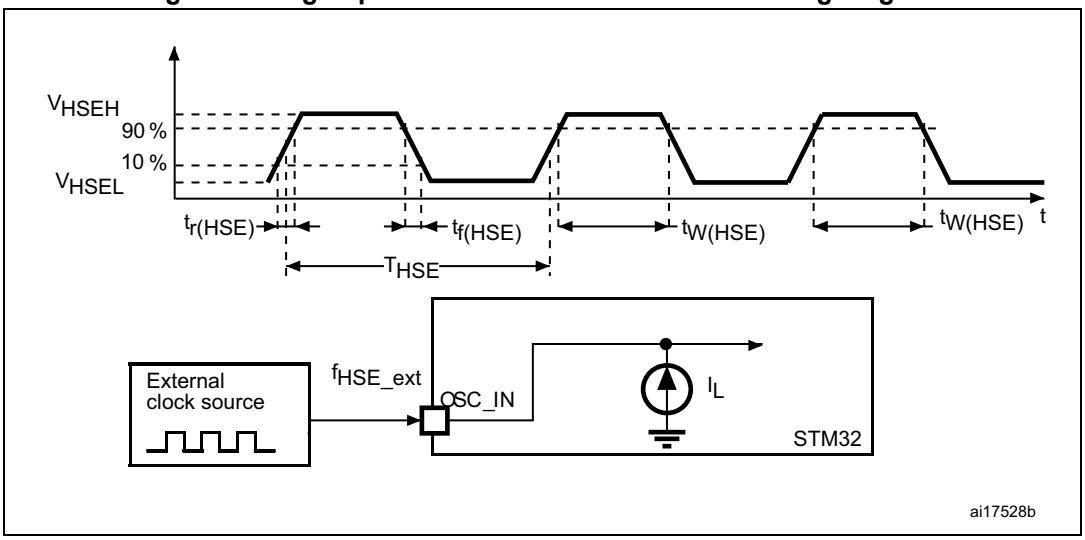
The external clock signal has to respect the *Table 59: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 17*.

Table 41. High-speed external user clock characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	4	25	50	MHz
V_{HSEH}	Digital OSC_IN input high-level voltage	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input low-level voltage	V_{SS}	-	0.3 V_{DD}	
$t_{W(HSE)}$	OSC_IN high or low time	7	-	-	ns

1. Guaranteed by design.

Figure 17. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 59: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 18*.

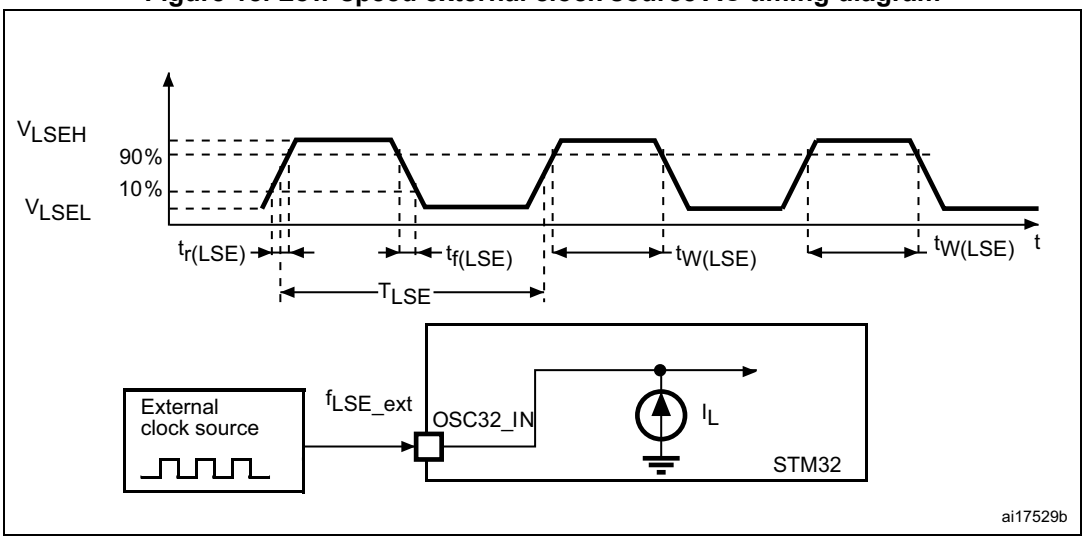
Table 42. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 18. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 43. 4-48 MHz HSE oscillator characteristics(1)

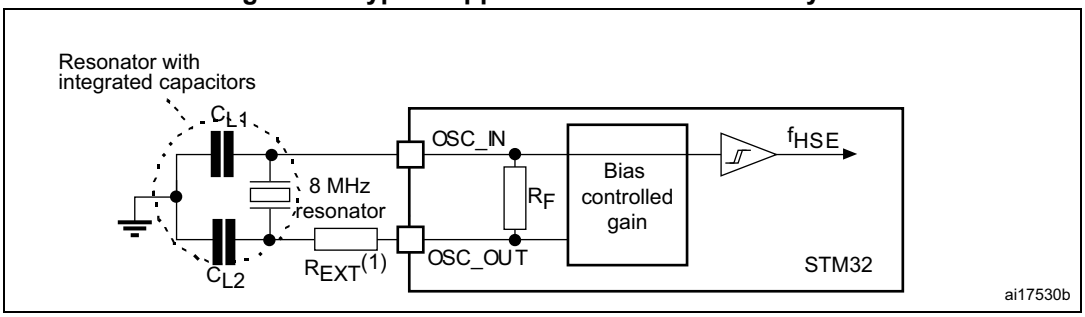
Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	4	mA
		V_{DD}=3 V, Rm=30 Ω C_L=10pF@4MHz	-	0.35	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 8 MHz	-	0.40	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 16 MHz	-	0.45	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 32 MHz	-	0.65	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 48 MHz	-	0.95	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
t_{SU}(4)	Start-up time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 19*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 19. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 44. Low-speed external user clock characteristics(1)

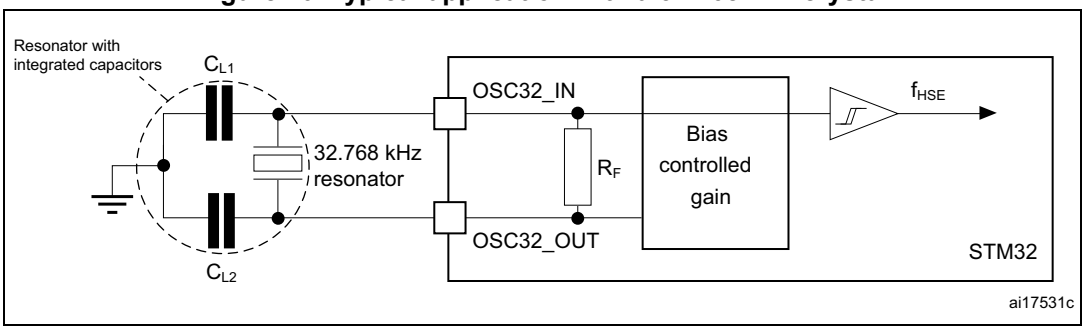
Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 00, Low drive capability	-	290	-	nA
		LSEDRV[1:0] = 01, Medium Low drive capability	-	390	-	
		LSEDRV[1:0] = 10, Medium high drive capability	-	550	-	
		LSEDRV[1:0] = 11, High drive capability	-	900	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(3)	Startup time	VDD is stabilized	-	2	-	s

1. Guaranteed by design.

2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for STM8AL/AF/S, STM32 MCUs and MPUs”.
3. t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768k Hz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for STM8AL/AF/S, STM32 MCUs and MPUs” available from the ST website www.st.com.

Figure 20. Typical application with a 32.768 kHz crystal



1. *An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

6.3.9 Internal clock source characteristics

The parameters given in *Table 45* and *Table 48* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*.

48 MHz high-speed internal RC oscillator (HSI48)

Table 45. HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD}=3.3 V, TJ=30 °C	47.5(1)	48	48.5(1)	MHz
TRIM(2)	USER trimming step	-	-	0.17	-	%
USER TRIM COVERAGE(3)	USER TRIMMING Coverage	± 32 steps	-	±5.45	-	%
DuCy(HSI48)(2)	Duty Cycle	-	45	-	55	%
ACCHSI48_REL(3)	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD}=1.62 to 3.6 V, T_J=-40 to 125 °C	–4.5	-	3.5	%
ΔVDD(HSI48)(3)	HSI48 oscillator frequency drift with V_{DD}(4)	V_{DD}=3 to 3.6 V	-	0.025	0.05	%
		V_{DD}=1.62 V to 3.6 V	-	0.05	0.1	
$t_{su(HSI48)}$(2)	HSI48 oscillator start-up time	-	-	2.1	3.5	µs
$I_{DD(HSI48)}$(2)	HSI48 oscillator power consumption	-	-	350	400	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(5)	-	-	± 0.15	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(5)	-	-	± 0.25	-	ns

1. Guaranteed by test in production.
2. Guaranteed by design.
3. Guaranteed by characterization.
4. These values are obtained by using the formula:
(Freq(3.6V) - Freq(3.0V)) / Freq(3.0V) or (Freq(3.6V) - Freq(1.62V)) / Freq(1.62V).
5. Jitter measurements are performed without clock source activated in parallel.

64 MHz high-speed internal RC oscillator (HSI)

Table 46. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	V_{DD}=3.3 V, T_J=30 °C	63.7(2)	64	64.3(2)	MHz
TRIM	HSI user trimming step	Trimming is not a multiple of 32	-	0.24	0.32	%
		Trimming is 128, 256 and 384	−5.2	−1.8	-	
		Trimming is 64, 192, 320 and 448	−1.4	−0.8	-	
		Other trimming are a multiple of 32 (not including multiple of 64 and 128)	−0.6	−0.25	-	
DuCy(HSI)	Duty Cycle	-	45	-	55	%
$\Delta_{VDD\ (HSI)}$	HSI oscillator frequency drift over V_{DD} (reference is 3.3 V)	V_{DD}=1.62 to 3.6 V	−0.12	-	0.03	%
$\Delta_{TEMP\ (HSI)}$	HSI oscillator frequency drift over temperature (reference is 64 MHz)	T_J=-20 to 105 °C	−1(3)	-	1(3)	%
		T_J=−40 to $T_J$max °C	−2(3)	-	1(3)	
t_{su}(HSI)	HSI oscillator start-up time	-	-	1.4	2	µs
t_{stab}(HSI)	HSI oscillator stabilization time	at 1% of target frequency	-	4	8	µs
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	400	µA

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by test in production.
3. Guaranteed by characterization.

4 MHz low-power internal RC oscillator (CSI)

Table 47. CSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CSI}	CSI frequency	V_{DD}=3.3 V, T_J=30 °C	3.96(2)	4	4.04(2)	MHz
TRIM	Trimming step	-	-	0.35	-	%
DuCy(CSI)	Duty Cycle	-	45	-	55	%

Table 47. CSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Δ_{TEMP} (CSI)	CSI oscillator frequency drift over temperature	T_J = 0 to 85 °C	-	−3.7(3)	4.5(3)	%
		T_J = −40 to 125 °C	-	−11(3)	7.5(3)	
D_{VDD} (CSI)	CSI oscillator frequency drift over V_{DD}	V_{DD} = 1.62 to 3.6 V	-	−0.06	0.06	%
$t_{su(CSI)}$	CSI oscillator startup time	-	-	1	2	µs
$t_{stab(CSI)}$	CSI oscillator stabilization time (to reach ±3% of f_{CSI})	-	-	4	8	cycle
$I_{DD(CSI)}$	CSI oscillator power consumption	-	-	23	30	µA

1. Guaranteed by design.
2. Guaranteed by test in production.
3. Guaranteed by characterization.

Low-speed internal (LSI) RC oscillator

Table 48. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(1)	LSI frequency	V_{DD} = 3.3 V, T_J = 25 °C	31.4	32	32.6	kHz
		T_J = –40 to 105 °C, V_{DD} = 1.62 to 3.6 V	29.76	-	33.60	
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	80	130	µs
$t_{stab(LSI)}$(2)	LSI oscillator stabilization time (5% of final value)	-	-	120	170	
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	-	130	280	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.10 PLL characteristics

The parameters given in *Table 49* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 49. PLL characteristics (wide VCO frequency range)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	2	-	16	MHz
	PLL input clock duty cycle	-	10	-	90	%

Table 49. PLL characteristics (wide VCO frequency range)(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{PLL_P_OUT}$	PLL multiplier output clock P	VOS1		1.5	-	400(2)	MHz
		VOS2		1.5	-	300	
		VOS3		1.5	-	200	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q/R	VOS1		1.5	-	400(2)	
		VOS2		1.5	-	300	
		VOS3		1.5	-	200	
f_{VCO_OUT}	PLL VCO output	-		192	-	836	
t_{LOCK}	PLL lock time	Normal mode		-	50(3)	150(3)	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)		-	58(3)	166(3)	
Jitter	Cycle-to-cycle jitter(4)	VCO = 192 MHz		-	134	-	±ps
		VCO = 200 MHz		-	134	-	
		VCO = 400 MHz		-	76	-	
		VCO = 800 MHz		-	39	-	
	Long term jitter	Normal mode		-	±0.7	-	%
		Sigma-delta mode (CKIN = 16 MHz)		-	±0.8	-	
$I_{DD(PLL)}$(3)	PLL power consumption on V_{DD}	VCO freq = 420 MHz	V_{DDA}	-	440	1150	µA
			V_{CORE}	-	530	-	
		VCO freq = 150 MHz	V_{DDA}	-	180	500	
			V_{CORE}	-	200	-	

1. Guaranteed by design unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation (400 MHz for VOS1, 300 MHz for VOS2, 200 MHz for VOS3).
3. Guaranteed by characterization results.
4. Integer mode only.

Table 50. PLL characteristics (medium VCO frequency range)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	1	-	2	MHz
	PLL input clock duty cycle	-	10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS1	1.17	-	210	MHz
		VOS2	1.17	-	210	
		VOS3	1.17	-	200	
f_{VCO_OUT}	PLL VCO output	-	150	-	420	MHz
t_{LOCK}	PLL lock time	Normal mode	-	60(2)	100(2)	µs
		Sigma-delta mode	forbidden	-	-	µs

Table 50. PLL characteristics (medium VCO frequency range)(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter	Cycle-to-cycle jitter(3)	-	VCO = 150 MHz	-	145	-	+/- ps
			VCO = 300 MHz	-	91	-	
			VCO = 400 MHz	-	64	-	
			VCO = 420 MHz	-	63	-	
	Period jitter	f_{PLL_OUT} = 50 MHz	VCO = 150 MHz	-	55	-	+/- ps
			VCO = 400 MHz	-	30	-	
	Long term jitter	Normal mode	VCO = 150 MHz	-	-	-	%
			VCO = 300 MHz	-	-	-	
			VCO = 400 MHz	-	+/-0.3	-	
I(PLL)(2)	PLL power consumption on V_{DD}	VCO freq = 420MHz	VDD	-	440	1150	µA
			VCORE	-	530	-	
		VCO freq = 150MHz	VDD	-	180	500	
			VCORE	-	200	-	

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by characterization results.
3. Integer mode only.

6.3.11 Memory characteristics

Flash memory

The characteristics are given at T_J = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 51. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode	-	6.5	-	mA
		Write / Erase 16-bit mode	-	11.5	-	
		Write / Erase 32-bit mode	-	20	-	
		Write / Erase 64-bit mode	-	35	-	

Table 52. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word (266 bits) programming time	Program/erase parallelism x 8	-	290	580(2)	µs
		Program/erase parallelism x 16	-	180	360	
		Program/erase parallelism x 32	-	130	260	
		Program/erase parallelism x 64	-	100	200	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism x 8	-	2	4	s
		Program/erase parallelism x 16	-	1.8	3.6	
		Program/erase parallelism x 32	-	1.1	2.2	
		Program/erase parallelism x 64	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism x 8	-	13	26	
		Program/erase parallelism x 16	-	8	16	
		Program/erase parallelism x 32	-	6	12	
		Program/erase parallelism x 64	-	5	10	
V_{prog}	Programming voltage	Program parallelism x 8	1.62	-	3.6	V
		Program parallelism x 16				
		Program parallelism x 32				
		Program parallelism x 64	1.8	-	3.6	

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 10K erase operations.

Table 53. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_J = –40 to +125 °C (6 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle at T_A = 85 °C	30	Years
		10 kcycles at T_A = 55 °C	20	

1. Guaranteed by characterization results.

6.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 54*. They are based on the EMS levels and classes defined in application note AN1709.

Table 54. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, UFBGA240, $f_{rcc_c_ck}$ = 400 MHz, conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance		4B

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 55. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/400 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, UFBGA240 package, conforming to IEC61967-2	0.1 to 30 MHz	6	dBµV
			30 to 130 MHz	5	
			130 MHz to 1 GHz	13	
			1 GHz to 2 GHz	7	
			EMI Level	2.5	-

6.3.13 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 56. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	All	1C	1000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All	C1	250	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 57. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_A = +25 °C conforming to JESD78	II level A

6.3.14 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 58. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	PA7, PC5, PG1, PB14, PJ7, PA11, PA12, PA13, PA14, PA15, PJ12, PB4	5	0	mA
	PA2, PH2, PH3, PE8, PA6, PA7, PC4, PE7, PE10, PE11	0	NA	
	PA0, PA_C, PA1, PA1_C, PC2, PC2_C, PC3, PC3_C, PA4, PA5, PH4, PH5, BOOT0	0	0	
	All other I/Os	5	NA	

1. Guaranteed by characterization.

6.3.15 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 59: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 23: General operating conditions*. All I/Os are CMOS and TTL compliant (except for BOOT0).

For information on GPIO configuration, refer to the application note AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption” available from the ST website www.st.com.

Table 59. I/O static characteristics

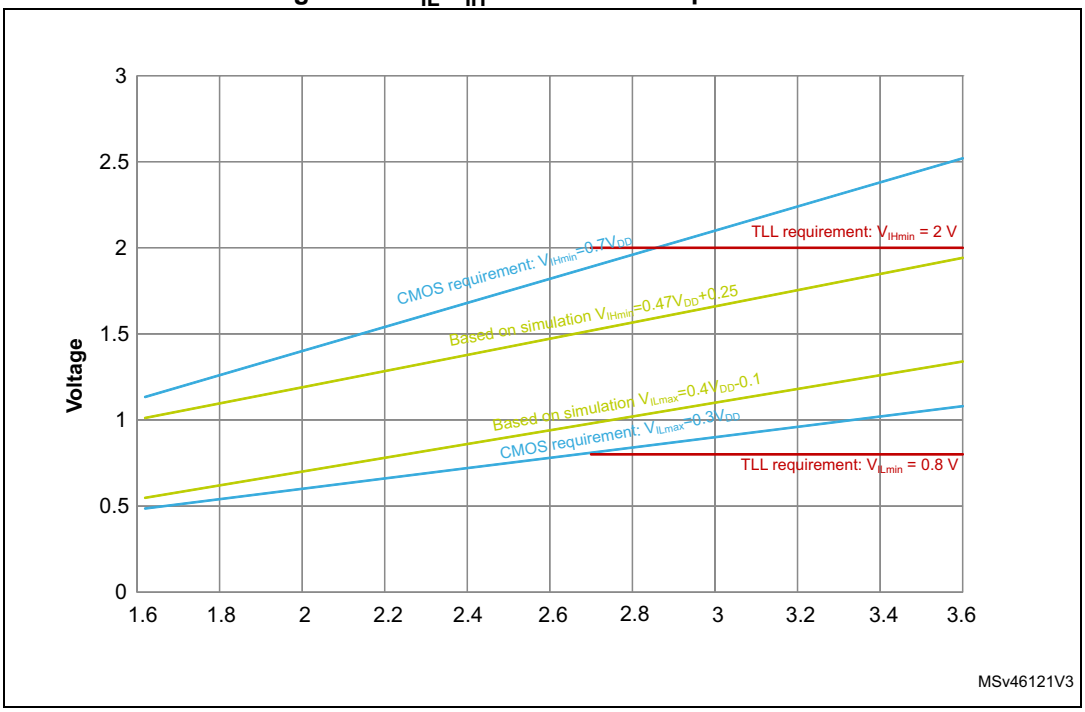
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.3V_{DD}$(1)	V
	I/O input low level voltage except BOOT0		-	-	$0.4V_{DD}-0.1$(2)	
	BOOT0 I/O input low level voltage		-	-	$0.19V_{DD}+0.1$(2)	
V_{IH}	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	$0.7V_{DD}$(1)	-	-	V
	I/O input high level voltage except BOOT0(3)		$0.47V_{DD}+0.25$(2)	-	-	
	BOOT0 I/O input high level voltage(3)		$0.17V_{DD}+0.6$(2)	-	-	
V_{HYS}(2)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V< V_{DDIOx} <3.6 V	-	250	-	mV
	BOOT0 I/O input hysteresis		-	200	-	
I_{leak}(4)	FT_xx Input leakage current(2)	0< V_{IN} ≤ Max(V_{DDXXX})(9)	-	-	+/-250	nA
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(6)(9)	-	-	1500	
	FT_u IO	0< V_{IN} ≤ Max(V_{DDXXX})(9)	-	-	+/- 350	
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(6)(9)	-	-	5000(7)	
	TT_xx Input leakage current	0< V_{IN} ≤ Max(V_{DDXXX}) (9)	-	-	+/-250	
	VPP (BOOT0 alternate function)	0< V_{IN} ≤ V_{DDIOX}	-	-	15	
		V_{DDIOX} < V_{IN} ≤ 9 V			35	
R_{PU}	Weak pull-up equivalent resistor(8)	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(8)	V_{IN}=V_{DD}(9)	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Compliant with CMOS requirement.
2. Guaranteed by design.

3. V_{DDIOx} represents V_{DDIO1}, V_{DDIO2} or V_{DDIO3}. V_{DDIOx}= V_{DD}.
4. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total_Ileak_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x $I_{lkg(Max)}$.
5. All FT_xx IO except FT_lu, FT_u and PC3.
6. V_{IN} must be less than Max(VDDXXX) + 3.6 V.
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, $V_{DD33USB}$) +0.3 V, the internal pull-up and pull-down resistors must be disabled.
8. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).
9. Max(VDDXXX) is the maximum value of all the I/O supplies.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 21*.

Figure 21. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 21*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 21*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 60* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 60. Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO}=8 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO}=-8 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO}=8 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO}=-8 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO}=20 mA 2.7 V≤ V_{DD} ≤3.6 V	-	1.3	
V_{OH}(3)	Output high level voltage	I_{IO}=-20 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−1.3	-	
V_{OL}(3)	Output low level voltage	I_{IO}=4 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage	I_{IO}=-4 mA 1.62 V≤V_{DD}<3.6 V	V_{DD}−-0.4	-	
V_{OLFM+}(3)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO}= 20 mA 2.3 V≤ V_{DD}≤3.6 V	-	0.4	
		I_{IO}= 10 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 20: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Table 61. Output voltage characteristics for PC13, PC14, PC15 and PI8(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO}=3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO}=-3 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO}=3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO}=-3 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO}=1.5 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	I_{IO}=-1.5 mA 1.62 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 20: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of SYSCFG_CCCSR register can be used to optimize the I/O speed when the product voltage is below 2.5 V.

Table 62. Output timing characteristics (HSLV OFF)(1)(2)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	12	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	12	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	16	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	4	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	16.6	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	33.3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	13.3	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
01	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	60	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	80	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	110	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	5.2	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.2	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	7.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	2.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	5.2	

Table 62. Output timing characteristics (HSLV OFF)(1)(2) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
10	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	85	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	35	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	110	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	40	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	166	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	85	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	3.8	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	6.9	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	2.8	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	5.2	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	1.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	3.3	
11	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	100	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	50	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	133	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	66	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	220	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	100	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	3.3	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	6.6	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	2.4	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	4.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	1.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	2.7	

1. Guaranteed by design.
2. The frequency of the GPIOs that can be supplied in V_{BAT} mode (PC13, PC14, PC15 and PI8) is limited to 2 MHz
3. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
4. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
5. Compensation system enabled.

Output buffer timing characteristics (HSLV option enabled)

Table 63. Output timing characteristics (HSLV ON)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	11	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	9	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	
01	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	50	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	58	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	66	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	4.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
10	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	55	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	80	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	133	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.8	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	4	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	2.4	
11	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	60	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	90	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	175	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.3	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	3.6	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	1.9	

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 59: I/O static characteristics*).

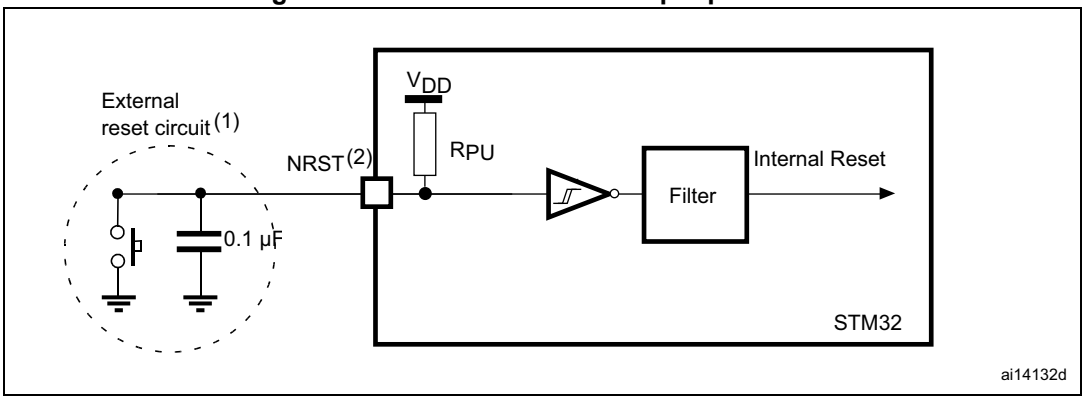
Unless otherwise specified, the parameters given in *Table 64* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 64. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	1.71 V < V_{DD} < 3.6 V	300	-	-	
		1.62 V < V_{DD} < 3.6 V	1000	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 22. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 59*. Otherwise the reset is not taken into account by the device.

6.3.17 FMC characteristics

Unless otherwise specified, the parameters given in *Table 65* to *Table 78* for the FMC interface are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

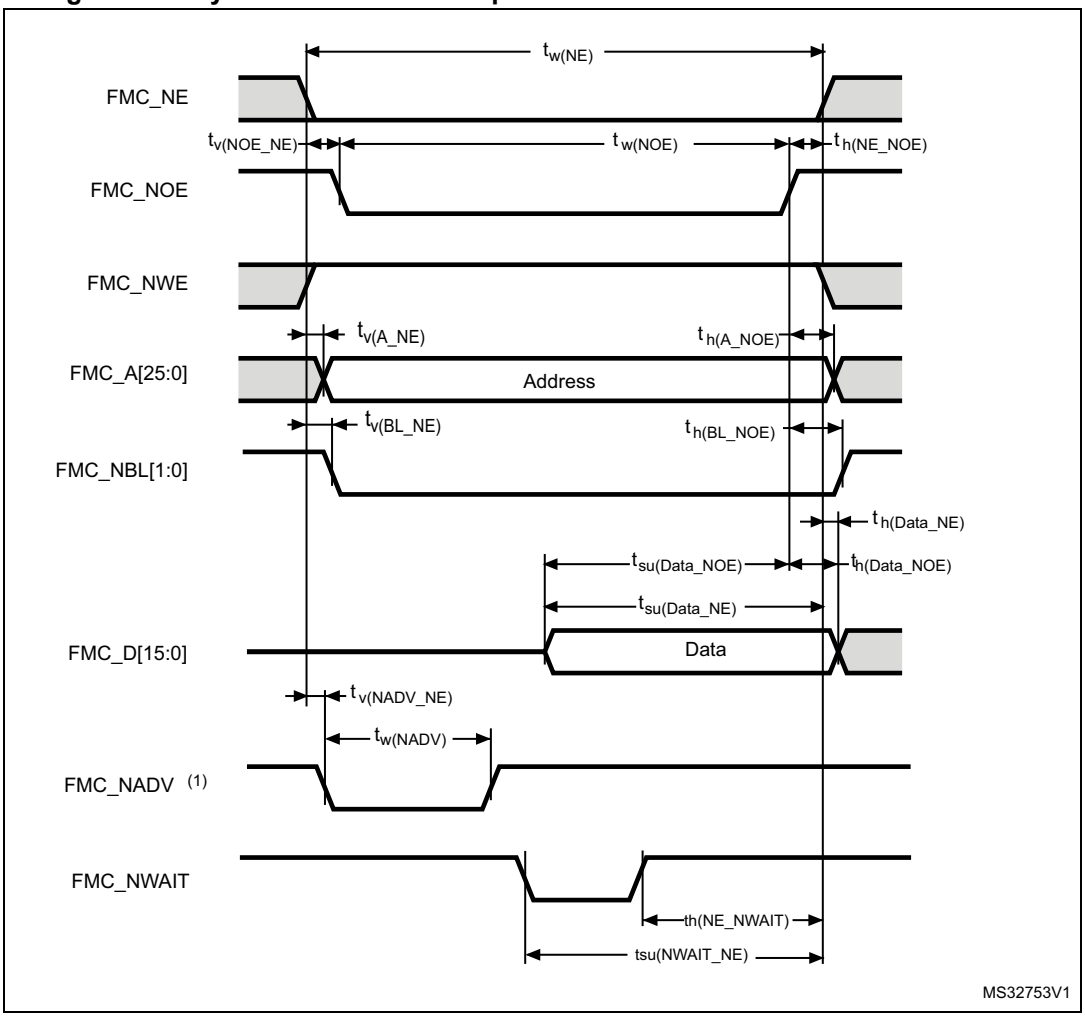
Asynchronous waveforms and timings

Figure 23 through *Figure 26* represent asynchronous waveforms and *Table 65* through *Table 72* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capcitive load C_L = 30 pF

In all timing tables, the T_{KERCK} is the $f_{mc_ker_ck}$ clock period.

Figure 23. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 65. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{fmc_ker_ck} - 1$	$2\ T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	11	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	11	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck} + 1$	

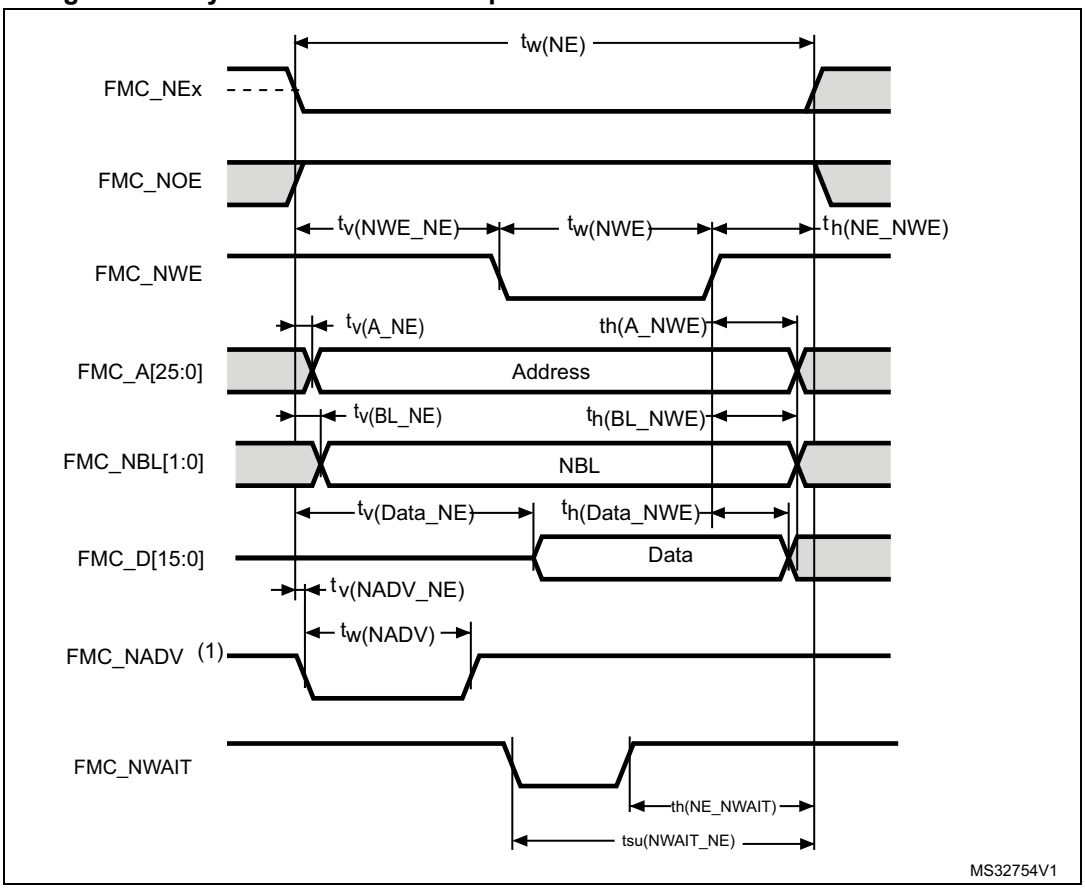
1. Guaranteed by characterization results.

Table 66. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{fmc_ker_ck} + 1$	$7T_{fmc_ker_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc_ker_ck} - 1$	$5T_{fmc_ker_ck} + 1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc_ker_ck} - 0.5$		
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4T_{fmc_ker_ck} + 11$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$3T_{fmc_ker_ck} + 11.5$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Figure 24. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 67. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck} - 1$	$3T_{fmc_ker_ck}$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck}$	$T_{fmc_ker_ck} + 1$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck}$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{fmc_ker_ck} + 2.5$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck}+0.5$	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck} + 1$	

1. Guaranteed by characterization results.

Table 68. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck} - 1$	$8T_{fmc_ker_ck} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc_ker_ck} - 1.5$	$6T_{fmc_ker_ck} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 13$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck} + 13$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Figure 25. Asynchronous multiplexed PSRAM/NOR read waveforms

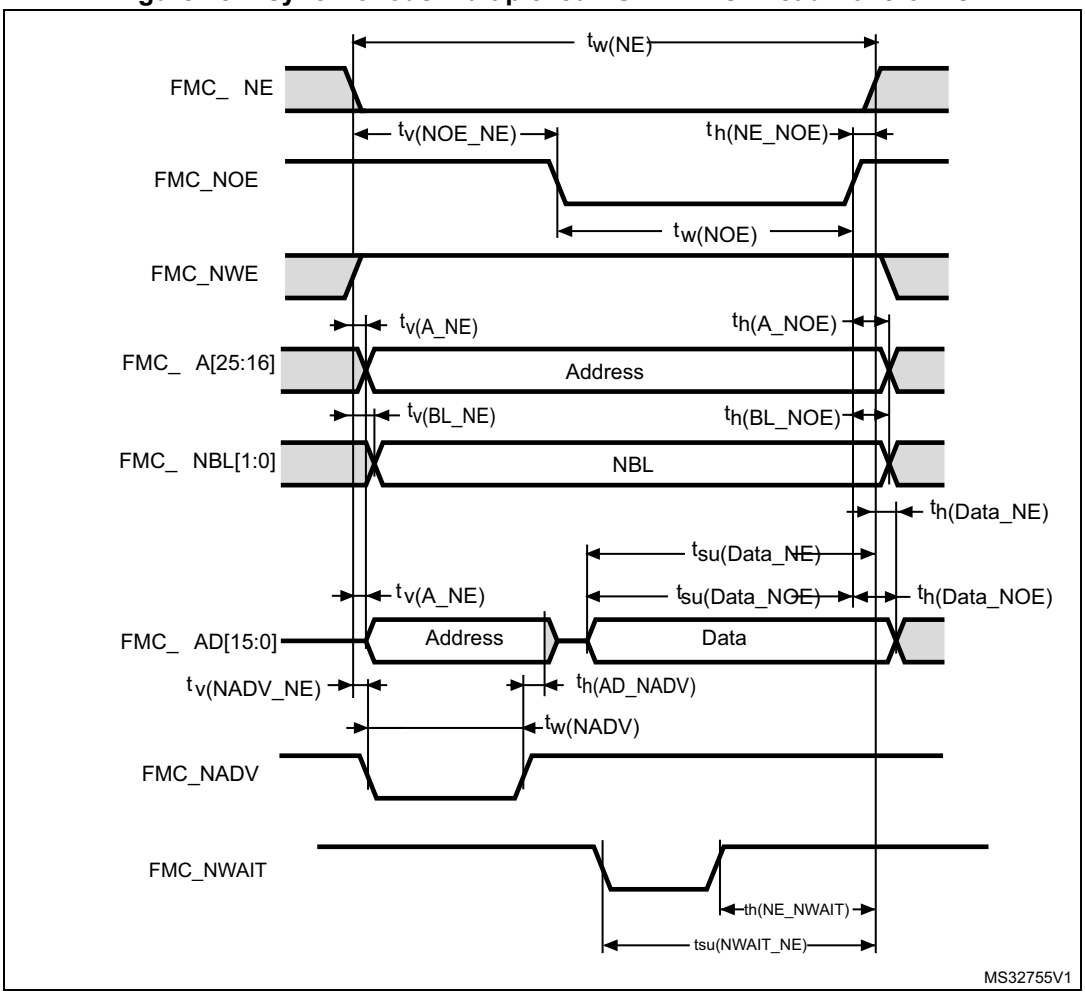


Table 69. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck} - 1$	$3T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc_ker_ck}$	$2T_{fmc_ker_ck} + 0.5$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck}+1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{h(BL_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} - 2$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	$T_{fmc_ker_ck} - 2$	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Guaranteed by characterization results.

Table 70. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck} - 1$	$8T_{fmc_ker_ck}$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc_ker_ck} - 1.5$	$5T_{fmc_ker_ck} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 3$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}$	-	

1. Guaranteed by characterization results.

Figure 26. Asynchronous multiplexed PSRAM/NOR write waveforms

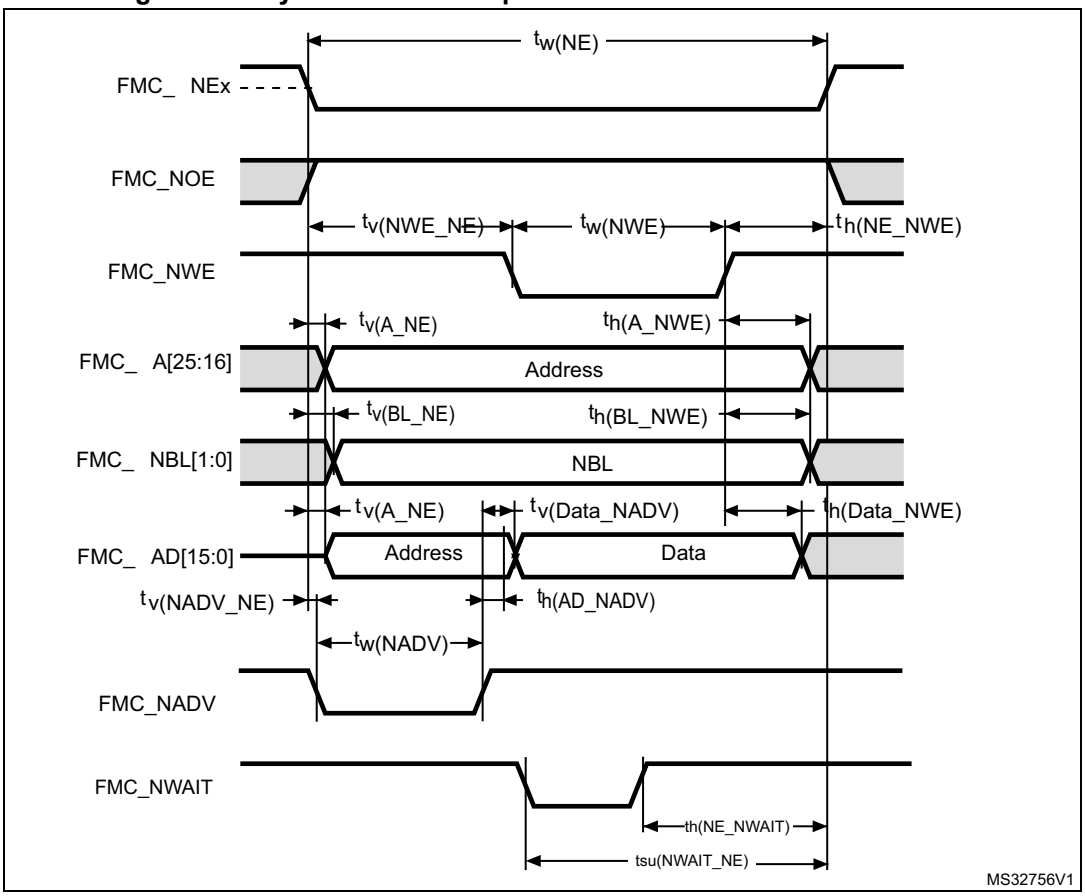


Table 71. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_c} - 1$	$4T_{fmc_ker_ck}$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_c} - 1$	$T_{fmc_ker_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc_ker_ck} - 0.5$	$2T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck}$	$T_{fmc_ker_ck} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck}+0.5$	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck}+0.5$	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc_ker_ck} + 2$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck}+0.5$	-	

1. Guaranteed by characterization results.

Table 72. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck} - 1$	$9T_{fmc_ker_ck}$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc_ker_ck} - 0.5$	$7T_{fmc_ker_ck} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{fmc_ker_ck} + 3$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 27 through *Figure 30* represent synchronous waveforms and *Table 73* through *Table 76* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc_ker_ck}$ is the $f_{mc_ker_ck}$ clock period, with the following FMC_CLK maximum values:

- For 2.7 V<V_{DD}<3.6 V, FMC_CLK =100 MHz at 20 pF
- For 1.8 V<V_{DD}<1.9 V, FMC_CLK =100 MHz at 20 pF
- For 1.62 V<V_{DD}<1.8 V, FMC_CLK =100 MHz at 15 pF

Figure 27. Synchronous multiplexed NOR/PSRAM read timings

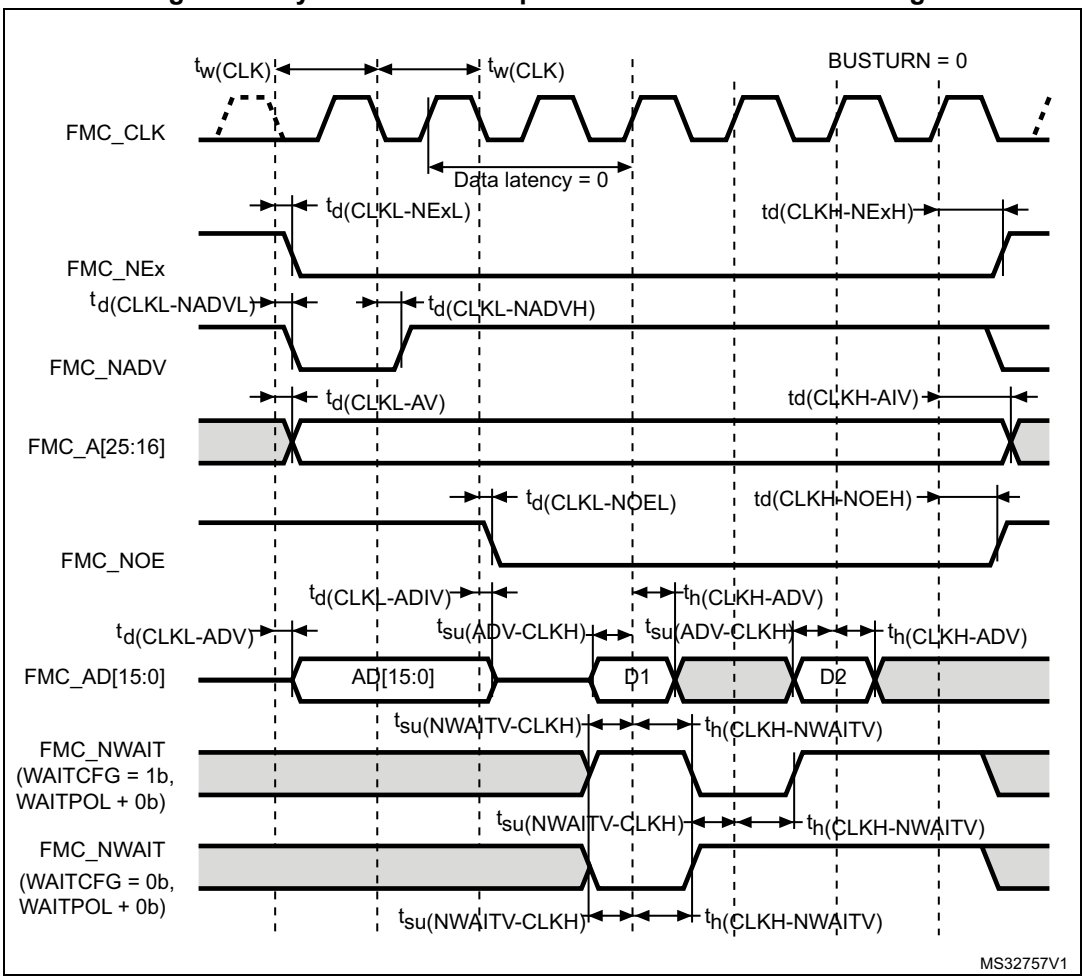


Table 73. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc_ker_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	3	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	0	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	

1. Guaranteed by characterization results.

Figure 28. Synchronous multiplexed PSRAM write timings

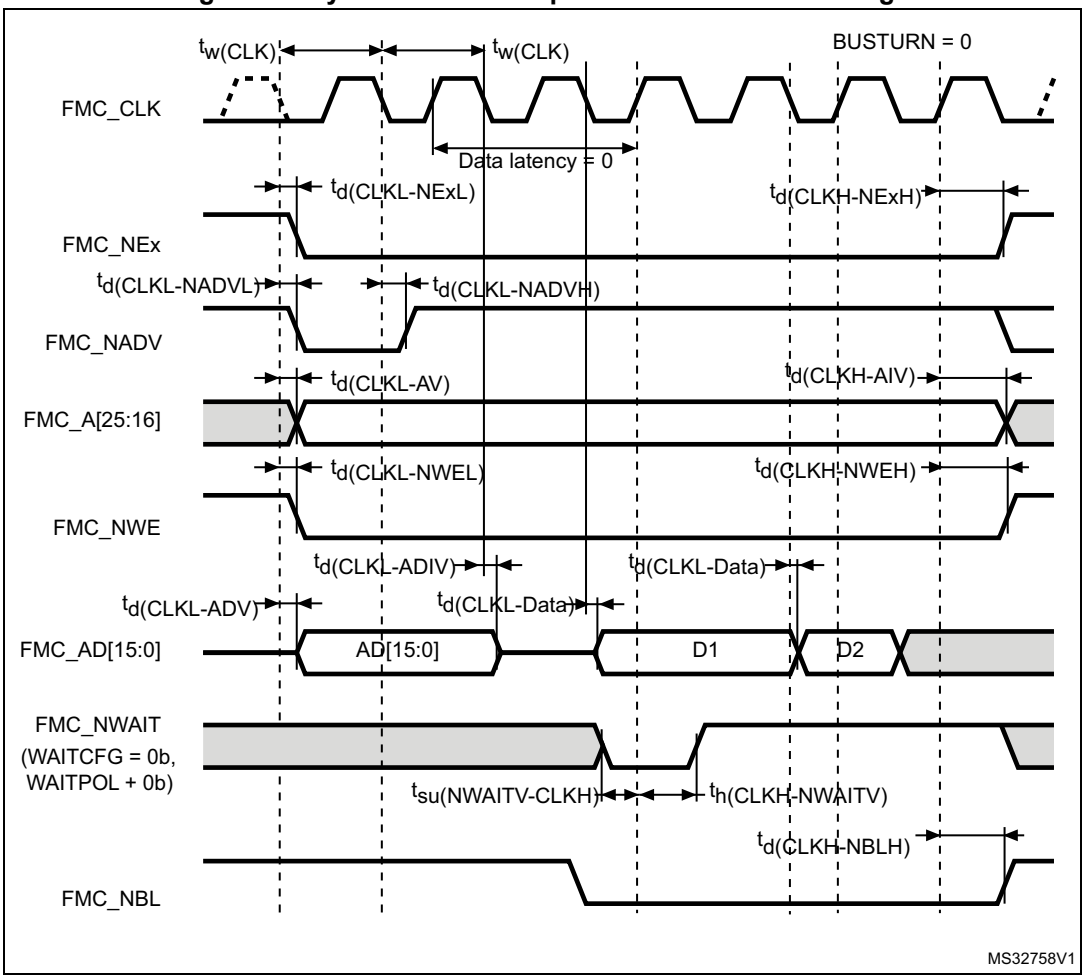


Table 74. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc_ker_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	2.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Figure 29. Synchronous non-multiplexed NOR/PSRAM read timings

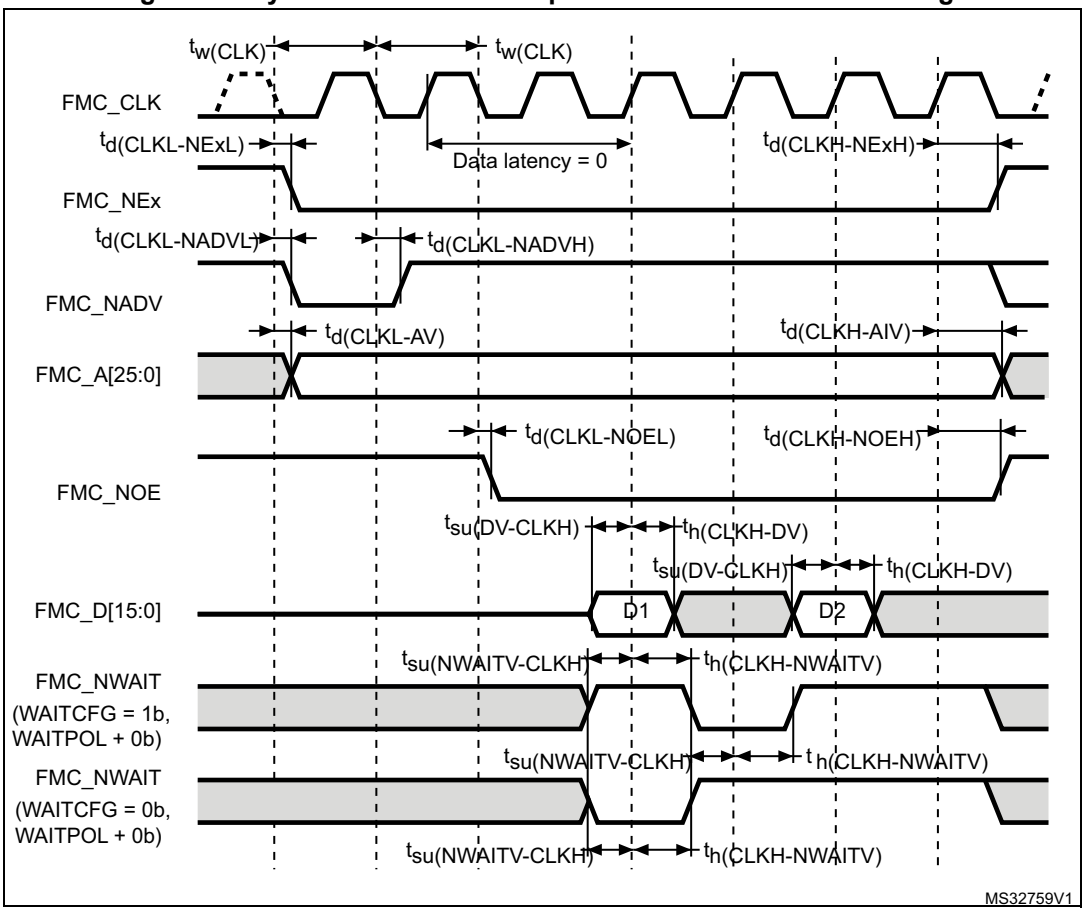


Table 75. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck} - 1$	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc_ker_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	0	-	
$t_{SU(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	

1. Guaranteed by characterization results.

Figure 30. Synchronous non-multiplexed PSRAM write timings

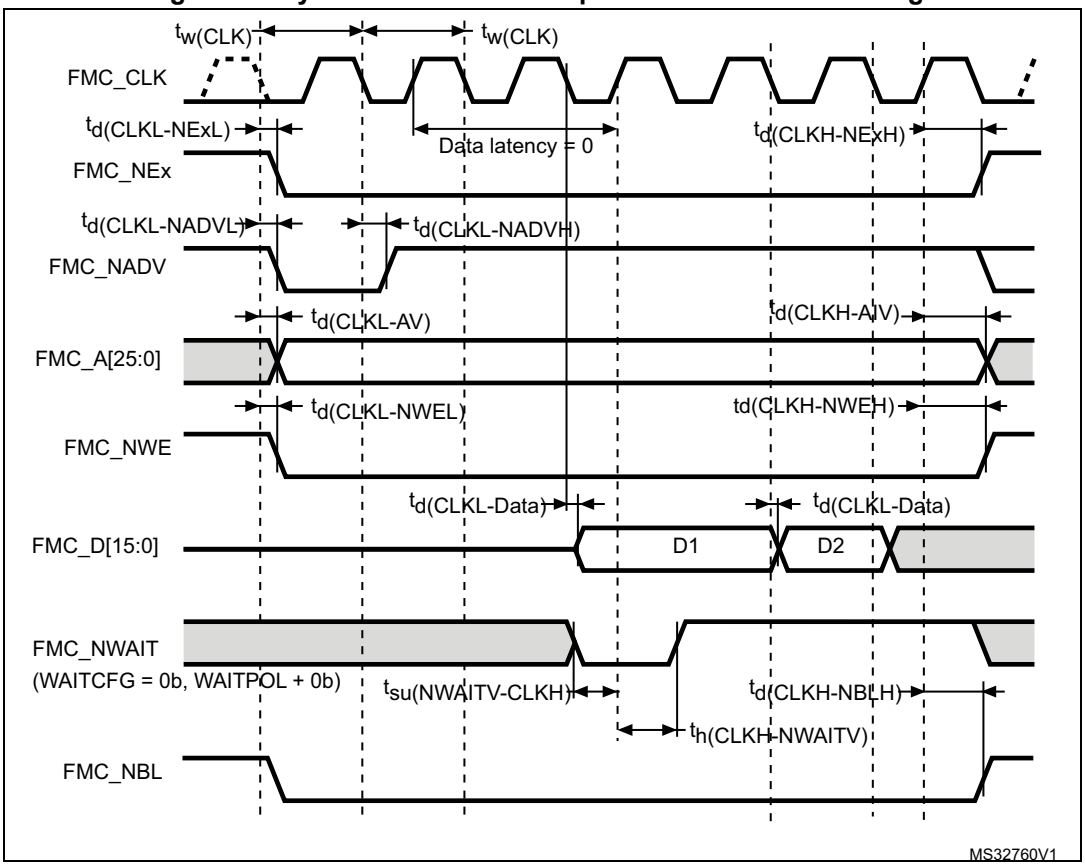


Table 76. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc_ker_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc_ker_ck} + 1$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc_ker_ck} + 1$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 31 through *Figure 34* represent synchronous waveforms, and *Table 77* and *Table 78* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- C_L = 30 pF

In all timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

Figure 31. NAND controller waveforms for read access

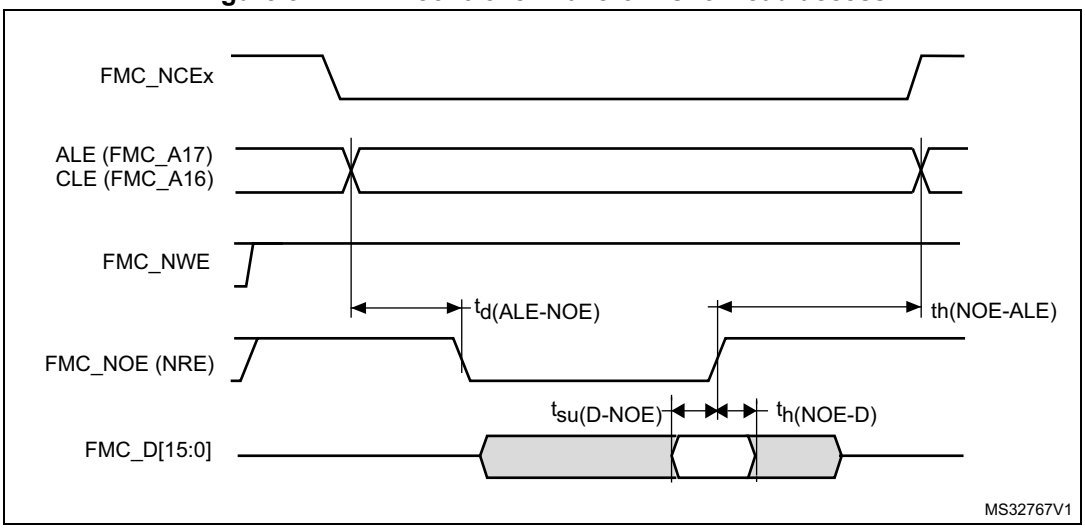


Figure 32. NAND controller waveforms for write access

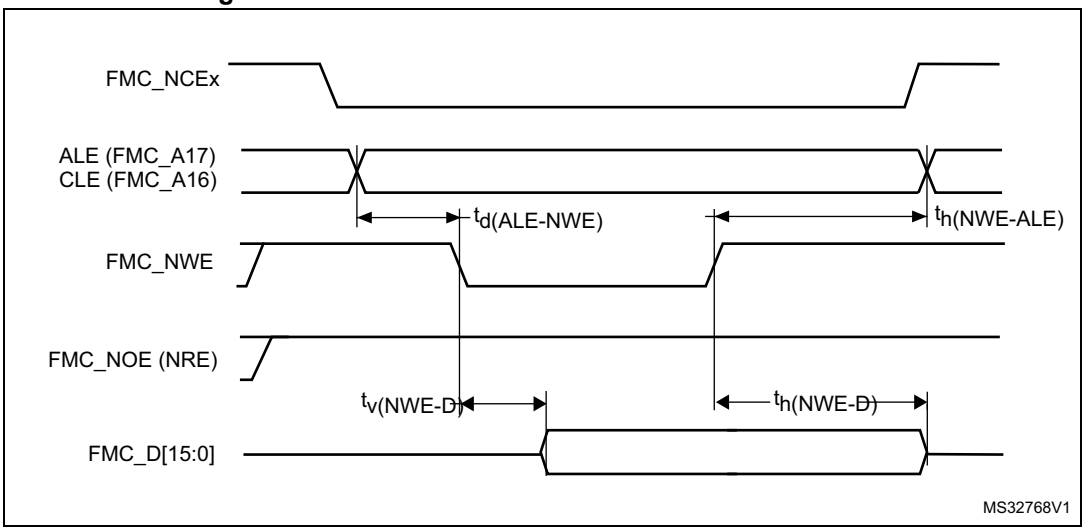


Figure 33. NAND controller waveforms for common memory read access

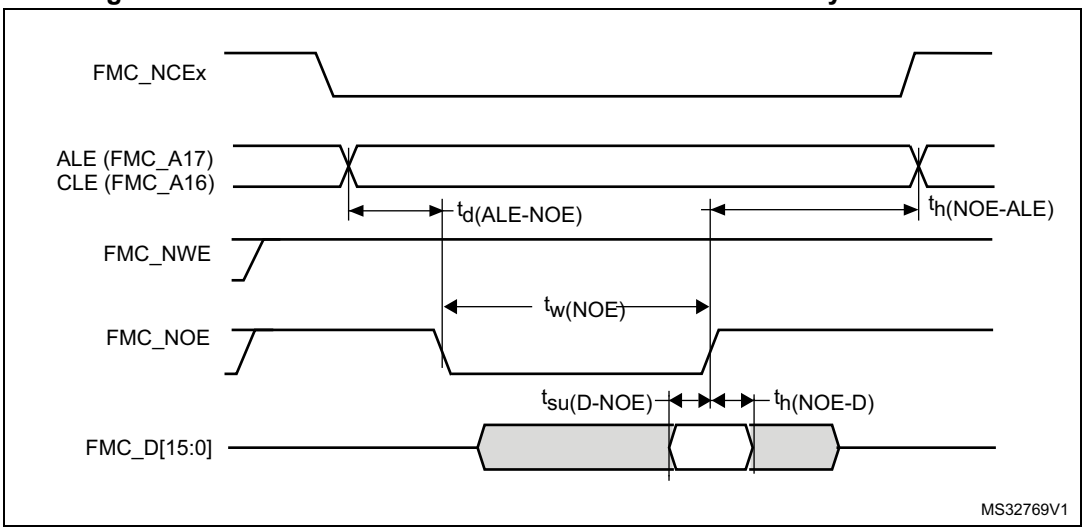


Figure 34. NAND controller waveforms for common memory write access

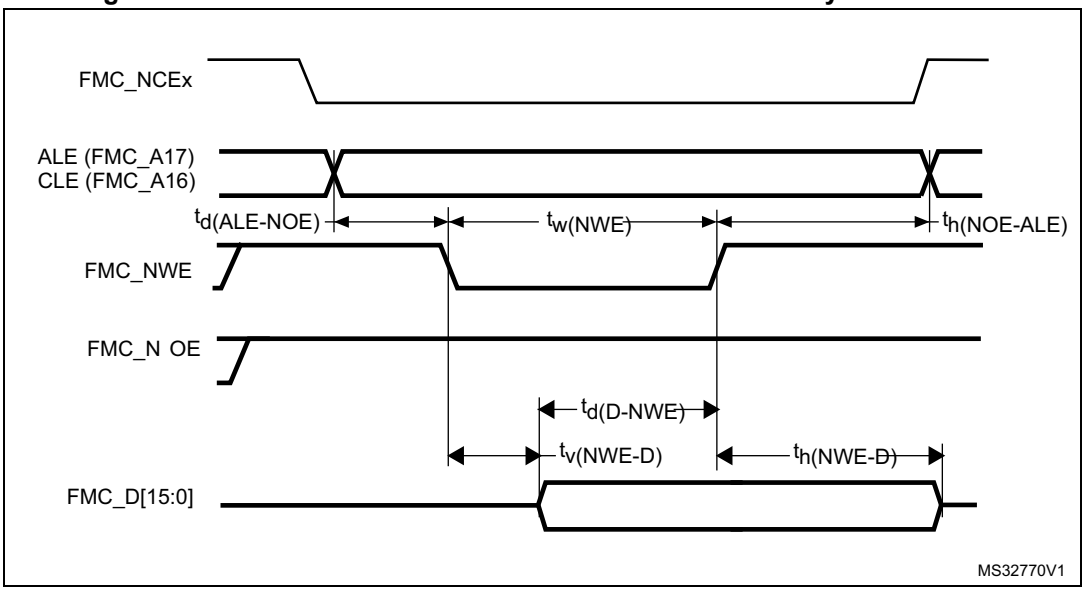


Table 77. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc_ker_ck} - 0.5$	$4T_{fmc_ker_ck} + 0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	8	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc_ker_ck} + 1$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{fmc_ker_ck} - 2$	-	

1. Guaranteed by characterization results.

Table 78. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc_ker_ck} - 0.5$	$4T_{fmc_ker_ck} + 0.5$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc_ker_ck} - 0.5$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc_ker_ck} - 1$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc_ker_ck} + 0.5$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc_ker_ck} - 1$	-	

1. Guaranteed by characterization results.

SDRAM waveforms and timings

In all timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period, with the following FMC_SDCLK maximum values:

- For 1.8 V < V_{DD} < 3.6V: FMC_SDCLK = 100 MHz at 20 pF
- For 1.62 V< V_{DD} < 1.8 V, FMC_SDCLK = 100 MHz at 15 pF

Figure 35. SDRAM read access waveforms (CL = 1)

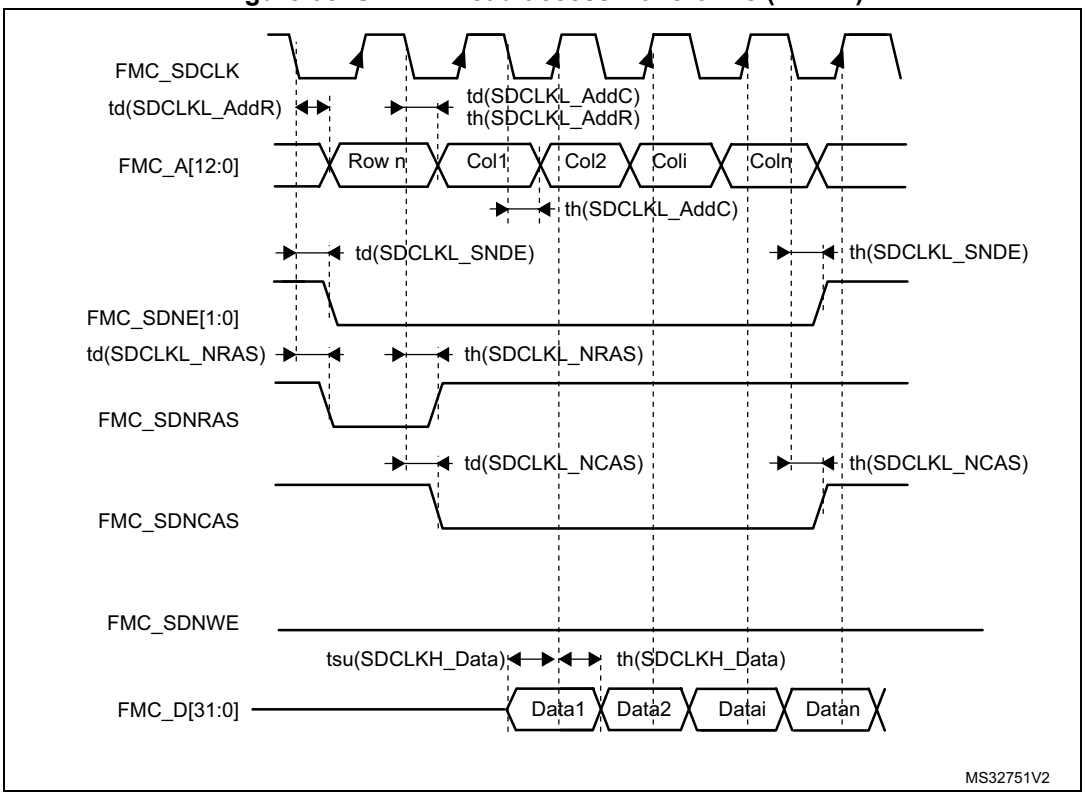


Table 79. SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck} + 0.5$	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	3	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 80. LPSDR SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck} + 0.5$	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	3	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	0.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	2.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Figure 36. SDRAM write access waveforms

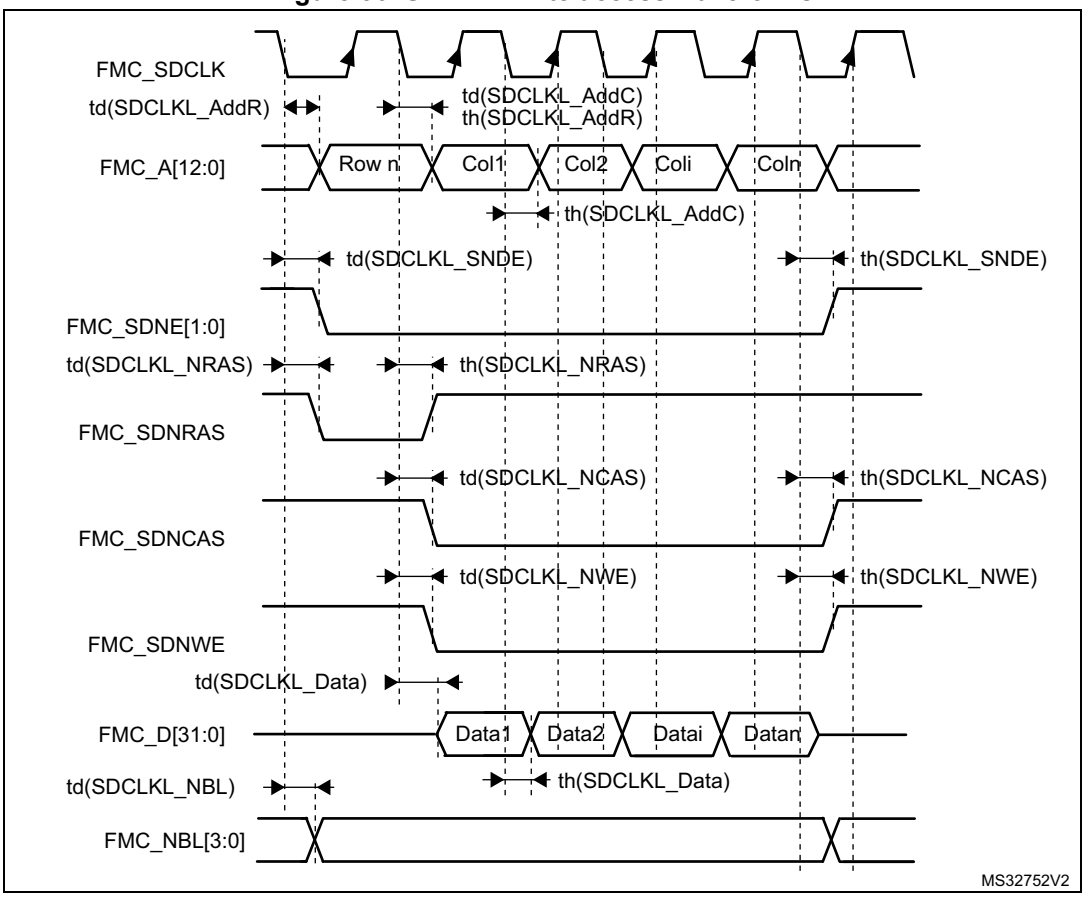


Table 81. SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck} + 0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	3	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL_SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL_SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL-_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.

Table 82. LPSDR SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck} + 0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	2.5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	2.5	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	3	
$t_{h(SDCLKL-\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

6.3.18 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 83* and *Table 84* for QUADSPI are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled
- HSLV activated when V_{DD}≤2.7 V

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 83. QUADSPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/T_{CK}	QUADSPI clock frequency	2.7 V ≤ V_{DD}<3.6 V C_L=20 pF	-	-	133	MHz
		1.62 V<V_{DD}<3.6 V C_L=15 pF	-	-	100	
$t_{w(CKH)}$	QUADSPI clock high and low time	-	T_{CK}/2–0.5	-	T_{CK}/2	ns
$t_{w(CKL)}$			T_{CK}/2	-	T_{CK}/2 + 0.5	
$t_{s(IN)}$	Data input setup time	2.7 V ≤ V_{DD} < 3.6 V	2	-	-	
		1.62 V ≤ V_{DD} < 3.6 V	2.5	-	-	
$t_{h(IN)}$	Data input hold time	2.7 V ≤ V_{DD} < 3.6 V	1	-	-	
		1.62 V ≤ V_{DD} < 3.6 V	1.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	1.5	2	
$t_{h(OUT)}$	Data output hold time	-	0.5	-	-	

1. Guaranteed by characterization results.

Table 84. QUADSPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1/t(CK)}$	QUADSPI clock frequency	2.7 V<V_{DD}<3.6 V CL=20 pF	-	-	100	MHz
		1.62 V<V_{DD}<3.6 V CL=15 pF	-	-	100	
$t_{w(CKH)}$	QUADSPI clock high and low time	-	T_{CK}/2 –0.5	-	T_{CK}/2	ns
$t_{w(CKL)}$			T_{CK}/2	-	T_{CK}/2+0.5	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	2.7 V ≤ V_{DD} < 3.6 V	3	-	-	
		1.62 V ≤ V_{DD} < 3.6 V	1	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	2.7 V ≤ V_{DD} < 3.6 V	1	-	-	
		1.62 V ≤ V_{DD} < 3.6 V	1.5	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	DHHC=0	-	3.5	4	
		DHHC=1 Pres=1, 2...	-	T_{CK}/4+3.5	T_{CK}/4+4	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	DHHC=0	3	-	-	
		DHHC=1 Pres=1, 2...	T_{CK}/4+3	-	-	

1. Guaranteed by characterization results.

Figure 37. Quad-SPI timing diagram - SDR mode

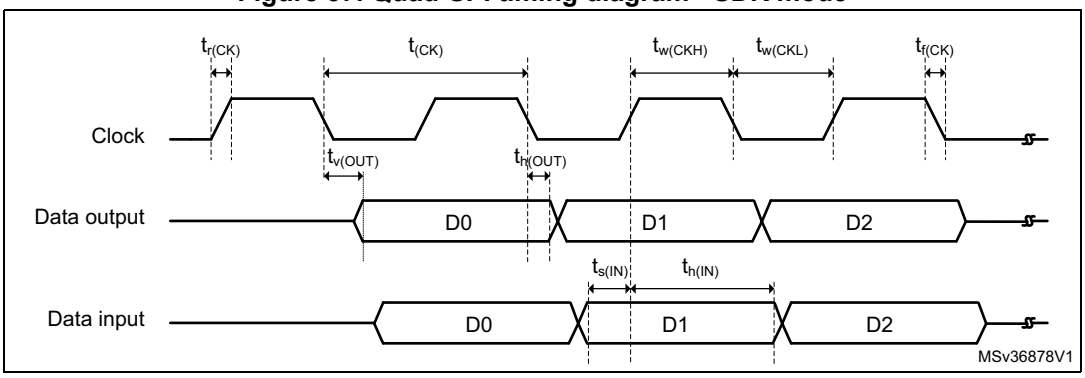
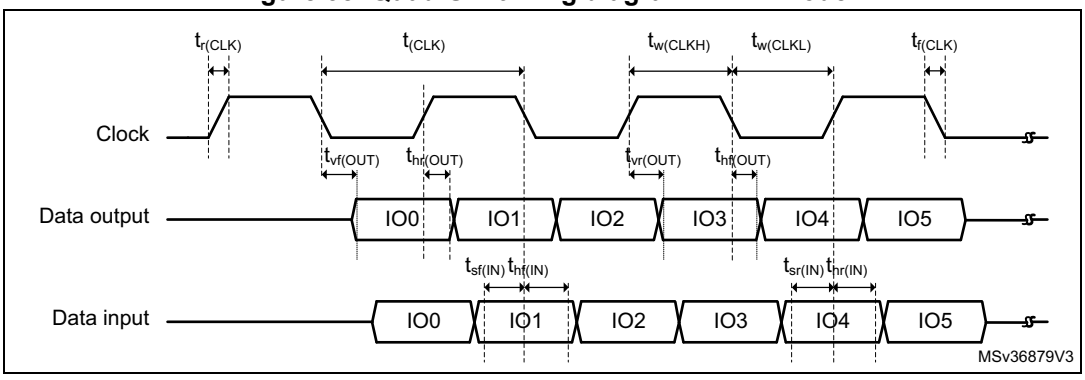


Figure 38. Quad-SPI timing diagram - DDR mode



6.3.19 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 86* for the delay block are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage summarized in *Table 23: General operating conditions*.

Table 85. Dynamics characteristics: Delay Block characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	1400	2200	2400	ps
t_{Δ}	Unit Delay	-	35	40	45	

1. Guaranteed by characterization results.

6.3.20 16-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 86* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 86. ADC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog power supply	-		1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V		2	-	V_{DDA}	V
		$V_{DDA} < 2$ V		V_{DDA}			
V_{REF-}	Negative reference voltage	-		V_{SSA}			
f_{ADC}	ADC clock frequency	2 V ≤ V_{DDA} ≤ 3.3 V	BOOST = 1	-	-	36	MHz
			BOOST = 0	-	-	20	
f_S	Sampling rate for Fast channels, BOOST = 1, f_{ADC} = 36 MHz(2)	16-bit resolution		-	-	3.60(2)	MSPS
		14-bit resolution		-	-	4.00(2)	
		12-bit resolution		-	-	4.50(2)	
		10-bit resolution		-	-	5.00(2)	
		8-bit resolution				6.00(2)	
	Sampling rate for Fast channels, BOOST = 0, f_{ADC} = 20 MHz	16-bit resolution		-	-	2.00(2)	
		14-bit resolution		-	-	2.20(2)	
		12-bit resolution		-	-	2.50(2)	
		10-bit resolution		-	-	2.80(2)	
		8-bit resolution				3.30(2)	
	Sampling rate for Slow channels, BOOST = 0, f_{ADC} = 10 MHz	16-bit resolution		-	-	1.00	
		14-bit resolution		-	-	1.00	
		12-bit resolution		-	-	1.00	
		10-bit resolution		-	-	1.00	
		8-bit resolution				1.00	

Table 86. ADC characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG}	External trigger frequency	f_{ADC} = 36 MHz	-	-	3.6	MHz
		16-bit resolution	-	-	10	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-	$V_{REF}/2-10\%$	$V_{REF}/2$	$V_{REF}/2+10\%$	
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	4	-	pF
t_{ADCREG_STUP}	ADC LDO startup time	-	-	5	10	µs
t_{STAB}	ADC power-up time	LDO already started	1			conversion cycle
t_{CAL}	Offset and linearity calibration time	-	165,010			$1/f_{ADC}$
t_{OFF_CAL}	Offset calibration time	-	1,280			
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	1.5	2	2.5	
		CKMODE = 01	-	-	2	
		CKMODE = 10			2.25	
		CKMODE = 11			2.125	
$t_{LATRINJ}$	Trigger conversion latency for regular and injected channels when a regular conversion is aborted	CKMODE = 00	2.5	3	3.5	
		CKMODE = 01	-	-	3	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_S	Sampling time	-	1.5	-	810.5	
t_{CONV}	Total conversion time (including sampling time)	N-bit resolution	t_S + 0.5 + N/2 (9 to 648 cycles in 14-bit mode)			

1. Guaranteed by design.
2. These values are obtained using the following formula: $f_S = f_{ADC}/ t_{CONV}$, where f_{ADC} = 36 MHz and t_{CONV} = 1,5 cycle sampling time + t_{SAR} sampling time. Refer to the product reference manual for the value of t_{SAR} depending on resolution.
3. Depending on the package, V_{REF+} can be internally connected to V_{DDA} and V_{REF-} to V_{SSA}.

Table 87. ADC accuracy(1)(2)(3)

Symbol	Parameter	Conditions(4)		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	BOOST = 1	-	±6	-	±LSB
			BOOST = 0	-	±8	-	
		Differential	BOOST = 1	-	±10	-	
			BOOST = 0	-	±16	-	
ED	Differential linearity error	Single ended	BOOST = 1	-	2	-	
			BOOST = 0	-	1	-	
		Differential	BOOST = 1	-	8	-	
			BOOST = 0	-	2	-	
EL	Integral linearity error	Single ended	BOOST = 1	-	±6	-	
			BOOST = 0	-	±4	-	
		Differential	BOOST = 1	-	±6	-	
			BOOST = 0	-	±4	-	
ENOB(5)	Effective number of bits (2 MSPS)	Single ended	BOOST = 1	-	11.6	-	bits
			BOOST = 0	-	12	-	
		Differential	BOOST = 1	-	13.3	-	
			BOOST = 0	-	13.5	-	
SINAD(5)	Signal-to-noise and distortion ratio (2 MSPS)	Single ended	BOOST = 1	-	71.6	-	dB
			BOOST = 0	-	74	-	
		Differential	BOOST = 1	-	81.83	-	
			BOOST = 0	-	83	-	
SNR(5)	Signal-to-noise ratio (2 MSPS)	Single ended	BOOST = 1	-	72	-	
			BOOST = 0	-	74	-	
		Differential	BOOST = 1	-	82	-	
			BOOST = 0	-	83	-	
THD(5)	Total harmonic distortion	Single ended	BOOST = 1	-	−78	-	
			BOOST = 0	-	−80	-	
		Differential	BOOST = 1	-	−90	-	
			BOOST = 0	-	−95	-	

1. Guaranteed by characterization for BGA packages, the values for LQFP packages might differ.
2. ADC DC accuracy values are measured after internal calibration.
3. The above table gives the ADC performance in 16-bit mode.
4. ADC clock frequency ≤ 36 MHz, 2 V ≤ V_{DDA} ≤3.3 V, 1.6 V ≤ V_{REF} ≤ V_{DDA}, BOOSTEN (for I/O) = 1.
5. ENOB, SINAD, SNR and THD are specified for V_{DDA} = V_{REF} = 3.3 V.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion

being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.

Figure 39. ADC accuracy characteristics

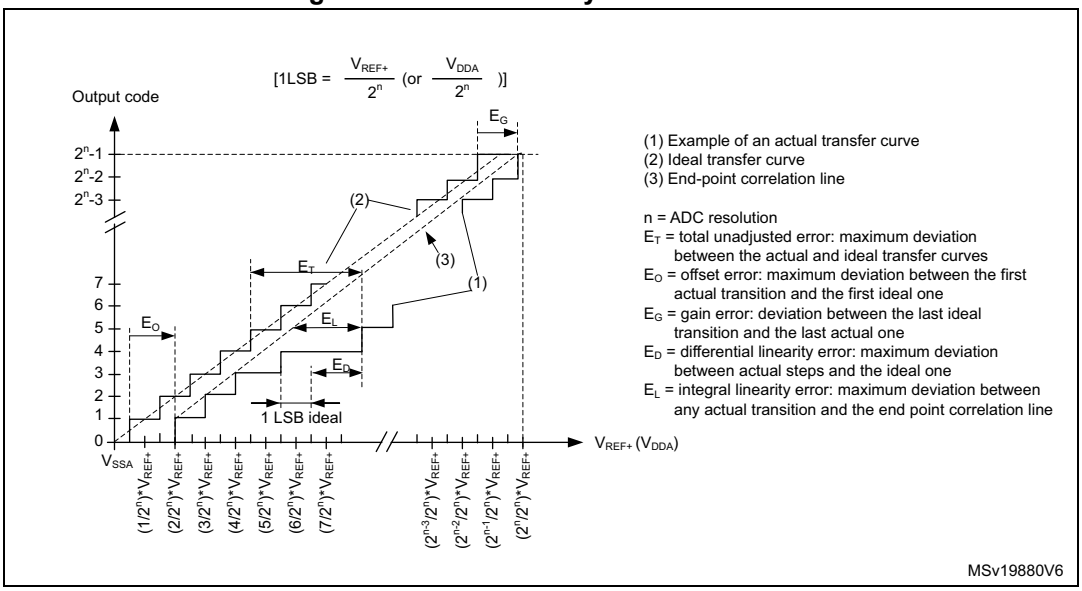
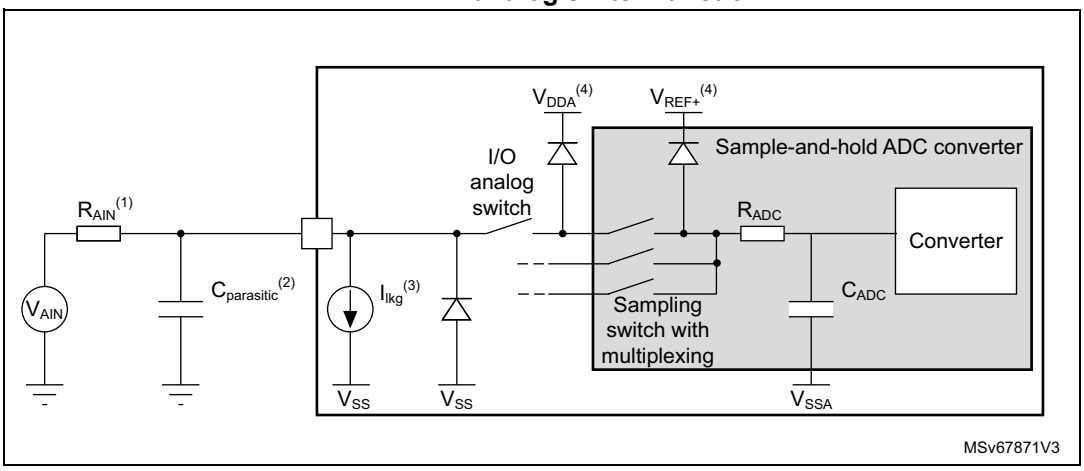


Figure 40. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function

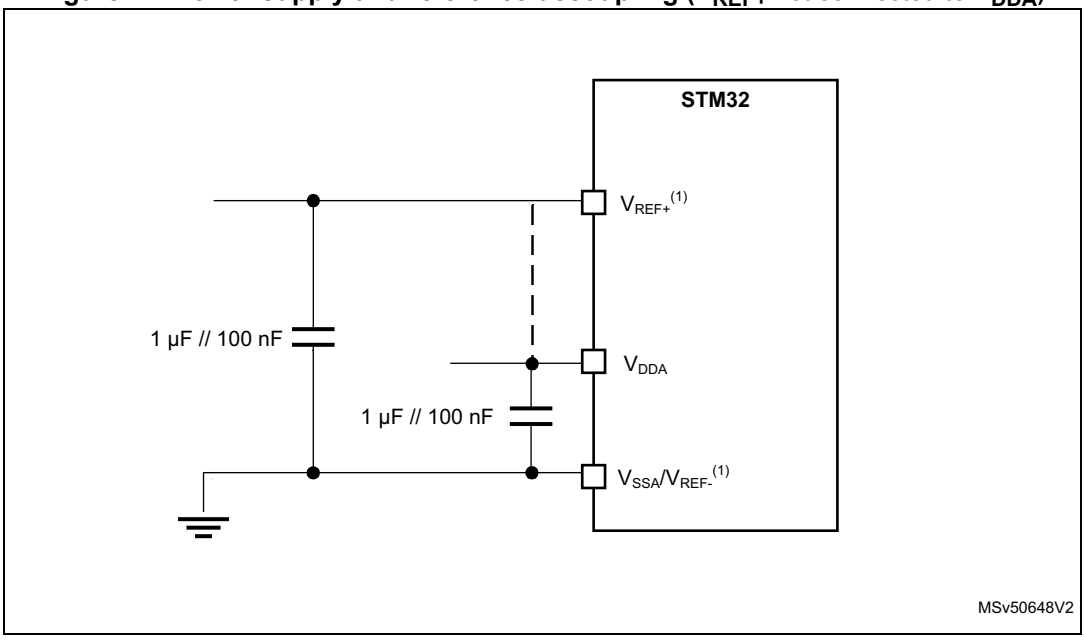


1. Refer to *Section 6.3.20: 16-bit ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 59: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 59: I/O static characteristics* for the value of I_{lkg}.
4. Refer to *Figure 14: Power supply scheme*.

General PCB design guidelines

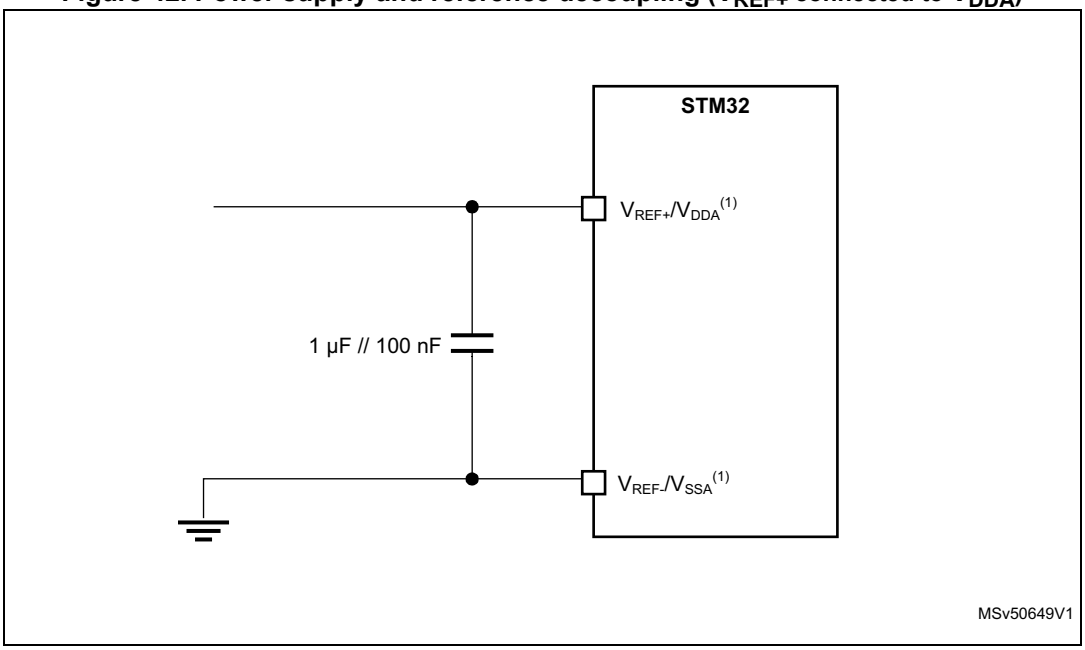
Power supply decoupling should be performed as shown in *Figure 41* or *Figure 42*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 41. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is available on all package whereas the V_{REF-} s available only on UFBGA176+25 and TFBGA240+25. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

Figure 42. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is available on all package whereas the V_{REF-} s available only on UFBGA176+25 and TFBGA240+25. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

6.3.21 DAC electrical characteristics

Table 88. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	3.3	3.6	V
V_{REF+}	Positive reference voltage	-		1.80	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	
R_L	Resistive Load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O(2)	Output Impedance	DAC output buffer OFF		10.3	13	16	
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	kΩ
			V_{DD} = 2.0 V	-	-	2.6	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	kΩ
			V_{DD} = 2.0 V	-	-	18.7	
C_L(2)	Capacitive Load	DAC output buffer OFF		-	-	50	pF
C_{SH}(2)		Sample and Hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} −0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode, DAC output buffer OFF, ±1LSB C_L=10 pF		-	1.7(2)	2(2)	µs
t_{WAKEUP}(3)	Wakeup time from off state (setting the Enx bit in the DAC Control register) until the ±1LSB final value	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, R_L = 5 kΩ		-	5	7.5	µs
V_{offset}(2)	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	850	-	µV
		V_{REF+} = 1.8 V		-	425	-	

Table 88. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDA(DAC)}$	DAC quiescent consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	360	-	µA
			No load, worst code (0xF1C)	-	490	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	20	-	
		Sample and Hold mode, C_{SH}=100 nF		-	$360*T_{ON}/(T_{ON}+T_{OFF})$	-	
$I_{DDV}(DAC)$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	170	-	
			No load, worst code (0xF1C)	-	170	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	160	-	
		Sample and Hold mode, Buffer ON, C_{SH}=100 nF (worst code)		-	$170*T_{ON}/(T_{ON}+T_{OFF})$	-	
		Sample and Hold mode, Buffer OFF, C_{SH}=100 nF (worst code)		-	$160*T_{ON}/(T_{ON}+T_{OFF})$	-	

1. Guaranteed by characterization results.
2. Guaranteed by design.
3. In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).

Table 89. DAC accuracy(1)

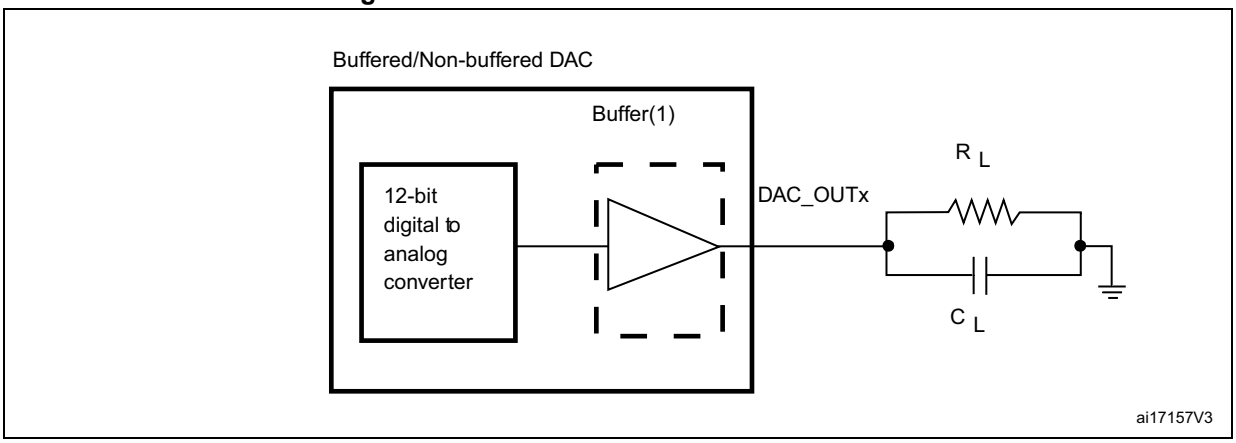
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity(2)	DAC output buffer ON		-	±2	-	LSB
		DAC output buffer OFF		-	±2	-	
INL	Integral non linearity(3)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	±4	-	LSB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	±4	-	
Offset	Offset error at code 0x800 (3)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	V_{REF+} = 3.6 V	-	-	±12	LSB
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±8	

Table 89. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±5	LSB
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	$V_{REF+} = 3.6$ V	-	-	±5	LSB
			$V_{REF+} = 1.8$ V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ		-	-	±1	%
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±1	
TUE	Total unadjusted error	DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±12	LSB
SNR	Signal-to-noise ratio(6)	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz, BW = 500 KHz		-	67.8	-	dB
SINAD	Signal-to-noise and distortion ratio(6)	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz		-	67.5	-	dB
ENOB	Effective number of bits	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz		-	10.9	-	bits

1. Guaranteed by characterization.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2 V) when the buffer is ON.
6. Signal is -0.5dBFS with $F_{sampling}$=1 MHz.

Figure 43. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.22 Voltage reference buffer characteristics

Table 90. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	VSCALE = 000	2.8	3.3	3.6	V
			VSCALE = 001	2.4	-	3.6	
			VSCALE = 010	2.1	-	3.6	
			VSCALE = 011	1.8	-	3.6	
		Degraded mode	VSCALE = 000	1.62	-	2.80	
			VSCALE = 001	1.62	-	2.40	
			VSCALE = 010	1.62	-	2.10	
			VSCALE = 011	1.62	-	1.80	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode	VSCALE = 000	-	2.5	-	
			VSCALE = 001	-	2.048	-	
			VSCALE = 010	-	1.8	-	
			VSCALE = 011	-	1.5	-	
		Degraded mode(2)	VSCALE = 000	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 001	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 010	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 011	V_{DDA}– 150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.2	%
C_L	Load capacitor	-	-	0.5	1	1.50	uF

Table 90. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
esr	Equivalent Serial Resistor of C_L	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal Mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	−40 °C < T_J < +125 °C	-	-	-	T_{coeff} xV_{REFINT} + 75	ppm/ °C
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100KHz	-	-	40	-	
t_{START}	Start-up time	C_L=0.5 µF	-	-	300	-	µs
		C_L=1 µF	-	-	500	-	
		C_L=1.5 µF	-	-	650	-	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(3)	-		-	8	-	mA
$I_{DDA(VREFBUF)}$	VREFBUF consumption from V_{DDA}	I_{LOAD} = 0 µA	-	-	15	25	µA
		I_{LOAD} = 500 µA	-	-	16	30	
		I_{LOAD} = 4 mA	-	-	32	50	

1. Guaranteed by design.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}−drop voltage).
3. To properly control VREFBUF I_{INRUSH} current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 1.8 V-3.6 V, 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VSCALE = 011, 010, 001 and 000, respectively.

6.3.23 Temperature sensor characteristics

Table 91. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	-	±3	°C
Avg_Slope(2)	Average slope	-	2	-	mV/°C
V_{30}(3)	Voltage at 30°C ± 5 °C	-	0.62	-	V
t_{start_run}(1)	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

1. Guaranteed by design.

2. Guaranteed by characterization.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

Table 92. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA}=3.3 V	0x1FF1 E820 -0x1FF1 E821
TS_CAL2	Temperature sensor raw data acquired value at 110 °C, V_{DDA}=3.3 V	0x1FF1 E840 - 0x1FF1 E841

6.3.24 Temperature and V_{BAT} monitoring

Table 93. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	26	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9	-	-	µs
$V_{BAThigh}$	High supply monitoring	-	3.55	-	V
V_{BATlow}	Low supply monitoring	-	1.36	-	

1. Guaranteed by design.

Table 94. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	KΩ
		VBRS in PWR_CR3= 1		1.5	-	

Table 95. Temperature monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	-	117	-	°C
$TEMP_{low}$	Low temperature monitoring	-	–25	-	

6.3.25 Voltage booster for analog switch

Table 96. Voltage booster for analog switch characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.62	2-6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.62 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

1. Guaranteed by characterization results.

6.3.26 Comparator characteristics

Table 97. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	3.3	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		Refer to V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	0.2	0.3	µA
		BRG_EN=1 (bridge enable)		-	0.8	1	
t_{START_SCALER}	Scaler startup time	-		-	140	250	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode		-	2	5	µs
		Medium mode		-	5	20	
		Ultra-low-power mode		-	15	80	
t_D	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode		-	50	80	ns
		Medium mode		-	0.5	1.2	µs
		Ultra-low-power mode		-	2.5	7	
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	High-speed mode		-	50	120	ns
		Medium mode		-	0.5	1.2	µs
		Ultra-low-power mode		-	2.5	7	
V_{offset}	Comparator offset error	Full common mode range		-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	10	-	
		Medium hysteresis		-	20	-	
		High hysteresis		-	30	-	
$I_{DDA(COMP)}$	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	800	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 27: Embedded reference voltage*.

6.3.27 Operational amplifier characteristics

Table 98. OPAMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage Range	-	2	3.3	3.6	V
CMIR	Common Mode Input Range	-	0	-	V_{DDA}	
VI_{OFFSET}	Input offset voltage	25°C, no load on output	-	-	±1.5	mV
		All voltages and temperature, no load	-	-	±2.5	
ΔVI_{OFFSET}	Input offset voltage drift	-	-	±3.0	-	µV/°C
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1*V_{DDA})	-	-	1.1	1.5	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9*V_{DDA})	-	-	1.1	1.5	
I_{LOAD}	Drive current	-	-	-	500	µA
I_{LOAD_PGA}	Drive current in PGA mode	-	-	-	270	
C_{LOAD}	Capacitive load	-	-	-	50	pF
CMRR	Common mode rejection ratio	-	-	80	-	dB
PSRR	Power supply rejection ratio	C_{LOAD} ≤ 50pf / R_{LOAD} ≥ 4 kΩ(2) at 1 kHz, V_{com}=V_{DDA}/2	50	66	-	dB
GBW	Gain bandwidth for high supply range	-	4	7.3	12.3	MHz
SR	Slew rate (from 10% and 90% of output voltage)	Normal mode	-	3	-	V/µs
		High-speed mode	-	30	-	
AO	Open loop gain	-	59	90	129	dB
φm	Phase margin	-	-	55	-	°
GM	Gain margin	-	-	12	-	dB

Table 98. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OHSAT}	High saturation voltage	I_{load}=max or R_{LOAD}=min(2), Input at V_{DDA}		V_{DDA} −100 mV	-	-	mV
V_{OLSAT}	Low saturation voltage	I_{load}=max or R_{LOAD}=min(2), Input at 0 V		-	-	100	
t_{WAKEUP}	Wake up time from OFF state	Normal mode	C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ(2), follower configuration	-	0.8	3.2	µs
		High speed	C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ(2), follower configuration	-	0.9	2.8	
PGA gain	Non inverting gain value	-		-	2	-	-
		-		-	4	-	-
		-		-	8	-	-
		-		-	16	-	-
	Inverting gain value	-		-	−1	-	-
		-		-	−3	-	-
		-		-	−7	-	-
		-		-	−15	-	-
$R_{network}$	R2/R1 internal resistance values in non-inverting PGA mode(3)	PGA Gain=2		-	10/10	-	kΩ/ kΩ
		PGA Gain=4		-	30/10	-	
		PGA Gain=8		-	70/10	-	
		PGA Gain=16		-	150/10	-	
	R2/R1 internal resistance values in inverting PGA mode(3)	PGA Gain=-1		-	10/10	-	
		PGA Gain=-3		-	30/10	-	
		PGA Gain=-7		-	70/10	-	
		PGA Gain=-15		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		−15	-	15	%
PGA BW	PGA bandwidth for different non inverting gain	Gain=2		-	GBW/2	-	MHz
		Gain=4		-	GBW/4	-	
		Gain=8		-	GBW/8	-	
		Gain=16		-	GBW/16	-	

Table 98. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
en	Voltage noise density	at 1 KHz	output loaded with 4 kΩ	-	140	-	nV/√Hz
		at 10 KHz		-	55	-	
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode, follower	-	570	1000	µA
		High-speed mode		-	610	1200	

1. Guaranteed by design, unless otherwise specified.
2. R_{LOAD} is the resistive load connected to VSSA or to VDDA.
3. R2 is the internal resistance between the OPAMP output and th OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.

6.3.28 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 99* for DFSDM are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDMx_CKINx, DFSDMx_DATINx, DFSDMx_CKOUT for DFSDMx).

Table 99. DFSDM measured timing - 1.62-3.6 V(1)

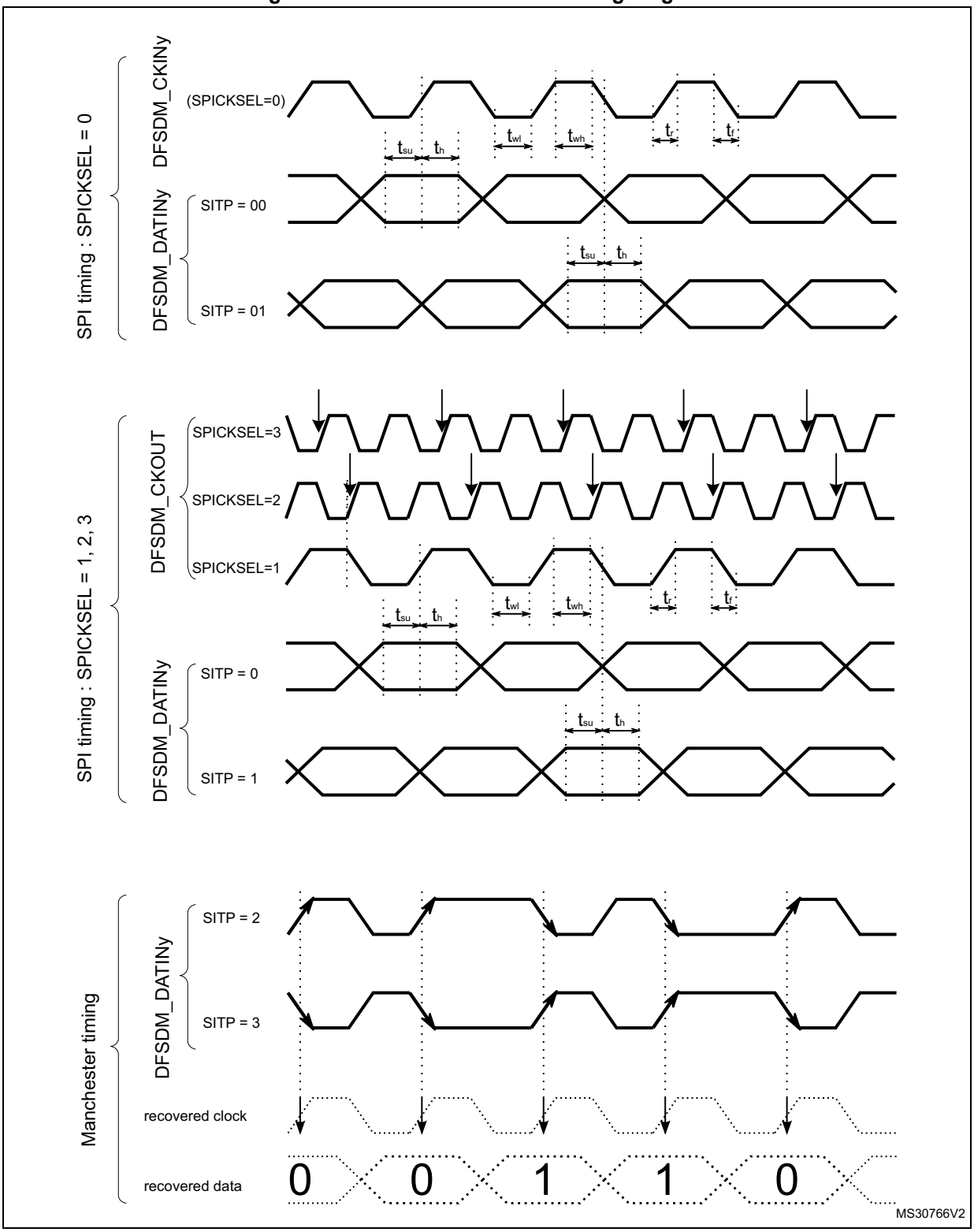
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.62 V < V_{DD} < 3.6 V		-	-	250	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 V < V_{DD} < 3.6 V		-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < V_{DD} < 3.6 V		-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 1.62 < V_{DD} < 3.6 V		-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 2.7 < V_{DD} < 3.6 V		-	-	20 ($f_{DFSDMCLK}$/4)	
f_{CKOUT}	Output clock frequency	1.62 < V_{DD} < 3.6 V		-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.62 < V_{DD} < 3.6 V	Even division, CKOUTDIV[7:0] = 1, 3, 5...	45	50	55	%
			Odd division, CKOUTDIV[7:0] = 2, 4, 6...	(((n/2+1)/(n+1))* 100)–5	(((n/2+1)/(n+1)) *100)	(((n/2+1)/(n+1))* 100)+5	

Table 99. DFSDM measured timing - 1.62-3.6 V(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V	$T_{CKIN}/2$ - 0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V	4	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V	0.5	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), 1.62 < V_{DD} < 3.6 V	(CKOUTDIV+1) * $T_{DFSDMCLK}$	-	(2*CKOUTDIV) * $T_{DFSDMCLK}$	

1. Guaranteed by characterization results.

Figure 44. Channel transceiver timing diagrams



6.3.29 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 100* for DCMI are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage summarized in *Table 23: General operating conditions*, with the following configuration:

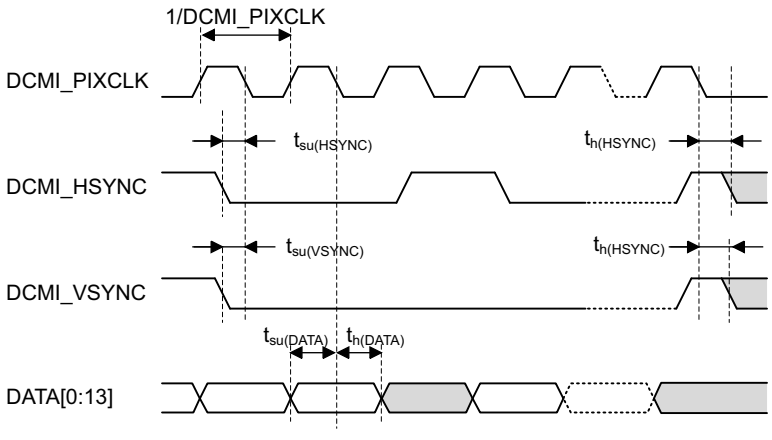
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Table 100. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/$f_{rcc_c_ck}$	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	80	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	1	-	ns
$t_{h(DATA)}$	Data input hold time	1	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	1.5	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	1	-	

1. Guaranteed by characterization results.

Figure 45. DCMI timing diagram



6.3.30 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 101* for LCD-TFT are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage summarized in *Table 23: General operating conditions*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled

Table 101. LTDC characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CLK}	LTDC clock output frequency	2.7 V < V_{DD} < 3.6 V, 20 pF	-	150	MHz
		2.7 V < V_{DD} < 3.6 V	-	133	
		1.62 V < V_{DD} < 3.6 V	-	90	
D_{CLK}	LTDC clock output duty cycle	-	45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time		$t_{w(CLK)}/2-0.5$	$t_{w(CLK)}/2+0.5$	ns
$t_{v(DATA)}$	Data output valid time		-	0.5	
$t_{h(DATA)}$	Data output hold time		0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time		-	0.5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time		0.5	-	

1. Guaranteed by characterization results.

Figure 46. LCD-TFT horizontal timing diagram

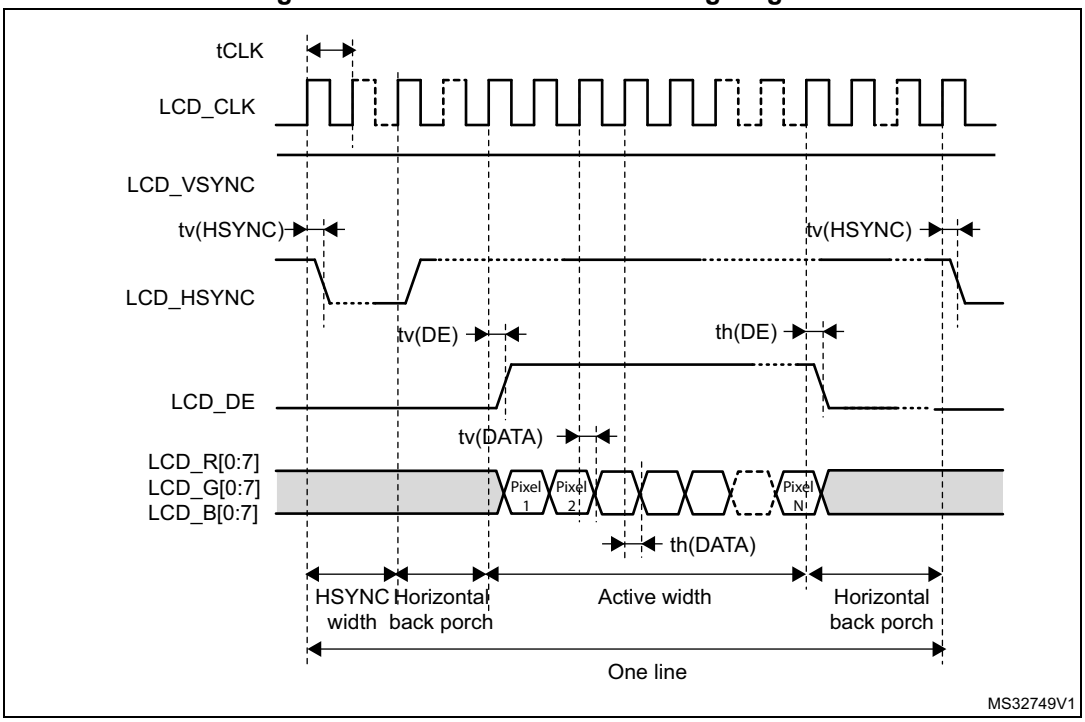
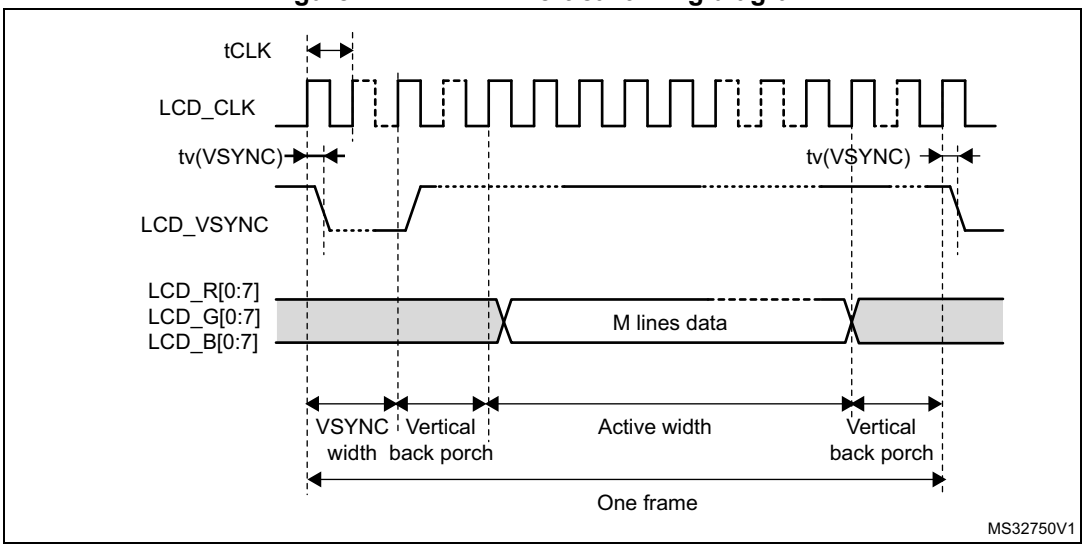


Figure 47. LCD-TFT vertical timing diagram



6.3.31 Timer characteristics

The parameters given in *Table 102* are guaranteed by design.

Refer to *Section 6.3.15: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 102. TIMx characteristics(1)(2)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 240 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 140 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 240 MHz	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 240 MHz, by setting the TIMPRE bit in the RCC_CFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = rcc_hclk1, otherwise TIMxCLK = 4x $F_{rcc_pclkx_d2}$.

6.3.32 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0433 reference manual) and when the i2c_ker_ck frequency is greater than the minimum shown in the table below:

Table 103. Minimum i2c_ker_ck frequency in all I²C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode		2	MHz
		Fast-mode	Analog filter ON DNF=0	8	
			Analog filter OFF DNF=1	9	
		Fast-mode Plus	Analog filter ON DNF=0	17	
			Analog filter OFF DNF=1	16	

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but still present.
- The 20 mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{load} supported in Fm+, which is given by these formulas:

  $t_{r(SDA/SCL)}=0.8473xR_pxC_{load}$

  $R_{p(min)}= (V_{DD}-V_{OL(max)})/I_{OL(max)}$

  Where R_p is the I2C lines pull-up. Refer to *Section 6.3.15: I/O port characteristics* for the I2C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to *Table 104* for the analog filter characteristics:

Table 104. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 105* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled
- HSLV activated when VDD ≤ 2.7 V

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 105. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 1.62 V≤V_{DD}≤3.6 V	-	-	90	MHz
		Master mode 2.7 V≤V_{DD}≤3.6 V SPI1,2,3			133	
		Master mode 2.7 V≤V_{DD}≤3.6 V SPI4,5,6			100	
		Slave receiver mode 1.62 V≤V_{DD}≤3.6 V SPI1,2,3			150	
		Slave receiver mode 1.62 V≤V_{DD}≤3.6 V SPI4,5,6			100	
		Slave mode transmitter/full duplex 2.7 V≤V_{DD}≤3.6 V			31	
		Slave mode transmitter/full duplex 1.62 V≤V_{DD}≤3.6 V			25	
$t_{su(NSS)}$	NSS setup time	Slave mode	2	-	-	ns
$t_{h(NSS)}$	NSS hold time		1	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PLCK} - 2	T_{PLCK}	T_{PLCK} + 2	

Table 105. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(MI)}$	Data input setup time	Master mode	2	-	-	ns
$t_{su(SI)}$		Slave mode	2	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	1	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	13	27	
$t_{dis(SO)}$	Data output disable time	Slave mode	0	1	5	
$t_{v(SO)}$	Data output valid time	Slave mode, 2.7 V≤V_{DD}≤3.6 V	-	11.5	16	
		Slave mode 1.62 V≤V_{DD}≤3.6 V	-	13	20	
$t_{v(MO)}$		Master mode	-	1	3	
$t_{h(SO)}$	Data output hold time	Slave mode, 1.62 V≤V_{DD}≤3.6 V	9	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.

Figure 48. SPI timing diagram - slave mode and CPHA = 0

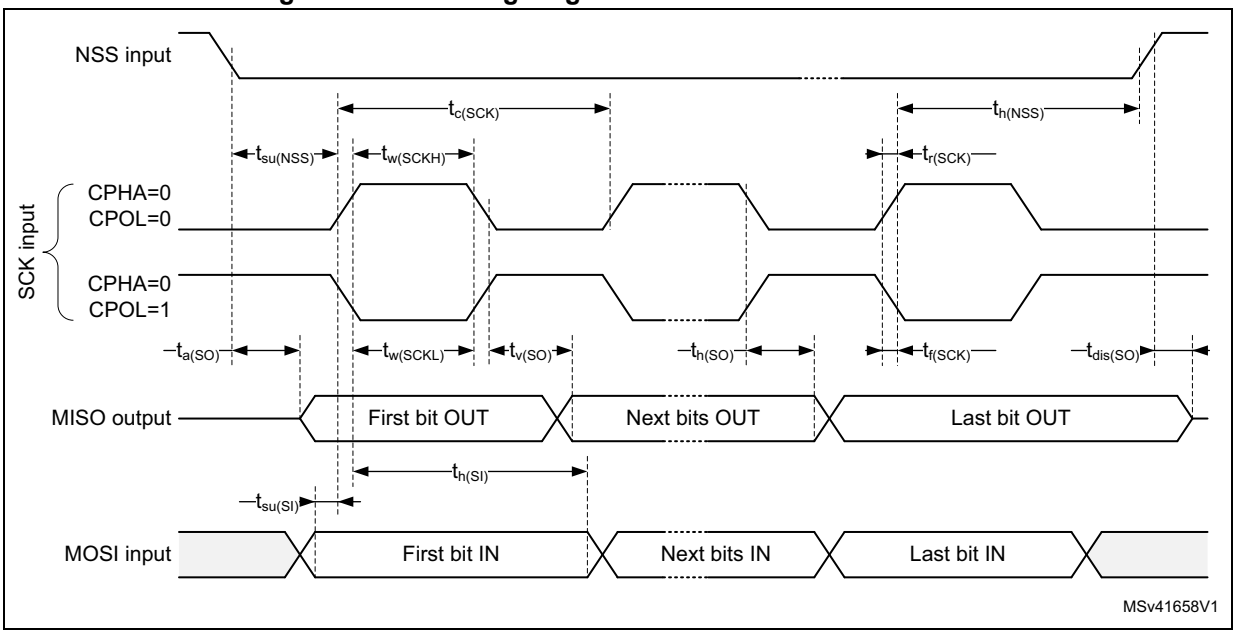
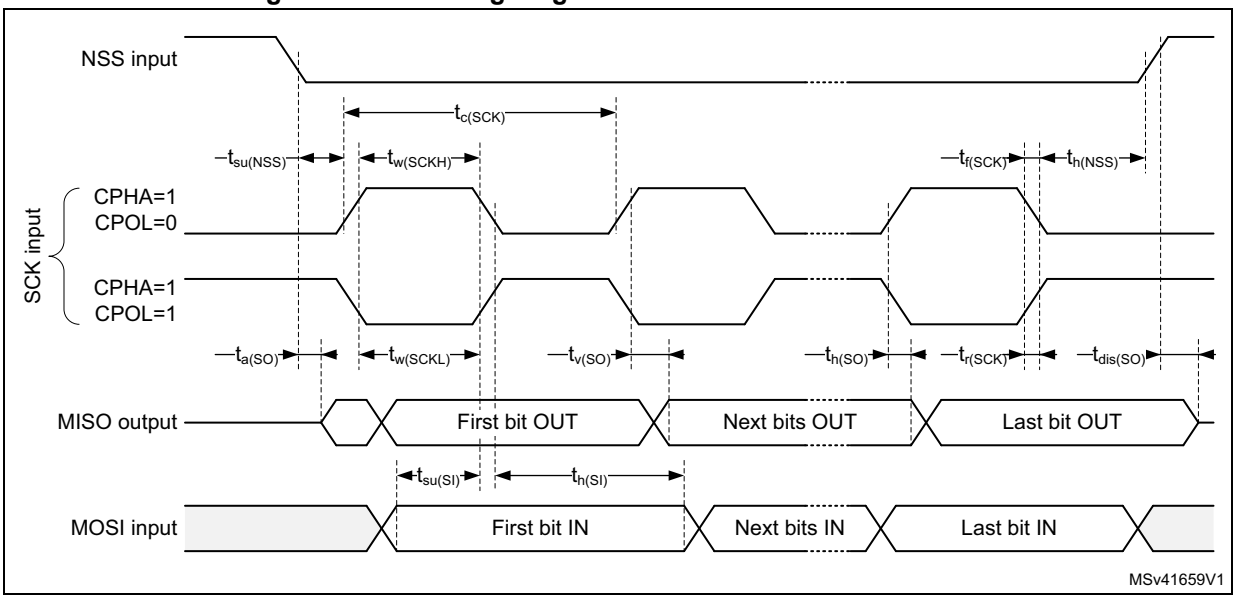
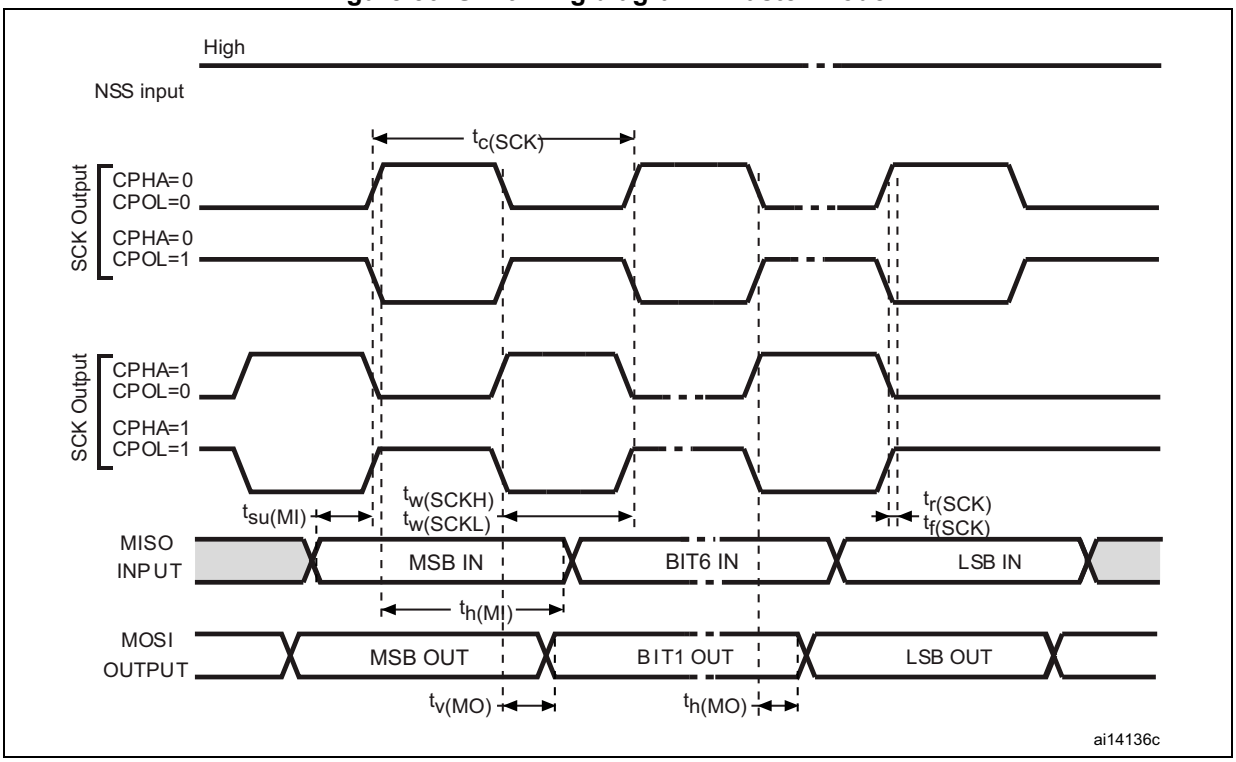


Figure 49. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 50. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 106* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled

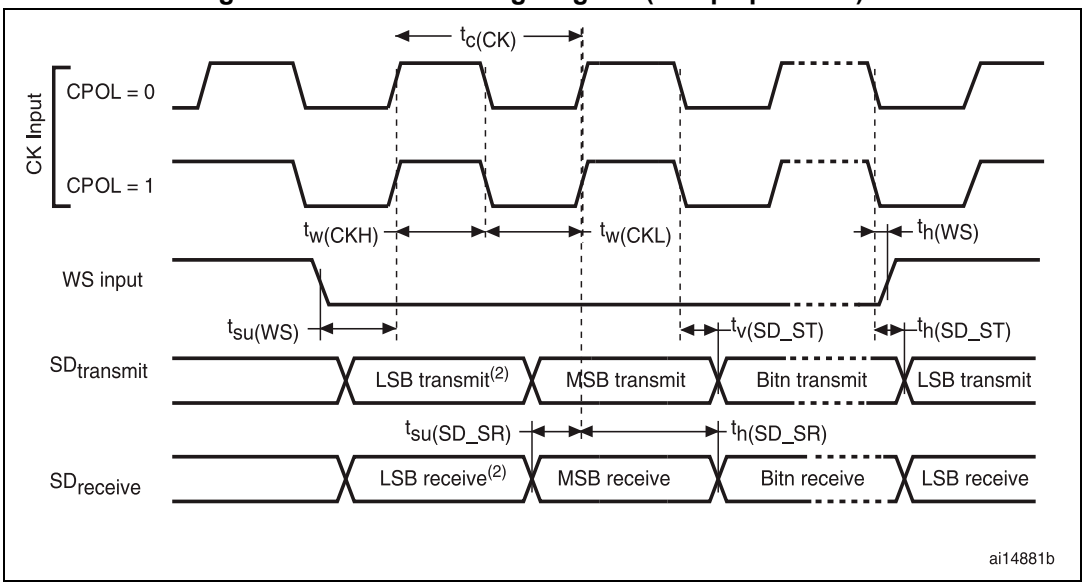
Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 106. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	$256F_S$	MHz
f_{CK}	I2S clock frequency	Master data	-	$64F_S$	MHz
		Slave data	-	$64F_S$	
$t_{v(WS)}$	WS valid time	Master mode	-	3.5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	1	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD_SR)}$		Slave receiver	1	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	4	-	
$t_{h(SD_SR)}$		Slave receiver	2	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	

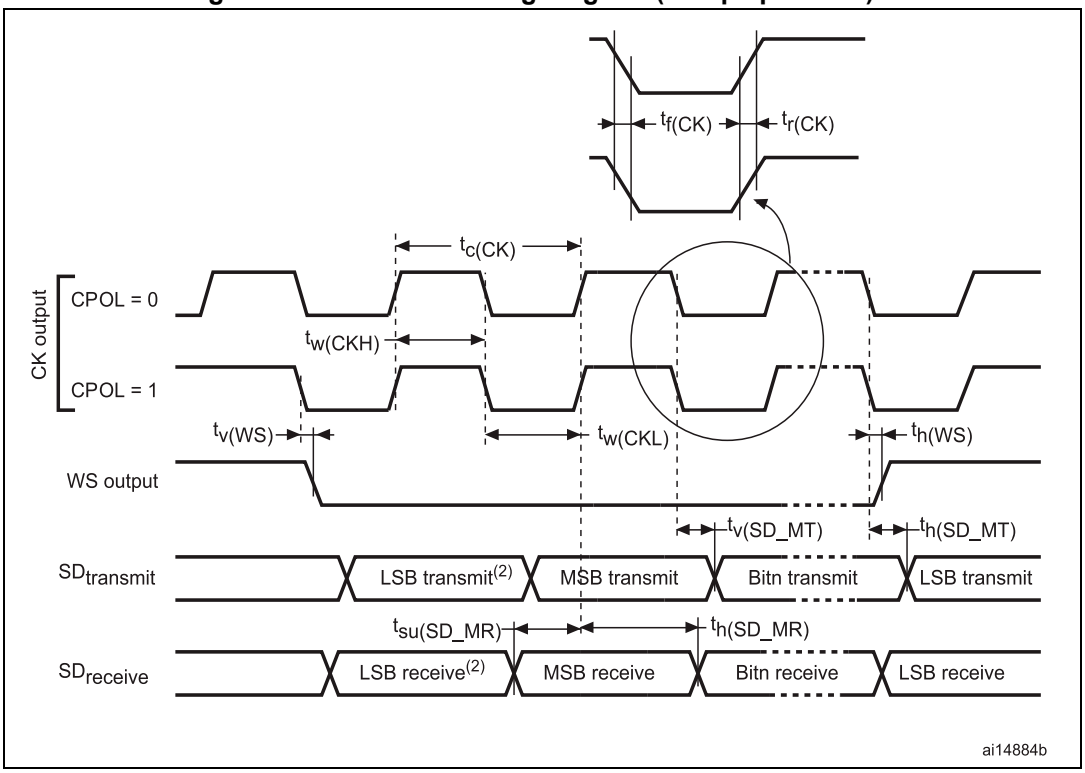
1. Guaranteed by characterization results.

Figure 51. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 52. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 107* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 107. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	256 x 8K	256xFs	MHz
F_{CK}	SAI clock frequency(2)	Master data: 32 bits	-	128xFs(3)	MHz
		Slave data: 32 bits	-	128xFs	
$t_{v(FS)}$	FS valid time	Master mode 2.7≤VDD≤3.6V	-	15	ns
		Master mode 1.71≤VDD≤3.6V	-	20	
$t_{su(FS)}$	FS setup time	Slave mode	7	-	
$t_{h(FS)}$	FS hold time	Master mode	1	-	
		Slave mode	1	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	0.5	-	
$t_{su(SD_B_SR)}$		Slave receiver	1	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD_B_SR)}$		Slave receiver	2	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7≤V_{DD}≤3.6V	-	17	ns
		Slave transmitter (after enable edge) 1.62≤V_{DD}≤3.6V	-	20	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	7	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7≤V_{DD}≤3.6V	-	17	
		Master transmitter (after enable edge) 1.62≤V_{DD}≤3.6V	-	20	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	7.55	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With F_S=192 kHz.

Figure 53. SAI master timing waveforms

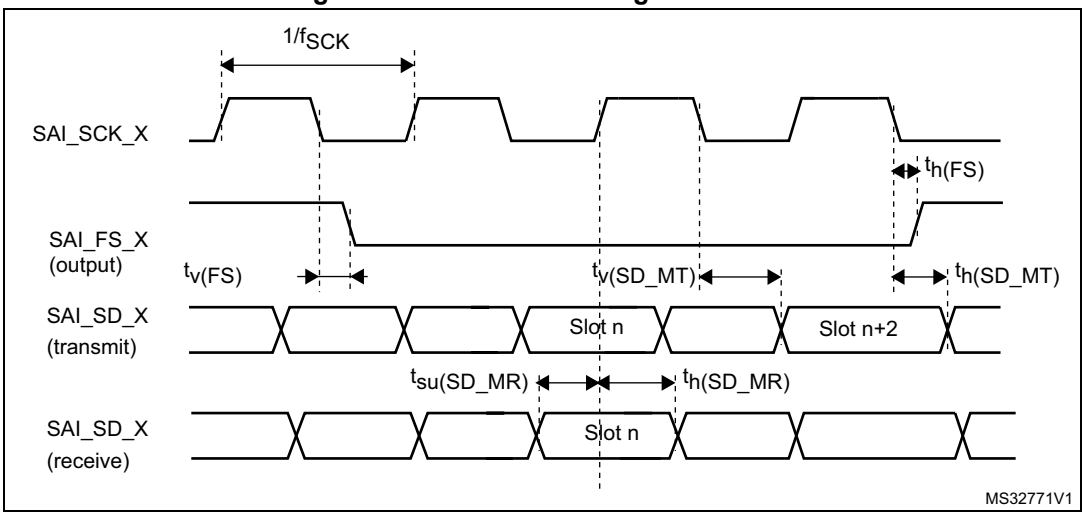
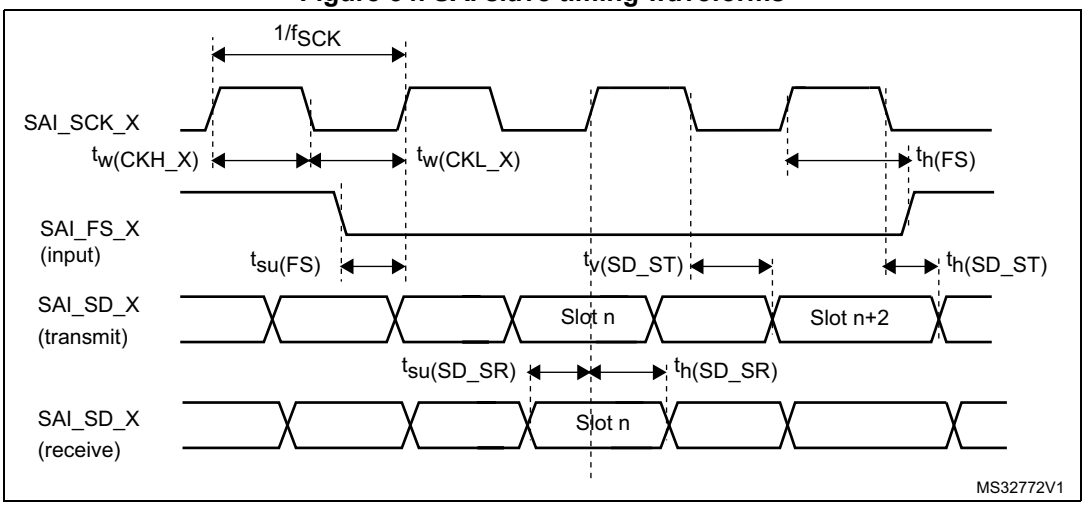


Figure 54. SAI slave timing waveforms



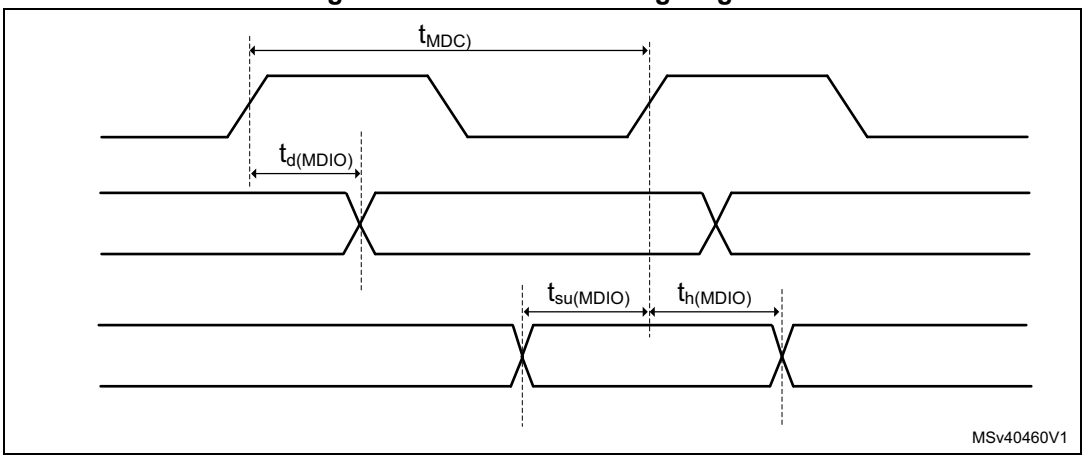
MDIO characteristics

Table 108. MDIO Slave timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
F_{sDC}	Management data clock	-	-	40	MHz
$t_{d(MDIO)}$	Management data input/output **output valid time**	7	8	20	ns
$t_{su(MDIO)}$	Management data input/output **setup time**	4	-	-	
$t_{h(MDIO)}$	Management data input/output **hold time**	1	-	-	

The MDIO controller is mapped on APB2 domain. The frequency of the APB bus should at least 1.5 times the MDC frequency: $F_{PCLK2} \geq 1.5 * F_{MDC}$.

Figure 55. MDIO Slave timing diagram



SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 109* for the SDIO/MMC interface are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled
- HSLV activated when VDD ≤ 2.7 V

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 109. Dynamic characteristics: SD / MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	125	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS/SDR/DDR mode						
t_{ISU}	Input setup time HS	f_{PP} ≥ 50 MHz	3	-	-	ns
t_{IH}	Input hold time HS		0.5	-	-	
t_{IDW}(3)	Input valid window (variable window)		3	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS/SDR/DDR mode						
t_{OV}	Output valid time HS	f_{PP} ≥ 50 MHz	-	3.5	5	ns
t_{OH}	Output hold time HS		2	-	-	

Table 109. Dynamic characteristics: SD / MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} =25 MHz	3	-	-	ns
t_{IHD}	Input hold time SD		0.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} =25 MHz	-	1	2	ns
t_{OHD}	Output hold default time SD		0	-	-	

1. Guaranteed by characterization results.
2. Above 100 MHz, C_L = 20 pF.
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Table 110. Dynamic characteristics: eMMC characteristics, V_{DD} = 1.71 to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	120	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	$f_{PP} \geq$ 50 MHz	2.5	-	-	ns
t_{IH}	Input hold time HS		1	-	-	
t_{IDW}(3)	Input valid window (variable window)		3.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	$f_{PP} \geq$ 50 MHz	-	5	7	ns
t_{OH}	Output hold time HS		3	-	-	

1. Guaranteed by characterization results.
2. C_L = 20 pF.
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Figure 56. SDIO high-speed mode

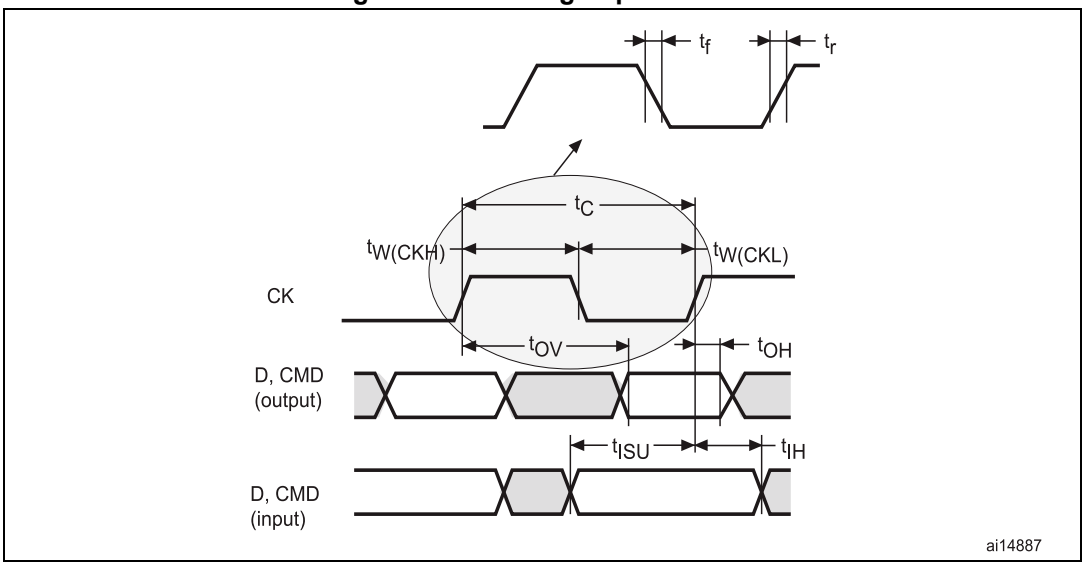


Figure 57. SD default mode

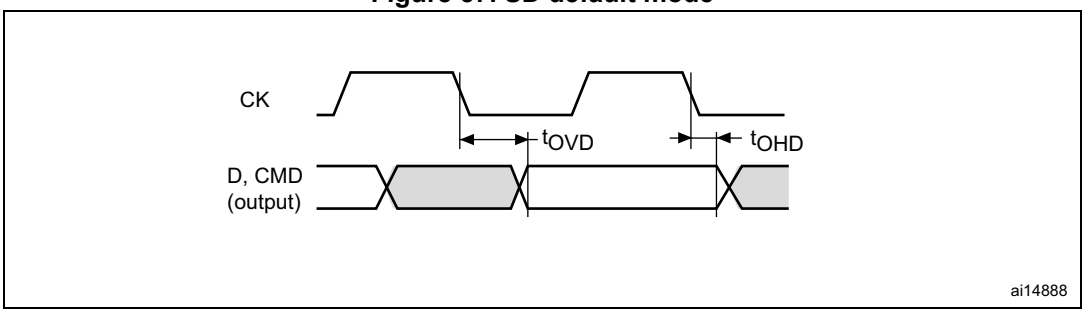
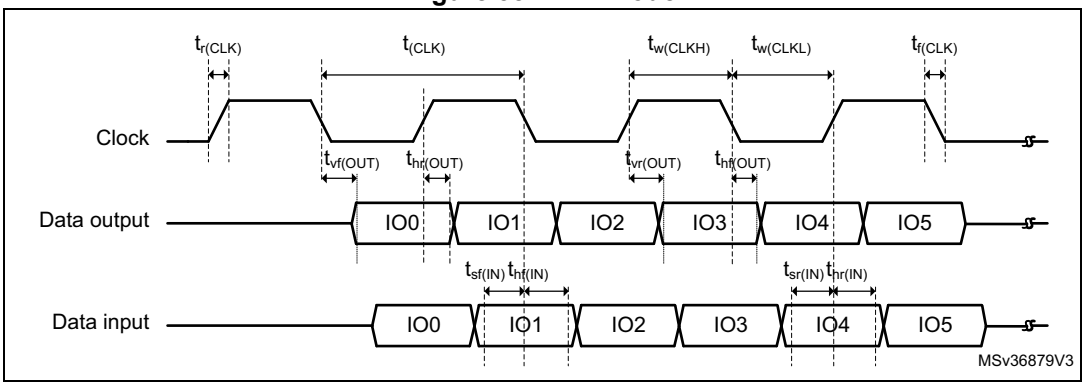


Figure 58. DDR mode



CAN (controller area network) interface

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (FDCANx_TX and FDCANx_RX).

USB OTG_FS characteristics

The USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 111. USB OTG_FS electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DD33USB}$	USB transceiver operating voltage	-	3.0(1)	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}	Output driver impedance(2)	Driver high and low	28	36	44	

1. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V voltage range.
2. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

USB OTG_HS characteristics

Unless otherwise specified, the parameters given in *Table 112* for ULPI are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

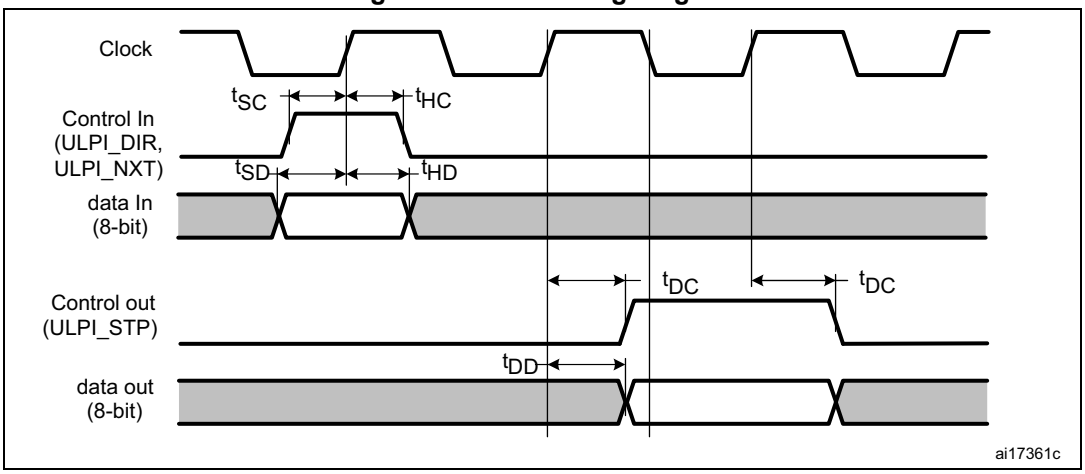
Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 112. Dynamic characteristics: USB ULPI(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	0.5	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	6.5	-	-	
t_{SD}	Data in setup time	-	2.5	-	-	
t_{HD}	Data in hold time	-	0	-	-	
t_{DC}/t_{DD}	Data/control output delay	2.7 V < V_{DD} < 3.6 V, C_L = 20 pF	-	6.5	8.5	
		-	-	6.5	13	
		1.7 V < V_{DD} < 3.6 V, C_L = 15 pF	-			

1. Guaranteed by characterization results.

Figure 59. ULPI timing diagram



Ethernet characteristics

Unless otherwise specified, the parameters given in *Table 113*, *Table 114* and *Table 115* for SMI, RMII and MII are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 113 gives the list of Ethernet MAC signals for the SMI and *Figure 60* shows the corresponding timing diagram.

Table 113. Dynamics characteristics: Ethernet MAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	400	400	403	ns
$T_{d(MDIO)}$	Write data valid time	1	1.5	3	
$t_{su(MDIO)}$	Read data setup time	8	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

Figure 60. Ethernet SMI timing diagram

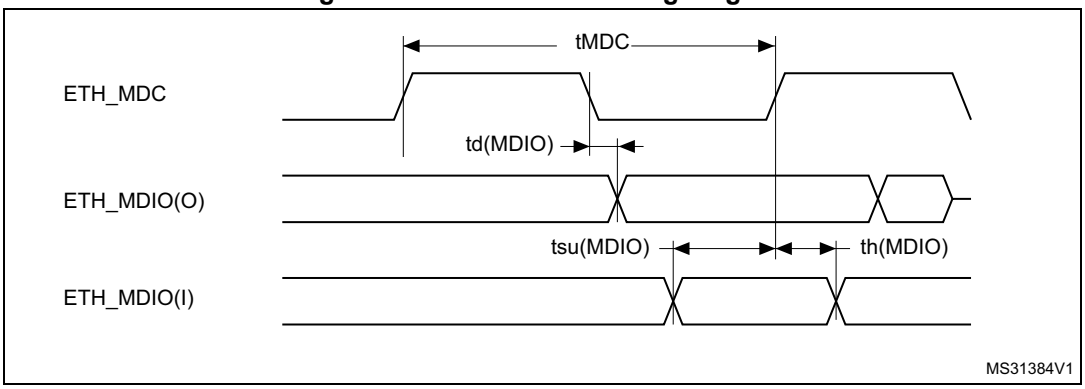


Table 114 gives the list of Ethernet MAC signals for the RMII and *Figure 61* shows the corresponding timing diagram.

Table 114. Dynamics characteristics: Ethernet MAC signals for RMII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	3	-	-	
$t_{su(CRS)}$	Carrier sense setup time	2.5	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	2	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	4	4.5	7	
$t_{d(TXD)}$	Transmit data valid delay time	7	7.5	11.5	

1. Guaranteed by characterization results.

Figure 61. Ethernet RMII timing diagram

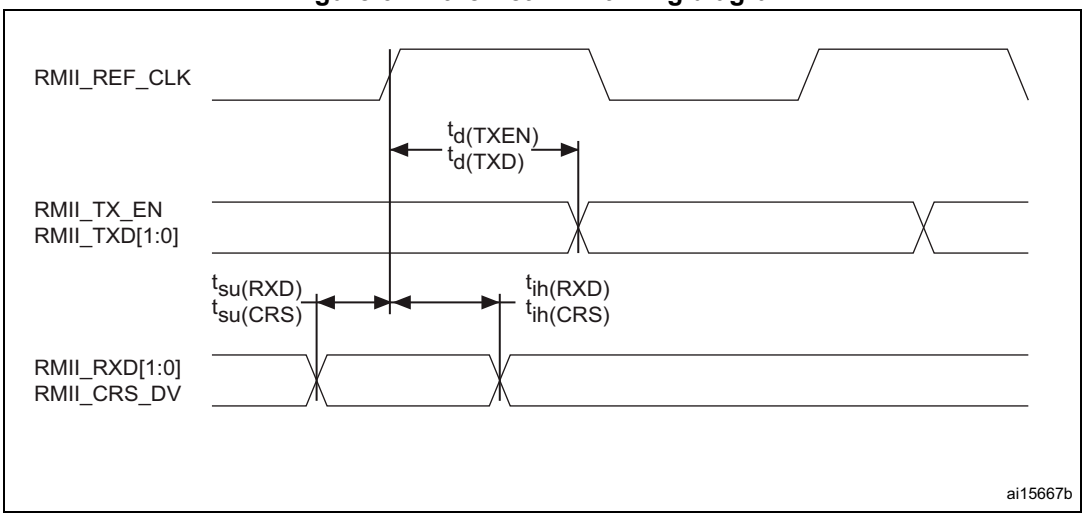


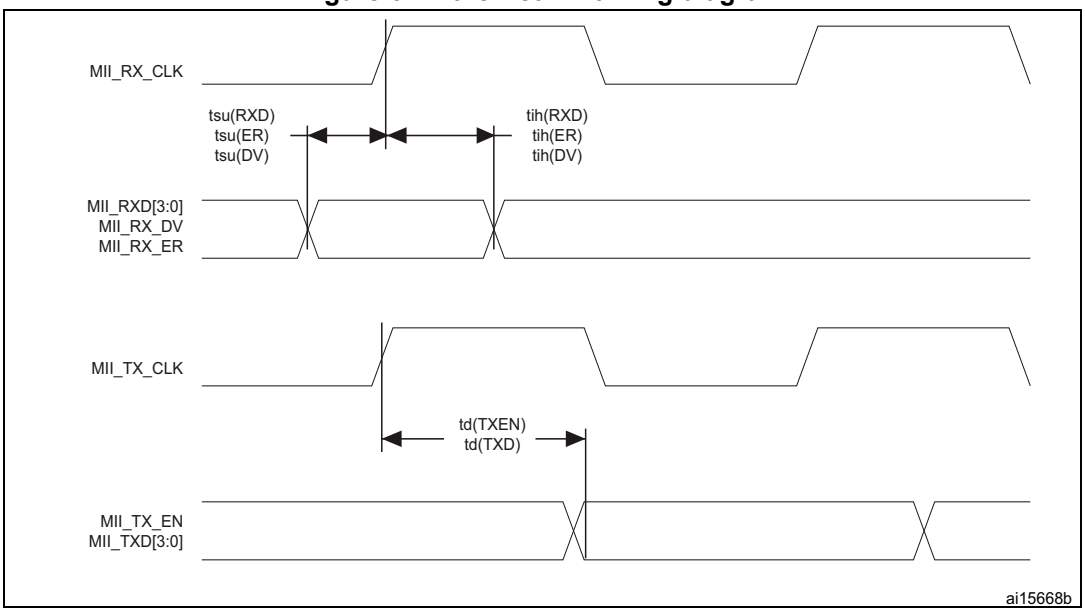
Table 115 gives the list of Ethernet MAC signals for MII and *Figure 62* shows the corresponding timing diagram.

Table 115. Dynamics characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	3	-	-	
$t_{su(DV)}$	Data valid setup time	1.5	-	-	
$t_{ih(DV)}$	Data valid hold time	1	-	-	
$t_{su(ER)}$	Error setup time	1.5	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	4.5	6.5	11	
$t_{d(TXD)}$	Transmit data valid delay time	7	7.5	15	

1. Guaranteed by characterization results.

Figure 62. Ethernet MII timing diagram



6.3.33 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 116* and *Table 117* for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x10
- Capacitive load C=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 116. Dynamics JTAG characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	T_{CK} clock frequency	2.7 V <V_{DD}< 3.6 V	-	-	37	MHz
$1/t_{c(TCK)}$		1.62 V <V_{DD}< 3.6 V	-	-	27.5	
$ti_{su(TMS)}$	TMS input setup time	-	2	-	-	ns
$ti_{h(TMS)}$	TMS input hold time	-	1	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	1.5	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	1	-	-	
$t_{ov\ (TDO)}$	TDO output valid time	2.7 V <V_{DD}< 3.6 V	-	8	13.5	
		1.62 V <V_{DD}< 3.6 V	-	8	18	
$t_{oh(TDO)}$	TDO output hold time	-	7	-	-	

1. Guaranteed by characterization results.

Table 117. Dynamics SWD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	2.7 V <V_{DD}< 3.6 V	-	-	71	MHz
$1/t_{c(SWCLK)}$		1.62 V <V_{DD}< 3.6 V	-	-	55.5	
$t_{isu(SWDIO)}$	SWDIO input setup time	-	2.5	-	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time	-	1	-	-	
$t_{ov\ (SWDIO)}$	SWDIO output valid time	2.7 V <V_{DD}< 3.6 V	-	8.5	14	
		1.62 V <V_{DD}< 3.6 V	-	8.5	18	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8	-	-	

1. Guaranteed by characterization results.

Figure 63. JTAG timing diagram

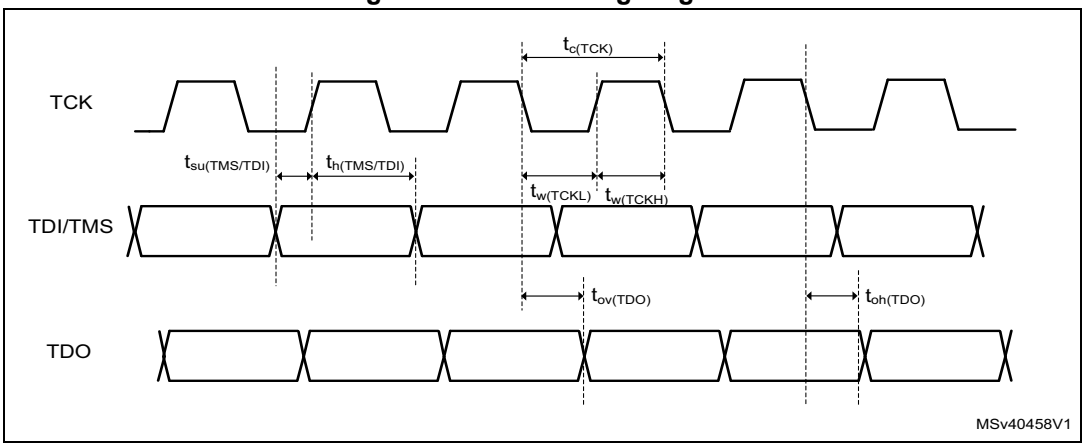
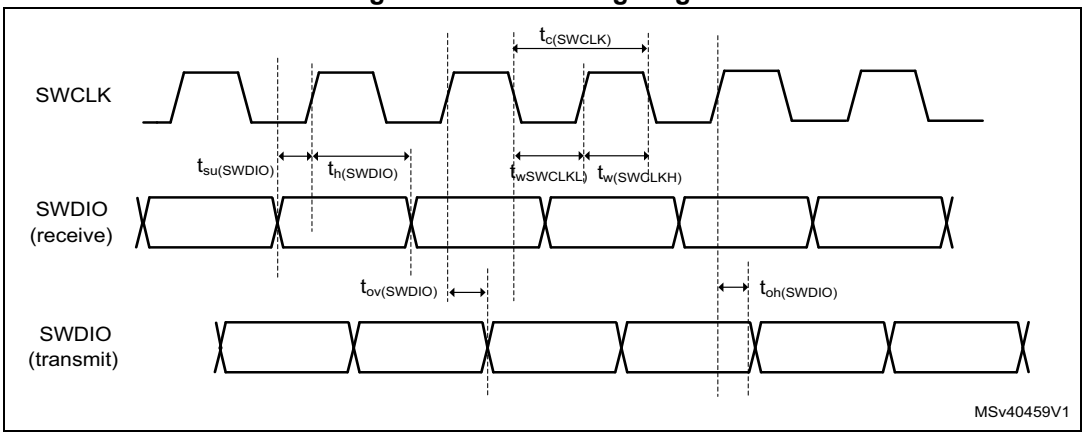


Figure 64. SWD timing diagram



7 Electrical characteristics (rev V)

7.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at T_J = 25 °C and $T_J = T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 65*.

7.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 66*.

Figure 65. Pin loading conditions

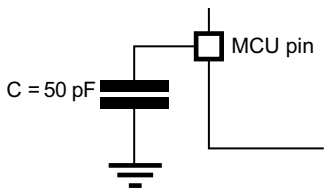
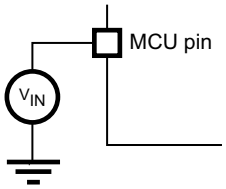
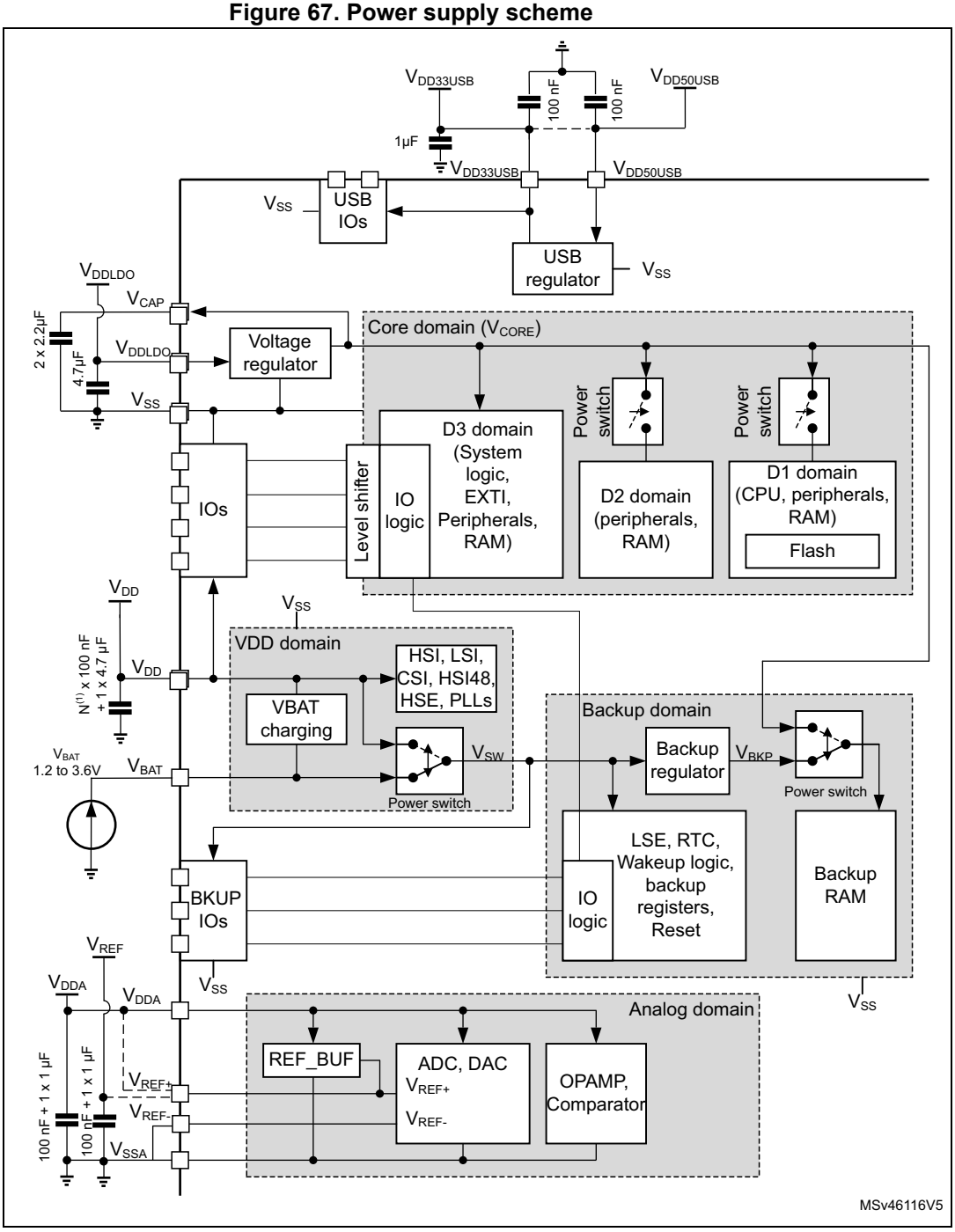


Figure 66. Pin input voltage



7.1.6 Power supply scheme

Figure 67. Power supply scheme



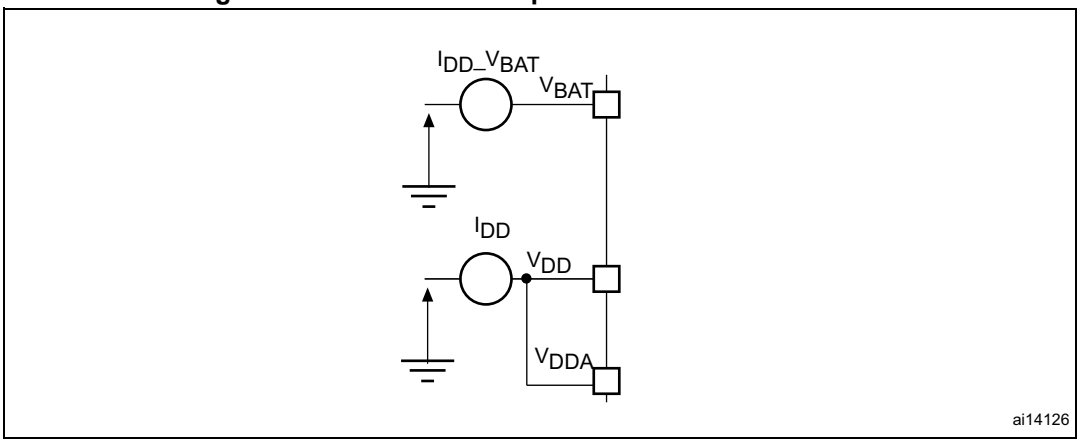
1. N corresponds to the number of VDD pins available on the package.
2. A tolerance of +/- 20% is acceptable on decoupling capacitors.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the

device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

7.1.7 Current consumption measurement

Figure 68. Current consumption measurement scheme



7.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 118: Voltage characteristics*, *Table 119: Current characteristics*, and *Table 120: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 118. Voltage characteristics (1)

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDLDO}, V_{DDA}, $V_{DD33USB}$, V_{BAT})	−0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}−0.3	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) +4.0(3)(4)	V
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	V
	Input voltage on BOOT0 pin	V_{SS}	9.0	V
	Input voltage on any other pins	V_{SS}-0.3	4.0	V
$\lvert\Delta V_{DDX}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 155: I/O current injection susceptibility* for the maximum allowed injected current values.

3. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
4. To sustain a voltage higher than 4V the internal pull-up/pull-down resistors must be disabled.

Table 119. Current characteristics

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	620	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	620	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST and B pins except PA4, PA5	−5/+0	
	Injected current on PA4, PA5	−0/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 118: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 120. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	− 65 to +150	°C
T_J	Maximum junction temperature	125	

7.3 Operating conditions

7.3.1 General operating conditions

Table 121. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	-	1.62(1)	-	3.6	V
V_{DDLDO}	Supply voltage for the internal regulator	$V_{DDLDO} \le V_{DD}$	1.62(1)	-	3.6	
$V_{DD33USB}$	Standard operating voltage, USB domain	USB used	3.0	-	3.6	V
		USB not used	0	-	3.6	
V_{DDA}	Analog operating voltage	ADC or COMP used	1.62	-	3.6	
		DAC used	1.8	-		
		OPAMP used	2.0	-		
		VREFBUF used	1.8	-		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0	-		
V_{IN}	I/O Input voltage	TT_xx I/O	−0.3	-	V_{DD}+0.3	
		BOOT0	0	-	9	
		All I/O except BOOT0 and TT_xx	−0.3	-	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$) +3.6V < 5.5V(2)(3)	
V_{CORE}	Internal regulator ON (LDO)	VOS3 (max frequency 200 MHz)	0.95	1.0	1.26	V
		VOS2 (max frequency 300 MHz)	1.05	1.10	1.26	
		VOS1 (max frequency 400 MHz)	1.15	1.20	1.26	
		VOS0(4) (max frequency 480 MHz(5))	1.26	1.35	1.40	
	Regulator OFF: external V_{CORE} voltage must be supplied from external regulator on two VCAP pins	VOS3 (max frequency 200 MHz)	0.98	1.03	1.26	
		VOS2 (max frequency 300 MHz)	1.08	1.13	1.26	
		VOS1 (max frequency 400 MHz)	1.17	1.23	1.26	
		VOS0 (max frequency 480 MHz(5))	1.37	1.38	1.40	

Table 121. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
f_{CPU}	Arm® Cortex®-M7 clock frequency	VOS3	-	-	200	MHz
		VOS2	-	-	300	
		VOS1	-	-	400	
		VOS0	-	-	480(5)	
f_{HCLK}	AHB clock frequency	VOS3	-	-	100	
		VOS2	-	-	150	
		VOS1	-	-	200	
		VOS0	-	-	240(5)	
f_{PCLK}	APB clock frequency	VOS3	-	-	50(6)	
		VOS2	-	-	75	
		VOS1	-	-	100	
		VOS0	-	-	120(5)	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		–40	85	°C
		Low-power dissipation(7)		–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation		–40	125	
		Low-power dissipation(4)		–40	130	
T_J	Junction temperature range	Suffix 6 version		–40	125	°C

1. When RESET is released functionality is guaranteed down to V_{BOR0} min
2. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, $V_{DD33USB}$) +0.3V, the internal Pull-up and Pull-Down resistors must be disabled.
4. VOS0 is available only when the LDO regulator is ON.
5. T_{Jmax} = 105 °C.
6. Maximum APB clock frequency when at least one peripheral is enabled.
7. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 8.9: Thermal characteristics*).

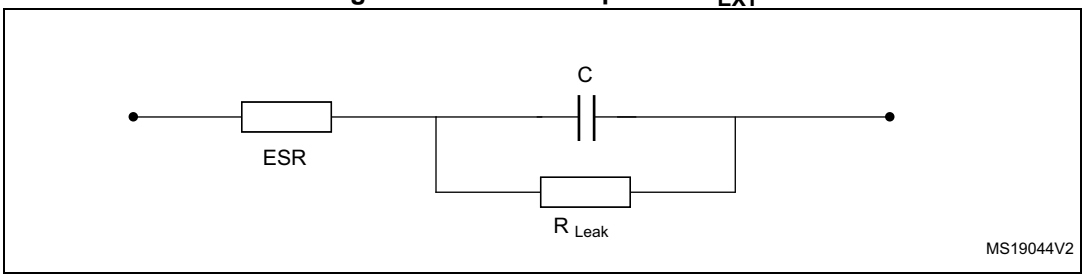
Table 122. Supply voltage and maximum frequency configuration

Power scale	V_{CORE} source	Max T_J (°C)	Max frequency (MHz)	Min V_{DDLDO} (V)
VOS0	LDO	105	480	1.7
VOS1	LDO	125	400	1.62
VOS2	LDO	125	300	1.62
VOS3	LDO	125	200	1.62
SVOS4	LDO	105	N/A	1.62
SVOS5	LDO	105	N/A	1.62

7.3.2 VCAP external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP pin. C_{EXT} is specified in *Table 123*. Two external capacitors can be connected to VCAP pins.

Figure 69. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 123. VCAP operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF(2)
ESR	ESR of external capacitor	< 100 mΩ

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.
2. This value corresponds to CEXT typical value. A variation of +/-20% is tolerated.

7.3.3 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 124. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	
t_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	0	∞	
	V_{DDUSB} fall time rate	10	∞	

7.3.4 Embedded reset and power control block characteristics

The parameters given in *Table 125* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*.

Table 125. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after BOR0 released	-	-	377	-	µs
$V_{BOR0/POR/PDR}$	Brown-out reset threshold 0 (V_{POR}/V_{PDR} thresholds)	Rising edge(1)	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable Voltage Detector threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge in Run mode	2.69	2.76	2.83	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BOR (unless BOR0) and PVD	Hysteresis in Run mode	-	100	-	mV
$I_{DD_BOR_PVD}$(1)	BOR(2) (unless BOR0) and PVD consumption from V_{DD}	-	-		0.630	µA

Table 125. Reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVM_0}	Analog voltage detector for V_{DDA} threshold 0	Rising edge	1.66	1.71	1.76	V
		Falling edge	1.56	1.61	1.66	
V_{AVM_1}	Analog voltage detector for V_{DDA} threshold 1	Rising edge	2.06	2.12	2.19	
		Falling edge	1.96	2.02	2.08	
V_{AVM_2}	Analog voltage detector for V_{DDA} threshold 2	Rising edge	2.42	2.50	2.58	
		Falling edge	2.35	2.42	2.49	
V_{AVM_3}	Analog voltage detector for V_{DDA} threshold 3	Rising edge	2.74	2.83	2.91	
		Falling edge	2.64	2.72	2.80	
V_{hyst_VDDA}	Hysteresis of V_{DDA} voltage detector	-	-	100	-	mV
I_{DD_PVM}	PVM consumption from $V_{DD(1)}$	-	-	-	0.25	µA
I_{DD_VDDA}	Voltage detector consumption on V_{DDA}(1)	Resistor bridge	-	-	2.5	µA

1. Guaranteed by design.
2. BOR0 is enabled in all modes and its consumption is therefore included in the supply current characteristics tables (refer to *Section 7.3.6: Supply current characteristics*).

7.3.5 Embedded reference voltage

The parameters given in *Table 126* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*.

Table 126. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltages	-40°C < TJ < 125 °C, V_{DD} = 3.3 V	1.180	1.216	1.255	V
$t_{S_vrefint}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}(1)(2)	VBAT sampling time when reading the internal VBAT reference voltage	-	9	-	-	
I_{refbuf}(2)	Reference Buffer consumption for ADC	V_{DDA}=3.3 V	9	13.5	23	µA
ΔV_{REFINT}(2)	Internal reference voltage spread over the temperature range	-40°C < T_J < 125 °C	-	5	15	mV
T_{coeff}(2)	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$(2)	Average Voltage coefficient	3.0V < V_{DD} < 3.6V	-	10	1370	ppm/V

Table 126. Embedded reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT_DIV1}	1/4 reference voltage	-	-	25	-	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage	-	-	50	-	
V_{REFINT_DIV3}	3/4 reference voltage	-	-	75	-	

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Guaranteed by design.

Table 127. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA} = 3.3 V	1FF1E860 - 1FF1E861

7.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 68: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{ACLK} frequency (refer to the table “Number of wait states according to CPU clock ($f_{rcc_c_ck}$) frequency and V_{CORE} range” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency divided by 2 and the APB clock frequency is AHB clock frequency divided by 2.

The parameters given in the below tables are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 121: General operating conditions*.

Table 128. Typical and maximum current consumption in Run mode, code with data processing running from ITCM, LDO regulator ON(1)

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ	Max(2)				Unit
						Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	480	148	226	307	390	-	mA
				400	125	-	-	-	-	
			VOS1	400	110	168	230	296	384	
				300	84	-	-	-	-	
			VOS2	300	76	114	170	224	297	
				216	56	88	152	205	278	
				200	53	-	-	-	-	
			VOS3	200	47	71	121	164	223	
				180	43	64	116	159	218	
				168	40	63	115	158	217	
				144	35	55	109	153	212	
				60	16	36	92	135	194	
				25	12	24	83	126	185	
		All peripherals enabled	VOS0	480	226	348	439	550	-	
				400	190	-	-	-	-	
			VOS1	400	167	256	327	416	536	
				300	135	-	-	-	-	
			VOS2	300	122	183	248	320	419	
				200	85	-	-	-	-	
			VOS3	200	76	116	174	233	313	

1. Data are in DTCM for best computation performance, the cache has no influence on consumption in this case.
2. Guaranteed by characterization results, unless otherwise specified.

Table 129. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, cache ON, LDO regulator ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ	Max(1)				Unit
						Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	480	110	222	304	388	-	mA
				400	91	-	-	-	-	
			VOS1	400	80	162	228	294	381	
				300	61.5	-	-	-	-	
			VOS2	300	55	111	168	222	294	
				200	38.5	-	-	-	-	
			VOS3	200	34.5	69	120	163	222	
		All peripherals enabled	VOS0	480	220	342	436	546	-	
				400	195	-	-	-	-	
			VOS1	400	175	264	336	424	544	
				300	135	-	-	-	-	
			VOS2	300	120	180	246	318	418	
				200	83	-	-	-	-	
			VOS3	200	75	114	173	232	312	

1. Guaranteed by characterization results, unless otherwise specified.

Table 130. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, cache OFF, LDO regulator ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ	Max(1)				Unit
						Tj=25°C	Tj=85°C	Tj=105 °C	Tj=125 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	480	87	157	259	342	453	mA
			VOS1	400	73	123	201	267	355	
			VOS2	300	52	85	150	204	277	
			VOS3	200	34	54	109	152	212	
		All peripherals enabled	VOS0	480	168	276	390	504	658	
			VOS1	400	135	224	308	397	519	
			VOS2	300	100	154	228	301	401	
			VOS3	200	70	103	167	226	307	

1. Guaranteed by characterization results, unless otherwise specified.

Table 131. Typical and maximum current consumption batch acquisition mode, LDO regulator ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ	Max(1)				Unit
						Tj=25°C	Tj=85°C	Tj=105 °C	Tj=125 °C	
I_{DD}	Supply current in batch acquisition mode	D1 Standby, D2 Standby, D3 Run	VOS3	64	2.7	4.7	12.9	19.0	27.5	mA
				8	1.1	-	-	-	-	
		D1 Stop, D2 Stop, D3 Run	VOS3	64	5.4	18.4	83.7	132.6	202.4	
				8	3.8	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

Table 132. Typical and maximum current consumption in Stop, LDO regulator ON

Symbol	Parameter	Conditions		Typ	Max(1)				Unit
					Tj=25°C	Tj=85°C	Tj=105 °C	Tj=125 °C	
$I_{DD\ (Stop)}$	D1 Stop, D2 Stop, D3 Stop	Flash memory OFF, no IWDG	SVOS5	1.27	6.3	42.5	72.0	-	mA
			SVOS4	1.96	9.4	57.4	94.6	-	
			SVOS3	2.78	13.8	75.9	121.3	183.8	
		Flash memory ON, no IWDG	SVOS5	1.27	6.3	42.5	72.0	-	
			SVOS4	2.25	9.8	57.9	95.2	-	
			SVOS3	3.07	14.1	76.4	122.0	184.8	
	D1 Stop, D2 Standby, D3 Stop	Flash memory OFF, no IWDG	SVOS5	0.91	4.6	30.4	51.2	-	
			SVOS4	1.42	6.8	41.1	67.3	-	
			SVOS3	2.02	10.0	54.4	86.6	130.0	
		Flash memory ON, no IWDG	SVOS5	0.91	4.6	30.4	51.2	-	
			SVOS4	1.70	7.2	41.5	67.9	-	
			SVOS3	2.31	10.3	54.9	87.1	130.8	
	D1 Standby, D2 Stop, D3 Stop	Flash memory OFF, no IWDG	SVOS5	0.49	2.4	16.5	28.0	-	
			SVOS4	0.76	3.6	22.2	36.6	-	
			SVOS3	1.10	5.3	29.3	46.9	71.2	
	D1 Standby, D2 Standby, D3 Stop		SVOS5	0.15	0.7	4.3	7.3	-	
			SVOS4	0.22	1.0	5.8	9.6	-	
			SVOS3	0.35	1.5	7.8	12.3	18.6	

1. Guaranteed by characterization results, unless otherwise specified.

Table 133. Typical and maximum current consumption in Sleep mode, LDO regulator

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ	Max(1)				Unit
						Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	
$I_{DD\ (Sleep)}$	Supply current in Sleep mode	All peripherals disabled	VOS0	480	50.7	96.3	253.4	366.1		mA
				400	43.4	87.8	245.5	357.9		
			VOS1	400	35.3	66.5	181.3	265.8	379.6	
				300	27.9	-	-	-	-	
			VOS2	300	24.6	47.3	139.1	207.3	300.4	
				200	18.8	-	-	-	-	
			VOS3	200	16.5	33.6	106.4	160.9	236.1	
		All peripherals enabled	VOS0	480	136.0	194.7	348.5	464.4		
				400	115.0	169.0	325.9	441.7		
			VOS1	400	97.7	138.2	251.3	338.4	456.4	
				300	74.9	-	-	-	-	
			VOS2	300	67.3	95.8	187.6	257.9	354.1	
				200	52.8	-	-	-	-	
			VOS3	200	47.1	69.3	141.4	197.7	275.1	

1. Guaranteed by characterization results, unless otherwise specified.

Table 134. Typical and maximum current consumption in Standby

Symbol	Parameter	Conditions		Typ				Max(1)				Unit
								3 V				
		Backup SRAM	RTC and LSE	1.62 V	2.4 V	3 V	3.3 V	Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	
I_{DD} (Standby)	Supply current in Standby mode	OFF	OFF	1,92	1,95	2,06	2,16	4	18	40	90	µA
		ON	OFF	3,33	3,44	3,6	3,79	8.2	47	83	141	
		OFF	ON	2,43	2,57	2,77	2,95	-	-	-	-	
		ON	ON	3,82	4,05	4,31	4,55	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

Table 135. Typical and maximum current consumption in V_{BAT} mode

Symbol	Parameter	Conditions		Typ				Max(1)				Unit
		Backup SRAM	RTC and LSE	1.2 V	2 V	3 V	3.4 V	3 V				
								Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	
I_{DD} (VBAT)	Supply current in V_{BAT} mode	OFF	OFF	0,02	0,02	0,03	0,05	0,5	4,1	10	24	µA
		ON	OFF	1,33	1,45	1,58	1,7	4,4	22	48	87	
		OFF	ON	0,46	0,57	0,75	0,87	-	-	-	-	
		ON	ON	1,77	2	2,3	2,5	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 156: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 136: Peripheral current consumption in Run mode*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- $f_{rcc_c_ck}$ is the CPU clock. $f_{PCLK} = f_{rcc_c_ck}/4$, and $f_{HCLK} = f_{rcc_c_ck}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{rcc_c_ck}$ = 480 MHz (Scale 0), $f_{rcc_c_ck}$ = 400 MHz (Scale 1), $f_{rcc_c_ck}$ = 300 MHz (Scale 2), $f_{rcc_c_ck}$ = 200 MHz (Scale 3)
- The ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 136. Peripheral current consumption in Run mode

Bus	Peripheral	VOS0	VOS1	VOS2	VOS3	Unit
AHB3	MDMA	4.6	3.8	3.4	3.2	µA/MHz
	DMA2D	2.9	2.4	2.1	1.9	
	JPGDEC	4.1	3.7	3.4	3.1	
	FLASH	17.0	15.0	14.0	12.0	
	FMC registers	0.9	1.1	0.9	0.8	
	FMC kernel	7.0	6.1	5.6	5.0	
	QUADSPI registers	1.5	1.5	1.4	1.3	
	QSPI kernel	1.0	0.9	0.8	0.7	
	SDMMC1 registers	8.2	7.2	6.7	6.0	
	SDMMC1 kernel	1.3	1.2	0.9	0.9	
	DTCM1	7.9	6.8	6.0	5.3	
	DTCM2	8.3	7.2	6.4	5.7	
	ITCM	7.0	6.3	5.6	5.1	
	D1SRAM1	13.0	11.0	9.9	8.7	
	AHB3 bridge	35.0	32.0	29.0	26.0	
	Total AHB3	**120**	**106**	**96**	**86**	
AHB1	DMA1	54.0	48.0	41.0	37.0	
	DMA2	55.0	49.0	42.0	37.0	
	ADC12 registers	4.5	4.1	3.7	3.3	
	ADC12 kernel	1.0	0.7	0.4	0.6	
	ART accelerator	4.1	3.7	3.2	2.9	
	ETH1MAC	17.0	15.0	14.0	12.0	
	ETH1TX	0.1	0.1	0.1	0.1	
	ETH1RX	0.1	0.1	0.1	0.1	
	USB1 OTG registers	23.0	21.0	19.0	17.0	
	USB1 OTG kernel	8.2	0.5	8.3	8.2	
	USB1 ULPI	0.1	0.1	0.1	0.1	
	USB2 OTG registers	21.0	19.0	17.0	15.0	
	USB2 OTG kernel	8.5	0.4	8.6	8.3	
	USB2 ULPI	23.0	19.0	20.0	19.0	
	AHB1 bridge	0.1	0.1	0.1	0.1	
	Total AHB1	**220**	**181**	**178**	**161**	

Table 136. Peripheral current consumption in Run mode (continued)

Bus	Peripheral	VOS0	VOS1	VOS2	VOS3	Unit
AHB2	DCMI	2.1	1.9	1.8	1.6	µA/MHz
	CRYPT	0.1	0.1	0.1	0.1	
	HASH	0.1	0.1	0.1	0.1	
	RNG registers	1.7	2.0	1.3	1.2	
	RNG kernel	11.0	0.1	9.7	9.4	
	SDMMC2 registers	47.0	41.0	37.0	34.0	
	SDMMC2 kernel	1.7	1.2	1.1	1.0	
	D2SRAM1	5.7	4.9	4.4	3.9	
	D2SRAM2	5.2	4.5	4.0	3.5	
	D2SRAM3	4.1	3.6	3.2	2.8	
	AHB2 bridge	0.1	0.1	0.1	0.1	
	Total AHB2	**79**	**60**	**63**	**58**	
AHB4	GPIOA	1.5	1.3	1.3	1.1	
	GPIOB	1.2	1.0	1.0	0.9	
	GPIOC	0.8	0.7	0.7	0.6	
	GPIOD	1.1	1.0	1.0	0.9	
	GPIOE	0.7	0.7	0.7	0.6	
	GPIOF	0.8	0.8	0.7	0.6	
	GPIOG	0.9	0.8	0.8	0.7	
	GPIOH	1.1	1.0	1.0	0.9	
	GPIOI	0.9	0.9	0.8	0.7	
	GPIOJ	0.8	0.8	0.7	0.7	
	GPIOK	0.7	0.8	0.7	0.6	
	CRC	0.4	0.5	0.4	0.3	
	BDMA	6.6	5.9	5.3	4.8	
	ADC3 registers	1.7	1.5	1.2	1.2	
	ADC3 kernel	0.4	0.3	0.5	0.2	
	BKPRAM	2.3	1.9	1.7	1.5	
	AHB4 bridge	0.1	0.1	0.1	0.1	
	Total AHB4	**22**	**20**	**19**	**16**	
APB3	WWDG1	0.7	0.5	0.5	0.2	µA/MHz
	LCD-TFT	81.0	36.0	33.0	30.0	
	APB3 bridge	0.3	0.2	0.1	0.1	
	Total APB3	**87**	**41**	**38**	**34**	

Table 136. Peripheral current consumption in Run mode (continued)

Bus	Peripheral	VOS0	VOS1	VOS2	VOS3	Unit
APB1	TIM2	7.7	3.6	3.3	3.0	µA/MHz
	TIM3	6.7	3.2	3.0	2.7	
	TIM4	6.3	3.1	2.8	2.5	
	TIM5	7.4	3.5	3.2	2.8	
	TIM6	1.4	0.7	0.8	0.6	
	TIM7	1.4	0.7	0.7	0.6	
	TIM12	3.2	1.5	1.5	1.3	
	TIM13	2.3	1.1	1.1	0.9	
	TIM14	2.1	1.1	1.1	0.9	
	LPTIM1 registers	0.7	0.5	0.8	0.7	
	LPTIM1 kernel	2.4	2.3	1.9	1.7	
	WWDG2	0.6	0.5	0.5	0.4	
	SPI2 registers	2.0	1.8	1.7	1.4	
	SPI2 kernel	0.8	0.6	0.5	0.6	
	SPI3 registers	1.8	1.6	1.6	1.3	
	SPI3 kernel	0.7	0.9	0.7	0.7	
	SPDIFRX1 registers	0.5	0.7	0.7	0.6	
	SPDIFRX1 kernel	3.5	2.8	2.4	2.2	
	USART2 registers	1.9	1.7	1.4	1.3	
	USART2 kernel	4.3	3.9	3.6	3.2	
	USART3 registers	1.9	1.7	1.4	1.3	
	USART3 kernel	4.4	3.9	3.5	3.2	
	UART4 registers	1.7	1.5	1.4	1.4	
	UART4 kernel	3.9	3.4	3.1	2.8	
	UART5 registers	1.6	1.4	1.4	1.3	
	UART5 kernel	3.8	3.4	3.0	2.7	
	I2C1 registers	1.1	0.8	0.9	0.8	
	I2C1 kernel	2.5	2.3	2.0	1.9	
	I2C2 registers	1.0	0.8	0.9	0.8	

Table 136. Peripheral current consumption in Run mode (continued)

Bus	Peripheral	VOS0	VOS1	VOS2	VOS3	Unit
APB1 (continued)	I2C2 kernel	2.3	2.2	1.9	1.7	µA/MHz
	I2C3 registers	0.8	1.0	0.8	0.8	
	I2C3 kernel	2.4	1.9	1.8	1.6	
	HDMI-CEC registers	0.7	0.5	0.6	0.5	
	HDMI-CEC kernel	0.1	0.1	3.2	0.1	
	DAC12	3.6	1.3	1.2	1.0	
	USART7 registers	1.8	1.8	1.6	1.4	
	USART7 kernel	4.0	3.3	3.0	2.8	
	USART8 registers	2.0	1.6	1.6	1.4	
	USART8 kernel	3.9	3.4	3.1	2.8	
	CRS	6.4	5.5	5.0	4.5	
	SWPMI registers	2.7	2.4	2.3	1.9	
	SWPMI kernel	0.1	0.1	0.1	0.1	
	OPAMP	0.2	0.3	0.3	0.2	
	MDIO	3.3	2.9	2.6	2.3	
	FDCAN registers	19.0	17.0	15.0	13.0	
	FDCAN kernel	9.1	7.9	6.9	6.4	
	APB1 bridge	0.1	0.1	0.1	0.1	
	Total APB1	**142**	**108**	**102**	**88**	
APB2	TIM1	11.0	5.0	4.5	4.0	
	TIM8	10.0	4.7	4.3	3.8	
	USART1 registers	3.6	2.5	2.7	2.9	
	USART1 kernel	0.1	0.1	0.1	0.1	
	USART6 registers	4.5	3.0	3.1	3.4	
	USART6 kernel	0.1	0.1	0.1	0.1	
	SPI1 registers	2.0	1.7	1.6	1.4	
	SPI1 kernel	0.9	0.8	0.7	0.6	
	SPI4 registers	2.1	1.7	1.6	1.5	
	SPI4 kernel	0.6	0.5	0.5	0.3	
	TIM15	5.5	2.5	2.3	2.1	
	TIM16	4.1	2.0	1.8	1.7	
	TIM17	4.1	1.9	1.8	1.6	
	SPI5 registers	2.0	1.8	1.6	1.3	
	SPI5 kernel	0.5	0.4	0.4	0.5	
	SAI1 registers	1.3	1.1	1.1	1.0	

Table 136. Peripheral current consumption in Run mode (continued)

Bus	Peripheral	VOS0	VOS1	VOS2	VOS3	Unit
APB2 (continued)	SAI1 kernel	1.4	1.1	1.0	0.8	µA/MHz
	SAI2 registers	1.5	1.3	1.2	1.0	
	SAI2 kernel	1.1	1.0	0.9	0.9	
	SAI3 registers	1.6	1.3	1.1	1.0	
	SAI3 kernel	1.1	1.2	1.1	0.9	
	DFSDM1 registers	6.5	5.8	5.2	4.7	
	DFSDM1 kernel	0.3	0.2	0.2	0.4	
	HRTIM	84.0	39.0	35.0	32.0	
	APB2 bridge	0.2	0.1	0.1	0.2	
	Total APB2	**150**	**81**	**74**	**68**	
APB4	SYSCFG	0.9	1.0	0.7	0.8	
	LPUART1 registers	1.1	1.3	1.0	0.8	
	LPUART1 kernel	2.9	2.2	2.2	2.1	
	SPI6 registers	1.8	1.6	1.4	1.3	
	SPI6 kernel	0.4	0.4	0.5	0.3	
	I2C4 registers	0.9	0.7	0.7	0.4	
	I2C4 kernel	2.2	2.1	1.9	1.8	
	LPTIM2 registers	0.8	0.6	0.7	0.5	
	LPTIM2 kernel	2.3	2.1	1.8	1.4	
	LPTIM3 registers	0.7	0.7	0.7	0.4	
	LPTIM3 kernel	2.1	1.7	1.6	1.5	
	LPTIM4 registers	0.8	0.4	0.6	0.4	
	LPTIM4 kernel	2.2	2.0	1.7	1.5	
	LPTIM5 registers	0.5	0.4	0.6	0.4	
	LPTIM5 kernel	2.0	1.8	1.5	1.2	
	COMP12	0.6	0.4	0.5	0.2	
	VREF	0.4	0.2	0.2	0.1	
	RTC	1.1	0.9	1.0	0.6	
	SAI4 registers	1.7	1.4	1.3	1.0	
	SAI4 kernel	2.0	2.0	1.8	1.6	
	APB4 bridge	0.1	0.1	0.1	0.1	
	Total APB4	**28**	**24.4**	**22.4**	**18.9**	

7.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 137* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PC1) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 137. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep	-	9	10	CPU clock cycles
t_{WUSTOP}(2)	Wakeup from Stop	VOS3, HSI, Flash memory in normal mode	4.4	5.6	µs
		VOS3, HSI, Flash memory in low-power mode	12	15	
		VOS4, HSI, Flash memory in normal mode	15	20	
		VOS4, HSI, Flash memory in low-power mode	23	28	
		VOS5, HSI, Flash memory in normal mode	39	71	
		VOS5, HSI, Flash memory in low-power mode	39	47	
		VOS3, CSI, Flash memory in normal mode	30	37	
		VOS3, CSI, Flash memory in low power mode	36	50	
		VOS4, CSI, Flash memory in normal mode	38	48	
		VOS4, CSI, Flash memory in low-power mode	47	61	
		VOS5, CSI, Flash memory in normal mode	68	75	
		VOS5, CSI, Flash memory in low-power mode	68	77	
t_{WUSTOP_KERON}(2)	Wakeup from Stop, clock kept running	VOS3, HSI, Flash memory in normal mode	2.6	3.4	
		VOS3, CSI, Flash memory in normal mode	26	36	
$t_{WUSTDBY}$(2)	Wakeup from Standby mode	-	390	500	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

7.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

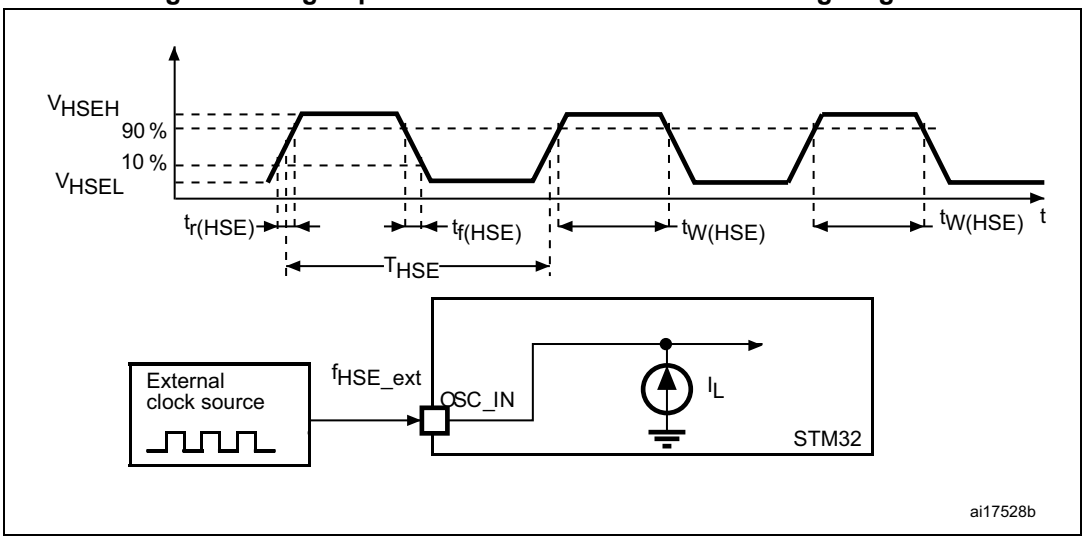
The external clock signal has to respect the *Table 156: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 70*.

Table 138. High-speed external user clock characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	4	25	50	MHz
V_{HSEH}	Digital OSC_IN input high-level voltage	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input low-level voltage	V_{SS}	-	0.3 V_{DD}	
$t_{W(HSE)}$	OSC_IN high or low time	7	-	-	ns

1. Guaranteed by design.

Figure 70. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 156: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 71*.

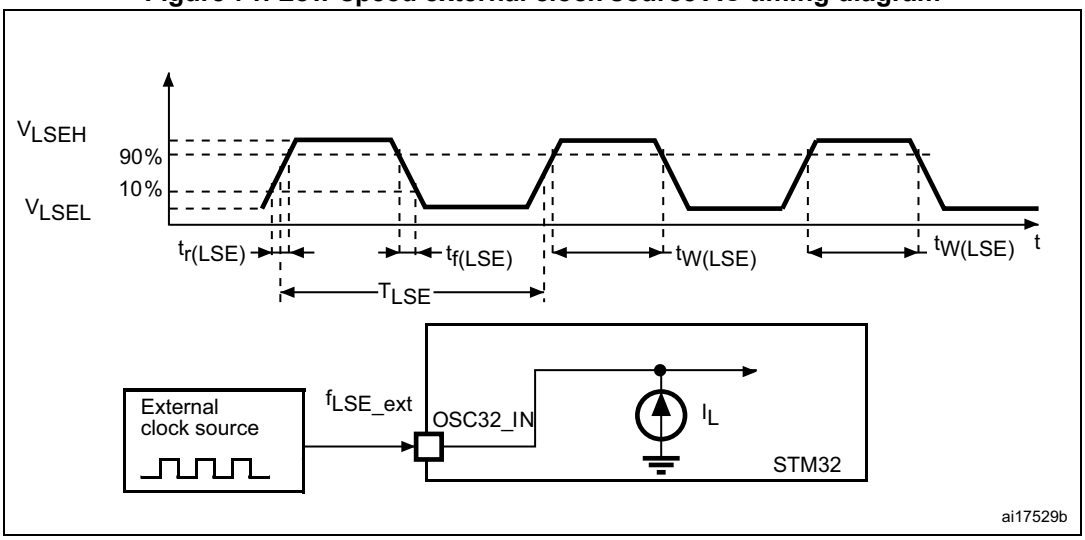
Table 139. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AL/AF/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 71. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 140*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 140. 4-48 MHz HSE oscillator characteristics(1)

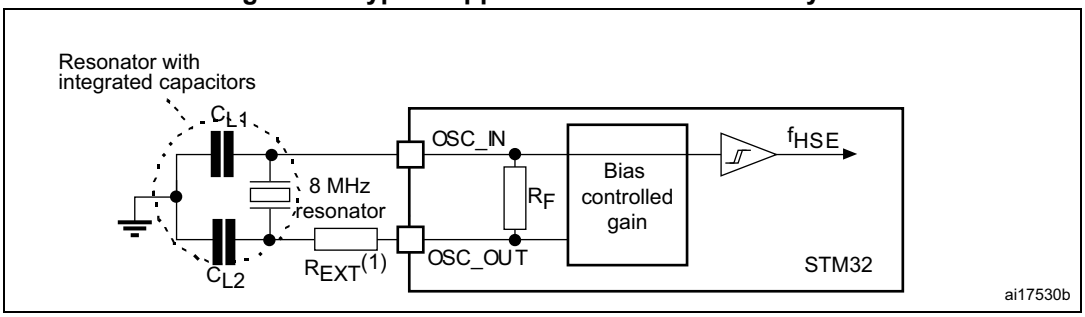
Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	4	mA
		V_{DD}=3 V, Rm=30 Ω C_L=10pF@4MHz	-	0.35	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 8 MHz	-	0.40	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 16 MHz	-	0.45	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 32 MHz	-	0.65	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 48 MHz	-	0.95	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
t_{SU}(4)	Start-up time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 72*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 72. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 141*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

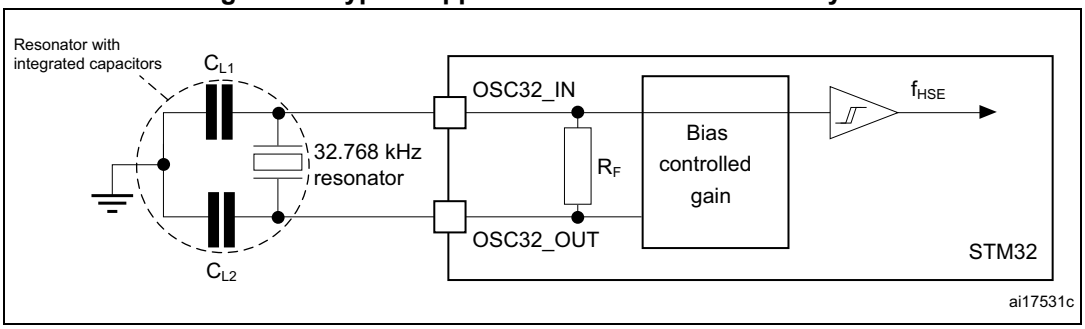
Table 141. Low-speed external user clock characteristics(1)

Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 00, Low drive capability	-	290	-	nA
		LSEDRV[1:0] = 01, Medium Low drive capability	-	390	-	
		LSEDRV[1:0] = 10, Medium high drive capability	-	550	-	
		LSEDRV[1:0] = 11, High drive capability	-	900	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(3)	Startup time	VDD is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for STM8AL/AF/S, STM32 MCUs and MPUs”.
3. t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768k Hz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AL/AF/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 73. Typical application with a 32.768 kHz crystal



1. *An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

7.3.9 Internal clock source characteristics

The parameters given in *Table 142* to *Table 145* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*.

48 MHz high-speed internal RC oscillator (HSI48)

Table 142. HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD}=3.3 V, TJ=30 °C	47.5(1)	48	48.5(1)	MHz
TRIM(2)	USER trimming step	-	-	0.175	-	%
USER TRIM COVERAGE(3)	USER TRIMMING Coverage	± 32 steps	±4.79	±5.60	-	%
DuCy(HSI48)(2)	Duty Cycle	-	45	-	55	%
ACCHSI48_REL(3)(4)	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	T_J=-40 to 125 °C	–4.5	-	3.5	%
Δ_{VDD}(HSI48)(3)	HSI48 oscillator frequency drift with V_{DD}(5)	V_{DD}=3 to 3.6 V	-	0.025	0.05	%
		V_{DD}=1.62 V to 3.6 V	-	0.05	0.1	
$t_{su(HSI48)}$(2)	HSI48 oscillator start-up time	-	-	2.1	4.0	µs
$I_{DD(HSI48)}$(2)	HSI48 oscillator power consumption	-	-	350	400	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(6)	-	-	± 0.15	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(6)	-	-	± 0.25	-	ns

1. Guaranteed by test in production.
2. Guaranteed by design.
3. Guaranteed by characterization.

4. ΔfHSI = ACCHSI48_REL + Δ_{VDD}.
5. These values are obtained by using the formula: (Freq(3.6V) - Freq(3.0V)) / Freq(3.0V) or (Freq(3.6V) - Freq(1.62V)) / Freq(1.62V).
6. Jitter measurements are performed without clock source activated in parallel.

64 MHz high-speed internal RC oscillator (HSI)

Table 143. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	V_{DD}=3.3 V, T_J=30 °C	63.7(2)	64	64.3(2)	MHz
TRIM	HSI user trimming step	Trimming is not a multiple of 32	-	0.24	0.32	%
		Trimming is 128, 256 and 384	−5.2	−1.8	-	
		Trimming is 64, 192, 320 and 448	−1.4	−0.8	-	
		Other trimming are a multiple of 32 (not including multiple of 64 and 128)	−0.6	−0.25	-	
DuCy(HSI)	Duty Cycle	-	45	-	55	%
$\Delta_{VDD\ (HSI)}$	HSI oscillator frequency drift over V_{DD} (reference is 3.3 V)	V_{DD}=1.62 to 3.6 V	−0.12	-	0.03	%
$\Delta_{TEMP\ (HSI)}$	HSI oscillator frequency drift over temperature (reference is 64 MHz)	T_J=-20 to 105 °C	−1(3)	-	1(3)	%
		T_J=−40 to $T_J$max °C	−2(3)	-	1(3)	
t_{su}(HSI)	HSI oscillator start-up time	-	-	1.4	2	µs
t_{stab}(HSI)	HSI oscillator stabilization time	at 1% of target frequency	-	4	8	µs
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	400	µA

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by test in production.
3. Guaranteed by characterization.

4 MHz low-power internal RC oscillator (CSI)

Table 144. CSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CSI}	CSI frequency	V_{DD}=3.3 V, T_J=30 °C	3.96(2)	4	4.04(2)	MHz
TRIM	Trimming step	-	-	0.35	-	%
DuCy(CSI)	Duty Cycle	-	45	-	55	%
Δ_{TEMP} (CSI)	CSI oscillator frequency drift over temperature	T_J = 0 to 85 °C	-	−3.7(3)	4.5(3)	%
		T_J = −40 to 125 °C	-	−11(3)	7.5(3)	

Table 144. CSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
D_{VDD} (CSI)	CSI oscillator frequency drift over V_{DD}	V_{DD} = 1.62 to 3.6 V	-	−0.06	0.06	%
$t_{su(CSI)}$	CSI oscillator startup time	-	-	1	2	µs
$t_{stab(CSI)}$	CSI oscillator stabilization time (to reach ±3% of f_{CSI})	-	-	-	4	cycle
$I_{DD(CSI)}$	CSI oscillator power consumption	-	-	23	30	µA

1. Guaranteed by design.
2. Guaranteed by test in production.
3. Guaranteed by characterization.

Low-speed internal (LSI) RC oscillator

Table 145. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.3 V, T_J = 25 °C	31.4(1)	32	32.6(1)	kHz
		T_J = –40 to 110 °C, V_{DD} = 1.62 to 3.6 V	29.76(2)	-	33.6(2)	
		T_J = –40 to 125 °C, V_{DD} = 1.62 to 3.6 V	29.4	-	33.6	
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	80	130	µs
$t_{stab(LSI)}$(3)	LSI oscillator stabilization time (5% of final value)	-	-	120	170	
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	-	130	280	nA

1. Guaranteed by test in production.
2. Guaranteed by characterization results.
3. Guaranteed by design.

7.3.10 PLL characteristics

The parameters given in *Table 146* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*.

Table 146. PLL characteristics (wide VCO frequency range)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		2	-	16	MHz
	PLL input clock duty cycle	-		10	-	90	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	VOS0		1.5	-	480(2)	MHz
		VOS1		1.5	-	400(2)	
		VOS2		1.5	-	300(2)	
		VOS3		1.5	-	200(2)	
f_{VCO_OUT}	PLL VCO output	-		192	-	960	
t_{LOCK}	PLL lock time	Normal mode		-	50(3)	150(3)	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)		-	58(3)	166(3)	
Jitter	Cycle-to-cycle jitter(4)	-	VCO = 192 MHz	-	134	-	±ps
			VCO = 200 MHz	-	134	-	
			VCO = 400 MHz	-	76	-	
			VCO = 800 MHz	-	39	-	
	Long term jitter	Normal mode	VCO = 800 MHz	-	±0.7	-	%
		Sigma-delta mode (CKIN = 16 MHz)	VCO = 800 MHz	-	±0.8	-	
$I_{DD(PLL)}$(3)	PLL power consumption on V_{DD}	VCO freq = 836 MHz	V_{DDA}	-	590	1500	µA
			V_{CORE}	-	720	-	
		VCO freq = 192 MHz	V_{DDA}	-	180	600	
			V_{CORE}	-	280	-	

1. Guaranteed by design unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation (480 MHz for VOS0, 400 MHz for VOS1, 300 MHz for VOS2, 200 MHz for VOS3).
3. Guaranteed by characterization results.
4. Integer mode only.

Table 147. PLL characteristics (medium VCO frequency range)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		1	-	2	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS1		1.17	-	210	MHz
		VOS2		1.17	-	210	
		VOS3		1.17	-	200	
f_{VCO_OUT}	PLL VCO output	-		150	-	420	
t_{LOCK}	PLL lock time	Normal mode		-	60(2)	100(2)	µs
		Sigma-delta mode		forbidden			
Jitter	Cycle-to-cycle jitter(3)	-	VCO = 150 MHz	-	145	-	±ps
			VCO = 300 MHz	-	91	-	
			VCO = 400 MHz	-	64	-	
			VCO = 420 MHz	-	63	-	
	Period jitter	f_{PLL_OUT} = 50 MHz	VCO = 150 MHz	-	55	-	±-ps
			VCO = 400 MHz	-	30	-	
	Long term jitter	Normal mode	VCO = 400 MHz	-	±0.3	-	%
I(PLL)(2)	PLL power consumption on V_{DD}	VCO freq = 420MHz	VDD	-	440	1150	µA
			VCORE	-	530	-	
		VCO freq = 150MHz	VDD	-	180	500	
			VCORE	-	200	-	

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by characterization results.
3. Integer mode only.

7.3.11 Memory characteristics

Flash memory

The characteristics are given at T_J = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 148. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode	-	6.5	-	mA
		Write / Erase 16-bit mode	-	11.5	-	
		Write / Erase 32-bit mode	-	20	-	
		Write / Erase 64-bit mode	-	35	-	

Table 149. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word (266 bits) programming time	Program/erase parallelism x 8	-	290	580(2)	µs
		Program/erase parallelism x 16	-	180	360	
		Program/erase parallelism x 32	-	130	260	
		Program/erase parallelism x 64	-	100	200	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism x 8	-	2	4	s
		Program/erase parallelism x 16	-	1.8	3.6	
		Program/erase parallelism x 32	-	1.1	2.2	
		Program/erase parallelism x 64	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism x 8	-	13	26	
		Program/erase parallelism x 16	-	8	16	
		Program/erase parallelism x 32	-	6	12	
		Program/erase parallelism x 64	-	5	10	
V_{prog}	Programming voltage	Program parallelism x 8	1.62	-	3.6	V
		Program parallelism x 16				
		Program parallelism x 32				
		Program parallelism x 64	1.8	-	3.6	

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 10K erase operations.

Table 150. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_J = –40 to +125 °C (6 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle at T_A = 85 °C	30	Years
		10 kcycles at T_A = 55 °C	20	

1. Guaranteed by characterization results.

7.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 151*. They are based on the EMS levels and classes defined in application note AN1709.

Table 151. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, UFBGA240, $f_{rcc_c_ck}$ = 400 MHz, conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 152. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/400 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, UFBGA240 package, conforming to IEC61967-2	0.1 to 30 MHz	11	dBµV
			30 to 130 MHz	6	
			130 MHz to 1 GHz	12	
			1 GHz to 2 GHz	7	
			EMI Level	2.5	-

7.3.13 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 153. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	All	1C	1000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All	C1	250	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 154. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_A = +25 °C conforming to JESD78	II level A

7.3.14 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 155. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	PA7, PC5, PG1, PB14, PJ7, PA11, PA12, PA13, PA14, PA15, PJ12, PB4	5	0	mA
	PA2, PH2, PH3, PE8, PA6, PA7, PC4, PE7, PE10, PE11	0	NA	
	PA0, PA_C, PA1, PA1_C, PC2, PC2_C, PC3, PC3_C, PA4, PA5, PH4, PH5, BOOT0	0	0	
	All other I/Os	5	NA	

1. Guaranteed by characterization.

7.3.15 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 156: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 121: General operating conditions*. All I/Os are CMOS and TTL compliant (except for BOOT0).

For information on GPIO configuration, refer to the application note AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption” available from the ST website www.st.com.

Table 156. I/O static characteristics

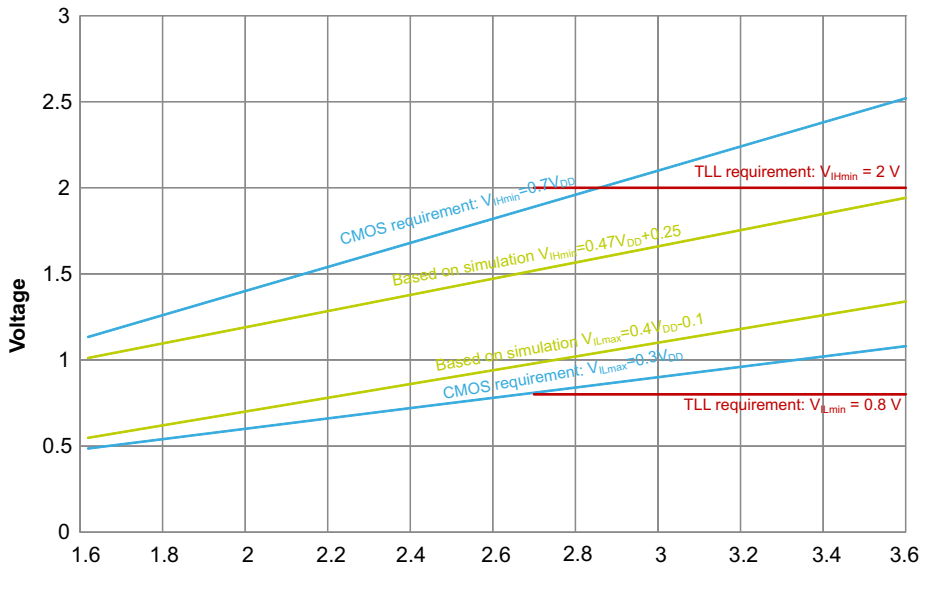
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.3V_{DD}$(1)	V
	I/O input low level voltage except BOOT0		-	-	$0.4V_{DD}-0.1$(2)	
	BOOT0 I/O input low level voltage		-	-	$0.19V_{DD}+0.1$(2)	
V_{IH}	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	$0.7V_{DD}$(1)	-	-	V
	I/O input high level voltage except BOOT0(3)		$0.47V_{DD}+0.25$(2)	-	-	
	BOOT0 I/O input high level voltage(3)		$0.17V_{DD}+0.6$(2)	-	-	
V_{HYS}(2)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V< V_{DDIOx} <3.6 V	-	250	-	mV
	BOOT0 I/O input hysteresis		-	200	-	
I_{leak}(4)	FT_xx Input leakage current(2)	0< V_{IN} ≤ Max(V_{DDXXX})(9)	-	-	+/-250	nA
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(6)(9)	-	-	1500	
	FT_u IO	0< V_{IN} ≤ Max(V_{DDXXX})(9)	-	-	+/- 350	
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(6)(9)	-	-	5000(7)	
	TT_xx Input leakage current	0< V_{IN} ≤ Max(V_{DDXXX}) (9)	-	-	+/-250	
	VPP (BOOT0 alternate function)	0< V_{IN} ≤ V_{DDIOX}	-	-	15	
		V_{DDIOX} < V_{IN} ≤ 9 V			35	
R_{PU}	Weak pull-up equivalent resistor(8)	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(8)	V_{IN}=V_{DD}(9)	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Compliant with CMOS requirements.
2. Guaranteed by design.

3. V_{DDIOx} represents V_{DDIO1}, V_{DDIO2} or V_{DDIO3}. V_{DDIOx}= V_{DD}.
4. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total_Ileak_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x $I_{lkg(Max)}$.
5. All FT_xx IO except FT_lu, FT_u and PC3.
6. V_{IN} must be less than Max(VDDXXX) + 3.6 V.
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, $V_{DD33USB}$) +0.3 V, the internal pull-up and pull-down resistors must be disabled.
8. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).
9. Max(VDDXXX) is the maximum value of all the I/O supplies.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 74*.

Figure 74. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 7.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 119*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 119*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 157: Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8* and *Table 158: Output voltage characteristics for PC13, PC14, PC15 and PI8* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 157. Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO}=8 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO}=-8 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO}=8 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO}=-8 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO}=20 mA 2.7 V≤ V_{DD} ≤3.6 V	-	1.3	
V_{OH}(3)	Output high level voltage	I_{IO}=-20 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−1.3	-	
V_{OL}(3)	Output low level voltage	I_{IO}=4 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage	I_{IO}=-4 mA 1.62 V≤V_{DD}<3.6 V	V_{DD}−-0.4	-	
V_{OLFM+}(3)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO}= 20 mA 2.3 V≤ V_{DD}≤3.6 V	-	0.4	
		I_{IO}= 10 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 118: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Table 158. Output voltage characteristics for PC13, PC14, PC15 and PI8(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO}=3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO}=-3 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO}=3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(2)	Output high level voltage	TTL port(2) I_{IO}=-3 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}(2)	Output low level voltage	I_{IO}=1.5 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(2)	Output high level voltage	I_{IO}=-1.5 mA 1.62 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 118: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of SYSCFG_CCCSR register can be used to optimize the I/O speed when the product voltage is below 2.7 V.

Table 159. Output timing characteristics (HSLV OFF)(1)(2)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	12	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	12	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	16	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	4	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	16.6	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	33.3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	13.3	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
01	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	60	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	80	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	110	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	5.2	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.2	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	7.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	2.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	5.2	

Table 159. Output timing characteristics (HSLV OFF)(1)(2) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
10	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	85	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	35	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	110	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	40	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	166	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	85	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	3.8	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	6.9	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	2.8	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	5.2	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	1.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V^{v}	-	3.3	
11	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V^{v}	-	100	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	50	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V^{v}	-	133	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	66	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	220	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	100	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	3.3	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	6.6	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	2.4	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	4.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	1.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	2.7	

1. Guaranteed by design.
2. The frequency of the GPIOs that can be supplied in V_{BAT} mode (PC13, PC14, PC15 and PI8) is limited to 2 MHz
3. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
4. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
5. Compensation system enabled.

Output buffer timing characteristics (HSLV option enabled)

Table 160. Output timing characteristics (HSLV ON)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	11	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	9	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	
01	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	50	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	58	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	66	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	4.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
10	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	55	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	80	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	133	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.8	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	4	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	2.4	
11	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	60	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	90	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	175	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.3	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	3.6	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	1.9	

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

7.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 156: I/O static characteristics*).

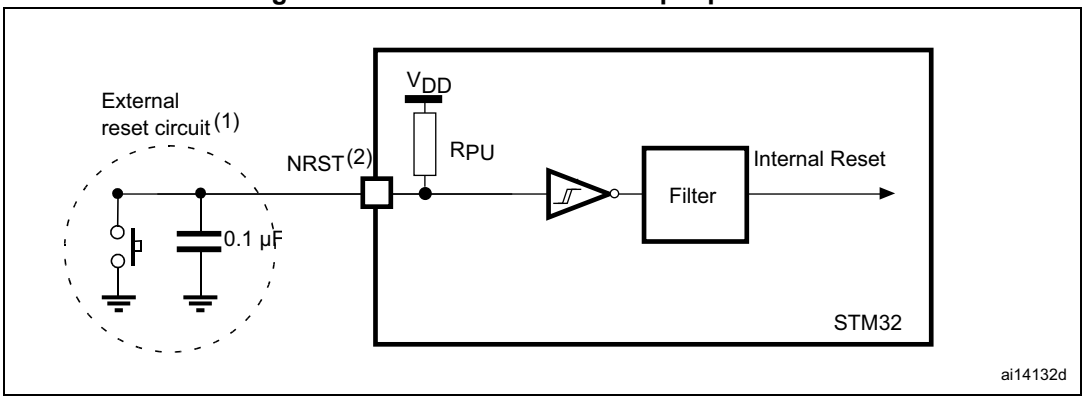
Unless otherwise specified, the parameters given in *Table 161* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*.

Table 161. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	1.71 V < V_{DD} < 3.6 V	300	-	-	
		1.62 V < V_{DD} < 3.6 V	1000	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 75. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 156*. Otherwise the reset is not taken into account by the device.

7.3.17 FMC characteristics

Unless otherwise specified, the parameters given in *Table 162* to *Table 175* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1.

Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics.

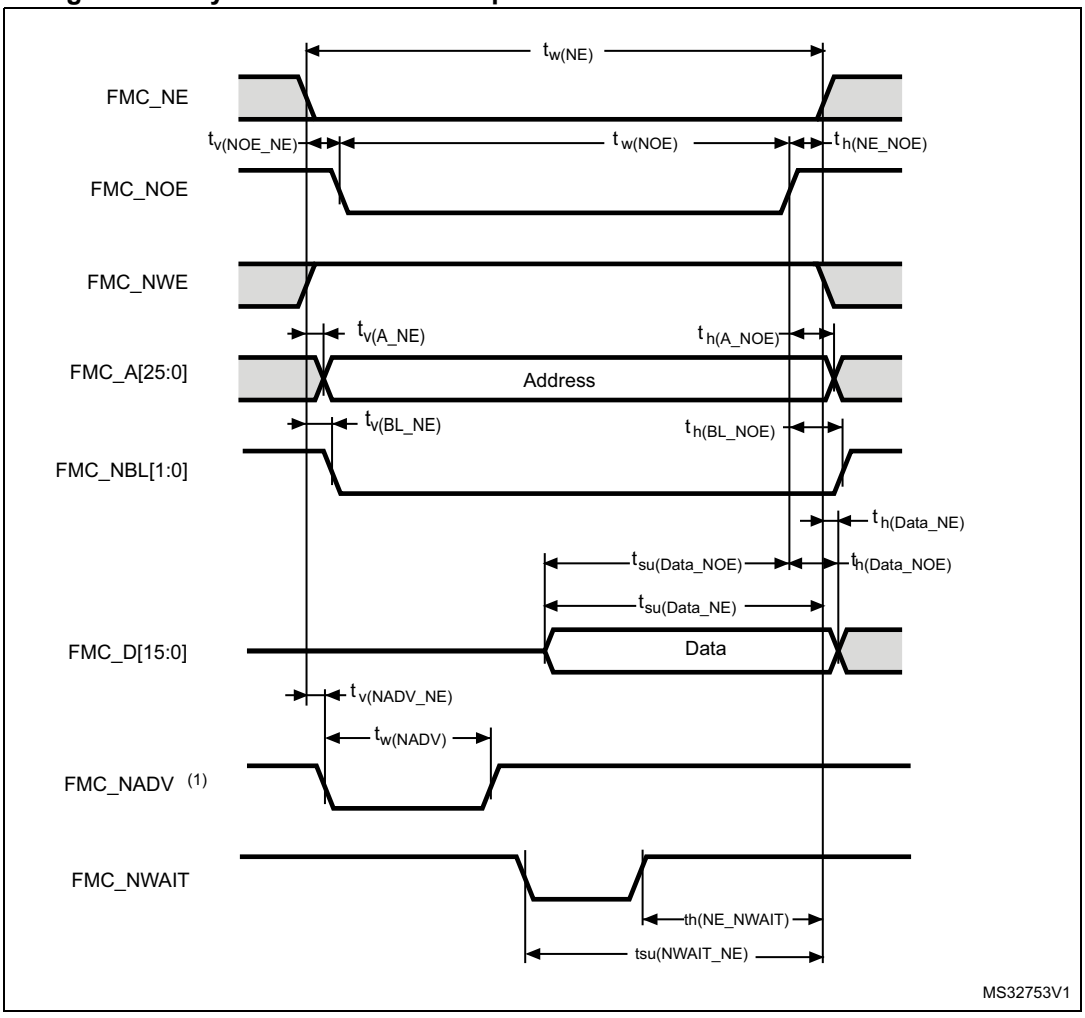
Asynchronous waveforms and timings

Figure 76 through *Figure 78* represent asynchronous waveforms and *Table 162* through *Table 169* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all timing tables, the T_{KERCK} is the $f_{mc_ker_ck}$ clock period.

Figure 76. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 162. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck}-1$	$3T_{fmc_ker_ck}+1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc_ker_ck}-1$	$2T_{fmc_ker_ck}+1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	11	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	11	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck}+1$	

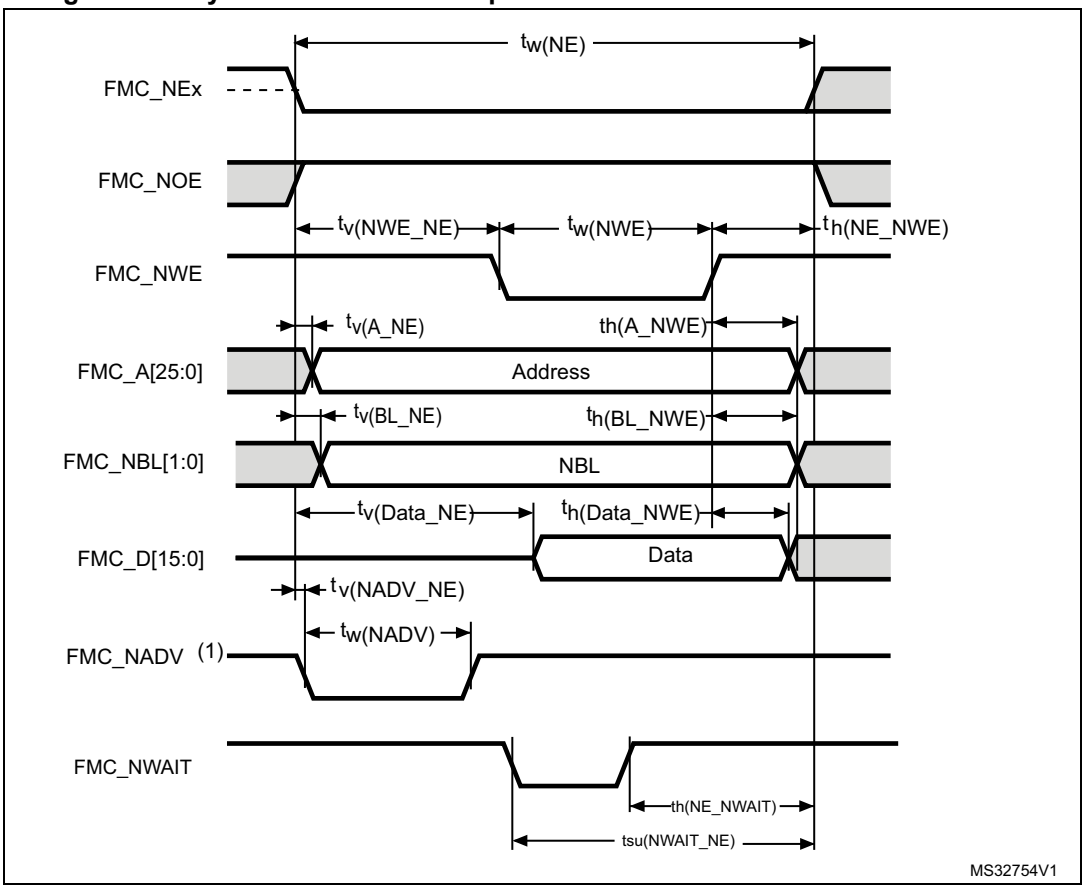
1. Guaranteed by characterization results.

Table 163. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{fmc_ker_ck}+1$	$7T_{fmc_ker_ck}+1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$5T_{fmc_ker_ck}-1$	$5T_{fmc_ker_ck}+1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc_ker_ck}-0.5$	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4T_{fmc_ker_ck}+11$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$3T_{fmc_ker_ck}+11.5$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Figure 77. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 164. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck} - 1$	$3T_{fmc_ker_ck}$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck}$	$T_{fmc_ker_ck}+1$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck}+0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck}$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{fmc_ker_ck}+ 2.5$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck}+0.5$	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck}+ 1$	

1. Guaranteed by characterization results.

Table 165. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck} - 1$	$8T_{fmc_ker_ck}+1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc_ker_ck} - 1.5$	$6T_{fmc_ker_ck}+0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck}+13$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}+13$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Figure 78. Asynchronous multiplexed PSRAM/NOR read waveforms

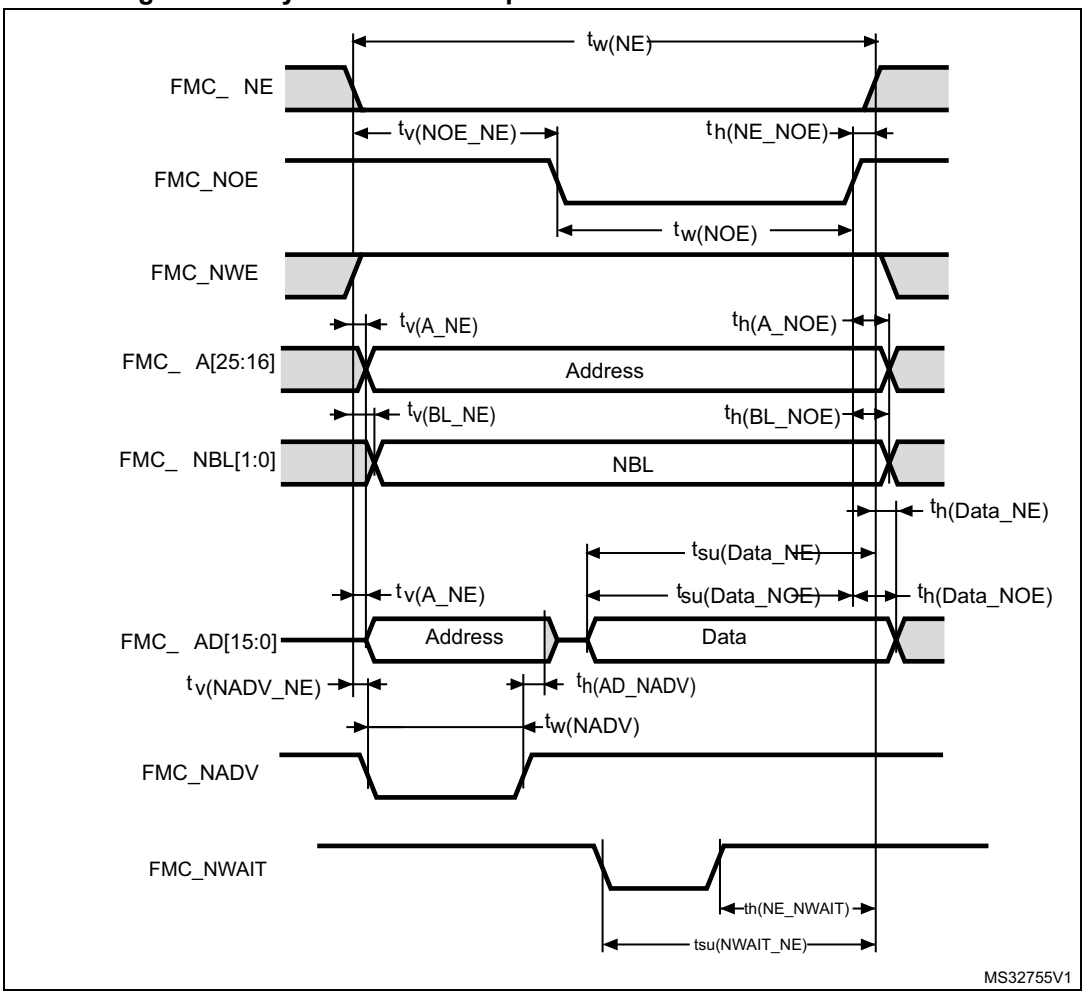


Table 166. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck} - 1$	$4T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc_ker_ck}$	$2T_{fmc_ker_ck} + 0.5$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high)	$T_{fmc_ker_ck} + 0.5$	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	11	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	11	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Guaranteed by characterization results.

Table 167. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck} - 1$	$8T_{fmc_ker_ck}$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc_ker_ck} - 1.5$	$5T_{fmc_ker_ck} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4T_{fmc_ker_ck} + 11$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$3T_{fmc_ker_ck} + 11.5$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Table 168. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck} - 1$	$4T_{fmc_ker_ck}$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc_ker_ck} - 0.5$	$2T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck}$	$T_{fmc_ker_ck} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	$T_{fmc_ker_ck} + 0.5$	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc_ker_ck} + 2$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck} + 0.5$	-	

1. Guaranteed by characterization results.

Table 169. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck} - 1$	$9T_{fmc_ker_ck}$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc_ker_ck} - 0.5$	$7T_{fmc_ker_ck} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 11$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck} + 11.5$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Synchronous waveforms and timings

Figure 79 through *Figure 82* represent synchronous waveforms and *Table 170* through *Table 173* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc_ker_ck}$ is the $f_{mc_ker_ck}$ clock period, with the following FMC_CLK maximum values:

- For 2.7 V<V_{DD}<3.6 V, FMC_CLK = 125 MHz at 20 pF
- For 1.8 V<V_{DD}<1.9 V, FMC_CLK = 100 MHz at 20 pF
- For 1.62 V<V_{DD}<1.8 V, FMC_CLK = 100 MHz at 15 pF

Figure 79. Synchronous multiplexed NOR/PSRAM read timings

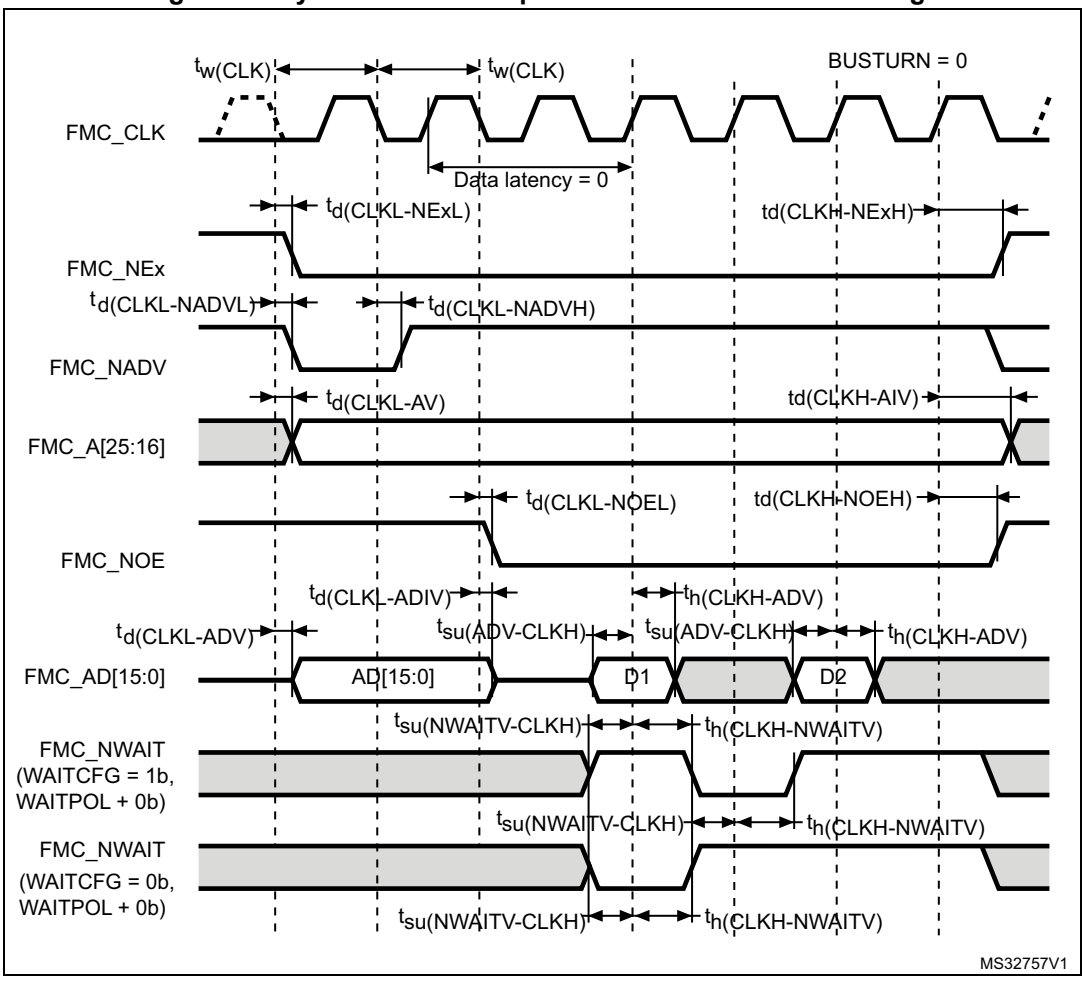


Table 170. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck}-1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc_ker_ck}+0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc_ker_ck}-0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	3	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	0	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	

1. Guaranteed by characterization results.

Figure 80. Synchronous multiplexed PSRAM write timings

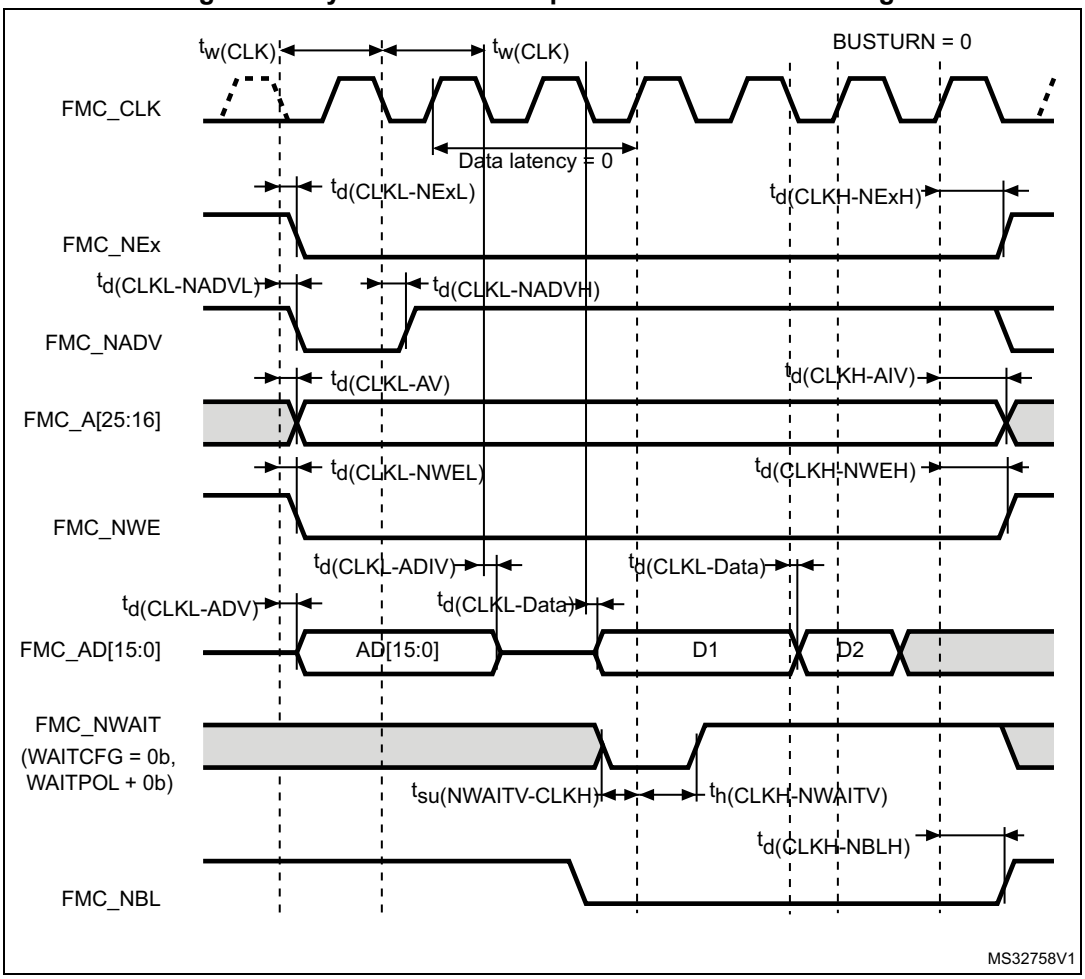


Table 171. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, V_{DD} = 2.7 to 3.6 V	$2T_{fmc_ker_ck} - 1$ 1	-	Ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x =0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$T_{fmc_ker_ck}$ +0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x =16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x =16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc_ker_ck}$ +0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to to FMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	2.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc_ker_ck}$ +0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Figure 81. Synchronous non-multiplexed NOR/PSRAM read timings

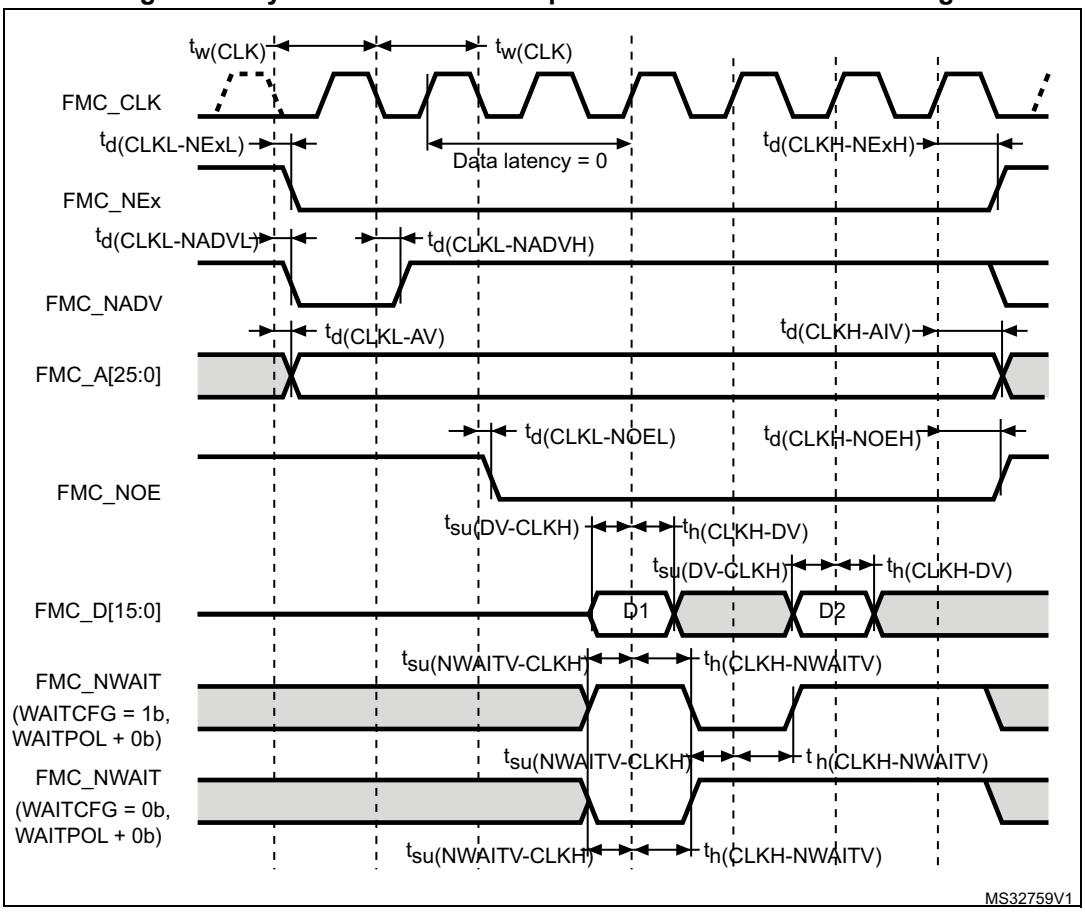


Table 172. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck}-1$	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$2T_{fmc_ker_ck}+0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$2T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$2T_{fmc_ker_ck}-0.5$	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	0	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	

1. Guaranteed by characterization results.

Figure 82. Synchronous non-multiplexed PSRAM write timings

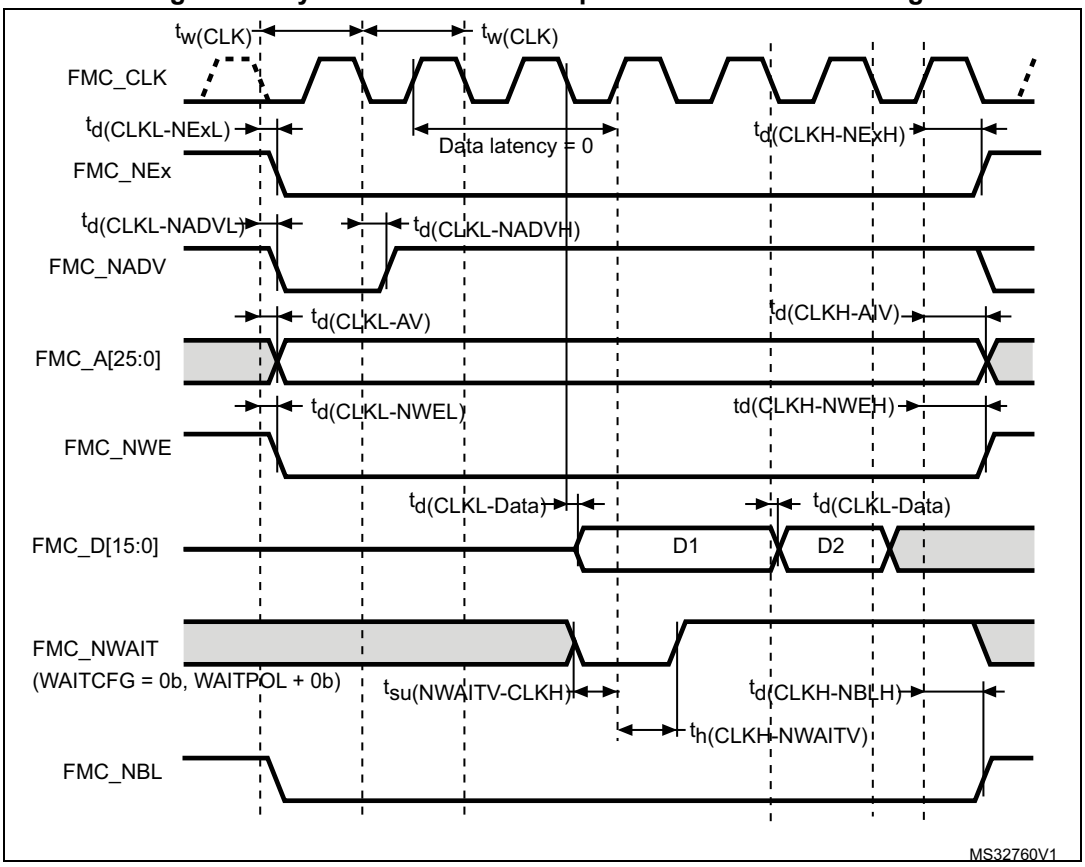


Table 173. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc_ker_ck}$**+0.5**	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	**0**	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc_ker_ck}+1$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc_ker_ck}+1$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 83 through *Figure 86* represent synchronous waveforms, and *Table 174* and *Table 175* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- Capacitive load C_L = 30 pF

In all timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

Figure 83. NAND controller waveforms for read access

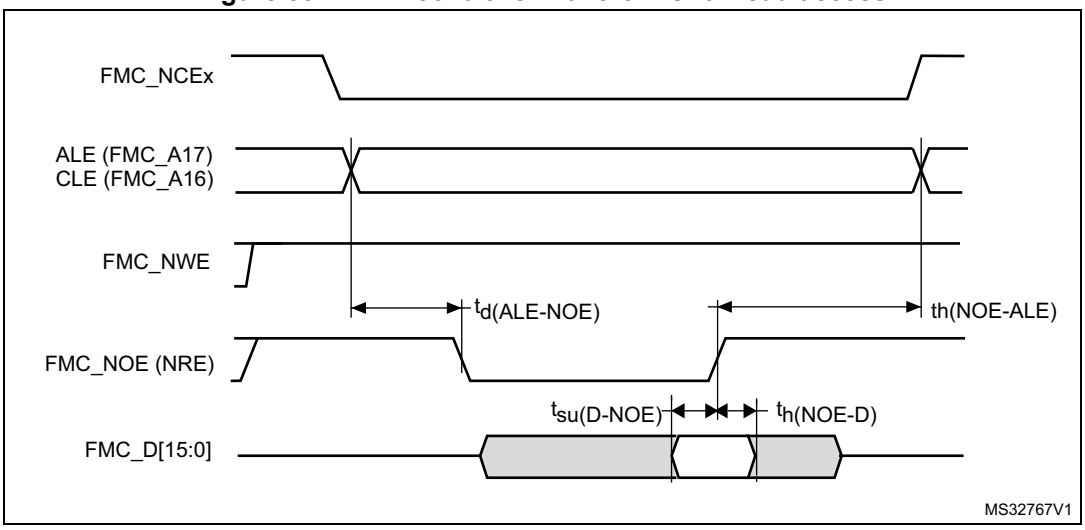


Figure 84. NAND controller waveforms for write access

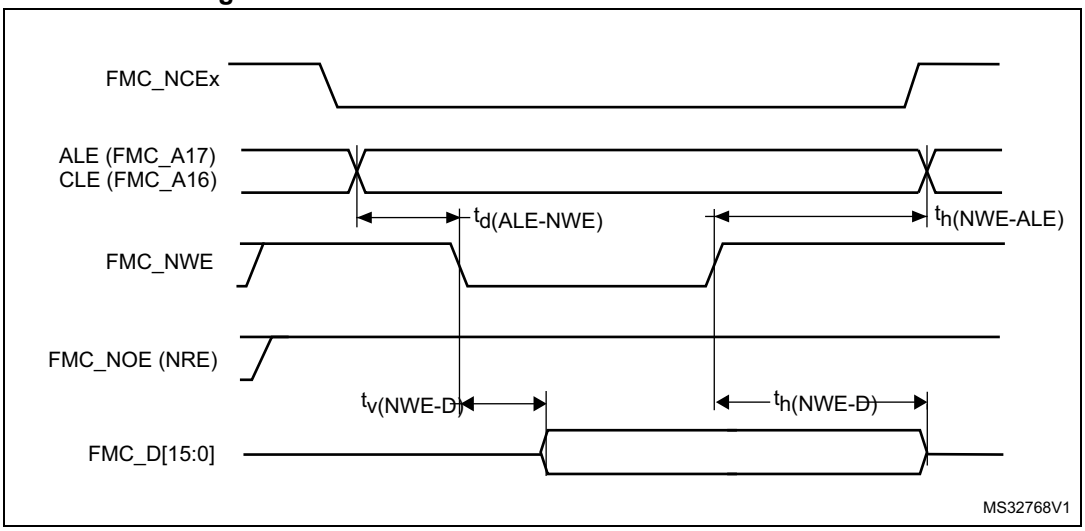


Figure 85. NAND controller waveforms for common memory read access

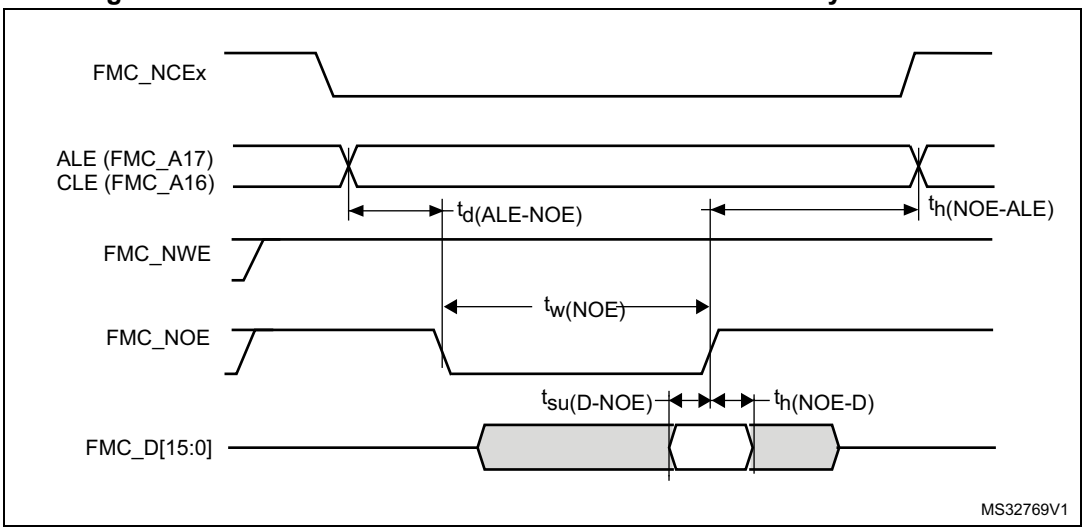


Figure 86. NAND controller waveforms for common memory write access

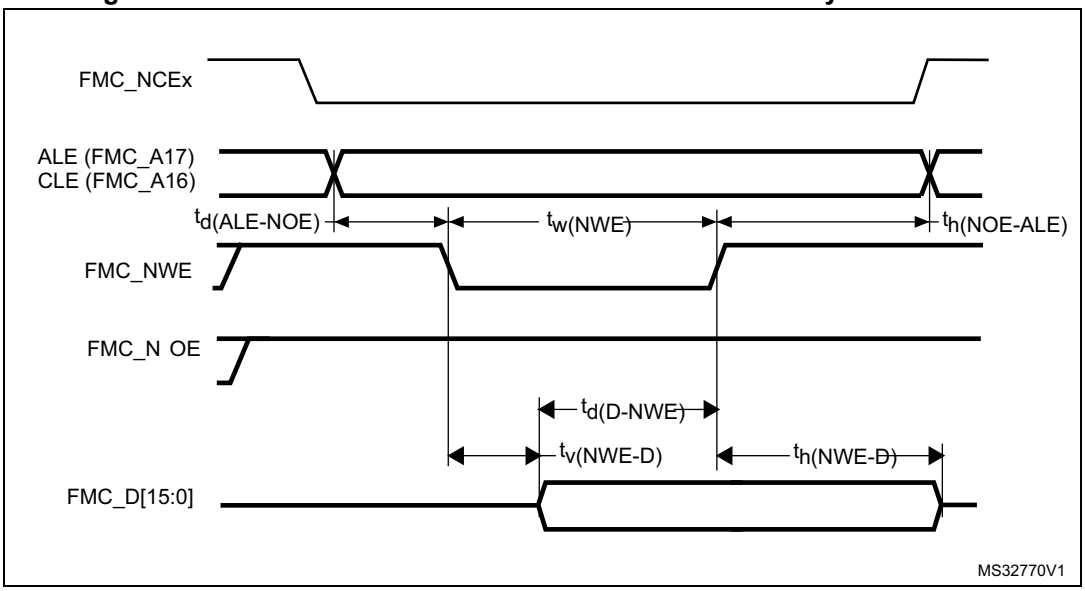


Table 174. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc_ker_ck} - 0.5$	$4T_{fmc_ker_ck}+0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	8	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc_ker_ck}$ +1	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{fmc_ker_ck}$ –2	-	

1. Guaranteed by characterization results.

Table 175. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc_ker_ck} - 0.5$	$4T_{fmc_ker_ck}$ +0.5	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc_ker_ck} - 0.5$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc_ker_ck} - 1$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc_ker_ck}$ +0.5	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc_ker_ck} - 1$	-	

1. Guaranteed by characterization results.

SDRAM waveforms and timings

In all timing tables, the TKERCK is the fmc_ker_ck clock period, with the following FMC_SDCLK maximum values:

- For 2.7 V<V_{DD}<3.6 V: FMC_SDCLK =110 MHz at 20 pF
- For 1.8 V<V_{DD}<1.9 V: FMC_SDCLK =100 MHz at 20 pF
- For 1.62 V<$_{DD}$<1.8 V, FMC_SDCLK =100 MHz at 15 pF

Figure 87. SDRAM read access waveforms (CL = 1)

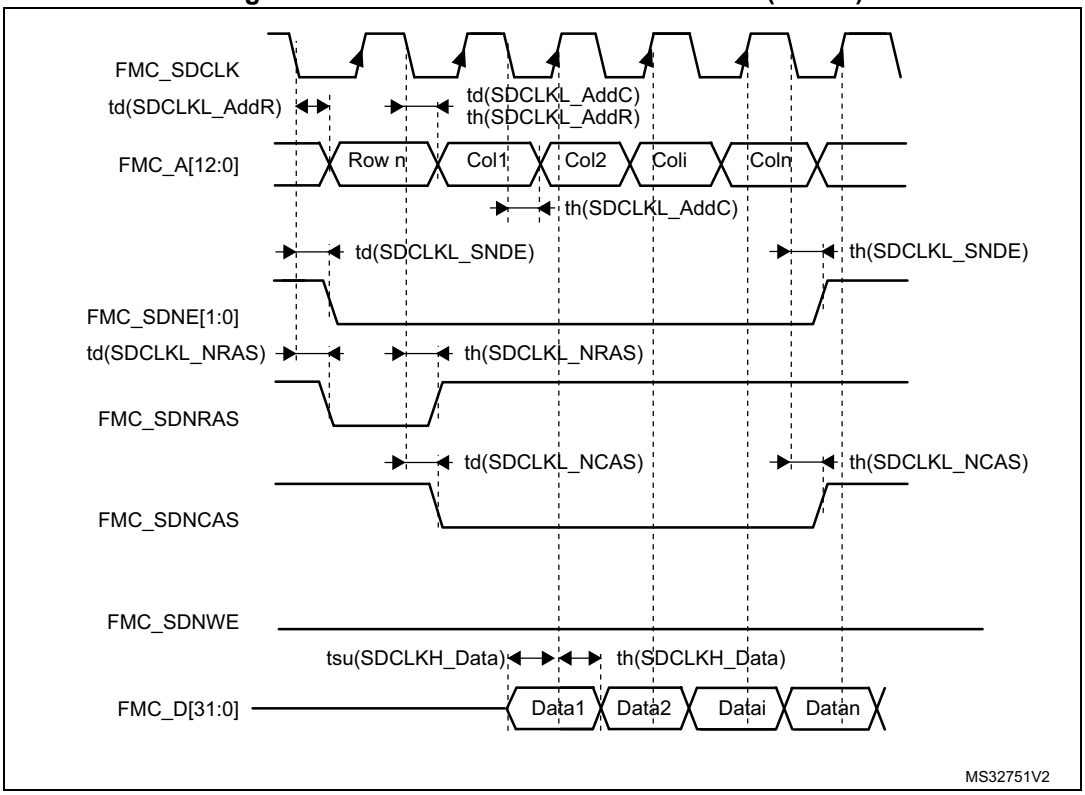


Table 176. SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck}$ +0.5	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	3	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 177. LPSDR SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck}$+0.5	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	3	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	0.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	2.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Figure 88. SDRAM write access waveforms

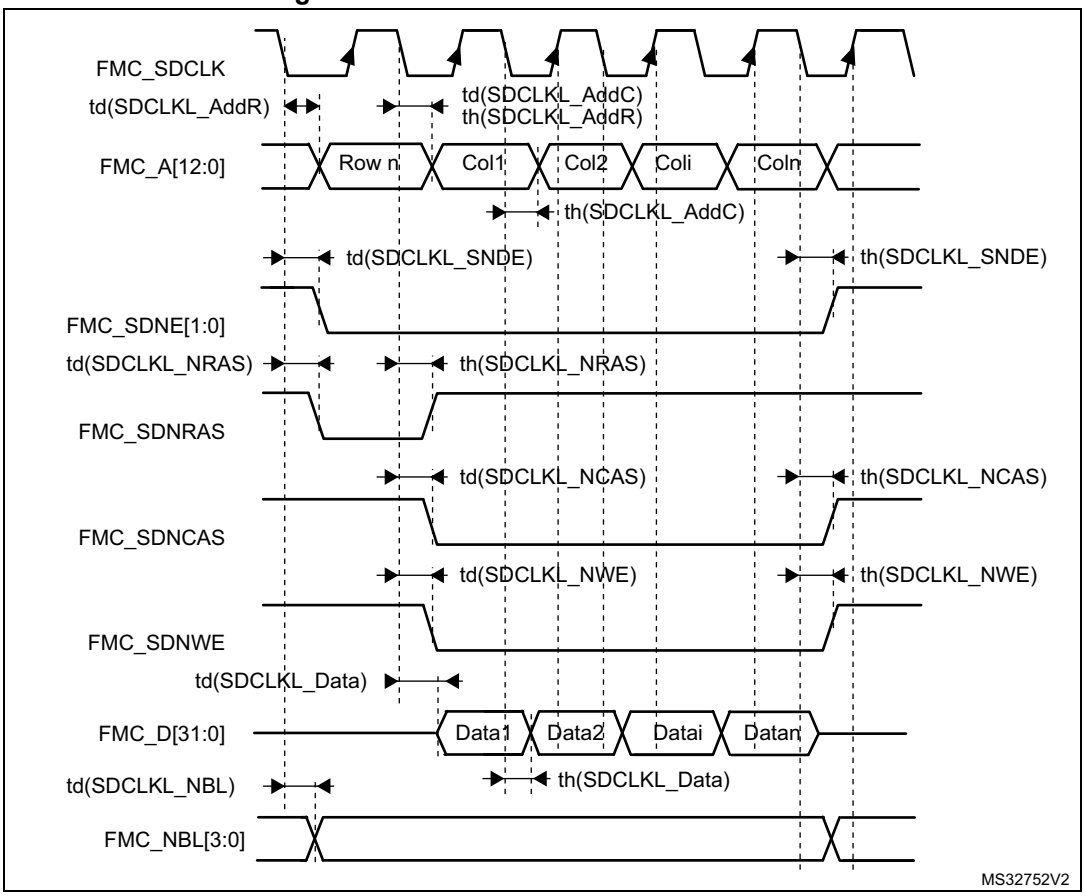


Table 178. SDRAM Write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck}+0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	1	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL_SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL_SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL-_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.

Table 179. LPSDR SDRAM Write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck}+0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	2.5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	2.5	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL- SDNE)}$	Chip select valid time	-	3	
$t_{h(SDCLKL- SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

7.3.18 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 180* and *Table 181* for QUADSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1

Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics.

The following table summarizes the parameters measured in SDR mode.

Table 180. QUADSPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1}1/T_{CK}$	QUADSPI clock frequency	2.7<V_{DD}<3.6 V CL = 20 pF	-	-	133	MHz
		1.62<V_{DD}<3.6 V CL = 15 pF	-	-	100	
$t_{w(CKH)}$	QUADSPI clock high and low time Even division	PRESCALER[7:0] = n = 0,1,3,5...	T_{CK}/2–0.5	-	T_{CK}/2	ns
$t_{w(CKL)}$			T_{CK}/2	-	T_{CK}/2+0.5	
$t_{w(CKH)}$	QUADSPI clock high and low time Odd division	PRESCALER[7:0] = n = 2,4,6,8...	(n/2)*T_{CK}/(n+1)-0.5	-	(n/2)*T_{CK}/ (n+1)	
$t_{w(CKL)}$			(n/2+1)*T_{CK}/(n+1)	-	(n/2+1)*T_{CK}/ (n+1)+0.5	
$t_{s(IN)}$	Data input setup time	2.7<V_{DD}<3.6 V	2	-	-	
		1.62<V_{DD}<3.6 V	2	-	-	
$t_{h(IN)}$	Data input hold time	2.7<V_{DD}<3.6 V	1	-	-	
		1.62<V_{DD}<3.6 V	2.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	1	2	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

1. Guaranteed by characterization results.

The following table summarizes the parameters measured in DDR mode.

Table 181. QUADSPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1}1/T_{CK}$	QUADSPI clock frequency	2.7<V_{DD}<3.6 V CL = 20 pF	-	-	100	MHz
		1.62<V_{DD}<3.6 V CL = 15 pF	-	-	100	
$t_{w(CKH)}$	QUADSPI clock high and low time Even division	PRESCALER[7:0] = n = 0,1,3,5...	T_{CK}/2–0.5	-	T_{CK}/2	ns
$t_{w(CKL)}$			T_{CK}/2	-	T_{CK}/2+0.5	
$t_{w(CKH)}$	QUADSPI clock high and low time Odd division	PRESCALER[7:0] = n = 2,4,6,8...	(n/2)*T_{CK}/ (n+1)-0.5	-	(n/2)*T_{CK}/ (n+1)	
$t_{w(CKL)}$			(n/2+1)*T_{CK}/ (n+1)	-	(n/2+1)*T_{CK} / (n+1)+0.5	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	2.7<V_{DD}<3.6 V	2.5	-	-	
		1.62<V_{DD}<3.6 V	1.5			
$t_{hr(IN)}$,$t_{hf(IN)}$	Data input hold time	2.7<V_{DD}<3.6 V	1	-	-	
		1.62<V_{DD}<3.6 V	2.5			
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	DHHC=0	-	5	6	
		DHHC=1 PRESCALER[7:0] = 1,2…	-	T_{CK}/4+1	T_{CK}/4+2	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	DHHC=0	3	-	-	
		DHHC=1 PRESCALER[7:0]=1 ,2…	T_{CK}/4	-	-	

1. Guaranteed by characterization results.

Figure 89. QUADSPI timing diagram - SDR mode

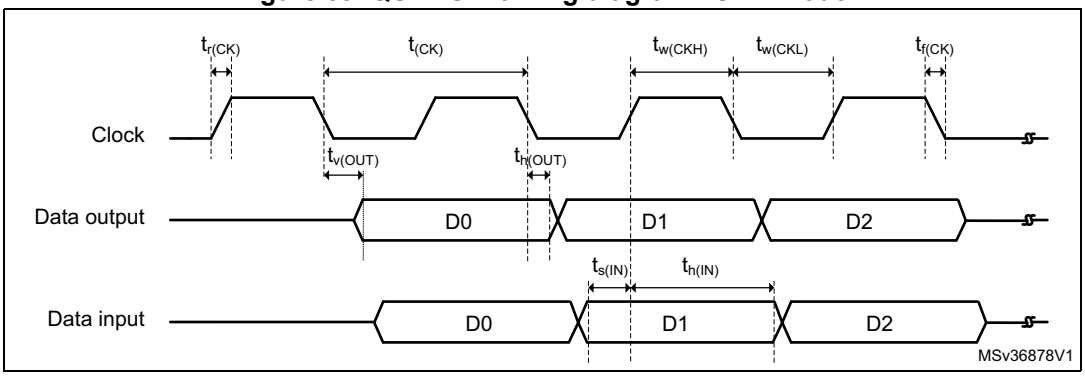
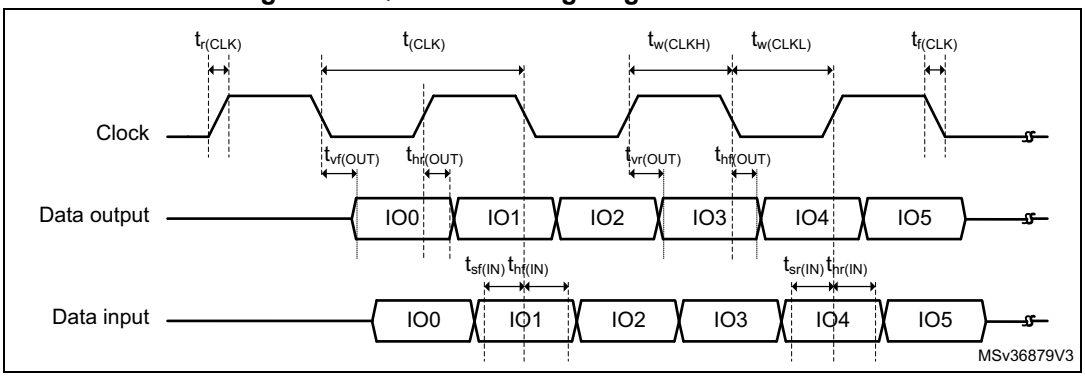


Figure 90. Quad-SPI timing diagram - DDR mode



7.3.19 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 182* for Delay Block are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and VDD supply voltage summarized in *Table 121: General operating conditions*, with the following configuration:

Table 182. Delay Block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	1400	2200	2400	ps
t_{Δ}	Unit Delay	-	35	40	45	-

7.3.20 16-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 183* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 121: General operating conditions*.

Table 183. ADC characteristics(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-		1.62	-	3.6	V
V_{REF+}	Positive reference voltage	-		1.62	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-		V_{SSA}			V
f_{ADC}	ADC clock frequency	1.62 V ≤ VDDA ≤ 3.6 V	BOOST = 11	0.12	-	50	MHz
			BOOST = 10	0.12	-	25	
			BOOST = 01	0.12	-	12.5	
			BOOST = 00	-	-	6.25	

Table 183. ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions				Min	Typ	Max	Unit
f_s(3)	Sampling rate for Direct channels(4)	Resolution = 16 bits, V_{DDA} >2.5 V	T_J = 90 °C	f_{ADC}=36 MHz	SMP = 1.5	-	-	3.60	MSps
		Resolution = 16 bits		f_{ADC}=37 MHz	SMP = 2.5	-	-	3.35	
		Resolution = 14 bits	T_J = 125 °C	f_{ADC} = 50 MHz	SMP = 2.5	-	-	5.00	
		Resolution = 12 bits		f_{ADC} = 50 MHz	SMP = 2.5	-	-	5.50	
		Resolution = 10 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	7.10	
		Resolution = 8 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	8.30	
	Sampling rate for Fast channels	Resolution = 16 bits, V_{DDA} >2.5 V	T_J = 90 °C	f_{ADC}=32 MHz	SMP = 2.5	-	-	2.90	
		Resolution = 16 bits		f_{ADC}=31 MHz	SMP = 2.5	-	-	2.80	
		Resolution = 14 bits	T_J = 125 °C	f_{ADC} = 33 MHz	SMP = 2.5	-	-	3.30	
		Resolution = 12 bits		f_{ADC} = 39 MHz	SMP = 2.5	-	-	4.30	
		Resolution = 10 bits		f_{ADC} = 48 MHz	SMP = 2.5	-	-	6.00	
		Resolution = 8 bits		f_{ADC} = 50 MHz	SMP = 2.5	-	-	7.10	
	Sampling rate for Slow channels	Resolution = 16 bits	T_J = 90 °C	f_{ADC} = 10 MHz	SMP = 1.5	-	-	1.00	
		resolution = 14 bits	T_J = 125 °C			-	-		
		resolution = 12 bits				-	-		
		resolution = 10 bits				-	-		
		resolution = 8 bits				-	-		
t_{TRIG}	External trigger period	Resolution = 16 bits				-	-	10	1/ f_{ADC}
V_{AIN}(5)	Conversion voltage range	-				0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-				V_{REF}/2 − 10%	V_{REF}/ 2	V_{REF}/2 + 10%	V
R_{AIN}(6)	External input impedance	Resolution = 16 bits, T_J = 125 °C		-	-	-	-	170	Ω
		Resolution = 14 bits, T_J = 125 °C		-	-	-	-	435	
		Resolution = 12 bits, T_J =125 °C		-	-	-	-	1150	
		Resolution = 10 bits, T_J = 125 °C		-	-	-	-	5650	
		Resolution = 8 bits, T_J = 125 °C		-	-	-	-	26500	
C_{ADC}	Internal sample and hold capacitor	-				-	4	-	pF
$t_{ADCVREG_STUP}$	ADC LDO startup time	-				-	5	10	us
t_{STAB}	ADC Power-up time	LDO already started				1	-	-	conversion cycle
t_{CAL}	Offset and linearity calibration time	-				165010	-	-	1/f_{ADC}
t_{OFF_CAL}	Offset calibration time	-				1280	-	-	1/f_{ADC}

Table 183. ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency regular and injected channels without conversion abort	CKMODE = 00			1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01			-	-	2.5	
		CKMODE = 10			-	-	2.5	
		CKMODE = 11			-	-	2.25	
$t_{LATRINJ}$	Trigger conversion latency regular injected channels aborting a regular conversion	CKMODE = 00			2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01			-	-	3.5	
		CKMODE = 10			-	-	3.5	
		CKMODE = 11			-	-	3.25	
t_S	Sampling time	-			1.5	-	810.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits			ts + 0.5 + N/2	-	-	$1/f_{ADC}$

Table 183. ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{DDA_D} (ADC)	ADC consumption on V_{DDA}, BOOST=11, Differential mode	Resolution = 16 bits, f_{ADC}=25 MHz	-	-	-	1440	-	µA
		Resolution = 14 bits, f_{ADC}=30 MHz	-	-	-	1350	-	
		Resolution = 12 bits, f_{ADC}=40 MHz	-	-	-	990	-	
	ADC consumption on V_{DDA} BOOST=10, Differential mode f_{ADC}=25 MHz	Resolution = 16 bits	-	-	-	1080	-	
		Resolution = 14 bits	-	-	-	810	-	
		Resolution = 12 bits	-	-	-	585	-	
	ADC consumption on V_{DDA} BOOST=01, Differential mode f_{ADC}=12.5 MHz	Resolution = 16 bits	-	-	-	630	-	
		Resolution = 14 bits	-	-	-	432	-	
		Resolution = 12 bits	-	-	-	315	-	
	ADC consumption on V_{DDA} BOOST=00, Differential mode f_{ADC}=6.25 MHz	Resolution = 16 bits	-	-	-	360	-	
		Resolution = 14 bits	-	-	-	270	-	
		Resolution = 12 bits	-	-	-	225	-	
I_{DDA_SE}(ADC)	ADC consumption on V_{DDA} BOOST=11, Single-ended mode	Resolution = 16 bits, f_{ADC}=25 MHz	-	-	-	720	-	
		Resolution = 14 bits, f_{ADC}=30 MHz	-	-	-	675	-	
		Resolution = 12 bits, f_{ADC}=40 MHz	-	-	-	495	-	
	ADC consumption on V_{DDA} BOOST=10, Singl-ended mode f_{ADC}=25 MHz	Resolution = 16 bits	-	-	-	540	-	
		Resolution = 14 bits	-	-	-	405	-	
		Resolution = 12 bits	-	-	-	292.5	-	
	ADC consumption on V_{DDA} BOOST=01, Single-ended mode f_{ADC}=12.5 MHz	Resolution = 16 bits	-	-	-	315	-	
		Resolution = 14 bits	-	-	-	216	-	
		Resolution = 12 bits	-	-	-	157.5	-	
	ADC consumption on V_{DDA} BOOST=00, Single-ended mode f_{ADC}=6.25 MHz	Resolution = 16 bits	-	-	-	180	-	
		Resolution = 14 bits	-	-	-	135	-	
		Resolution = 12 bits	-	-	-	112.5	-	
I_{DD} (ADC)	ADC consumption on V_{DD}	f_{ADC}=50 MHz	-	-	-	400	-	
		f_{ADC}=25 MHz	-	-	-	220	-	
		f_{ADC}=12.5 MHz	-	-	-	180	-	
		f_{ADC}=6.25 MHz	-	-	-	120	-	
		f_{ADC}=3.125 MHz	-	-	-	80	-	

1. Guaranteed by design.
2. The voltage booster on ADC switches must be used for VDDA < 2.4 V (embedded I/O switches).
3. These values are valid for UFBGA169 and one ADC. Refer to *Getting started with the STM32H7 Series MCU 16-bit ADC (*AN5354) for values of other packages and multiple ADCs operation.
4. Direct channels are connected to analog I/Os (PA0_C, PA1_C, PC2_C and PC3_C) to optimize ADC performance.
5. Depending on the package, V_{REF+} can be internally connected to V_{DDA} and V_{REF-} to V_{SSA}.
6. The tolerance is 10 LSBs for 16-bit resolution, 4 LSBs for 14-bit resolution, and 2 LSBs for 12-bit, 10-bit and 8-bit resolutions.

Table 184. Minimum sampling time vs R_{AIN} (1)(2)

Resolution	RAIN (Ω)	Minimum sampling time (s)		
		Direct channels(3)	Fast channels(4)	Slow channels(5)
16 bits	47	7.37E-08	1.14E-07	1.72E-07
14 bits	47	6.29E-08	9.74E-08	1.55E-07
	68	6.84E-08	1.02E-07	1.58E-07
	100	7.80E-08	1.12E-07	1.62E-07
	150	9.86E-08	1.32E-07	1.80E-07
	220	1.32E-07	1.61E-07	2.01E-07
12 bits	47	5.32E-08	8.00E-08	1.29E-07
	68	5.74E-08	8.50E-08	1.32E-07
	100	6.58E-08	9.31E-08	1.40E-07
	150	8.37E-08	1.10E-07	1.51E-07
	220	1.11E-07	1.34E-07	1.73E-07
	330	1.56E-07	1.78E-07	2.14E-07
	470	2.16E-07	2.39E-07	2.68E-07
	680	3.01E-07	3.29E-07	3.54E-07
10 bits	47	4.34E-08	6.51E-08	1.08E-07
	68	4.68E-08	6.89E-08	1.11E-07
	100	5.35E-08	7.55E-08	1.16E-07
	150	6.68E-08	8.77E-08	1.26E-07
	220	8.80E-08	1.08E-07	1.40E-07
	330	1.24E-07	1.43E-07	1.71E-07
	470	1.69E-07	1.89E-07	2.13E-07
	680	2.38E-07	2.60E-07	2.80E-07
	1000	3.45E-07	3.66E-07	3.84E-07
	1500	5.15E-07	5.35E-07	5.48E-07
	2200	7.42E-07	7.75E-07	7.78E-07
	3300	1.10E-06	1.14E-06	1.14E-06

Table 184. Minimum sampling time vs R_{AIN} (1)(2) (continued)

Resolution	RAIN (Ω)	Minimum sampling time (s)		
		Direct channels(3)	Fast channels(4)	Slow channels(5)
8 bits	47	3.32E-08	5.10E-08	8.61E-08
	68	3.59E-08	5.35E-08	8.83E-08
	100	4.10E-08	5.83E-08	9.22E-08
	150	5.06E-08	6.76E-08	9.95E-08
	220	6.61E-08	8.22E-08	1.11E-07
	330	9.17E-08	1.08E-07	1.32E-07
	470	1.24E-07	1.40E-07	1.63E-07
	680	1.74E-07	1.91E-07	2.12E-07
	1000	2.53E-07	2.70E-07	2.85E-07
	1500	3.73E-07	3.93E-07	4.05E-07
	2200	5.39E-07	5.67E-07	5.75E-07
	3300	8.02E-07	8.36E-07	8.38E-07
	4700	1.13E-06	1.18E-06	1.18E-06
	6800	1.62E-06	1.69E-06	1.68E-06
	10000	2.36E-06	2.47E-06	2.45E-06
	15000	3.50E-06	3.69E-06	3.65E-06

1. Guaranteed by design.
2. Data valid at up to 125 °C, with a 47 pF PCB capacitor, and V_{DDA}=1.6 V.
3. Direct channels are connected to analog I/Os (PA0_C, PA1_C, PC2_C and PC3_C) to optimize ADC performance.
4. Fast channels correspond to PF3, PF5, PF7, PF9, PA6, PC4, PB1, PF11 and PF13.
5. Slow channels correspond to all ADC inputs except for the Direct and Fast channels.

Table 185. ADC accuracy(1)(2)

Symbol	Parameter	Conditions(3)		Min	Typ	Max	Unit
ET	Total undadjusted error	Direct channel	Single ended	-	+10/–20	-	LSB
			Differential	-	±15	-	
		Fast channel	Single ended	-	+10/–20	-	
			Differential	-	±15	-	
		Slow channel	Single ended	-	±10	-	
			Differential		±10	-	
EO	Offset error	-		-	±10	-	
EG	Gain error	-		-	±15	-	
ED	Differential linearity error	Single ended		-	+3/–1	-	
		Differential		-	+4.5/–1	-	
EL	Integral linearity error	Direct channel	Single ended	-	±11	-	
			Differential	-	±7	-	
		Fast channel	Single ended	-	±13	-	
			Differential	-	±7	-	
		Slow channel	Single ended	-	±10	-	
			Differential	-	±6	-	
ENOB	Effective number of bits	Single ended		-	12.2	-	Bits
		Differential		-	13.2	-	
SINAD	Signal-to-noise and distortion ratio	Single ended		-	75.2	-	dB
		Differential		-	81.2	-	
SNR	Signal-to-noise ratio	Single ended		-	77.0	-	
		Differential		-	81.0	-	
THD	Total harmonic distortion	Single ended		-	87	-	
		Differential		-	90	-	

1. Data guaranteed by characterization for BGA packages. The values for LQFP packages might differ.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC clock frequency = 25 MHz, ADC resolution = 16 bits, V_{DDA}=V_{REF+}=3.3 V and BOOST=11.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 7.3.14* does not affect the ADC accuracy.

Figure 91. ADC accuracy characteristics

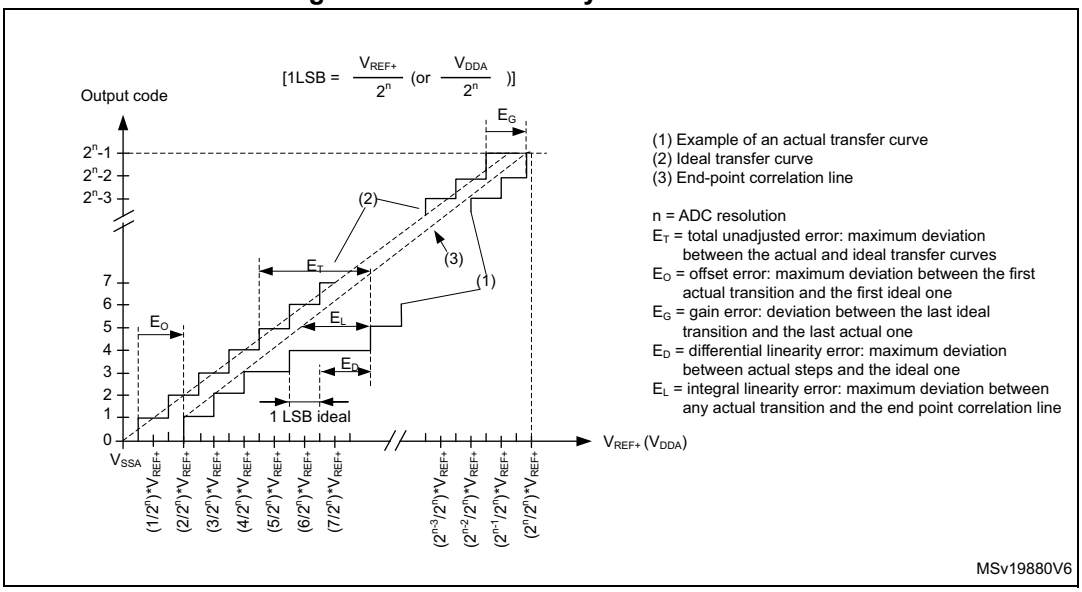
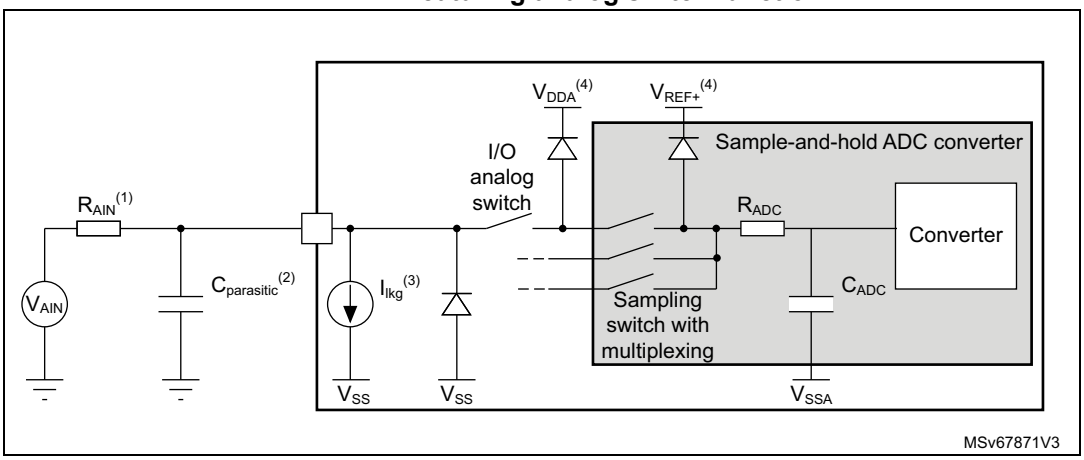


Figure 92. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function

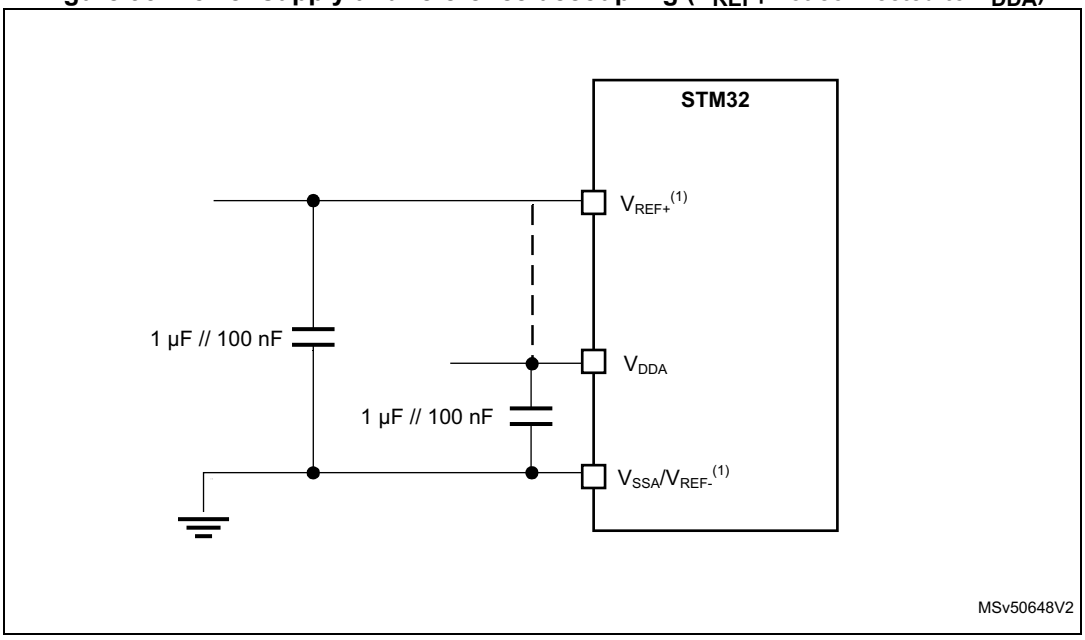


1. Refer to *Section 7.3.20: 16-bit ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 156: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 156: I/O static characteristics* for the value of I_{lkg}.
4. Refer to *Figure 67: Power supply scheme*.

General PCB design guidelines

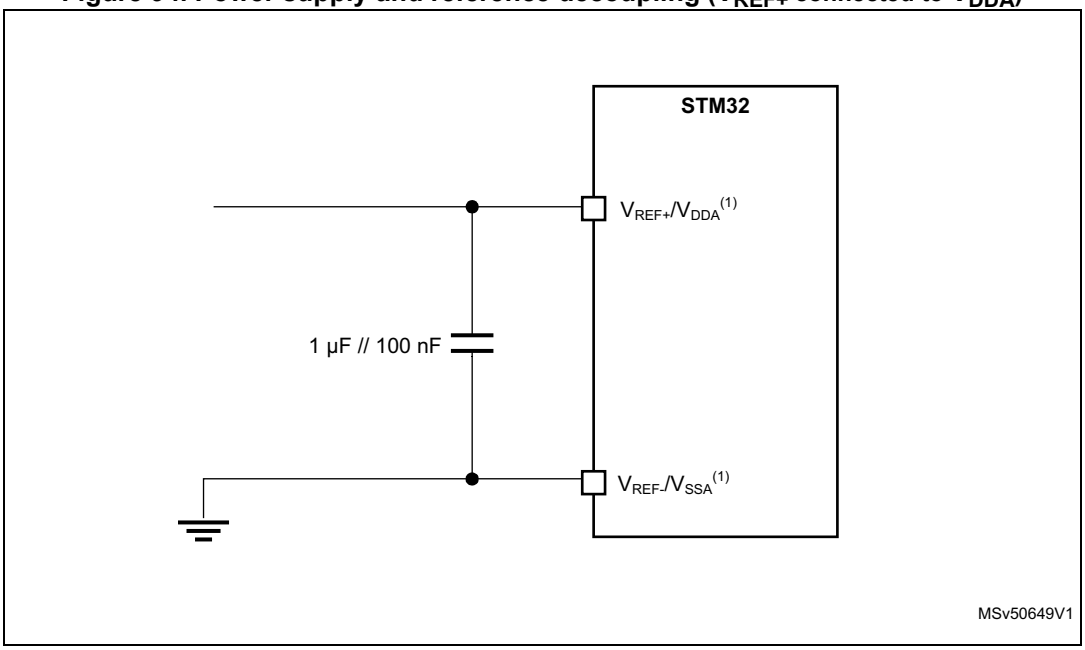
Power supply decoupling should be performed as shown in *Figure 93* or *Figure 94*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 93. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is available on all package whereas the V_{REF-} s available only on UFBGA176+25 and TFBGA240+25. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

Figure 94. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is available on all package whereas the V_{REF-} s available only on UFBGA176+25 and TFBGA240+25. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

7.3.21 DAC characteristics

Table 186. DAC characteristics(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	3.3	3.6	V
V_{REF+}	Positive reference voltage	-		1.80	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	
R_L	Resistive Load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		10.3	13	16	
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	kΩ
			V_{DD} = 2.0 V	-	-	2.6	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	kΩ
			V_{DD} = 2.0 V	-	-	18.7	
C_L	Capacitive Load	DAC output buffer OFF		-	-	50	pF
C_{SH}		Sample and Hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} −0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	±0.5 LSB	-	2.05	-	µs
			±1 LSB	-	1.97	-	
			±2 LSB	-	1.67	-	
			±4 LSB	-	1.66	-	
			±8 LSB	-	1.65	-	
		Normal mode, DAC output buffer OFF, ±1LSB C_L=10 pF		-	1.7	2	
t_{WAKEUP}(3)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until the final value of ±1LSB is reached	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L = 5$ kΩ		-	5	7.5	µs
		Normal mode, DAC output buffer OFF, $C_L \leq 10$ pF			2	5	
PSRR	DC V_{DDA} supply rejection ratio	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L = 5$ kΩ		-	−80	−28	dB

Table 186. DAC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{SAMP}	Sampling time in Sample and Hold mode C_L=100 nF (code transition between the lowest input code and the highest input code when DAC_OUT reaches the ±1LSB final value)	MODE<2:0>_V12=100/101 (BUFFER ON)		-	0.7	2.6	ms
		MODE<2:0>_V12=110 (BUFFER OFF)		-	11.5	18.7	
		MODE<2:0>_V12=111 (INTERNAL BUFFER OFF)		-	0.3	0.6	µs
C_{lint}	Internal sample and hold capacitor	-		1.8	2.2	2.6	pF
t_{TRIM}	Middle code offset trim time	Minimum time to verify the each code		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	850	-	µV
		V_{REF+} = 1.8 V		-	425	-	
$I_{DDA(DAC)}$	DAC quiescent consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	360	-	µA
			No load, worst code (0xF1C)	-	490	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	20	-	
		Sample and Hold mode, C_{SH}=100 nF		-	$360*T_{ON}/(T_{ON}+T_{OFF})$ (4)	-	
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	170	-	
			No load, worst code (0xF1C)	-	170	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	160	-	
		Sample and Hold mode, Buffer ON, C_{SH}=100 nF (worst code)		-	$170*T_{ON}/(T_{ON}+T_{OFF})$ (4)	-	
		Sample and Hold mode, Buffer OFF, C_{SH}=100 nF (worst code)		-	$160*T_{ON}/(T_{ON}+T_{OFF})$ (4)	-	

1. Guaranteed by design unless otherwise specified.

2. TBD stands for “to be defined”.
3. In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).
4. T_{ON} is the refresh phase duration, while T_{OFF} is the hold phase duration. Refer to the product reference manual for more details.

Table 187. DAC accuracy(1)

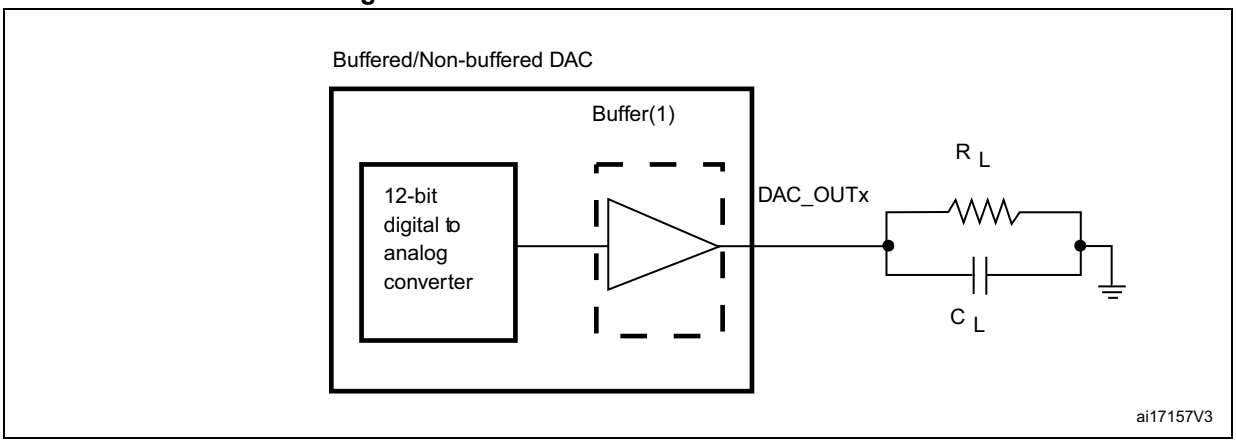
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity(2)	DAC output buffer ON		−2	-	2	LSB
		DAC output buffer OFF		−2	-	2	
-	Monotonicity	10 bits		-	-	-	-
INL	Integral non linearity(3)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		−4	-	4	LSB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		−4	-	4	
Offset	Offset error at code 0x800 (3)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	$V_{REF+} = 3.6$ V	-	-	±15	LSB
			$V_{REF+} = 1.8$ V	-	-	±30	
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±5	LSB
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	$V_{REF+} = 3.6$ V	-	-	±6	LSB
			$V_{REF+} = 1.8$ V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON,$C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	-	±1	%
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±1	
SNR	Signal-to-noise ratio(6)	DAC output buffer ON,$C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 kHz, BW = 500 KHz		-	67.8	-	dB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L,1 kHz, BW = 500 KHz		-	67.8	-	
THD	Total harmonic distortion(6)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 kHz		-	−78.6	-	dB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L, 1 kHz		-	−78.6	-	
SINAD	Signal-to-noise and distortion ratio(6)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 kHz		-	67.5	-	dB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L, 1 kHz		-	67.5	-	

Table 187. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz	-	10.9	-	bits
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L, 1 kHz	-	10.9	-	

1. Guaranteed by characterization.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2 V) when the buffer is ON.
6. Signal is −0.5dBFS with $F_{sampling}$=1 MHz.

Figure 95. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

7.3.22 Voltage reference buffer characteristics

Table 188. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	VSCALE = 000	2.8	3.3	3.6	V
			VSCALE = 001	2.4	-	3.6	
			VSCALE = 010	2.1	-	3.6	
			VSCALE = 011	1.8	-	3.6	
		Degraded mode	VSCALE = 000	1.62	-	2.80	
			VSCALE = 001	1.62	-	2.40	
			VSCALE = 010	1.62	-	2.10	
			VSCALE = 011	1.62	-	1.80	
V_{REFBUF_OUT}	Voltage Reference Buffer Output, at 30 °C, I_{load}= 100 µA	Normal mode	VSCALE = 000	2.498	2.5	2.5035	
			VSCALE = 001	2.046	2.049	2.052	
			VSCALE = 010	1.801	1.804	1.806	
			VSCALE = 011	1.4995	1.5015	1.504	
		Degraded mode(2)	VSCALE = 000	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 001	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 010	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 011	V_{DDA}– 150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
C_L	Load capacitor	-	-	0.5	1	1.50	uF
esr	Equivalent Serial Resistor of C_L	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal Mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	−40 °C < T_J < +125 °C		-	-	T_{coeff} V_{REFINT} + 100	ppm/ °C
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100KHz	-	-	40	-	

Table 188. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{START}	Start-up time	C_L=0.5 µF	-	-	300	-	µs
		C_L=1 µF	-	-	500	-	
		C_L=1.5 µF	-	-	650	-	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(3)	-		-	8	-	mA
$I_{DDA(VREFBUF)}$	VREFBUF consumption from V_{DDA}	I_{LOAD} = 0 µA	-	-	15	25	µA
		I_{LOAD} = 500 µA	-	-	16	30	
		I_{LOAD} = 4 mA	-	-	32	50	

1. Guaranteed by design.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}−drop voltage).
3. To properly control VREFBUF I_{INRUSH} current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 1.8 V-3.6 V, 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VSCALE = 011, 010, 001 and 000, respectively.

7.3.23 Temperature sensor characteristics

Table 189. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	-	±3	°C
Avg_Slope(2)	Average slope	-	2	-	mV/°C
V_{30}(3)	Voltage at 30°C ± 5 °C	-	0.62	-	V
t_{start_run}	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

1. Guaranteed by design.
2. Guaranteed by characterization.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

Table 190. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA} = 3.3 V	0x1FF1 E820 -0x1FF1 E821
TS_CAL2	Temperature sensor raw data acquired value at 130 °C, V_{DDA} = 3.3 V	0x1FF1 E840 - 0x1FF1 E841

7.3.24 Temperature and V_{BAT} monitoring

Table 191. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	26	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9	-	-	µs
$V_{BAThigh}$	High supply monitoring	-	3.55	-	V
V_{BATlow}	Low supply monitoring	-	1.36	-	

1. Guaranteed by design.

Table 192. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	KΩ
		VBRS in PWR_CR3= 1		1.5	-	

Table 193. Temperature monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	-	117	-	°C
$TEMP_{low}$	Low temperature monitoring	-	–25	-	

7.3.25 Voltage booster for analog switch

Table 194. Voltage booster for analog switch characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.62	2.6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.62 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

1. Guaranteed by characterization results.

7.3.26 Comparator characteristics

Table 195. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	3.3	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-		(2)			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	0.2	0.3	µA
		BRG_EN=1 (bridge enable)		-	0.8	1	
t_{START_SCALER}	Scaler startup time	-		-	140	250	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode		-	2	5	µs
		Medium mode		-	5	20	
		Ultra-low-power mode		-	15	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode		-	50	80	ns
		Medium mode		-	0.5	1.2	µs
		Ultra-low-power mode		-	2.5	7	
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	High-speed mode		-	50	120	ns
		Medium mode		-	0.5	1.2	µs
		Ultra-low-power mode		-	2.5	7	
V_{offset}	Comparator offset error	Full common mode range		-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		5	10	22	
		Medium hysteresis		8	20	37	
		High hysteresis		16	30	52	
$I_{DDA(COMP)}$	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	800	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 126: Embedded reference voltage*.

3. Guaranteed by characterization results.

7.3.27 Operational amplifier characteristics

Table 196. Operational amplifier characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage Range	-	2	3.3	3.6	V
CMIR	Common Mode Input Range	-	0	-	V_{DDA}	
VI_{OFFSET}	Input offset voltage	25°C, no load on output	-	-	±1.5	mV
		All voltages and temperature, no load	-	-	±2.5	
ΔVI_{OFFSET}	Input offset voltage drift	-	-	±3.0	-	µV/°C
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage ($0.1*V_{DDA}$)	-	-	1.1	1.5	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage ($0.9*V_{DDA}$)	-	-	1.1	1.5	
I_{LOAD}	Drive current	-	-	-	500	µA
I_{LOAD_PGA}	Drive current in PGA mode	-	-	-	270	
C_{LOAD}	Capacitive load	-	-	-	50	pF
CMRR	Common mode rejection ratio	-	-	80	-	dB
PSRR	Power supply rejection ratio	$C_{LOAD} \le 50pf$ / $R_{LOAD} \ge 4\ k\Omega$[1] at 1 kHz, $V_{com}=V_{DDA}/2$	50	66	-	dB
GBW	Gain bandwidth for high supply range	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV	4	7.3	12.3	MHz
SR	Slew rate (from 10% and 90% of output voltage)	Normal mode	-	3	-	V/µs
		High-speed mode	-	30	-	
AO	Open loop gain	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV	59	90	129	dB
φm	Phase margin	-	-	55	-	°
GM	Gain margin	-	-	12	-	dB
V_{OHSAT}	High saturation voltage	I_{load}=max or R_{LOAD}=min, Input at V_{DDA}	V_{DDA} −100 mV	-	-	mV
V_{OLSAT}	Low saturation voltage	I_{load}=max or R_{LOAD}=min, Input at 0 V	-	-	100	

Table 196. Operational amplifier characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WAKEUP}	Wake up time from OFF state	Normal mode	C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ, follower configuration	-	0.8	3.2	µs
		High speed mode	C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ, follower configuration	-	0.9	2.8	
PGA gain	Non inverting gain error value	PGA gain = 2		−1	-	1	%
		PGA gain = 4		−2	-	2	
		PGA gain = 8		−2.5	-	2.5	
		PGA gain = 16		−3	-	3	
	Inverting gain error value	PGA gain = 2		−1	-	1	
		PGA gain = 4		−1	-	1	
		PGA gain = 8		−2	-	2	
		PGA gain = 16		−3	-	3	
	External non-inverting gain error value	PGA gain = 2		−1	-	1	
		PGA gain = 4		−3	-	3	
		PGA gain = 8		−3.5	-	3.5	
		PGA gain = 16		−4	-	4	
$R_{network}$	R2/R1 internal resistance values in non-inverting PGA mode(2)	PGA Gain=2		-	10/10	-	kΩ/ kΩ
		PGA Gain=4		-	30/10	-	
		PGA Gain=8		-	70/10	-	
		PGA Gain=16		-	150/10	-	
	R2/R1 internal resistance values in inverting PGA mode(2)	PGA Gain = -1		-	10/10	-	
		PGA Gain = -3		-	30/10	-	
		PGA Gain = -7		-	70/10	-	
		PGA Gain = -15		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		−15	-	15	%

Table 196. Operational amplifier characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PGA BW	PGA bandwidth for different non inverting gain	Gain=2		-	GBW/2	-	MHz
		Gain=4		-	GBW/4	-	
		Gain=8		-	GBW/8	-	
		Gain=16		-	GBW/16	-	
	PGA bandwidth for different inverting gain	Gain = -1		-	5.00	-	MHz
		Gain = -3		-	3.00	-	
		Gain = -7		-	1.50	-	
		Gain = -15		-	0.80	-	
en	Voltage noise density	at 1 KHz	output loaded with 4 kΩ	-	140	-	nV/√Hz
		at 10 KHz		-	55	-	
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode, follower	-	570	1000	µA
		High-speed mode		-	610	1200	

1. R_{LOAD} is the resistive load connected to VSSA or to VDDA.
2. R2 is the internal resistance between the OPAMP output and th OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.

7.3.28 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 197* for DFSDM are derived from tests performed under the ambient temperature, fPCLKx frequency and supply voltage conditions summarized in *Table 121: General operating conditions*.

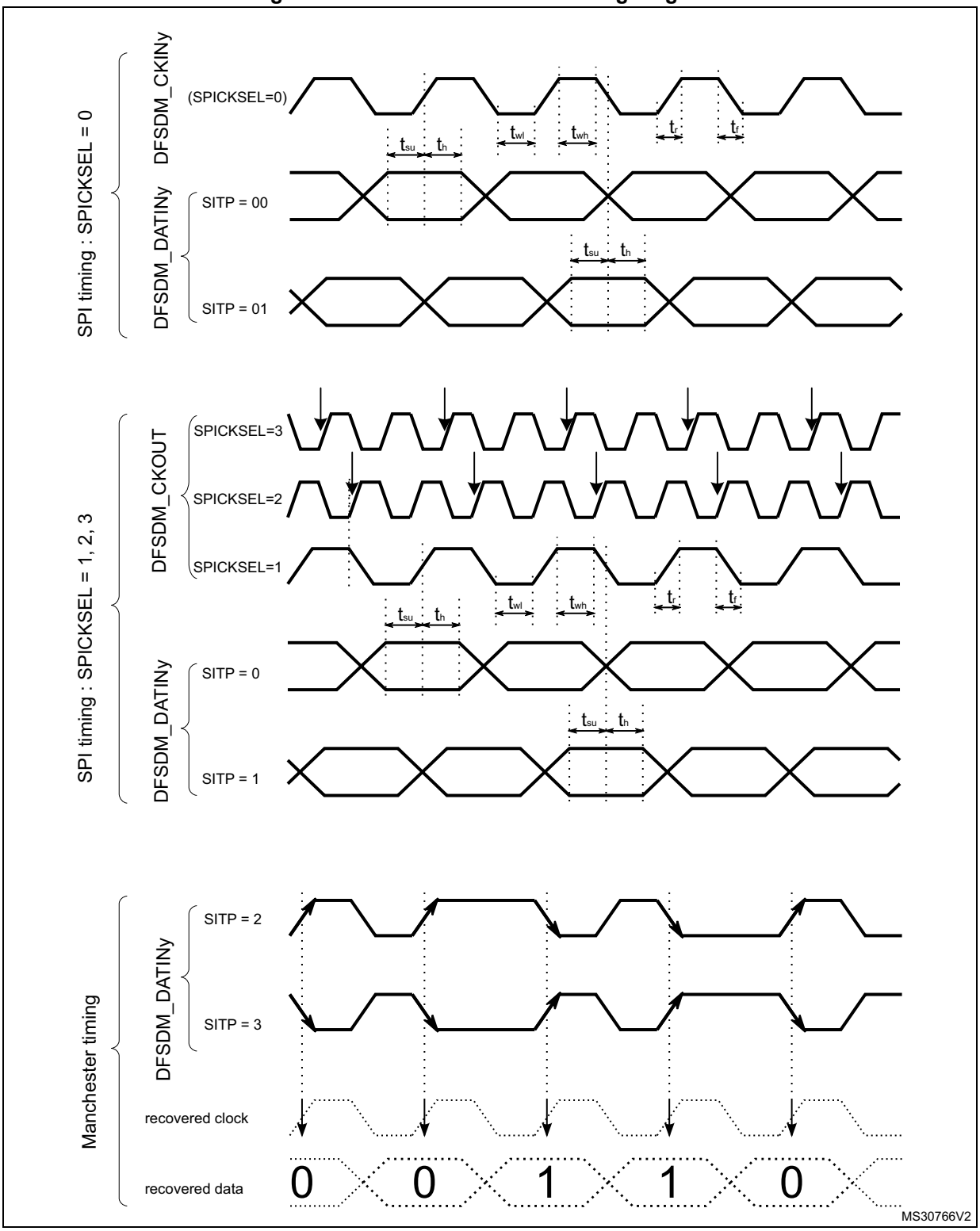
- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS1

Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (DiFSDM_CKINx, DFSDM_DATINx, DFSDM_CKOUT for DFSDM).

Table 197. DFSDM measured timing - 1.62-3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.62 < V_{DD} < 3.6 V		-	-	250	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V		-	-	20	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < V_{DD} < 3.6 V		-	-	20	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]'0), 1.62 < V_{DD} < 3.6 V		-	-	20	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]'0), 2.7 < V_{DD} < 3.6 V		-	-	20	
f_{CKOUT}	Output clock frequency	1.62 < V_{DD} < 3.6 V		-	-	20	
$DuCy_{CK\ OUT}$	Output clock frequency duty cycle	1.62 < V_{DD} < 3.6 V	Even division, CKOUTDIV[7:0] = 1, 3, 5...	45	50	55	%
			Odd division, CKOUTDIV[7:0] = 2, 4, 6...	(((n/2+1)/(n+1)) *100)–5	(((n/2+1)/(n+1)) *100)	(((n/2+1)/(n+1)) *100)+5	
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V		T_{CKIN}/2-0.5	T_{CKIN}/2	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V		1.5	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V		0.5	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]'0), 1.62 < V_{DD} < 3.6 V		(CKOUTDIV+1) * $T_{DFSDMCLK}$	-	(2*CKOUTDIV) * $T_{DFSDMCLK}$	

Figure 96. Channel transceiver timing diagrams



7.3.29 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 198* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in *Table 121: General operating conditions*, with the following configuration:

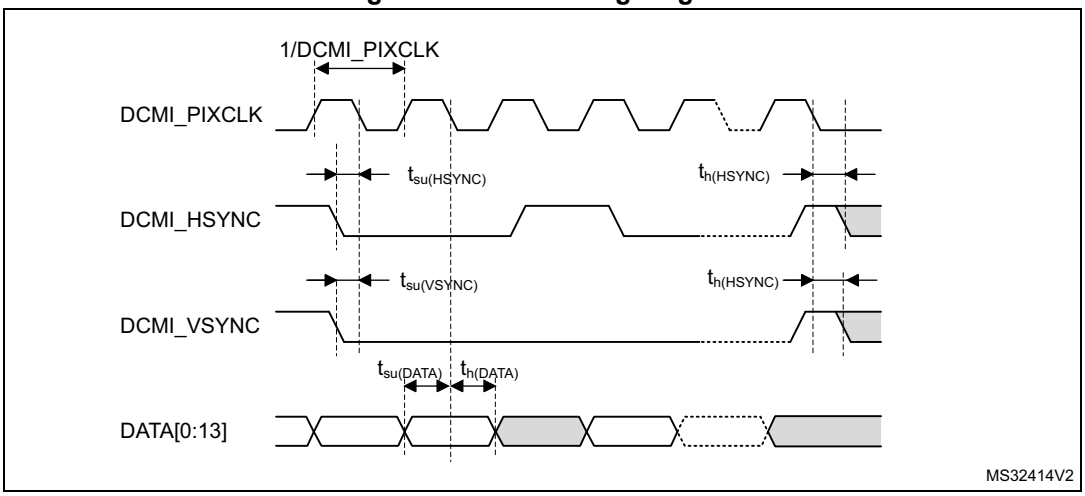
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS1

Table 198. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	-
DCMI_PIXCLK	Pixel Clock input	-	80	MHz
D_{pixel}	Pixel Clock input duty cycle	30	70	%
$t_{su(}$DATA)	Data input setup time	3	-	-
t_h(DATA)	Data hold time	1	-	
tsu(HSYNC), tsu(VSYNC)	DCMI_HSYNC/ DCMI_VSYNC input setup time	2	-	ns
th(HSYNC), th(VSYNC)	DCMI_HSYNC/ DCMI_VSYNC input hold time	1	-	-

1. Guaranteed by characterization results.

Figure 97. DCMI timing diagram



7.3.30 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 199* for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in *Table 121: General operating conditions*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: 0.5VDD
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1

Table 199. LTDC characteristics(1)

Symbol	Parameter		Min	Max	Unit
f_{CLK}	LTDC clock output frequency	2.7<V_{DD}<3.6 V 20pF	-	150	MHz
		2.7<V_{DD}<3.6 V		133	
		1.62<V_{DD}<3.6 V		90	
D_{CLK}	LTDC clock output duty cycle		45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time		$t_{w(CLK)}$//2-0.5	$t_{w(CLK)}$//2+0.5	-
$t_{v(DATA)}$	Data output valid time	2.7<V_{DD}<3.6 V	-	0.5	
$t_{h(DATA)}$		1.62<V_{DD}<3.6 V		5	
$t_{v(DATA)}$	Data output hold time		0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	2.7<V_{DD}<3.6 V	-	0.5	
		1.62<V_{DD}<3.6 V	-	5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time		0	-	

1. Guaranteed by characterization results.

Figure 98. LCD-TFT horizontal timing diagram

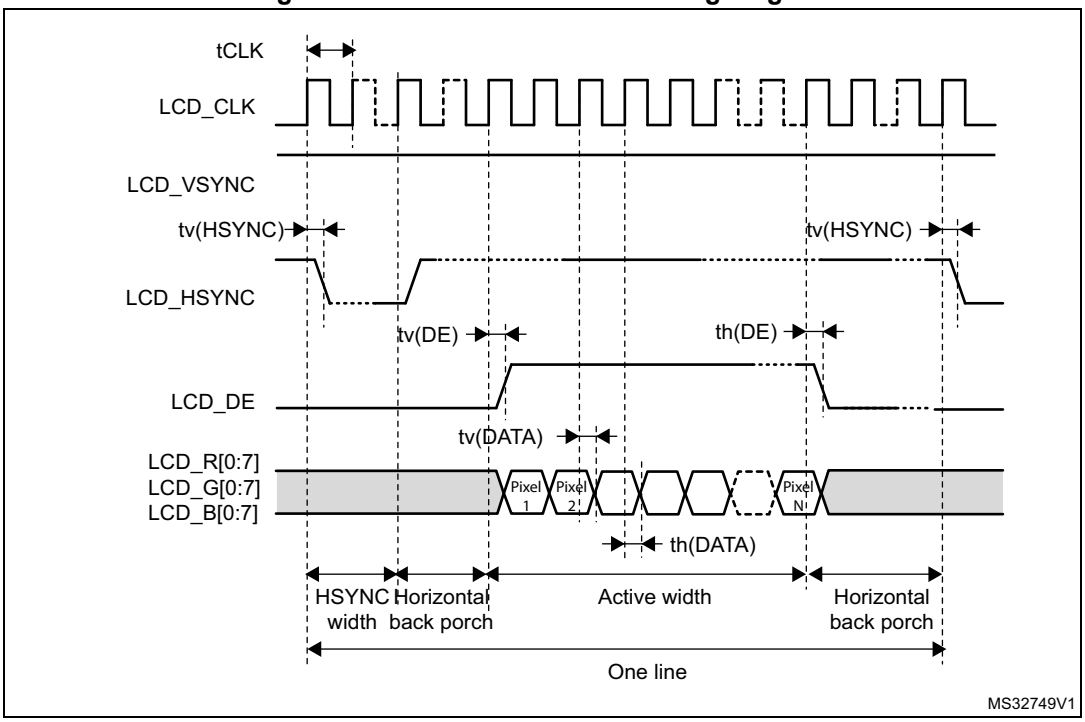
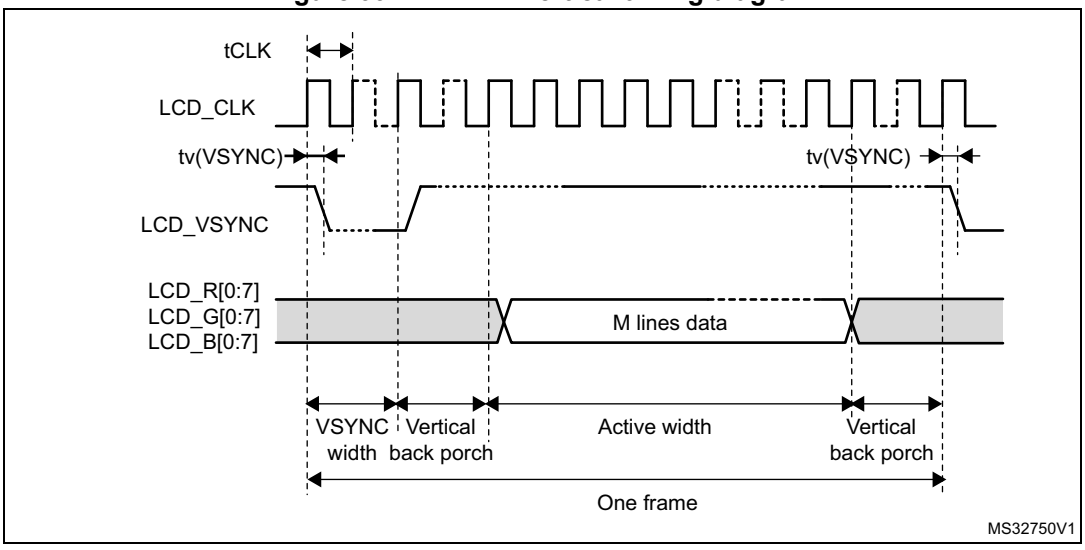


Figure 99. LCD-TFT vertical timing diagram



7.3.31 Timer characteristics

The parameters given in *Table 200* are guaranteed by design.

Refer to *Section 7.3.15: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 200. TIMx characteristics(1)(2)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 240 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 120 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 240 MHz	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 240 MHz, by setting the TIMPRE bit in the RCC_CFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = rcc_hclk1, otherwise TIMxCLK = 4x $F_{rcc_pclkx_d2}$.

7.3.32 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I2C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to RM0399 reference manual) and when the i2c_ker_ck frequency is greater than the minimum shown in the table below:

Table 201. Minimum i2c_ker_ck frequency in all I²C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog Filtre ON DNF=0	8	
			Analog Filtre OFF DNF=1	9	
		Fast-mode Plus	Analog Filtre ON DNF=0	17	
			Analog Filtre OFF DNF=1	16	-

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but still present.
- The 20 mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{Load} supported in Fm+, which is given by these formulas:

  $t_{r(SDA/SCL)}=0.8473xR_PxC_{Load}$

  $R_{P(min)}= (V_{DD}-V_{OL(max)})/I_{OL(max)}$

  Where R_P is the I2C lines pull-up. Refer to *Section 7.3.15: I/O port characteristics* for the I²C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 202. I²C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by analog filter	50(2)	80(3)	ns

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

USART interface characteristics

Unless otherwise specified, the parameters given in *Table 203* for USART are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS1

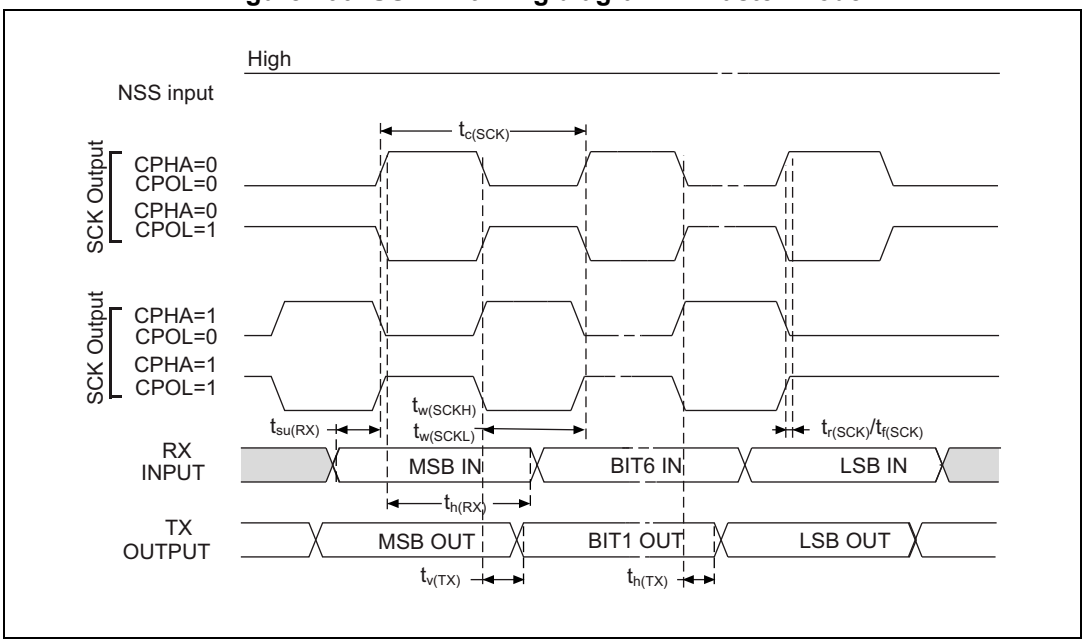
Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 203. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	12.5	MHz
		Slave mode			25	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker}+1	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	CK high and low time	Master mode	$1/f_{CK}/2-2$	$1/f_{CK}/2$	$1/f_{CK}/2+2$	
$t_{su(RX)}$	Data input setup time	Master mode	t_{ker}+6	-	-	ns
		Slave mode	1.5	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0	-	-	
		Slave mode	1.5	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode	-	12	20	
		Master mode	-	0.5	1	
$t_{h(TX)}$	Data output hold time	Slave mode	9	-	-	
		Master mode	0	-	-	

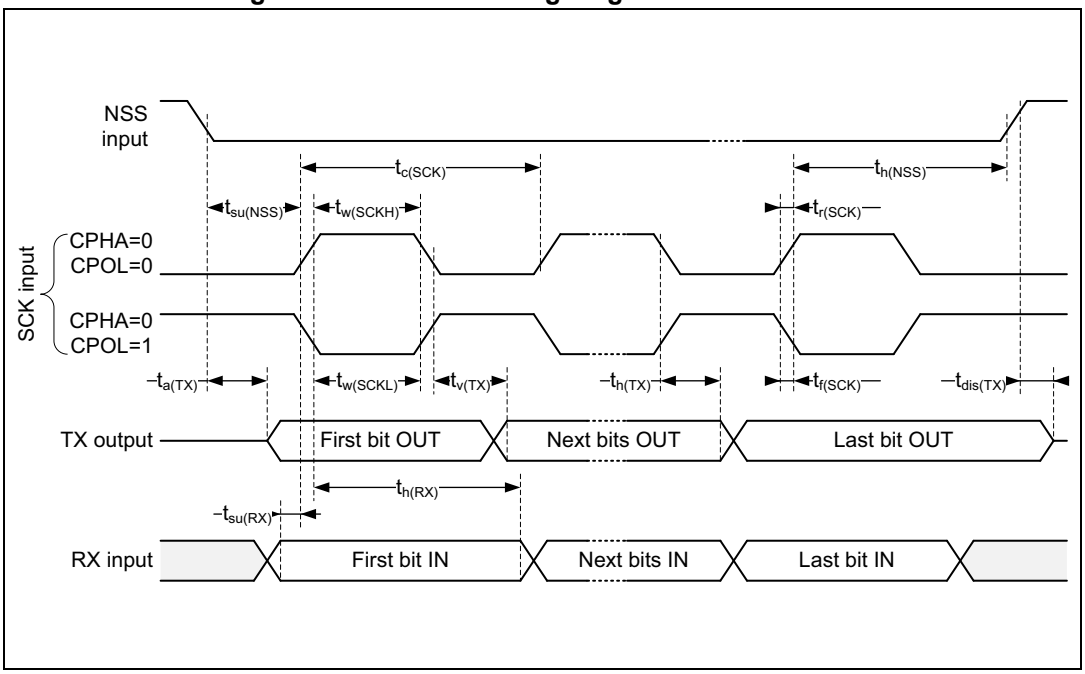
1. Guaranteed by characterization results.

Figure 100. USART timing diagram in Master mode



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 101. USART timing diagram in Slave mode



SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 204* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS1

Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 204. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode 1.62<V_{DD}<3.6 V SPI1, 2, 3	-	-	80	MHz
		Master mode 2.7<V_{DD}<3.6 V SPI1, 2, 3			100	
		Master mode 1.62<V_{DD}<3.6 V SPI4, 5, 6			50	
		Slave receiver mode 1.62<V_{DD}<3.6 V			100	
		Slave mode transmitter/full duplex 2.7<V_{DD}<3.6 V			31	
		Slave mode transmitter/full duplex 1.62 <V_{DD}<3.6 V			29	
$t_{su(NSS)}$	NSS setup time	Slave mode	2	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode	1	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PCLK}-2	T_{PCLK}	T_{PCLK}+2	
$t_{su(MI)}$	Data input setup time	Master mode	2	-	-	ns
$t_{su(SI)}$		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	3	-	-	
$t_{h(SI)}$		Slave mode	2	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	13	27	
$t_{dis(SO)}$	Data output disable time	Slave mode	0	1	5	
$t_{v(SO)}$	Data output valid time	Slave mode 2.7<V_{DD}<3.6 V	-	12.5	16	
		Slave mode 1.62<V_{DD}<3.6 V	-	12.5	17	
$t_{v(MO)}$		Master mode	-	1	3	
$t_{h(SO)}$	Data output hold time	Slave mode 1.62<V_{DD}<3.6 V	10	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.

Figure 102. SPI timing diagram - slave mode and CPHA = 0

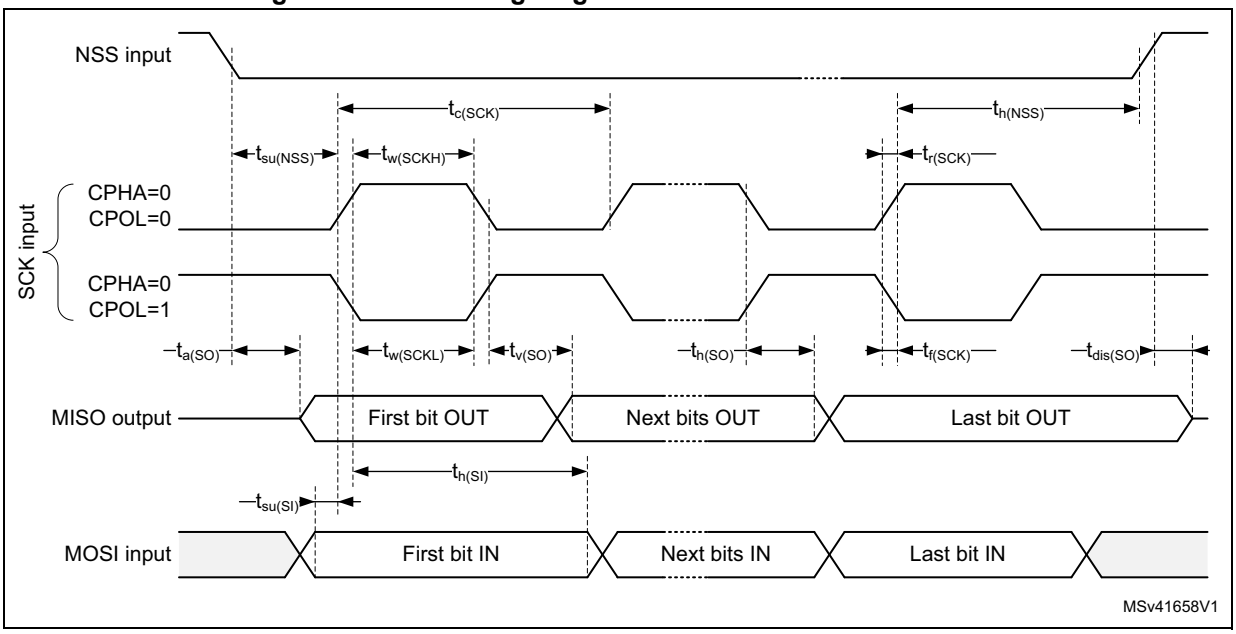
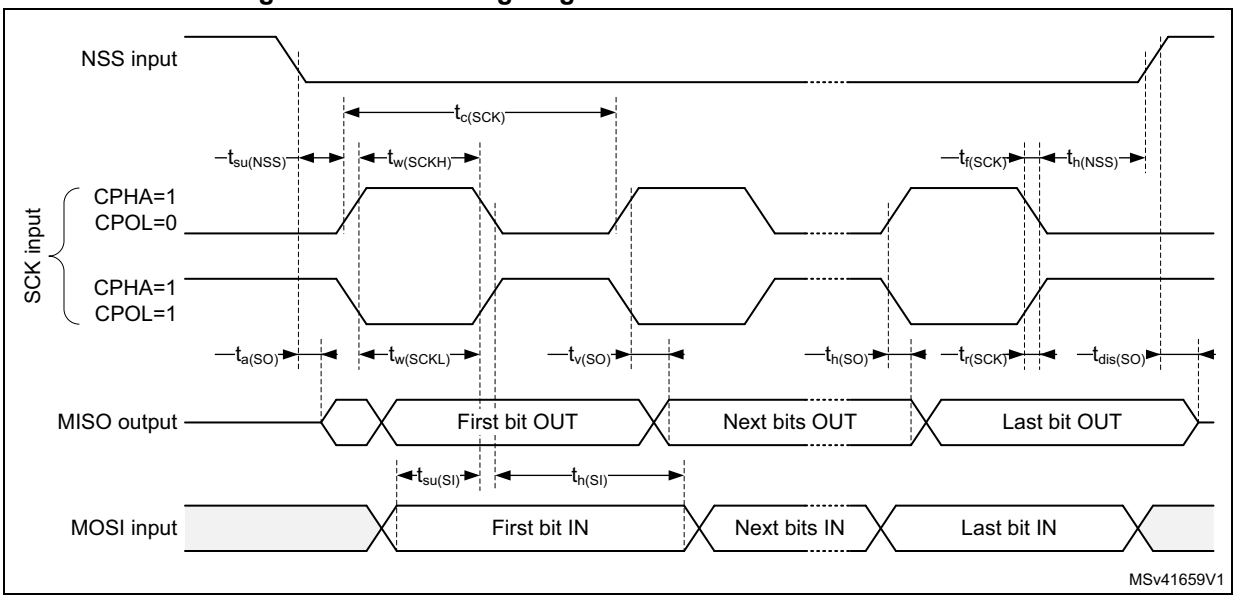
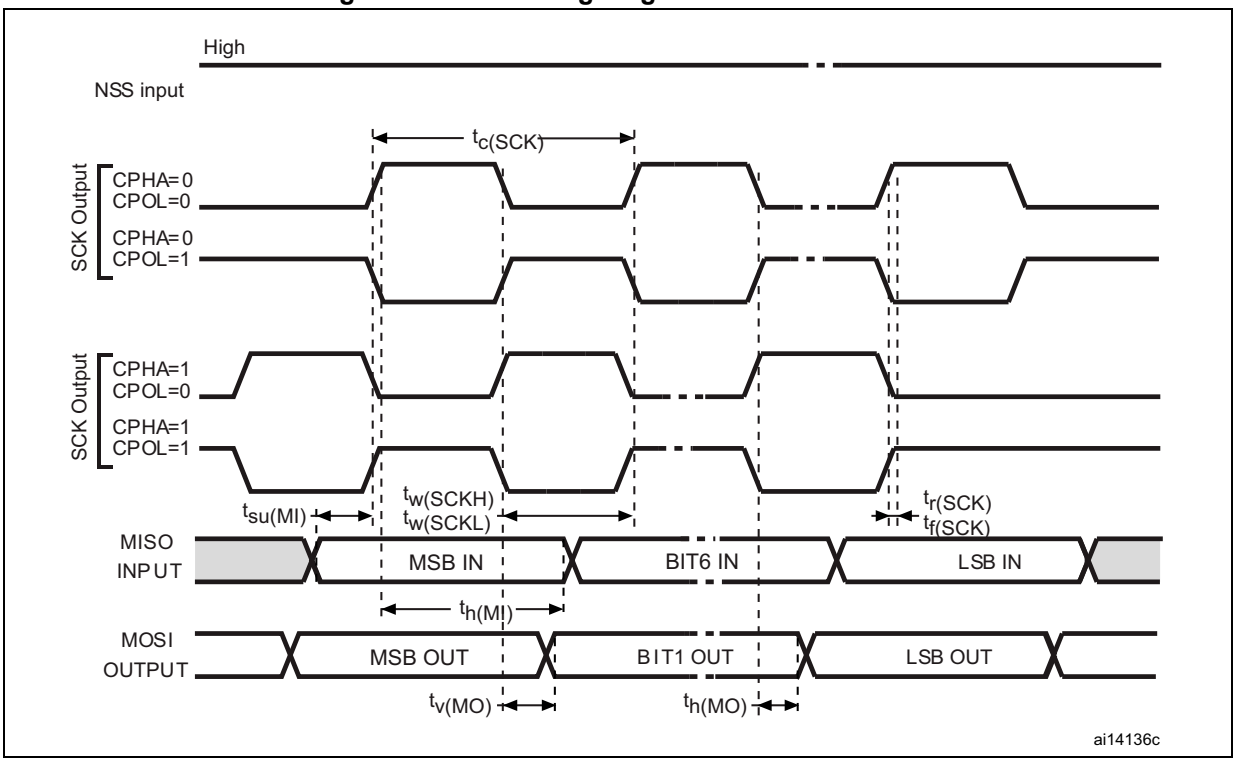


Figure 103. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 104. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

I²S Interface characteristics

Unless otherwise specified, the parameters given in *Table 205* for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS1

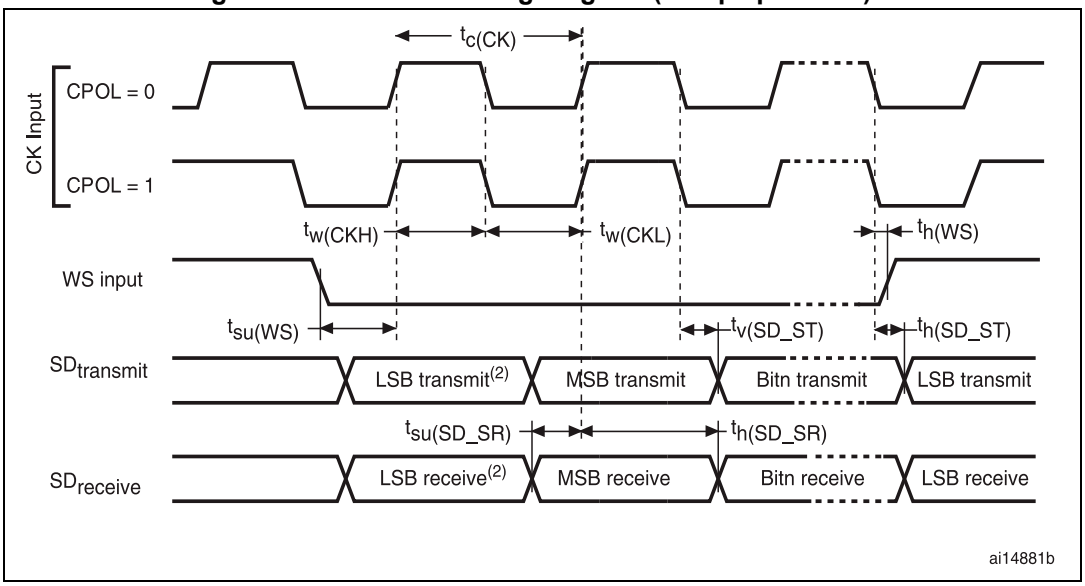
Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,WS).

Table 205. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I²S main clock output	-	256x8K	$256F_S$	MHz
f_{CK}	I²S clock frequency	Master data	-	$64F_S$	MHz
		Slave data	-	$64F_S$	
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	1	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD_SR)}$		Slave receiver	1	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	4	-	
$t_{h(SD_SR)}$		Slave receiver	2	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	17	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	

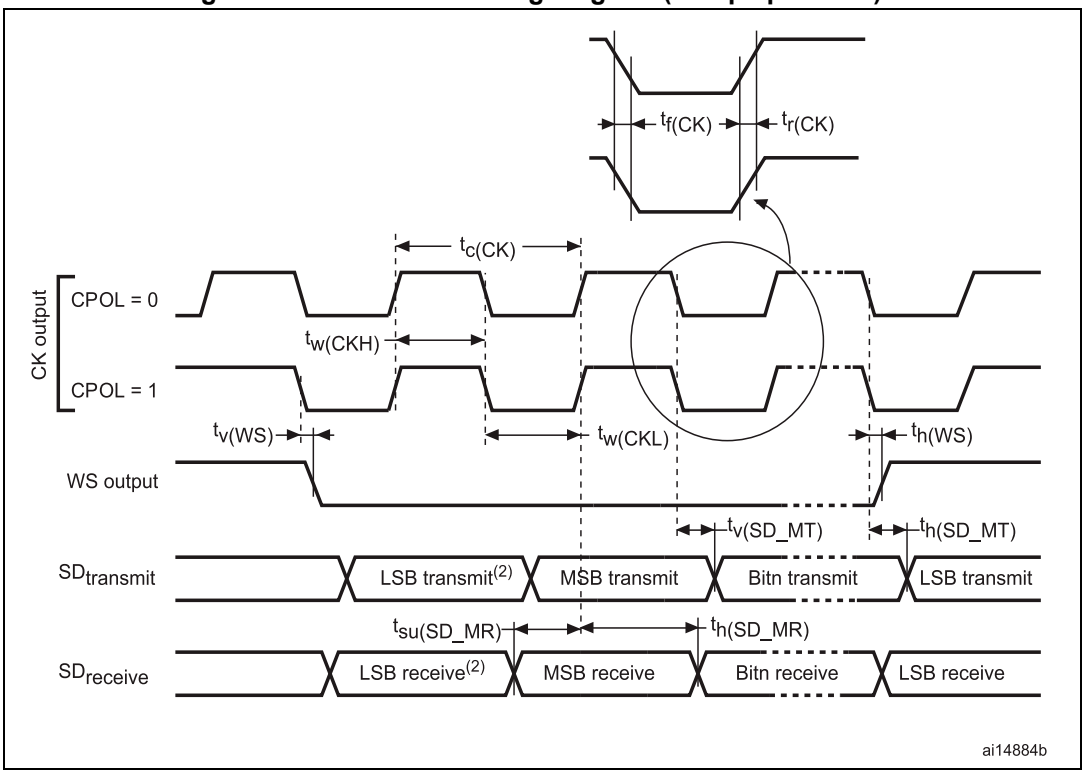
1. Guaranteed by characterization results.

Figure 105. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 106. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 206* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 121: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- IO Compensation cell activated.
- Measurement points are done at CMOS levels: 0.5VDD
- VOS level set to VOS1.

Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 206. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	256x8K	$256xF_S$	MHz
f_{CK}	SAI clock frequency(2)	Master Data: 32 bits	-	$128xF_S$(3)	
		Slave Data: 32 bits	-	$128xF_S$(3)	

Table 206. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(FS)}$	F_S valid time	Master mode $2.7 \le V_{DD} \le 3.6$	-	13	ns
		Master mode $1.62 \le V_{DD} \le 3.6$	-	20	
$t_{su(FS)}$	F_S hold time	Master mode	8	-	
$t_{h(FS)}$	F_S setup time	Slave mode	1	-	
	F_S hold time	Slave mode	1	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	0.5	-	
$t_{su(SD_B_SR)}$		Slave receiver	1	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD_B_SR)}$		Slave receiver	2	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) $2.7 \le V_{DD} \le 3.6$	-	14	
		Slave transmitter (after enable edge) $1.62 \le V_{DD} \le 3.6$	-	20	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) $2.7 \le V_{DD} \le 3.6$	-	12	
		Master transmitter (after enable edge) $1.62 \le V_{DD} \le 3.6$	-	19	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	7.5	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With F_S=192 kHz.

Figure 107. SAI master timing waveforms

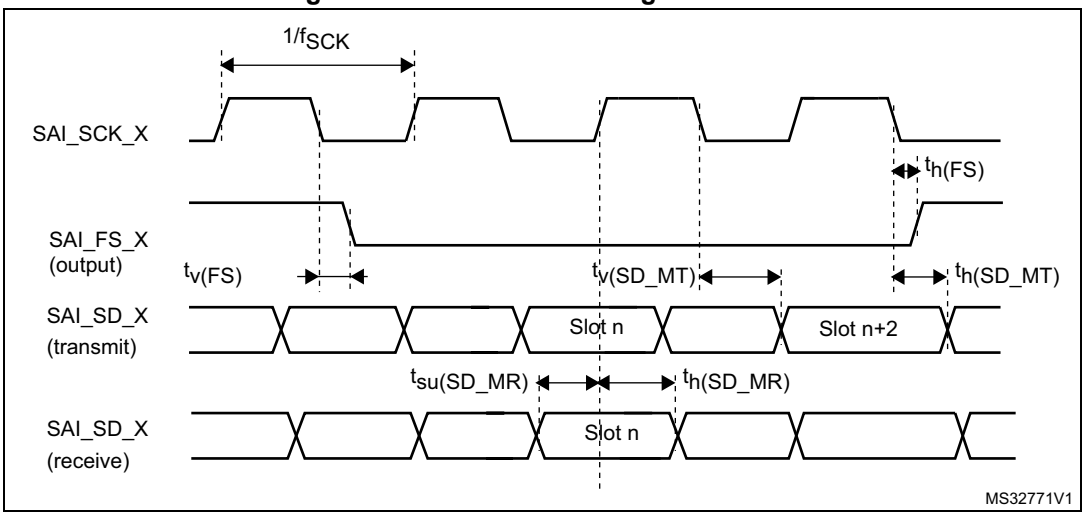
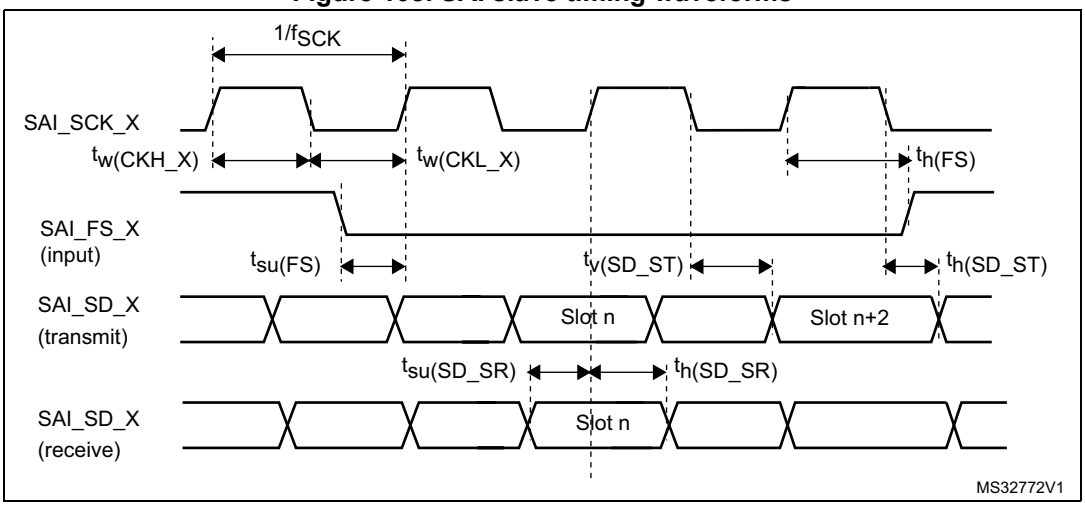


Figure 108. SAI slave timing waveforms

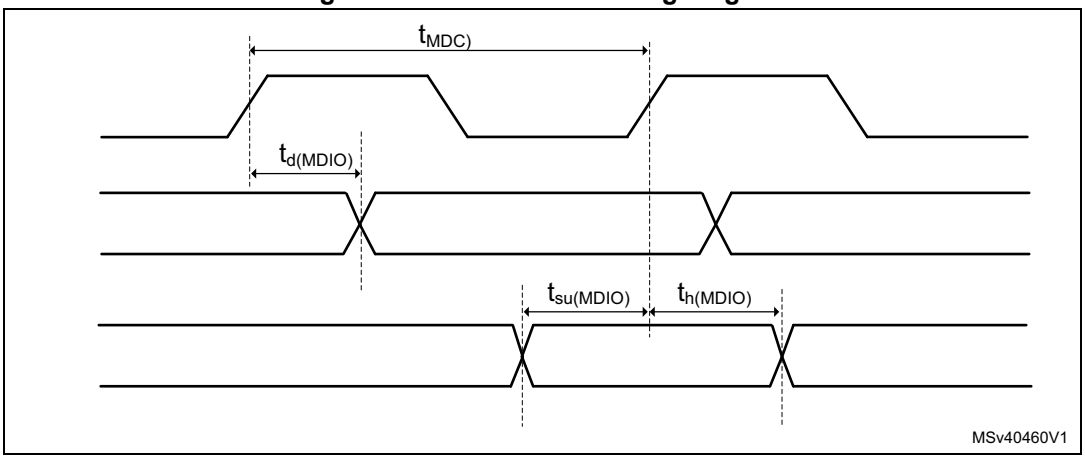


MDIO characteristics

Table 207. MDIO Slave timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
F_{MDC}	Management Data Clock	-	-	30	MHz
$t_{d(MDIO)}$	Management Data Iput/output output valid time	8	10	19	ns
$t_{su(MDIO)}$	Management Data Iput/output setup time	1	-	-	
$t_{h(MDIO)}$	Management Data Iput/output hold time	1	-	-	

Figure 109. MDIO Slave timing diagram



SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 208* and *Table 209* for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage summarized in *Table 121: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1

Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 208. Dynamics characteristics: SD / MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	133	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} =52MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} =52MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(3)/DDR(3) mode						
t_{ISU}	Input setup time HS	-	2.5	-	-	ns
t_{IH}	Input hold time HS	-	0.5	-	-	
t_{IDW}(4)	Input valid window (variable window)	-	3	-	-	-
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR/DDR(3) mode						
t_{OV}	Output valid time HS	-	-	3.5	5	ns
t_{OH}	Output hold time HS	-	3	-	-	

Table 208. Dynamics characteristics: SD / MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	2.5		-	ns
t_{IHD}	Input hold time SD	-	0.5		-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	0.5	2	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. Guaranteed by characterization results.
2. Above 100 MHz, C_L = 20 pF.
3. An external voltage converter is required to support SD 1.8 V.
4. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Table 209. Dynamics characteristics: eMMC characteristics VDD = 1.71V to 1.9V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	120	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} =52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} =52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	-	2	-	-	ns
t_{IH}	Input hold time HS	-	1.5	-	-	
t_{IDW}(3)	Input valid window (variable window)	-	3.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OVD}	Output valid time HS	-	-	5	7	ns
t_{OHD}	Output hold time HS	-	3	-	-	

1. Guaranteed by characterization results.
2. C_L = 20 pF.
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Figure 110. SDIO high-speed mode

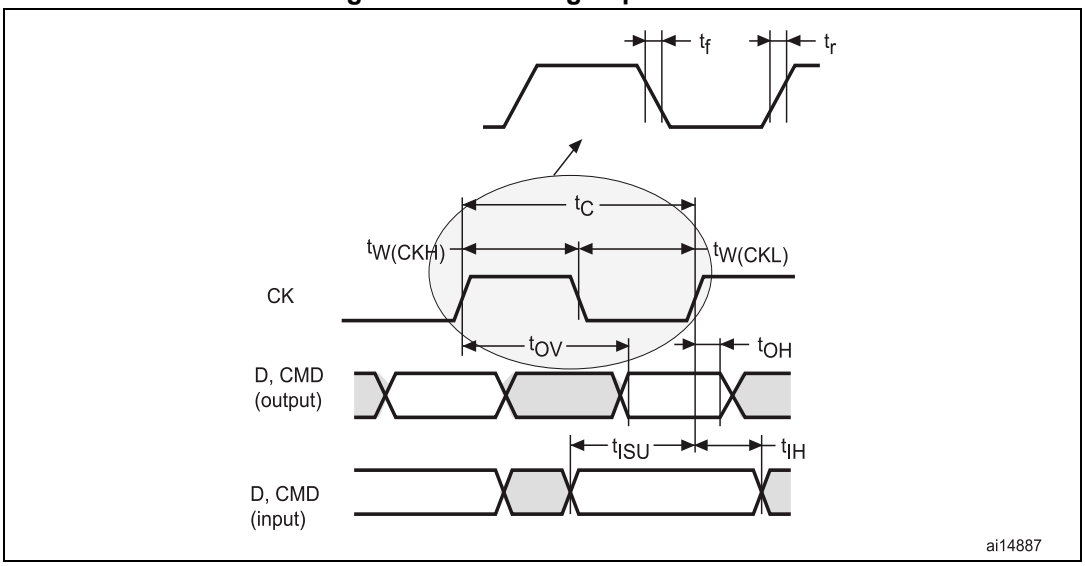


Figure 111. SD default mode

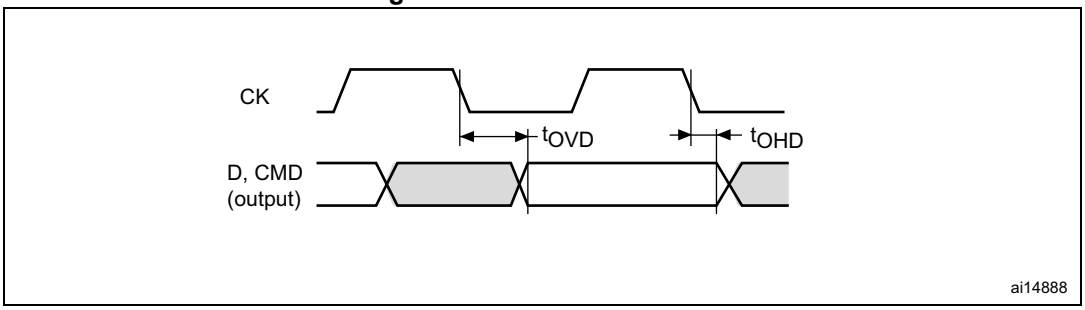
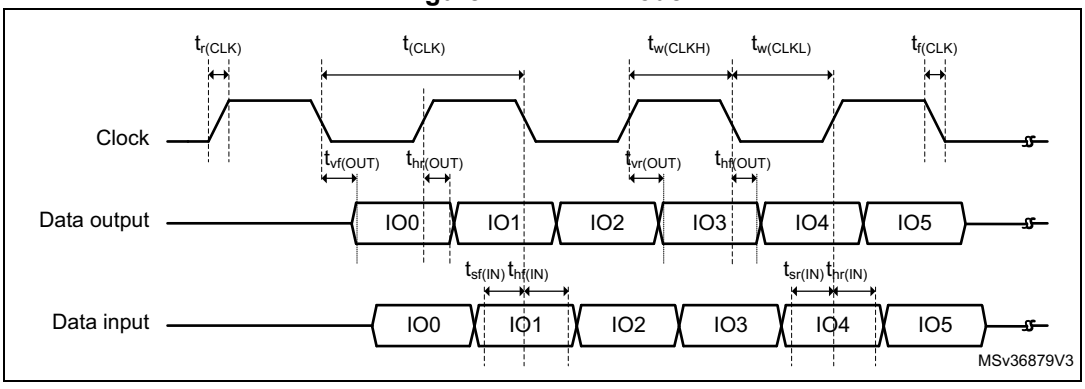


Figure 112. DDR mode



USB OTG_FS characteristics

The USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 210. USB OTG_FS electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DD33USB}$	USB transceiver operating voltage	-	3.0(1)	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}	Output driver impedance(2)	Driver high and low	28	36	44	

1. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V voltage range.
2. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

USB OTG_HS characteristics

Unless otherwise specified, the parameters given in *Table 211* for ULPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in *Table 121: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS1

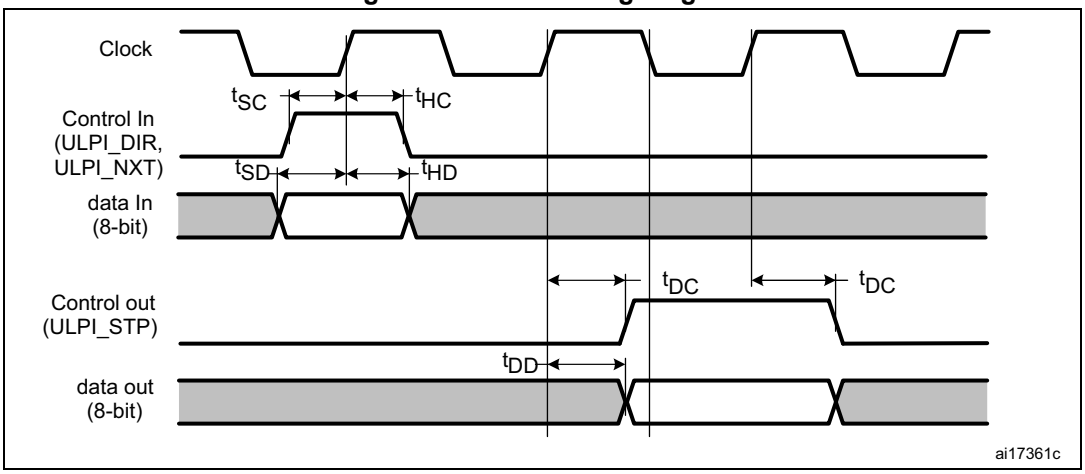
Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 211. Dynamics characteristics: USB ULPI(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR , ULPI_NXT) setup time	-	2.5	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	2	-	-	
t_{SD}	Data in setup time	-	2.5	-	-	
t_{HD}	Data in hold time	-	0	-	-	
t_{DC}/t_{DD}	Control/Datal output delay	$2.7<V_{DD}<3.6$ V C_L=20 pF	-	9	9.5	
		$1.71<V_{DD}<3.6$ V C_L=15 pF	-	9	14	

1. Guaranteed by characterization results.

Figure 113. ULPI timing diagram



Ethernet interface characteristics

Unless otherwise specified, the parameters given in *Table 212*, *Table 213* and *Table 214* for SMI, RMII and MII are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage conditions summarized in *Table 121: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L=20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS1

Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output characteristics:

Table 212. Dynamics characteristics: Ethernet MAC signals for SMI (1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	400	400	403	ns
$T_{d(MDIO)}$	Write data valid time	0.5	1.5	4	
$t_{su(MDIO)}$	Read data setup time	12.5	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

Figure 114. Ethernet SMI timing diagram

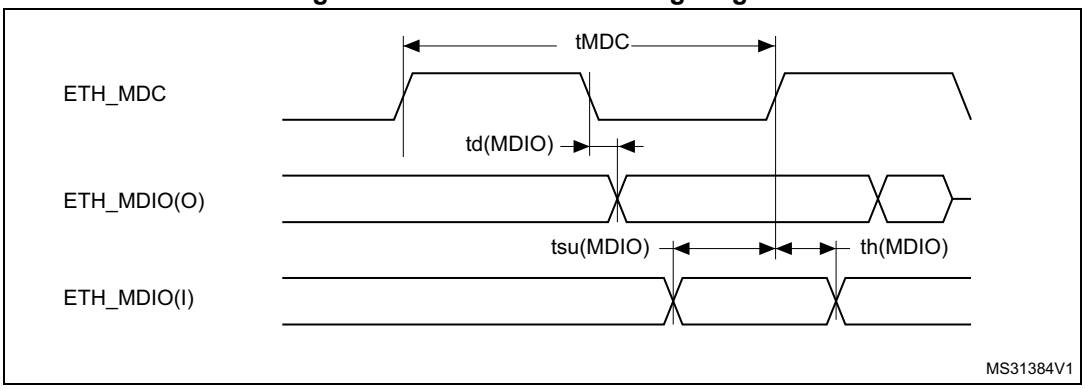


Table 213. Dynamics characteristics: Ethernet MAC signals for RMII (1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(CRS)}$	Carrier sense setup time	1.5	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	1.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	7	8	9.5	
$t_{d(TXD)}$	Transmit data valid delay time	8	9	11	

1. Guaranteed by characterization results.

Figure 115. Ethernet RMII timing diagram

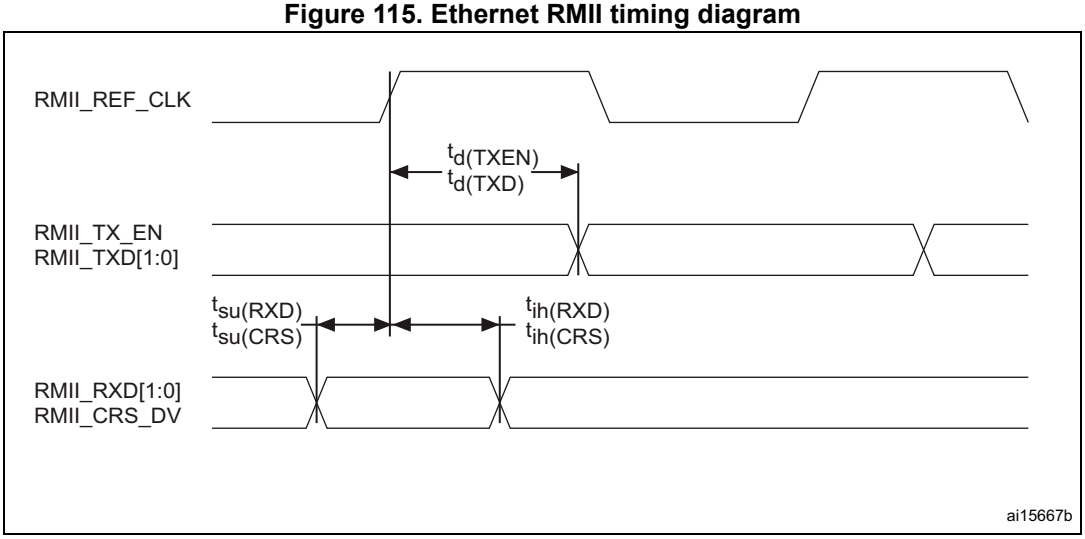
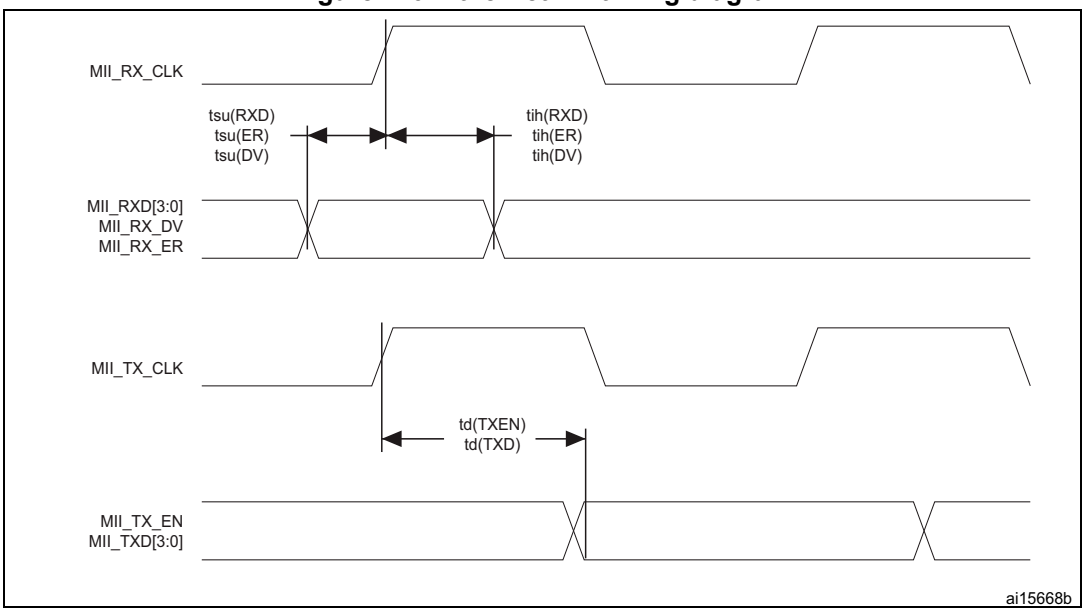


Table 214. Dynamics characteristics: Ethernet MAC signals for MII (1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(DV)}$	Data valid setup time	1.5	-	-	
$t_{ih(DV)}$	Data valid hold time	1.5	-	-	
$t_{su(ER)}$	Error setup time	1.5	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	9	10	11	
$t_{d(TXD)}$	Transmit data valid delay time	8.5	9.5	12.5	

1. Guaranteed by characterization results.

Figure 116. Ethernet MII timing diagram



JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 215* and *Table 216* for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage summarized in *Table 121: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x10
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS1

Refer to *Section 7.3.15: I/O port characteristics* for more details on the input/output characteristics:

Table 215. Dynamics JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	T_{CK} clock frequency	2.7V <V_{DD}< 3.6 V	-	-	37	MHz
$1/t_{c(TCK)}$		1.62 <V_{DD}< 3.6 V	-	-	27.5	
$ti_{su(TMS)}$	TMS input setup time	-	2.5	-	-	
$ti_{h(TMS)}$	TMS input hold time	-	1	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	1.5	-	-	-
$ti_{h(TDI)}$	TDI input hold time	-	1	-	-	-
$t_{ov(TDO)}$	TDO output valid time	2.7V <V_{DD}< 3.6 V	-	8	13.5	-
		1.62 <V_{DD}< 3.6 V	-	8	18	-
$t_{oh(TDO)}$	TDO output hold time	-	7	-	-	-

Table 216. Dynamics SWD characteristics:

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	2.7V <V_{DD}< 3.6 V	-	-	71	MHz
$1/t_{c(SWCLK)}$		1.62 <V_{DD}< 3.6 V	-	-	52.5	
$t_{isu(SWDIO)}$	SWDIO input setup time	-	2.5	-	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time	-	1	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	2.7V <V_{DD}< 3.6 V	-	8.5	14	
		1.62 <V_{DD}< 3.6 V	-	8.5	19	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8	-	-	

Figure 117. JTAG timing diagram

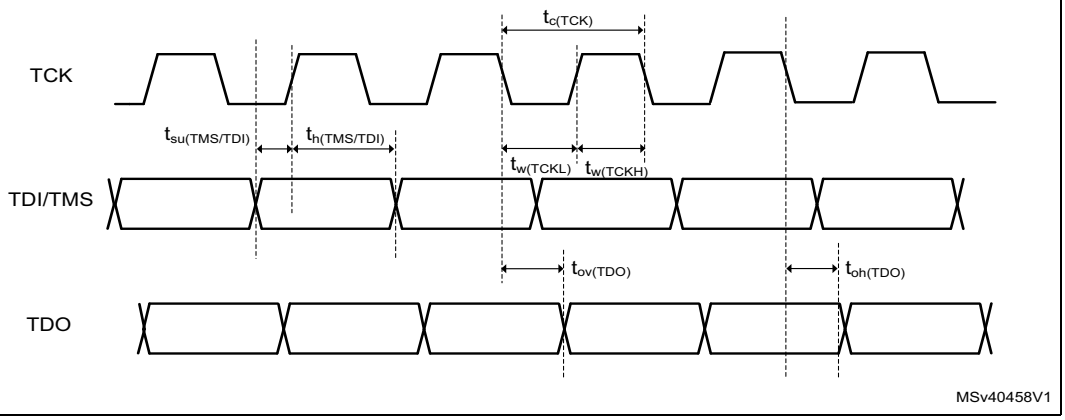
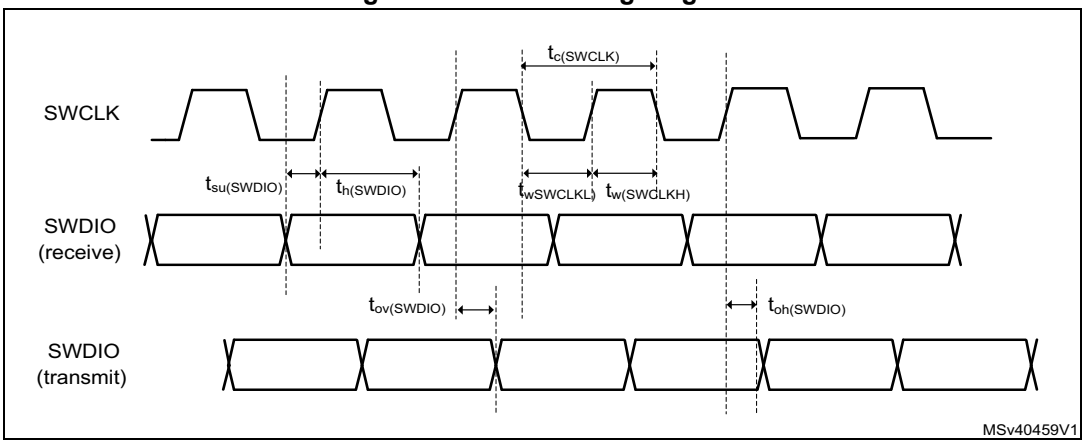


Figure 118. SWD timing diagram



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status *are available at www.st.com.* ECOPACK is an ST trademark.

8.1 LQFP100 package information

The LQFP100 is a 100-pin, 14 x 14 mm low-profile quad flat package.

Note: See list of notes in the Notes section.

Figure 119. LQFP100 - Outline(15)

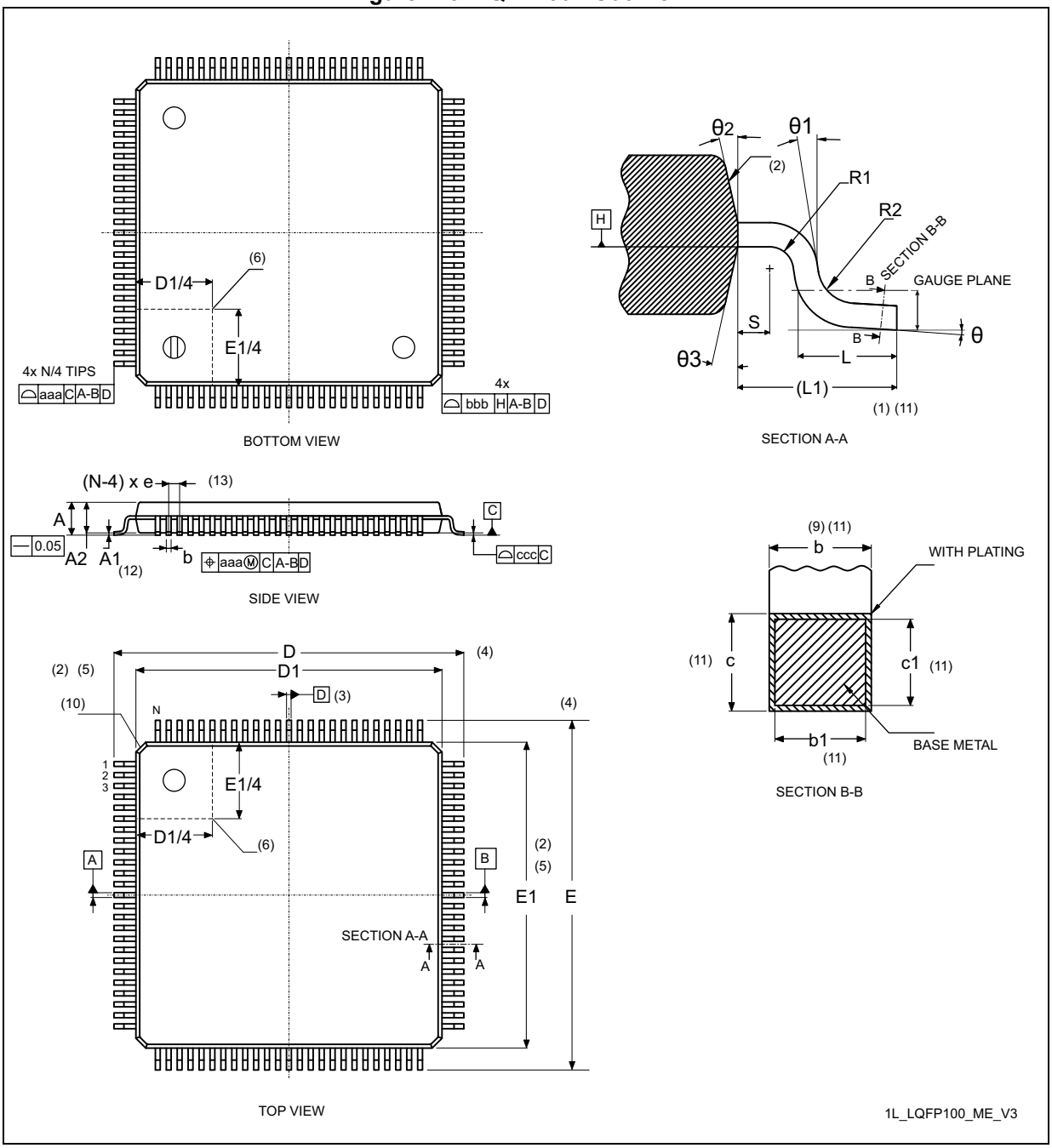


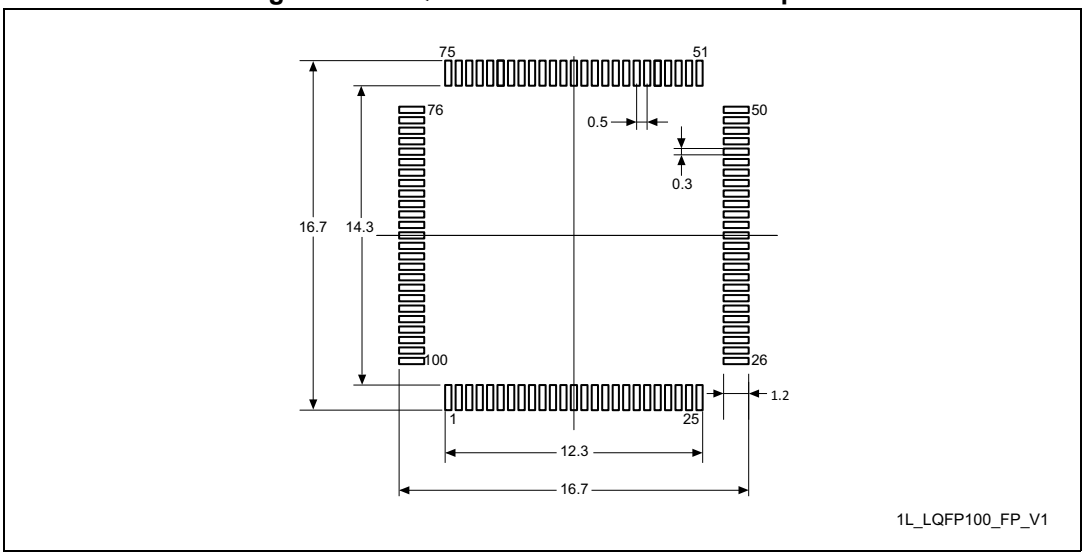
Table 217. LQFP100 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	1.50	1.60	-	0.0590	0.0630
A1[12]	0.05	-	0.15	0.0019	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	16.00			0.6299		
D1[2][5]	14.00			0.5512		
E[4]	16.00			0.6299		
E1[2][5]	14.00			0.5512		
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.177	0.0236	0.0295
L1[1][11]	1.00			-	0.0394	-
N	100					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 120. LQFP100 - Recommended footprint



1. Dimensions are expressed in millimeters.

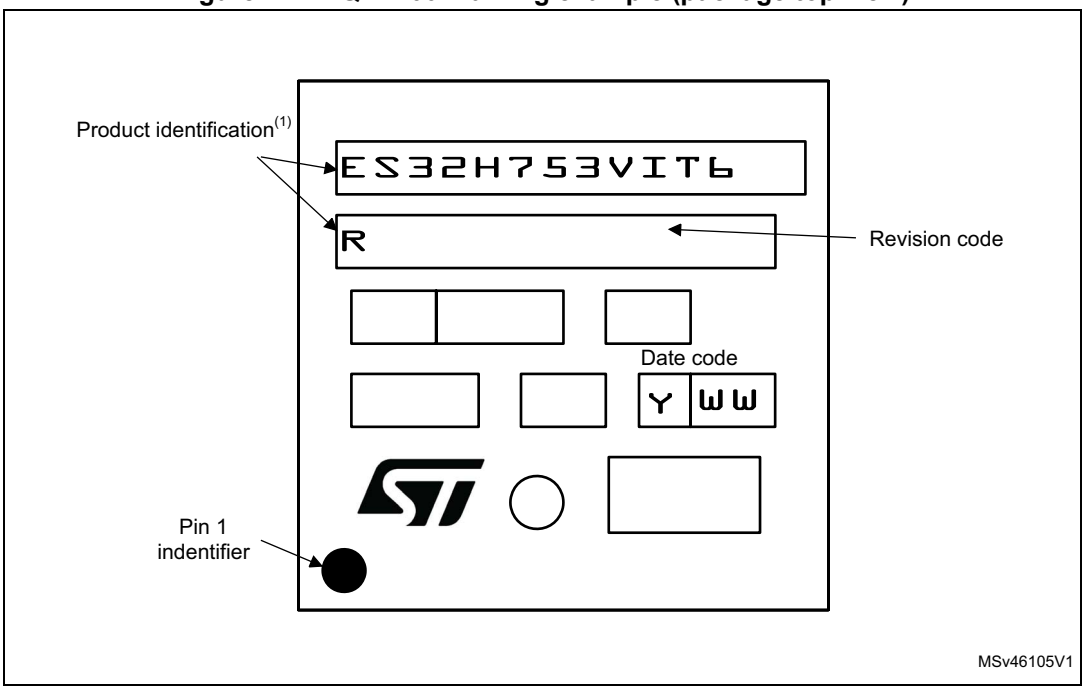
Device marking for LQFP100

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 121. LQFP100 marking example (package top view)

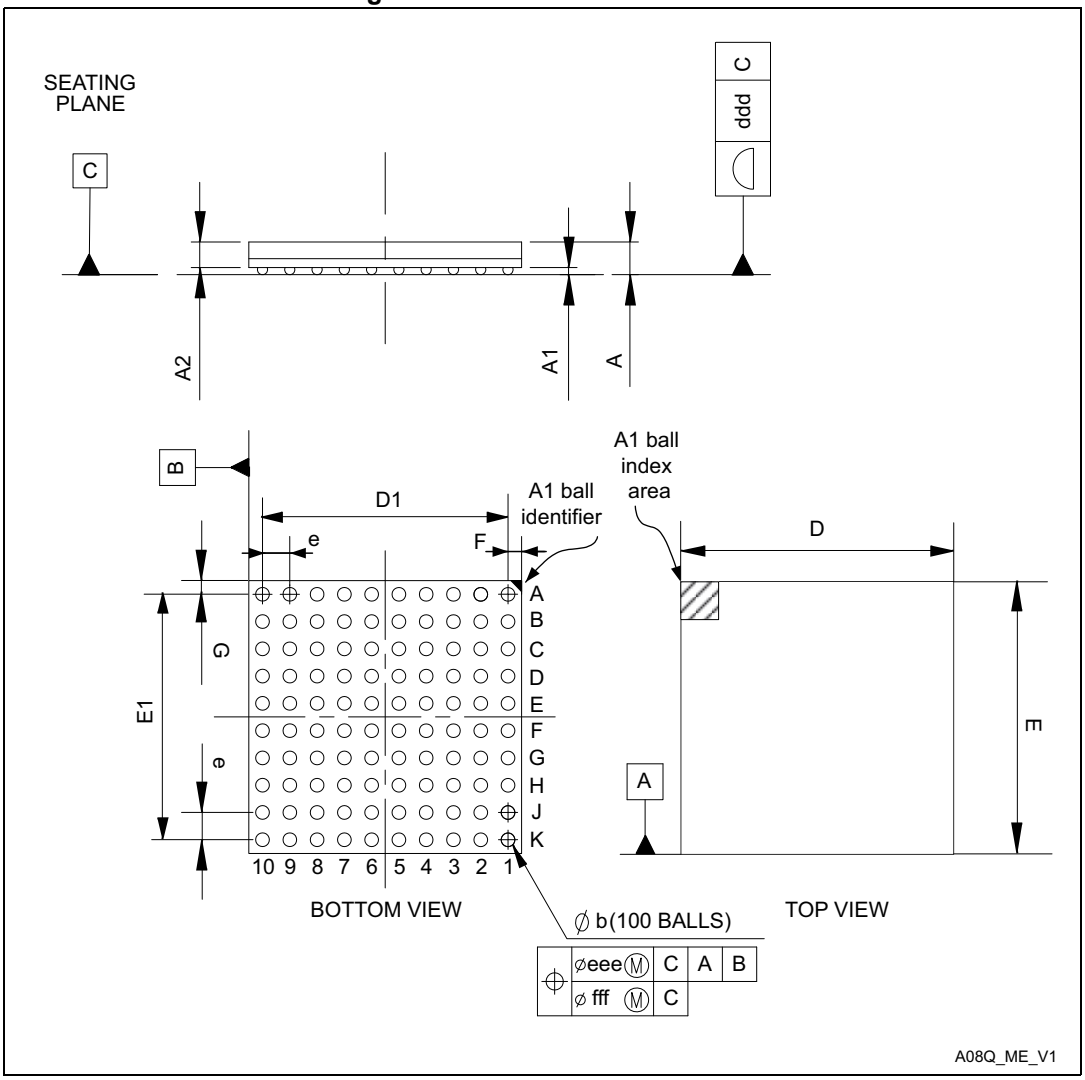


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.2 TFBGA100 package information

The TFBGA100 is a 100-ball, 8 x 8 mm, 0.8 mm pitch, thin fine-pitch ball grid array package.

Figure 122. TFBGA100 - Outline



1. Drawing is not to scale.

Table 218. TFBGA100 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	7.850	8.000	8.150	0.3091	0.3150	0.3209

Table 218. TFBGA100 - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D1	-	7.200		-	0.2835	-
E	7.850	8.000	8.150	0.3091	0.3150	0.3209
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	0.400	-	-	0.0157	-
G	-	0.400	-	-	0.0157	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 123. TFBGA100 - Recommended footprint

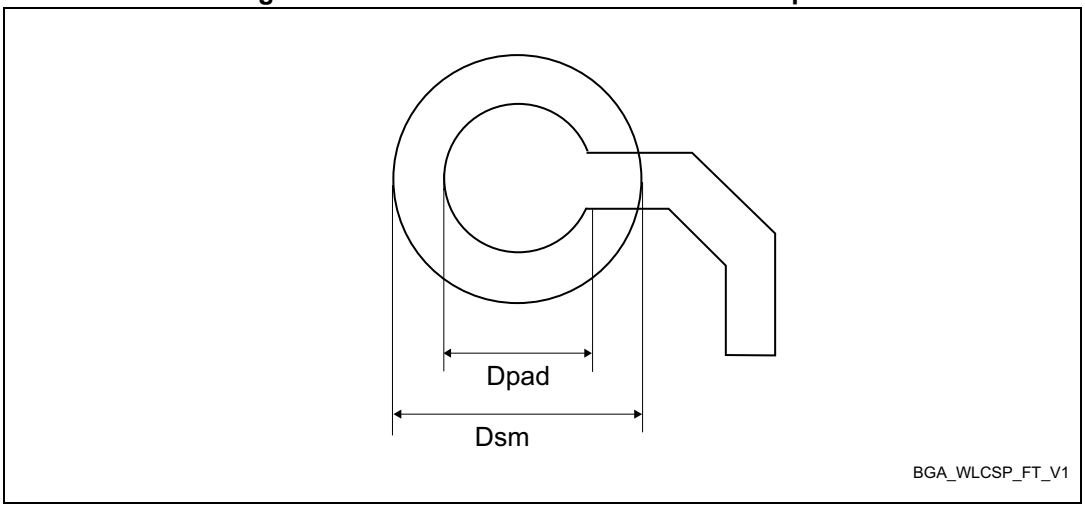


Table 219. TFBGA100 - Recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

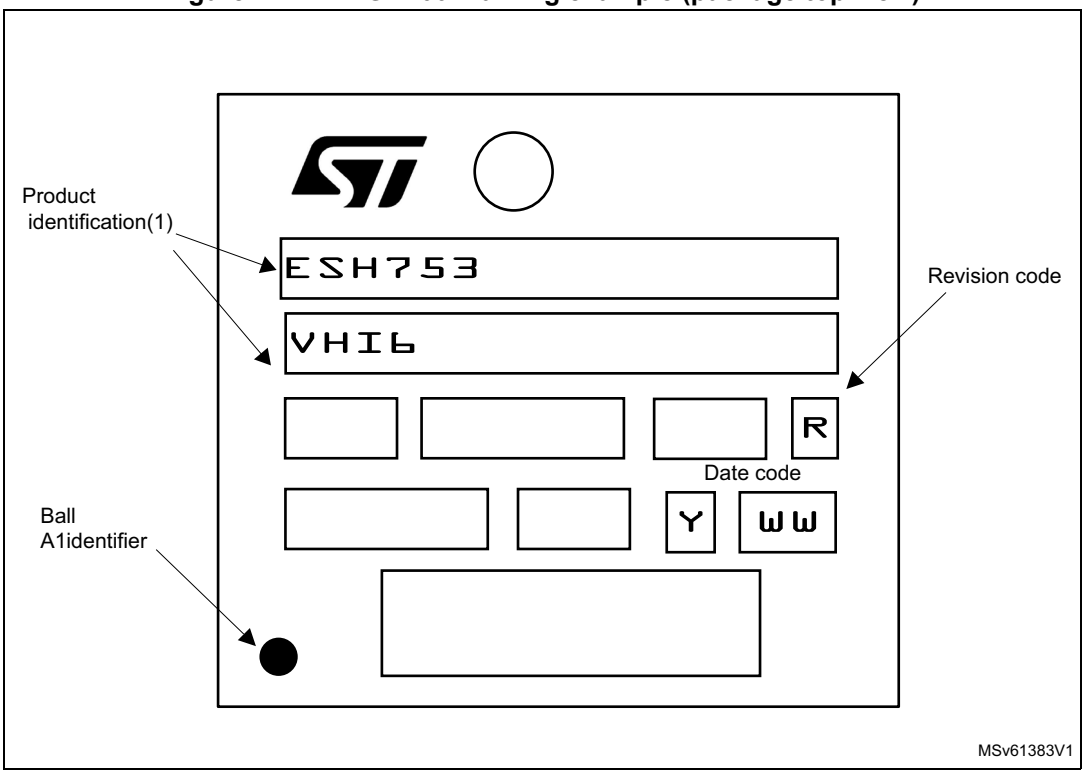
Device marking for TFBGA100

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 124. TFBGA100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.3 LQFP144 package information

The LQFP144 is a 144-pin, 20 x 20 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 125. LQFP144 - Outline(15)

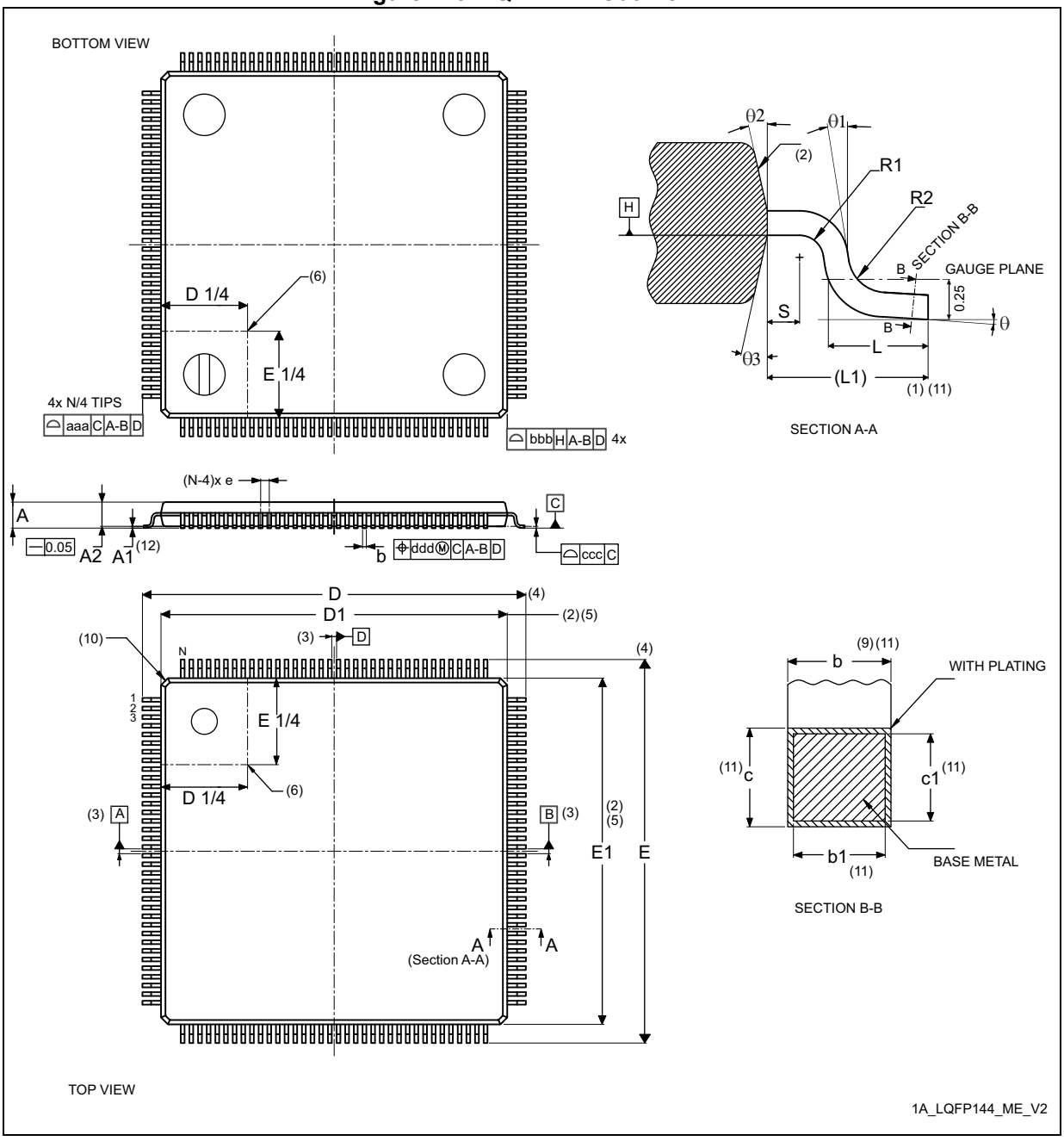


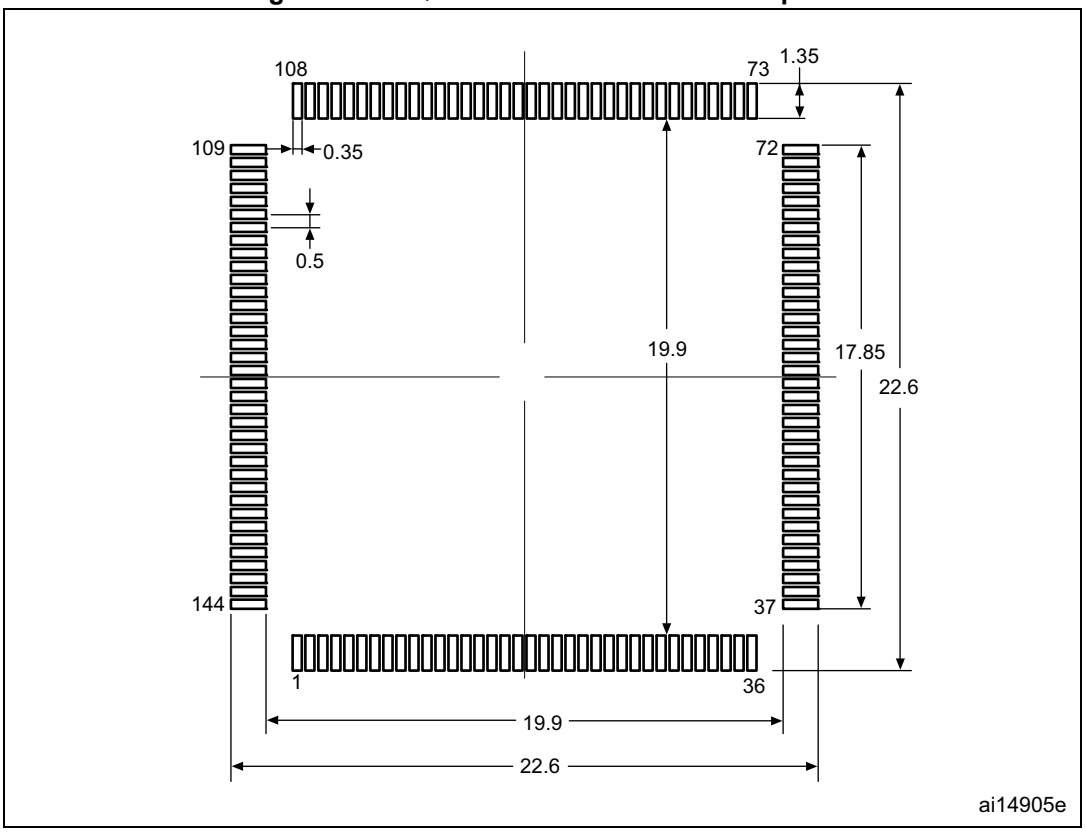
Table 220. LQFP144 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	22.00 BSC			0.8661 BSC		
D1[2][5]	20.00 BSC			0.7874 BSC		
E[4]	22.00 BSC			0.8661 BSC		
E1[2][5]	20.00 BSC			0.7874 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	144					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 126. LQFP144 - Recommended footprint



1. Dimensions are expressed in millimeters.

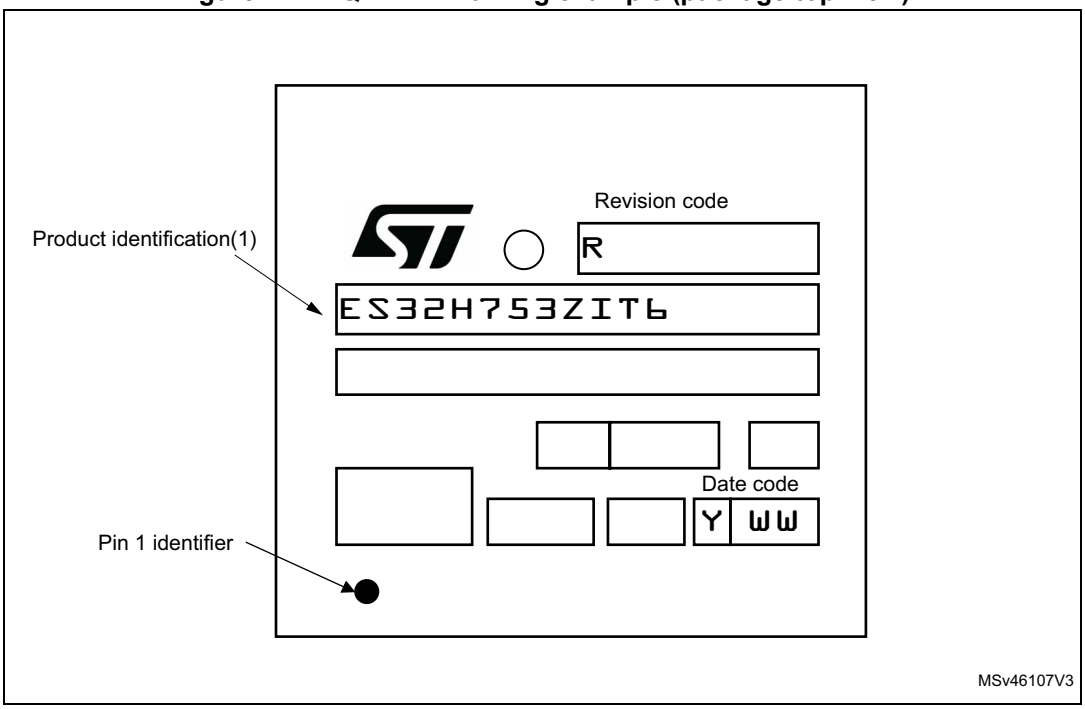
Device marking for LQFP144

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 127. LQFP144 marking example (package top view)

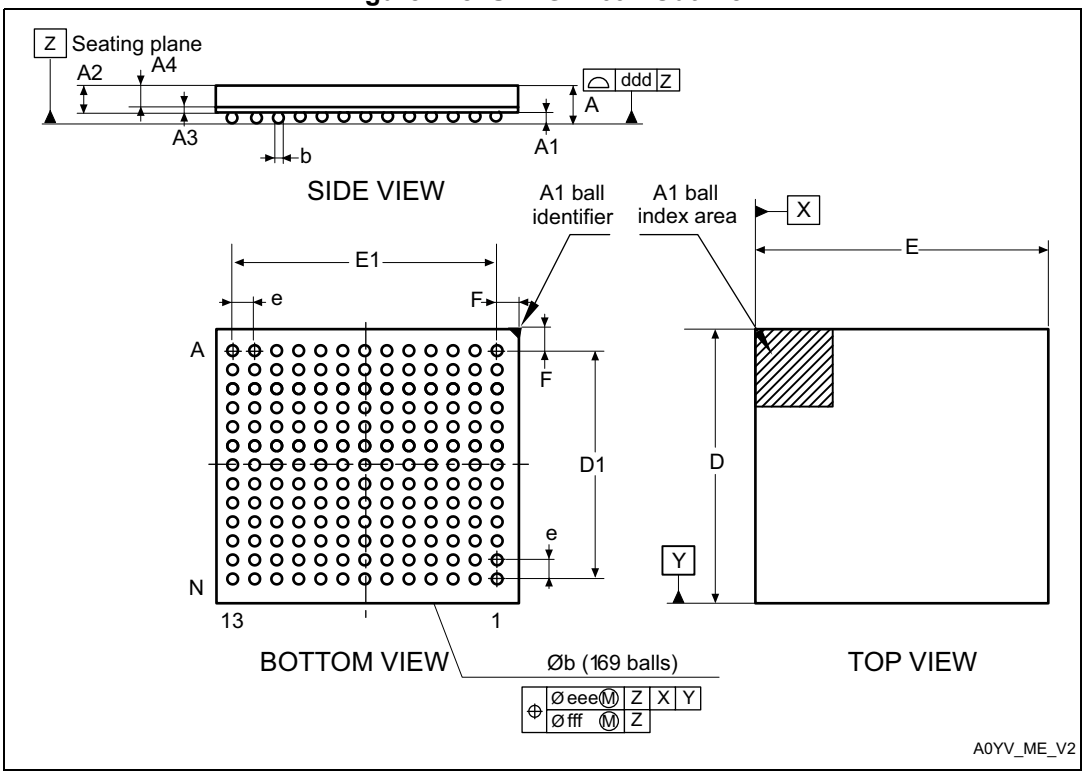


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.4 UFBGA169 package information

The UFBGA169 is a 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Figure 128. UFBGA169 - Outline



1. Drawing is not in scale.

Table 221. UFBGA169 - Mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-

Table 221. UFBGA169 - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	0.450	0.500	0.550	0.0177	0.0197	0.0217
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 129. UFBGA169 - Recommended footprint

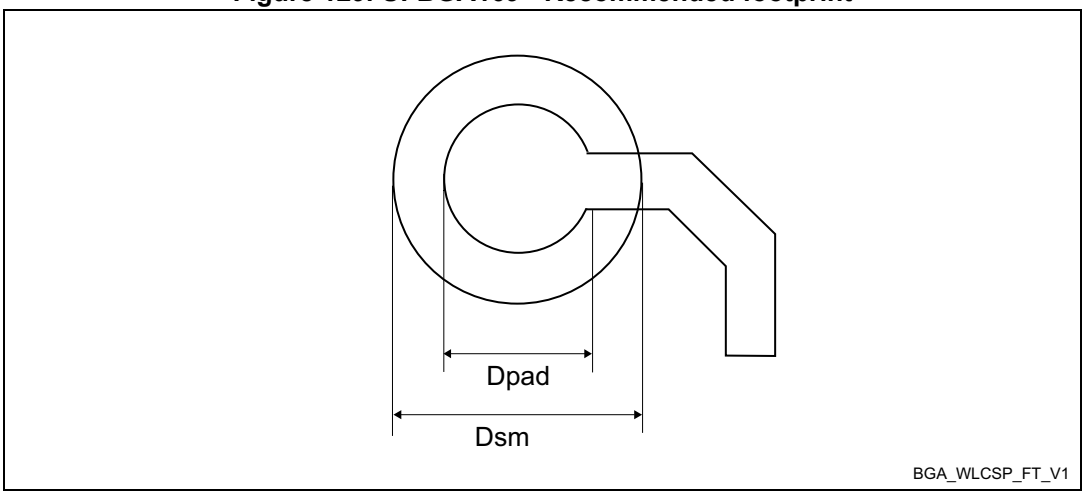


Table 222. UFBGA169 - Recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non-solder mask defined (NSMD) pads are recommended.

Note: 4 to 6 mils solder paste screen printing process.

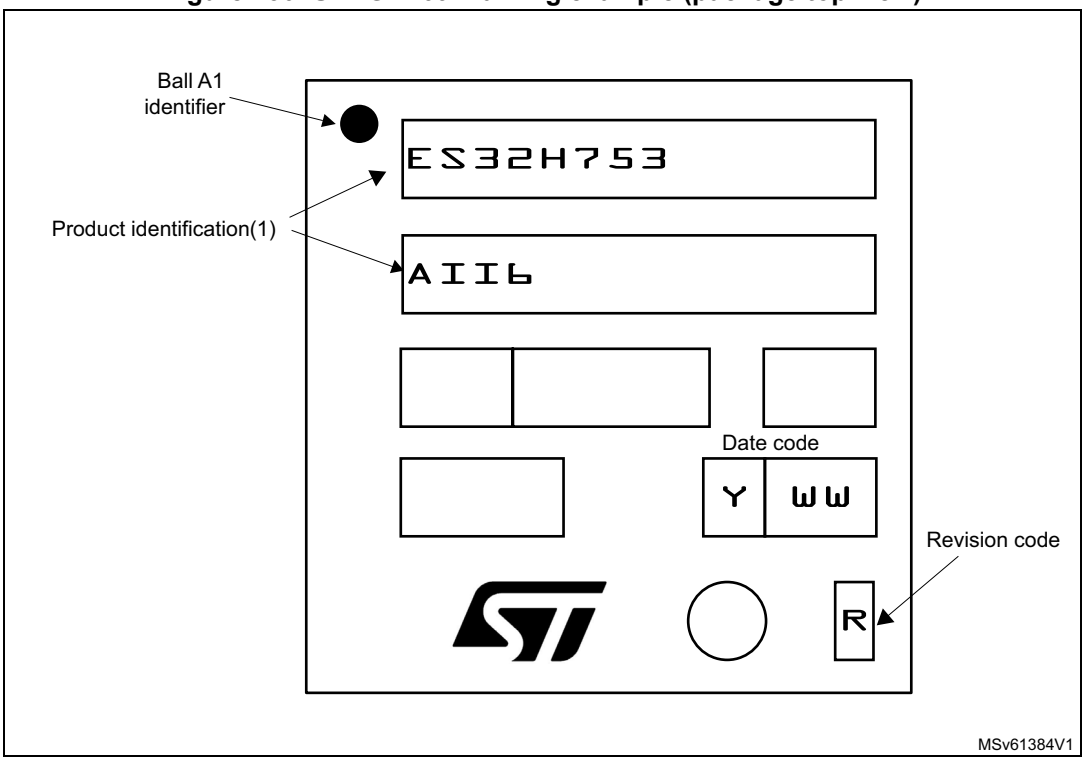
Device marking for UFBGA169

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 130. UFBGA169 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.5 LQFP176 package information

The LQFP176 is a 176-pin, 24 x 24 mm, 0.5 mm pitch, low profile quad flat package.

Note: See list of notes in the Notes section.

Figure 131. LQFP176 - Outline

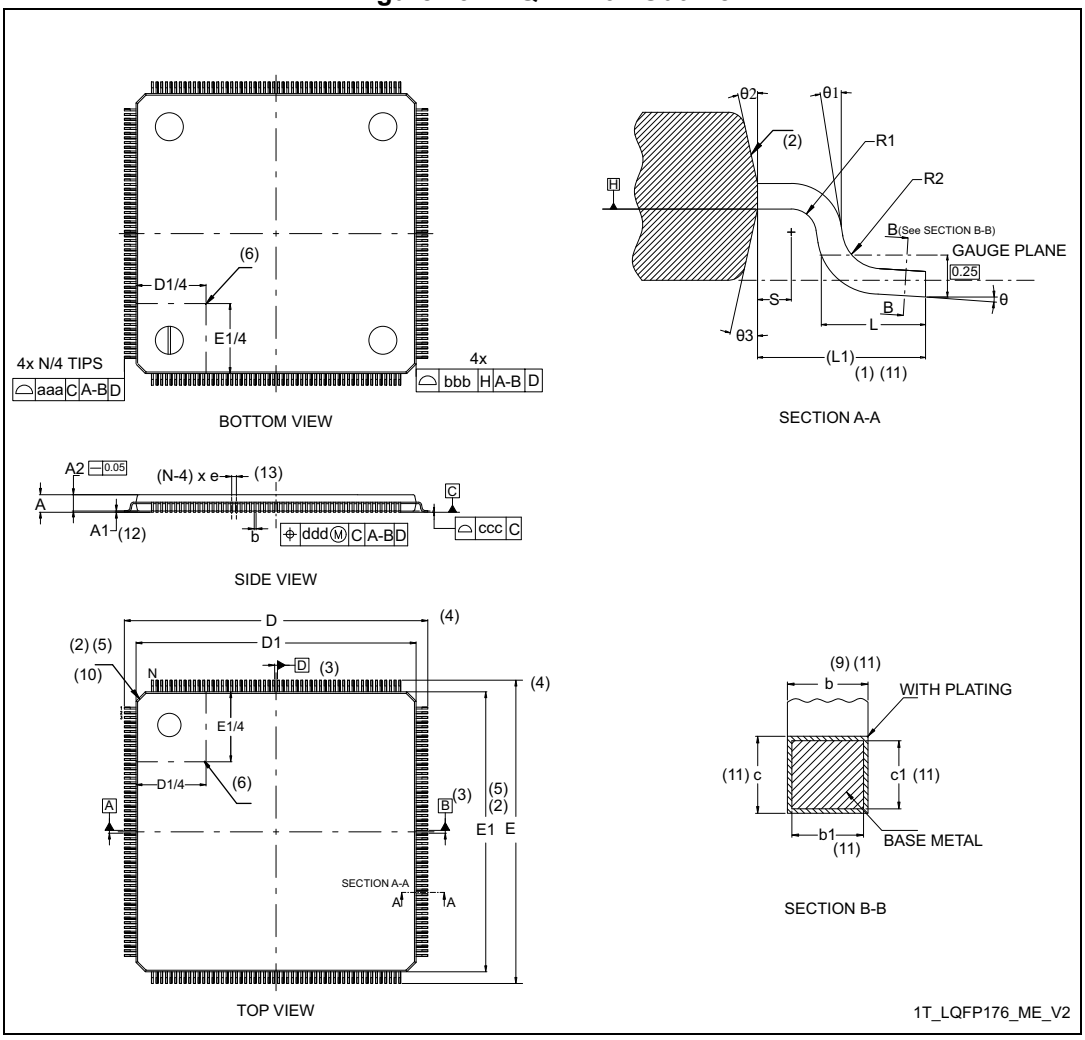


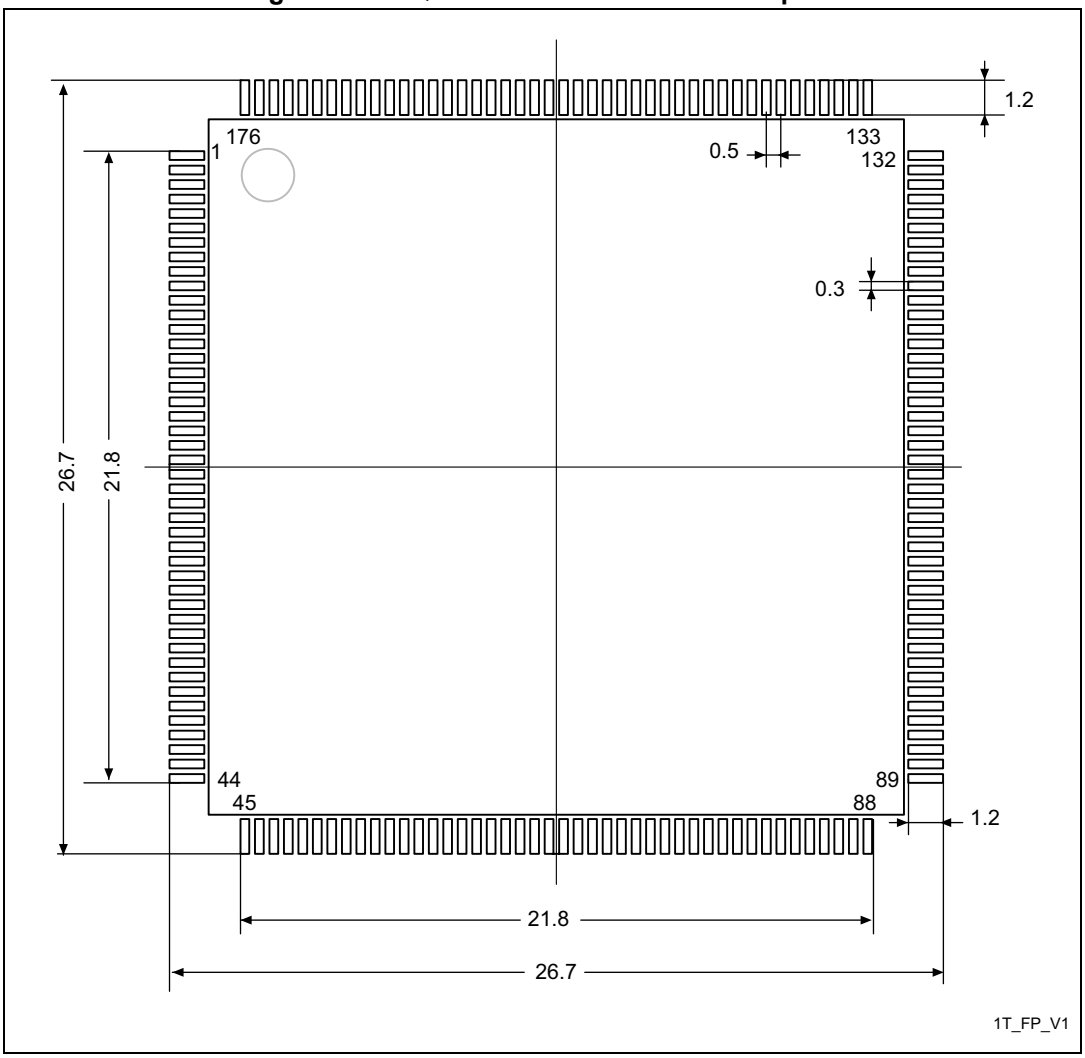
Table 223. LQFP176 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b[9][11]	0.170	0.220	0.270	0.0067	0.0087	0.0106
b1[11]	0.170	0.200	0.230	0.0067	0.0079	0.0091
c[11]	0.090	-	0.200	0.0035	-	0.0079
c1[11]	0.090	-	0.160	0.0035	-	0.063
D[4]	26.000			1.0236		
D1[2][5]	24.000			0.9449		
E[4]	26.000			0.0197		
E1[2][5]	24.000			0.9449		
e	0.500			0.1970		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1[1][11]	1			0.0394 REF		
N[13]	176					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.080	-	-	0.0031	-	-
R2	0.080	-	0.200	0.0031	-	0.0079
S	0.200	-	-	0.0079	-	-
aaa	0.200			0.0079		
bbb	0.200			0.0079		
ccc	0.080			0.0031		
ddd	0.080			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 132. LQFP176 - Recommended footprint



1. Dimensions are expressed in millimeters.

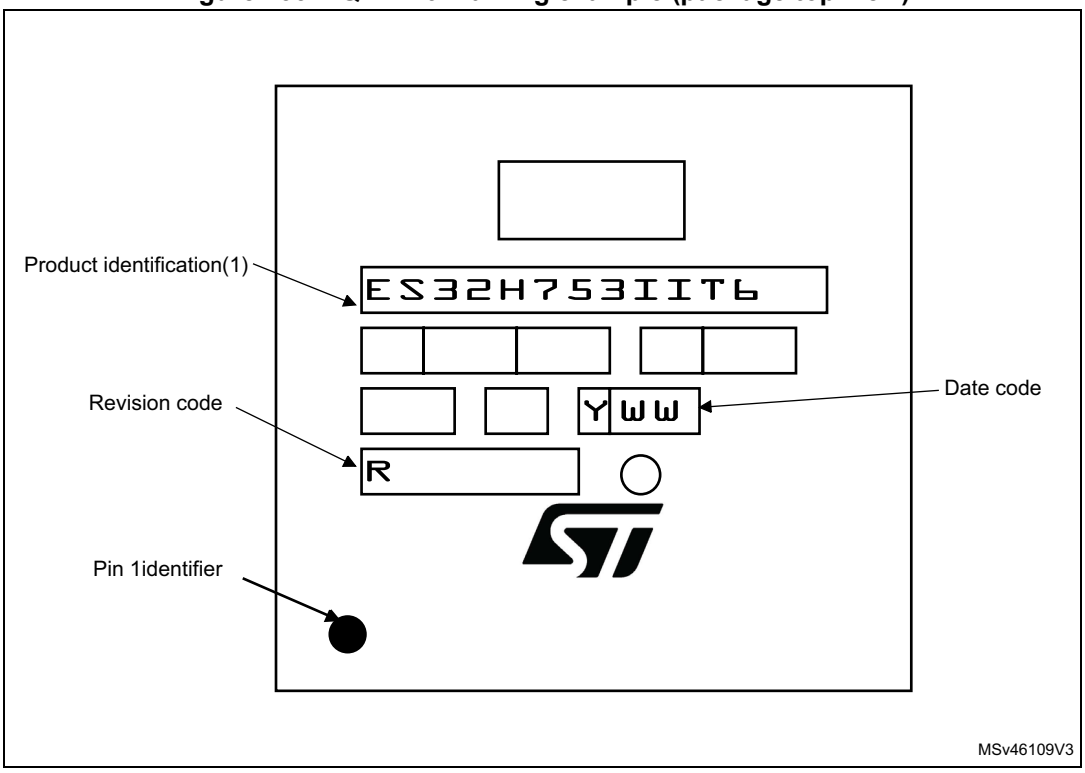
Device marking for LQFP176

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 133. LQFP176 marking example (package top view)

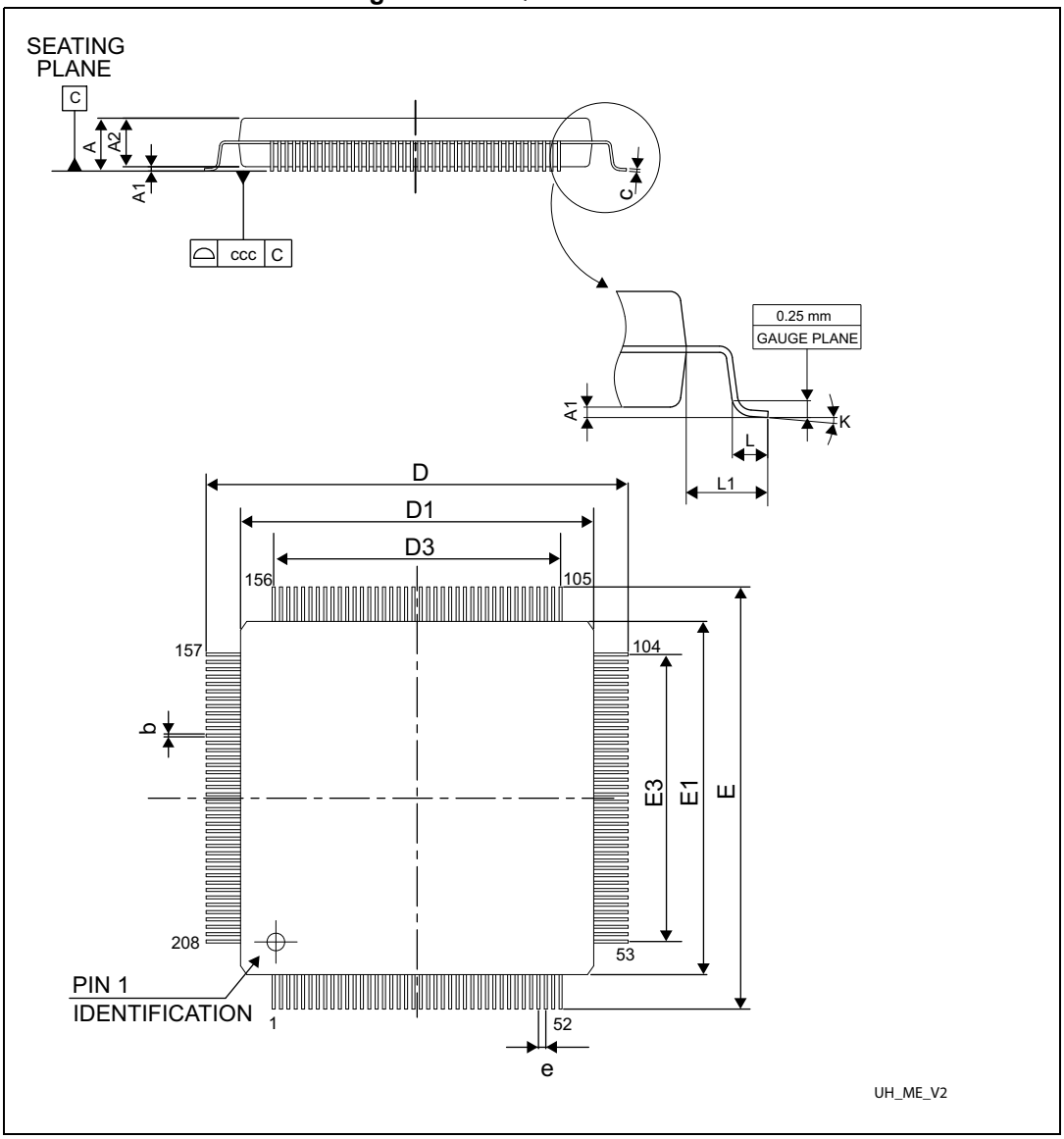


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.6 LQFP208 package information

The LQFP208 is a 208-pin, 28 x 28 mm low-profile quad flat package.

Figure 134. LQFP208 - Outline



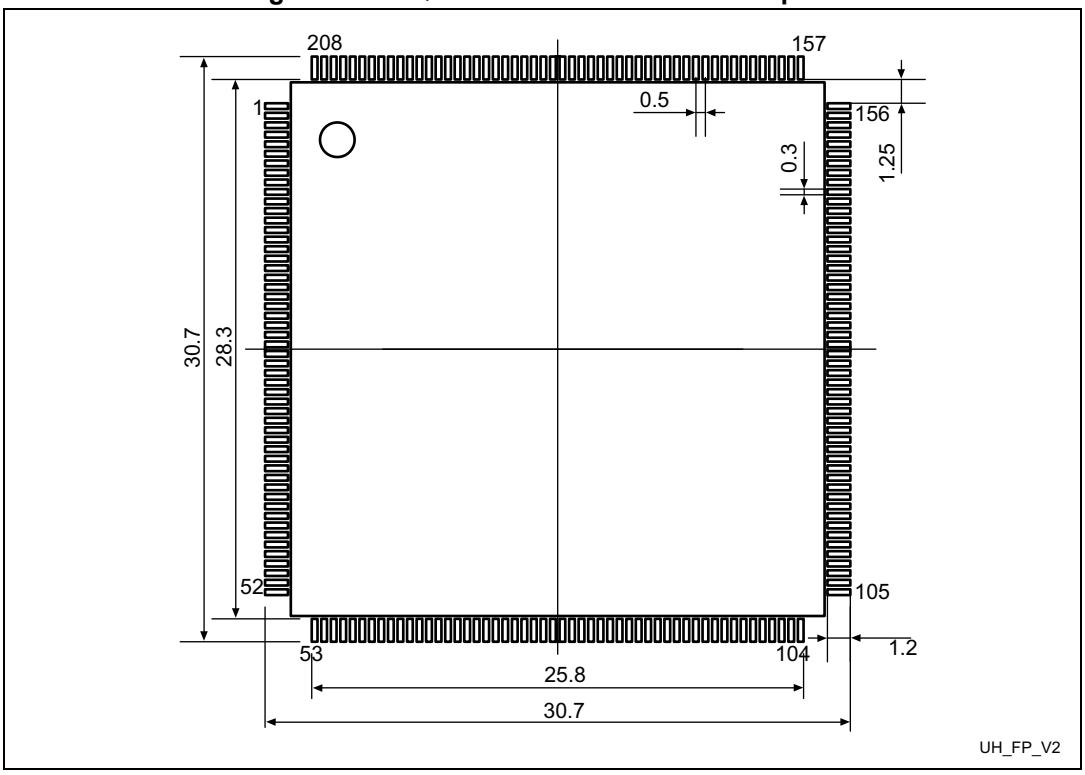
1. Drawing is not to scale.

Table 224. LQFP208 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	29.800	30.000	30.200	1.1811	1.1732	1.1890
D1	27.800	28.000	28.200	1.1024	1.0945	1.1102
D3	-	25.500	-	-	1.0039	-
E	29.800	30.000	30.200	1.1811	1.1732	1.1890
E1	27.800	28.000	28.200	1.1024	1.0945	1.1102
E3	-	25.500	-	-	1.0039	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 135. LQFP208 - Recommended footprint



1. Dimensions are expressed in millimeters.

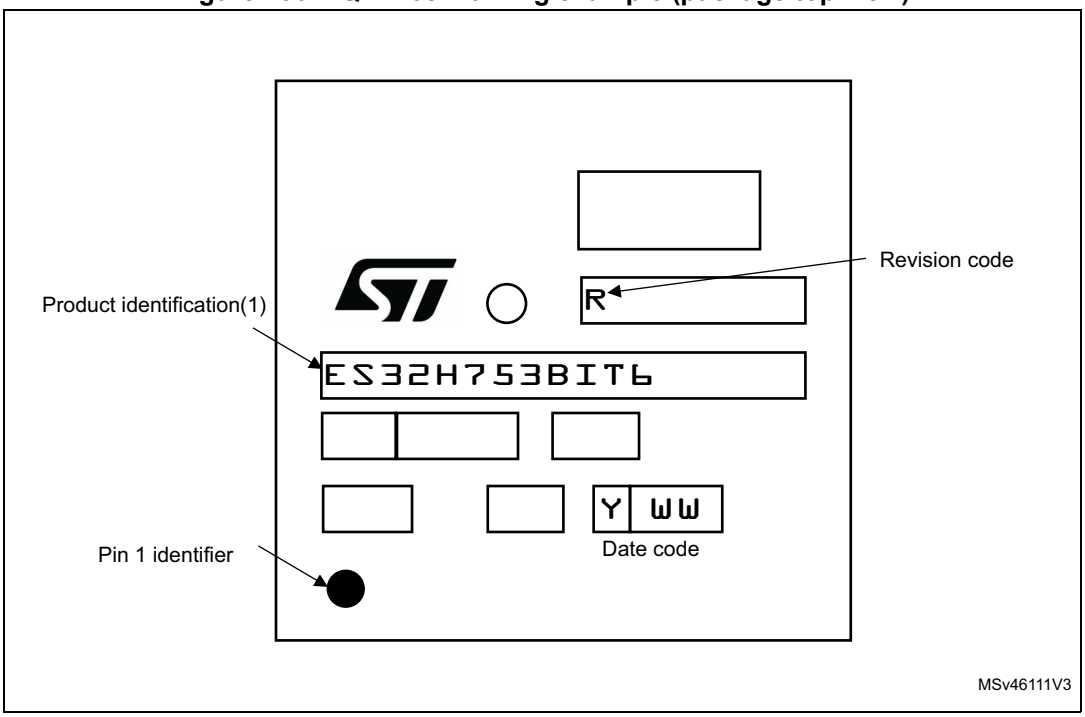
Device marking for LQFP208

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 136. LQFP208 marking example (package top view)

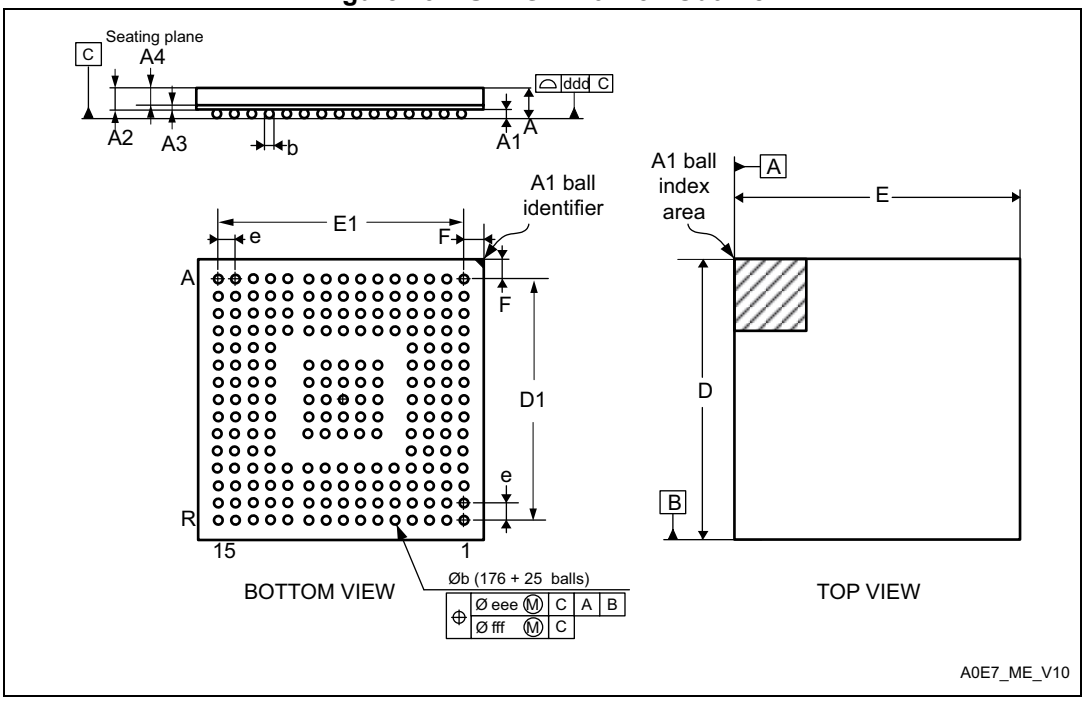


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.7 UFBGA176+25 package information

The UFBGA176+25 is a 176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package.

Figure 137. UFBGA176+25 - Outline



1. Drawing is not to scale.

Table 225. UFBGA(176+25) - Mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
F	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 225. UFBGA(176+25) - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 138. UFBGA176+25 - Recommended footprint

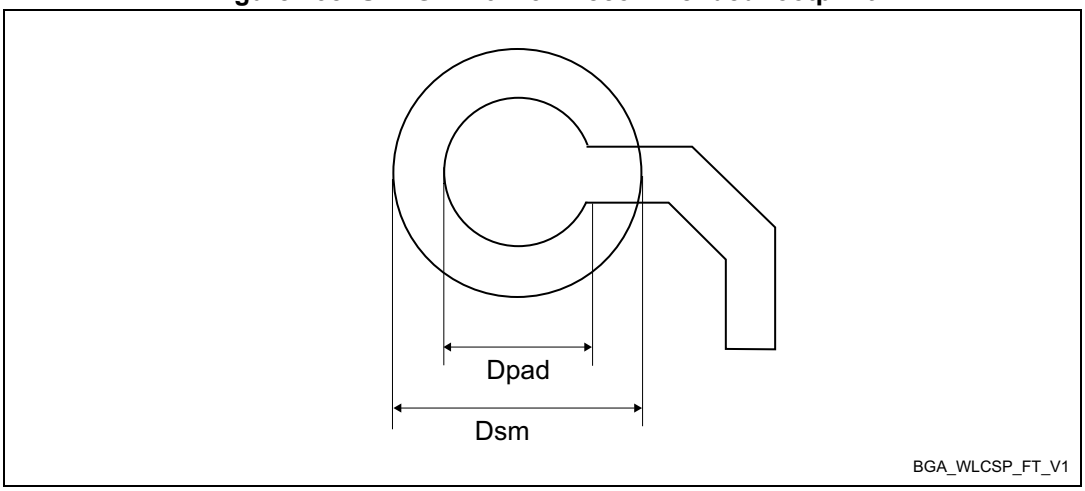


Table 226. UFBGA176+25 - Recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

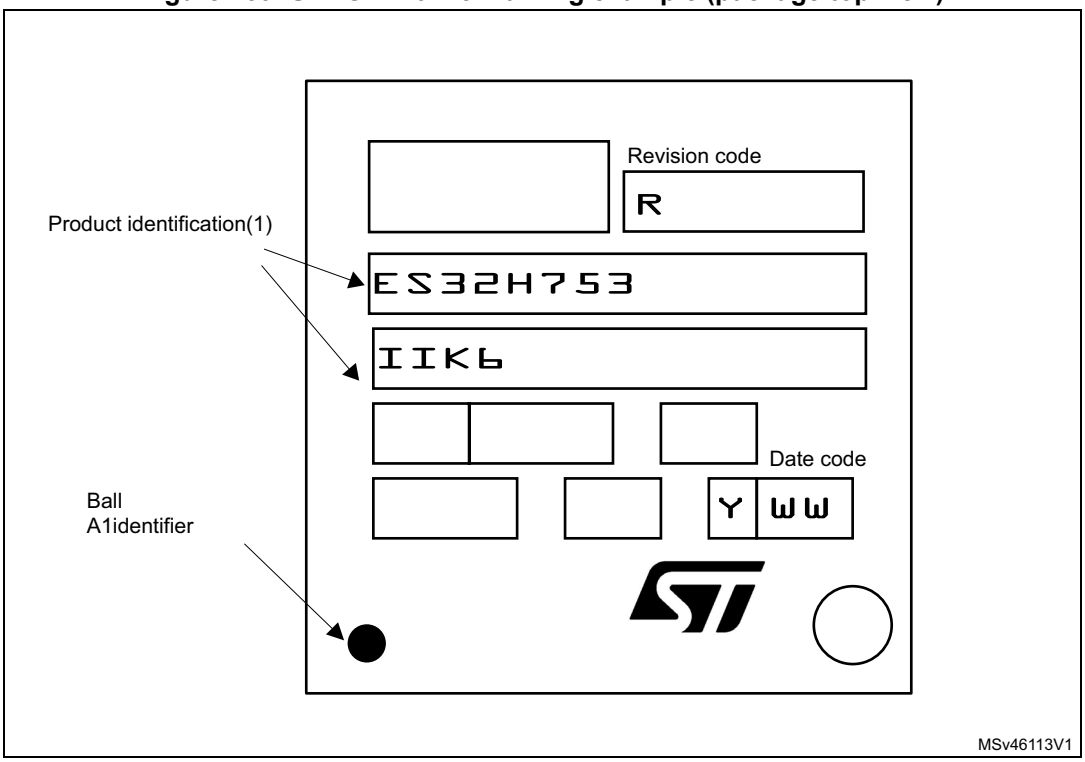
Device marking for UFBGA176+25

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 139. UFBGA176+25 marking example (package top view)

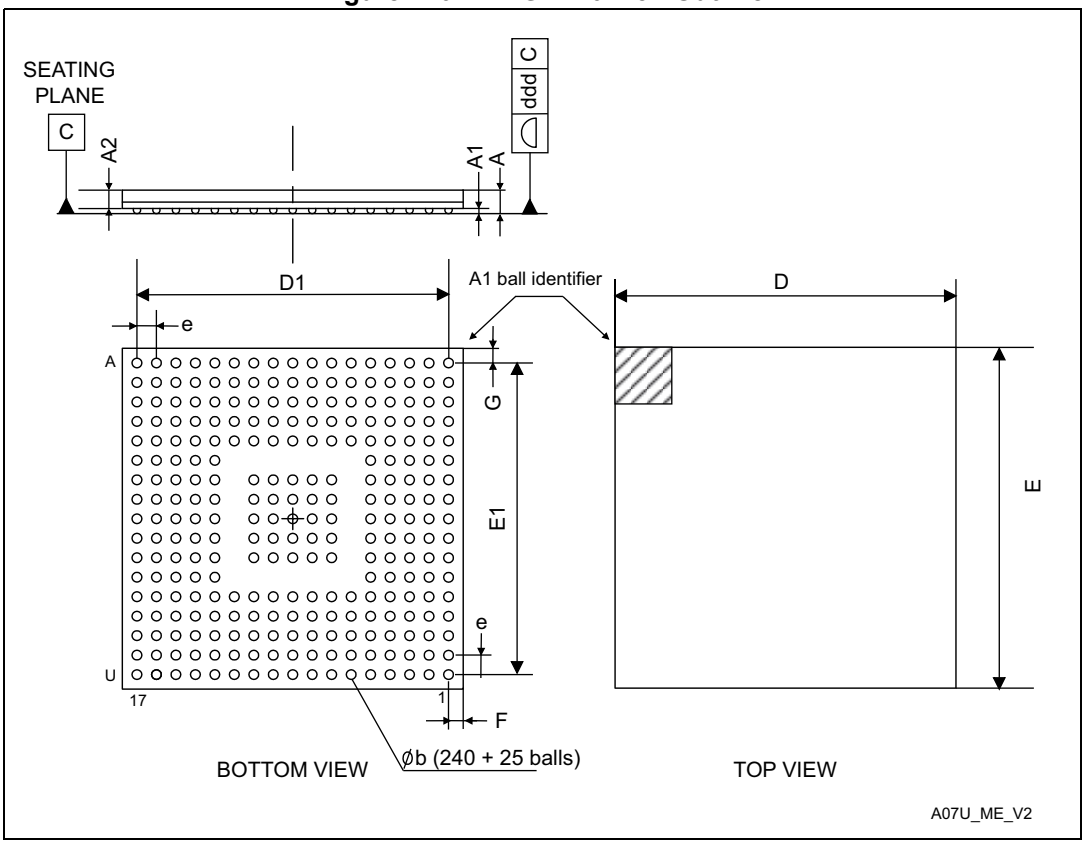


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.8 TFBGA240+25 package information

The TFBGA240+25 is a 240+25-ball, 14x14 mm, 0.8 mm pitch, fine pitch ball grid array package.

Figure 140. TFBGA240+25 - Outline



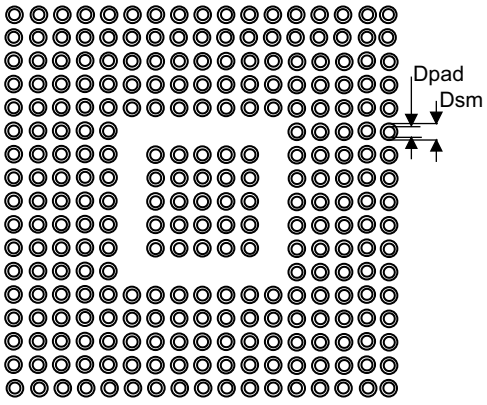
1. Dimensions are expressed in millimeters.

Table 227. TFBG240+25 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	13.850	14.000	14.150	0.5453	0.5512	0.5571
D1	-	12.800	-	-	0.5039	-
E	13.850	14.000	14.150	0.5453	0.5512	0.5571
E1	-	12.800	-	-	0.5039	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
G	-	0.600	-	-	0.0236	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 141. TFBGA240+25 - Recommended footprint



1. Dimensions are expressed in millimeters.

Table 228. TFBGA240+25 - Recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	0.100 mm

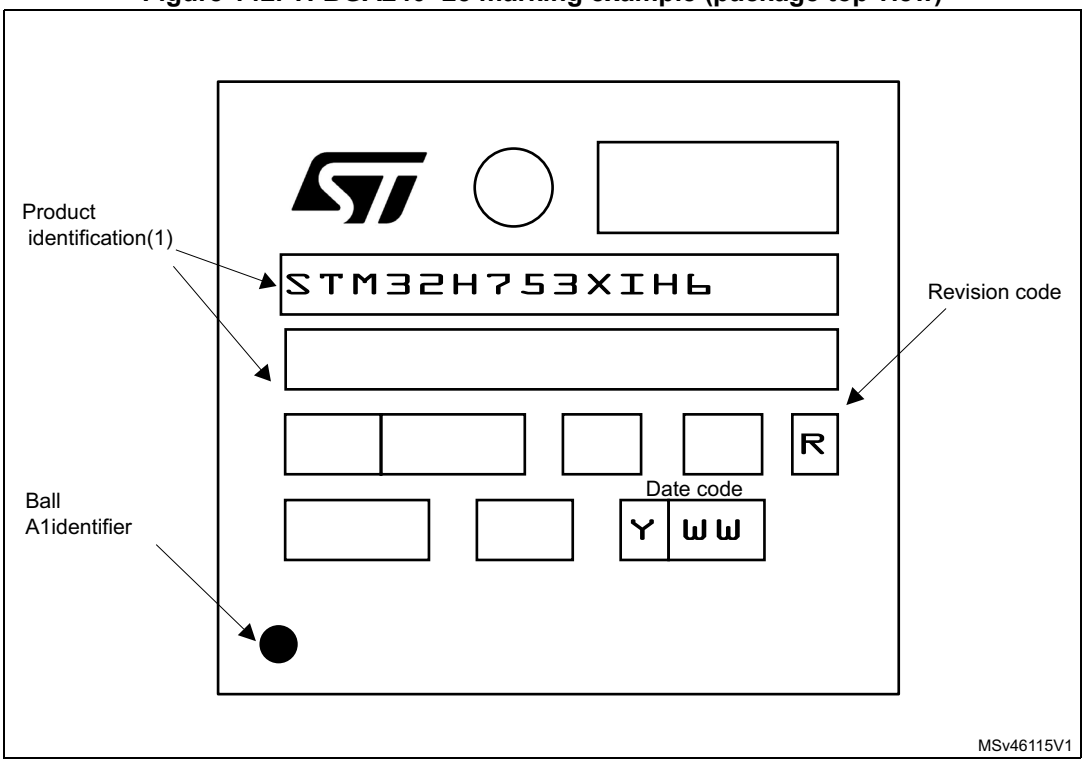
Device marking for TFBGA240+25

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 142. TFBGA240+25 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8.9 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 229. Thermal characteristics

Symbol	Definition	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	**Thermal resistance junction-ambient** LQFP100 - 14 x 14 mm /0.5 mm pitch	45.0	°C/W
		Thermal resistance junction-ambient TFBGA100 - 8 x 8 mm /0.8 mm pitch	39.3	
		Thermal resistance junction-ambient LQFP144 - 20 x 20 mm /0.5 mm pitch	43.7	
		Thermal resistance junction-ambient UFBGA169 - 7 x 7 mm /0.5 mm pitch	37.7	
		Thermal resistance junction-ambient LQFP176 - 24 x 24 mm /0.5 mm pitch	43.0	
		Thermal resistance junction-ambient LQFP208 - 28 x 28 mm /0.5 mm pitch	42.4	
		Thermal resistance junction-ambient UFBGA176+25 - 10 x 10 mm /0.65 mm pitch	37.4	
		Thermal resistance junction-ambient TFBGA240+25 - 14 x 14 mm / 0.8 mm pitch	36.6	

Table 229. Thermal characteristics (continued)

Symbol	Definition	Parameter	Value	Unit
Θ_{JB}	Thermal resistance junction-board	**Thermal resistance junction-ambient** LQFP100 - 14 x 14 mm /0.5 mm pitch	36.3	°C/W
		Thermal resistance junction-ambient TFBGA100 - 8 x 8 mm /0.8 mm pitch	21.1	
		Thermal resistance junction-ambient LQFP144 - 20 x 20 mm /0.5 mm pitch	38.3	
		Thermal resistance junction-ambient UFBGA169 - 7 x 7 mm /0.5 mm pitch	17.3	
		Thermal resistance junction-ambient LQFP176 - 24 x 24 mm /0.5 mm pitch	39.4	
		Thermal resistance junction-ambient LQFP208 - 28 x 28 mm /0.5 mm pitch	40.3	
		Thermal resistance junction-ambient UFBGA176+25 - 10 x 10 mm /0.65 mm pitch	19.3	
		Thermal resistance junction-ambient TFBGA240+25 - 14 x 14 mm / 0.8 mm pitch	24.3	
Θ_{JC}	Thermal resistance junction-case	**Thermal resistance junction-ambient** LQFP100 - 14 x 14 mm /0.5 mm pitch	11.5	°C/W
		Thermal resistance junction-ambient TFBGA100 - 8 x 8 mm /0.8 mm pitch	17.1	
		Thermal resistance junction-ambient LQFP144 - 20 x 20 mm /0.5 mm pitch	11.3	
		Thermal resistance junction-ambient UFBGA169 - 7 x 7 mm /0.5 mm pitch	11	
		Thermal resistance junction-ambient LQFP176 - 24 x 24 mm /0.5 mm pitch	11.2	
		Thermal resistance junction-ambient LQFP208 - 28 x 28 mm /0.5 mm pitch	11.1	
		Thermal resistance junction-ambient UFBGA176+25 - 10 x 10 mm /0.65 mm pitch	23.9	
		Thermal resistance junction-ambient TFBGA240+25 - 14 x 14 mm / 0.8 mm pitch	7.4	

8.9.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.
- For information on thermal management, refer to application note “Thermal management guidelines for STM32 32-bit Arm Cortex MCUs applications” (AN5036) available from *www.st.com*.

9 Ordering information

Example: STM32 H 753 X I T 6 TR(1)

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

H = High performance

Device subfamily

753 = STM32H7x3 with cryptographic accelerator

Pin count

V = 100 pins

Z = 144 pins

A = 169 pins

I = 176 pins/balls

B = 208 pins

X = 240 balls

Flash memory size

I = 2 Mbytes

Package

T = LQFP ECOPACK2

K = UFBGA pitch 0.65 mm ECOPACK2

I = UFBGA pitch 0.5 mm ECOPACK2

H = TFBGA ECOPACK2

Temperature range

6 = –40 to 85 °C

Packing

TR = tape and reel

No character = tray or tube

1. The tape and reel packing is not available on all packages.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

10 Revision history

Table 230. Document revision history

Date	Revision	Changes
22-Jun-2017	1	Initial release.
27-Sep-2017	2	Updated list of features. Changed datasheet status to “production data”. Added UFBGA169 and TFBGA100 packages as well as notes related to TFBGA100 and UFBGA169 status on cover page and in *Table 2: STM32H753xI features and peripheral counts*. Differentiated number of GPIOs for each package in *Table 2: STM32H753xI features and peripheral counts*. Updated *Error code correction (ECC)* in *Section 3.3.3: Embedded SRAM*. Change PWR_CR3 into PWR_D3CR in *Section 3.5.1: Power supply scheme*. Updated *Section 3.12: Nested vectored interrupt controller (NVIC)*. Added *Table 4: DFSDM implementation* in *Section 3.23: Digital filter for sigma-delta modulators (DFSDM)*. Changed PC2/3 to PC2/3_C and VDD33USB to VDD in *Figure 4: LQFP100 pinout*. Changed PC2/3 to PC2/3_C in *Figure 6: LQFP144 pinout*. Changed PC2/3 to PC2/3_C in *Figure 8: LQFP176 pinout*. Changed PC2/3 to PC2/3_C in *Figure 10: LQFP208 pinout*. *Table 8: Pin/ball definition*: – Modified PA7, PC4, PC5, PB1, PG1, PE7, PE8 and PE9 I/O structure – TFBGA240 +25: removed duplicate occurrence of F1, F2 and P17 pin; added notes related to F1, F2, G2 pin connection; added note on E1, L16, L17, M16, M17, K16, K17, N17. – UFBGA176+25: changed G10 pin name to VSS. – Added note to VREF+ pin. Added current consumption corresponding to 125 °C ambient temperature in *Section 6.3.6: Supply current characteristics*. Replaced FMC_CLK by FMC_SDCLK in *Section : SDRAM waveforms and timings*. Changed description of the last five f_S values and updated $t_{LATRINJ}$in *Table 86: ADC characteristics*. For TFBGA100, TFBGA240+25 and UFBGA169, updated thermal resistance power-junction in *Table 229: Thermal characteristics* as well as power dissipation in *Table 23: General operating conditions*.
23-Oct-2017	3	Total current consumption changed to 4 µA minimum in *Features*. Updated *Figure 7: UFBGA169 ballout*. Updated dpad and dsm in *Table 228: TFBGA240+25 - Recommended PCB design rules (0.8 mm pitch BGA)*.

Table 230. Document revision history

Date	Revision	Changes
18-May-2018	4	Updated LSI clock frequency and ADC on cover page. Removed note related to UFBGA169 package. Updated ADC features on cover page and in *Table 2: STM32H753xI features and peripheral counts*. Added Arm trademark notice in *Section 1: Introduction*. Updated USB OTG interfaces to add crystal-less capability. Updated *Figure 1: STM32H753xI block diagram*. Updated GPIO default mode in *Section 3.8: General-purpose input/outputs (GPIOs)*. Added ADC sampling rate values in *Section 3.17: Analog-to-digital converters (ADCs)*. Updated *Section 3.18: Temperature sensor*. Updated LCD-TFT FIFO Size in *Section 3.25: LCD-TFT controller*. *Section 3.34: Serial peripheral interfaces (SPI)/integrated interchip sound interfaces (I2S)*: changed maximum SPI frequency to 150 Mbits/s. Modified number of bidirectional endpoints in *Section 3.41: Universal serial bus on-the-go high-speed (OTG_HS)*. *Table 8: Pin/ball definition*: – Updated PC14 and PC15 function after reset. – Changed CAN1_TX/RX to FDCAN1_TX/RX and CAN1_TXFD/RXFD to FDCAN1_TXFD_MODE/RXFD_MODE – Changed CAN2_TX/RX to FDCAN2_TX/RX and CAN2_TXFD/RXFD to FDCAN2_TXFD_MODE/RXFD_MODE Replaced VCAP1/2/3 and VDDLDO1/2/3 by VCAP and VDDLDO, respectively. Updated PA0, PA13, PA14, PC14 and PC15 pin/ball signals in pinout/ballout schematics. Replaced f_{ACLK} by $f_{rcc_c_ck}$ in *Section : Typical and maximum current consumption*. Replaced system clock by CPU clock and f_{ACLK} by $f_{rcc_c_ck}$ in *Section : On-chip peripheral current consumption*. Updated Note *2.* in *Table 26: Reset and power control block characteristics*. Updated *Table 27: Embedded reference voltage*, *Table 29: Typical and maximum current consumption in Run mode, code with data processing running from ITCM, regulator ON*, *Table 30: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, cache ON, regulator ON* and *Table 35: Typical and maximum current consumption in Stop mode, regulator ON*. Updated typical and maximum current consumption in *Table 36: Typical and maximum current consumption in Standby mode* and *Table 37: Typical and maximum current consumption in VBAT mode*. Added note to f_{LSI} in *Table 48: LSI oscillator characteristics*.

Table 230. Document revision history

Date	Revision	Changes
18-May-2018	4 (continued)	Updated *Figure 21: VIL/VIH for all I/Os except BOOT0*. Added note in *Table 83: QUADSPI characteristics in SDR mode*, *Table 84: QUADSPI characteristics in DDR mode* and *Table 85: Dynamics characteristics: Delay Block characteristics*. *Section 6.3.20: 16-bit ADC characteristics*: updated THD conditions in *Table 87: ADC accuracy*; removed formula to compute R_{AIN}. Changed decoupling capacitor value to 100 nF in *Section : General PCB design guidelines*. Added note in *Table 88: DAC characteristics*, *Table 96: Voltage booster for analog switch characteristics*, *Table 99: DFSDM measured timing - 1.62-3.6 V*, *Table 116: Dynamics JTAG characteristics* and *Table 117: Dynamics SWD characteristics*. Updated *Figure 127: LQFP144 marking example (package top view)*, *Figure 133: LQFP176 marking example (package top view)* and *Figure 136: LQFP208 marking example (package top view)*. Updated TFBGA240+25 package information to final mechanical data.
13-Jul-2018	5	Added description of power-up and power-down phases in *Section 3.5.1: Power supply scheme*. Removed ETH_TX_ER from *Table 8: Pin/ball definition* and *Table 9: Port A alternate functions* to *Table 19: Port K alternate functions*. Added note related to decoupling capacitor tolerance below *Figure 14: Power supply scheme*. Added note *2.* related to CEXT in *Table 24: VCAP operating conditions*. Updated *Table 45: HSI48 oscillator characteristics*, *Table 46: HSI oscillator characteristics* and *Table 47: CSI oscillator characteristics*. Renamed *Table 49* into “PLL characteristics (wide VCO frequency range)” and updated note *2.*. Added *Table 50: PLL characteristics (medium VCO frequency range)*. Updated T_{coeff} in *Table 90: VREFBUF characteristics*. Updated t_{S_vbat} in *Table 93: V_{BAT} monitoring characteristics*. Updated *Table 98: OPAMP characteristics*.

Table 230. Document revision history

Date	Revision	Changes
05-Apr-2019	6	Changed maximum Arm Core-M7 frequency to 480 MHz. *Features*: – Changed operational amplifier bandwidth to 7.3 MHz – Updated high-resolution timer to 2.1 ns – Updated low-power consumption feature Changed FMC NOR/NAND maximum clock frequency to 100 MHz in *Features* and *Synchronous waveforms and timings*. Updated voltage scaling in *Section 3.5.1: Power supply scheme*. Added VOS0 in *Section 3.5.3: Voltage regulator*. Updated HSE clock in *Section 3.7.1: Clock management*. Added note related to VDDLDO in *Table 8: Pin/ball definition*. Updated *Section 6: Electrical characteristics (rev Y)*: – Added note *2.* related to CEXT in *Table 24: VCAP operating conditions* – Updated f_{HSI48} in *Table 45: HSI48 oscillator characteristics*. – Updated t_{stab} in *Table 46: HSI oscillator characteristics*. – Added *Table 61: Output voltage characteristics for PC13, PC14, PC15 and PI8*. – Updated *Table 59: I/O static characteristics* and *Figure 21: VIL/VIH for all I/Os except BOOT0*. – Added note related to PC13, PC14, PC15 an PI8 limited frequency in *Table 62: Output timing characteristics (HSLV OFF)*. – Updated note 2 below *Figure 22: Recommended NRST pin protection*. – *Table 86: ADC characteristics*: updated f_S and added note related to f_S formula; updated t_{CAL}. – Renamed *Section 6.3.24* into *Temperature and VBAT monitoring* and content updated. – Updated $f_{DFSDMCLK}$ in *Table 99: DFSDM measured timing - 1.62-3.6 V*. Added *Section 7: Electrical characteristics (rev V)*. *Section 8: Package information*: – Updated paragraph introducing all package marking schematics to add the new sentence “The printed markings may differ depending on the supply chain.” – Added *Section : Device marking for TFBGA100* and *Section : Device marking for UFBGA169*. – Updated *Table 229: Thermal characteristics*. Added note related to ECOPACK®2 compliance in *Table 9: Ordering information*.
24-Apr-2019	7	Updated *Figure 1: STM32H753xI block diagram* Updated *Table 8: Pin/ball definition*. Updated *Table 9* to *Table 19* (alternate functions). Updated *Table 38: Peripheral current consumption in Run mode*. Updated *Table 136: Peripheral current consumption in Run mode*. Updated *Table 183: ADC characteristics*. Updated *Table 184: Minimum sampling time vs RAIN*. Updated *Table 185: ADC accuracy*.

Table 230. Document revision history

Date	Revision	Changes
4-Mar-2022	8	Added reference to errata sheet ES0392 in *Section 1: Introduction*. ***Section 2: Description*** *Table 2: STM32H753xI features and peripheral counts*: removed note indicating that packages are under development, split number of ADC channels into Direct, Fast and Slow channels; and added number of wakeup and tamper pins. Changed APB1 and APB2 maximum frequency to 120 MHZ in *Figure 1: STM32H753xI block diagram*. ***Section 3: Functional overview*** Added connection between SDMMC2 and D2-to-D3 AHB bus in *Figure 3: STM32H753xI bus matrix*. Updated *Section 3.27: True random number generator (RNG)*. Added Full-duplex mode in *Section 3.34: Serial peripheral interfaces (SPI)/integrated interchip sound interfaces (I2S)*. Updated number of microphones that can be supported by the SAI in *Section 3.35: Serial audio interfaces (SAI)*. ***Section 5: Pin descriptions*** Updated J1, F1, F2 and G2 signals and added notes 2, 3 and 4 in *Figure 11: TFBGA240+25 ballout*. Removed FDCAN1_RXFD_MODE, FDCAN1_TXFD_MODE, FDCAN2_RXFD_MODE and FDCAN2_TXFD_MODE functions from *Table 8: Pin/ball definition* and all alternate function tables. Additional modifications made on *Table 8: Pin/ball definition*: added note to VDD50USB, change PB1 I/O structure to TT_a, replaced PI8 WKUP3 additional function by WKUP2, replaced PC13 WKUP2 additional function by WKUP3, changed F1 and G2 to VSS. ***Section 6: Electrical characteristics (rev Y)*:** – Updated *Section 6.2: Absolute maximum ratings* introduction to add device mission profile. – Updated *Figure 14: Power supply scheme*. – Power dissipation (P_D) removed from *Table 23: General operating conditions* since this parameter is redundant with Θ_{JA} thermal resistance. – Updated *Table 41: High-speed external user clock characteristics*. – *Table 52: Flash memory programming*: removed reference to single bank configuration in title and updated $t_{ERASE128KB}$ typical and maximum values. – Added reference to AN4899 in *Section 6.3.15: I/O port characteristics*. Updated F_{max} for speed 10 and 11 in *Table 62: Output timing characteristics (HSLV OFF)*. Updated notes in *Table 63: Output timing characteristics (HSLV ON)*. – Updated $t_{su(DV-CLKH)}$/$t_{h(DV-CLKH)}$ and $t_{su(NWAIT-CLKH)}$/$t_{h(NWAIT-CLKH)}$ in *Table 73: Synchronous multiplexed NOR/PSRAM read timings*. Changed $t_{(NWAIT-CLKH)}$ to $t_{su(NWAIT-CLKH)}$ and updated $t_{su(DV-CLKH)}$/$t_{h(DV-CLKH)}$ and $t_{su(NWAIT-CLKH)}$/$t_{h(NWAIT-CLKH)}$ in *Table 75: Synchronous non-multiplexed NOR/PSRAM read timings*. – Replaced FMC_CLK by FMC_SDCLK in *Section : SDRAM waveforms and timings* – Updated $t_{su(SDCLKH_Data)}$ and $t_{h(SDCLKH_Data)}$ in *Table 79: SDRAM read timings* and *Table 80: LPSDR SDRAM read timings*.

Table 230. Document revision history

Date	Revision	Changes
4-Mar-2022	8 (continued)	***Section 6: Electrical characteristics (rev Y)*** **(continued)** – Updated $t_{s(IN)}$ and $t_{h(IN)}$ in *Table 83: QUADSPI characteristics in SDR mode* $t_{sr(IN)}/t_{sf(IN)}$ and $t_{hr(IN)}/t_{hf(IN)}$ in *Table 84: QUADSPI characteristics in DDR mode*. Updated *Figure 38: Quad-SPI timing diagram - DDR mode*. – Updated maximum sampling time (t_S) value in *Table 86: ADC characteristics*. Updated *Figure 39: ADC accuracy characteristics*, *Figure 40: Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function* and *Figure 41: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})*. – Updated T_L maximum value in *Table 91: Temperature sensor characteristics*. – Updated $f_{DFSDMCLK}$ and $DuCy_{CKOUT}$ in *Table 99: DFSDM measured timing - 1.62-3.6 V*. – Updated $f_{TIMxCLK}$ to match an APB1/2 maximum frequency of 120 MHZ in *Table 102: TIMx characteristics*. – Updated $t_{su(MI)}$ and $t_{h(MI)}$ minimum values in *Table 105: SPI dynamic characteristics*. – Updated t_{ISU}, t_{IH}, t_{ISUD} and t_{IHD} in *Table 109: Dynamic characteristics: SD / MMC characteristics, VDD = 2.7 to 3.6 V*, and t_{ISU}, t_{IH} in *Table 110: Dynamic characteristics: eMMC characteristics, VDD = 1.71 to 1.9 V*. Updated *Figure 58: DDR mode*. ***Section 7: Electrical characteristics (rev V)*****:** – Updated *Figure 67: Power supply scheme*. – Updated *Section 7.2: Absolute maximum ratings* introduction to device mission profile. – Power dissipation (P_D) removed from *Table 121: General operating conditions* since this parameter is redundant with Θ_{JA} thermal resistance. – Replaced Min V_{DD} by Min V_{DDLDO} in *Table 122: Supply voltage and maximum frequency configuration*. – Updated *Table 138: High-speed external user clock characteristics*. – *Table 149: Flash memory programming*: removed reference to single bank configuration in title, and updated $t_{ERASE128KB}$. – Updated condition related to $f_{rcc_c_ck}$ in *Section : On-chip peripheral current consumption*. – Added reference to AN4899 in *Section 7.3.15: I/O port characteristics*. Updated F_{max} for speed 10 and 11 in *Table 159: Output timing characteristics (HSLV OFF)*. Changed capacitance value for speed 10 and t_r/t_f, and speed for 11 and $t_r/t_f/F_{max}$ *Table 160: Output timing characteristics (HSLV ON)*. – Updated $t_{su(DV-CLKH)}/t_{h(DV-CLKH)}$ and $t_{su(NWAIT-CLKH)}/t_{h(NWAIT-CLKH)}$ in *Table 170: Synchronous multiplexed NOR/PSRAM read timings*. Changed $t_{(NWAIT-CLKH)}$ to $t_{su(NWAIT-CLKH)}$ and updated $t_{su(DV-CLKH)}/t_{h(DV-CLKH)}$ and $t_{su(NWAIT-CLKH)}/t_{h(NWAIT-CLKH)}$ in *Table 172: Synchronous non-multiplexed NOR/PSRAM read timings*. Updated $t_{su(SDCLKH_Data)}$ and $t_{h(SDCLKH_Data)}$ in *Table 176: SDRAM read timings* and *Table 177: LPSDR SDRAM read timings*. Replaced FMC_CLK by FMC_SDCLK in *Section : SDRAM waveforms and timings*. – Updated $t_{s(IN)}$ and $t_{h(IN)}$ in *Table 180: QUADSPI characteristics in SDR mode* and $t_{sr(IN)}/t_{sf(IN)}$ and $t_{hr(IN)}/t_{hf(IN)}$ in *Table 181: QUADSPI characteristics in DDR mode*. Updated *Figure 90: Quad-SPI timing diagram - DDR mode*.

Table 230. Document revision history

Date	Revision	Changes
4-Mar-2022	8 (continued)	***Section 7: Electrical characteristics (rev V)*** **(continued):** – Updated notes *4.* and *5.* in *Table 184: Minimum sampling time vs RAIN*. Added reference to AN5354 application note in note of *Table 183: ADC characteristics*. Updated *Figure 91: ADC accuracy characteristics* and *Figure 92: Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function* – Changed V_{DAC_OUT} maximum value to V_{REF+} −0.2 in *Table 186: DAC characteristics* – Updated T_L maximum value in*Table 189: Temperature sensor characteristics*. – Modified *Figure 93: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})*. – Updated $DuCy_{CKOUT}$ in *Table 197: DFSDM measured timing - 1.62-3.6 V*. – Updated *Figure 100: USART timing diagram in Master mode* and *Figure 101: USART timing diagram in Slave mode* – Updated $t_{su(MI)}$ and $t_{h(MI)}$ in *Table 204: SPI dynamic characteristics*. – Updated t_{ISU}, t_{IH}, t_{ISUD}, t_{IHD} and t_{OH} in *Table 208: Dynamics characteristics: SD / MMC characteristics, VDD = 2.7 to 3.6 V*, and t_{ISU}, t_{IH} in *Table 209: Dynamics characteristics: eMMC characteristics VDD = 1.71V to 1.9V*. Modified *Figure 112: DDR mode*. – Added *Section : USB OTG_FS characteristics*. ***Section 8: Package information*** Added Θ_{JB} and Θ_{JC} for UFBGA169. Updated *Section 8.1: LQFP100 package information*, *Section 8.3: LQFP144 package information*, *Figure 123: TFBGA100 - Recommended footprint*, *Section 8.5: LQFP176 package information*, *Section 8.7: UFBGA176+25 package information*, *Figure 136: LQFP208 marking example (package top view)* and *Table 228: TFBGA240+25 - Recommended PCB design rules (0.8 mm pitch BGA)*. Added *Figure 129: UFBGA169 - Recommended footprint* and *Table 222: UFBGA169 - Recommended PCB design rules (0.5 mm pitch BGA)*. ***Section 9: Ordering information*** Added note related to the availability of tape and reel packing in *Section 9: Ordering information*.

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