THE DATASHEET OF

LT3782AEUFD#PBF

2-Phase Step-Up DC/DC Controller

FEATURES

- **2-Phase Operation Reduces Required Input and Output Capacitance**
- **Programmable Switching Frequency: 150kHz to 500kHz**
- **6V to 40V Input Range**
- **10V Gate Drive with V_{CC} ≥13V**
- **High Current Gate Drive (4A)**
- Programmable Soft-Start and Current Limit
- Programmable Slope Compensation for High Noise Immunity
- MOSFET Gate Signals with Programmable Falling Edge Delay for External Synchronous Drivers
- Programmable Undervoltage Lockout
- Programmable Duty Cycle Clamp (50% or Higher)
- Thermally Enhanced 28-Lead TSSOP and 4mm × 5mm QFN Packages

APPLICATIONS

- Industrial Equipment
- Telecom Infrastructure
- Interleaved Isolated Power Supply

DESCRIPTION

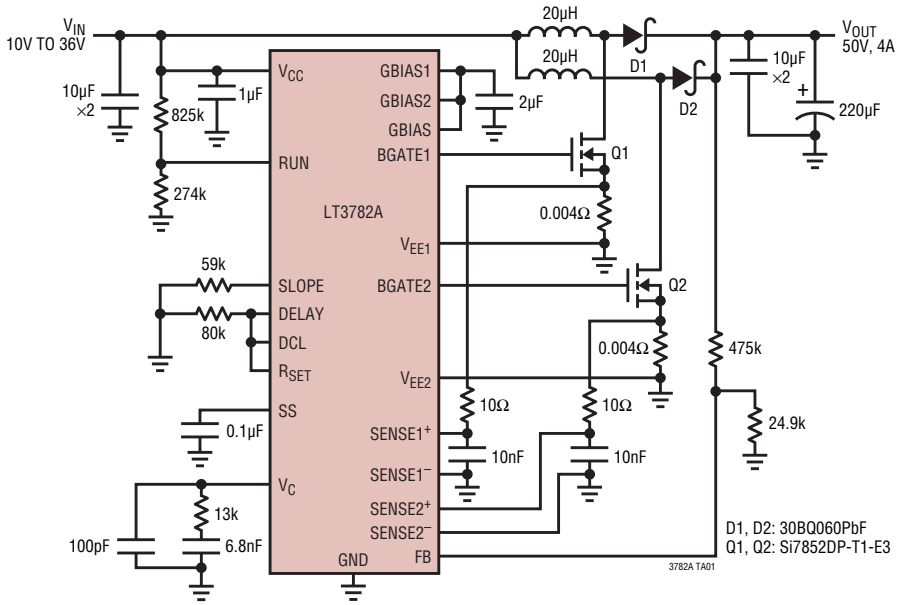
The LT®3782A is a current mode 2-phase step-up DC/DC converter controller. Its high switching frequency (up to 500kHz) and 2-phase operation reduce system filtering capacitance and inductance requirements.

With 10V gate drive (V_{CC} ≥13V) and 4A peak drive current, the LT3782A can drive most industrial grade high power MOSFETs with high efficiency. For synchronous applications, the LT3782A provides synchronous gate signals with programmable falling edge delay to avoid cross conduction when using external MOSFET drivers. Other features include programmable undervoltage lockout, soft-start, current limit, duty cycle clamp (50% or higher) and slope compensation. The LT3782A is identical to the LT3782 except that the LT3782A has a tighter current sense mismatch tolerance.

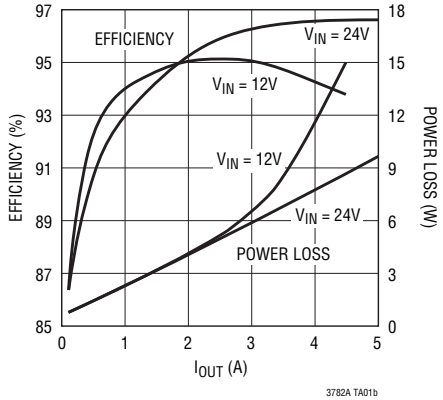
The LT3782A is available in thermally enhanced 28-lead TSSOP and 4mm × 5mm QFN packages.

TYPICAL APPLICATION

50V 4A Boost Converter



Efficiency and Power Loss vs Load Current

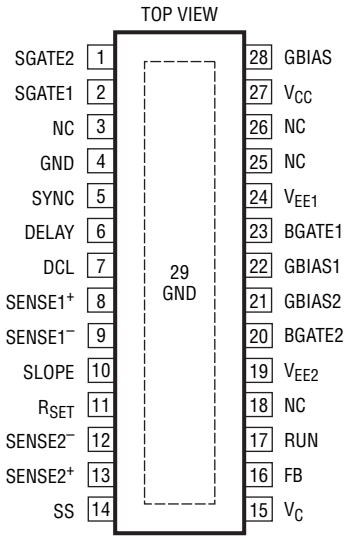


ABSOLUTE MAXIMUM RATINGS (Note 1)

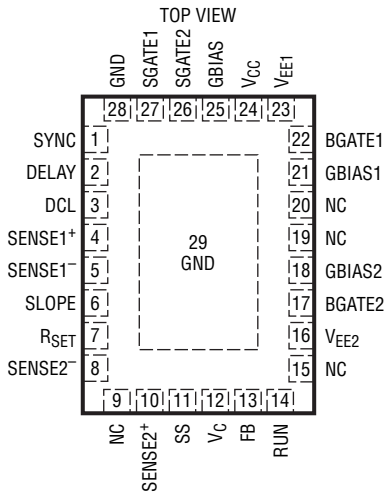
V_{CC} Supply Voltage 40V
GBIAS, GBIAS1, GBIAS2 Pin
(Externally Forced) 14V
SYNC, RUN Pin 30V
Operating Junction Temperature
Range (Notes 2, 3) ..... –40°C to 125°C

SS ..... 300µA Max I_{SS}
SENSE1+, SENSE2+,
SENSE1–, SENSE2– ..... –0.3V to 2V
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
For FE Package ..... 300°C

PIN CONFIGURATION



FE PACKAGE
28-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 30°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3782AEFE#PBF	LT3782AEFE#TRPBF	LT3782AFE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3782AIFE#PBF	LT3782AIFE#TRPBF	LT3782AFE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3782AEUFD#PBF	LT3782AEUFD#TRPBF	3782A	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3782AIUFD#PBF	LT3782AIUFD#TRPBF	3782A	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3782AEFE	LT3782AEFE#TR	LT3782AFE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3782AIFE	LT3782AIFE#TR	LT3782AFE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3782AEUFD	LT3782AEUFD#TR	3782A	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3782AIUFD	LT3782AIUFD#TR	3782A	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{CC} = 13V, R_{SET} = 80k, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overall						
Supply Voltage (V_{CC})		●	6		40	V
Supply Current (I_{VCC})	$V_C \le 0.5V$ (Switching Off), $V_{CC} \le 40V$			11	16	mA
Shutdown						
RUN Threshold		●	2.3	2.44	2.6	V
RUN Threshold Hysteresis				80		mV
Supply Current in Shutdown	$1V \le RUN \le V_{REF}$ $RUN \le 0.3V$, $V_{CC} \le 30V$			0.4 40	0.65 90	mA µA
RUN Pin Input Current	V_{RUN} = 2.3V	●		–0.5	–2	µA
Voltage Amplifier g_m						
Reference Voltage (V_{REF})		 ●	2.42 2.4	2.44	2.464 2.488	V V
Transconductance	V_{VC} = 1V, ΔI_{VC} = ±2µA	●	200	260	370	µmho
Input Current I_{FB}	$V_{FB} = V_{REF}$	●		0.2	0.6	µA
V_C High	I_{VC} = 0			1.5		V
V_C Low	I_{VC} = 0			0.35	0.4	V
Source Current I_{VC}	V_{VC} = 0.7V – 1V, $V_{FB} = V_{REF}$ – 100mV		8	11	14	µA
Sink Current I_{VC}	V_{VC} = 0.7V – 1V, $V_{FB} = V_{REF}$ + 100mV		13	20	28	µA
V_C Threshold for Switching Off (BGATE1, BGATE2 Low)		●	0.3			V
Soft-Start Current I_{SS}	V_{SS} = 0.1V – 2.8V		6	10	15	µA
Current Amplifier CA1, CA2						
Voltage Gain $\Delta V_C/\Delta V_{SENSE}$				4		
Current Limit ($V_{SENSE1}^+ - V_{SENSE1}^-$) ($V_{SENSE2}^+ - V_{SENSE2}^-$)	V_{FB} = 2.3V		55	63	70	mV
Current Limit Mismatch	($\Delta V_{SENSE1} - \Delta V_{SENSE2}$), V_{FB} = 2.3V		–10		10	mV
Input Current (I_{SENSE1}^+, I_{SENSE1}^-, I_{SENSE2}^+, I_{SENSE2}^-)	ΔV_{SENSE} = 0V			60		µA
Oscillator						
Switching Frequency	R_{SET} = 130k R_{SET} = 80k R_{SET} = 40k	● ● ●	130 212 386	154 250 465	177 288 533	kHz kHz kHz
Synchronization Pulse Threshold on SYNC Pin	Rising Edge V_{SYNC}		0.8	1.2	2	V
Synchronization Frequency Range (Note: Operation Switching Frequency Equals Half of the Synchronization Frequency)	R_{SET} = 130k R_{SET} = 80k R_{SET} = 40k		180 290 550		240 392 715	kHz kHz kHz
V_{RSET}	R_{SET} = 80k			2.3		V
Maximum Duty Cycle	$V_{FB} = V_{REF}$ – 25mV, R_{SET} > 80k R_{SET} = 40k	● ●	90 83	94 90		% %
Duty Cycle Limit	R_{SET} = 80k, $V_{DCL} \le 0.3V$ V_{DCL} = 1.2V $V_{DCL} = V_{RSET}$			50 75 Max Duty Cycle		% %
DCL Pin Input Current	$V_{DCL} \le 0.3V$	●		–0.1	–0.3	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{CC} = 13V, R_{SET} = 80k, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Driver						
V_{GBIAS}	I_{GBIAS} < 70mA	●	10.2	11	11.7	V
BGATE1, BGATE2 High Voltage	13V ≤ V_{CC} ≤ 24V, I_{BGATE} = –100mA V_{CC} = 8V, I_{BGATE} = –100mA	● ●	7.8 3.8	9.2 5	10.5	V V
BGATE1, BGATE2 Source Current (Peak)	Capacitive Load >22µF Capacitive Load >50µF			3 4		A A
BGATE1, BGATE2 Low Voltage	8V ≤ V_{CC} ≤ 24V, I_{BGATE} = 100mA	●		0.5	0.7	V
BGATE1, BGATE2 Sink Current (Peak)	Capacitive Load >22µF Capacitive Load >50µF			3 4		A A
SGATE1, SGATE2 High Voltage	8V ≤ V_{CC} ≤ 24V, I_{SGATE} = –20mA	●	4.5	5.5	6.7	V
SGATE1, SGATE2 Low Voltage	8V ≤ V_{CC} ≤ 24V, I_{SGATE} = 20mA			0.5	0.7	V
SGATE1, SGATE2 Peak Current	500pF Load			100		mA
Delay of BGATE High	DELAY Pin and R_{SET} Pin Shorted V_{DELAY} = 1V V_{DELAY} = 0.5V V_{DELAY} = 0.25V			100 150 250 500		ns ns ns ns
Delay Pin Input Current	V_{DELAY} = 0.25V	●		–0.1	–0.3	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

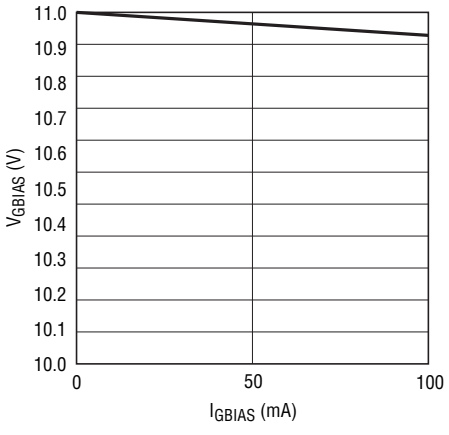
Note 2: The LT3782AE is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3782AI is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

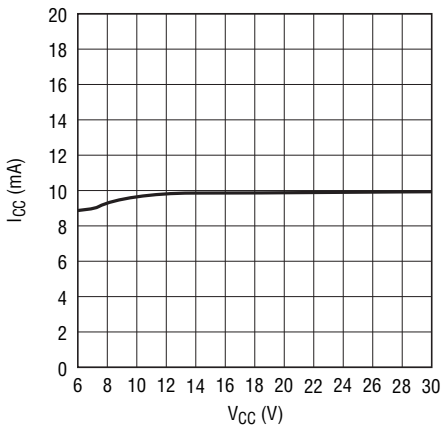
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless otherwise noted.

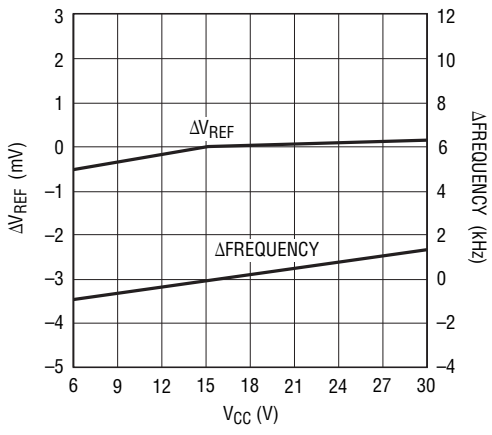
V_{GBIAS} vs I_{GBIAS}



I_{CC} vs V_{CC}

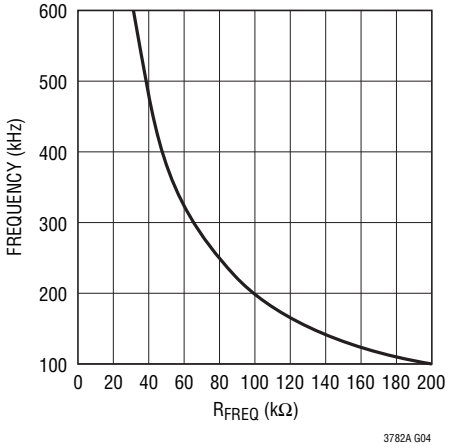


ΔV_{REF} vs V_{CC}, ΔFrequency vs V_{CC} (R_{SET} = 80k)

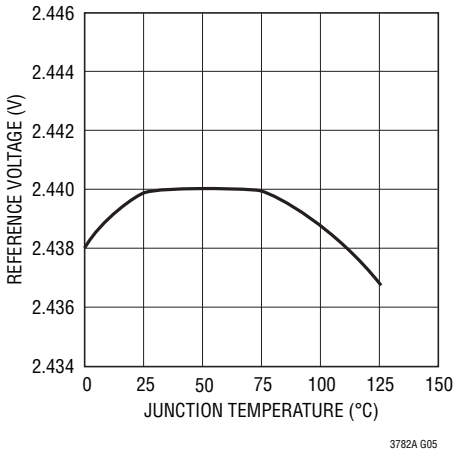


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

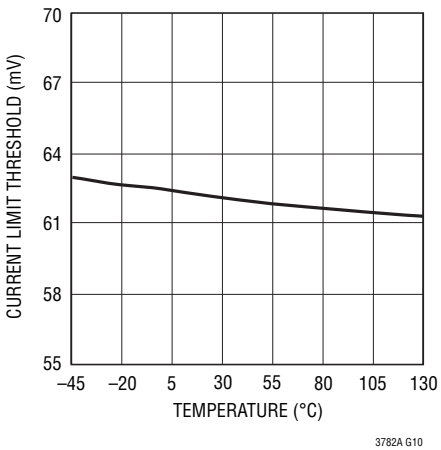
Switching Frequency vs R_{FREQ}



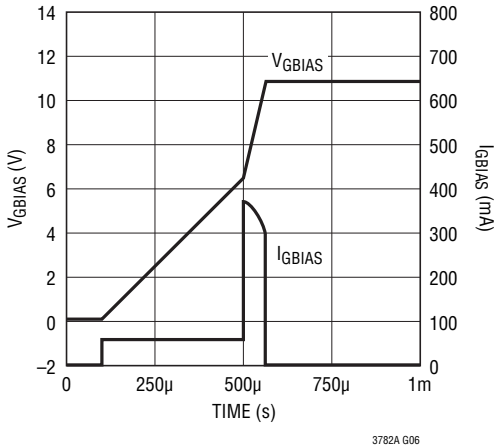
Reference Voltage vs Temperature



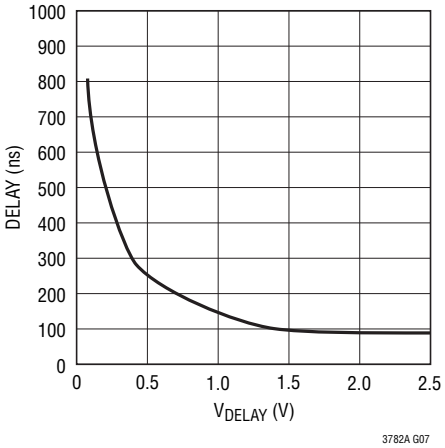
Current Limit Threshold vs Temperature



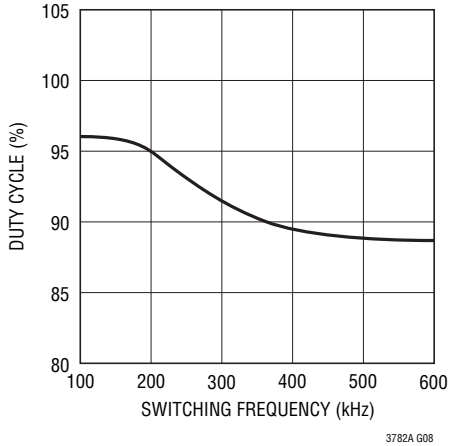
V_{GBIAS} vs I_{GBIAS} at Start-Up (Charging 2µF)



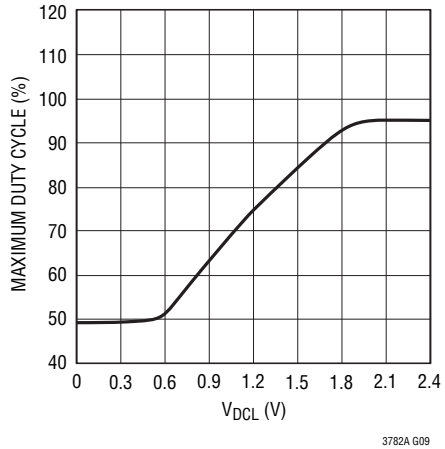
SGATE (Low) to BGATE (High) Delay vs V_{DELAY} (R_{SET} = 80k)



Switching Frequency vs Duty Cycle



Maximum Duty Cycle Limit vs V_{DCL} (R_{SET} = 80k)



PIN FUNCTIONS (FE/UFD)

SGATE2 (Pin 1/Pin 26): Second Phase Synchronous Drive Signal. An external driver buffer is needed to drive the top synchronous power FET.

SGATE1 (Pin 2/Pin 27): First Phase Synchronous Drive Signal. An external driver buffer is needed to drive the top synchronous power FET.

GND (Pin 4, Exposed Pad Pin 29/Pin 28, Exposed Pad Pin 29): Ground. Solder the exposed pad to the PCB ground plane for rated thermal performance. The exposed pad should be connected to the GND pin as close to the IC as possible.

SYNC (Pin 5/Pin 1): Synchronization Input. The pulse width can range from 10% to 70%. Note that the operating frequency is half of the sync frequency.

DELAY (Pin 6/Pin 2): When synchronous drivers are used, the programmable delay that delays BGATE turns on after SGATE turns off.

DCL (Pin 7/Pin 3): This pin programs the limit of the maximum duty cycle. When connected to V_{RSET}, it operates at natural maximum duty cycle, approximately 90%.

SENSE1$^+$ (Pin 8/Pin 4): First Phase Current Sense Amplifier Positive Input. An RC filter is required across the current sense resistor. Current limit threshold is set at 63mV.

SENSE1$^-$ (Pin 9/Pin 5): First Phase Current Sense Amplifier Negative Input.

SLOPE (Pin 10/Pin 6): A resistor from SLOPE to GND increases the internal current mode PWM slope compensation.

R_{SET} (Pin 11/Pin 7): A resistor from R_{SET} to GND sets the oscillator charging current and the operating frequency.

SENSE2$^-$ (Pin 12/Pin 8): Second Phase Current Sense Amplifier Negative Input.

SENSE2$^+$ (Pin 13/Pin 10): Second Phase Current Sense Amplifier Positive Input. An RC filter is required across the current sense resistor. Current limit threshold is set at 63mV.

SS (Pin 14/Pin 11): Soft-Start. A capacitor on this pin sets the output ramp up rate. The typical time for SS to reach the programmed level is (C • 2.44V)/10µA.

V_C (Pin 15/Pin 12): The output of the g_m error amplifier and the control signal of the current loop of the current-mode PWM. Switching starts at 0.7V, and higher V_C voltages corresponds to higher inductor current.

FB (Pin 16/Pin 13): Error Amplifier Inverting Input. A resistor divider to this pin sets the output voltage.

RUN (Pin 17/Pin 14): LT3782A goes into shutdown mode when V_{RUN} is below 2.3V and goes to low bias current shutdown mode when V_{RUN} is below 0.3V.

V_{EE2} (Pin 19/Pin 16): Gate Driver BGATE2 Ground. This pin should be connected to ground as close to the IC as possible.

BGATE2 (Pin 20/Pin 17): Second Phase MOSFET Driver.

GBIAS2 (Pin 21/Pin 18): Bias for Gate Driver BGATE2. Should be connected to GBIAS or an external power supply between 12V to 14V.

GBIAS1 (Pin 22/Pin 21): Bias for Gate Driver BGATE1. Should be connected to GBIAS2.

BGATE1 (Pin 23/Pin 22): First Phase MOSFET Driver.

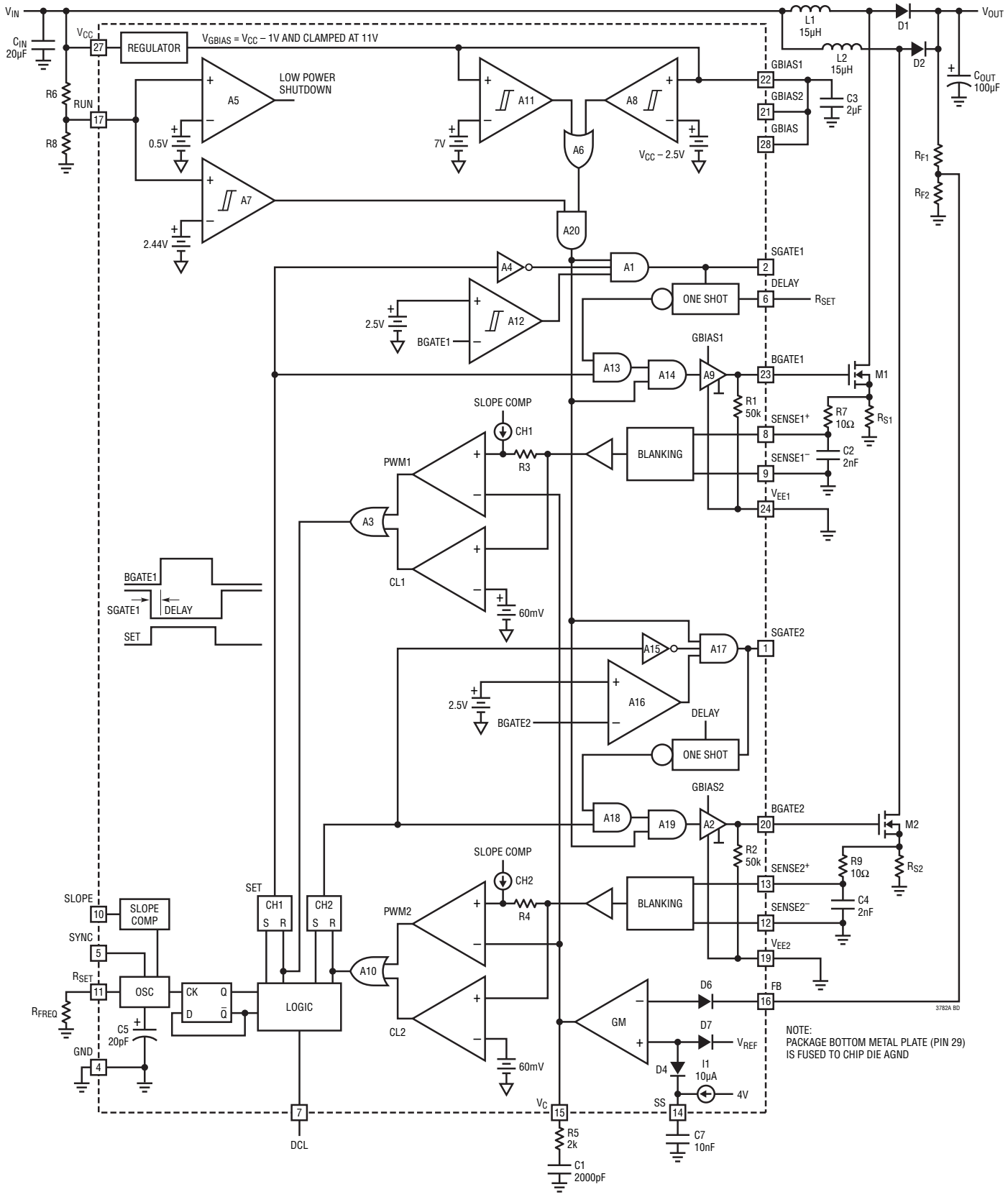
V_{EE1} (Pin 24/Pin 23): Gate Driver BGATE1 Ground. This pin should be connected to ground as close to the IC as possible.

V_{CC} (Pin 27/Pin 24): Chip Power Supply. Good supply bypassing is required.

GBIAS (Pin 28/Pin 25): Internal 11V regulator output for biasing internal circuitry. Should be connected to GBIAS1 and GBIAS2. A bypass low ESR capacitor of 2µF or larger is needed and should be connected directly to the pin to minimize parasitic impedance.

NC (Pins 3, 18, 25, 26/Pins 9, 15, 19, 20): Not Connected. Can be connected to GND.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Operation

The LT3782A is a two phase constant frequency current mode boost controller. Switching frequency can be programmed up to 500kHz. During normal switching cycles, the two channels are controlled by internal flip-flops and are 180 degrees out-of-phase.

Referring to the Block Diagram, the LT3782A's basic functions include a transconductance amplifier (g_m) to regulate the output voltage and to control the current mode PWM current loop. It also includes the necessary logic and flip-flop to control the PWM switching cycles, two high speed gate drivers to drive high power N-channel MOSFETs, and 2-phase control signals to drive external gate drivers for optional synchronous operation.

In normal operation, each switching cycle starts with a switch turn-on. The inductor current of each channel is sampled through the current sense resistor and amplified then compared to the error amplifier output V_C to turn the switch off. The phase delay of the second channel is controlled by the divide-by-two D flip-flop and is exactly 180 degrees out-of-phase of the first channel. With a resistor divider connected to the FB pin, the output voltage is programmed to the desired value. The 10V gate drivers are sufficient to drive most high power N-channel MOSFET in many industrial applications.

Additional important features include shutdown, current limit, soft-start, synchronization and programmable maximum duty cycle. Additional slope compensation can be added also.

Output Voltage Programming

With a 2.44V feedback reference voltage V_{REF}, the output V_{OUT} is programmed by a resistor divider as shown in the Block Diagram.

$$V_{OUT} = 2.44\left(1+\frac{R_{F1}}{R_{F2}}\right)$$

Soft-Start and Shutdown

During soft-start, the voltage on the SS pin (V_{SS}) controls the output voltage. The output voltage thus ramps up following V_{SS}. The effective range of V_{SS} is from 0V to 2.44V. The typical time for the output to reach the programmed level is:

$$t = \frac{C \bullet 2.44V}{10\mu A}$$

C is the capacitor connected from the SS pin to GND.

Undervoltage Lockout and Shutdown

Only when V_{RUN} is higher than 2.45V V_{GBIAS} will be active and the switching enabled. The LT3782A goes into low current shutdown when V_{RUN} is below 0.3V. A resistor divider can be used on RUN pin to set the desired V_{CC} undervoltage lockout voltage. 80mV of hysteresis is built in on RUN pin thresholds.

Oscillation Frequency Setting and Synchronization

The switching frequency of LT3782A can be set up to 500kHz by a resistor R_{FREQ} from pin R_{SET} to ground.

For f_{SET} = 250kHz, R_{FREQ} = 80k

Once the switching frequency f_{SET} is chosen, R_{FREQ} can be found from the Switching Frequency vs R_{FREQ} graph found under the Typical Performance Characteristics section.

Note that because of the 2-phase operation, the internal oscillator is running at twice the switching frequency. To synchronize the LT3782A to the system frequency f_{SYSTEM}, the synchronizing frequency f_{SYNC} should be two times f_{SYSTEM}, and the LT3782A switching frequency f_{SET} should be set below 80% of f_{SYSTEM}.

$f_{SYNC} = 2f_{SYSTEM}$ and $f_{SET} < (f_{SYSTEM} \bullet 0.8)$

For example, to synchronize the LT3782A to 200kHz system frequency f_{SYSTEM}, f_{SYNC} needs to be set at 400kHz and f_{SET} needs to be set at 160kHz. From the Switching Frequency vs R_{FREQ} graph found under the Typical Performance Characteristics section, R_{FREQ} = 130k.

APPLICATIONS INFORMATION

With a 200ns one-shot timer on chip, the LT3782A provides flexibility on the external sync pulse width. The sync pulse threshold is about 1.2V (Figure 1). This pin can be floated when the sync function is not used.

Current Limit

Current limit is set by the 63mV threshold across SEN1P, SEN1N for channel one and SEN2P, SEN2N for channel two. By connecting an external resistor R_S (see Block Diagram), the current limit is set for 63mV/R_S. R_S should be placed very close to the power switch with very short traces. A low pass R_C filter is needed across R_S to filter out the switching spikes. Good Kelvin sensing is required for accurate current limit. The input bypass capacitor ground should be at the same ground point of the current sense resistor to minimize the ground current path.

Synchronous Rectifier Switches

For high output voltage applications, the power loss of the catch diodes are relatively small because of high duty cycle. If diodes power loss or heat is a concern, the LT3782A provides PWM signals through SGATE1 and SGATE2 pins to drive external MOSFET drivers for synchronous rectifier operation. Note that SGATE drives the top switch and BGATE drives the bottom switch. To avoid cross conduction between top and bottom switches, the BGATE turn-on is delayed 100ns (when DELAY pin is tied to R_{SET} pin) from SGATE turn-off (see Figure 2). If a longer delay is needed to compensate for the propagation delay of external gate driver, a resistor divider can be used from R_{SET} to ground to program V_{DELAY} for the longer delay needed. For example, for a switching frequency of 250kHz and delay of 150ns, then R_{FREQ1} + R_{FREQ2} should be 80k and V_{DELAY} should be 1V, with V_{RSET} = 2.3V then R_{FREQ1} = 47.5k and R_{FREQ2} = 32.5k (see Figure 3).

Duty Cycle Limit

When DCL pin is shorted to R_{SET} pin and switching frequency is less than 250kHz (R_{FREQ} > 80k), the maximum duty cycle of LT3782A will be at least 90%. The maximum duty cycle can be clamped to 50% by grounding the DCL pin or to 75% by forcing the V_{DCL} voltage to 1.2V with a resistor divider from R_{SET} pin to ground. The typical DCL pin input current is 0.1µA.

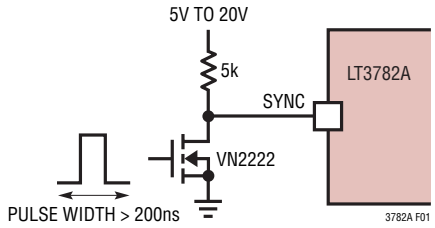


Figure 1. Synchronizing with External Clock

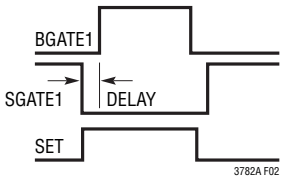


Figure 2. Delay Timing

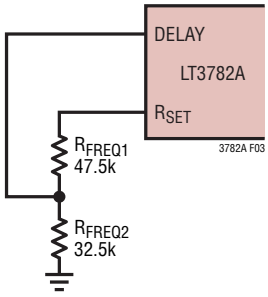


Figure 3. Increase Delay Time

APPLICATIONS INFORMATION

Slope Compensation

The LT3782A is designed for high voltage and/or high current applications, and very often these applications generate noise spikes that can be picked up by the current sensing amplifier and cause switching jitter. To avoid switching jitter, careful layout is absolutely necessary to minimize the current sensing noise pickup. Sometimes increasing slope compensation to overcome the noise can help to reduce jitter. The built-in slope compensation can be increased by adding a resistor R_{SLOPE} from SLOPE pin to ground. Note that smaller R_{SLOPE} increases slope compensation and the minimum R_{SLOPE} allowed is $R_{FREQ}/2$.

Layout Considerations

To prevent EMI, the power MOSFETs and input bypass capacitor leads should be kept as short as possible. A ground plane should be used under the switching circuitry to prevent interplane coupling and to act as a thermal spreading path. Note that the bottom pad of the package is the heat sink, as well as the IC signal ground, and must be soldered to the ground plane.

In a boost converter, the conversion gain (assuming 100% efficiency) is calculated as (ignoring the forward voltage drop of the boost diode):

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

where D is the duty ratio of the main switch. D can then be estimated from the input and output voltages:

$$D = 1-\frac{V_{IN}}{V_{OUT}}; D_{MAX} = 1-\frac{V_{IN(MIN)}}{V_{OUT}}$$

The Peak and Average Input Currents

The control circuit in the LT3782A measures the input current by using a sense resistor in each MOSFET source, so the output current needs to be reflected back to the input in order to dimension the power MOSFET properly. Based on the fact that, ideally, the output power is equal to the input power, the maximum average input current is:

$$I_{IN(MAX)} = \frac{I_{O(MAX)}}{1-D_{MAX}}$$

The peak current is:

$$I_{IN(PEAK)} = 1.2 \bullet \frac{I_{O(MAX)}}{1-D_{MAX}}$$

The maximum duty cycle, D_{MAX}, should be calculated at minimum V_{IN}.

Power Inductor Selection

In a boost circuit, a power inductor should be designed to carry the maximum input DC current. The inductance should be small enough to generate enough ripple current to provide adequate signal to noise ratio to the LT3782A. An empirical starting of the inductor ripple current (per phase) is about 40% of maximum DC current, which is half of the input DC current in a 2-phase circuit:

$$\Delta I_L \cong 40\% \bullet \frac{I_{OUT(MAX)} \bullet V_{OUT}}{2V_{IN}} = 20\% \bullet \frac{I_{OUT(MAX)} \bullet V_{OUT}}{V_{IN}}$$

where V_{IN}, V_{OUT} and I_{OUT} are the DC input voltage, output voltage and output current, respectively.

And the inductance is estimated to be:

$$L = \frac{V_{IN} \bullet D}{f_S \bullet \Delta I_L}$$

where f_S is the switching frequency per phase.

The saturation current level of inductor is estimated to be:

$$I_{SAT} \geq \frac{\Delta I_L}{2} + \frac{I_{IN}}{2} \cong 70\% \bullet \frac{I_{OUT(MAX)} \bullet V_{OUT}}{V_{IN(MIN)}}$$

APPLICATIONS INFORMATION

Sense Resistor Selection

During the switch on-time, the control circuit limits the maximum voltage drop across the sense resistor to about 63mV. The peak inductor current is therefore limited to 63mV/R. The relationship between the maximum load current, duty cycle and the sense resistor R_{SENSE} is:

$$R \le V_{SENSE(MAX)} \bullet \frac{1-D_{MAX}}{1.2 \bullet \frac{I_{O(MAX)}}{2}}$$

Power MOSFET Selection

Important parameters for the power MOSFET include the drain-to-source breakdown voltage (BV_{DSS}), the threshold voltage ($V_{GS(TH)}$), the on-resistance ($R_{DS(ON)}$) versus gate-to-source voltage, the gate-to-source and gate-to-drain charges (Q_{GS} and Q_{GD}, respectively), the maximum drain current ($I_{D(MAX)}$) and the MOSFET's thermal resistances ($R_{TH(JC)}$ and $R_{TH(JA)}$).

The gate drive voltage is set by the 10V GBIAS regulator. Consequently, 10V rated MOSFETs are required in most high voltage LT3782A applications.

Pay close attention to the BV_{DSS} specifications for the MOSFETs relative to the maximum actual switch voltage in the application. The switch node can ring during the turn-off of the MOSFET due to layout parasitics. Check the switching waveforms of the MOSFET directly across the drain and source terminals using the actual PC board layout (not just on a lab breadboard!) for excessive ringing.

Calculating Power MOSFET Switching and Conduction Losses and Junction Temperatures

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current and the junction temperature itself (due to the positive temperature coefficient of its $R_{DS(ON)}$). As a result, some iterative calculation is normally required to determine a reasonably accurate value. Care should be taken to ensure that the converter is capable of delivering the required load current over all operating conditions (line voltage and temperature), and for the worst-case specifications for $V_{SENSE(MAX)}$ and the $R_{DS(ON)}$ of the MOSFET listed in the manufacturer's data sheet.

The power dissipated by the MOSFET in a 2-phase boost converter is:

$$P_{FET} = \frac{\left(\frac{I_{O(MAX)}}{2}\right)^2}{(1-D)} \bullet R_{DS(ON)} \bullet D \bullet \rho_T + k \bullet V_O^2 \bullet \frac{\left(\frac{I_{O(MAX)}}{2}\right)}{(1-D)} \bullet C_{RSS} \bullet f$$

The first term in the equation above represents the I^2R losses in the device, and the second term, the switching losses. The constant, k = 1.7, is an empirical factor inversely related to the gate drive current and has the dimension of 1/current. The ρ_T term accounts for the temperature coefficient of the $R_{DS(ON)}$ of the MOSFET, which is typically 0.4%/°C. Figure 4 illustrates the variation of normalized $R_{DS(ON)}$ over temperature for a typical power MOSFET.

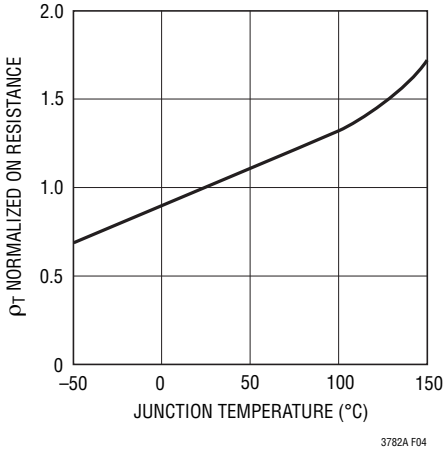


Figure 4. Normalized $R_{DS(ON)}$ vs Temperature

APPLICATIONS INFORMATION

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

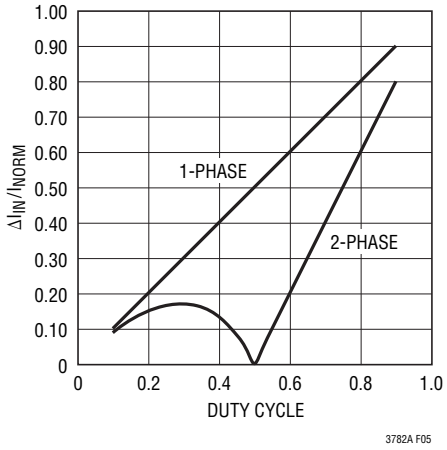
$$T_J = T_A + P_{FET} \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(CA)}$). This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Input Capacitor Choice

The input capacitor must have high enough voltage and ripple current ratings to handle the maximum input voltage and RMS ripple current rating. The input ripple current in a boost circuit is very small because the input current is continuous. With 2-phase operation, the ripple cancellation will further reduce the input capacitor ripple current rating. The ripple current is plotted in Figure 5. Please note that the ripple current is normalized against:

$$I_{norm} = \frac{V_{IN}}{L \bullet f_S}$$



$$I_{norm} = \frac{V_{IN}}{L \bullet f_S}$$

The RMS Ripple Current is About 29% of the Peak-to-Peak Ripple Current.

Figure 5. Normalized Input Peak-to-Peak Ripple Current

Output Capacitor Selection

The voltage rating of the output capacitor must be greater than the maximum output voltage with sufficient derating. Because the ripple current in output capacitor is a pulsating square wave in a boost circuit, it is important that the ripple current rating of the output capacitor be high enough to deal with this large ripple current. Figure 6 shows the output ripple current in the 1- and 2-phase designs. As shown, the output ripple current of a 2-phase boost circuit reaches almost zero when the duty cycle equals 50% or the output voltage is twice as much as the input voltage. Thus the 2-phase technique significantly reduces the output capacitor size.

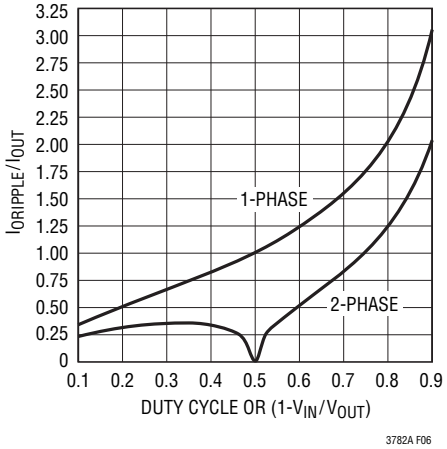


Figure 6. Normalized Output RMS Ripple Currents in Boost Converter: 1-Phase and 2-Phase. I_{OUT} Is the DC Output Current.

APPLICATIONS INFORMATION

For a given V_{IN} and V_{OUT}, we can calculate the duty cycle D and then derive the output RMS ripple current from Figure 6. After choosing output capacitors with sufficient RMS ripple current rating, we also need to consider the ESR requirement if electrolytic caps, tantalum caps, POSCAPs or SP CAPs are selected. Given the required output ripple voltage spec ΔV_{OUT} (in RMS value) and the calculated RMS ripple current ΔI_{OUT}, one can estimate the ESR value of the output capacitor to be

$$ESR \leq \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

External Regulator to Bias Gate Drivers

For applications with V_{IN} higher than 24V, the IC temperature may get too high. To reduce heat, an external regulator between 12V to 14V should be used to override the internal V_{GBIAS} regulator to supply the current needed for BGATE1 and BGATE2 (see Figure 7).

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power (¥100%). Percent efficiency can be expressed as:

% Efficiency = 100% – (L1 + L2 + L3 + …),

where L1, L2, etc. are the individual loss components as a percentage of the input power. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources usually account for the majority of the losses in LT3782A application circuits:

1. The supply current into V_{IN}. The V_{IN} current is the sum of the DC supply current I_Q (given in the Electrical Characteristics) and the MOSFET driver and control currents. The DC supply current into the V_{IN} pin is typically about 7mA and represents a small power loss (much less than 1%) that increases with V_{IN}. The driver current results from switching the gate capacitance of the power MOSFET; this current is typically much larger than the DC current. Each time the MOSFET is switched on and then off, a packet of gate charge Q_G is transferred from GBIAS to ground. The resulting dQ/dt is a current that must be supplied to the GBIAS capacitor through the V_{IN} pin by an external supply. In normal operation:

   $I_{Q(TOT)} \approx I_Q = f \bullet Q_G$

   $P_{IC} = V_{IN} \bullet (I_Q + f \bullet Q_G)$

2. Power MOSFET switching and conduction losses:

$$P_{FET} = \left(\frac{\frac{I_{O(MAX)}}{2}}{1-D_{MAX}} \right)^2 \bullet R_{DS(ON)} \bullet D_{MAX} \bullet \rho_T$$

$$+ k \bullet V_O^2 \bullet \frac{\frac{I_{O(MAX)}}{2}}{1-D_{MAX}} \bullet C_{RSS} \bullet f$$

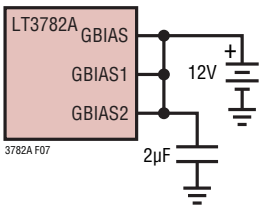


Figure 7

APPLICATIONS INFORMATION

3. The I^2R losses in the sense resistor can be calculated almost by inspection:

$$P_{R(SENSE)} = \left(\frac{\frac{I_{O(MAX)}}{2}}{1-D_{MAX}} \right)^2 \bullet R \bullet D_{MAX}$$

4. The losses in the inductor are simply the DC input current squared times the winding resistance. Expressing this loss as a function of the output current yields:

$$P_{R(WINDING)} = \left(\frac{\frac{I_{O(MAX)}}{2}}{1-D_{MAX}} \right)^2 \bullet R_W$$

5. Losses in the boost diode. The power dissipation in the boost diode is:

$$P_{DIODE} = \frac{I_{O(MAX)}}{2} \bullet V_D$$

   The boost diode can be a major source of power loss in a boost converter. For 13.2V input, 42V output at 3A, a Schottky diode with a 0.4V forward voltage would dissipate 600mW, which represents about 1% of the input power. Diode losses can become significant at low output voltages where the forward voltage is a significant percentage of the output voltage.

6. Other losses, including C_{IN} and C_O ESR dissipation and inductor core losses, generally account for less than 2% of the total losses.

PCB Layout Considerations

To achieve best performance from an LT3782A circuit, the PC board layout must be carefully done. For lower power applications, a two-layer PC board is sufficient. However, at higher power levels, a multiplayer PC board is recommended. Using a solid ground plane under the circuit is the easiest way to ensure that switching noise does not affect the operation.

In order to help dissipate the power from MOSFETs and diodes, keep the ground plane on the layers closest to the layers where power components are mounted. Use power planes for MOSFETs and diodes in order to improve the spreading of the heat from these components into the PCB.

For best electrical performance, the LT3782A circuit should be laid out as follows:

Place all power components in a tight area. This will minimize the size of high current loops. Orient the input and output capacitors and current sense resistors in a way that minimizes the distance between the pads connected to ground plane.

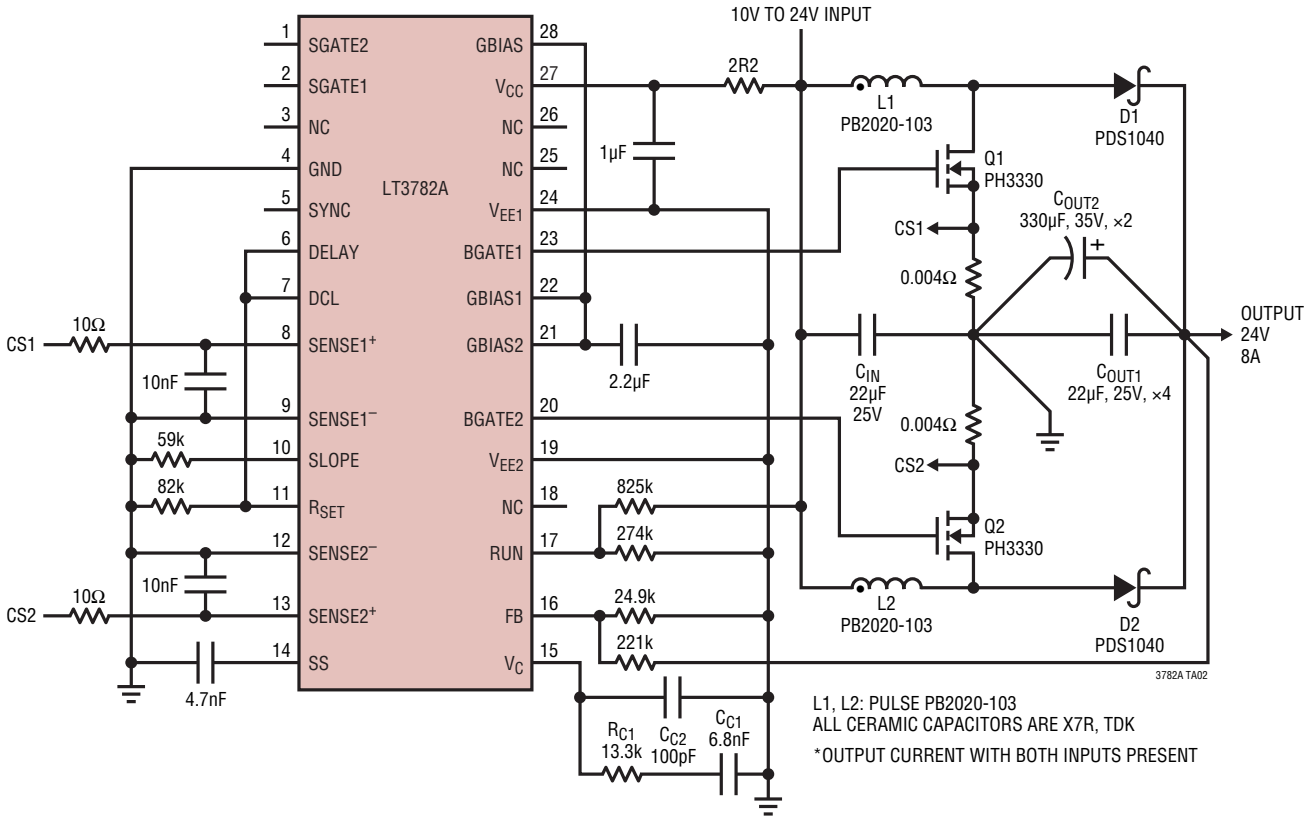
Place the LT3782A and associated components tightly together and next to the section with power components.

Use a local via to ground plane for all pads that connect to ground. Use multiple vias for power components.

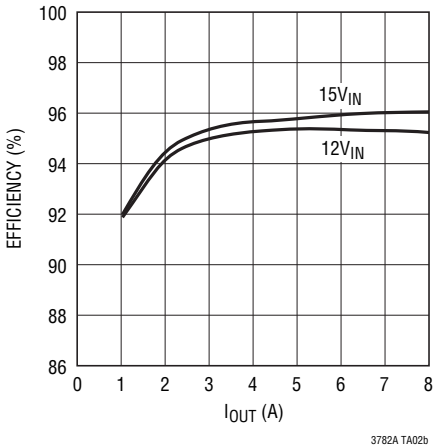
Connect the current sense inputs of LT3782A directly to the current sense resistor pads. Connect the current sense traces on the opposite sides of pads from the traces carrying the MOSFETs source currents to ground. This technique is referred to as Kelvin sensing.

TYPICAL APPLICATIONS

10V to 24V Input to 24V, 8A Output Boost Converter

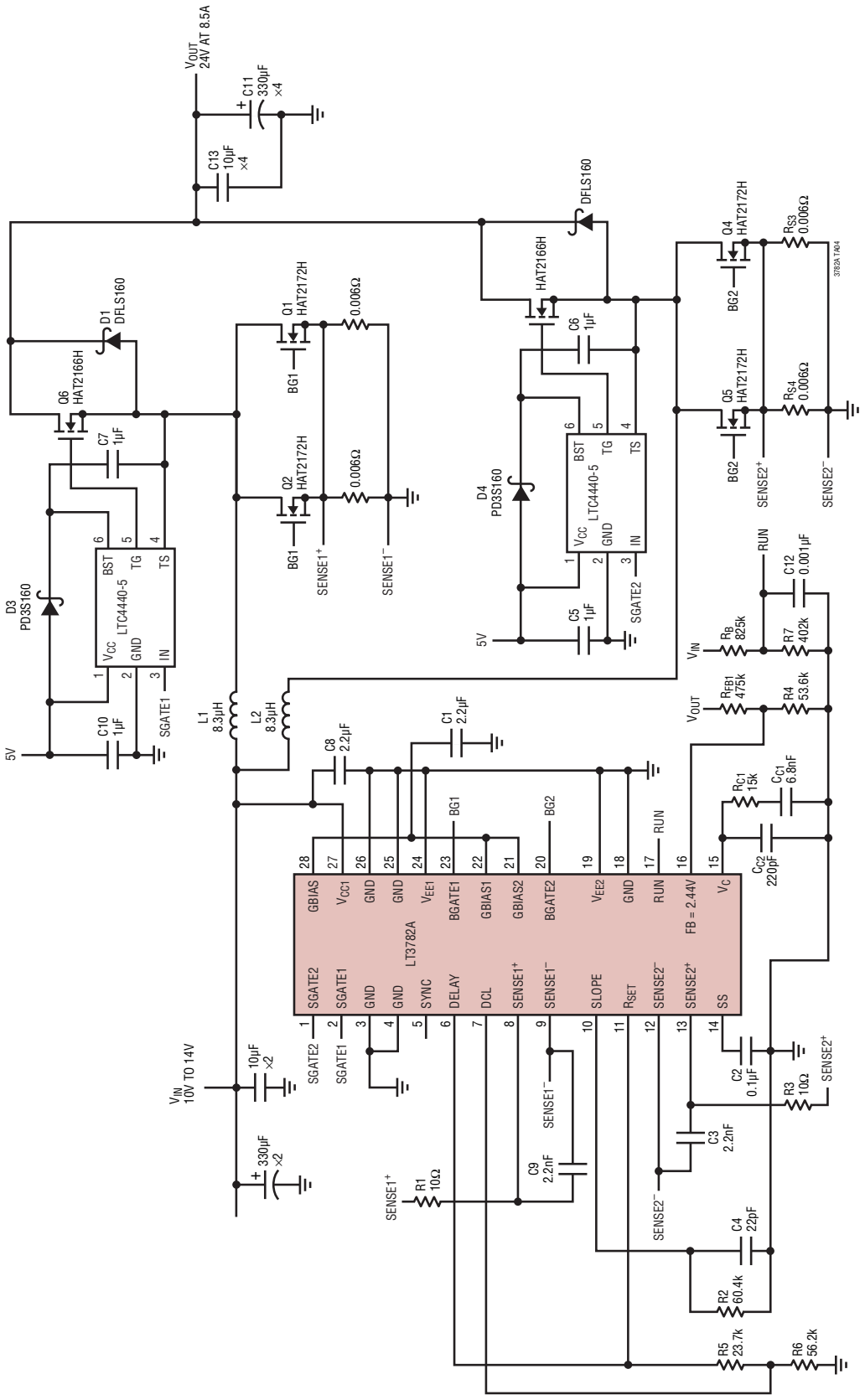


Efficiency



TYPICAL APPLICATIONS

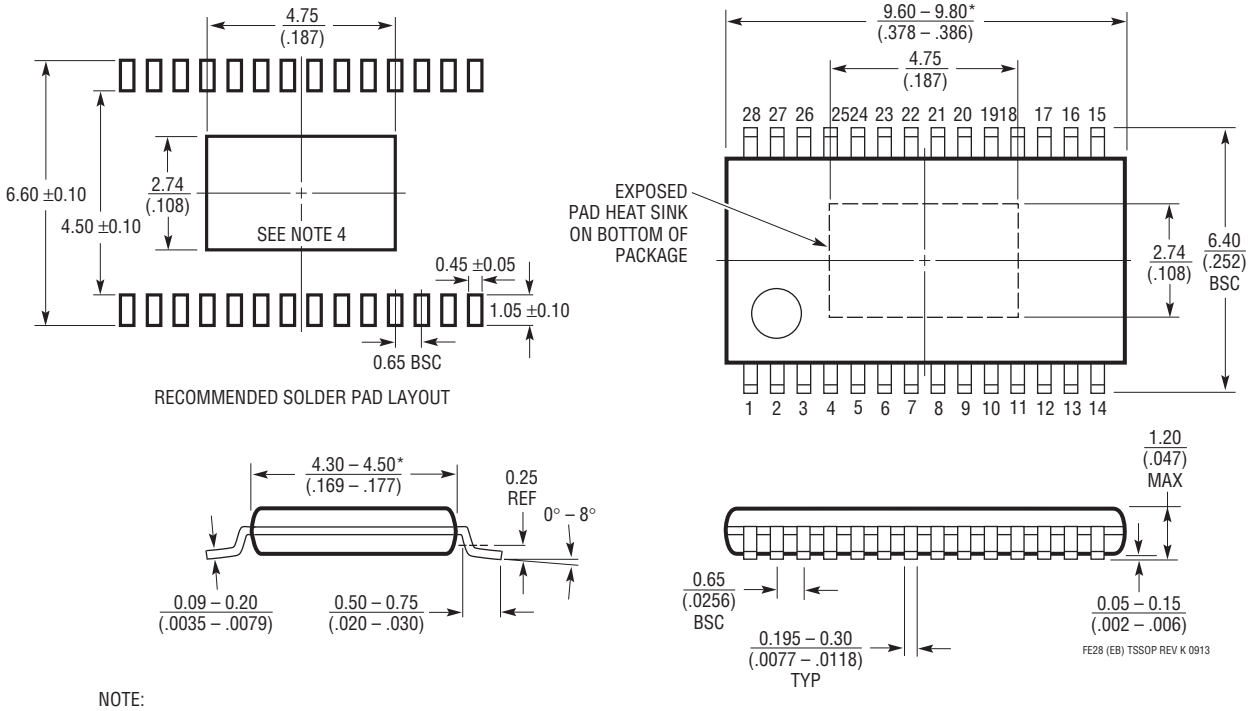
12V Input to 24V at 8.5A Output Synchronous Boost Converter



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation EB

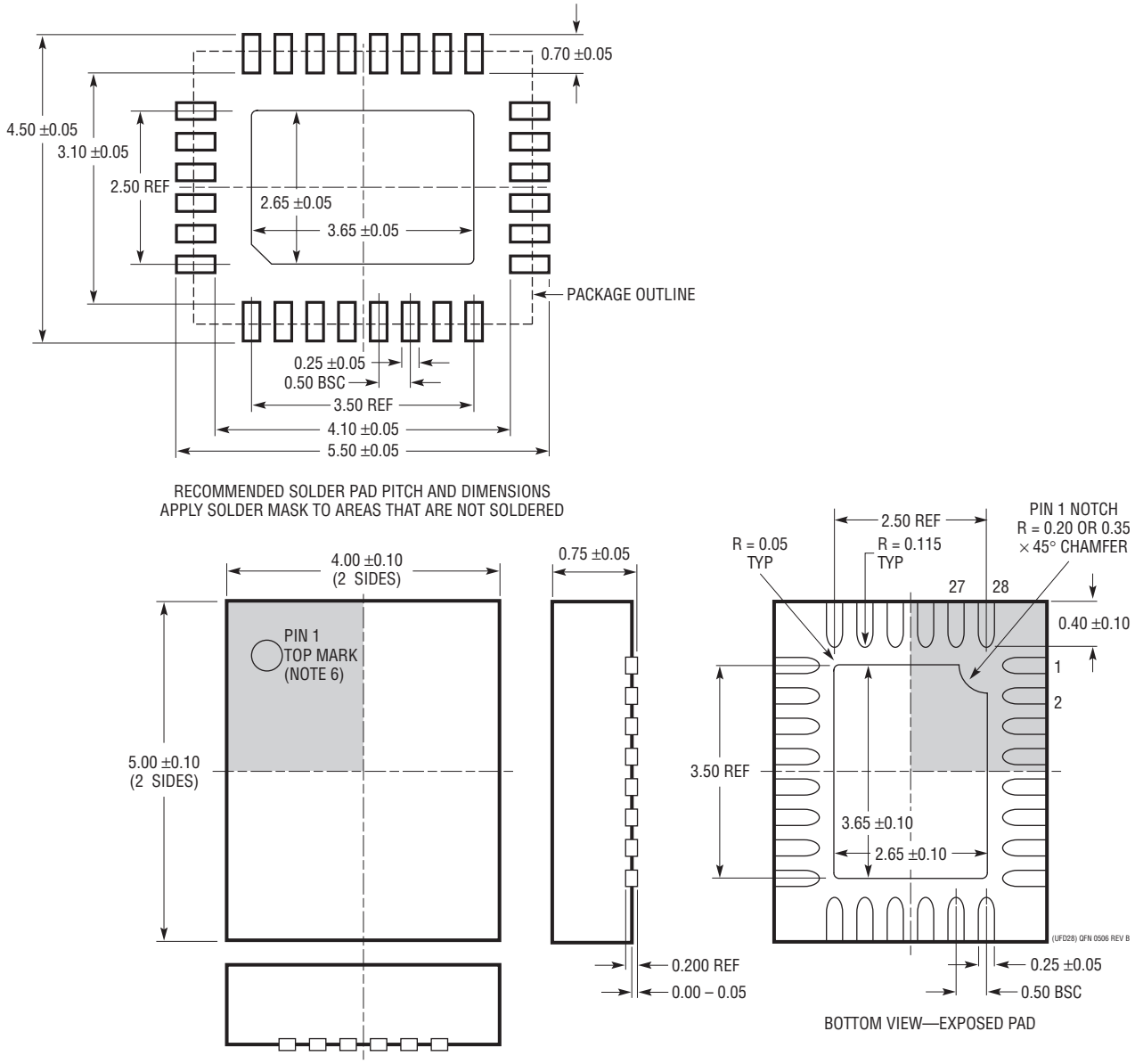


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



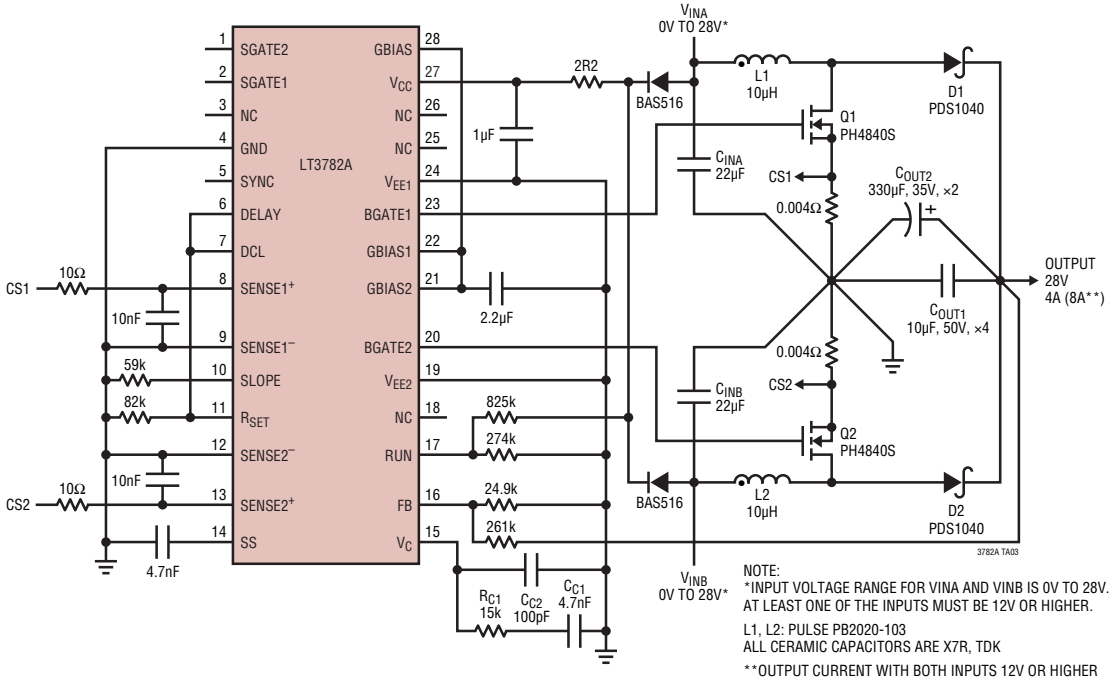
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/10	Change Ambient Temp on FE Package	2
		Changes to Order Information	2
		Addition to Note 2	4
		Change T_A = 25°C to T_J = 25°C	3, 4, 5
		Changes to Pin Functions	6
		Changes to Block Diagram	7
		Changes to Typical Applications	16, 20
		Updated Related Parts	20
B	4/10	Add Part Numbers for D1, D2, Q1 and Q2 on Typical Application	1
		Addition to Note 2	4
C	4/14	Adjusted RUN Threshold in the Electrical Characteristics table.	3
		Changed the RUN Pin description in the Pin Functions section.	6
		Changed Duty Cycle Limit in the Applications Information section.	9

TYPICAL APPLICATION

28V Output Base Station Power Converter with Redundant Input



NOTE:
*INPUT VOLTAGE RANGE FOR VINA AND VINB IS 0V TO 28V. AT LEAST ONE OF THE INPUTS MUST BE 12V OR HIGHER.

L1, L2: PULSE PB2020-103
ALL CERAMIC CAPACITORS ARE X7R, TDK

**OUTPUT CURRENT WITH BOTH INPUTS 12V OR HIGHER

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3862/LTC3862-1	Multiphase Current Mode Step-Up DC/DC Controller	2.5V ≤ V_{IN} ≤ 32V, 5V or 10V Gate Drive, 75kHz to 500kHz, TSSOP-24, SSOP-24, 5mm × 5mm QFN-24
LTC3788/LTC3788-1	Multiphase, Dual Output Synchronous Step-Up Controller	2.5V ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHz to 900kHz, 5mm × 5mm QFN-32, SSOP-28
LTC3813	100V Maximum V_{OUT} Current Mode Synchronous Step-Up DC/DC Controller	No R_{SENSE}™, 1Ω Gate Driver, Adjustable Off-Time, SSOP-28
LTC3814-5	60V Maximum V_{OUT} Current Mode Synchronous Step-Up DC/DC Controller	No R_{SENSE}, 1Ω Gate Driver, Adjustable Off-Time, TSSOP-16
LTC1871/LTC1871-1/ LTC1871-7	Wide Input Range, No R_{SENSE} Low Quiescent Current Flyback, Boost and SEPIC DC/DC Controller	Adjustable Fixed Synchronizable 50kHz to 1MHz Operating Frequency, 2.5V ≤ V_{IN} ≤ 36V, MSOP-10
LT3757	Boost, Flyback, SEPIC and Inverting DC/DC Controller	2.9V ≤ V_{IN} ≤ 40V, Adjustable Fixed Synchronizable 100kHz to 1MHz Operating Frequency, 3mm × 3mm DFN-10 and MSOP-10E
LT3758	Boost, Flyback, SEPIC and Inverting DC/DC Controller	5.5V ≤ V_{IN} ≤ 100V, Adjustable Fixed Synchronizable 100kHz to 1MHz Operating Frequency, 3mm × 3mm DFN-10 and MSOP-10E
LTC3805/LTC3805-5	Adjustable Frequency Boost, Flyback and SEPIC DC/DC Controller	V_{IN} and V_{OUT} Limited Only by External Components, 3mm × 3mm DFN-10, MSOP-10E
LTC3803/LTC3803-3/ LTC3803-5	Flyback DC/DC Controller with Fixed 200kHz or 300kHz Operating Frequency	V_{IN} and V_{OUT} Limited Only by External Components, 6-Pin ThinSOT™ Package
LTC3872	No R_{SENSE} Current Mode Boost DC/DC Controller	550kHz Fixed Frequency, 2.75V ≤ V_{IN} ≤ 9.8V, ThinSOT Package
LTC3780	High Efficiency Synchronous 4-Switch Buck-Boost DC/DC Controller	4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 30V, SSOP-24, 5mm × 5mm QFN-32

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- Shortage Management
- Alternative Solution
- Excess Inventory Management