THE DATASHEET OF

DS90C387VJDX/NOPB

www.win-source.net 0086-755-83957316

DS90C387, DS90CF388 Dual Pixel LVDS Display Interface (LDI)-SVGA/QXGA

Check for Samples: DS90C387, DS90CF388

FEATURES

- **Complies with OpenLDI Specification for Digital Display Interfaces**
- **32.5 to 112/170MHz Clock Support for DS90C387, 40 to 112MHz Clock Support for DS90CF388**
- **Supports SVGA through QXGA Panel Resolutions**
- **Drives Long, Low Cost Cables**
- **Up to 5.38Gbps Bandwidth**
- **Pre-Emphasis Reduces Cable Loading Effects**
- **DC Balance Data Transmission Provided by Transmitter Reduces ISI Distortion**
- **Cable Deskew of +/−1 LVDS Data Bit Time (up to 80 MHz Clock Rate) of Pair-to-Pair Skew at Receiver Inputs; Intra-Pair Skew Tolerance of 300ps**
- **Dual Pixel Architecture Supports Interface to GUI and Timing Controller; Optional Single Pixel Transmitter Inputs Support Single Pixel GUI Interface**
- **Transmitter Rejects Cycle-to-Cycle Jitter**
- **5V Tolerant on Data and Control Input Pins**
- **Programmable Transmitter Data and Control Strobe Select (Rising or Falling Edge Strobe)**
- **Backward Compatible Configuration Select with FPD-Link**
- **Optional Second LVDS Clock for Backward Compatibility w/ FPD-Link**
- **Support for Two Additional User-Defined Control Signals in DC Balanced Mode**
- **Compatible with ANSI/TIA/EIA-644-1995 LVDS Standard**

DESCRIPTION

The DS90C387/DS90CF388 transmitter/receiver pair is designed to support dual pixel data transmission between Host and Flat Panel Display up to QXGA resolutions. The transmitter converts 48 bits (Dual Pixel 24-bit color) of CMOS/TTL data into 8 LVDS (Low Voltage Differential Signalling) data streams. Control signals (VSYNC, HSYNC, DE and two user-defined signals) are sent during blanking intervals. At a maximum dual pixel rate of 112MHz, LVDS data line speed is 672Mbps, providing a total throughput of 5.38Gbps (672 Megabytes per second). Two other modes are also supported. 24-bit color data (single pixel) can be clocked into the transmitter at a maximum rate of 170MHz. In this mode, the transmitter provides single-to-dual pixel conversion, and the output LVDS clock rate is 85MHz maximum. The third mode provides inter-operability with FPD-Link devices.

The LDI chipset is improved over prior generations of FPD-Link devices and offers higher bandwidth support and longer cable drive with three areas of enhancement. To increase bandwidth, the maximum pixel clock rate is increased to 112 (170) MHz and 8 serialized LVDS outputs are provided. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. A cable deskew capability has been added to deskew long cables of pair-to-pair skew of up to +/−1 LVDS data bit time (up to 80 MHz Clock Rate). These three enhancements allow cables 5+ meters in length to be driven. This chipset is an ideal means to solve EMI and cable size problems for high-resolution flat panel applications. It provides a reliable interface based on LVDS technology that delivers the bandwidth needed for high-resolution panels while maximizing bit times, and keeping clock rates low to reduce EMI and shielding requirements. For more details, please refer to Applications Information.

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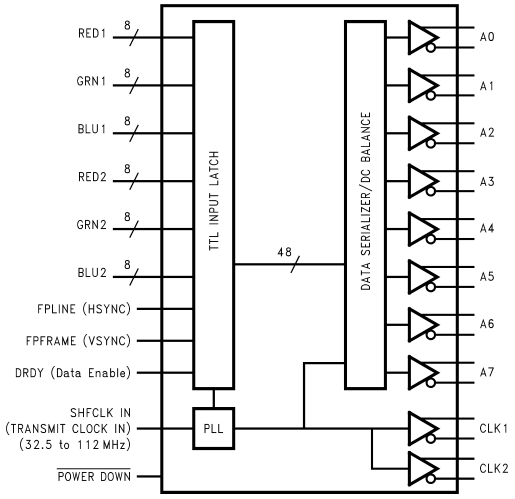
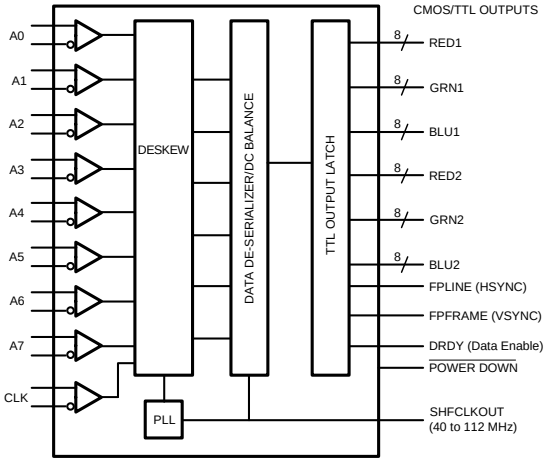
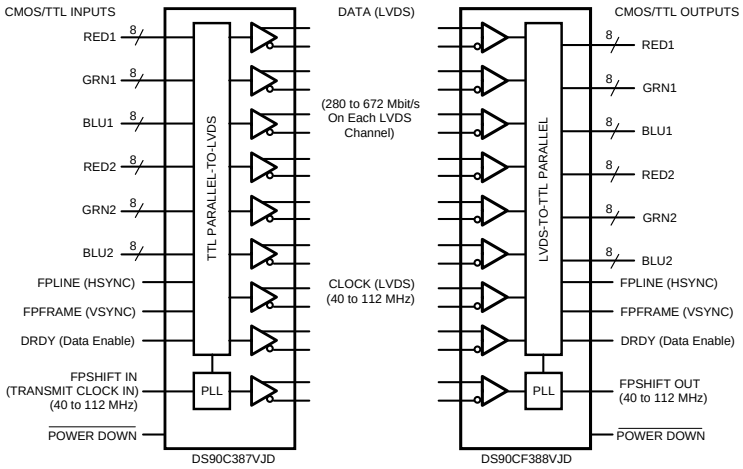
Transmitter Block Diagram



Receiver Block Diagram



Generalized Block Diagram



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})			−0.3V to +4V
CMOS/TTL Input Voltage			−0.3V to +5.5V
CMOS/TTL Output Voltage			−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage			−0.3V to +3.6V
LVDS Driver Output Voltage			−0.3V to +3.6V
LVDS Output Short Circuit Duration			Continuous
Junction Temperature			+150°C
Storage Temperature			−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)			+260°C
Maximum Package Power Dissipation Capacity at 25°C, 100 TQFP Package		DS90C387	2.8W
		DS90CF388	2.8W
Package Derating		DS90C387	18.2mW/°C above +25°C
		DS90CF388	18.2mW/°C above +25°C
ESD Rating	DS90C387	HBM, 1.5kΩ, 100pF	> 6 kV
		EIAJ, 0Ω, 200pF	> 300 V
	DS90CF388	HBM, 1.5kΩ, 100pF	> 2 kV
		EIAJ, 0Ω, 200pF	> 200 V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature ($T_{A)}$	−10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{p-p}

Electrical Characteristics(1)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMOS/TTL DC SPECIFICATIONS (Tx inputs, Rx outputs, control inputs and outputs)						
V_{IH}	High Level Input Voltage		2.0		5.0	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA	2.7	2.9		V
		I_{OH} = −2 mA	2.7	2.85		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}		+1.8	+15	µA
		V_{IN} = GND	−15	0		µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			−120	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

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Electrical Characteristics[1] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States					35	mV
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−10	mA
I_{OZ}	Output TRI-STATE Current	$\overline{PD}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	µA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (Figure 1 and Figure 3), DUAL=High (48-bit RGB), BAL=High (enabled)	f = 32.5 MHz		91.4	140	mA
			f = 65 MHz		106	160	mA
			f = 85 MHz		135	183	mA
			f = 112 MHz		155	210	mA
ICCTG	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern (Figure 2 and Figure 3), DUAL=High (48-bit RGB), BAL=High (enabled)	f = 32.5 MHz		62.6	120	mA
			f = 65 MHz		84.4	130	mA
			f = 85 MHz		89.0	145	mA
			f = 112 MHz		94.5	155	mA
ICCTZ	Transmitter Supply Current, Power Down	$\overline{PD}$ = Low Driver Outputs in TRI-STATE under Powerdown Mode			4.8	50	µA

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Electrical Characteristics[1] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern (Figure 1 and Figure 4), DUAL (48-bit RGB), BAL=High (enabled)	f = 40MHz		125	160	mA
			f = 65 MHz		200	250	mA
			f = 85 MHz		240	275	mA
			f = 112 MHz		250	300	mA
ICCRG	Receiver Support Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern (Figure 2 and Figure 4), DUAL (48-bit RGB), BAL=High (enabled)	f = 40MHz		60	95	mA
			f = 65 MHz		95	125	mA
			f = 85 MHz		115	150	mA
			f = 112 MHz		150	270	mA
ICCRZ	Receiver Supply Current, Power Down	$\overline{PD}$ = Low Receiver Outputs stay low during Powerdown mode			255	300	µA

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Unit
TCIT	TxCLK IN Transition Time (Figure 5)	DUAL=Gnd or Vcc	1.0	2.0	3.0	ns
		DUAL=1/2Vcc	1.0	1.5	1.7	ns
TCIP	TxCLK IN Period (Figure 6)	DUAL=Gnd or Vcc	8.928	T	30.77	ns
		DUAL=1/2Vcc	5.88		15.38	ns
TCIH	TxCLK in High Time (Figure 6)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK in Low Time (Figure 6)		0.35T	0.5T	0.65T	ns
TXIT	TxIN Transition Time		1.5		6.0	ns

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Unit
LLHT	LVDS Low-to-High Transition Time (Figure 3), PRE = 0.75V (disabled)			0.14	0.7	ns
	LVDS Low-to-High Transition Time (Figure 3), PRE = Vcc (max)			0.11	0.6	ns
LHLT	LVDS High-to-Low Transition Time (Figure 3), PRE = 0.75V (disabled)			0.16	0.8	ns
	LVDS High-to-Low Transition Time (Figure 3), PRE = Vcc (max)			0.11	0.7	ns
TBIT	Transmitter Output Bit Width	DUAL=Gnd or Vcc		1/7 TCIP		ns
		DUAL=1/2Vcc		2/7 TCIP		ns
TPPOS	Transmitter Pulse Positions - Normalized	f = 33 to 70 MHz	−250	0	+250	ps
		f = 70 to 112 MHz	−200	0	+200	ps
TCCS	TxOUT Channel to Channel Skew			100		ps
TSTC	TxIN Setup to TxCLK IN (Figure 6)		2.7			ns
THTC	TxIN Hold to TxCLK IN (Figure 6)		0			ns
TJCC	Transmitter Jitter Cycle-to-cycle (Figure 14 and Figure 15) , DUAL=Vcc [1]	f = 112 MHz		85	100	ps
		f = 85 MHz		60	75	ps
		f = 65 MHz		70	80	ps
		f = 56 MHz		100	120	ps
		f = 32.5 MHz		75	110	ps
TPLLS	Transmitter Phase Lock Loop Set (Figure 8)				10	ms

(1) The limits are based on bench characterization of the device's jitter response over the power supply voltage range. Output clock jitter is measured with a cycle-to-cycle jitter of ±3ns applied to the input clock signal while data inputs are switching (see Figure 14 and Figure 15). A jitter event of 3ns, represents worse case jump in the clock edge from most graphics VGA chips currently available. This parameter is used when calculating system margin as described in AN-1059 (SNLA050).

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Transmitter Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
TPDD	Transmitter Powerdown Delay (Figure 10)			100	ns

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Unit
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 4), Rx data out			1.52	2.0	ns
	CMOS/TTL Low-to-High Transition Time (Figure 4), Rx clock out			0.5	1.0	ns
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 4), Rx data out			1.7	2.0	ns
	CMOS/TTL High-to-Low Transition Time (Figure 4), Rx clock out			0.5	1.0	ns
RCOP	RxCLK OUT Period (Figure 7)		8.928	T	25	ns
RCOH	RxCLK OUT High Time (Figure 7)(1)	f = 112 MHz	3.5			ns
		f = 85 MHz	4.5			ns
RCOL	RxCLK OUT Low Time (Figure 7)(1)	f = 112 MHz	3.5			ns
		f = 85 MHz	4.5			ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 7)(1)	f = 112 MHz	2.4			ns
		f = 85 MHz	3.0			ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 7)(1)	f = 112 MHz	3.4			ns
		f = 85 MHz	4.75			ns
RPLLS	Receiver Phase Lock Loop Set (Figure 9)				10	ms
RPDD	Receiver Powerdown Delay (Figure 11)				1	µs

(1) The Minimum and Maximum Limits are based on statistical analysis of the device performance over voltage and temperature ranges. This parameter is functionally tested on Automatic Test Equipment (ATE). ATE is limited to 85MHz. A sample of characterization parts have been bench tested to verify functional performance.

Chipset RSKM Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(1) (2). See Applications Information for more details on this parameter and how to apply it.

Symbol	Parameter		Min	Typ	Max	Unit
RSKM	Receiver Skew Margin without Deskew in non-DC Balance Mode, (Figure 12), (3)	f = 112 MHz	170			ps
		f = 100 MHz	170	240		ps
		f = 85MHz	300	350		ps
		f = 66MHz	300	350		ps
RSKM	Receiver Skew Margin without Deskew in DC Balance Mode, (Figure 12)(3)	f = 112 MHz	170			ps
		f = 100 MHz	170	200		ps
		f = 85 MHz	250	300		ps
		f = 66 MHz	250	300		ps
		f = 50MHz	100	350		ps
		f = 40MHz	94	530		ps

(1) The Minimum and Maximum Limits are based on statistical analysis of the device performance over voltage and temperature ranges. This parameter is functionally tested on Automatic Test Equipment (ATE). ATE is limited to 85MHz. A sample of characterization parts have been bench tested to verify functional performance.

(2) Typical values for RSKM and RSKMD are applicable for fixed V_{CC} and T_A for the Transmitter and Receiver (both are assumed to be at the same V_{CC} and T_A points).

(3) Receiver Skew Margin (RSKM) is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter output pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPOS). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable) and clock jitter.RSKM ≥ cable skew (type, length) + source clock jitter (cycle to cycle, TJCC) + ISI (if any). See Applications Information for more details.

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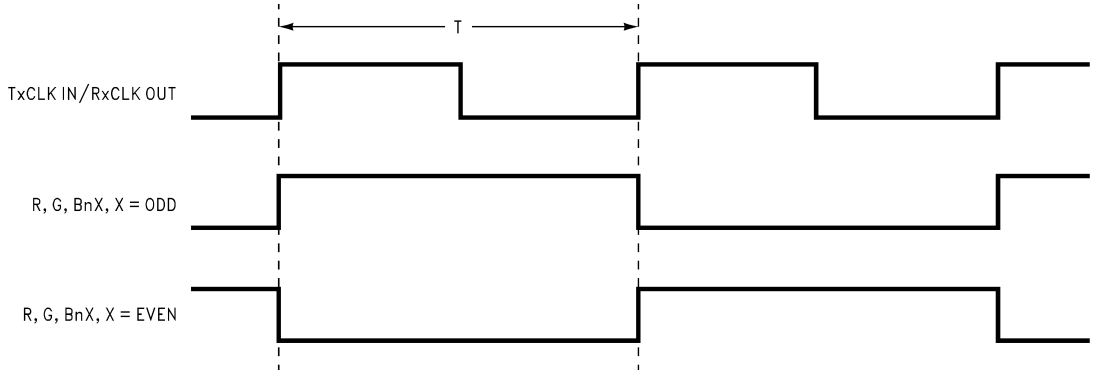
Chipset RSKM Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1) (2). See Applications Information for more details on this parameter and how to apply it.

Symbol	Parameter		Min	Typ	Max	Unit
RSKMD	Receiver Skew Margin with Deskew in DC Balance, (Figure 13)(4)	f = 40 to 80 MHz	0.25TBIT			ps
RDR	Receiver Deskew Range	f = 80 MHz	± 1			TBIT
RDSS	Receiver Deskew Step Size	f = 80 MHz		0.3 TBIT		ns

(4) Receiver Skew Margin with Deskew (RSKMD) is defined as the valid data sampling region at the receiver inputs. The DESKEW function will constrain the receiver's sampling strobes to the middle half of the LVDS bit and removes (adjusts for) fixed interconnect skew. This margin (RSKMD) allows for inter-symbol interference (dependent on type/length of cable), Transmitter Pulse Position (TPPOS) variance, and LVDS clock jitter (TJCC).RSKMD ≥ ISI + TPPOS(variance) + source clock jitter (cycle to cycle). See Applications Information for more details.

AC Timing Diagrams



A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

B. Figure 1 and Figure 2 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Figure 1. "Worst Case" Test Pattern

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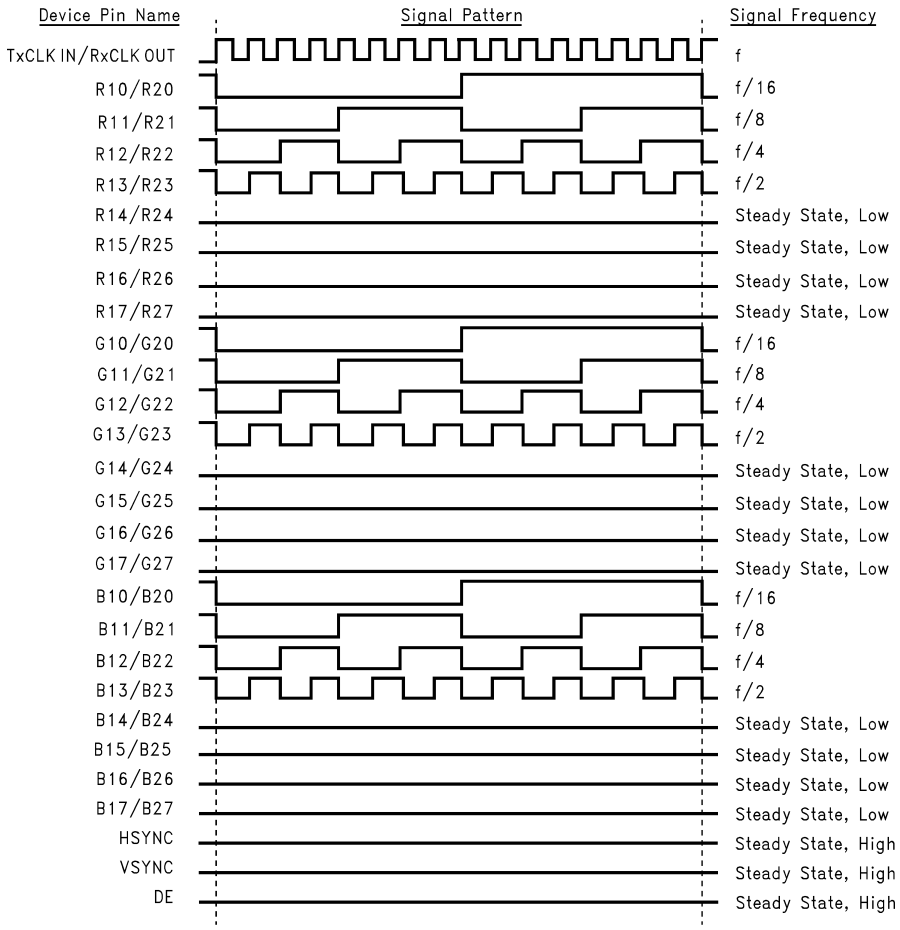

A. The 16 grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

B. Figure 1 and Figure 2 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Figure 2. “16 Grayscale” Test Pattern

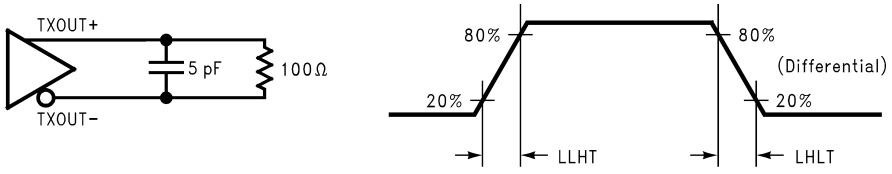

Figure 3. DS90C387 (Transmitter) LVDS Output Load and Transition Times

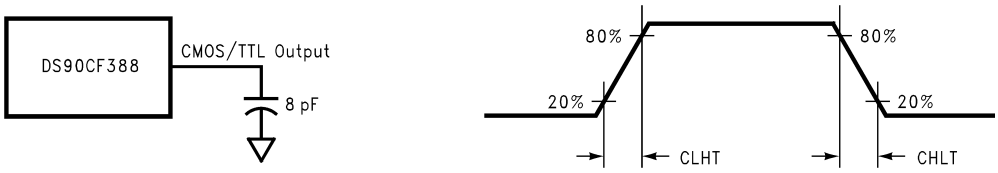

Figure 4. DS90CF388 (Receiver) CMOS/TTL Output Load and Transition Times

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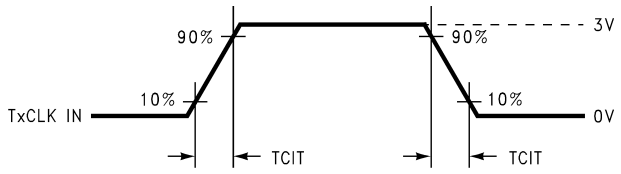

Figure 5. DS90C387 (Transmitter) Input Clock Transition Time

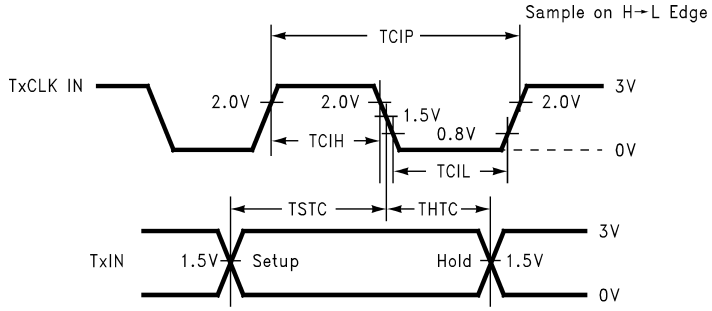

Figure 6. DS90C387 (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

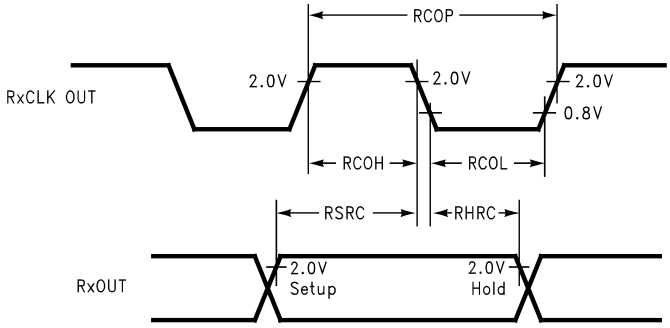

Figure 7. DS90CF388 (Receiver) Setup/Hold and High/Low Times

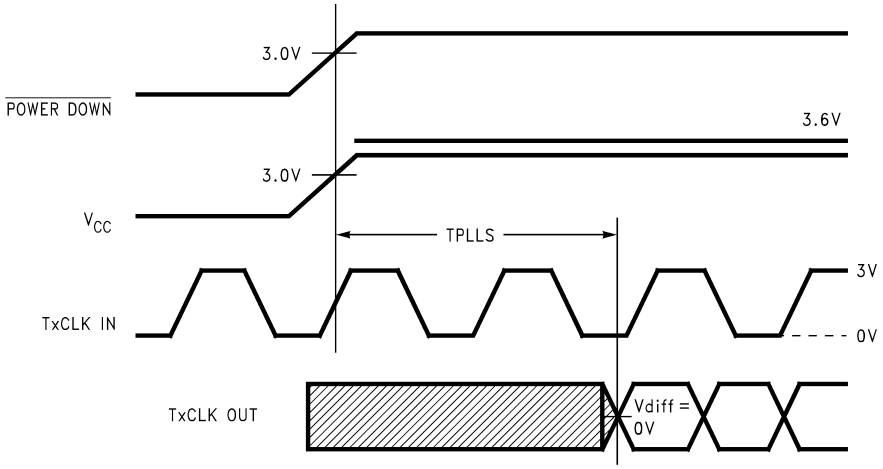

Figure 8. DS90C387 (Transmitter) Phase Lock Loop Set Time

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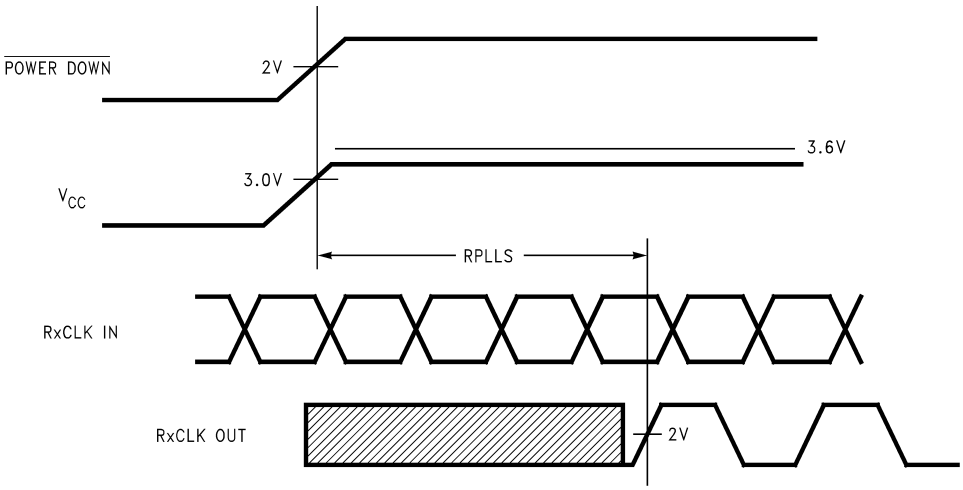

Figure 9. DS90CF388 (Receiver) Phase Lock Loop Set Time

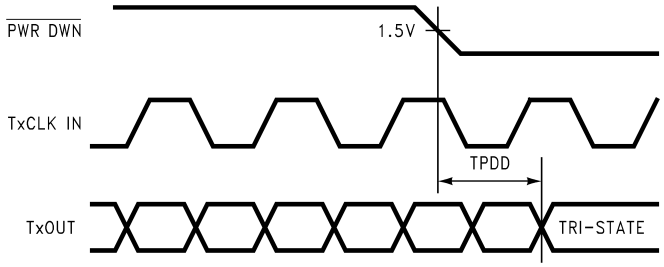

Figure 10. Transmitter Power Down Delay

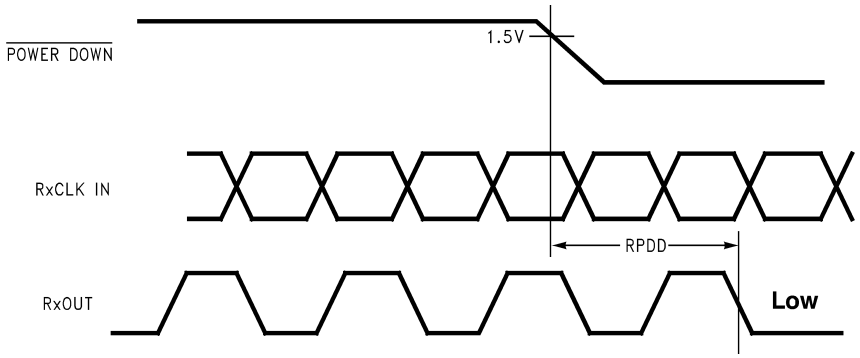

Figure 11. Receiver Power Down Delay

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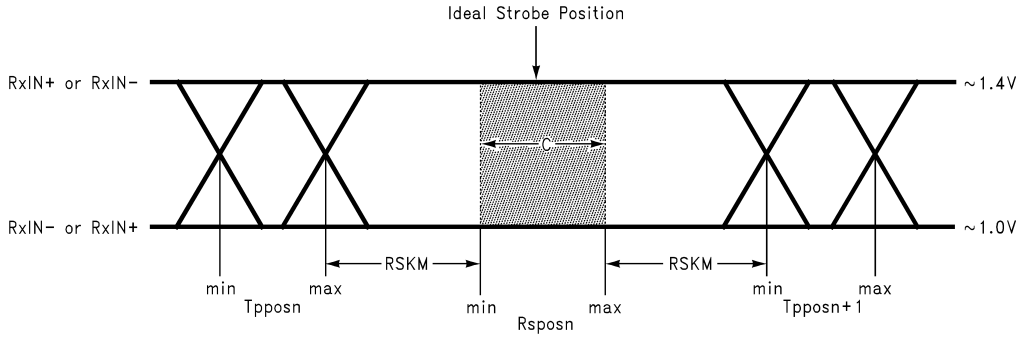
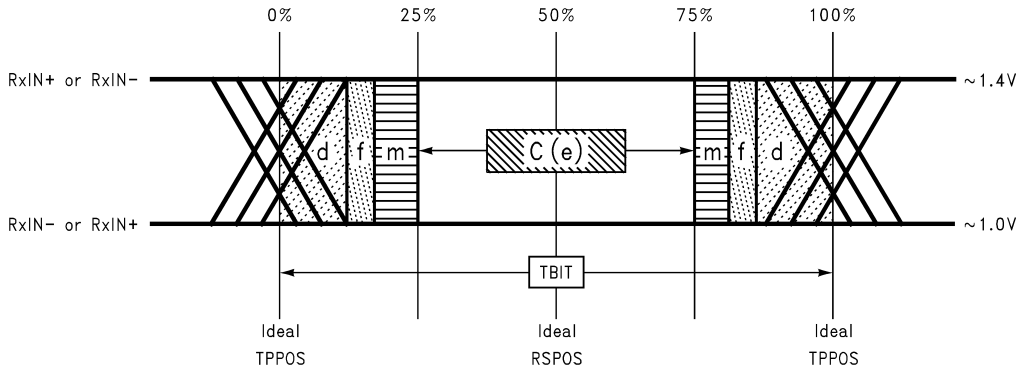


C — Setup and Hold Time (Internal data sampling window) defined by RSPOS (receiver input strobe position) min and max
TPPOS — Transmitter output pulse position (min and max)
RSKM ≥ Cable Skew (type, length) + LVDS Source Clock Jitter (cycle to cycle) + ISI (Inter-symbol interference)
- Cable Skew—typically 10 ps to 40 ps per foot, media dependent
- TJCC — Cycle-to-cycle LVDS Output jitter (TJCC) is less than 100 ps (worse case estimate).
- ISI is dependent on interconnect length; may be zero

See Applications Information for more details.

Figure 12. Receiver Skew Margin



C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
RSKMD ≥ TPPOSvariance (d) + TJCC (output jitter)(f) + ISI (m)
- d = Tppos — Transmitter output pulse position (min and max)
- f = TJCC — Cycle-to-cycle LVDS Output jitter (TJCC) is less than 100 ps (worse case estimate).
- m = extra margin - assigned to ISI in long cable applications

See Applications Information for more details.

Figure 13. Receiver Skew Margin (RSKMD) with DESKEW

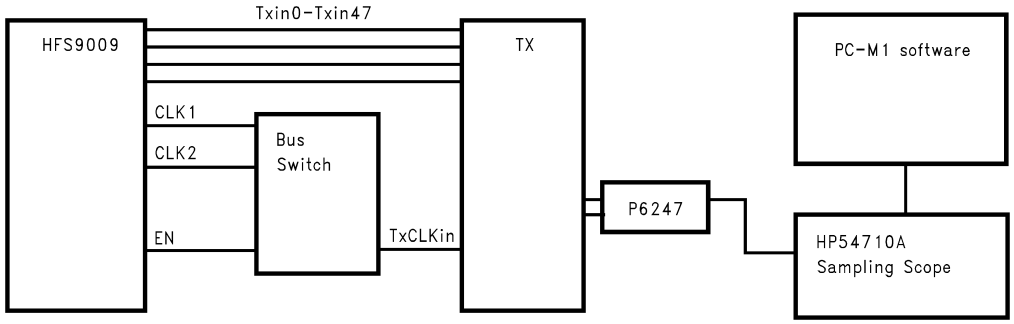


Figure 14. TJCC Test Setup - DS90C387

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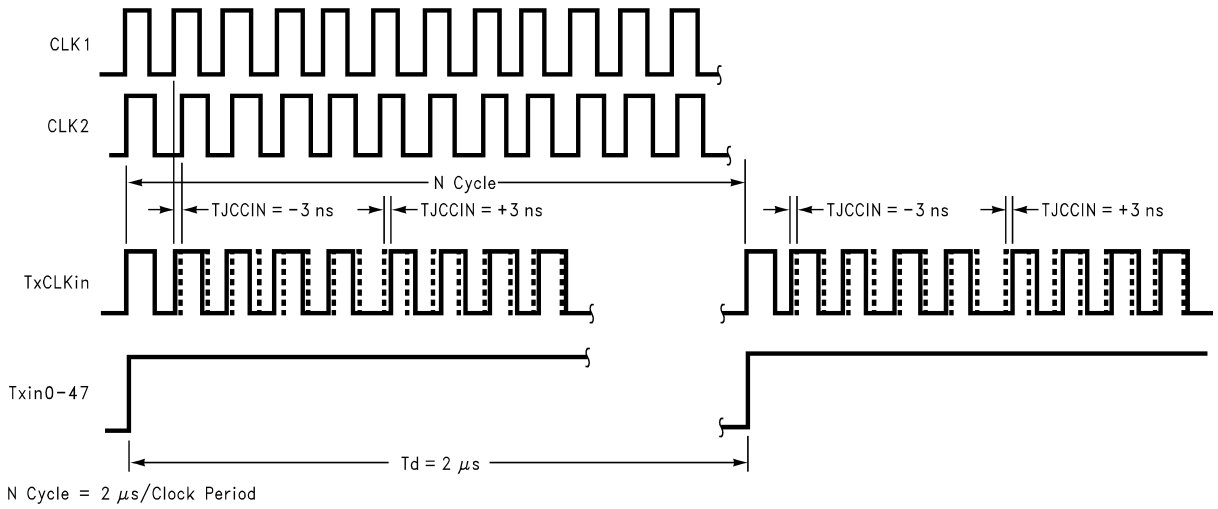

Figure 15. Timing Diagram of the Input Cycle-to-Cycle Clock Jitter

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DS90C387 PIN DESCRIPTIONS — FPD LINK TRANSMITTER

Pin Name	I/O	No.	Description
Rn, Gn, Bn, DE, HSYNC, VSYNC	I	51	TTL level input. This includes: 16 Red, 16 Green, 16 Blue, and 3 control lines HSYNC, VSYNC, DE (Data Enable).(1)
AnP	O	8	Positive LVDS differential data output.
AnM	O	8	Negative LVDS differential data output.
CLKIN	I	1	TTL level clock input.
R_FB	I	1	Programmable data strobe select. Rising data strobe edge selected when input is high. (1)
R_FDE	I	1	Programmable control (DE) strobe select. Tied high for data active when DE is high. (1)
CLK1P	O	1	Positive LVDS differential clock output.
CLK1M	O	1	Negative LVDS differential clock output.
$\overline{PD}$	I	1	TTL level input. Assertion (low input) tri-states the outputs, ensuring low current at power down. (1)
PLLSEL	I	1	PLL range select. This pin must be tied to V_{CC} for auto-range. NC or tied to Ground is reserved for future use. Typical shift point is between 55 and 68 MHz. (1) (2)
BAL	I	1	Mode select for DC Balanced (new) or non-DC Balanced (backward compatible) interface. DC Balance is active when input is high. NC or tied to Ground, the DC Balance function is disabled. (1) (3) (4)
PRE	I	1	Pre-emphasis level select. Pre-emphasis is active when input is tied to V_{CC} through external pull-up resistor. Resistor value determines pre-emphasis level (see Pre-Emphasis). For normal LVDS drive level (No pre-emphasis) leave this pin open (do not tie to ground).(1)
DUAL	I	1	Three-mode select for dual pixel, single pixel, or single pixel input to dual pixel output operation. Single pixel mode when input is low (only LVDS channels A0 thru A3 and CLK1 are active) for power savings. Dual mode is active when input is high. Single in - dual out when input is at 1/2 Vcc. (1) Figure 16
V_{CC}	I	4	Power supply pins for TTL inputs and digital circuitry.
GND	I	5	Ground pins for TTL inputs and digital circuitry.
$PLLV_{CC}$	I	2	Power supply pin for PLL circuitry.
PLLGND	I	3	Ground pins for PLL circuitry.
$LVDSV_{CC}$	I	3	Power supply pin for LVDS outputs.
LVDSGND	I	4	Ground pins for LVDS outputs.
CLK2P/NC	O	1	Additional positive LVDS differential clock output. Identical to CLK1P. No connect if not used.
CLK2M/NC	O	1	Additional negative LVDS differential clock output. Identical to CLK1M. No connect if not used.

(1) Inputs default to “low” when left open due to internal pull-down resistor.
(2) The PLL range shift point is in the 55 - 68 MHz range, typically the shift will occur during the lock time.
(3) DC Balancing is functionally tested on Automatic Test Equipment (ATE) at 85 MHz only. A sample of characterization units have been bench tested at 112 MHz to verify full speed performance.
(4) The DS90CF388 is designed to automatically detect the DC Balance or non-DC Balance transmitted data from the DS90C387 and deserialize the LVDS data according to the defined bit mapping.

DS90CF388 PIN DESCRIPTIONS — FPD LINK RECEIVER

Pin Name	I/O	No.	Description
AnP	I	8	Positive LVDS differential data inputs.
AnM	I	8	Negative LVDS differential data inputs.
Rn, Gn, Bn, DE, HSYNC, VSYNC	O	51	TTL level data outputs. This includes: 16 Red, 16 Green, 16 Blue, and 3 control lines— HSYNC (LP), VSYNC (FLM), DE (Data Enable).
RxCLK INP	I	1	Positive LVDS differential clock input.
RxCLK INM	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
R_FDE	I	1	Programmable control (DE) strobe select. Tied high for data active when DE is high. (1)
PLLSEL	I	1	PLL range select. This pin must be tied to V_{CC} for auto-range. NC or tied to Ground is reserved for future use. Typical shift point is between 55 and 68 MHz. (2) (3)

(1) Inputs default to “low” when left open due to internal pull-down resistor.
(2) DC Balancing is functionally tested on Automatic Test Equipment (ATE) at 85 MHz only. A sample of characterization units have been bench tested at 112 MHz to verify full speed performance.
(3) The PLL range shift point is in the 55 - 68 MHz range, typically the shift will occur during the lock time.

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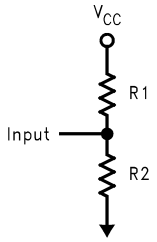
DS90CF388 PIN DESCRIPTIONS — FPD LINK RECEIVER (continued)

Pin Name	I/O	No.	Description
BAL	I	1	Mode select for DC Balanced (new) or non-DC Balanced (backward compatible) interface. BAL = LOW for non-DC Balanced mode. BAL = HIGH for DC Balanced Mode (Auto-detect mode), with this pin HIGH the received LVDS clock signal is used to determine if the interface is in new or backward compatible mode. (1) (2) (4)
DESKEW	I	1	Deskew and oversampling “on/off” select. Deskew is active when input is high. Only supported in DC Balance mode (BAL=High). To complete the deskew operation, a minimum of four clock cycles is required during blanking time. (1)
$\overline{PD}$	I	1	TTL level input. When asserted (low input) the receiver data outputs are low and clock output is high. (1)
STOPCLK	O	1	Indicates receiver clock input signal is not present with a logic high. With a clock input present, a low logic is indicated.
V_{CC}	I	6	Power supply pins for TTL outputs and digital circuitry.
GND	I	8	Ground pins for TTL outputs and digital circuitry
$PLLV_{CC}$	I	1	Power supply for PLL circuitry.
PLLGND	I	2	Ground pin for PLL circuitry.
$LVDSV_{CC}$	I	2	Power supply pin for LVDS inputs.
LVDSGND	I	3	Ground pins for LVDS inputs.
CNTLE, CNTLF	O	2	TTL level data outputs. User-defined control signals - no connect when not used.

(4) The DS90CF388 is designed to automatically detect the DC Balance or non-DC Balance transmitted data from the DS90C387 and deserialize the LVDS data according to the defined bit mapping.



Recommend using R1=R2=10kΩ for single to dual mode

Figure 16. Resistor Network for “DUAL” pin input

LVDS Interface

Table 1. LVDS DATA BIT NAMING CONVENTION

X	Y	Z	Description
X=R			Red
X=G			Green
X=B			Blue
	Y=1		Odd (First) Pixel
	Y=2		Even (Second) Pixel
		Z=0-7	LVDS bit number (not VGA controller LSB to MSB)

Table 2. SINGLE PIXEL PER CLOCK INPUT APPLICATION DATA MAPPING (DUAL=GND)

VGA - TFT Data Signals Color Bits			Transmitter input pin names	Receiver output pin names	TFT Panel Data Signals	
	24-bit	18-bit	DS90C387	DS90CF388	18-bit	24-bit
LSB	R0		R16	R16		R0
	R1		R17	R17		R1
	R2	R0	R10	R10	R0	R2

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Table 2. SINGLE PIXEL PER CLOCK INPUT APPLICATION DATA MAPPING (DUAL=GND) (continued)

VGA - TFT Data Signals Color Bits			Transmitter input pin names	Receiver output pin names	TFT Panel Data Signals	
	R3	R1	R11	R11	R1	R3
	R4	R2	R12	R12	R2	R4
	R5	R3	R13	R13	R3	R5
	R6	R4	R14	R14	R4	R6
MSB	R7	R5	R15	R15	R5	R7
LSB	G0		G16	G16		G0
	G1		G17	G17		G1
	G2	G0	G10	G10	G0	G2
	G3	G1	G11	G11	G1	G3
	G4	G2	G12	G12	G2	G4
	G5	G3	G13	G13	G3	G5
	G6	G4	G14	G14	G4	G6
MSB	G7	G5	G15	G15	G5	G7
LSB	B0		B16	B16		B0
	B1		B17	B17		B1
	B2	B0	B10	B10	B0	B2
	B3	B1	B11	B11	B1	B3
	B4	B2	B12	B12	B2	B4
	B5	B3	B13	B13	B3	B5
	B6	B4	B14	B14	B4	B6
MSB	B7	B5	B15	B15	B5	B7

Table 3. DUAL PIXEL PER CLOCK INPUT APPLICATION DATA MAPPING (DUAL=VCC)

VGA - TFT Data Signals Color Bits			Transmitter input pin names	Receiver output pin names	TFT Panel Data Signals	
	48-bit	36-bit	DS90C387	DS90CF388	36-bit	48-bit
LSB	RO0		R16	R16		RO0
	RO1		R17	R17		RO1
	RO2	RO0	R10	R10	RO0	RO2
	RO3	RO1	R11	R11	RO1	RO3
	RO4	RO2	R12	R12	RO2	RO4
	RO5	RO3	R13	R13	RO3	RO5
	RO6	RO4	R14	R14	RO4	RO6
MSB	RO7	RO5	R15	R15	RO5	RO7
LSB	GO0		G16	G16		GO0
	GO1		G17	G17		GO1
	GO2	GO0	G10	G10	GO0	GO2
	GO3	GO1	G11	G11	GO1	GO3
	GO4	GO2	G12	G12	GO2	GO4
	GO5	GO3	G13	G13	GO3	GO5
	GO6	GO4	G14	G14	GO4	GO6
MSB	GO7	GO5	G15	G15	GO5	GO7
LSB	BO0		B16	B16		BO0
	BO1		B17	B17		BO1
	BO2	BO0	B10	B10	BO0	BO2
	BO3	BO1	B11	B11	BO1	BO3
	BO4	BO2	B12	B12	BO2	BO4

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Table 3. DUAL PIXEL PER CLOCK INPUT APPLICATION DATA MAPPING (DUAL=VCC) (continued)

VGA - TFT Data Signals Color Bits			Transmitter input pin names	Receiver output pin names	TFT Panel Data Signals	
	BO5	BO3	B13	B13	BO3	BO5
	BO6	BO4	B14	B14	BO4	BO6
MSB	BO7	BO5	B15	B15	BO5	BO7
LSB	RE0		R26	R26		RE0
	RE1		R27	R27		RE1
	RE2	RE0	R20	R20	RE0	RE2
	RE3	RE1	R21	R21	RE1	RE3
	RE4	RE2	R22	R22	RE2	RE4
	RE5	RE3	R23	R23	RE3	RE5
	RE6	RE4	R24	R24	RE4	RE6
MSB	RE7	RE5	R25	R25	RE5	RE7
LSB	GE0		G26	G26		GE0
	GE1		G27	G27		GE1
	GE2	GE0	G20	G20	GE0	GE2
	GE3	GE1	G21	G21	GE1	GE3
	GE4	GE2	G22	G22	GE2	GE4
	GE5	GE3	G23	G23	GE3	GE5
	GE6	GE4	G24	G24	GE4	GE6
MSB	GE7	GE5	G25	G25	GE5	GE7
LSB	BE0		B26	B26		BE0
	BE1		B27	B27		BE1
	BE2	BE0	B20	B20	BE0	BE2
	BE3	BE1	B21	B21	BE1	BE3
	BE4	BE2	B22	B22	BE2	BE4
	BE5	BE3	B23	B23	BE3	BE5
	BE6	BE4	B24	B24	BE4	BE6
MSB	BE7	BE5	B25	B25	BE5	BE7

Table 4. SINGLE PIXEL PER CLOCK INPUT-TO-DUAL PIXEL PER CLOCK OUTPUT DATA MAPPING (DUAL=1/2VCC)

VGA - TFT Data Signals Color Bits			Transmitter input pin names	Receiver output pin names	TFT Panel Data Signals	
	24-bit	18-bit	DS90C387	DS90CF388	36-bit	48-bit
LSB	R0		R16	R16		RO0
	R1		R17	R17		RO1
	R2	R0	R10	R10	RO0	RO2
	R3	R1	R11	R11	RO1	RO3
	R4	R2	R12	R12	RO2	RO4
	R5	R3	R13	R13	RO3	RO5
	R6	R4	R14	R14	RO4	RO6
MSB	R7	R5	R15	R15	RO5	RO7
LSB	G0		G16	G16		GO0
	G1		G17	G17		GO1
	G2	G0	G10	G10	GO0	GO2
	G3	G1	G11	G11	GO1	GO3
	G4	G2	G12	G12	GO2	GO4
	G5	G3	G13	G13	GO3	GO5

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Table 4. SINGLE PIXEL PER CLOCK INPUT-TO-DUAL PIXEL PER CLOCK OUTPUT DATA MAPPING (DUAL=1/2VCC) (continued)

VGA - TFT Data Signals Color Bits			Transmitter input pin names	Receiver output pin names	TFT Panel Data Signals	
	G6	G4	G14	G14	GO4	GO6
MSB	G7	G5	G15	G15	GO5	GO7
LSB	B0		B16	B16		BO0
	B1		B17	B17		BO1
	B2	B0	B10	B10	BO0	BO2
	B3	B1	B11	B11	BO1	BO3
	B4	B2	B12	B12	BO2	BO4
	B5	B3	B13	B13	BO3	BO5
	B6	B4	B14	B14	BO4	BO6
MSB	B7	B5	B15	B15	BO5	BO7
			R16	R26		RE0
			R17	R27		RE1
			R10	R20	RE0	EO2
			R11	R21	RE1	RE3
			R12	R22	RE2	RE4
			R13	R23	RE3	RE5
			R14	R24	RE4	RE6
			R15	R25	RE5	RE7
			G16	G26		GE0
			G17	G27		GE1
			G10	G20	GE0	GE2
			G11	G21	GE1	GE3
			G12	G22	GE2	GE4
			G13	G23	GE3	GE5
			G14	G24	GE4	GE6
			G15	G25	GE5	GE7
			B16	B26		BE0
			B17	B27		BE1
			B10	B20	BE0	BE2
			B11	B21	BE1	BE3
			B12	B22	BE2	BE4
			B13	B23	BE3	BE5
			B14	B24	BE4	BE6
			B15	B25	BE5	BE7

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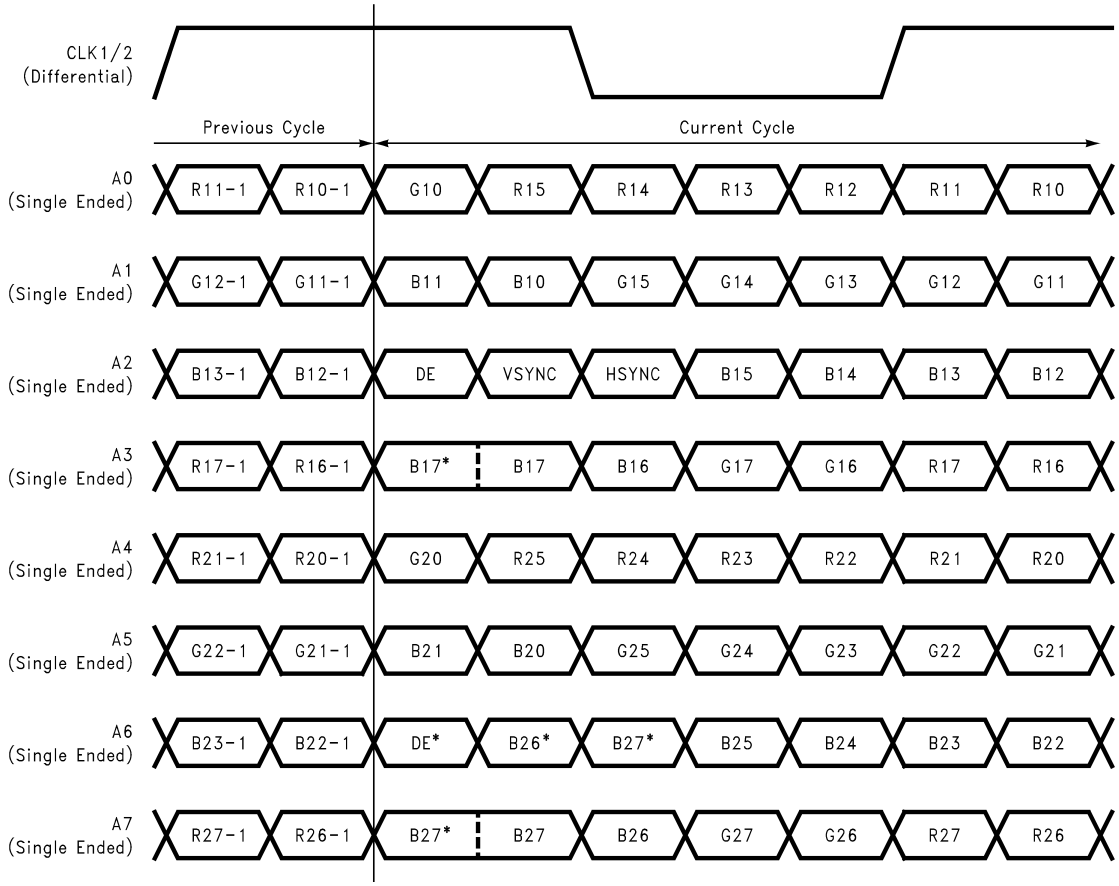

NOTE: Redundant copies of certain signals are also sent. These signals are denoted with an * symbol. The DS90CF388 does not sample the bits show with an * symbol. Optional feature supported: Pre-emphasis. See Applications Information for additional details.

Figure 17. TTL Data Inputs Mapped to LVDS Outputs
Non-DC Balanced Mode (Backward Compatible, BAL=Low)

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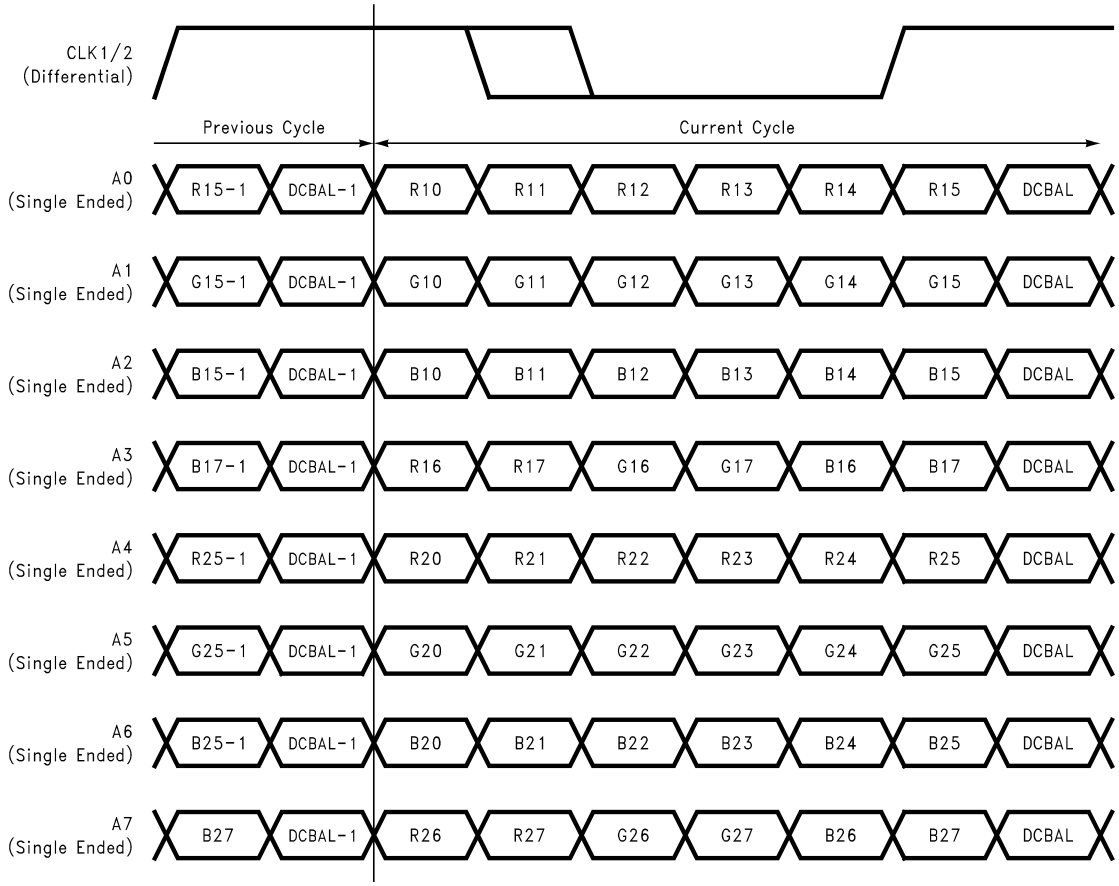

NOTE: The LVDS Clock signal is also DC Balanced in this mode. The rising edge location is fixed, but the location of the falling edge will be in one of two locations as shown above. Optional features supported: Pre-emphasis, and Deskew.

Figure 18. 48 Parallel TTL Data Inputs Mapped to LVDS Outputs DC Balanced Mode - Data Enabled, BAL=High

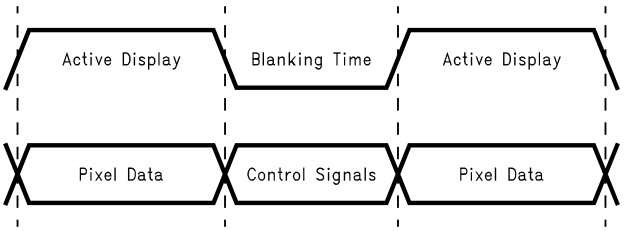

Figure 19. Control Signals Transmitted During Blanking

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Control Signal	Signal Level	Channel	Pattern
DE	HIGH	TxCLKOUT	1111000 or 1110000
	LOW		1111100 or 1100000
HSYNC	HIGH	TXOUT0	1100000 or 1111100
	LOW		1110000 or 1111000
VSYNC	HIGH	TXOUT1	1100000 or 1111100
	LOW		1110000 or 1111000
CNTLF	HIGH	TXOUT4	1100000 or 1111100
	LOW		1110000 or 1111000
CNTLE	HIGH	TXOUT5	1100000 or 1111100
	LOW		1110000 or 1111000

NOTE: The control signal during blanking shown above is for R_FDE=High, when R_FDE=Low all the low/high patterns are reversed.

Figure 20. Control Signals Transmitted During Blanking

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APPLICATIONS INFORMATION

HOW TO CONFIGURE THE DS90C387 AND DS90CF388 FOR MOST COMMON APPLICATION

1. To configure for single input pixel-to-dual pixel output application, the DS90C387 “DUAL” pin must be set to 1/2 Vcc=1.65V. This may be implemented using pull-up and pull-down resistors of 10kΩ each as shown in Figure 16. A capacitor between “DUAL” pin and ground will help to stabilize the DC voltage level in a noisy environment. In this configuration, the input signals (single pixel) are split into odd and even pixel (dual pixels) starting with the odd (first) pixel outputs A0-to-A3 the next even (second) pixel outputs to A4-to-A7. The splitting of the data signal also starts with DE (data enable) transitioning from logic low to high indicating active data. The "R_FDE" pin must be set high in this case. This is supported in DC Balanced and non-DC Balanced (BAL=low or high) data transmission. The number of clock cycles during blanking must be an EVEN number. This configuration will allow the user to interface to an LDI receiver (DS90CF388) or if in the non-DC Balanced mode (BAL=low) then two FPD-Link 'notebook' receivers (DS90CF384A). The DC Balance feature is recommended for monitor applications which require >2meters of cable length. Notebook applications should disable this feature to reduce the current consumption of the chipset. Note that only the DS90C387/DS90CF388 support the DC Balance data transmission feature.
2. To configure for single pixel or dual pixel application using the DS90C387/DS90CF388, the “DUAL” pin must be set to Vcc (dual) or Gnd (single). In dual mode, the transmitter-DS90C387 has two LVDS clock outputs enabling an interface to two FPD-Link 'notebook' receivers (DS90CF384A or DS90CF386). In single mode, outputs A4-to-A7 and CLK2 are disabled which reduces power dissipation. Both single and dual mode also support the DC Balance data transmission feature, which should only be used for monitor application.
3. The DS90CF388 is able to support single or dual pixel interface up to 112MHz operating frequency. This receiver may also be used to interface to a VGA controller with an integrated LVDS transmitter without DC Balance data transmission. In this case, the receivers “BAL” pin must be tied low (DC Balance disabled).

NEW FEATURES DESCRIPTION

Pre-Emphasis

Adds extra current during LVDS logic transition to reduce the cable loading effects. Pre-emphasis strength is set via a DC voltage level applied from min to max (0.75V to Vcc) at the “PRE” pin. A higher input voltage on the ”PRE” pin increases the magnitude of dynamic current during data transition. The “PRE” pin requires one pull-up resistor (Rpre) to Vcc in order to set the DC level. There is an internal resistor network, which cause a voltage drop. See Table 5 and Table 6 to set the voltage level.

Table 5. PRE-EMPHASIS DC VOLTAGE LEVEL WITH (RPRE)(1)

Rpre	Resulting PRE Voltage	Effects
1MΩ or NC	0.75V	Standard LVDS
50kΩ	1.0V	
9kΩ	1.5V	50% pre-emphasis
3kΩ	2.0V	
1kΩ	2.6V	
100Ω	Vcc	100% pre-emphasis

(1) This is based on testing with standard shield twisted pair cable. The amount of pre-emphasis will vary depending on the type of cable, length and operating frequency.

Table 6. PRE-EMPHASIS NEEDED PER CABLE LENGTH

Frequency	PRE Voltage	Typical cable length
112MHz	1.0V	2 meters
112MHz	1.5V	5 meters
80MHz	1.0V	2 meters
80MHz	1.2V	7 meters

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Table 6. PRE-EMPHASIS NEEDED PER CABLE LENGTH (continued)

Frequency	PRE Voltage	Typical cable length
65MHz	1.5V	10 meters
56MHz	1.0V	10 meters

DC Balance

In the Balanced operating modes, in addition to pixel and control information an additional bit is transmitted on every LVDS data signal line during each cycle of active data as shown in Figure 18. This bit is the DC Balance bit (DCBAL). The purpose of the DC Balance bit is to minimize the short- and long-term DC bias on the signal lines. This is achieved by selectively sending the pixel data either unmodified or inverted.

The value of the DC Balance bit is calculated from the running word disparity and the data disparity of the current word to be sent. The data disparity of the current word shall be calculated by subtracting the number of bits of value 0 from the number of bits value 1 in the current word. Initially, the running word disparity may be any value between +7 and −6. The running word disparity shall be calculated as a continuous sum of all the modified data disparity values, where the unmodified data disparity value is the calculated data disparity minus 1 if the data is sent unmodified and 1 plus the inverse of the calculated data disparity if the data is sent inverted. The value of the running word disparity shall saturate at +7 and −6.

The value of the DC Balance bit (DCBAL) shall be 0 when the data is sent unmodified and 1 when the data is sent inverted. To determine whether to send pixel data unmodified or inverted, the running word disparity and the current data disparity are used. If the running word disparity is positive and the current data disparity is positive, the pixel data shall be sent inverted. If the running word disparity is positive and the current data disparity is zero or negative, the pixel data shall be sent unmodified. If the running word disparity is negative and the current data disparity is positive, the pixel data shall be sent unmodified. If the running word disparity is negative and the current data disparity is zero or negative, the pixel data shall be sent inverted. If the running word disparity is zero, the pixel data shall be sent inverted.

Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. These enhancements allow cables 5 to 10+ meters in length to be driven.

CONTROL SIGNAL SENT DURING BLANKING (DC BALANCE MODE)

The data enable control signal (DE) is used in the DC Balanced mode to distinguish between pixel data and control information being sent. It must be continuously available to the device in order to correctly separate pixel data from control information. For this reason, DE shall be sent on the clock signals, LVDS CLK1 and CLK2, when operating in the DC Balanced mode. If the value of the control to be sent is 1 (active display), the value of the control word sent on the clock signals shall be 1111000 or 1110000. If the value of the control to be sent is 0 (blanking time), the value of the control word sent on the clock signals shall be 1111100 or 1100000. This is true when R_FDE=High. See Transmitter Pin Descriptions and Receiver Pin Descriptions.

The control information, such as HSYNC and VSYNC, is always sent unmodified. The value of the control word to send is determined by the running word disparity and the value of the control to be sent. If the running word disparity is positive and the value of the control to be sent is 0, the control word sent shall be 1110000. If the running word disparity is zero or negative and the control word to be sent is 0, the control word sent shall be 1111000. If the running word disparity is positive and the value of the control to be sent is 1, the control word sent shall be 1100000. If the running word disparity is zero or negative and the value of the control to be sent is 1, the control word sent shall be 1111100. The DC Balance bit shall be sent as 0 when sending control information during blanking time. See Figure 19.

RGB outputs on the DS90CF388 are forced LOW during the blanking time.

Note that in the backward compatible mode (BAL=low) control and data is sent as regular LVDS data. See Figure 17.

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SUPPORT OF CNTLE, CNTLF

The 387/388 will also support the transmission of one or two additional user-defined control signals in the 'dual pixel' DC Balanced output mode which are active during blanking while VSYNC is low. The additional control signals, referred to as CNTLE and CNTLF, should be multiplexed with data signals and provided to the transmitter inputs. Inputs B26 - CNTLF and B27 - CNTLE are designated for this purpose. When operating in 'DC Balanced' mode, controls (CNTLE, CNTLF) are transmitted on LVDS channels A4 and A5 during the blanking interval when VSYNC is low. CNTLE and CNTLF are sampled ONE (1) clock cycle after VSYNC transitions from a HIGH to a LOW state. CNTLE and CNTLF are sampled on each cycle until VSYNC transitions from a LOW to a HIGH, and they are then latched until the next VSYNC LOW cycle. Refer to Figure 20 for details. These signals may be active only during blanking while VSYNC is low. Control signal levels are latched and held in the last valid state when VSYNC transitions from low to high. These control signals are available as TTL outputs on the receiver. CNTLE and CNTLF outputs on the DS90CF388 should be left as a no connect (NC) when not used.

Deskew

The OpenLDI receiver (DS90CF388) is able to tolerate a minimum of 300ps skew between the signals arriving on a single differential pair (intra-pair) and a minimum of ±1 LVDS data bit time skew between signals arriving on dependent differential pair (pair-to-pair). This is supported in the DC Balance data transmission mode only. Each data channel is deskewed independently and is tuned with a step size of 1/3 of a bit time over a range of +/−1 TBIT. The Deskew feature operates up to clock rates of 80 MHz only. When using the DESKEW feature, the sampling strobe will remain within the middle third of the LVDS sub symbol.To complete the deskew operation, a minimum of four clock cycles is required during blanking time. This allows the chipset to support reduced blanking applications.

Backwards Compatible Mode with FPD-Link

The transmitter provides a second LVDS output clock. Both LVDS clocks will be identical in 'Dual pixel mode'. This feature supports backward compatibility with the previous generation of devices - the second clock allows the transmitter to interface to panels using a 'dual pixel' configuration of two 24-bit or 18-bit 'notebook' receivers.

Note that redundant copies of certain signals are also sent. These signals are denoted with an * symbol, and are shown in Figure 17. The DS90CF388 does not sample the bits show with an * symbol. If interfaceing with FPD-Link Receivers, these signals may be recovered if desired.

Pre-emphasis feature is available for use in both the DC Balanced and non-DC Balanced (backwards compatible) modes.

Transmitter Features

The transmitter is designed to reject cycle-to-cycle jitter which may be seen at the transmitter input clock. Very low cycle-to-cycle jitter is passed on to the transmitter outputs. Cycle-to-cycle jitter has been measured over frequency to be less than 100 ps with input step function jitter applied. This should be subtracted from the RSKM/RSKMD budget as shown and described in Figure 12 and Figure 13. This rejection capability significantly reduces the impact of jitter at the TXinput clock pin, and improves the accuracy of data sampling in the receiver. Transmitter output jitter is effected by PLLVCC noise and input clock jitter - minimize supply noise and use a low jitter clock source to limit output jitter. Timing and control signals (VSYNC, HSYNC, DE and two user-defined signals) are sent during blanking intervals to ensure correct reception of these critical signals.

The transmitter is offered with programmable edge data strobes for convenient interface with a variety of graphics controllers. The transmitter can be programmed for rising edge strobe or falling edge strobe through a dedicated pin. A rising edge transmitter will inter-operate with a falling edge receiver without any translation logic.

RSKM - Receiver Skew Margin

RSKM is a chipset parameter and is explained in AN-1059 (SNLA050) in detail. It is the difference between the transmitter's pulse position and the receiver's strobe window. RSKM must be greater than the summation of: Interconnect skew, LVDS Source Clock Jitter (TJCC), and ISI (if any). See Figure 12. Interconnect skew includes PCB traces differences, connector skew and cable skew for a cable application. PCB trace and connector skew can be compensated for in the design of the system. Cable skew is media type and length dependant.

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RSKMD - Receiver Skew Margin with DESKEW

RSKMD is a chipset parameter and is applicable when the DESKEW feature of the DS90CF388 is employed. It is the difference between the receiver's strobe window and the ideal pulse locations. The DESKEW feature adjusts for skew between each data channel and the clock channel. This feature is supported up to 80 MHz clock rate. RSKMD must be greater than the summation of: Transmitter's Pulse Position variance, LVDS Source Clock Jitter (TJCC), and ISI (if any). See Figure 12. With Deskew, RSKMD is ≥ 25% of TBIT. Deskew compensates for interconnect skew which includes PCB traces differences, connector skew and cable skew (for a cable application). PCB trace and connector skew can be compensated for in the design of the system. Note, cable skew is media type and length dependant. Cable length may be limited by the RSKMD parameter prior to the interconnect skew reaching 1 TBIT in length due to ISI effects.

POWER DOWN

Both transmitter and receiver provide a power down feature. When asserted current draw through the supply pins is minimized and the PLLs are shut down. The transmitter outputs are in TRI-STATE when in power down mode. The receiver outputs are forced to a active LOW state when in the power down mode. (See Transmitter Pin Descriptions and Receiver Pin Descriptions). The $\overline{PD}$ pin should be driven HIGH to enable the device once V_{CC} is stable.

DS90C387A/DS90CF388A

The DS90C387/CF388 chipset is electrically similar to the DS90C387A/CF388A. The DS90C387A/CF388A is recommended if support of longer cable drive is not required. DC Balance data transmission and cable deskew features are disabled to minimize overall power dissipation. The devices will also directly inter-operate with existing FPD-Link devices for backward compatibility.

Configuration Table

Table 7. TRANSMITTER / RECEIVER CONFIGURATION TABLE

Pin	Condition	Configuration
R_FB (Tx only)	R_FB = V_{CC}	Rising Edge Data Strobe
	R_FB = GND	Falling Edge Data Strobe
R_FDE (both Tx and Rx)	R_FDE = V_{CC}	Active data DE = High
	R_FDE = GND	Active data DE = Low
BAL (both Tx and Rx)	BAL=V_{CC}	DC Balanced enabled
	BAL=Gnd	DC Balanced disabled (backward compatible to FPD-Link)
DUAL (Tx only)	DUAL=V_{CC}	48-bit color (dual pixel) support
	DUAL=1/2V_{CC}	Single-to-dual support
	DUAL=Gnd	24-bit color (single pixel) support

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Pin Diagrams

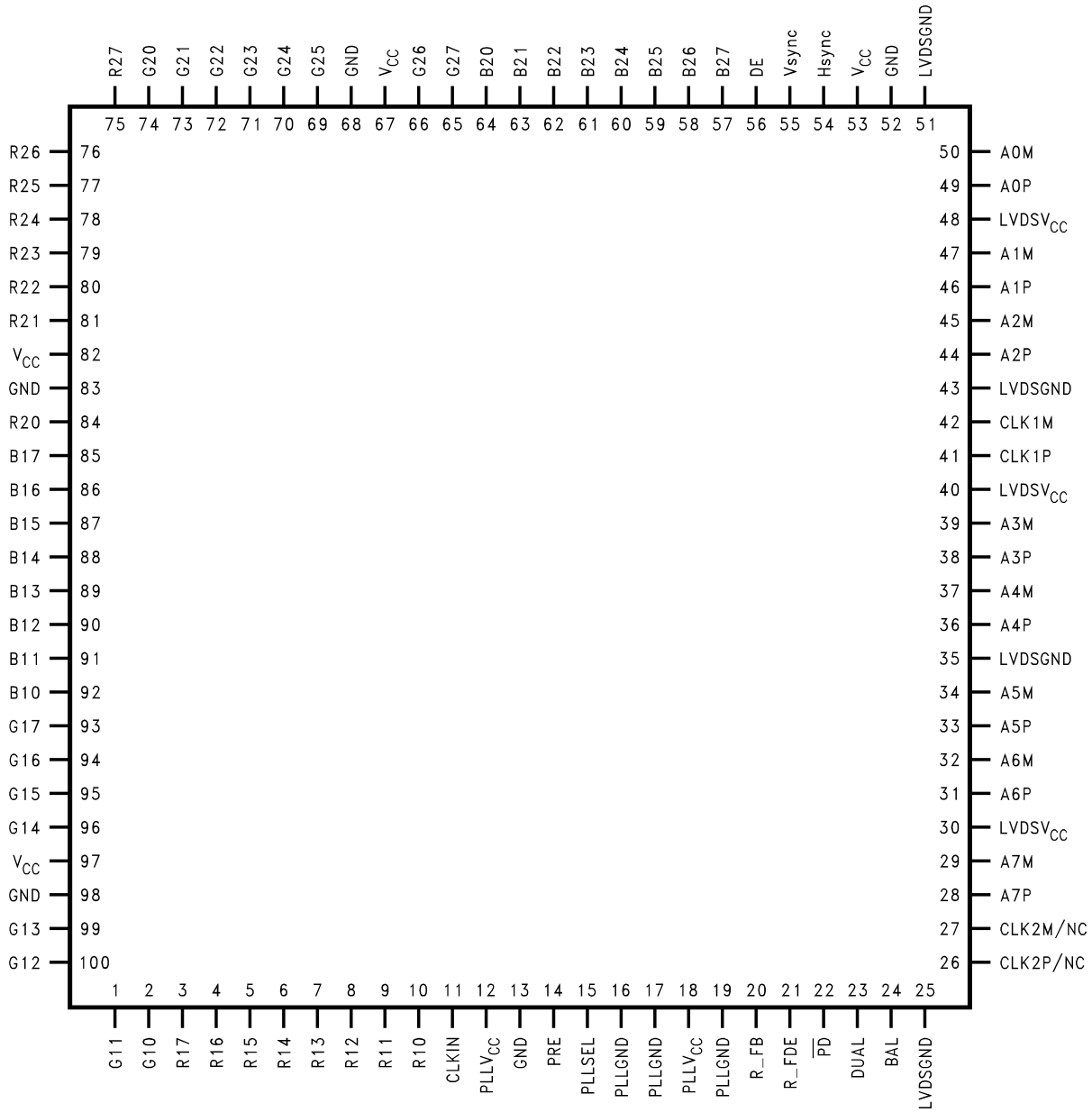

Figure 21. Transmitter-DS90C387
See Package Number NEZ0100A

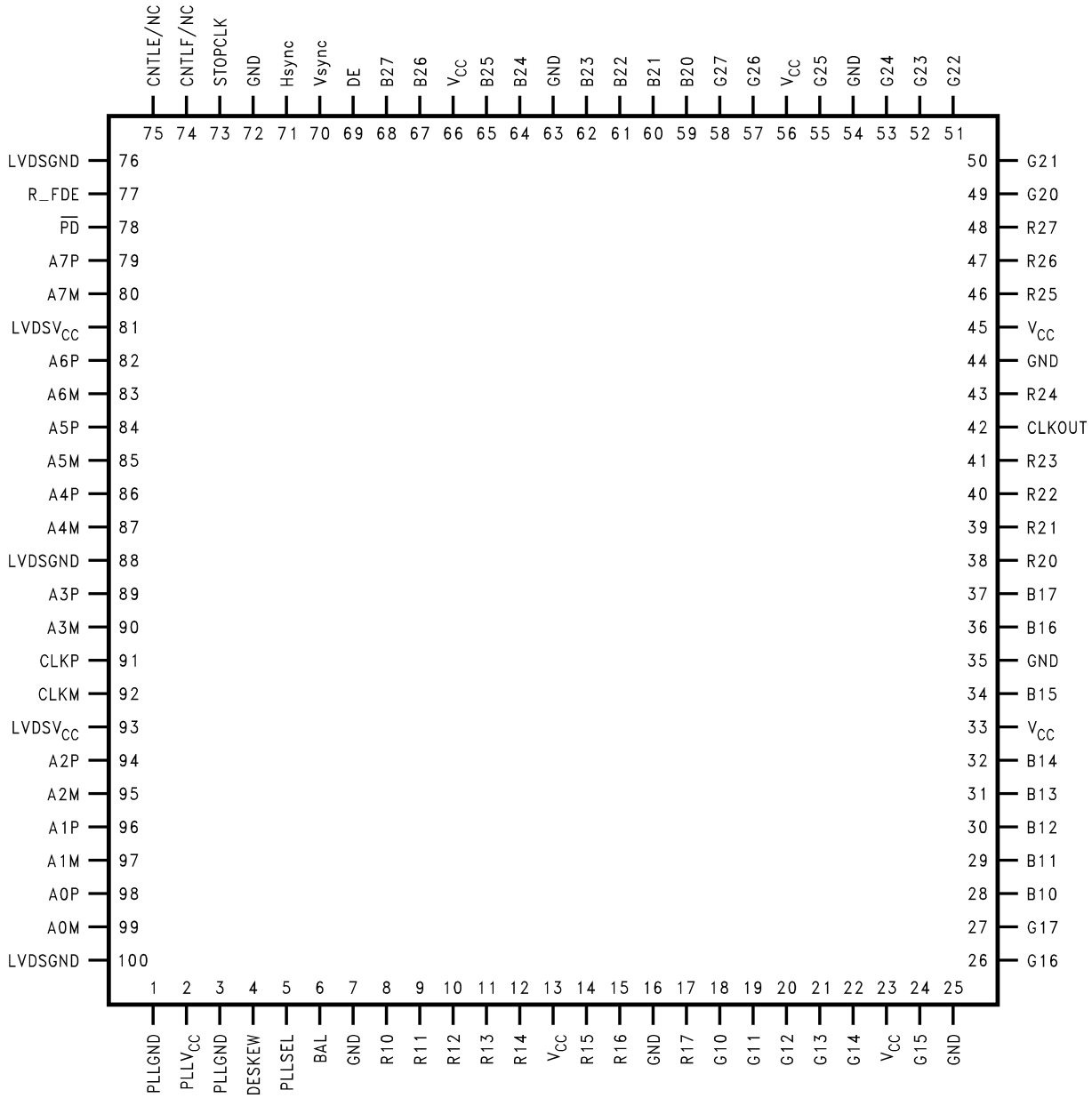

Figure 22. Receiver-DS90CF388
See Package Number NEZ0100A

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REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	26

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90C387VJD	NRND	TQFP	NEZ	100	90	TBD	Call TI	Call TI	-10 to 70	DS90C387VJD >B	
DS90C387VJD/NOPB	ACTIVE	TQFP	NEZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90C387VJD >B	Samples
DS90C387VJDX/NOPB	ACTIVE	TQFP	NEZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90C387VJD >B	Samples
DS90CF388VJD/NOPB	ACTIVE	TQFP	NEZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90CF388VJD >B	Samples
DS90CF388VJDX/NOPB	ACTIVE	TQFP	NEZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90CF388VJD >B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

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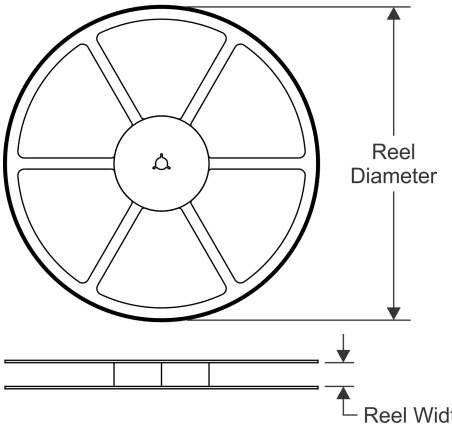
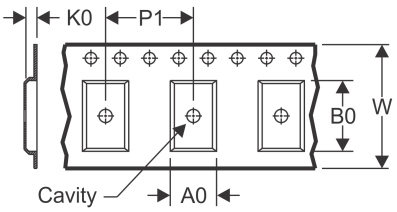
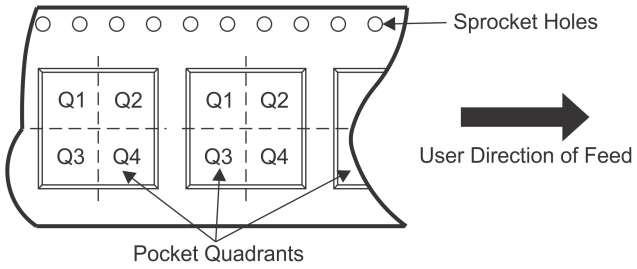


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

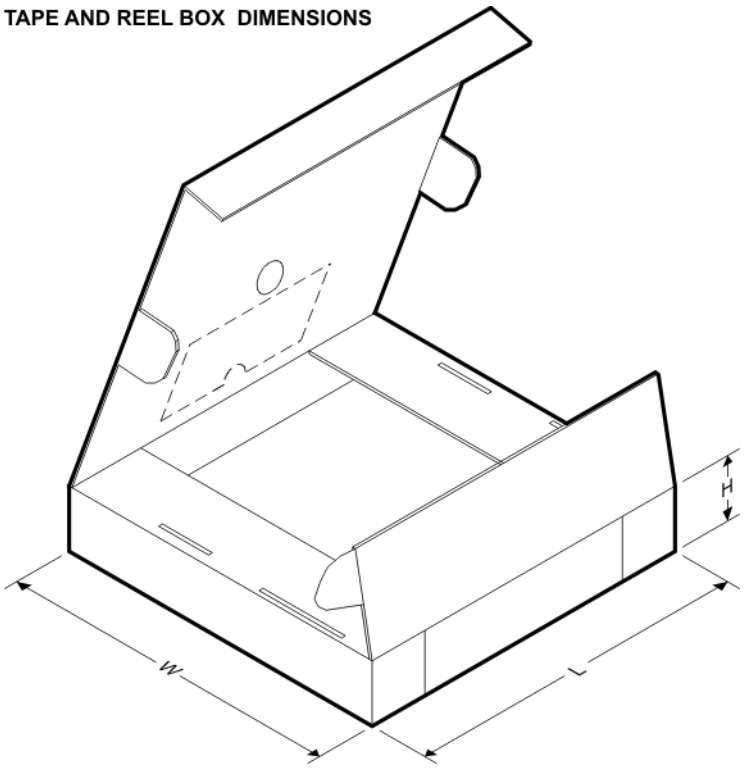
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C387VJDX/NOPB	TQFP	NEZ	100	1000	330.0	32.4	18.0	18.0	1.6	24.0	32.0	Q2
DS90CF388VJDX/NOPB	TQFP	NEZ	100	1000	330.0	32.4	18.0	18.0	1.6	24.0	32.0	Q2

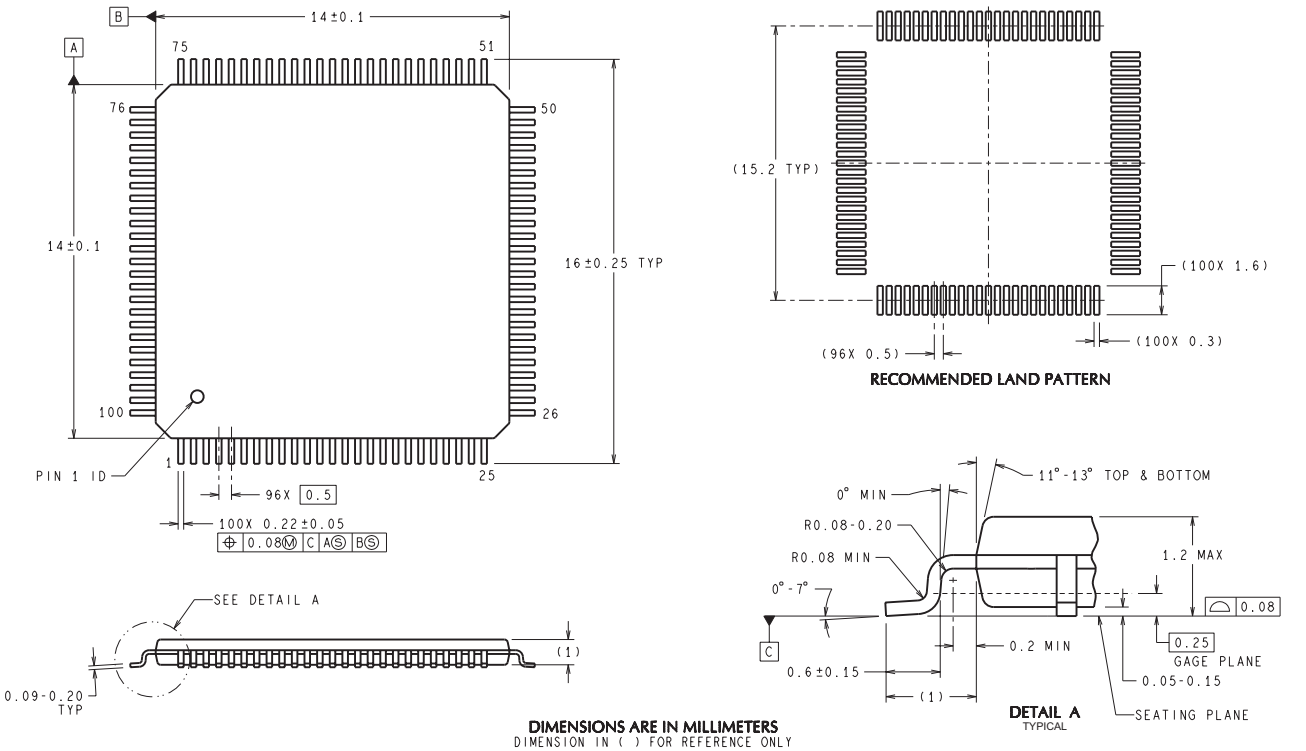
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C387VJDX/NOPB	TQFP	NEZ	100	1000	367.0	367.0	55.0
DS90CF388VJDX/NOPB	TQFP	NEZ	100	1000	367.0	367.0	55.0

PFD0100A



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