THE DATASHEET OF

DS90UR916QSQX/NOPB

www.win-source.net 0086-755-83957316

DS90UR916Q 5 - 65 MHz 24-bit Color FPD-Link II Deserializer with Image Enhancement

Check for Samples: DS90UR916Q

FEATURES

- **5 – 65 MHz PCLK support (140 Mbps – 1.82 Gbps)**
- **RGB888 + VS, HS, DE Support**
- **Image Enhancement - White Balance LUTs and Adaptive Hi-FRC Dithering**
- **AC Coupled STP Interconnect Cable up to 10 Meters**
- **@ Speed Link BIST Mode and Reporting Pin**
- **I2C Compatible Serial Control Bus**
- **Power Down Mode Minimizes Power Dissipation**
- **1.8V or 3.3V Compatible LVCMOS I/O Interface**
- **Automotive Grade Product: AEC-Q100 Grade 2 Qualified**
- **>8 kV HBM and ISO 10605 ESD Rating**
- **FAST Random Ddata Lock; No Reference Clock Required**
- **Adjustable Input Receiver Equalization**
- **LOCK (Real Time Link Status) Reporting Pin**
- **EMI Minimization on Output Parallel Bus (SSCG)**
- **Output Slew Control (OS)**
- **Backward Compatible Mode for Operation with Older Generation Devices**

APPLICATIONS

- **Automotive Display for Navigation**
- **Automotive Display for Entertainment**

DESCRIPTION

The DS90UR916Q FPD-Link II deserializer operates with the DS90UR905Q FPD-Link II serializer to deliver 24-bit digital video data over a single differential pair. The DS90UR916Q provides features designed to enhance image quality at the display. The high speed serial bus scheme of FPD-Link II greatly eases system design by eliminating skew problems between clock and data, reduces the number of connector pins, reduces the interconnect size, weight, and cost, and overall eases PCB layout. In addition, internal DC balanced decoding is used to support AC-coupled interconnects.

The DS90UR916Q Des (deserializer) recovers the data (RGB) and control signals and extracts the clock from the serial stream. The Des locks to the incoming serial data stream without the use of a training sequence or special SYNC patterns, and does not require a reference clock. A link status (LOCK) output signal is provided. The DS90UR916Q is ideally suited for 24-bit color applications. White balance lookup tables and adaptive Hi-FRC dithering provide the user a cost-effective means to enhance display image quality.

Serial transmission is optimized with user selectable receiver equalization. EMI is minimized by the use of low voltage differential signaling, output slew control, and the Des may be configured to generate Spread Spectrum Clock and Data on its parallel outputs.

The DS90UR916Qis offered in a 60-pin WQFN package. It is specified over the automotive AEC-Q100 grade 2 temperature range of -40°C to +105°C.

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Applications Diagram

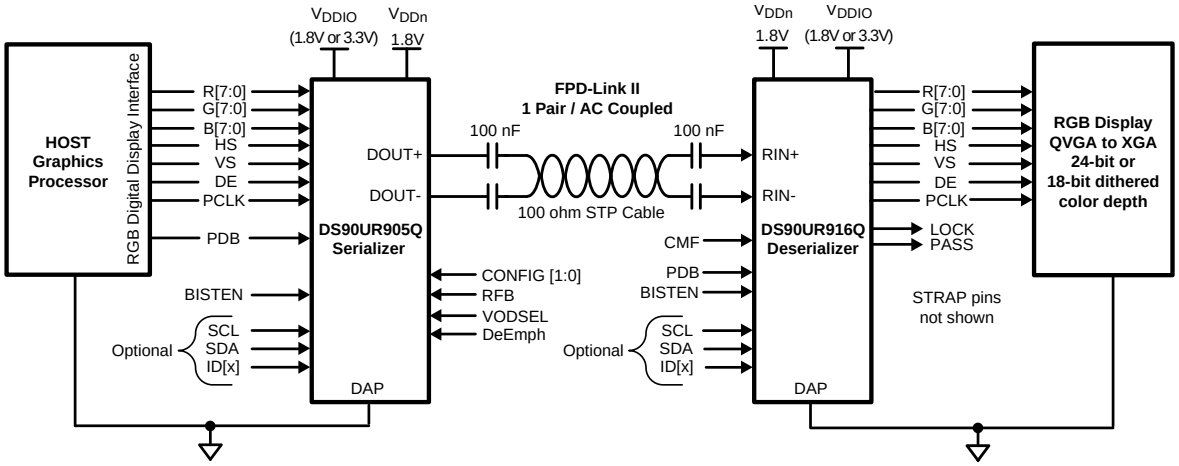

Figure 1.

Block Diagrams

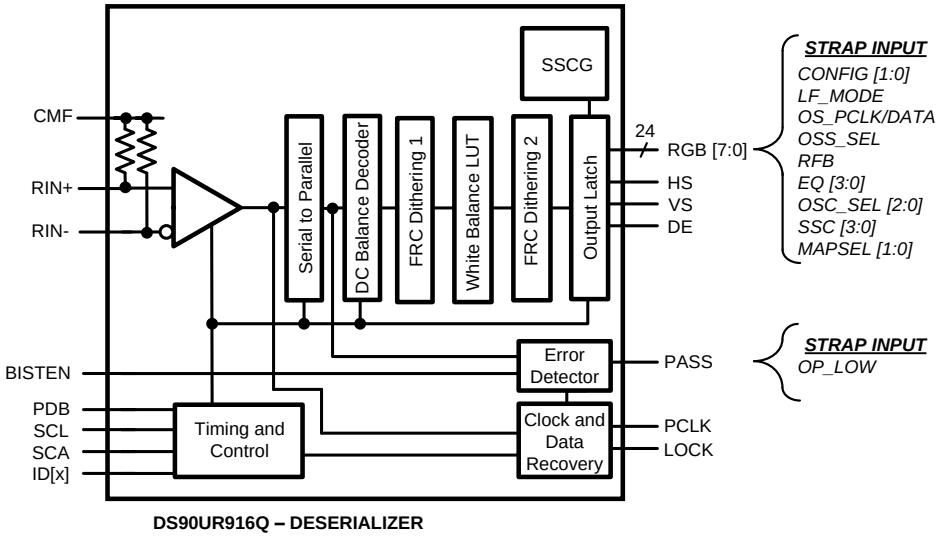

Figure 2.

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DS90UR916Q Pin Diagram

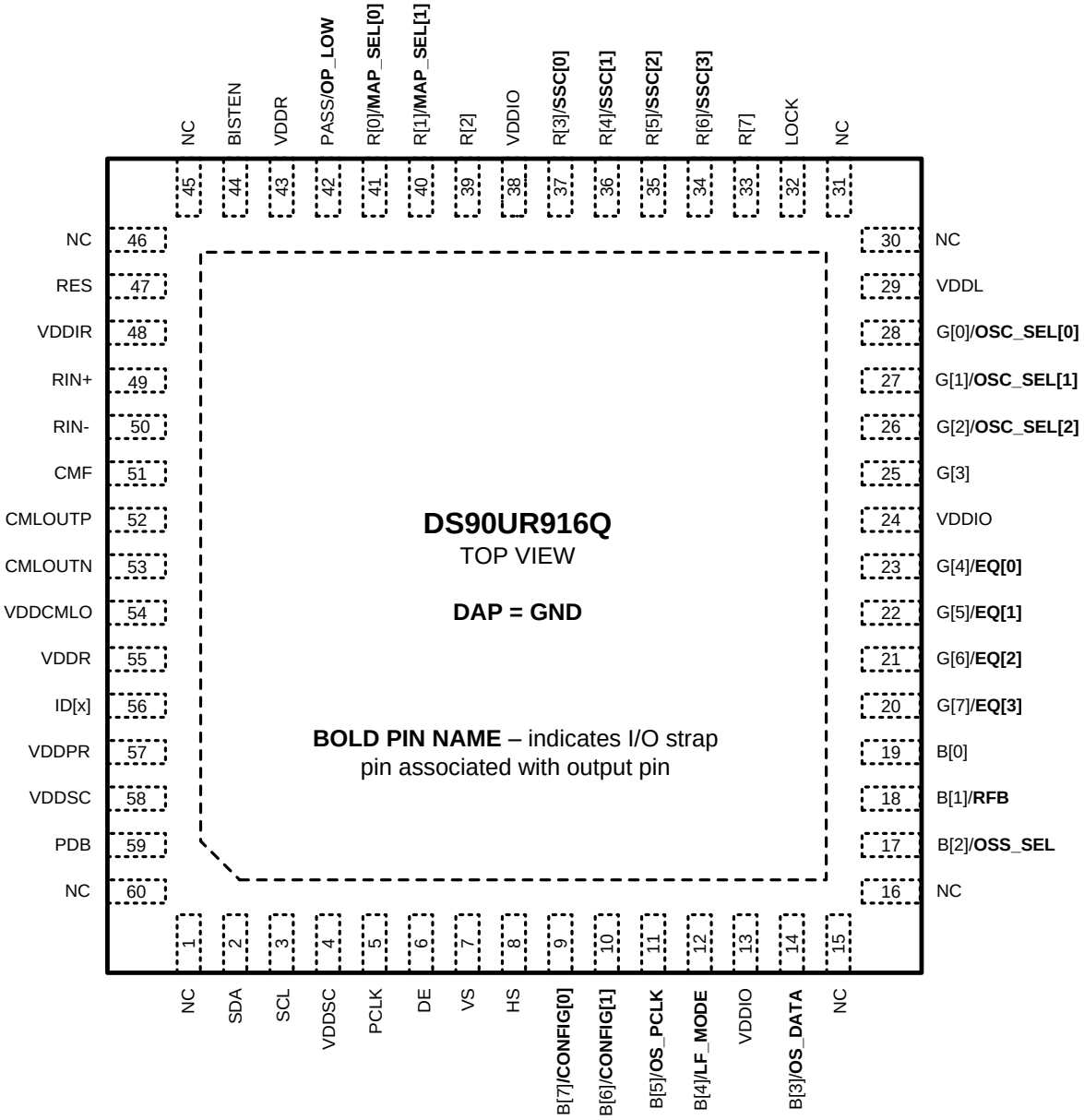

Figure 3. Deserializer - DS90UR916Q — Top View

DS90UR916Q Deserializer Pin Descriptions[1]

Pin Name	Pin #	I/O, Type	Description
LVCMOS Parallel Interface			
R[7:0]	33, 34, 35, 36, 37, 39, 40, 41	I, STRAP, O, LVCMOS	RED Parallel Interface Data Output Pins (MSB = 7, LSB = 0) In power-down (PDB = 0), outputs are controlled by the OSS_SEL (See Table 5). These pins are inputs during power-up (See STRAP Inputs).
G[7:0]	20, 21, 22, 23, 25, 26, 27, 28	I, STRAP, O, LVCMOS	GREEN Parallel Interface Data Output Pins (MSB = 7, LSB = 0) In power-down (PDB = 0), outputs are controlled by the OSS_SEL (See Table 5). These pins are inputs during power-up (See STRAP Inputs).
B[7:0]	9, 10, 11, 12, 14, 17, 18, 19	I, STRAP, O, LVCMOS	BLUE Parallel Interface Data Output Pins (MSB = 7, LSB = 0) In power-down (PDB = 0), outputs are controlled by the OSS_SEL (See Table 5). These pins are inputs during power-up (See STRAP Inputs).
HS	8	O, LVCMOS	Horizontal Sync Output In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See Table 5). Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 PCLKs.
VS	7	O, LVCMOS	Vertical Sync Output In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See Table 5). Video control signal is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
DE	6	O, LVCMOS	Data Enable Output In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See Table 5). Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 PCLKs.
PCLK	5	O, LVCMOS	Pixel Clock Output In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See Table 5). Strobe edge set by RFB function.
LOCK	32	O, LVCMOS	LOCK Status Output LOCK = 1, PLL is Locked, outputs are active LOCK = 0, PLL is unlocked, RGB[7:0], HS, VS, DE and PCLK output states are controlled by OSS_SEL (See Table 5). May be used as Link Status or to flag when Video Data is active (ON/OFF).
PASS	42	O, LVCMOS	PASS Output (BIST Mode) PASS = 1, error free transmission PASS = 0, one or more errors were detected in the received payload Route to test point for monitoring, or leave open if unused.
Control and Configuration — STRAP PINS For a High State, use a 10 kΩ pull up to V_{DDIO}; for a Low State, the IO includes an internal pull down. The STRAP pins are read upon power-up and set device configuration. Pin Number listed along with shared RGB Output name in square brackets.			
CONFIG[1:0]	10 [B6], 9 [B7]	STRAP I, LVCMOS w/ pull-down	Operating Modes — Pin or Register Control These pins determine the DS90UR916's operating mode and interfacing device. CONFIG[1:0] = 00: Interfacing to DS90UR905, Control Signal Filter DISABLED CONFIG[1:0] = 01: Interfacing to DS90UR905, Control Signal Filter ENABLED CONFIG[1:0] = 10: Interfacing to DS90UR241 CONFIG[1:0] = 11: Interfacing to DS90C241
LF_MODE	12 [B4]	STRAP I, LVCMOS w/ pull-down	SSCG Low Frequency Mode — Pin or Register Control Only required when SSCG is enabled, otherwise LF_MODE condition is a DON'T CARE (X). LF_MODE = 1, SSCG in low frequency mode (PCLK = 5-20 MHz) LF_MODE = 0, SSCG in high frequency mode (PCLK = 20-65 MHz)
OS_PCLK	11 [B5]	STRAP I, LVCMOS w/ pull-down	PCLK Output Slew Select — Pin or Register Control OS_PCLK = 1, increased PCLK slew OS_PCLK = 0, normal (default)
OS_DATA	14 [B3]	STRAP I, LVCMOS w/ pull-down	Data Output Slew Select — Pin or Register Control OS_DATA = 1, increased DATA slew OS_DATA = 0, normal (default)

(1) 1 = HIGH, 0 = LOW.

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DS90UR916Q Deserializer Pin Descriptions(1) (continued)

Pin Name	Pin #	I/O, Type	Description
OP_LOW	42 PASS	STRAP I, LVCMOS w/ pull-down	Outputs held Low when LOCK = 1 — Pin or Register Control NOTE: IT IS NOT RECOMMENDED TO USE ANY OTHER STRAP OPTIONS WITH THIS STRAP FUNCTION OP_LOW = 1: all outputs are held LOW during power up until released by programming OP_LOW release/set register HIGH NOTE: Before the device is powered up, the outputs are in tri-state. See Figure 23 and Figure 24. OP_LOW = 0: all outputs toggle normally as soon as LOCK goes HIGH (default).
OSS_SEL	17 [B2]	STRAP I, LVCMOS w/ pull-down	Output Sleep State Select — Pin or Register Control NOTE: OSS_SEL STRAP CANNOT BE USED IF OP_LOW =1 OSS_SEL is used in conjunction with PDB to determine the state of the outputs when inactive. (See Table 5).
RFB	18 [B1]	STRAP I, LVCMOS w/ pull-down	Pixel Clock Output Strobe Edge Select — Pin or Register Control RFB = 1, parallel interface data and control signals are strobed on the rising clock edge. RFB = 0, parallel interface data and control signals are strobed on the falling clock edge.
EQ[3:0]	20 [G7], 21 [G6], 22 [G5], 23 [G4]	STRAP I, LVCMOS w/ pull-down	Receiver Input Equalization — Pin or Register Control (See Table 2).
OSC_SEL[2:0]	26 [G2], 27 [G1], 28 [G0]	STRAP I, LVCMOS w/ pull-down	Oscillator Select — Pin or Register Control (See Table 6 and Table 7).
SSC[3:0]	34 [R6], 35 [R5], 36 [R4], 37 R[3]	STRAP I, LVCMOS w/ pull-down	Spread Spectrum Clock Generation (SSCG) Range Select — Pin or Register Control (See Table 3 and Table 4).
MAP_SEL[1:0]	40 [R1], 41 [R0]	STRAP I, LVCMOS w/ pull-down	Bit Mapping Backward Compatibility / DS90UR241 Options — Pin or Register Control Normal setting to b'00. See (Table 8).
Control and Configuration			
PDB	59	I, LVCMOS w/ pull-down	Power Down Mode Input PDB = 1, Des is enabled (normal operation). Refer to POWER UP REQUIREMENTS AND PDB PIN in the Applications Information Section. PDB = 0, Des is in power-down. When the Des is in the power-down state, the LVCMOS output state is determined by Table 5. Control Registers are **RESET**.
ID[x]	56	I, Analog	Serial Control Bus Device ID Address Select — Optional Resistor to Ground and 10 kΩ pull-up to 1.8V rail. (See Table 9).
SCL	3	I, LVCMOS	Serial Control Bus Clock Input - Optional SCL requires an external pull-up resistor to V_{DDIO}.
SDA	2	I/O, LVCMOS Open Drain	Serial Control Bus Data Input / Output - Optional SDA requires an external pull-up resistor to V_{DDIO}.
BISTEN	44	I, LVCMOS w/ pull-down	BIST Enable Input — Optional BISTEN = 1, BIST is enabled BISTEN = 0, BIST is disabled
RES	47	I, LVCMOS w/ pull-down	***Reserved*** - tie LOW
NC	1, 15, 16, 30, 31, 45, 46, 60		Not Connected Leave pin open (float)

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DS90UR916Q Deserializer Pin Descriptions(1) (continued)

Pin Name	Pin #	I/O, Type	Description
FPD-Link II Serial Interface			
RIN+	49	I, LVDS	True Input. The input must be AC Coupled with a 100 nF capacitor.
RIN-	50	I, LVDS	Inverting Input. The input must be AC Coupled with a 100 nF capacitor.
CMF	51	I, Analog	Common-Mode Filter VCM center-tap is a virtual ground which may be ac-coupled to ground to increase receiver common mode noise immunity. Recommended value is 4.7 µF or higher.
CMLOUTP	52	O, LVDS	Test Monitor Pin — EQ Waveform NC or connect to test point. Requires Serial Bus Control to enable.
CMLOUTN	53	O, LVDS	Test Monitor Pin — EQ Waveform NC or connect to test point. Requires Serial Bus Control to enable.
Power and Ground(2)			
VDDL	29	Power	Logic Power, 1.8 V ±5%
VDDIR	48	Power	Input Power, 1.8 V ±5%
VDDR	43, 55	Power	RX High Speed Logic Power, 1.8 V ±5%
VDDSC	4, 58	Power	SSCG Power, 1.8 V ±5%
VDDPR	57	Power	PLL Power, 1.8 V ±5%
VDDCMLO	54	Power	RX High Speed Logic Power, 1.8 V ±5%
VDDIO	13, 24, 38	Power	LVCMOS I/O Power, **1.8 V ±5% OR 3.3 V ±10%** (V_{DDIO})
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. **Connected to the ground plane** (GND) with at least 9 vias.

(2) The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage – V_{DDn} (1.8V)		−0.3V to +2.5V
Supply Voltage – V_{DDIO}		−0.3V to +4.0V
LVCMOS I/O Voltage		−0.3V to +(VDDIO + 0.3V)
Receiver Input Voltage		−0.3V to (VDD + 0.3V)
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C
60L WQFN Package	Maximum Power Dissipation Capacity at 25°C 470mW	470mW
	Derate above 25C	$1/\theta_{JA}$ mW / °C
	θ_{JA}(based on 9 thermal vias)	24.6 °C/W
	θ_{JC}(based on 9 thermal vias)	2.8 °C/W
ESD Rating (HBM)		≥±8 kV
ESD Rating (CDM)		≥±1 kV
ESD Rating (MM)		≥±250 V
ESD Rating (ISO10605), R_D = 2kΩ, C_S = 150pF or R_D = 2kΩ, C_S = 330pF or R_D = 330Ω, C_S = 150pF		
Air Discharge (R_{IN+}, R_{IN-})		≥±30 kV
Contact Discharge (R_{IN+}, R_{IN-})		≥±10 kV
ESD Rating (ISO10605), R_D = 330Ω, C_S = 330pF		
Air Discharge (R_{IN+}, R_{IN-})		≥±15 kV
Contact Discharge (R_{IN+}, R_{IN-})		≥±10 kV
ESD Rating (IEC 61000–4–2), R_D = 330Ω, C_S = 150pF		
Air Discharge (R_{IN+}, R_{IN-})		≥±25 kV
Contact Discharge (R_{IN+}, R_{IN-})		≥±10 kV
For soldering specifications see product folder at www.ti.com and SNOA549		

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
PCLK Clock Frequency	5		65	MHz
Supply Noise[1]			50	mV_{P-P}

(1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8V) supply with amplitude = 100 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 750 kHz. The Des on the other hand shows no error when the noise frequency is less than 400 kHz.

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Deserializer DC Electrical Characteristics (1)(2)(3)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
3.3 V I/O LVCMOS DC SPECIFICATIONS – V_{DDIO} = 3.0 to 3.6V							
V_{IH}	High Level Input Voltage		PDB, BISTEN	2.2		V_{DDIO}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}		−15	±1	+15	µA
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, OS_PCLK/DATA = L	R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, LOCK, PASS	2.4	V_{DDIO}		V
V_{OL}	Low Level Output Voltage	I_{OL} = +2 mA, OS_PCLK/DATA = L	R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, LOCK, PASS	GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{DDIO} = 3.3V V_{OUT} = 0V, OS_PCLK/DATA = L/H	PCLK		36		mA
	Output Short Circuit Current	V_{DDIO} = 3.3V V_{OUT} = 0V OS_PCLK/DATA = L/H	Des Outputs		37		mA
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, OSS_SEL = 0V, V_{OUT} = 0V or V_{DDIO}	Outputs	−15		+15	µA
1.8 V I/O LVCMOS DC SPECIFICATIONS – V_{DDIO} = 1.71 to 1.89V							
V_{IH}	High Level Input Voltage		PDB, BISTEN	1.235		V_{DDIO}	V
V_{IL}	Low Level Input Voltage			GND		0.595	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}		−15	±1	+15	µA
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, OS_PCLK/DATA = L	R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, LOCK, PASS	V_{DDIO} − 0.45	V_{DDIO}		V
V_{OL}	Low Level Output Voltage	I_{OL} = +2 mA, OS_PCLK/DATA = L		GND		0.45	V
I_{OS}	Output Short Circuit Current	V_{DDIO} = 1.8V V_{OUT} = 0V OS_PCLK/DATA = L/H	PCLK		18		mA
	Output Short Circuit Current	V_{DDIO} = 1.8V V_{OUT} = 0V OS_PCLK/DATA = L/H	Des Outputs		18		mA
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, OSS_SEL = 0V, V_{OUT} = 0V or V_{DDIO}	Outputs	-15		+15	µA
V_{TH}	Differential Input Threshold High Voltage	V_{CM} = +1.2V (Internal V_{BIAS})	RIN+, RIN-	+50			mV
V_{TL}	Differential Input Threshold Low Voltage			−50			mV
V_{CM}	Common Mode Voltage, Internal V_{BIAS}				1.2		V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}		-15		+15	µA
R_T	Internal Termination Resistor			80	100	120	Ω

(1) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

(2) Typical values represent most likely parametric norms at V_{DD} = 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(3) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

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Deserializer DC Electrical Characteristics[1][2][3] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
CML DRIVER OUTPUT DC SPECIFICATIONS – EQ TEST PORT								
V_{OD}	Differential Output Voltage	R_L = 100Ω		CMLOUTP, CMLOUTN		542		mV
V_{OS}	Offset Voltage Single-ended	R_L = 100Ω				1.4		V
R_T	Internal Termination Resistor				80	100	120	Ω
SUPPLY CURRENT								
I_{DD1}	Deserializer Supply Current (includes load current)	Checker Board Pattern, OS_PCLK/DATA = H, EQ = 001, SSCG=ON,CMLOUTP/N enabled C_L = 4pF, Figure 4	V_{DD}= 1.89V	All V_{DD} pins		93	110	mA
I_{DDIO1}			V_{DDIO}=1.89V	V_{DDIO}		33	45	mA
			V_{DDIO} = 3.6V			62	75	mA
I_{DDZ}	Deserializer Supply Current Power Down	PDB = 0V, All other LVCMOS Inputs = 0V	V_{DD}= 1.89V	All V_{DD} pins		40	3000	µA
			V_{DDIO}=1.89V	V_{DDIO}		5	50	µA
I_{DDIOZ}			V_{DDIO} = 3.6V			10	100	µA

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	PCLK Output Period		PCLK	15.38	T	200	ns
t_{RDC}	PCLK Output Duty Cycle	SSCG=OFF, 5–65MHz	PCLK	43	50	57	%
		SSCG=ON, 5–20MHz		35	59	65	%
		SSCG=ON, 20–65MHz		40	53	60	%
t_{CLH}	LVCMOS Low-to-High Transition Time, Figure 5	V_{DDIO} = 1.8V C_L = 4 pF (lumped load)	PCLK/RGB[7:0], HS, VS, DE		2.1		ns
		V_{DDIO} = 3.3V C_L = 4 pF (lumped load)			2.0		ns
t_{CHL}	LVCMOS High-to-Low Transition Time, Figure 5	V_{DDIO} = 1.8V C_L = 4 pF (lumped load)	PCLK/RGB[7:0], HS, VS, DE		1.6		ns
		V_{DDIO} = 3.3V C_L = 4 pF (lumped load)			1.5		ns
t_{ROS}	Data Valid before PCLK – Set Up Time, Figure 9	V_{DDIO} = 1.71 to 1.89V or 3.0 to 3.6V C_L = 4 pF (lumped load)	RGB[7:0], HS, VS, DE	0.27	0.45		T
t_{ROH}	Data Valid after PCLK – Hold Time, Figure 9	V_{DDIO} = 1.71 to 1.89V or 3.0 to 3.6V C_L = 4 pF (lumped load)	RGB[7:0], HS, VS, DE	0.4	0.55		T
t_{HBLANK}	Horizontal Blanking Time		HS	6			t_{RCP}
t_{DDLT}	Deserializer Lock Time, Figure 8	SSC[3:0] = 0000 (OFF)[1]	PCLK = 5 MHz		3		ms
		SSC[3:0] = 0000 (OFF)[1]	PCLK = 65MHz		4		ms
		SSC[3:0] = ON[1]	PCLK = 5MHz		30		ms
		SSC[3:0] = ON[1]	PCLK = 65MHz		6		ms
t_{DD}	Des Delay - Latency, Figure 6				139*T	140*T	ns
t_{DPJ}[2]	Des Period Jitter	SSC[3:0] = OFF[3][4]	PCLK = 5 MHz		975	1700	ps
			PCLK = 10 MHz		500	1000	ps
			PCLK = 65 MHz		550	1250	ps

(1) t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active PCLK.
(2) Specification is ensured by design and is not tested in production.
(3) t_{DPJ} is the maximum amount the period is allowed to deviate over many samples.
(4) Specification is ensured by characterization and is not tested in production.

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Deserializer Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{DCCJ} (2)	Des Cycle-to-Cycle Jitter	SSC[3:0] = OFF (4) (5)	PCLK = 5 MHz		675	1150	ps
			PCLK = 10 MHz		375	900	ps
			PCLK = 65 MHz		500	1150	ps
t_{RJIT}	Des Input Jitter Tolerance, Figure 11	EQ = OFF, SSCG = OFF, PCLK = 65MHz	for jitter freq < 2MHz		0.9		UI (6)
			for jitter freq > 6MHz		0.5		UI
BIST Mode							
t_{PASS}	BIST PASS Valid Time, BISTEN = 1, Figure 12				1	10	ns
SSCG Mode							
f_{DEV}	Spread Spectrum Clocking Deviation Frequency		PCLK = 5 to 65 MHz, SSC[3:0] = ON	±0.5		±2	%
f_{MOD}	Spread Spectrum Clocking Modulation Frequency		PCLK = 5 to 65 MHz, SSC[3:0] = ON	8		100	kHz

(5) t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles.
(6) UI – Unit Interval is equivalent to one serialized data bit width (1UI = 1 / 28*PCLK). The UI scales with PCLK frequency.

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Recommended Timing for the Serial Control Bus

Over +3.3V supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	Standard Mode	>0		100	kHz
		Fast Mode	>0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_{HIGH}	SCL High Period	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{HD;STA}$	Hold time for a start or a repeated start condition, Figure 13	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{SU:STA}$	Set Up time for a start or a repeated start condition, Figure 13	Standard Mode	4.7			us
		Fast Mode	0.6			us
$t_{HD;DAT}$	Data Hold Time, Figure 13	Standard Mode	0		3.45	us
		Fast Mode	0		0.9	us
$t_{SU;DAT}$	Data Set Up Time, Figure 13	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Set Up Time for STOP Condition, Figure 13	Standard Mode	4.0			us
		Fast Mode	0.6			us
t_{BUF}	Bus Free Time Between STOP and START, Figure 13	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_r	SCL & SDA Rise Time, Figure 13	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time, Figure 13	Standard Mode			300	ns
		Fast mode			300	ns

DC and AC Serial Control Bus Characteristics

Over 3.3V supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL	2.2		V_{DDIO}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.8	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}		SDA, IOL = 1.25mA	0		0.4	V
I_{in}		SDA or SCL, Vin = V_{DDIO} or GND	-15		+15	µA
t_R	SDA RiseTime – READ	SDA, RPU = X, Cb ≤ 400pF		40		ns
t_F	SDA Fall Time – READ			25		ns
$t_{SU;DAT}$	Set Up Time — READ			520		ns
$t_{HD;DAT}$	Hold Up Time — READ			55		ns
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

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AC Timing Diagrams and Test Circuits

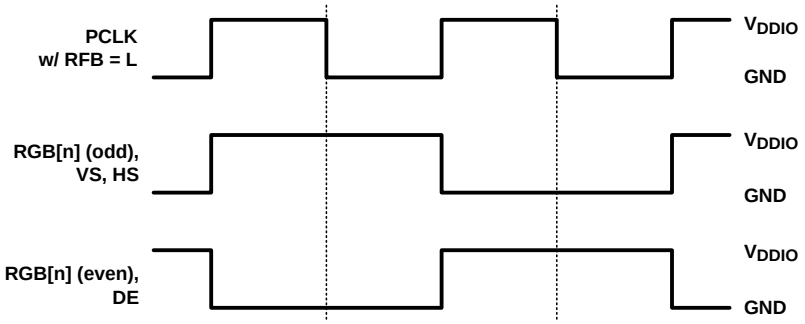

Figure 4. Checkerboard Data Pattern

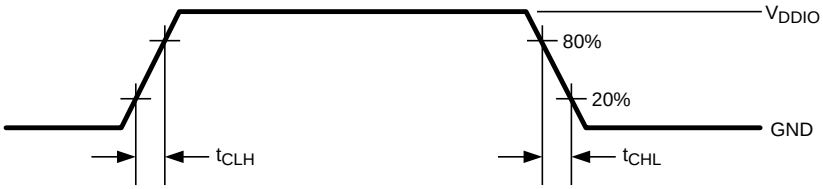

Figure 5. Deserializer LVCMOS Transition Times

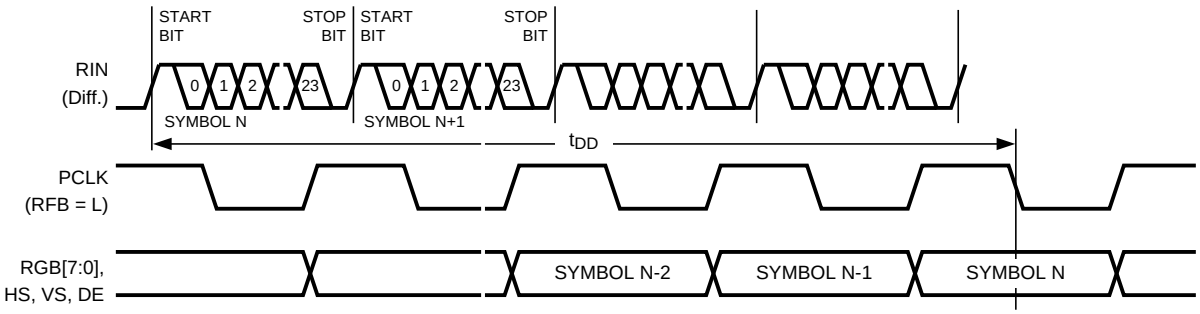

Figure 6. Deserializer Delay – Latency

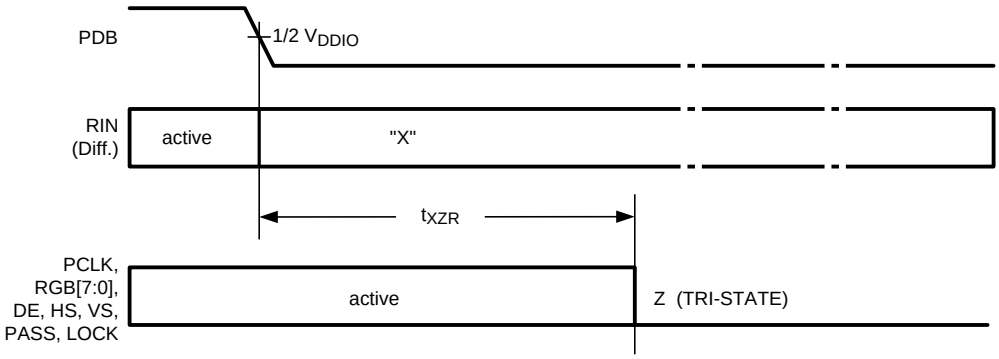

Figure 7. Deserializer Disable Time (OSS_SEL = 0)

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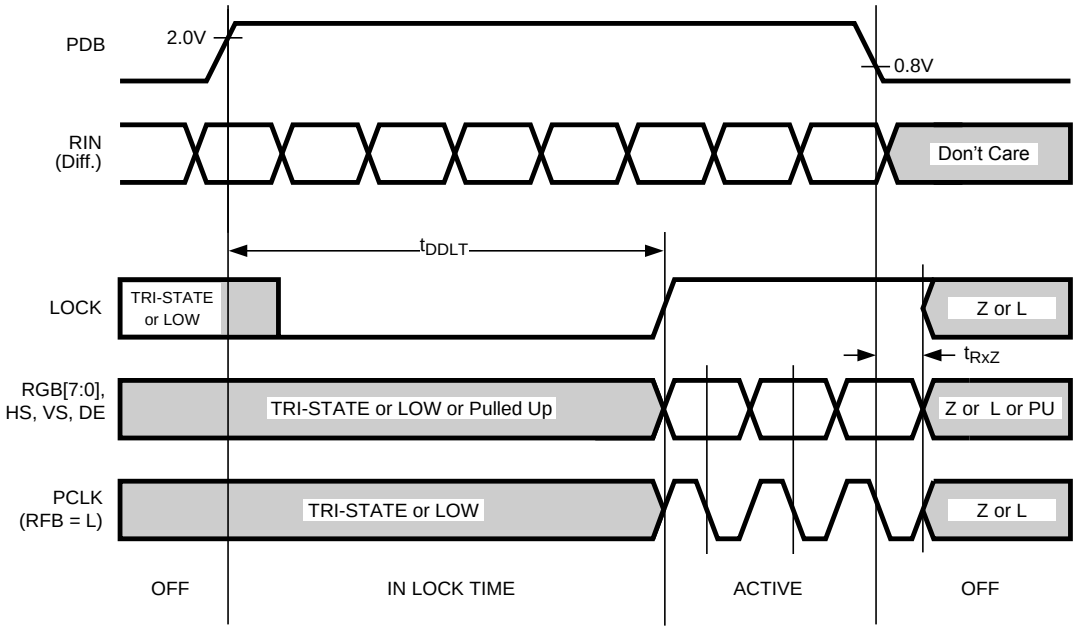

Figure 8. Deserializer PLL Lock Times and PDB TRI-STATE Delay(1)

Note: (1) When the Serializer output is at TRI-STATE the Deserializer will lose PLL lock. Resynchronization / Relock must occur before data transfer require t_{PLD}

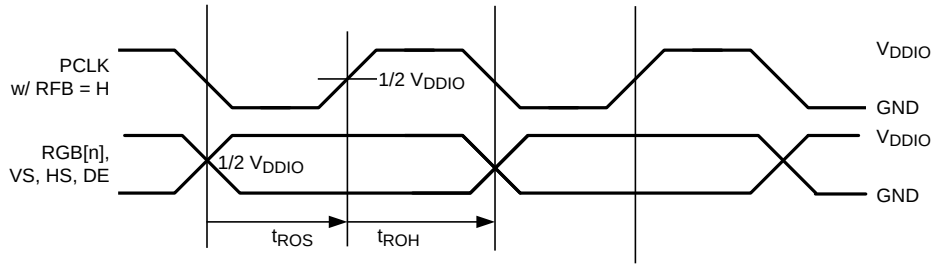

Figure 9. Deserializer Output Data Valid (Setup and Hold) Times with SSCG = Off

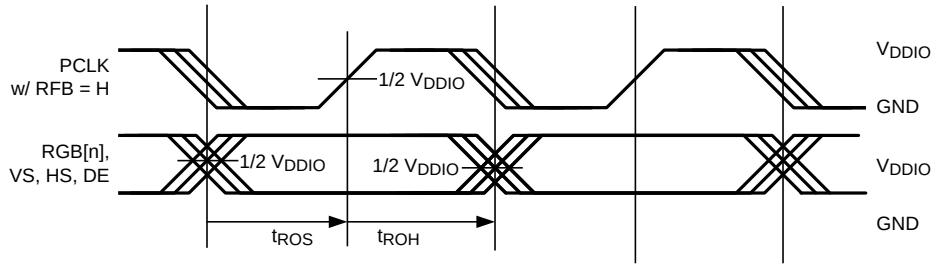

Figure 10. Deserializer Output Data Valid (Setup and Hold) Times with SSCG = On

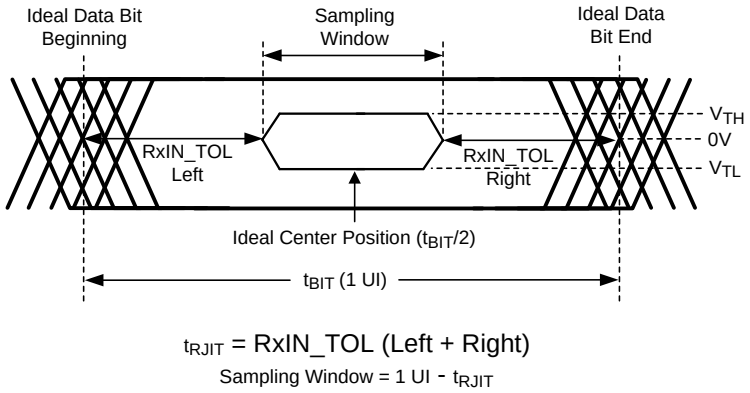

Figure 11. Receiver Input Jitter Tolerance

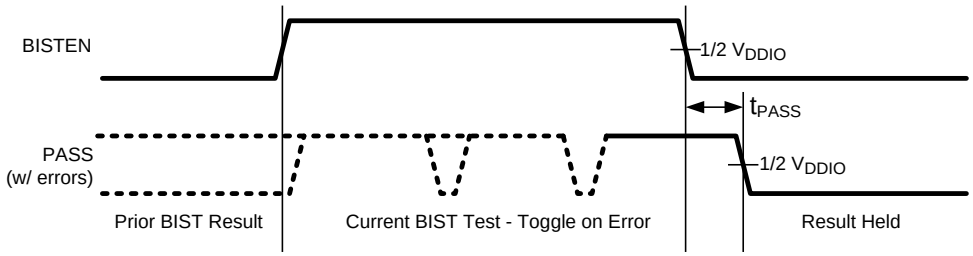

Figure 12. BIST PASS Waveform

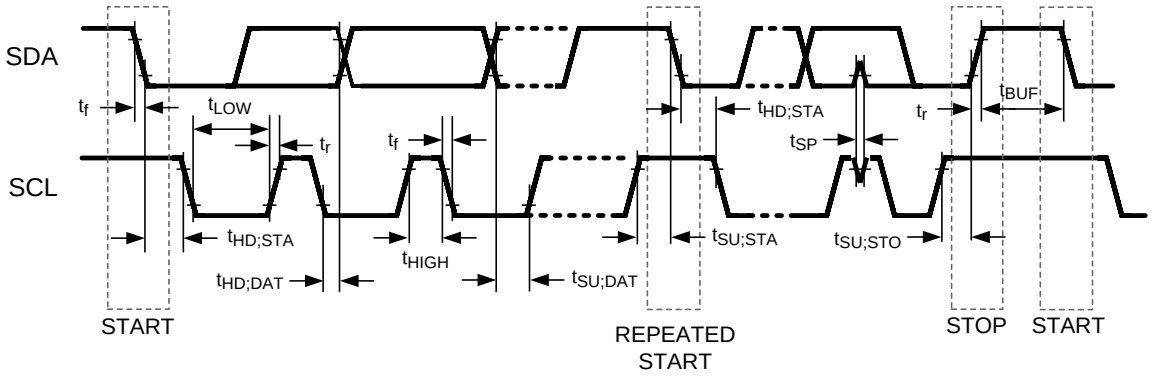

Figure 13. Serial Control Bus Timing Diagram

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FUNCTIONAL DESCRIPTION

The DS90UR905 / DS90UR916Q chipset transmits and receives 27-bits of data (24-high speed color bits and 3 low speed video control signals) over a single serial FPD-Link II pair operating at 140Mbps to 1.82Gbps. The serial stream also contains an embedded clock, video control signals and the DC-balance information which enhances signal quality and supports AC coupling. The pair is intended for use with each other but is backward compatible with previous generations of FPD-Link II as well.

The Des can attain lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The Des also synchronizes to the Ser regardless of the data pattern, delivering true automatic “plug and lock” performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The Des recovers the clock and data by extracting the embedded clock information, validating and then deserializing the incoming data stream providing a parallel LVCMOS video bus to the display. White balance LUTs and dithering features are provided to enable display image enhancement.

The DS90UR905 / DS90UR916Q chipset can operate in 24-bit color depth (with VS,HS,DE encoded in the DCA bit) or in 18-bit color depth (with VS, HS, DE encoded in DCA or mapped into the high-speed data bits). In 18–bit color applications, the three video signals maybe sent encoded via the DCA bit (restrictions apply) or sent as “data bits” along with three additional general purpose signals.

Data Transfer

The DS90UR905 / DS90UR916Q chipset will transmit and receive a pixel of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always HIGH and C0 is always LOW. b[23:0] contain the scrambled RGB data. DCB is the DC-Balanced control bit. DCB is used to minimize the short and long-term DC bias on the signal lines. This bit determines if the data is unmodified or inverted. DCA is used to validate data integrity in the embedded data stream and can also contain encoded control (VS,HS,DE). Both DCA and DCB coding schemes are generated by the Ser and decoded by the Des automatically. Figure 14 illustrates the serial stream per PCLK cycle.

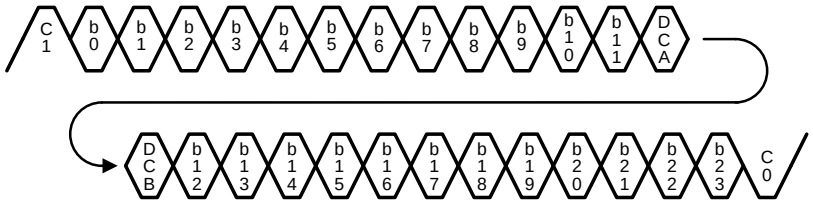

Figure 14. FPD-Link II Serial Stream (905/916)

Des OPERATING MODES AND BACKWARD COMPATIBILITY (CONFIG[1:0])

The DS90UR916Q is also backward compatible with previous generations of FPD-Link II. Configuration modes are provided for backwards compatibility with the DS90C124 FPD-Link II Generation 1, and also the DS90UR124 FPD-Link II Generation 2 chipset by setting the respective mode with the CONFIG[1:0] pins or control register as shown in Table 1. The selection also determines whether the Video Control Signal filter feature is enabled or disabled in Normal mode.

When the DS90UR916 deserializer is configured to operate in backward compatible modes the image enhancement features (white balance and FRC dithering) are **not** available.

Table 1. DS90UR916Q Des Modes

CONFIG1	CONFIG0	Mode	Des Device
L	L	Normal Mode, Control Signal Filter disabled	DS90UR905
L	H	Normal Mode, Control Signal Filter enabled	DS90UR905
H	L	Backwards Compatible GEN2	DS90UR241
H	H	Backwards Compatible GEN1	DS90C241

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Video Control Signal Filter

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled:
  - DE and HS — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled:
  - DE and HS — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS — Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals. See Figure 15.

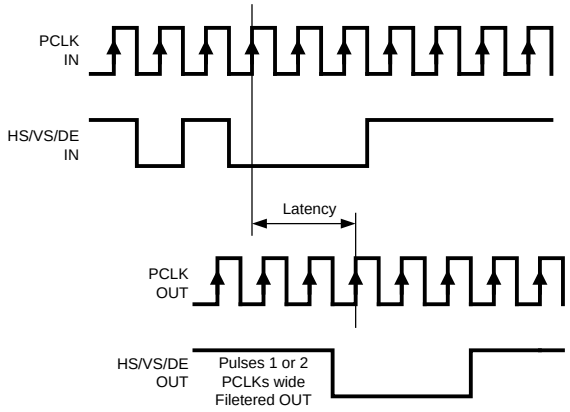

Figure 15. Video Control Signal Filter Waveform

DESERIALIZER Functional Description

The Des converts a single input serial data stream to a wide parallel output bus, and also provides a signal check for the chipset Built In Self Test (BIST) mode. Several image enhancement features are provided (Note that these features are not available when operating in backward compatible modes). White balance LUTs allow the user to define and target the color temperature of the display. Adaptive Hi-FRC dithering enables the presentation of “true-color” images on an 18–bit color display. The device can be configured via external pins and strap pins or through the optional serial control bus. The Des features enhance signal quality on the link by supporting: an equalizer input and also the FPD-Link II data coding that provides randomization, scrambling, and DC balancing of the data. The Des includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data and also the output spread spectrum clock generation (SSCG) support. The Des features power saving features with a power down mode, and optional LVCMOS (1.8 V) interface compatibility.

Image Enhancement Features

White Balance

The White Balance feature enables similar display appearance when using LCD’s from different vendors. It compensates for native color temperature of the display, and adjusts relative intensities of R, G, B to maintain specified color temperature. Programmable control registers are used to define the contents of three LUTs (8-bit color value for Red, Green and Blue) for the White Balance Feature. The LUTs map input RGB values to new output RGB values. There are three LUTs, one LUT for each color. Each LUT contains 256 entries, 8-bits per entry with a total size of 6144 bits (3 x 256 x 8). All entries are readable and writable. Calibrated values are loaded into registers through the I2C interface (deserializer is a slave device). This feature may also be applied to lower color depth applications such as 18–bit (666) and 16–bit (565). White balance is enabled and configured via serial bus register control.

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LUT contents. The user must define and load the contents of the LUT for each color (R,G,B). Regardless of the color depth being driven (888, 666, 656), the user must always provide contents for 3 complete LUTs - 256 colors x 8 bits x 3 tables. Unused bits - LSBs -shall be set to “0” by the user.

When 24-bit (888) input data is being driven to a 24-bit display, each LUT (R, G and B) must contain 256 unique 8-bit entries. The 8-bit white balanced data is then available at the output of the DS90UR916 deserailizer, and driven to the display.

When 18-bit (666) input data is being driven to an 18-bit display, the white balance feature may be used in one of two ways. First, simply load each LUT with 256, 8-bit entries. Each 8-bit entry is a 6-bit value (6 MSBs) with the 2 LSBs set to “00”. Thus as total of 64 unique 6-bit white balance output values are available for each color (R, G and B). The 6-bit white balanced data is available at the output of the DS90UR916 deserializer, and driven directly to the display.

Alternatively, with 6-bit input data the user may choose to load complete 8-bit values into each LUT. This mode of operation provides the user with finer resolution at the LUT output to more closely achieve the desired white point of the calibrated display. Although 8-bit data is loaded, only 64 unique 8-bit white balance output values are available for each color (R, G and B). The result is 8-bit white balanced data. Before driving to the output of the deserializer, the 8-bit data must be reduced to 6-bit with an FRC dithering function. To operate in this mode, the user must configure the DS90UR916 to enable the FRC2 function.

Examples of the three types of LUT configurations described are shown in Figure 16.

*Enabling white balance.*The user must load all 3 LUTs prior to enabling the white balance feature. The following sequence must be followed by the user.

To initialize white balance after power-on:

1. Load contents of all 3 LUTs . This requires a sequential loading of LUTs - first RED, second GREEN, third BLUE. 256, 8-bit entries must be loaded to each LUT. Page registers must be set to select each LUT.

2. Enable white balance

By default, the LUT data may not be reloaded after initialization at power-on.

An option does exist to allow LUT reloading after power-on and initial LUT loading (as described above). This option may only be used after enabling the white balance reload feature via the associated serial bus control register. In this mode the LUTs may be reloaded by the master controller via I2C. This provides the user with the flexibility to refresh LUTs periodically , or upon system requirements to change to a new set of LUT values. The host controller loads the updated LUT values via the serial bus interface. There is no need to disable the white balance feature while reloading the LUT data. Refreshing the white balance to the new set of LUT data will be seamless - no interruption of displayed data.

It is important to note that initial loading of LUT values requires that all 3 LUTs be loaded sequentially. When reloading, partial LUT updates may be made. Refer to *USING IMAGE ENHANCEMENT FEATURES* for a detailed description of the LUT loading and reloading procedures.

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8-bit in / 8 bit out

Gray level Entry	Data Out (8-bits)
0	00000000b
1	00000001b
2	00000011b
3	00000011b
4	00000110b
5	00000110b
6	00000111b
7	00000111b
8	00001000b
9	00001010b
10	00001001b
11	00001011b
⋮	⋮
248	11111010b
249	11111010b
250	11111011b
251	11111011b
252	11111110b
253	11111101b
254	11111101b
255	11111111b

6-bit in / 6 bit out

Gray level Entry	Data Out (8-bits)
0	000000**00**b
1	N/A
2	N/A
3	N/A
4	000001**00**b
5	N/A
6	N/A
7	N/A
8	000010**00**b
9	N/A
10	N/A
11	N/A
⋮	⋮
248	111110**00**b
249	N/A
250	N/A
251	N/A
252	111111**00**b
253	N/A
254	N/A
255	N/A

6-bit in / 8 bit out

Gray level Entry	Data Out (8-bits)
0	00000001b
1	N/A
2	N/A
3	N/A
4	00000110b
5	N/A
6	N/A
7	N/A
8	00001011b
9	N/A
10	N/A
11	N/A
⋮	⋮
248	11111010b
249	N/A
250	N/A
251	N/A
252	11111111b
253	N/A
254	N/A
255	N/A

Figure 16. White Balance LUT Configurations

Adaptive Hi-FRC Dithering

The Adaptive FRC Dithering Feature delivers product-differentiating image quality. It reduces 24-bit RGB (8 bits per sub-pixel) to 18-bit RGB (6 bits per sub-pixel), smoothing color gradients, and allowing the flexibility to use lower cost 18-bit displays. FRC (Frame Rate Control) dithering is a method to emulate “missing” colors on a lower color depth LCD display by changing the pixel color slightly with every frame. FRC is achieved by controlling on and off pixels over multiple frames (Temporal). Static dithering regulates the number of on and off pixels in a small defined pixel group (Spatial). The FRC module includes both Temporal and Spatial methods and also Hi-FRC. Conventional FRC can display only 16,194,277 colors with 6-bit RGB source. “Hi-FRC” enables full (16,777,216) color on an 18-bit LCD panel. The “adaptive” FRC module also includes input pixel detection to apply specific Spatial dithering methods for smoother gray level transitions. When enabled, the lower LSBs of each RGB output are not active; only 18 bit data (6 bits per R,G and B) are driven to the display. This feature is enabled via serial bus register control.

Two FRC functional blocks are available, and may be independently enabled. FRC1 precedes the white balance LUT, and is intended to be used when 24-bit data is being driven to an 18-bit display with a white balance LUT that is calibrated for an 18-bit data source. The second FRC block, FRC2, follows the white balance block and is intended to be used when fine adjustment of color temperature is required on an 18-bit color display, or when a 24-bit source drives an 18-bit display with a white balance LUT calibrated for 24-bit source data.

For proper operation of the FRC dithering feature, the user must provide a description of the display timing control signals. The timing mode, “sync mode” (HS, VS) or “DE only” must be specified, along with the active polarity of the timing control signals. All this information is entered to DS90UR916 control registers via the serial bus interface.

Adaptive Hi-FRC dithering consists of several components. Initially, the incoming 8-bit data is expanded to 9-bit data. This allows the effective dithered result to support a total of 16.7 million colors. The incoming 9-bit data is evaluated, and one of four possible algorithms is selected. The majority of incoming data sequences are supported by the default dithering algorithm. Certain incoming data patterns (black/white pixel, full on/off sub-pixel) require special algorithms designed to eliminate visual artifacts associated with these specific gray level transitions. Three algorithms are defined to support these critical transitions.

An example of the default dithering algorithm is illustrated in Figure 17. The “1” or “0” value shown in the table describes whether the 6-bit value is increased by 1 (“1”) or left unchanged (“0”). In this case, the 3 truncated LSBs are “001”.

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F0L0	Frame = 0, Line = 0
PD1	Pixel Data one
Cell Value 010	R[7:2]+0, G[7:2]+1, B[7:2]+0
LSB=001	three lsb of 9 bit data (8 to 9 for Hi-Frc)

Pixel Index	**PD1**	**PD2**	**PD3**	**PD4**	**PD5**	**PD6**	**PD7**	**PD8**	
LSB = 001									
F0L0	010	000	000	000	000	000	010	000	
F0L1	101	000	000	000	101	000	000	000	R = 4/32
F0L2	000	000	010	000	010	000	000	000	G = 4/32
F0L3	000	000	101	000	000	000	101	000	B = 4/32
F1L0	000	000	000	000	000	000	000	000	
F1L1	000	111	000	000	000	111	000	000	R = 4/32
F1L2	000	000	000	000	000	000	000	000	G = 4/32
F1L3	000	000	000	111	000	000	000	111	B = 4/32
F2L0	000	000	010	000	010	000	000	000	
F2L1	000	000	101	000	000	000	101	000	R = 4/32
F2L2	010	000	000	000	000	000	010	000	G = 4/32
F2L3	101	000	000	000	101	000	000	000	B = 4/32
F3L0	000	000	000	000	000	000	000	000	
F3L1	000	000	000	111	000	000	000	111	R = 4/32
F3L2	000	000	000	000	000	000	000	000	G = 4/32
F3L3	000	111	000	000	000	111	000	000	B = 4/32

Figure 17. Default FRC Algorithm

Signal Quality Enhancers

Des — Input Equalizer Gain (EQ)

The Des can enable receiver input equalization of the serial stream to increase the eye opening to the Des input. Note this function cannot be seen at the RxIN+/- input but can be observed at the serial test port (CMLOUTP/N) enabled via the Serial Bus control registers. The equalization feature may be controlled by the external pin or by register.

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Table 2. Receiver Equalization Configuration Table

INPUTS				Effect
EQ3	EQ2	EQ1	EQ0	
L	L	L	H	~1.5 dB
L	L	H	H	~3 dB
L	H	L	H	~4.5 dB
L	H	H	H	~6 dB
H	L	L	H	~7.5 dB
H	L	H	H	~9 dB
H	H	L	H	~10.5 dB
H	H	H	H	~12 dB
X	X	X	L	OFF*
* Default Setting is EQ = Off				

The quality of the equalized signal may be assessed by monitoring the differential eye opening at the CMLOUTP/N. The Receiver Differential Input Threshold and Input Jitter Tolerance define the acceptable data eye opening. A differential probe should be used to measure across a 100Ohm termination resistor between the CMLOUTP/N pins. Figure 18 illustrates the eye opening.

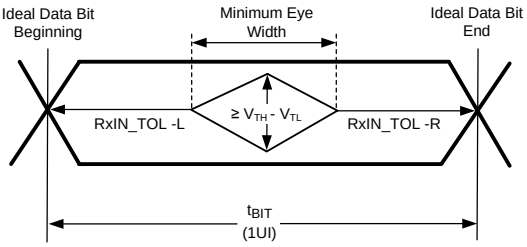

Figure 18. CMLOUT Eye Opening

EMI Reduction Features

Output Slew (OS_PCLK/DATA)

The parallel bus outputs (RGB[7:0], VS, HS, DE and PCLK) of the Des feature a selectable output slew. The DATA ((RGB[7:0], VS, HS, DE) are controlled by strap pin or register bit OS_DATA. The PCLK is controlled by strap pin or register bit OS_PCLK. When the OS_PCLK/DATA = HIGH, the maximum slew rate is selected. When the OS_PCLK/DATA = LOW, the minimum slew rate is selected. Use the higher slew rate setting when driving longer traces or a heavier capacitive load.

Common Mode Filter Pin (CMF) — Optional

The Des provides access to the center tap of the internal termination. A capacitor may be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 0.1µF capacitor may be connected to this pin to Ground.

SSCG Generation — Optional

The Des provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This will aid to lower system EMI. Output SSCG deviations to ±2.0% (4% total) at up to 35kHz modulations nominally are available. See Table 3. This feature may be controlled by external STRAP pins or by register.

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Table 3. SSCG Configuration (LF_MODE = L) — Des Output

SSC[3:0] Inputs LF_MODE = L (20 - 65 MHz)				Result	
SSC3	SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	L	Off	Off
L	L	L	H	±0.5	PCLK/2168
L	L	H	L	±1.0	
L	L	H	H	±1.5	
L	H	L	L	±2.0	
L	H	L	H	±0.5	PCLK/1300
L	H	H	L	±1.0	
L	H	H	H	±1.5	
H	L	L	L	±2.0	
H	L	L	H	±0.5	PCLK/868
H	L	H	L	±1.0	
H	L	H	H	±1.5	
H	H	L	L	±2.0	
H	H	L	H	±0.5	PCLK/650
H	H	H	L	±1.0	
H	H	H	H	±1.5	

Table 4. SSCG Configuration (LF_MODE = H) — Des Output

SSC[3:0] Inputs LH_MODE = H (5 - 20 MHz)				Result	
SSC3	SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	L	Off	Off
L	L	L	H	±0.5	PCLK/620
L	L	H	L	±1.0	
L	L	H	H	±1.5	
L	H	L	L	±2.0	
L	H	L	H	±0.5	PCLK/370
L	H	H	L	±1.0	
L	H	H	H	±1.5	
H	L	L	L	±2.0	
H	L	L	H	±0.5	PCLK/258
H	L	H	L	±1.0	
H	L	H	H	±1.5	
H	H	L	L	±2.0	
H	H	L	H	±0.5	PCLK/192
H	H	H	L	±1.0	
H	H	H	H	±1.5	

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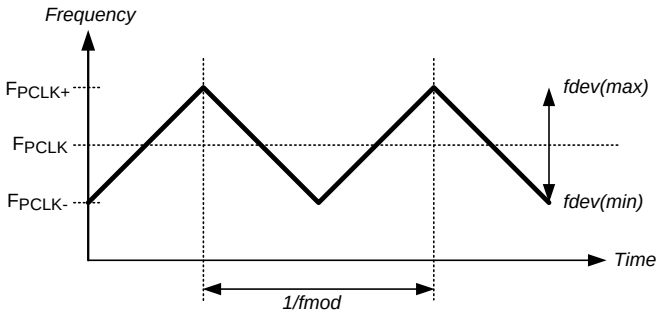

Figure 19. SSCG Waveform

1.8V or 3.3V VDDIO Operation

The Des parallel bus and Serial Bus Interface can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for target (Display) compatibility. The 1.8 V levels will offer a lower noise (EMI) and also a system power savings.

Power Saving Features

PowerDown Feature (PDB)

The Des has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the system to save power, disabling the Des when the display is not needed. An auto detect mode is also available. In this mode, the PDB pin is tied High and the Des will enter POWER DOWN when the serial stream stops. When the serial stream starts up again, the Des will lock to the input stream and assert the LOCK pin and output valid data. In POWER DOWN mode, the Data and PCLK output states are determined by the OSS_SEL status. Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

Stop Stream SLEEP Feature

The Des will enter a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the Des will then lock to the incoming signal and recover the data. Note – in STOP STREAM SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

CLOCK-DATA RECOVERY STATUS FLAG (LOCK) and OUTPUT STATE SELECT (OSS_SEL)

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK goes from TRI-STATE to LOW (depending on the value of the OSS_SEL setting). After the DS90UR916Q completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the parallel bus and PCLK outputs. The PCLK output is held at its current state at the change from OSC_CLK (if this is enabled via OSC_SEL) to the recovered clock (or vice versa).

If there is a loss of clock from the input serial stream, LOCK is driven Low and the state of the RGB/VS/HS/DE outputs are based on the OSS_SEL setting (STRAP PIN configuration or register).

Oscillator Output — Optional

The Des provides an optional PCLK output when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature may be controlled by the external pin or by register. See Table 6 and Table 7.

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Table 5. OSS_SEL and PDB Configuration — Des Outputs(1)

INPUTS			OUTPUTS			
Serial Input	**PDB**	**OSS_SEL**	**PCLK**	**RGB/HS/VS/DE**	**LOCK**	**PASS**
X	L	X	Z	Z	Z	Z
Static	H	L	L	L	L	L
Static	H	H	Z	Z*	L	L
Active	H	X	Active	Active	H	H

(1) If pin is strapped HIGH, output will be pulled up

Table 6. OSC (Oscillator) Mode — Des Output

INPUTS	OUTPUTS			
Embedded PCLK	**PCLK**	**RGB/HS/VS/DE**	**LOCK**	**PASS**
See(1)	OSC Output	L	L	L
Present	Toggling	Active	H	H

(1) Absent and OSC_SEL ≠ 000

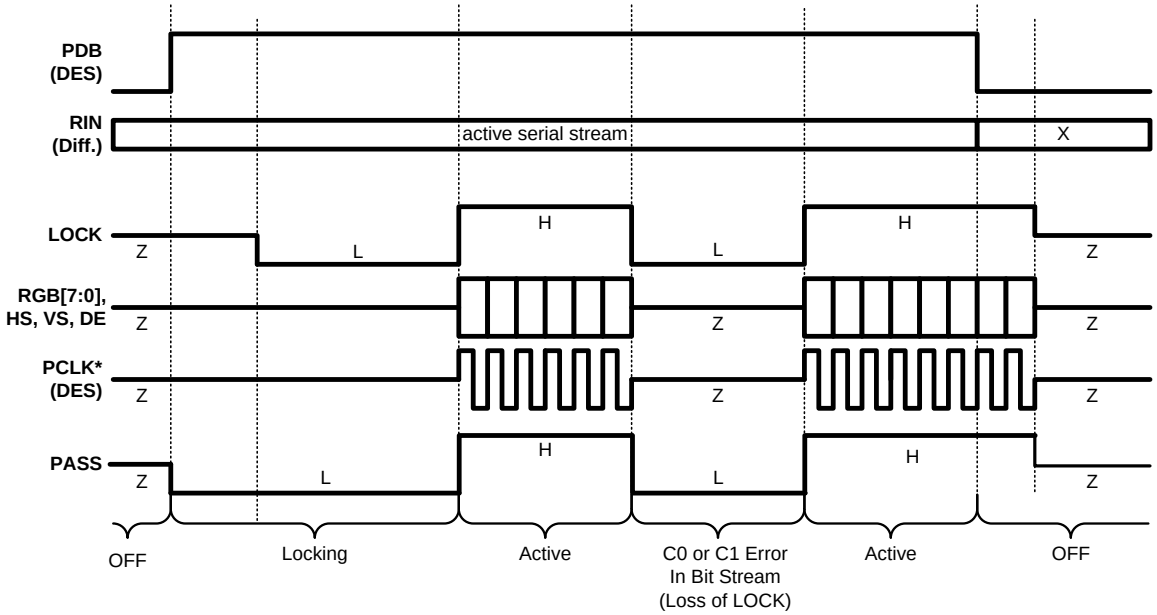

Figure 20. Des Outputs with Output State Select Low (OSS_SEL = H)

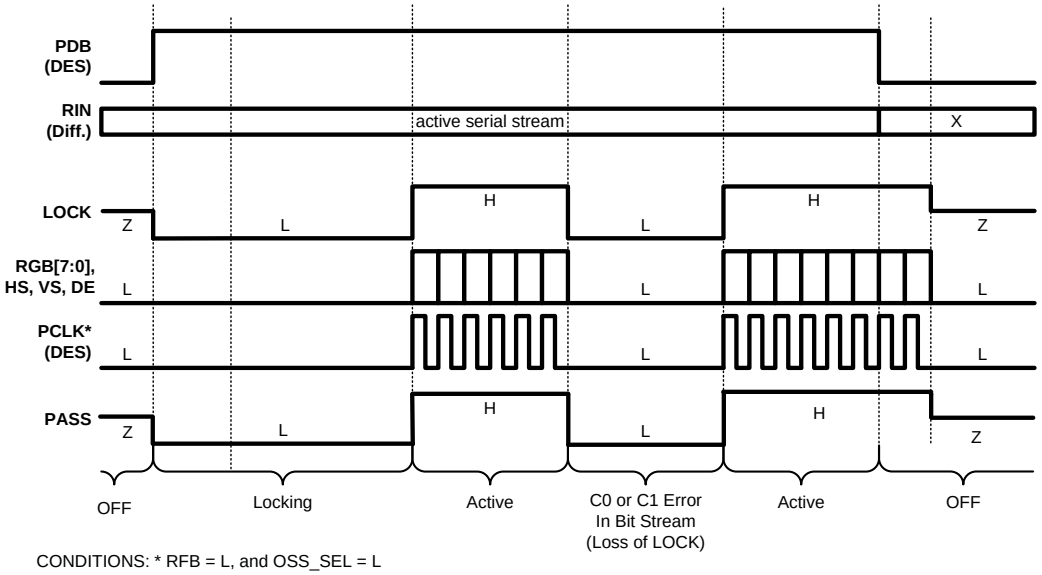

Figure 21. Des Outputs with Output State Select High (OSS_SEL = L)

Table 7. OSC_SEL (Oscillator) Configuration

OSC_SEL[2:0] INPUTS			PCLK Oscillator Output
OSC_SEL2	OSC_SEL1	OSC_SEL0	
L	L	L	Off – Feature Disabled – Default
L	L	H	50 MHz ±40%
L	H	L	25 MHz ±40%
L	H	H	16.7 MHz ±40%
H	L	L	12.5 MHz ±40%
H	L	H	10 MHz ±40%
H	H	L	8.3 MHz ±40%
H	H	H	6.3 MHz ±40%

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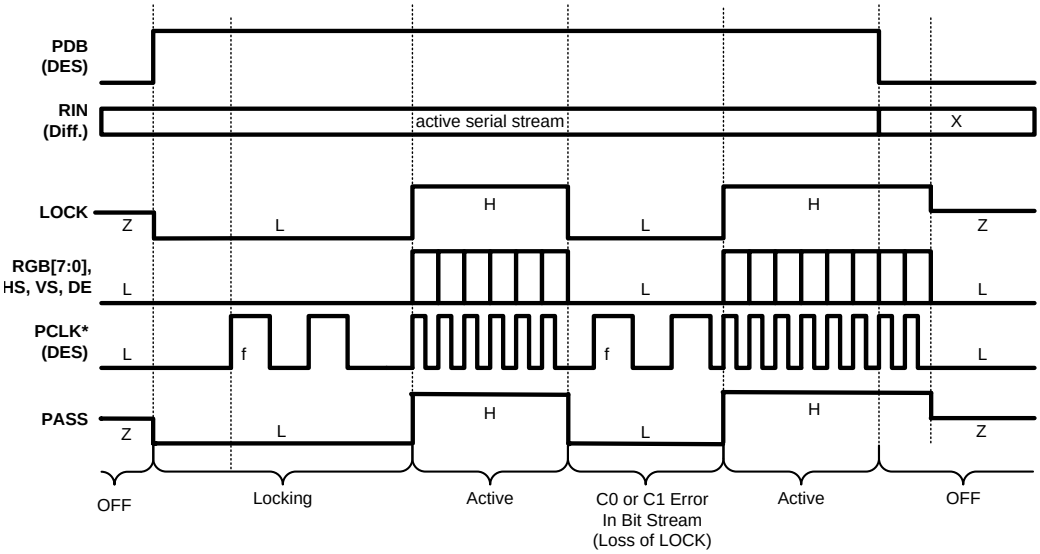

CONDITIONS: * RFB = L, OSS_SEL = L , and OSC_SEL not equal to 000.

Figure 22. Des Outputs with Output State High and PCLK Output Oscillator Option Enabled

OP_LOW — Optional

The OP_ LOW feature is used to hold the LVCMOS outputs (except the LOCK output) at a LOW state. This feature is enabled by setting the OP_LOW strap pin = HIGH, followed by the rising edge of PDB. The user must toggle the OP_LOW Set/Reset register bit to release the outputs to the normal toggling state. Note that the release of the outputs can only occur when LOCK is HIGH. When the OP_LOW feature is enabled, anytime LOCK = LOW, the LVCMOS outputs will toggle to a LOW state again. The OP_ LOW strap pin feature is assigned to output PASS pin 42.

Restrictions on other straps:

1) Other straps should not be used in order to keep RGB[7:0], HS, VS, DE, and PCLK at a true LOW state. Other features should be selected thru I2C.

2) OSS_SEL function is not available when O/P_LOW is tied H.

Outputs RGB[7:0], HSYNC, VSYNC, DE, and PCLK are in TRI-STATE before PDB toggles HIGH because the OP_LOW strap value has not been recognized until the DS90UR916 powers up. Figure 23 shows the user controlled release of OP_LOW and automatic reset of OP_LOW set on the falling edge of LOCK. Figure 24 shows the user controlled release of OP_LOW and manual reset of OP_LOW set. Note manual reset of OP_LOW can only occur when LOCK is H.

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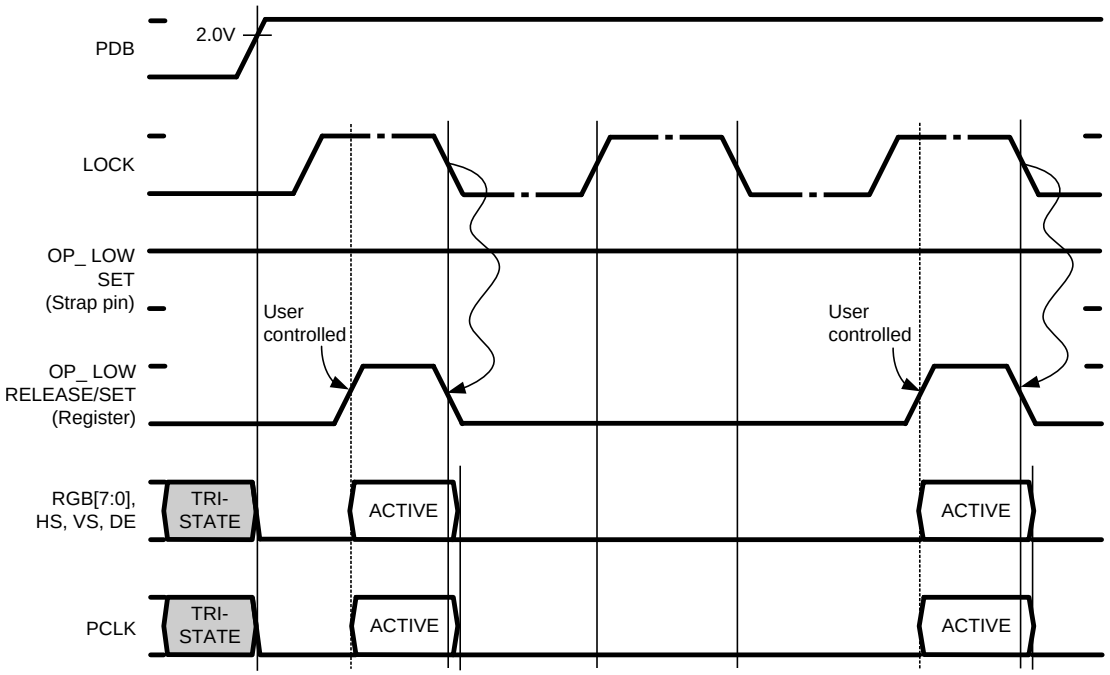

Figure 23. OP_LOW Auto Set

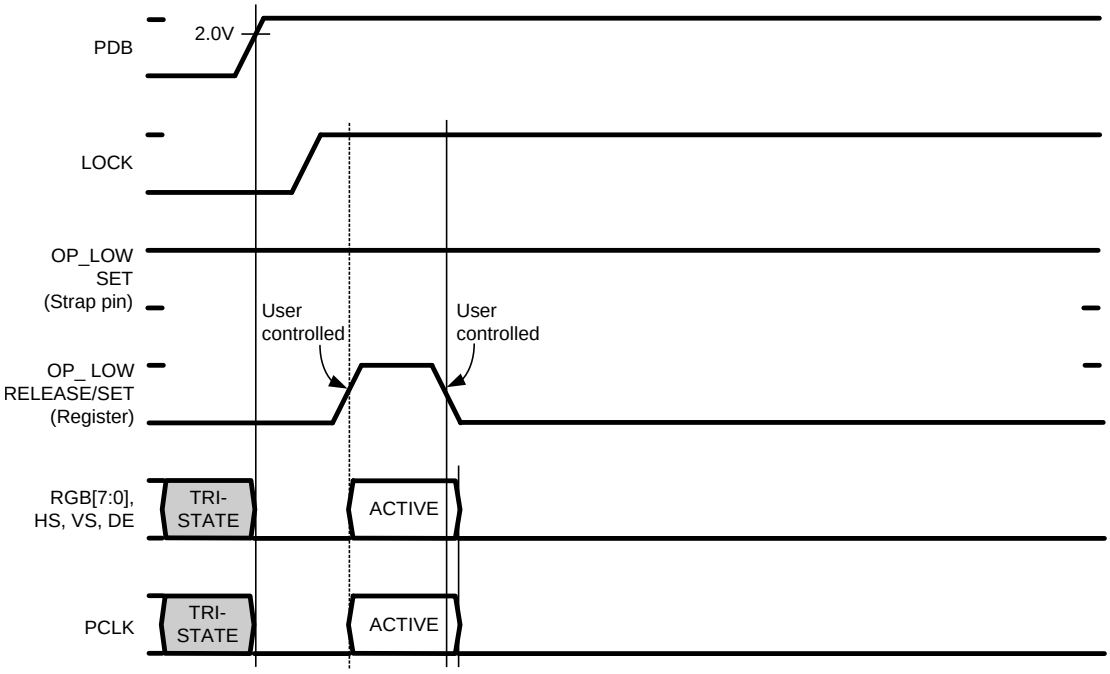

Figure 24. OP_LOW Manual Set/Reset

Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the data is strobed on. If RFB is High, output data is strobed on the Rising edge of the PCLK. If RFB is Low, data is strobed on the Falling edge of the PCLK. This allows for inter-operability with downstream devices. The Des output does not need to use the same edge as the Ser input. This feature may be controlled by the external pin or by register.

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Control Signal Filter — Optional

The Des provides an optional Control Signal (VS, HS, DE) filter that monitors the three video control signals and eliminates any pulses that are 1 or 2 PCLKs wide. Control signals must be 3 pixel clocks wide (in its HIGH or LOW state, regardless of which state is active). This is set by the CONFIG[1:0] or by the Control Register. This feature may be controlled by the external pin or by Register.

Low Frequency Optimization (LF_Mode)

This feature may be controlled by the external pin or by Register.

Des — Map Select

This feature may be controlled by the external pin or by Register.

Table 8. Map Select Configuration

INPUTS		Effect
MAPSEL1	**MAPSEL0**	
L	L	Bit 4, Bit 5 on LSB **DEFAULT**
L	H	LSB 0 or 1
H	H or L	LSB 0

Strap Input Pins

Configuration of the device maybe done via configuration input pins and the STRAP input pins, or via the Serial Control Bus. The STRAP input pins share select parallel bus output pins. They are used to load in configuration values during the initial power up sequence of the device. Only a pull-up on the pin is required when a HIGH is desired. By default the pad has an internal pull down, and will bias Low by itself. The recommended value of the pull up is 10 kΩ to V_{DDIO}; open (NC) for Low, no pull-down is required (internal pull-down). If using the Serial Control Bus, no pull ups are required.

Optional Serial Bus Control

Please see the following section on the optional Serial Bus Control Interface.

Optional BIST Mode

Please see the following section on the chipset BIST mode for details.

Built In Self Test (BIST)

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. In the BIST mode only a input clock is required along with control to the Ser and Des BISTEN input pins. The Ser outputs a test pattern (PRBS7) and drives the link at speed. The Des detects the PRBS7 pattern and monitors it for errors. A PASS output pin toggles to flag any payloads that are received with 1 to 24 errors. Upon completion of the test, the result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the Des BISTEN pin. During the BIST duration the deserializer data outputs toggle with a checkerboard pattern.

Inter-operability is supported between this FPD-Link II device and all FPD-Link II generations (Gen 1/2/3) — see respective datasheets for details on entering BIST mode and control.

Sample BIST Sequence

See Figure 25 for the BIST mode flow diagram.

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Step 1: Place the DS90UR905 Ser in BIST Mode by setting Ser BISTEN = H. For the DS90UR905 Ser or DS99R421 FPD-Link II Ser BIST Mode is enabled via the BISTEN pin. For the DS90C241 Ser or DS90UR241 Ser, BIST mode is enetered by setting all the input data of the device to Low state. A PCLK is required for all the Ser options. When the Des detects the BIST mode pattern and command (DCA and DCB code) the RGB and control signal outputs are shut off.

Step 2: Place the DS90UR916Q Des in BIST mode by setting the BISTEN = H. The Des is now in the BIST mode and checks the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the Des BISTEN pin is set Low. The Des stops checking the data and the final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: To return the link to normal operation, the Ser BISTEN input is set Low. The Link returns to normal operation.

Figure 26 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (De-Emphasis, VODSEL, or Rx Equalization).

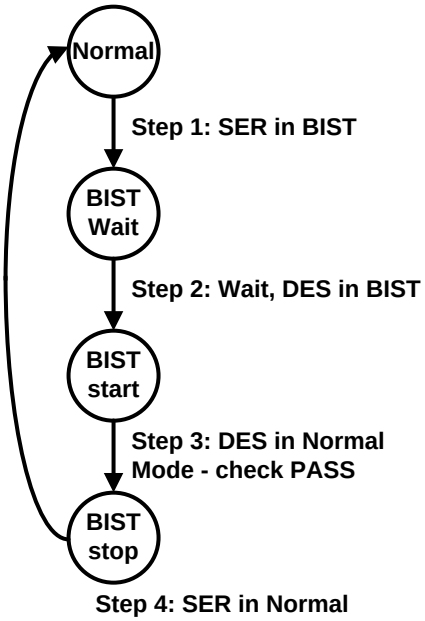

Figure 25. BIST Mode Flow Diagram

BER Calculations

It is possible to calculate the approximate Bit Error Rate (BER). The following is required:

- Pixel Clock Frequency (MHz)
- BIST Duration (seconds)
- BIST test Result (PASS)

The BER is less than or equal to one over the product of 24 times the PCLK rate times the test duration. If we assume a 65MHz PCLK, a 10 minute (600 second) test, and a PASS, the BERT is ≤ 1.07 X 10E-12

The BIST mode runs a check on the data payload bits. The LOCK pin also provides a link status. It the recovery of the C0 and C1 bits does not reconstruct the expected clock signal, the LOCK pin will switch Low. The combination of the LOCK and At-Speed BIST PASS pin provides a powerful tool for system evaluation and performance monitoring.

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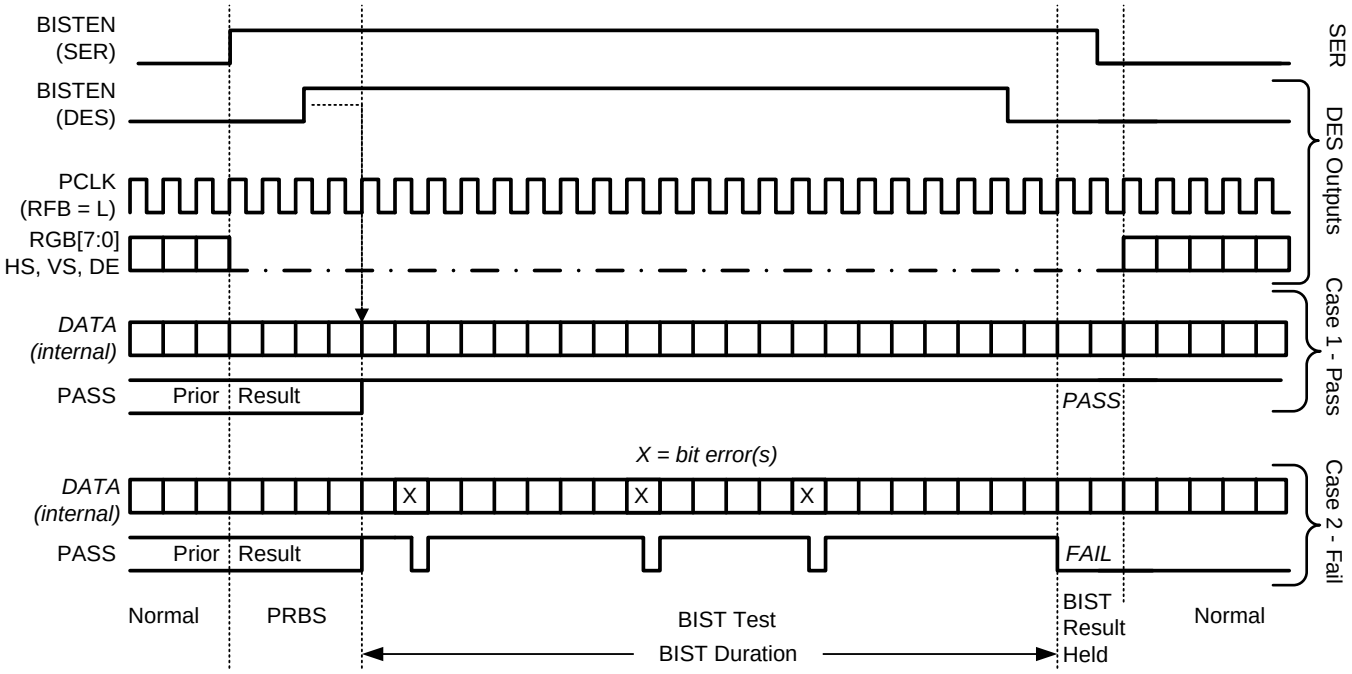

Figure 26. BIST Waveforms

Optional Serial Bus Control

The DS90UR916 may also be configured by the use of a serial control bus that is I2C protocol compatible. By default, the I2C reg_0x00'h is set to 00'h and all configuration is set by control/strap pins. A write of 01'h to reg_0x00'h will enable/allow configuration by registers; this will override the control/strap pins. Multiple devices may share the serial control bus since multiple addresses are supported. See Figure 27.

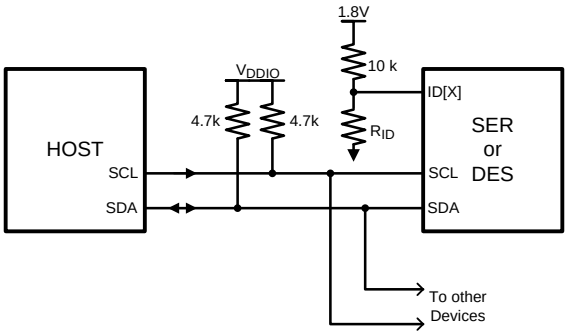

Figure 27. Serial Control Bus Connection

The serial bus is comprised of three pins. The SCL is a Serial Bus Clock Input. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull up resistor to V_{DDIO}. For most applications a 4.7 k pull up resistor to V_{DDIO} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

The third pin is the ID[X] pin. This pin sets one of four possible device addresses. Two different connections are possible. The pin may be pulled to V_{DD} (**1.8V, NOT V_{DDIO}**)) with a 10 kΩ resistor; or a 10 kΩ pull up resistor (to V_{DD}**1.8V, NOT V_{DDIO}**)) and a pull down resistor of the recommended value to set other three possible addresses may be used. See Table 9. Do not tie ID[x] directly to VSS.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH. See Figure 28.

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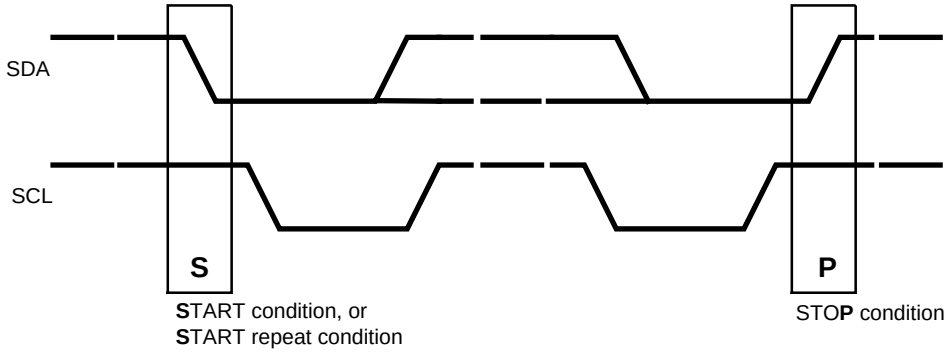

Figure 28. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 29 and a WRITE is shown in Figure 30.

If the Serial Bus is not required, the three pins may be left open (NC).

Table 9. ID[x] Resistor Value – DS90UR916Q Des

Resistor RID* kΩ (5% tol)	Address 7'b	Address 8'b 0 appended (WRITE)
0.47	7b' 111 0001 (h'71)	8b' 1110 0010 (h'E2)
2.7	7b' 111 0010 (h'72)	8b' 1110 0100 (h'E4)
8.2	7b' 111 0011 (h'73)	8b' 1110 0110 (h'E6)
Open	7b' 111 0110 (h'76)	8b' 1110 1100 (h'EC)

*Note: RID ≠ 0 ohm, do not connect directly to VSS (GND), this is not a valid address.

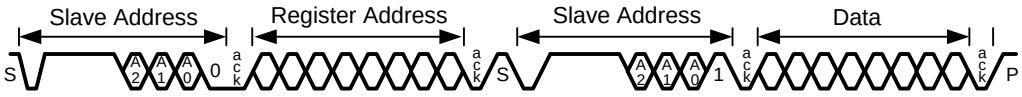

Figure 29. Serial Control Bus — READ

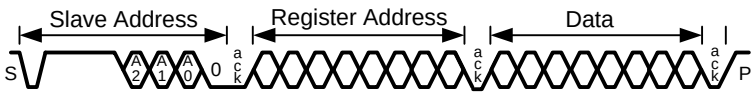

Figure 30. Serial Control Bus — WRITE

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Table 10. DESERIALIZER — Serial Bus Control Registers

PAGE	ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	0	0	Des Config 1	7	R/W	0	LFMODE	0: 20 to 65 MHz Operation 1: 5 to 20 MHz Operation
				6	R/W	0	OS_PCLK	0: Normal PCLK Output Slew 1: Increased PCLK Slew
				5	R/W	0	OS_DATA	0: Normal DATA OUTPUT Slew 1: Increased Data Slew
				4	R/W	0	RFB	0: Data strobed on Falling edge of PCLK 1: Data strobed on Rising edge of PCLK
				3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: Backwards Compatible (DS90UR241) 11: Backwards Compatible (DS90C241)
				1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: normal mode 1: Sleep Mode – **Register settings retained.**
				0	R/W	0	REG Control	0: Configurations set from control pins / STRAP pins 1: Configurations set from registers (except I2C_ID)
0	1	1	Slave ID	7	R/W	0		0: Address from ID[X] Pin 1: Address from Register
				6:0	R/W	1110000	ID[X]	Serial Bus Device ID, Four IDs are: 7b '1110 001 (h'71) 7b '1110 010 (h'72) 7b '1110 011 (h'73) 7b '1110 110 (h'76) All other addresses are ***Reserved***.
0	2	2	Des Features 1	7	R/W	0	OP_LOW Release/Set	0: set outputs state LOW (except LOCK) 1: release output LOW state, outputs toggling normally Note: This register only works during LOCK = 1.
				6	R/W	0	OSS_SEL	Output Sleep State Select 0:PCLK/RGB[7:0]/HS/VS/DE = L, LOCK = Normal, PASS = H 1:PCLK/RGB[7:0]/HS/VS/DE = Tri-State, LOCK = Normal, PASS = H
				5:4	R/W	00	MAP_SEL	Special for Backwards Compatible Mode with DS90UR241) 00: bit 4, 5 on LSB 01: LSB zero or one 10: LSB zero 11: LSB zero
				3	R/W	0	OP_LOW strap bypass	0: strap will determine whether OP_LOW feature is ON or OFF 1: Turns OFF OP_LOW feature
				2:0	R/W	00	OSC_SEL	000: OFF 001: 50 MHz ±40% 010: 25 MHz ±40% 011: 16.7 MHz ±40% 100: 12.5 MHz ±40% 101: 10 MHz ±40% 110: 8.3 MHz ±40% 111: 6.3 MHz ±40%

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Table 10. DESERIALIZER — Serial Bus Control Registers (continued)

PAGE	ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	3	3	Des Features 2	7:5	R/W	000	EQ Gain	000: ~1.625 dB 001: ~3.25 dB 010: ~4.87 dB 011: ~6.5 dB 100: ~8.125 dB 101: ~9.75 dB 110: ~11.375 dB 111: ~13 dB
				4	R/W	0	EQ Enable	0: EQ = disabled 1: EQ = enabled
				3:0	R/W	0000	SSC	**IF LF_MODE = 0, then**: 000: SSCG OFF 0001: fdev = ±0.5%, fmod = PCLK/2168 0010: fdev = ±1.0%, fmod = PCLK/2168 0011: fdev = ±1.5%, fmod = PCLK/2168 0100: fdev = ±2.0%, fmod = PCLK/2168 0101: fdev = ±0.5%, fmod = PCLK/1300 0110: fdev = ±1.0%, fmod = PCLK/1300 0111: fdev = ±1.5%, fmod = PCLK/1300 1000: fdev = ±2.0%, fmod = PCLK/1300 1001: fdev = ±0.5%, fmod = PCLK/868 1010: fdev = ±1.0%, fmod = PCLK/868 1011: fdev = ±1.5%, fmod = PCLK/868 1100: fdev = ±2.0%, fmod = PCLK/868 1101: fdev = ±0.5%, fmod = PCLK/650 1110: fdev = ±1.0%, fmod = PCLK/650 1111: fdev = ±1.5%, fmod = PCLK/650 **IF LF_MODE = 1, then**: 000: SSCG OFF 0001: fdev = ±0.5%, fmod = PCLK/620 0010: fdev = ±1.0%, fmod = PCLK/620 0011: fdev = ±1.5%, fmod = PCLK/620 0100: fdev = ±2.0%, fmod = PCLK/620 0101: fdev = ±0.5%, fmod = PCLK/370 0110: fdev = ±1.0%, fmod = PCLK/370 0111: fdev = ±1.5%, fmod = PCLK/370 1000: fdev = ±2.0%, fmod = PCLK/370 1001: fdev = ±0.5%, fmod = PCLK/258 1010: fdev = ±1.0%, fmod = PCLK/258 1011: fdev = ±1.5%, fmod = PCLK/258 1100: fdev = ±2.0%, fmod = PCLK/258 1101: fdev = ±0.5%, fmod = PCLK/192 1110: fdev = ±1.0%, fmod = PCLK/192 1111: fdev = ±1.5%, fmod = PCLK/192
0	4	4	CMLOUT Config	7	R/W	0	Repeater Enable	0: Output CMLOUTP/N = disabled 1: Output CMLOUTP/N = enabled
				6:0	R/W	0000000	***Reserved***	***Reserved***
0	21	15	FRC Configuration	7	R/W	0	Timing mode select	Select display timing mode 0: DE only mode 1: Sync mode (VS, HS)
				6	R/W	0	VS Polarity	0: Active HIGH 1: Active LOW
				5	R/W	0	HS Polarity	0: Active HIGH 1: Active LOW
				4	R/W	0	DE Polarity	0: Active HIGH 1: Active LOW
				3	R/W	0	FRC2 enable	0: FRC2 disabled 1: FRC2 enabled
				2	R/W	0	FRC1 enable	0: FRC1 disabled 1: FRC1 enabled
				[1:0]		0	***Reserved***	***Reserved***

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Table 10. DESERIALIZER — Serial Bus Control Registers (continued)

PAGE	ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	22	16	White Balance Configuration	[7:6]	R/W	0	Page Setting	00: Configuration Registers 01: Red LUT 10: Green LUT 11: Blue LUT
				5	R/W	0	White Balance Enable	0: WB disabled 1: WB enabled
				4	R/W	0	Reload Enable	0: Reload disabled 1: Reload enabled
				[3:0]		0	***Reserved***	***Reserved***
1	0 - 255	00 - FF	White Balance Red LUT	[FF:0]	R/W	N/A	Red LUT	256 8–bit entries to be applied to the Red subpixel data
2	0 - 255	00 - FF	White Balance Green LUT	[FF:0]	R/W	N/A	Green LUT	256 8–bit entries to be applied to the Green subpixel data
3	0 - 255	00 - FF	White Balance Blue LUT	[FF:0]	R/W	N/A	Blue LUT	256 8–bit entries to be applied to the Blue subpixel data

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APPLICATIONS INFORMATION

DISPLAY APPLICATION

The DS90UR905/916Q chipset is intended for interface between a host (graphics processor) and a Display. It supports an 24-bit color depth (RGB888) and up to 1024 X 768 display formats. In a RGB888 application, 24 color bits (R[7:0], G[7:0], B[7:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link with PCLK rates from 5 to 65 MHz. The chipset may also be used in 18-bit color applications. In this application three to six general purpose signals may also be sent from host to display.

The Des is expected to be located close to its target device. The interconnect between the Des and the target device is typically in the 1 to 3 inch separation range. The input capacitance of the target device is expected to be in the 5 to 10 pF range. Care should be taken on the PCLK output trace as this signal is edge sensitive and strobes the data. It is also assumed that the fanout of the Des is one. If additional loads need to be driven, a logic buffer or mux device is recommended.

TYPICAL APPLICATION CONNECTION

Figure 31 shows a typical application of the DS90UR916Q Des using serial bus control mode for a 65 MHz 24-bit Color Display Application. The LVDS inputs utilize 100 nF coupling capacitors to the line and the Receiver provides internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, seven 0.1 µF capacitors and two 4.7 µF capacitors should be used for local device bypassing. System GPO (General Purpose Output) signals control the PDB and the BISTEN pins. In this application the RRFB pin is tied Low to strobe the data on the falling edge of the PCLK.

The DS90UR916 will most often be used in serial bus control mode as this is required to enable the image enhancement features of the device. The schematic illustrates the proper connection of SDA and SCL to the pull-up resistors as well as the external resistor network to the ID[x] pin..

The interface to the target display is with 3.3V LVCMOS levels, thus the VDDIO pin is connected to the 3.3 V rail. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

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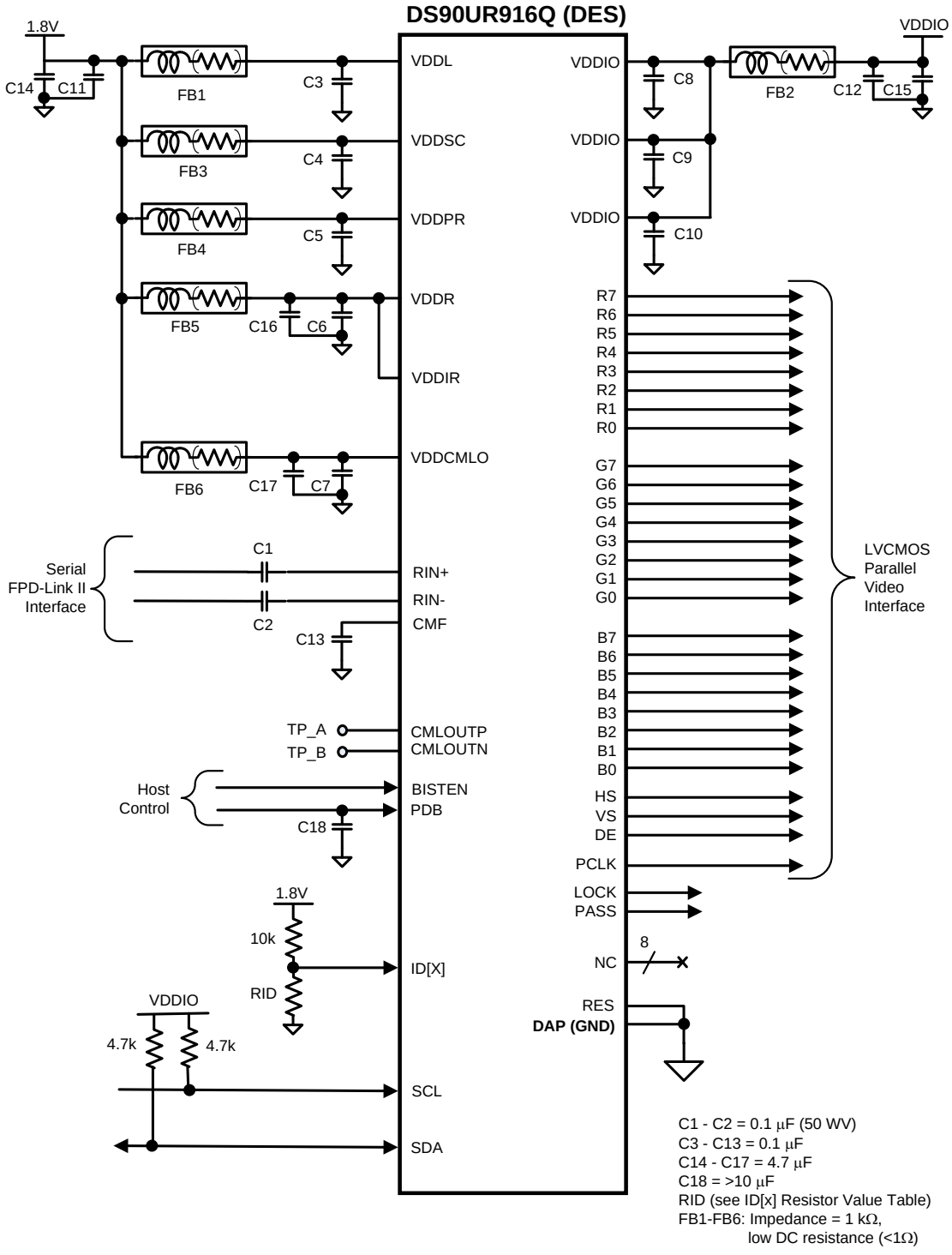

Figure 31. DS90UR916Q Typical Connection Diagram — Pin Control

POWER UP REQUIREMENTS AND PDB PIN

At power-on, the PDB pin must be LOW. The transition to the HIGH state (normal operating mode) may only occur after all power supplies are stable and above the minimum recommended operating voltage. All other LVCMOS inputs must also remain LOW prior to power supplies stabilized at the recommended operating voltages. Active driving of inputs and the transition of PDB to the HIGH state should be delayed 1usec after power supplies are stabilized.

TRANSMISSION MEDIA

The Ser/Des chipset is intended to be used in a point-to-point configuration, through a PCB trace, or through twisted pair cable. The Ser and Des provide internal terminations providing a clean signaling environment. The interconnect for LVDS should present a differential impedance of 100 Ohms. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements.

LIVE LINK INSERTION

The Ser and Des devices support live pluggable applications. The automatic receiver lock to random data “plug & go” hot insertion capability allows the DS90UR916Q to attain lock to the active data stream during a live insertion event.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in TI Application Note: AN-1187 (SNOA401).

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LVDS INTERCONNECT GUIDELINES

See AN-1108 (SNLA008) and AN-905 (SNLA035) for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the TI web site at: www.ti.com/lvds

USING IMAGE ENHANCEMENT FEATURES

The DS90UR916Q offers two FRC dithering blocks and one White Balance lookup table. Depending upon the color depth of the source data, display and LUT contents, these blocks may be independently enabled or disabled in various combinations. Refer to Table 11 below for recommendations.

Table 11. Enabling Image Enhancement Features

Source	White Balance LUT	Display	FRC1	FRC2
24-bit	24-bit	24-bit	Disabled	Disabled
24-bit	24-bit	18-bit	Disabled	Enabled
24-bit	18-bit	18-bit	Enabled	Disabled
18-bit	24-bit	24-bit	Disabled	Disabled
18-bit	24-bit	18-bit	Disabled	Enabled
18-bit	18-bit	18-bit	Disabled	Disabled

If the white balance feature is to be used all 3 LUTs must be fully loaded after initial power-up. LUTs must be loaded sequentially — first Red, second Green, third Blue — and all 256 values must be loaded into each LUT. **After power-up the following procedure must be followed.**

1. Power-on (reload = disable by default)
2. Enable WB
3. Set page Register RED
4. Initial RED LUT load (all 256 bytes) *'916 will self clear page register*
5. Set page Register GREEN
6. Initial GREEN LUT load (all 256 bytes) *'916 will self clear page register*
7. Set page Register BLUE
8. Initial BLUE LUT load (all 256 bytes) *'916 will self clear page register*

Once all LUTs are loaded, '916 will enable the WB output

To reload LUT contents, after the initial load at power-up, the following procedure must be followed.

1. Enable RELOAD
2. Set appropriate page register (RED, GREEN or BLUE)
3. Load new LUT values (any sequence, any order, any number)
4. Load appropriate R, G or B 255 value to clear page register
5. Set appropriate page register (RED, GREEN or BLUE)
6. Load new LUT values (any sequence, any order, any number)
7. Load appropriate R, G or B 255 value to clear page register

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8. Set appropriate page register (RED, GREEN or BLUE)
9. Load new LUT values (any sequence, any order, any number)
10. Load appropriate R, G or B 255 value to clear page register
11. Disable RELOAD

ALTERNATE COLOR / DATA MAPPING

Color Mapped data Pin names are provided to specify a recommended mapping for 24-bit Color Applications. Seven [7] is assumed to be the MSB, and Zero [0] is assumed to be the LSB. While this is recommended it is not required. When connecting to earlier generations of FPD-Link II Ser and Des devices, a color mapping review is recommended to ensure the correct connectivity is obtained. Table 12 provides examples for interfacing to 18-bit applications with or without the video control signals embedded. The DS90UR916Q Des also provides additional flexibility with the MAP_SEL feature as well.

Table 12. Alternate Color / Data Mapping — See Text Below

18-bit RGB	18-bit RGB	18-bit RGB	24-bit RGB	905 Pin Name		916 Pin Name	24-bit RGB	18-bit RGB	18-bit RGB	18-bit RGB
0	LSB R0	GP0	RO	RO		R0	R0	GP0	LSB R0	0
0	R1	GP1	R1	R1		R1	R1	GP1	R1	0
R0	R2	R0	R2	R2		R2	R2	R0	R2	R0
R1	R3	R1	R3	R3		R3	R3	R1	R3	R1
R2	R4	R2	R4	R4		R4	R4	R2	R4	R2
R3	MSB R5	R3	R5	R5		R5	R5	R3	MSB R5	R3
R4	LSB G0	R4	R6	R6		R6	R6	R4	LSB G0	R4
R5	G1	R5	R7	R7		R7	R7	R5	G1	R5
0	G2	GP2	G0	G0		G0	G0	GP2	G2	0
0	G3	GP3	G1	G1		G1	G1	GP3	G3	0
G0	G4	G0	G2	G2		G2	G2	G0	G4	G0
G1	MSB G5	G1	G3	G3		G3	G3	G1	MSB G5	G1
G2	LSB B0	G2	G4	G4		G4	G4	G2	LSB0	G2
G3	B1	G3	G5	G5		G5	G5	G3	B1	G3
G4	B2	G4	G6	G6		G6	G6	G4	B2	G4
G5	B3	G5	G7	G7		G7	G7	G5	B3	G5
0	B4	GP4	B0	B0		B0	B0	GP4	B4	0
0	MSB B5	GP5	B1	B1		B1	B1	GP5	MSB B5	0
B0	HS	B0	B2	B2		B2	B2	B0	HS	B0
B1	VS	B1	B3	B3		B3	B3	B1	VS	B1
B2	DE	B2	B4	B4		B4	B4	B2	DE	B2
B3	GP0	B3	B5	B5		B5	B5	B3	GP0	B3
B4	GP1	B4	B6	B6		B6	B6	B4	GP1	B4
B5	GP2	B5	B7	B7		B7	B7	B5	GP2	B5
HS	GND	HS	HS	HS		HS	HS	HS	GND	HS
VS	GND	VS	VS	VS		VS	VS	VS	GND	VS
DE	GND	DE	DE	DE		DE	DE	DE	GND	
Scenario 4	**Scenario 3**	**Scenario 2**	**Scenario 1**	**905 Pin Name**		**916 Pin Name**	**Scenario 1**	**Scenario 2**	**Scenario 3**	**Scenario 4**

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Scenario 4

Scenario 4 supports an 18-bit RGB color mapping and 3 embedded video control signals. All LSBs are set to “0”. FRC and white balance may be enabled with this scenario.

Scenario 3

Scenario 3 supports an 18-bit RGB color mapping, 3 un-embedded video control signals, and up to three general purpose signals. This scenario is NOT supported when FRC or white balance are enabled on the DS90UR916.

Scenario 2

Scenario 2 supports an 18-bit RGB color mapping, 3 embedded video control signals, and up to six general purpose signals. This scenario is NOT supported when FRC or white balance are enabled on the DS90UR916.

Scenario 1

Scenario 1 supports the 24-bit RGB color mapping, along with the 3 embedded video control signals. This is the native mode for the chipset. FRC and white balance may be enabled with this scenario.

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REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	39

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS90UR916QSQ/NOPB	ACTIVE	WQFN	NKB	60	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UR916QSQ	Samples
DS90UR916QSQE/NOPB	ACTIVE	WQFN	NKB	60	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UR916QSQ	Samples
DS90UR916QSQX/NOPB	ACTIVE	WQFN	NKB	60	2000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UR916QSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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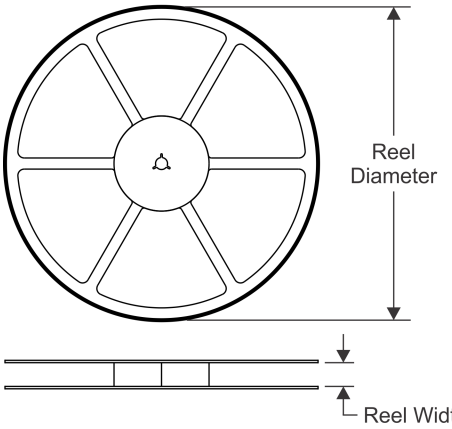
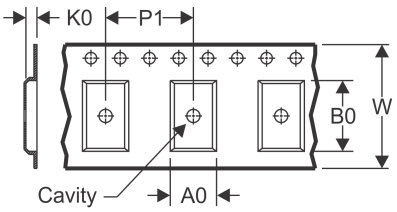
TAPE AND REEL INFORMATION

REEL DIMENSIONS

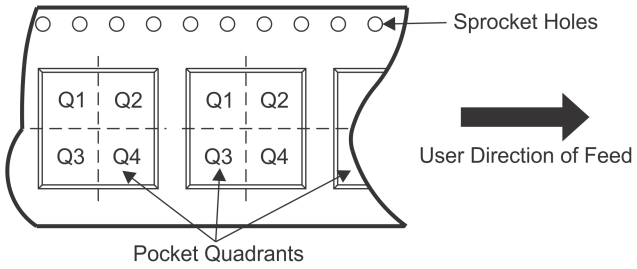


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

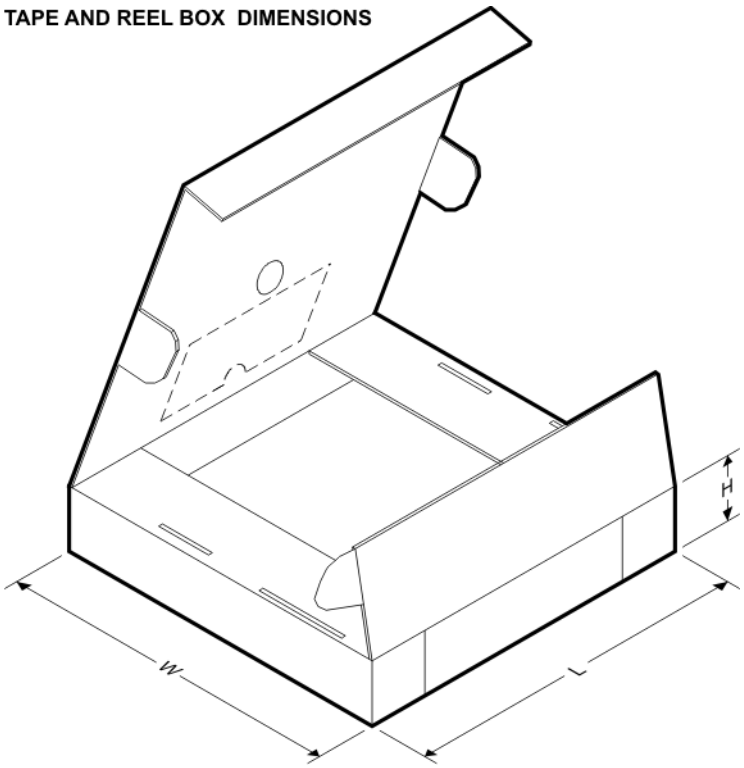
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UR916QSQ/NOPB	WQFN	NKB	60	1000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS90UR916QSQE/NOPB	WQFN	NKB	60	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS90UR916QSQX/NOPB	WQFN	NKB	60	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

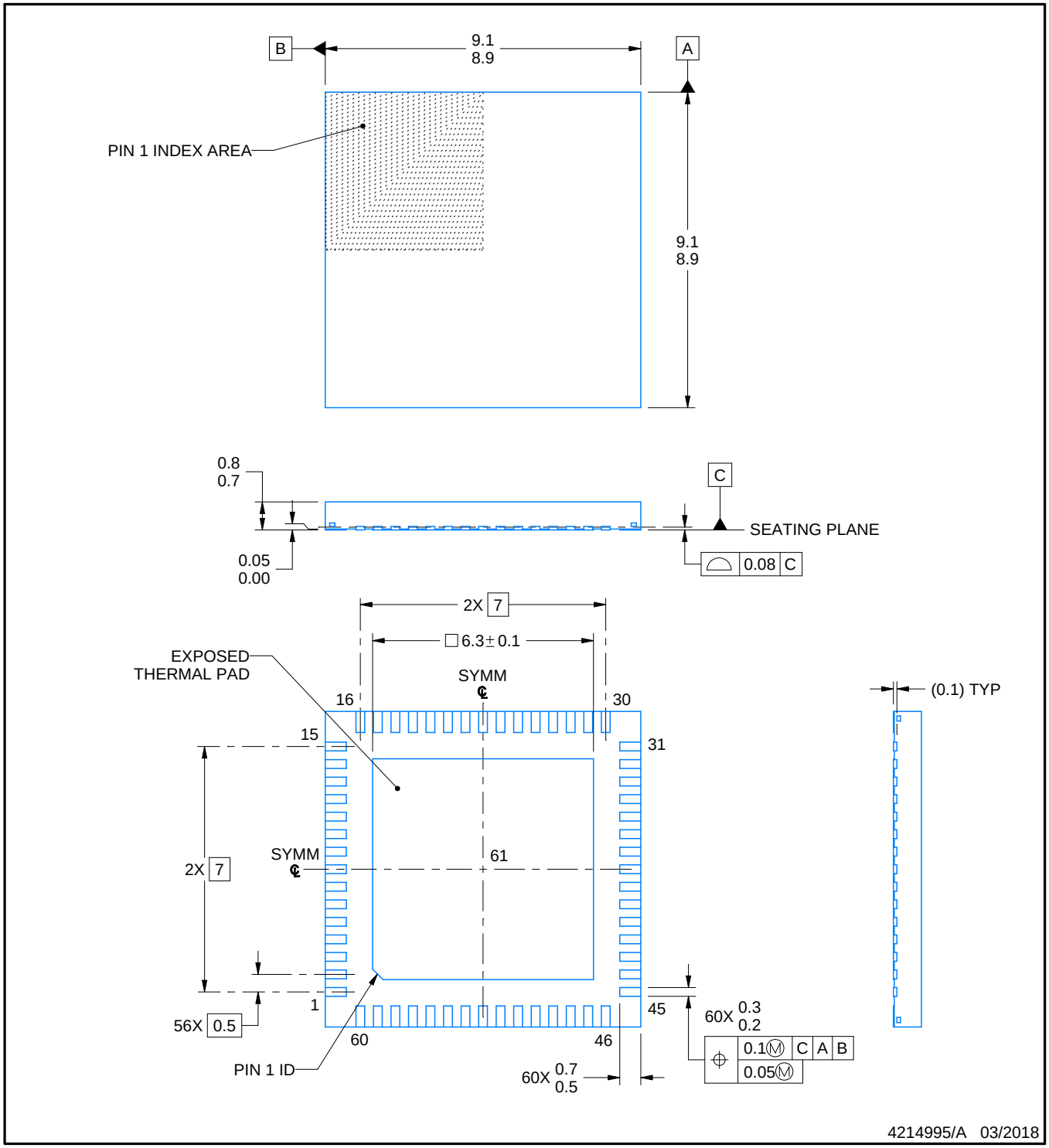
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UR916QSQ/NOPB	WQFN	NKB	60	1000	367.0	367.0	38.0
DS90UR916QSQE/NOPB	WQFN	NKB	60	250	210.0	185.0	35.0
DS90UR916QSQX/NOPB	WQFN	NKB	60	2000	367.0	367.0	38.0

NKB0060B

PACKAGE OUTLINE

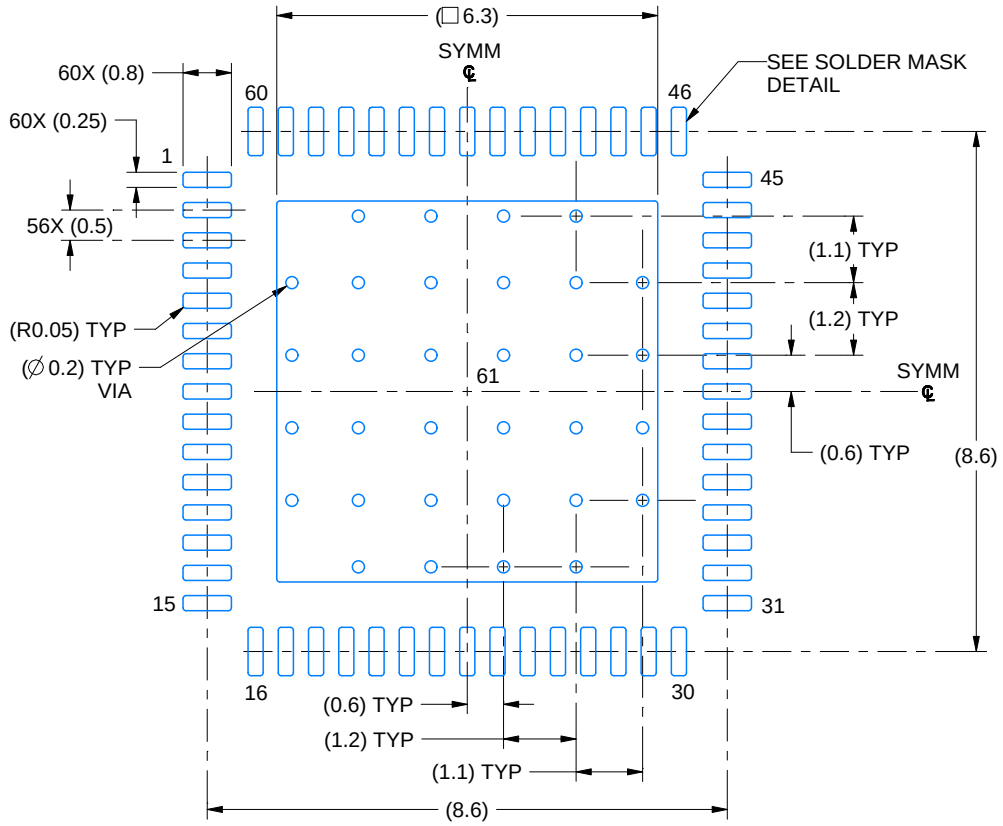
VQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

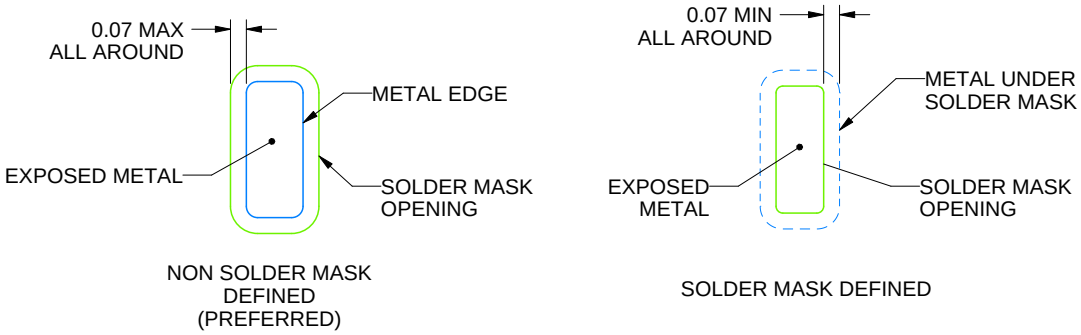


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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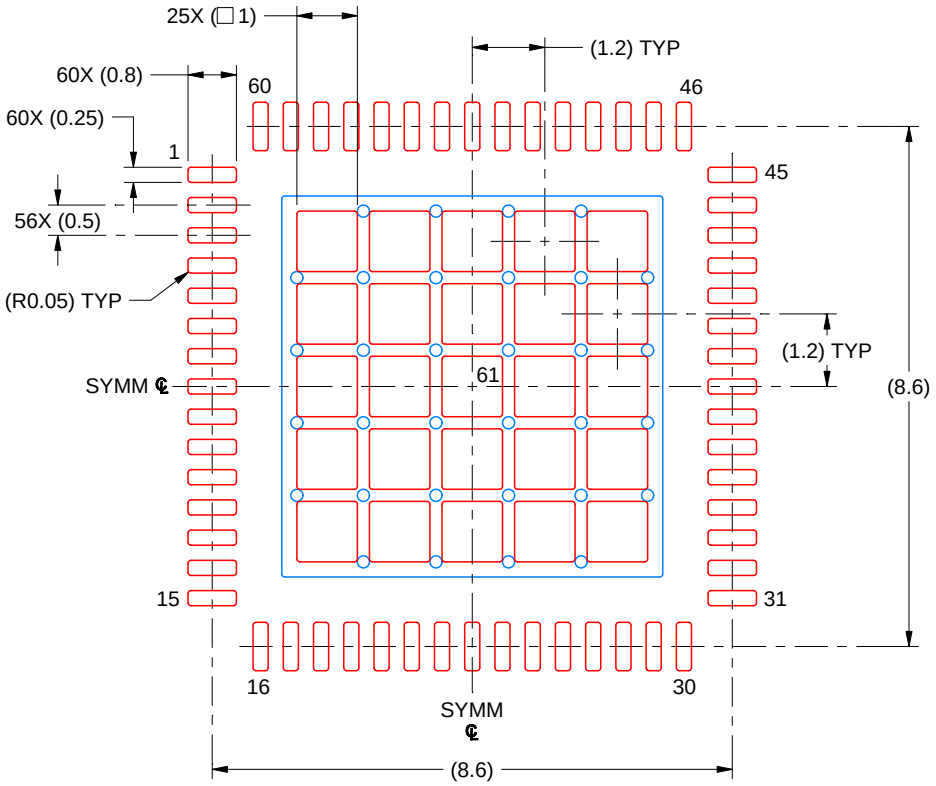
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

EXPOSED PAD 61
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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