THE DATASHEET OF

EL7554IREZ-T7

EL7554

Monolithic 4A DC/DC Step-Down Regulator

FN7360
Rev 5.00
November 5, 2007

The EL7554 is a full-feature synchronous 4A step-down regulator capable of up to 96% efficiency. This device operates from 3V to 6V V_{IN} input supply. With internal CMOS power FETs, the device can operate at up to 100% duty ratio, allowing for output voltage range from 0.8V up to nearly V_{IN}.The adjustable high switching frequency of up to 1MHz enables the use of small components, making the whole converter occupy less than 0.58 square inch with components on one side of the PCB. The EL7554 operates at constant frequency PWM mode, making external synchronization possible. The EL7554 features soft-start and full start-up control, which eliminates the in-rush current and enables users to control the start-up of multiple converters to any configuration with ease. The EL7554 also offers a ±5% voltage margining capability that allows raising and lowering of the supplies derived from the EL7554 to validate the performance and reliability of system cards quickly and easily during manufacturing testing. A junction temperature indicator conveniently monitors the silicon die temperature, saving designers time in the tedious thermal characterization.

An easy-to-use simulation tool is available for download and can be used to modify design parameters such as switching frequency, voltage ripple, ambient temperature, as well as view schematics waveforms, efficiency graphs, and complete BOM with Gerber layout.

The EL7554 is available in a 28 Ld HTSSOP package and is specified for operation over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
EL7554IRE*	7554IRE	-40 to +85	28 Ld HTSSOP	MDP0048
EL7554IREZ* (See Note)	7554IREZ	-40 to +85	28 Ld HTSSOP (Pb-free)	MDP0048

*Add “-T7” or “-T13” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Integrated MOSFETs
- 4A continuous output current
- Up to 96% efficiency
- All ceramic capacitors
- Multiple supply start-up tracking
- Built-in ±5% voltage margining
- 3V to 6V input voltage
- 0.58 in^2 footprint with components on one side of PCB
- Adjustable switching frequency to 1MHz
- Oscillator synchronization possible
- 100% duty ratio
- Junction temperature indicator
- Over-temperature protection
- Internal soft-start
- Variable output voltage down to 0.8V
- Power-good indicator
- 28 Ld HTSSOP package
- Pb-free available (RoHS compliant)

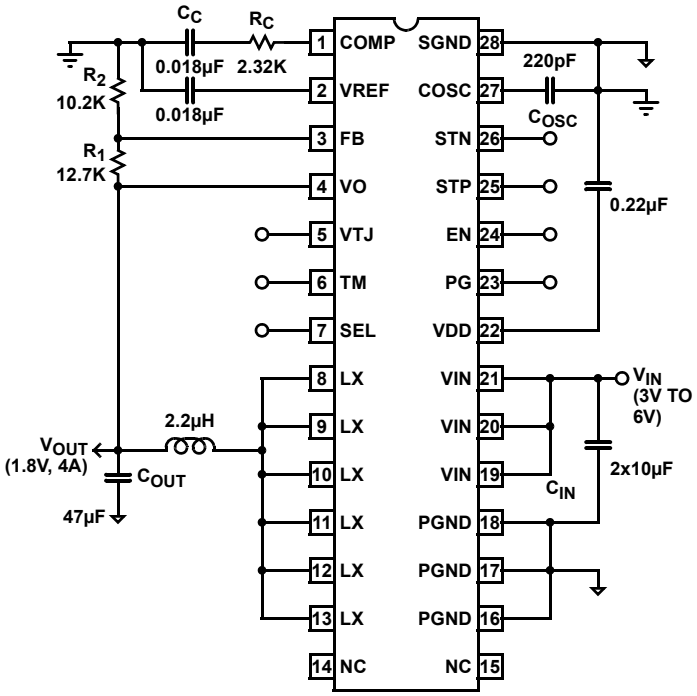
Applications

- Point-of-regulation power supplies
- FPGA Core and I/O supplies
- DSP, CPU Core, and IO supplies
- Logic/Bus supplies
- Portable equipment

Related Documentation

- Technical Brief 418 - Using the EL7554 Demo Board
- Easy to use applications software simulation tool available at www.intersil.com/dc-dc

Typical Application Diagram



Absolute Maximum Ratings (T_A = +25°C)

V_{IN}, V_{DD} to SGND . . . . . -0.3V to +6.5V
VX to PGND . . . . . -0.3V to V_{IN} +0.3V
SGND to PGND . . . . . -0.3V to +0.3V
COMP, V_{REF}, FB, V_O, V_{TJ}, TM,
SEL, PG, EN, STP, STN, C_{OSC} to SGND . . . . . -0.3V to V_{DD} +0.3V

Storage Temperature . . . . . .-65°C to +150°C
Junction Temperature . . . . . .+125°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

$V_{DD} = V_{IN}$ = 3.3V, $T_A = T_J$ = +25°C, C_{OSC} = 390pF, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		3		6	V
V_{REF}	Reference Accuracy		1.24	1.26	1.28	V
V_{REFTC}	Reference Temperature Coefficient			50		ppm/°C
$V_{REFLOAD}$	Reference Load Regulation	$0 < I_{REF} < 50\mu A$	-1			%
V_{RAMP}	Oscillator Ramp Amplitude			1.15		V
I_{OSC_CHG}	Oscillator Charge Current	$0.1V < V_{OSC} < 1.25V$		200		µA
I_{OSC_DIS}	Oscillator Discharge Current	$0.1V < V_{OSC} < 1.25V$		8		mA
I_{VDD}	V_{DD} Supply Current	V_{EN} = 1 (L disconnected)	2	2.7	5	mA
I_{VDD_OFF}	V_{DD} Standby Current	EN = 0		1	1.5	mA
V_{DD_OFF}	V_{DD} for Shutdown		2.4		2.65	V
V_{DD_ON}	V_{DD} for Startup		2.6		2.95	V
T_{OT}	Over-temperature Threshold			135		°C
T_{HYS}	Over-temperature Hysteresis			20		°C
I_{LEAK}	Internal FET Leakage Current	EN = 0, L_X = 6V (low FET), L_X = 0V (high FET)			10	µA
I_{LMAX}	Peak Current Limit		6			A
R_{DSON1}	PFET On Resistance			35	70	mΩ
$R_{DSONTC2}$	NFET On Resistance			30	60	mΩ
R_{DSONTC}	R_{DSON} Tempco			0.2		mΩ/°C
I_{STP}	STP Pin Input Pull-down Current	$V_{STP} = V_{IN}/2$	-4	2.5		µA
I_{STN}	STN Pin Input Pull-up Current	$V_{STN} = V_{IN}/2$		2.5	4	µA
V_{PGP}	Positive Power Good Threshold	With respect to target output voltage	6		14	%
V_{PGN}	Negative Power Good Threshold	With respect to target output voltage	-14		-6	%
V_{PG_HI}	Power Good Drive High	I_{PG} = 1mA	2.6			V
V_{PG_LO}	Power Good Drive Low	I_{PG} = -1mA			0.5	V
V_{OVP}	Output Over-voltage Protection			10		%
V_{FB}	Output Initial Accuracy	I_{LOAD} = 0A	0.79	0.8	0.81	V
V_{FB_LINE}	Output Line Regulation	V_{IN} = 3.3V, ΔV_{IN} = 10%, I_{LOAD} = 0A		0.2	0.5	%
GM_{EA}	Error Amplifier Transconductance	V_{CC} = 0.65V	85	125	165	µs
V_{FB_TC}	Output Temperature Stability	$0°C < T_A < +85°C$, I_{LOAD} = 3A		±1		%
F_S	Switching Frequency		300	370	440	kHz
I_{FB}	Feedback Input Pull-up Current	V_{FB} = 0V		100	200	nA

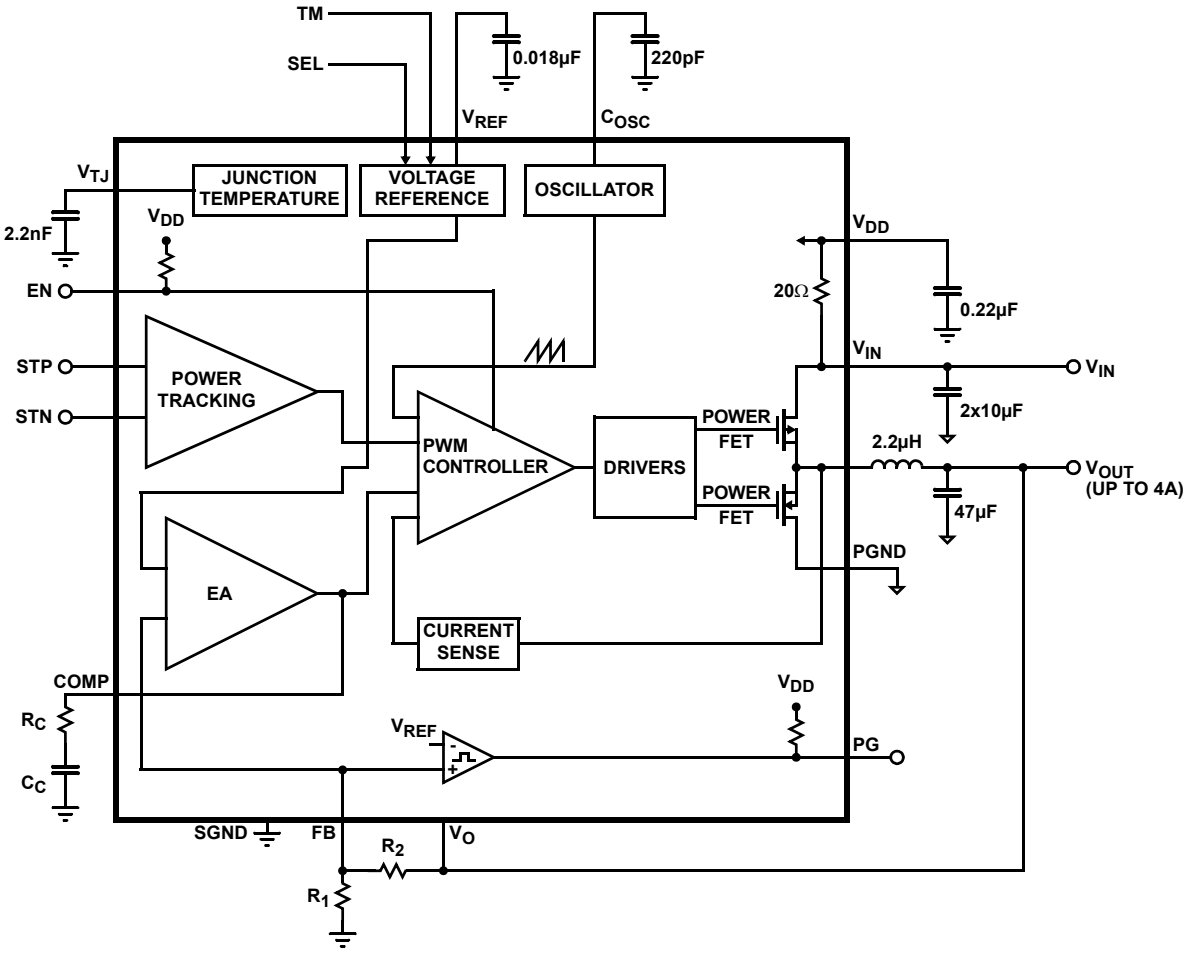
DC Electrical Specifications $V_{DD} = V_{IN} = 3.3V$, $T_A = T_J = +25°C$, $C_{OSC} = 390pF$, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{EN_HI}	EN Input High Level		2.6			V
V_{EN_LO}	EN Input Low Level				1	V
I_{EN}	Enable Pull-up Current	$V_{EN} = 0$	-4	-2.5		µA
TM, S_{EL_HI}	Input High Level		2.6			V
TM, S_{EL_LO}	Input Low Level				1	V

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	COMP	Error amplifier output; place loop compensation components here
2	VREF	Bandgap reference bypass capacitor; typically 0.01µF to 0.047µF to SGND
3	FB	Voltage feedback input; connected to external resistor divider between V_{OUT} and SGND for adjustable output; also used for speed-up capacitor connection
4	VO	Output sense for fixed output; also used for speed-up capacitor connection
5	VTJ	Junction temperature monitor output, connected to a 0.01µF - 0.047µF to SGND
6	TM	Stress test enable; allows ±5% output movement; needs a pull-down resistor (1k - 100k); connect to SGND if function is not used
7	SEL	Positive or negative voltage margining set pin; needs a pull-down resistor (1k - 100k); connect to SGND if function is not used
8, 9, 10, 11, 12, 13	LX	Inductor drive pin; high current output whose average voltage equals the regulator output voltage
14, 15	NC	Not used
16, 17, 18	PGND	Ground return of the regulator; connected to the source of the low-side synchronous NMOS Power FET
19, 20, 21	VIN	Power supply input of the regulator; connected to the drain of the high-side PMOS Power FET
22	VDD	Control circuit positive supply; connected to V_{IN} through an internal 20Ω resistor
23	PG	Power-good window comparator output; logic 1 when regulator output is within ±10% of target output voltage
24	EN	Chip enable, active high; a 2µA internal pull-up current enables the device if the pin is left open; a capacitor can be added at this pin to delay the start of a converter
25	STP	Auxilliary supply tracking positive input; tied to regulator output to synchronize start-up with a second supply; leave open for standalone operation; 2µA internal pull-up current
26	STN	Auxiliary supply tracking negative input; connect to output of a second supply to synchronize start-up; leave open for standalone operation; 2µA internal pull-up current
27	COSC	Oscillator timing capacitor (see performance curves)
28	SGND	Control circuit negative supply or signal ground

Block Diagram



Typical Performance Curves

$V_{IN} = V_D = 3.3V$, $V_O = 1.8V$, $I_O = 4A$, $L = 2.2\mu H$, $C_{IN} = 2x10\mu F$, $C_{OUT} = 47\mu F$, $C_{OSC} = 220pF$, $T_A = +25°C$ unless otherwise noted.

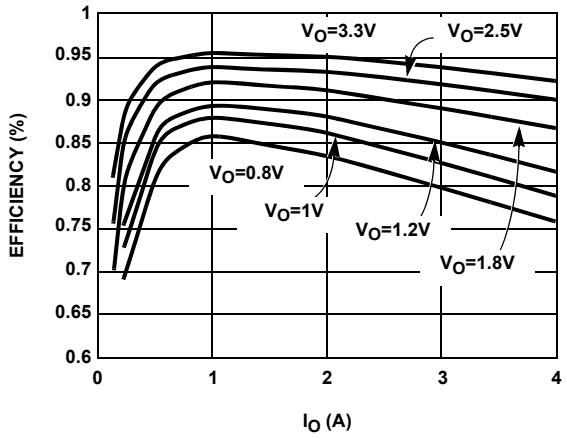


FIGURE 1. EFFICIENCY (V_{IN} = 5V)

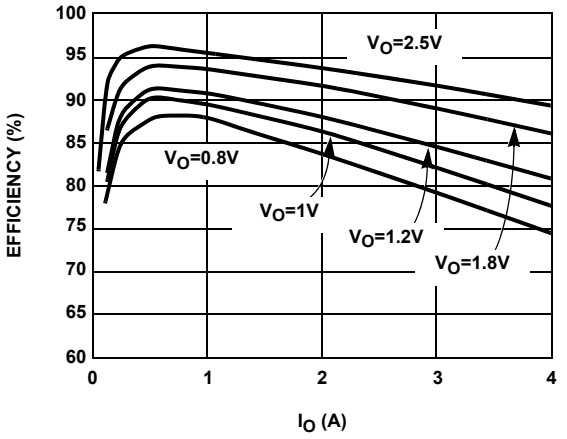


FIGURE 2. EFFICIENCY (V_{IN} = 3.3V)

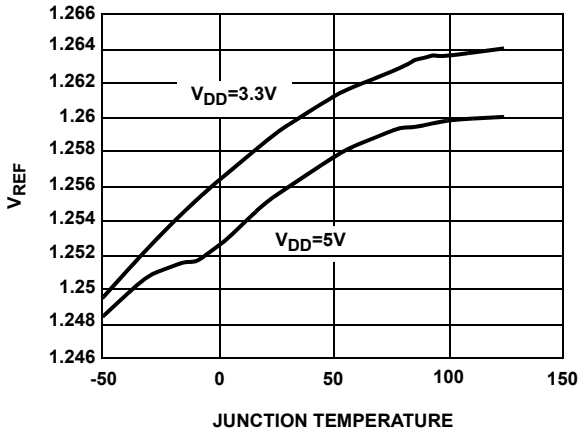


FIGURE 3. V_{REF} vs TEMPERATURE

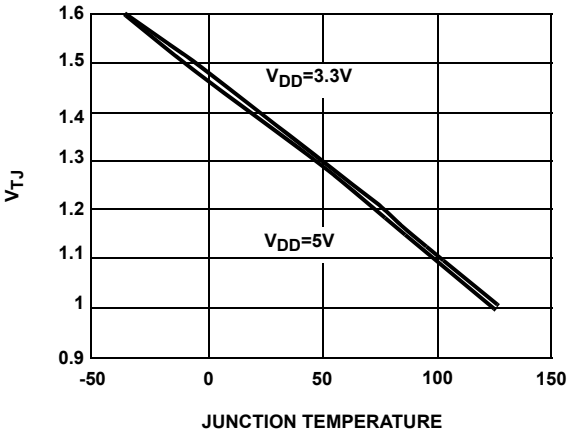


FIGURE 4. V_{TJ} vs TEMPERATURE

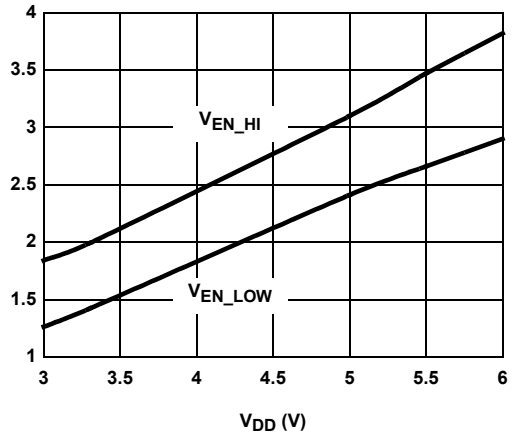


FIGURE 5. V_{EN_HI} & V_{EN_LOW} vs V_{DD}

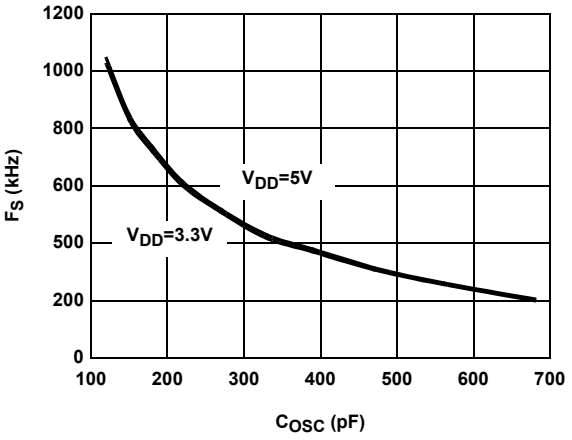


FIGURE 6. F_S vs C_{OSC}

Typical Performance Curves (Continued)

V_{IN} = V_D = 3.3V, V_O = 1.8V, I_O = 4A, L = 2.2µH, C_{IN} = 2x10µF, C_{OUT} = 47µF, C_{OSC} = 220pF, T_A = +25°C unless otherwise noted.

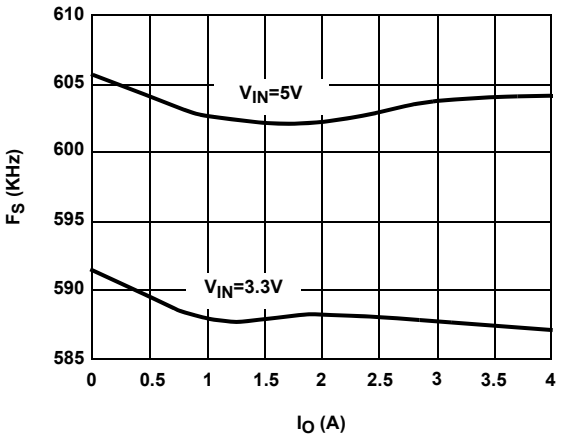


FIGURE 7. F_S vs I_O

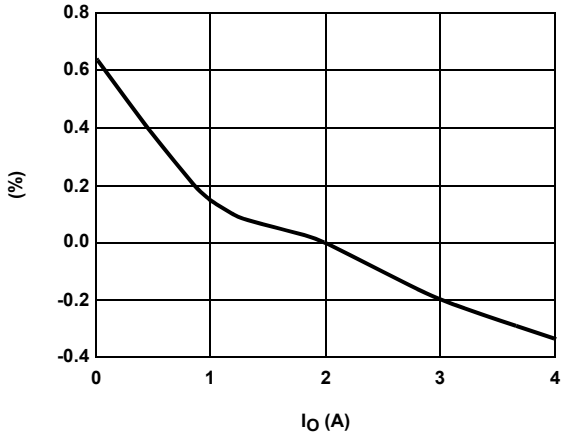


FIGURE 8. LOAD REGULATIONS

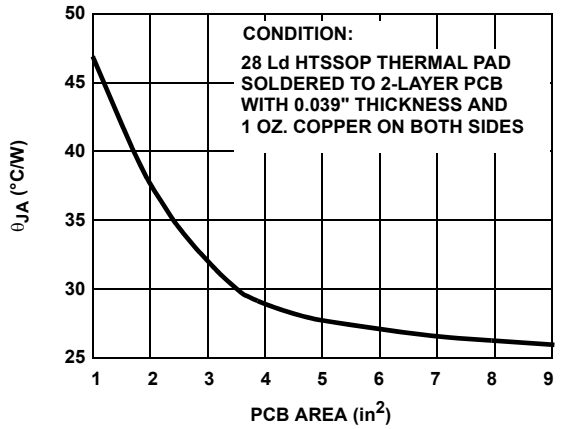


FIGURE 9. HTSSOP THERMAL RESISTANCE vs PCB AREA (NO AIR FLOW)

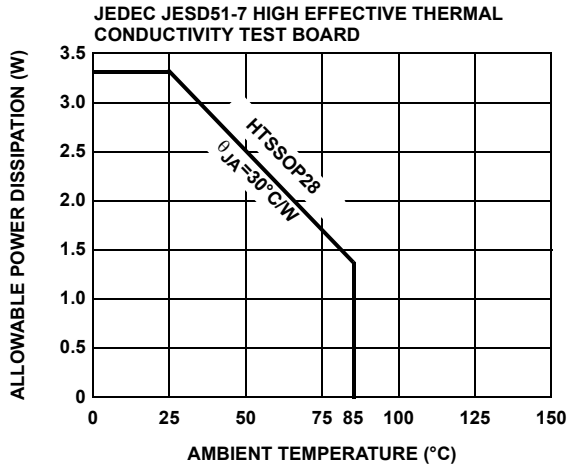


FIGURE 10. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

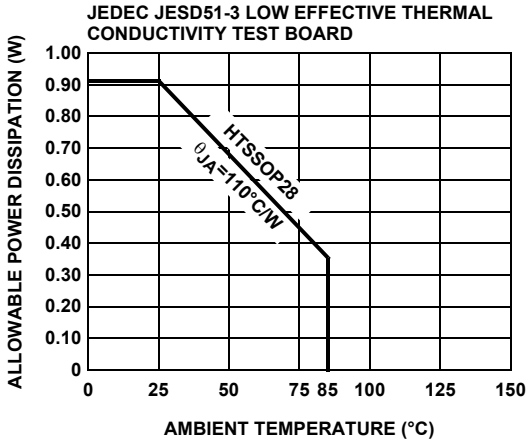


FIGURE 11. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Waveforms

V_{IN} = V_D = 3.3V, V_O = 1.8V, I_O = 4A, L = 2.2µH, C_{IN} = 2x10µF, C_{OUT} = 47µF, C_{OSC} = 220pF, T_A = +25°C unless otherwise noted.

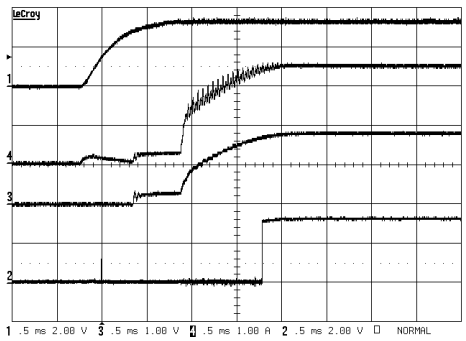


FIGURE 12. START-UP

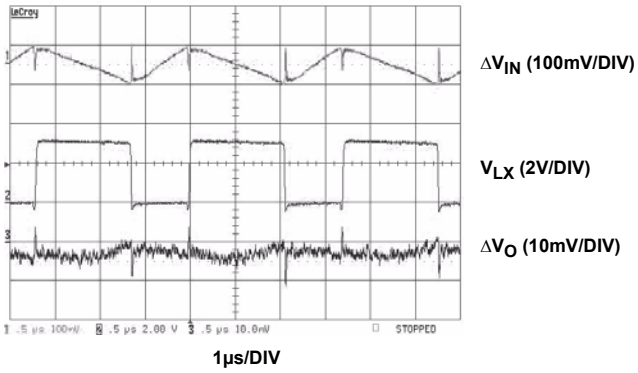


FIGURE 13. STEADY-STATE OPERATION

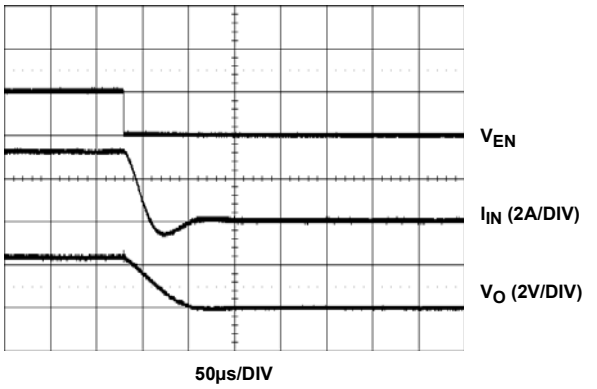


FIGURE 14. SHUT-DOWN

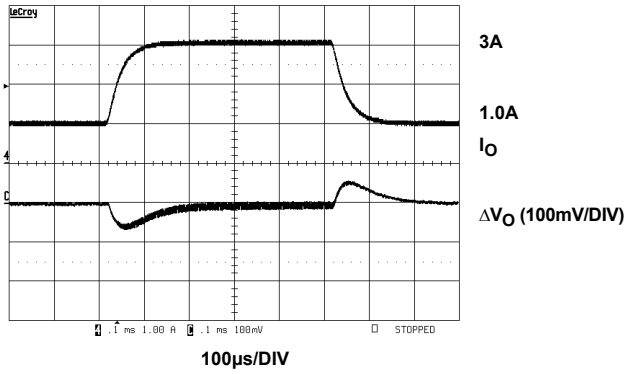


FIGURE 15. TRANSIENT RESPONSE

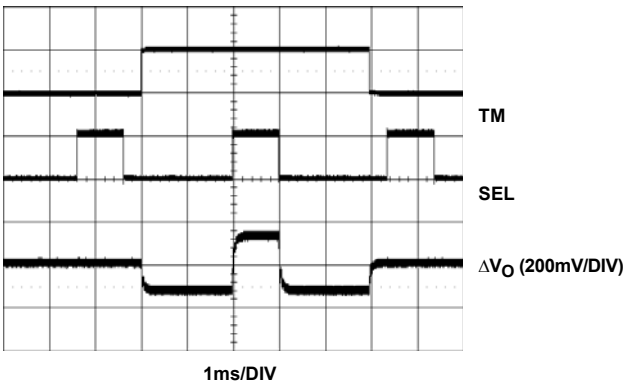


FIGURE 16. VOLTAGE MARGINING

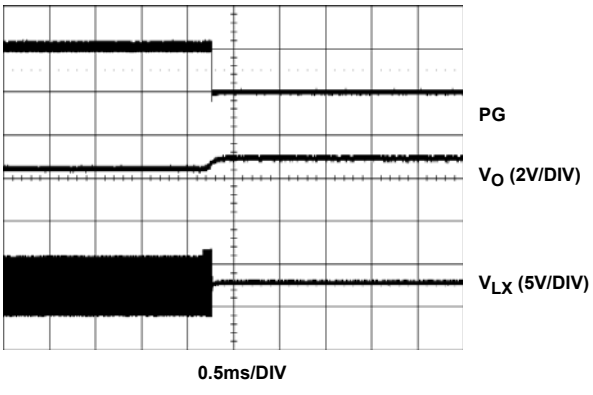


FIGURE 17. OVER-VOLTAGE SHUT-DOWN

Waveforms (Continued)

V_{IN} = V_D = 3.3V, V_O = 1.8V, I_O = 4A, L = 2.2µH, C_{IN} = 2x10µF, C_{OUT} = 47µF, C_{OSC} = 220pF, T_A = +25°C unless otherwise noted.

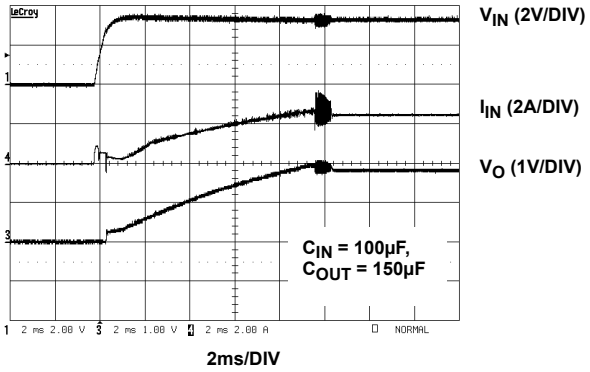


FIGURE 18. ADJUSTABLE START-UP

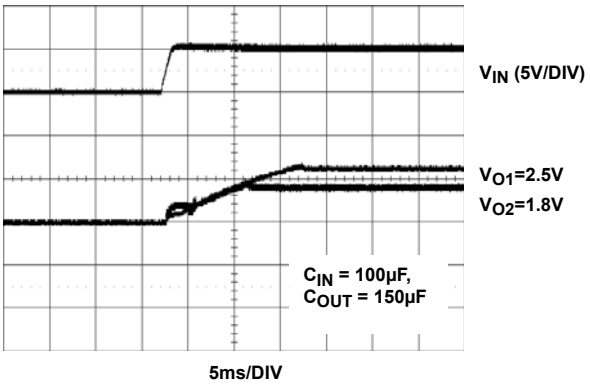


FIGURE 19. TRACKING START-UP

Detailed Description

The EL7554 is a full-feature synchronous 6A step-down regulator capable of up to 96% efficiency. This device operates from 3V to 6V V_{IN} input supply. With internal CMOS power FETs, the device can operate at up to 100% duty ratio, allowing for output voltage range from 0.8V up to nearly V_{IN}.The adjustable high switching frequency of up to 1MHz enables the use of small components, making the whole converter occupy less than 0.58 square inch with components on one side of the PCB. The EL7554 operates at constant frequency PWM mode, making external synchronization possible. Patented on-chip resistorless current-sensing enables current mode control, which provides over-current protection, and excellent step load response. The EL7554 features soft-start and full start-up control, which eliminate the in-rush current and enables users to control the start-up of multiple converters to any configuration with ease. The EL7554 also offers a ±5% voltage margining capability that allows raising and lowering of the supplies derived from the EL7554 to validate the performance and reliability of system cards quickly and easily during manufacturing testing. A junction temperature indicator conveniently monitors the silicon die temperature, saving designers time in the tedious thermal characterization.

Start-Up

The EL7554 employs a special soft-start to suppress the in-rush current (see Figure 12). The start-up process takes about 2ms and begins when the input voltage reaches about 2.8V and EN pin voltage 2V. When EN is released from LOW, or the converter comes out of thermal shut-down mode, the soft-start process repeats. When the input voltage ramps up too slowly, slight over- current at the input can occur. Connecting a small capacitor at EN will delay the start-up. The delay time T_D can be calculated by:

$$T_D = C_{EN} \times \frac{V_{EN\_HI}}{I_{EN}}$$

where:

- C_{EN} is the capacitance at EN pin
- V_{EN_HI} is the EN input high level (function of V_{DD} voltage, see Figure 5)
- I_{EN} is the EN pin pull-up current, nominal 2.5µA

If a slower than 2ms soft start-up is needed, please refer to Full Start-Up Control section.

Steady-State Operation

The converter always operates at fixed frequency continuous-conduction mode. For fast transient response, peak current control method is employed. The inductor current is sensed from the upper PFET. This current signal, the slope compensation, and the compensated error signal are fed to the PWM comparator to generate the PWM signal for the internal power switches. When the upper PFET is on, the low-side NFET is off and input voltage charges the inductor. When PFET is off, the NFET is on and energy stored in the inductor is dumped to the output to maintain constant output voltage. Therefore, the LX waveform is always a stable square waveform (see Figure 13) with peak close to V_{IN}. So LX is a good indication that the converter is operating properly.

100% Duty Ratio

EL7554 uses CMOS as internal synchronous power switches. The upper switch is a PMOS and the lower switch an NMOS. This not only saves a boot capacitor, it also allows 100% turn-on of the upper PFET switch, achieving

V_O close to V_{IN}. The maximum achievable V_O is:

$$V_O = V_{IN} - (R_L + R_{DSON1}) \times I_O$$

Where R_L is the DC resistance on the inductor and R_{DSON1} is the PFET on-resistance, nominal 35mΩ at room temperature with tempco of 0.2mΩ/°C.

Output Voltage Selection

The output voltage can be as high as the input voltage minus the PMOS and inductor voltage drops. Use R_1 and R_2 to set the output voltage according to the following formula:

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Standard values of R_1 and R_2 are listed in Table 1.

TABLE 1.

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	2	Open
1	2.49	10
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	36	11.5

Voltage Margining

The EL7554 has built-in 5% load stress test (commonly called voltage margining) function. Combinations of TM and SEL set the margins shown in Table 2. When this function is not used, both pins should be connected to SGND, either directly or through a 10kΩ resister. Figure 16 shows this feature.

TABLE 2.

CONDITION	TM	SEL	V_O
Normal	0	X	Nominal
High Margin	1	1	Nominal + 5%
Low Margin	1	0	Nominal - 5%

Switching Frequency

The regulator operates from 200kHz to 1MHz. The switching frequency is generated by a relaxation comparator and adjusted by a C_{OSC}. The triangle waveform has 95% duty ratio and runs from 0.2V to 1.2V. Please refer to Figure 6 for a specific frequency.

When external synchronization is required, use the following circuit for connection. Always choose the converter self-switching frequency 20% lower than the sync frequency to accommodate component variations.

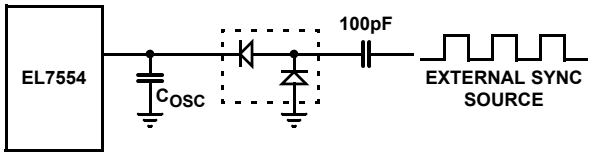


FIGURE 20. EXTERNAL SYNC CIRCUIT

Thermal Protection and Junction Temperature Indicator

An internal temperature sensor continuously monitors the junction temperature. In the event that the junction temperature exceeds +135°C, the regulator is in a fault condition and will shut down. When the temperature falls back below +110°C, the regulator goes through the soft-start procedure again.

The V_{TJ} pin is an accurate indicator of the internal silicon junction temperature T_J, which can be determined by the following formula. This saves engineering time.

$$T_J = 75 + \frac{1.2 - V_{TJ}}{0.00384}$$

where VTJ is the voltage at VTJ pin.

Under-Voltage Lockout (UVLO)

When V_{DD} falls bellow 2.5V, the regulator shuts down. When V_{DD} rises above 2.8V, converter goes through soft-start process again.

Power Good Indicator (PG) and Over-Voltage Protection

When the output reaches 10% of the preset voltage, the PG pin outputs a HI signal as shown in the start-up waveform (Figure 12). If the output voltage is higher than 10% of the preset value for any reason, PG will go low and the regulator will shut down. In addition to the indication power is good, the PG pin can be used for multiple regulators' start-up control as described in the next section.

Full Start-Up Control

The EL7554 offers full start-up control. The core of this control is a start-up comparator in front of the main PWM controller. The STP and STN are the inputs to the comparator, whose HI output forces the PWM comparator to skip switching cycles. The user can choose any of the following control configurations:

1. ADJUSTABLE SOFT-START

In this configuration, the ramp-up time is adjustable to any time longer than the building soft-start time of 2ms. The approximate ramp-up time, T_{ST}, is:

$$T_{ST} = RC\left(\frac{V_O}{V_{IN}}\right)$$

Figure 18 shows the waveforms.

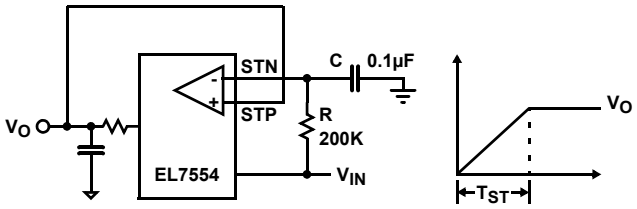


FIGURE 21. ADJUSTABLE START-UP

In this application, C_{IN} and C_{OUT} may be increased to reduce input/output ripple because the pulse skipping nature of the method.

2. CASCADE START-UP

In this configuration, EN pin of Regulator 2 is connected to the PG pin of Regulator 1 (Figure 22). V_{O2} will only start after V_{O1} is good.

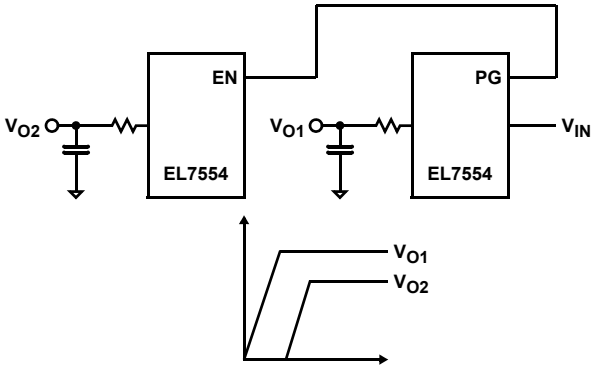


FIGURE 22. CASCADE START-UP

3. LINEAR START-UP

In the linear start-up tracking configuration, the regulator with lower output voltage, V_{O2}, tracks the one with higher output voltage, V_{O1}. The waveform is shown in Figure 19.

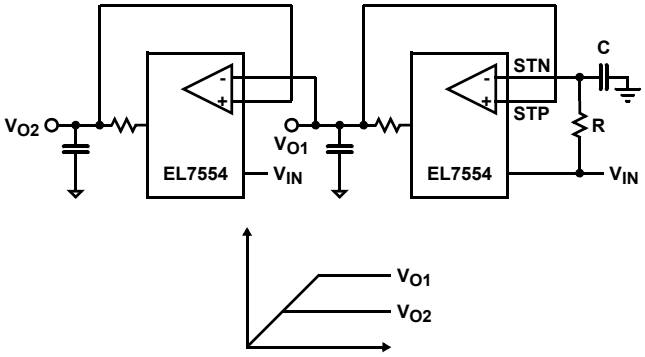


FIGURE 23. LINEAR START-UP TRACKING

4. OFFSET START-UP

Compared with the cascade start-up, this configuration allows Regulator 2 to begin the start-up process when V_{O1} reaches a particular value of $V_{REF}*(1+R_B/R_A)$ before PG goes HI, where V_{REF} is the regulator reference voltage. V_{REF}=1.26.

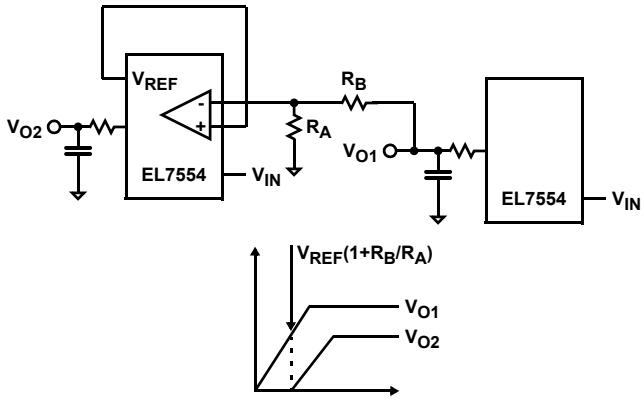


FIGURE 24. OFFSET START-UP TRACKING

Component Selection

INPUT CAPACITOR

The main functions of the input capacitor(s) are to maintain the input voltage steady and to filter out the pulse current passing through the upper switch. The root-mean-square value of this current is:

$$I_{IN,RMS} = \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \times I_O \approx 1/2(I_O)$$

for a wide range of V_{IN} and V_O.

For long-term reliability, the input capacitor or combination of capacitors must have the current rating higher than $I_{IN,RMS}$. Use X5R or X7R type ceramic capacitors, or SPCAP or POSCAP types of Polymer capacitors for their high current handling capability.

INDUCTOR

The NFET positive current limit is set at about 5A. For optimal operation, the peak-to-peak inductor current ripple ΔI_L should be less than 1A. The following equation gives the inductance value:

$$L = \frac{(V_{IN} - V_O) \times V_O}{V_{IN} \times \Delta I_L \times F_S}$$

The peak current the inductor sees is:

$$I_{LPK} = I_O + \frac{\Delta I_L}{2}$$

When inductor is chosen, make sure the inductor can handle this peak current and the average current of I_O.

OUTPUT CAPACITOR

If there is no holding time requirement for output; output voltage ripple and transient response are the main deciding factors in choosing the output capacitor. Initially, choose the

output capacitor with the ESR to satisfy the output ripple ΔV_O requirement:

$$\Delta V_O = \Delta I_L \times ESR$$

When output has a step load change ΔI_O, the initial voltage drop is ESR*ΔI_O. Then V_O will drop even further before the loop has the chance to respond. The higher the output capacitance, the lower the voltage drop is. Also, higher loop bandwidth will generate less voltage drop. Experiment with the transient response (see Figure 15) to determine the final values of output capacitance.

Like the input capacitor, it is recommended to use X5R or X7R type of ceramic capacitors, or SPCAP or POSCAP type of Polymer capacitors for the low ESR and high capacitance.

Generally, the AC current rating of the output capacitor is not a concern because the RMS current is only $1/\sqrt{12}$ of ΔI_L. This is easily satisfied.

LOOP COMPENSATION

Current mode converter forces the inductor current proportional to the error signal, thus gets rid of the 2nd order effect formed by the inductor and output capacitor. The PWM comparator and the inductor form an equivalent transconductance amplifier. So, a simple Type 1 compensator is good enough to generate a high bandwidth stable converter. The compensation capacitor and resister are decided by:

$$C_C = \frac{V_{FB} \times GM_{PWM} \times GM_{EA}}{\pi \times F_C \times I_{OUT}}$$

$$R_C = 2 \times R_{OUT} \times \frac{C_{OUT}}{C_C}$$

where:

- GM_{PWM} is the transconductance of the PWM comparator, GM_{PWM} = 120s

$$R_{OUT} = \frac{V_{OUT}}{I_{OUT}}$$

- V_{OUT} output voltage
- I_{OUT} output current
- C_{OUT} is output capacitance
- GM_{EA} is the transconductance of the error amplifier, GM_{EA} = 120µs
- F_C is the intended crossover frequency of the loop. For best performance, set this value to about one-tenth of the switching frequency.

Design Example

A 5V to 1.8V converter at 4A is needed.

1. Choose the input capacitor

The input capacitor or combination of capacitors has to be able to take about 1/2 of the output current, e.g., 2A. TDK's C3216X5RIA106M is rated at 2.7A, 6.3V, meeting the above criteria using 2 generators less input voltage ripple.

2. Choose the inductor. Set the converter switching frequency at 600kHz:

$$L = \frac{(V_{IN} - V_O) \times V_O}{V_{IN} \times \Delta I_L \times F_S}$$

ΔI_L = 1A yields 1.72µH. Leave some margin and choose L = 2.2µH. TDK RLF7030-2R2M5R4 has the required current rating.

3. Choose the output capacitor

L = 2.2µH yields about 0.9A inductor ripple current. 47µF ceramic capacitor has less than 5mΩ of ESR easily satisfying by the requirement. ESR is not the only factor deciding the output capacitance. As discussed earlier, output voltage droops less with more capacitance when converter is in load transient. Multiple iterations may be needed before final components are chosen.

4. Loop compensation

50kHz is the intended crossover frequency. With the conditions R_C and C_C are calculated as:

R_C = 2.32kΩ and C_C = 0.018pF

For convenience, Table 3 lists the compensation values for frequently used output voltages.

TABLE 3. COMPENSATION VALUES

V_O (V)	R_C (kΩ)	C_C (µF)
3.3	4.22	0.018
2.5	3.24	0.018
1.8	2.32	0.018
1.5	1.91	0.018
1.2	1.54	0.018
1	1.27	0.018
0.8	1.02	0.018

Thermal Management

The EL7554IRE is packaged in a thermally-efficient HTSSOP-28 package, which utilizes the exposed thermal pad at the bottom to spread heat through PCB metal.

Therefore:

1. The thermal pad must be soldered to the PCB
2. Maximize the PCB area
3. If a multiple layer PCB is used, thermal vias (13 to 25 mil) must be placed underneath the thermal pad to connect to ground plane(s). Do not place thermal reliefs on the vias. Figure 25 shows a typical connection.

The thermal resistance for this package is as low as +26°C/W for 2 layer PCB of 0.39" thickness (see Figure 9). The actual junction temperature can be measured at V_{TJ} pin.

The thermal performance of the IC is heavily dependent on the layout of the PCB. The user should exercise care during the design phase to ensure the IC will operate within the recommended environmental conditions.

Layout Considerations

The layout is very important for the converter to function properly. Follow these tips for best performance:

1. Separate the Power Ground (⏚) and Signal Ground (⏚); connect them only at one point right at the SGND pin
2. Place the input capacitor(s) as close to V_{IN} and PGND pins as possible
3. Make as small as possible the loop from LX pins to L to C_O to PGND pins
4. Place R_1 and R_2 pins as close to the FB pin as possible
5. Maximize the copper area around the PGND pins; do not place thermal relief around them
6. Thermal pad should be soldered to PCB. Place several via holes under the chip to the ground plane to help heat dissipation

The demo board is a good example of layout based on this outline. Please refer to the EL7554 Application Brief.

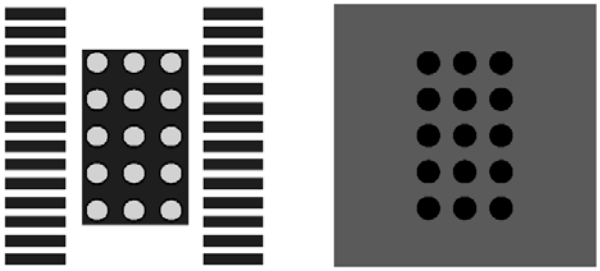
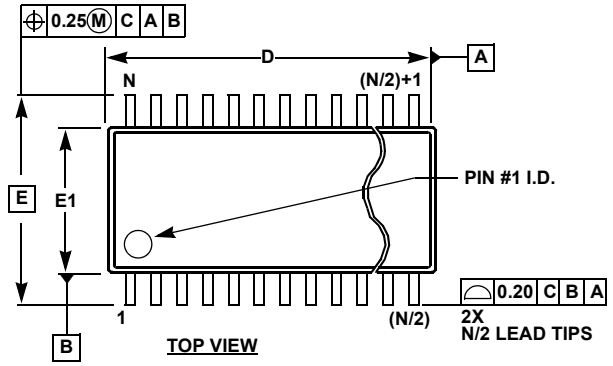
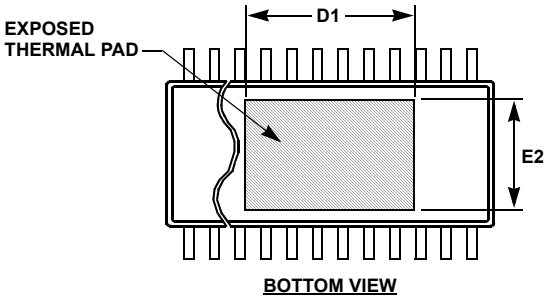
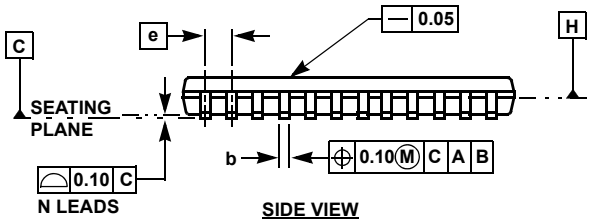


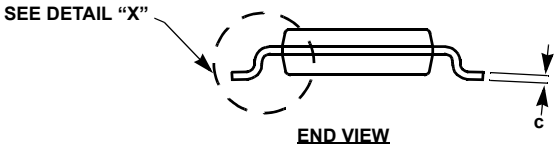
FIGURE 25. PCB LAYOUT - 28 Ld HTSSOP PACKAGE

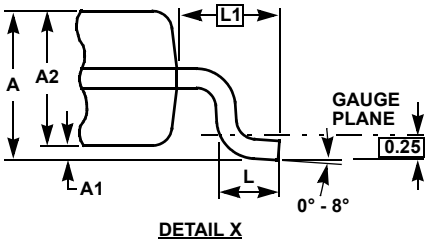
HTSSOP (Heat-Sink TSSOP) Family











MDP0048

HTSSOP (HEAT-SINK TSSOP) FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	20 LD	24 LD	28 LD	38 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.075	0.075	0.075	0.075	0.075	±0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/-0.10
b	0.25	0.25	0.25	0.25	0.22	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	6.50	7.80	9.70	9.70	±0.10
D1	3.2	4.2	4.3	5.0	7.25	Reference
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
E2	3.0	3.0	3.0	3.0	3.0	Reference
e	0.65	0.65	0.65	0.65	0.50	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
N	14	20	24	28	38	Reference

Rev. 3 2/07

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at Datum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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