



THE DATASHEET OF STM32H562ZIT6



Arm[®] Cortex[®]-M33 32-bit MCU +TrustZone[®] + FPU, 375 DMIPS, 250 MHz, 2-Mbyte flash, 640-Kbyte RAM, math accelerators

Datasheet - production data

Features

Includes ST state-of-the-art patented technology

Core

- Arm[®] Cortex[®]-M33 CPU with TrustZone[®], FPU, frequency up to 250 MHz, MPU, 375 DMIPS (Dhrystone 2.1)

ART Accelerator

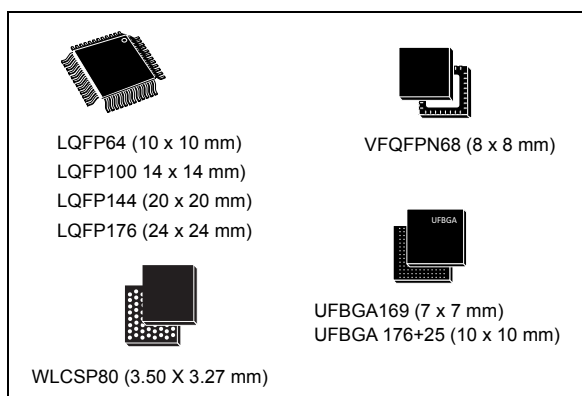
- 8-Kbyte instruction cache allowing 0-wait-state execution from flash and external memories
- 4-Kbyte data cache for external memories

Benchmarks

- 1.5 DMIPS/MHz (Dhrystone 2.1)
- 1023 CoreMark[®] (4.092 CoreMark[®]/MHz)

Memories

- Up to 2 Mbytes of embedded flash memory with ECC, two banks read-while-write
- Up to 48-Kbyte per bank with high-cycling capability (100 K cycles) for data flash
- 2-Kbyte OTP (one-time programmable)
- 640 Kbytes of SRAM (64-Kbyte SRAM2 with ECC and 320-Kbyte SRAM3 with flexible ECC)
- 4 Kbytes of backup SRAM available in the lowest power modes
- Flexible external memory controller with up to 16-bit data bus: SRAM, PSRAM, FRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- One Octo-SPI memory interface with support for serial PSRAM/NAND/NOR, hyper RAM/flash frame formats
- Two SD/SDIO/MMC interfaces



Clock management

- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- External oscillators: 4-50 MHz HSE, 32.768 kHz LSE

General-purpose inputs/outputs

- Up to 140 fast I/Os with interrupt capability (most 5 V tolerant)
- Up to ten I/Os with independent supply down to 1.08 V

Low-power consumption

- Sleep, Stop, and Standby modes
- V_{BAT} supply for RTC, 32 backup registers (32-bit)

Security

- Arm[®] TrustZone[®] with Armv8-M mainline security extension
- Up to eight configurable SAU regions
- TrustZone[®] aware and securable peripherals
- Flexible life cycle scheme with secure debug authentication
- SFI (secure firmware installation)
- Secure firmware upgrade support with TF-M

- HASH hardware accelerator
- ECDSA signature verification
- True random number generator, NIST SP800-90B compliant
- 96-bit unique ID
- Active tampers

Two DMA controllers to offload the CPU

- Two dual-port DMAs with FIFO

Mathematical acceleration

- CORDIC for trigonometric functions acceleration
- FMAC (filter mathematical accelerator)

Reset and supply management

- 1.71 V to 3.6 V application supply and I/O
- POR, PDR, PVD, and BOR
- Embedded regulator (LDO) or SMPS step-down converter regulator with configurable scalable output to supply the digital circuitry

Up to 24 timers

- 18 16-bit (including six low-power 16-bit timers available in Stop mode)
- Two 32-bit timers with up to four IC/OC/PWM or pulse counters and quadrature (incremental) encoder input
- Two watchdogs
- Two SysTick timers

Up to 34 communication interfaces

- Up to four I2Cs Fm+ (SMBus/PMBus®)

- One I3C
- Up to 12 U(S)ARTs (ISO7816 interface, LIN, IrDA, modem control) and one LPUART
- Up to six SPIs, including three muxed full-duplex I2S audio class accuracy via internal audio PLL or external clock, and up to five additional SPIs from five USARTs when configured in Synchronous mode (one additional SPI with OctoSPI)
- Two SAIs
- Two FDCANs
- One 8- to 14-bit camera interface
- One 16-bit parallel slave synchronous-interface
- One HDMI-CEC
- One Ethernet MAC interface with DMA controller
- One USB 2.0 full-speed host and device
- One USB Type-C®/USB Power Delivery r3.1

Analog

- Two 12-bit ADCs with up to 5 Msps in 12-bit
- Two 12-bit DACs
- Digital temperature sensor

Debug

- Authenticated debug and flexible device life cycle
- Serial wire-debug (SWD), JTAG, Embedded Trace Macrocell™ (ETM)

ECOPACK2 compliant packages

Table 1. Device summary

Reference	Part numbers
STM32H562xx	STM32H562AG, STM32H562AI, STM32H562IG, STM32H562II, STM32H562RG, STM32H562RI, STM32H562VG, STM32H562VI, STM32H562ZG, STM32H562ZI
STM32H563xx	STM32H563AG, STM32H563AI, STM32H563IG, STM32H563II, STM32H563MI, STM32H563RG, STM32H563RI, STM32H563VG, STM32H563VI, STM32H563ZG, STM32H563ZI

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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32H562xx and STM32H563xx microcontrollers.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32H562xx and STM32H563xx errata sheet.

For information on the Arm^{®(a)} Cortex[®]-M33 core, refer to the Cortex[®]-M33 Technical Reference Manual, available from the www.arm.com website.

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2 Description

The STM32H562xx and STM32H563xx devices are high-performance microcontrollers of the STM32H5 series, based on the high-performance Arm[®] Cortex[®]-M33 32-bit RISC core. They operate at a frequency of up to 250 MHz.

The Cortex[®]-M33 core features a single-precision floating-point unit (FPU), which supports all the Arm[®] single-precision data-processing instructions and all the data types.

The Cortex[®]-M33 core implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (up to 2 Mbytes of dual bank flash memory and 640 Kbytes of SRAM), a flexible external memory controller (FMC) for devices with packages of 100 pins and more, one OCTOSPI memory interface (at least one Quad-SPI available on all packages), and an extensive range of enhanced I/Os and peripherals connected to three APB buses, three AHB buses, and a 32-bit multi-AHB bus matrix.

The devices offer security foundation compliant with the trusted-based security architecture (TBSA) requirements from Arm[®]. They embed the features to implement a secure firmware update. Besides these capabilities, the devices incorporate a secure firmware installation that allows the customer to secure the provisioning of the code during its production. A flexible life cycle is managed thanks to multiple levels of protection and secure debug authentication. Firmware hardware isolation is supported thanks to securable peripherals, memories, and I/Os, and to privilege configuration of peripherals and memories.

The devices feature several protection mechanisms for embedded flash memory and SRAM: readout protection, write protection, secure, and hide protection areas.

Dedicated peripherals reinforce security: an HASH hardware accelerator, and a true random number generator.

The devices offer active tamper detection and protection against transient and environmental perturbation attacks, thanks to several internal monitoring, generating secret data erase in case of attack. This helps to fit the PCI requirements for point of sales applications.

The devices offer two fast 12-bit ADCs, two DAC channels, an internal voltage reference buffer, a low-power RTC, two 32-bit general-purpose timers, two 16-bit PWM timers dedicated to motor control, eight 16-bit general-purpose timers, two 16-bit basic timers, and six 16-bit low-power timers.

The devices also feature standard and advanced communication interfaces, namely: four I²Cs, one I3C, six SPIs, three I2Ss, six USARTs, six UARTs and one low-power UART, two SAIs, one digital camera interface (DCMI), up to two SDMMCs, up to two FDCANs, one USB full-speed, one USB Type-C[®]/USB power delivery controller, an Ethernet interface (available only on STM32H563xx).

The devices operate in the -40 to +85 °C (+130 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply.

A comprehensive set of power-saving modes allow the design of low-power applications.

Independent power supplies are supported: an analog independent supply input for ADC, DACs, a 3.3 V dedicated supply input for USB, and a dedicated supply input for some GPIOs and SDMMC. A VBAT input is available to connect a backup battery, to preserve the RTC functionality, and to backup 32 32-bit registers and a 4-Kbyte SRAM.

The devices offer eight packages, from 64 to 176 pins.

All packages are available with LDO or SMPS supply options for the V_{CORE} (except for LQFP64 and VFQFPN68 packages, not available in SMPS, and WLCSP80, not available in LDO).

Table 2. STM32H56xxx features and peripheral counts

Peripherals		STM32H563R/G	STM32H562R/G	STM32H563MI	STM32H563VI/G	STM32H562VI/G	STM32H563ZI/G	STM32H562ZI/G	STM32H563AI/G	STM32H562AI/G	STM32H563II/G	STM32H562II/G
Flash memory		Up to 2 Mbytes										
SRAM	System	640 (256 + 64 + 320) Kbytes										
	Backup	4 Kbytes										
Flexible memory controller for external memories (FMC)		No	Yes ⁽¹⁾	Yes ⁽²⁾	Yes							
OCTOSPI		1										
Timers	Advanced control	2 (16 bits)										
	General purpose	2 (32 bits) and 8 (16 bits)										
	Basic	2 (16 bits)										
	Low power	6 (16 bits)										
	SysTick timer	2										
	Watchdog timers (independent, window)	2										

Table 2. STM32H56xxx features and peripheral counts (continued)

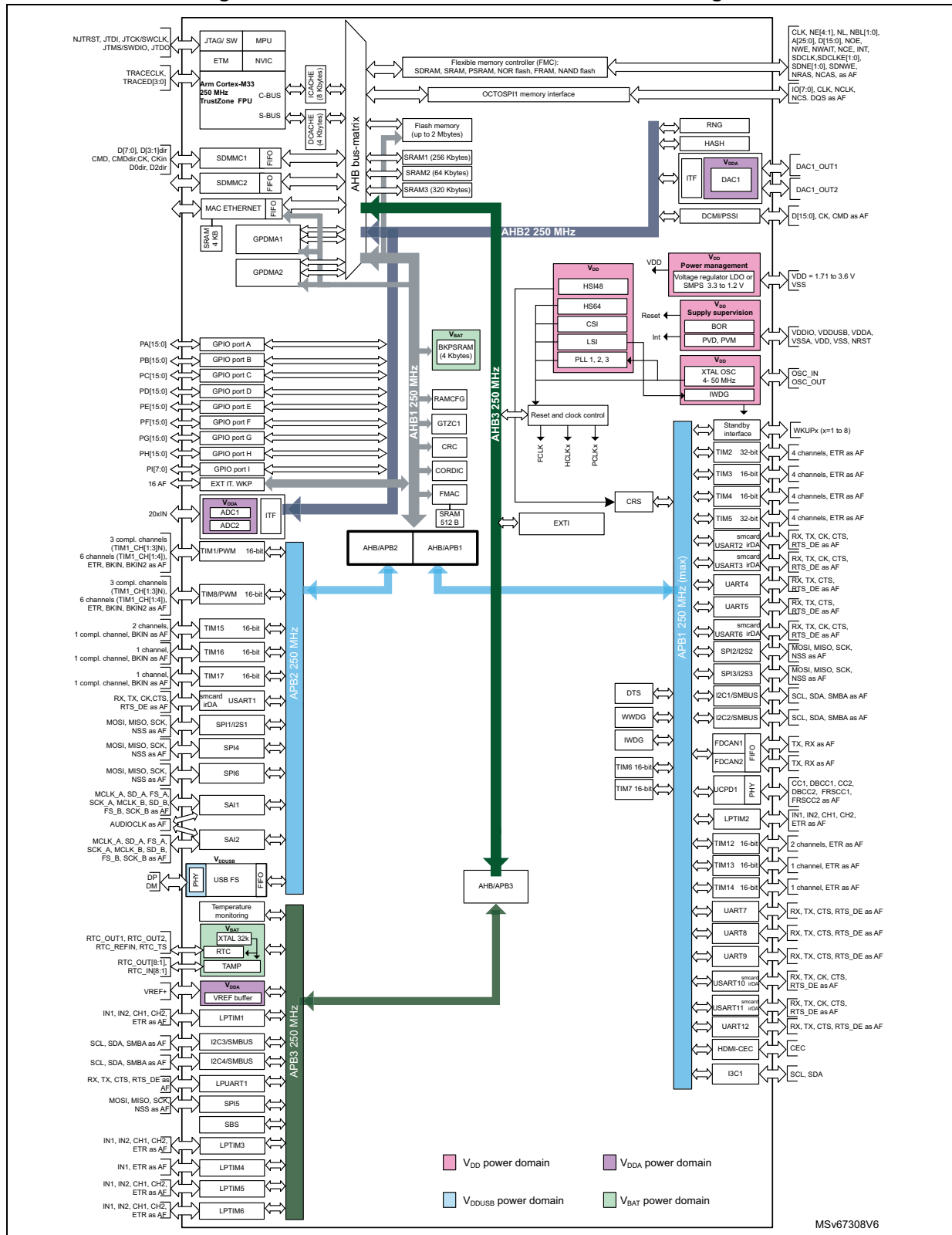
Peripherals		STM32H563R1/G	STM32H562R1/G	STM32H563M1	STM32H563V1/G	STM32H562V1/G	STM32H563Z1/G	STM32H562Z1/G	STM32H563A1/G	STM32H562A1/G	STM32H563I1/G	STM32H562I1/G	
Communication interfaces	SPI / I2S	4/3			5/3			6/3					
	I2C	4											
	I3C	1 ⁽³⁾											
	USART	5			6								
	UART	5			6								
	LPUART	1											
	SAI	2											
	FDCAN	2	1	2	1	2	1	2	1	2	1	2	1
	USB	Yes											
	UCPD	Yes											
	SDMMC	1			2	1	2	1	2	1	2	1	
	Digital camera interface (DCMI)/PSSI ⁽⁴⁾	Yes											
	Ethernet (legacy/SMPS)	Yes/No	No	No/Yes	Yes/No	No	Yes/No	No	Yes/Yes	No	Yes/Yes	No	
	HDMI-CEC	Yes											
CORDIC co-processor		Yes											
Filter mathematical accelerator (FMAC)		Yes											
Real time clock (RTC)		Yes											
Tamper pins (legacy/SMPS)		5/NA	NA/5	8/8									
Active tampers (legacy/SMPS) ⁽⁵⁾		4/NA	NA/4	7/7									
True random number generator		Yes											
HASH (SHA-512)		Yes											
PKA (ECDSA signature verification)		Yes											
GPIOs (legacy/SMPS)		53/NA ⁽⁶⁾	NA/57	80/78	80/NA	112/110	112/NA	136/134	136/eNA	140 ⁽⁷⁾ /139	140 ⁽⁷⁾		
Wakeup pins (legacy/SMPS)		6/NA ⁽⁸⁾	NA/6	7/7	7/NA	7/7	7/NA	8/8	8/NA	8/8	8/NA		
Number of I/Os down to 1.08 V (legacy/SMPS)		0/NA	NA/0	0/0	0/NA	10/10	10/NA	10/7	10/NA	10/7	10/NA		

Table 2. STM32H56xxx features and peripheral counts (continued)

Peripherals		STM32H563RI/G	STM32H562RI/G	STM32H563MI	STM32H563VI/G	STM32H562VI/G	STM32H563ZI/G	STM32H562ZI/G	STM32H563AI/G	STM32H562AI/G	STM32H563II/G	STM32H562II/G
ADC	12-bit ADC	2										
	Number of channels (legacy/SMPS)	16/NA	NA / 16	16 /14	16 /NA	20 /18	20 /NA	20 /20	20/ NA	20 /20	20/ NA	
DAC	12-bit DAC controller	1										
	Number of 12-bit D to A converters	2										
Internal voltage reference buffer		No			Yes							
Maximum CPU frequency		250 MHz										
Operating voltage		1.71 to 3.6 V										
Operating temperature	Ambient	– 40 to 85 °C / – 40 to 125 °C										
	Junction	Voltage range VOS0 (up to 250 MHz): -40 to 105 °C Voltage range VOS1 (up to 200 MHz): -40 to 130 °C										
Package		LQFP64 VFQFPN68	WLCSP80	LQFP100	LQFP144	UFBGA169	LQFP176 UFBGA176					

- 8-bit to interface LCD controller.
- For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
- Shares the I/Os with I2C4.
- DCMI and PSSI cannot be used at the same time, as they share the same circuitry.
- Active tamper in output sharing mode (one output shared by all inputs).
- 49 for LQFP64.
- 136 for LQFP176.
- 5 for VFQFPN68.

Figure 1. STM32H562xx and STM32H563xx block diagram



Note: PC[15:13] are in the V_{BAT} domain.

3 Functional overview

3.1 Arm Cortex-M33 core with TrustZone and FPU

The Cortex-M33 with TrustZone and FPU is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex-M33 processor delivers a high computational performance with low-power consumption and an advanced response to interrupts. It features:

- Arm TrustZone technology, using the Armv8-M main extension supporting secure and non-secure states
- Memory protection units (MPUs), supporting up to 16 regions for secure and non-secure applications
- Configurable secure attribute unit (SAU) supporting up to eight memory regions as secure or non-secure
- Floating-point arithmetic functionality with support for single precision arithmetic

The processor supports a set of DSP instructions that allows an efficient signal processing and a complex algorithm execution.

The Cortex-M33 processor supports the following bus interfaces:

- System AHB bus:
The system AHB (S-AHB) bus interface is used for any instruction fetch and data access to the memory-mapped SRAM, peripheral, external RAM and external device, or Vendor_SYS regions of the Armv8-M memory map.
- Code AHB bus:
The code AHB (C-AHB) bus interface is used for any instruction fetch and data access to the code region of the Armv8-M memory map.

Figure 1 shows the general block diagram of the STM32H562xx and STM32H563xx devices.

3.2 ART Accelerator (ICACHE and DCACHE)

3.2.1 Instruction cache (ICACHE)

The instruction cache (ICACHE) is introduced on C-AHB code bus of Cortex-M33 processor to improve performance when fetching instruction (or data) from both internal and external memories.

ICACHE offers the following features:

- Multi-bus interface:
 - slave port receiving the memory requests from the Cortex-M33 C-AHB code execution port
 - master1 port performing refill requests to internal memories (flash memory and SRAMs)
 - master2 port performing refill requests to external memories (external flash memory and RAMs through Octo-SPI and FMC interfaces)

- a second slave port dedicated to ICACHE registers access
- Close to 0 wait-states instructions/data access performance:
 - 0 wait-states on cache hit
 - hit-under-miss capability, allowing to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
 - critical-word-first refill policy, minimizing processor stalls on cache miss
 - hit ratio improved by two-way set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
 - dual master ports allowing to decouple internal and external memory traffic, respectively, on fast and slow buses, minimizing impact on interrupt latency
 - optimal cache line refill thanks to AHB burst transactions (of the cache line size)
 - performance monitoring by means of a hit counter and a miss counter
- Extension of cacheable region beyond the code memory space, by means of address remapping logic that allows four cacheable external regions to be defined
- Power consumption reduced intrinsically (more accesses to cache memory rather than to bigger main memories); even improved by configuring ICACHE as direct mapped (rather than the default two-way set-associative mode)
- TrustZone security support
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising

3.2.2 Data cache (DCACHE)

The data cache (DCACHE) is introduced on S-AHB system bus of Cortex-M33 processor to improve the performance of data traffic to/from external memories.

DCACHE offers the following features:

- Multi-bus interface:
 - slave port receiving the memory requests from the Cortex-M33 S-AHB system port
 - master port performing refill requests to external memories (external flash memory and RAMs through Octo-SPI and FMC interfaces)
 - a second slave port dedicated to DCACHE registers access
- Close to zero wait-states external data access performance:
 - zero wait-states on cache hit
 - hit-under-miss capability, allowing to serve new processor requests to cached data, while a line refill (due to a previous cache miss) is still ongoing
 - critical-word-first refill policy for read transactions, minimizing processor stalls on cache miss
 - hit ratio improved by two-way set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
 - optimal cache line refill thanks to AHB burst transactions (of the cache line size)
 - performance monitoring by means of two hit counters (for read and write) and two miss counters (for read and write)

- Supported cache accesses:
 - supports both write-back and write-through policies (selectable with AHB bufferable attribute)
 - read and write-back always allocated
 - write-through always non-allocated (write-around)
 - supports byte, half-word and word writes
- TrustZone security support
- Maintenance operations for software management of cache coherency:
 - full cache invalidation (non interruptible)
 - address range clean and/or invalidate operations (background task, interruptible)
- Error management: detection of error for master port request initiated by DCACHE (line eviction or clean operation), with optional interrupt raising

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by other active tasks. This memory area is organized into up to 20 protected areas (12 secure and 8 non-secure). The MPU regions and registers are banked across secure and non-secure states.

The MPU is especially helpful for applications where critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

If a program accesses a memory location prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

3.4 Embedded flash memory

The devices feature up to 2 Mbytes of embedded flash memory for storing programs and data. The flash memory supports a high-cycle data area of up to 100 K cycles.

The flash memory interface features:

- dual-bank operating modes
- read-while-write (RWW)

This allows a read operation to be performed from one bank while an erase or program operation is performed to the other bank. Each bank contains 128 pages of 8 Kbytes.

The flash memory embeds a 2-Kbyte OTP (one-time programmable) for user data, and up to 96 Kbytes supporting high cycling capability (100 K cycles), to use for data (EEPROM emulation).

Option bytes are available to set the flash memory protection mechanisms:

- Different product states for protecting memory content from debug access
- Write protection (WRP) to protect areas against erasing and programming. Two areas per bank can be selected with 8-Kbyte granularity.
- Sector group write-protection (WRPSG), protecting up to 32 groups of four sectors (32 Kbytes) per bank
- Two secure-only areas (one per user flash memory bank). When enabled, this area is accessible only if the STM32 device operates in Secure-access mode
- One HDP area per bank providing temporal isolation for startup code

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single-error detection and correction
- Double-error detection
- ECC fail address report

3.4.1 FLASH security and protections

Sensitive information is stored in the flash memory and it is important to protect the memory against unwanted operations such as reading confidential areas, illegal programming of immutable sectors, or malicious flash memory erasing.

For that purpose the following protection mechanisms are implemented:

- TrustZone backed watermark and block security protection
- Temporal isolation protection (HDP)
- Configuration protection
- User flash memory write protection
- Device non-volatile security life cycle and application boot state management
- OTP locking

Refer to the product reference manual for a detailed description of the security mechanisms.

3.4.2 FLASH privilege protection

Each flash memory sector can be programmed on the fly as privileged or unprivileged.

3.5 Embedded SRAMs

Four SRAMs are embedded in the STM32H562xx and STM32H563xx devices, each with specific features. SRAM1, SRAM2, and SRAM3 are the main SRAMs.

These SRAMs are made of several blocks that can be powered down in Stop mode to reduce consumption:

- SRAM1: 256 Kbytes
- SRAM2: 64 Kbytes with ECC
- SRAM3: 320 Kbytes with optional ECC. When ECC is enabled, 64 bytes are reserved for ECC
- BKPSRAM (backup SRAM): 4 Kbytes with optional ECC. The BKPSRAM can be retained in all low-power modes and when V_{DD} is off in VBAT mode.

Note: The ECC is supported by SRAM2, SRAM3, and BKPSRAM when enabled with the SRAM2_ECC, SRAM3_ECC, and BKPRAM_ECC user option bits.

3.5.1 SRAMs TrustZone security

When the TrustZone security is enabled, all SRAMs are secure after reset. The SRAM1, SRAM2, SRAM3, can be programmed as secure or non-secure by blocks, using the MPCBB (block-based memory protection controller).

The granularity of SRAM secure block based is a page of 512 bytes. Backup SRAM regions can be programmed as secure or non-secure with watermark, using the TZSC (TrustZone security controller) in the GTZC (global TrustZone controller).

3.5.2 SRAMs privilege protection

The SRAM1, SRAM2, SRAM3, can be programmed as privileged or non-privileged by blocks, using the MPCBB. The granularity of SRAM privilege block based is a page of 512 bytes. Backup SRAM regions can be programmed as privileged or non-privileged with watermark, using the TZSC (TrustZone security controller) in the GTZC (global TrustZone controller).

3.6 Security overview

The STM32H562xx and STM32H563xx security enables the possibility to reopen the debug mode even if the product is in secure state.

The reopening of the debug mode is controlled with a debug authentication procedure which permits the authentication of the host.

The sensible assets such as keys or secret codes must be protected when opening the debug mode. The protection is made via code protection and hardware keys storage solutions where all *root of trust* can be protected thanks to hardware mechanisms.

In cases where sensitive information cannot be protected, a partial or a full regression can be launched to start a debug. Regressions are enabled by a debug authentication method.

The STM32H562xx and STM32H563xx allow the developers to introduce their own root of trust solution (OEM-iROT), including their installation in a non-trusted environment, thanks to a secure firmware install (SFI) solution.

The STM32H562xx and STM32H563xx boot stages are isolated via a hardware mechanism called HDPL (temporal isolation level). The HDPL guarantees isolation of the different boot stages: ST assets, iROT (immutable root of trust), uROT (updatable root of trust), secure operating system and non-secure applications.

The devices embed a hardware key storage solution with a dedicated flash memory area per boot stages with access-control based on HDPL, which can be secure or non-secure.

STM32H562xx and STM32H563xx devices are powered by an Arm Cortex-M33 core, associated with all the TrustZone isolation infrastructure. This design permits to benefit from a run time isolation to run secure applications.

3.7 Boot modes

At startup, a BOOT0 pin and NSBOOTADD[31:8]/SECBOOTADD[31:8] option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory
 - Bootloader
 - ST immutable root of trust (ST-iROT)
 - Root security service (RSS)
 - Debug authentication library (RSS-DA)

Embedded bootloader

The embedded bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the flash memory by using USART, I2C, I3C, SPI, FDCAN, or USB_FS in device mode through the DFU (device firmware upgrade).

Refer to AN2606 *STM32 microcontroller system memory boot mode*.

Embedded root security services (RSS)

The embedded RSS are located in the secure information block, programmed by ST during production.

Refer to AN4992 *Overview secure firmware install (SFI)*.

Embedded immutable root of trust (ST-iROT)

The embedded ST-iROT in the system memory, programmed by ST during production. ST-iROT is the immutable root of trust managing the secure boot and secure install of the first updatable level to execute in a boot sequence.

Embedded debug authentication (ST-DA)

The embedded ST-DA in the system memory is programmed by ST during production. ST-DA is the library that manages the debug authentication protocol, making it possible to securely reopen the debug or to launch regressions on secured products in the field.

3.7.1 STM32H562/H563xx boot modes

[Table 3](#) and [Table 4](#), respectively, provide the detail of the boot mode when TrustZone is disabled (TZEN = 0xC3) and enabled (TZEN = 0xB4).

Table 3. STM32H562/H563 boot mode when TrustZone is disabled (TZEN = 0xC3)

PRODUCT_STATE	BOOT0 pin	Boot address option byte selection	Boot area	ST programmed default value
Open	0	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
-	1	NA	Bootloader	Bootloader
Provisioning	x	NA	RSS	RSS

Table 3. STM32H562/H563 boot mode when TrustZone is disabled (TZEN = 0xC3) (continued)

PRODUCT_STATE	BOOT0 pin	Boot address option byte selection	Boot area	ST programmed default value
Provisioned, Closed, Locked	x	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

Table 4. STM32H562/H563 boot mode when TrustZone is enabled (TZEN = 0xB4)

PRODUCT_STATE	BOOT0 pin	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000
-	1	NA	Bootloader	Bootloader
Provisioning	x	NA	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	x	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000

When TrustZone is enabled the boot space must be in secure area. SECBOOTADD0[24:0] option bytes are used to select the boot secure memory address. A unique boot entry option can be selected by setting the SECBOOT_LOCK option bit.

3.8 Global TrustZone controller (GTZC)

GTZC is used to configure TrustZone and privileged attributes within the full system.

The GTZC includes three different sub-blocks:

- TZSC: TrustZone security controller**
 This sub-block defines the secure/privilege state of slave/master peripherals. It also controls the non-secure area size for the watermark memory peripheral controller (MPCWM). The TZSC block informs some peripherals (such as RCC or GPIOs) about the secure status of each securable peripheral, by sharing with RCC and I/O logic.
- TZIC: TrustZone illegal access controller**
 This sub-block gathers all security illegal access events in the system and generates a secure interrupt towards NVIC.
- MPCBB: MPCBB: block-based memory protection controller**
 This sub-block controls secure states of all memory blocks (512-byte pages) of the associated SRAM. This peripheral aims at configuring the internal RAM in a TrustZone system product having segmented SRAM with programmable-security and privileged attributes.

The GTZC main features are:

- Three independent 32-bit AHB interfaces for TZSC, TZIC and MPCBB
- MPCBB and TZIC accessible only with secure transactions
 - Enable illegal access events that may trigger a secure interrupt
- Secure and non-secure access supported for privileged/non-privileged part of TZSC
- Set of registers to define product security settings:
 - Secure/privilege regions for external memories
 - Secure/privilege access mode for securable peripherals
 - Secure/privilege access mode for securable legacy masters

3.9 TrustZone security architecture

The security architecture is based on Arm TrustZone with the Armv8-M main extension.

The TrustZone security is activated by the TZEN option bit in the FLASH_OPTR register.

When the TrustZone is enabled, the SAU (security attribution unit) and IDAU (implementation defined attribution unit) define the access permissions based on secure and non-secure state.

- SAU: up to eight SAU configurable regions are available for security attribution.
- IDAU: It provides a first memory partition as non-secure or non-secure callable attributes. It is then combined with the results from the SAU security attribution and the higher security state is selected.

Based on IDAU security attribution, the flash memory, system SRAMs and peripherals memory space is aliased twice for secure and non-secure states. However, the external memories space is not aliased.

3.9.1 TrustZone peripheral classification

When the TrustZone security is active, a peripheral can be either securable or TrustZone-aware type as follows:

- securable: peripheral protected by an AHB/APB firewall gate controlled from TZSC to define security properties
- TrustZone-aware: peripheral connected directly to AHB or APB bus and implementing a specific TrustZone behavior such as a subset of registers being secure

3.9.2 Default TrustZone security state

The default system security state is detailed below:

- CPU:
 - Cortex-M33 is in secure state after reset. The boot address must be in secure address.
- Memory map:
 - SAU is fully secure after reset. Consequently, all memory map is fully secure. Up to eight SAU configurable regions are available for security attribution.
- Flash memory:
 - Flash memory security area is defined by watermark user options.

- Flash memory block based area is non-secure after reset.
- SRAMs:
 - All SRAMs are secure after reset. MPCBB (memory protection block based controller) is secure.
- External memories:
 - FMC, OCTOSPI banks are secure after reset. MPCWMx (memory protection watermark based controller) is secure.
- Peripherals
 - Securable peripherals are non-secure after reset.
 - TrustZone-aware peripherals are non-secure after reset. Their secure configuration registers are secure.
- All GPIOs are secure after reset.
- Interrupts:
 - NVIC: All interrupts are secure after reset. NVIC is banked for secure and non-secure state.
- TZIC: All illegal access interrupts are disabled after reset.

3.10 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
 - Core domain (V_{CORE})
 - V_{DD} domain
 - Backup domain (V_{BAT})
 - Analog domain (V_{DDA})
 - SMPS power stage (V_{DDSMPS} , available only on SMPS packages)
 - V_{DDIO2} domain
 - V_{DDUSB} for USB transceiver
- System supply voltage regulation
 - SMPS step down converter
 - Voltage regulator (LDO)
- Power supply supervision
 - POR/PDR monitor
 - BOR monitor
 - PVD monitor
- Power management
 - Operating modes
 - Voltage scaling control
 - Low-power modes
- VBAT battery charging
- TrustZone security and privileged protection

3.10.1 Power supply schemes

The devices require a 1.71 to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- $V_{DD} = 1.71 \text{ V to } 3.6 \text{ V}$
 V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- $V_{DDA} = 1.62 \text{ V (ADCs), } 1.8 \text{ V (DACs), or } 2.1 \text{ V (VREFBUF) to } 3.6 \text{ V}$
 V_{DDA} is the external analog power supply for ADCs, DACs and voltage reference buffer. This voltage level is independent from V_{DD} , and must preferably be connected to V_{DD} when these peripherals are not used.
- $V_{DDSMPS} = 1.71 \text{ V to } 3.6 \text{ V}$
 V_{DDSMPS} is the external power supply for the SMPS step down converter. It is provided externally through VDDSMPS supply pin and must be connected to the same supply than VDD.
- V_{LXSMPS} is the switched SMPS step down converter output. The SMPS power supply pins are available only on packages with SMPS step down converter option.
- $V_{DDUSB} = 3.0 \text{ V to } 3.6 \text{ V}$
 V_{DDUSB} is the external independent power supply for USB transceivers. It is independent from V_{DD} , and must preferably be connected to VDD when the USB is not used.
- $V_{DDIO2} = 1.08 \text{ V to } 3.6 \text{ V}$
 V_{DDIO2} is the external power supply for 10 I/Os (PD6, PD7, PG9:14, PB8, PB9). This voltage level is independent from V_{DD} , voltage and must preferably be connected to VDD when those pins are not used.
- $V_{BAT} = 1.2 \text{ V to } 3.6 \text{ V}$
 V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{REF-}, V_{REF+}
 V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.
 V_{REF+} can be grounded when ADC and DAC are not active.
 V_{REF-} and V_{REF+} pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.
When the V_{REF+} is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disabled.
 V_{REF-} must always be equal to V_{SSA} .

Depending upon the package, the devices embed an LDO and/or an SMPS regulator, to provide the V_{CORE} supply for digital peripherals, SRAM1, SRAM2, SRAM3 and embedded flash memory. The SMPS generates this voltage on VCAP (two pins), with a total external capacitor of 10 μF (typical). The SMPS requires an external coil. The LDO generates this voltage on VCAP pin connected to an external capacitor of 2x 2.2 μF (typical).

Both regulators can provide four different voltages (voltage scaling), and can operate in Stop modes.

Figure 2. STM32H562xx and STM32H563xx power supply overview (with SMPS)

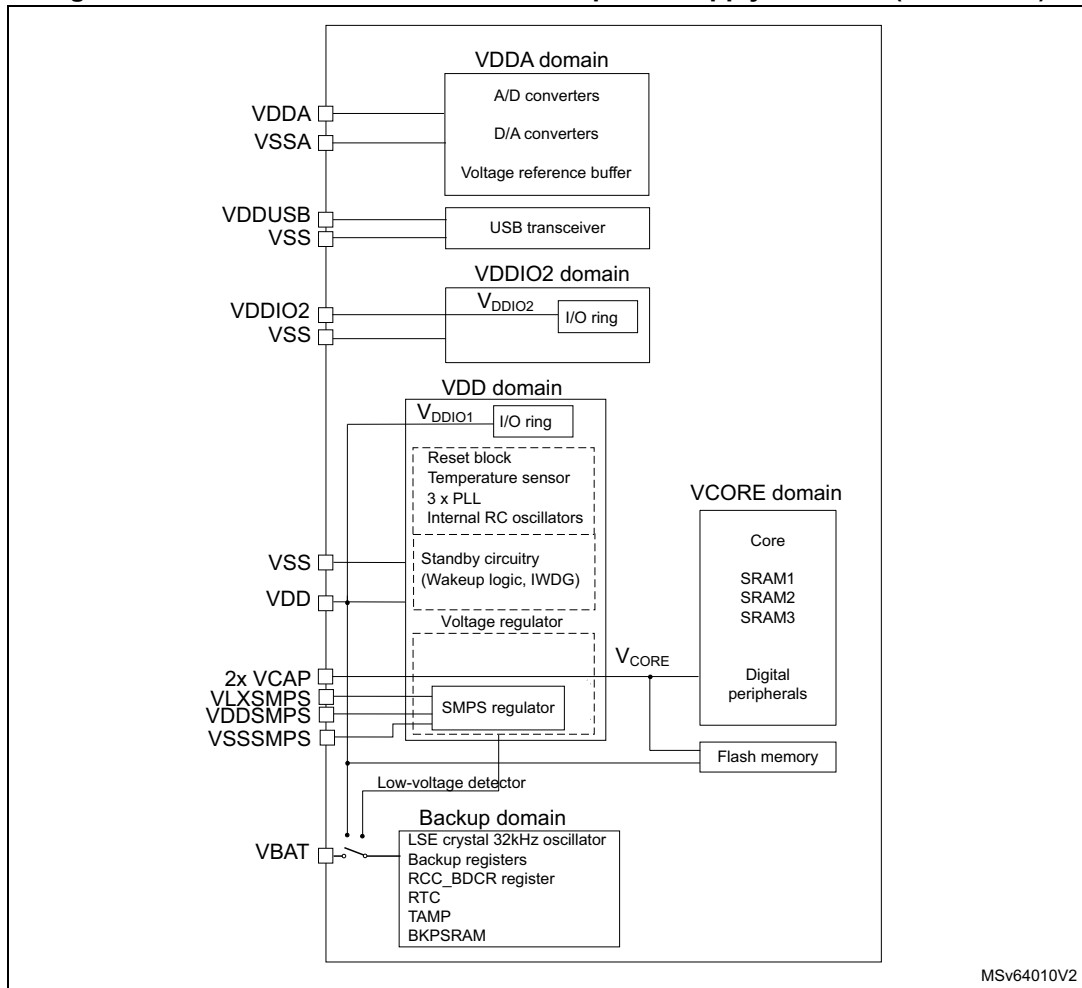
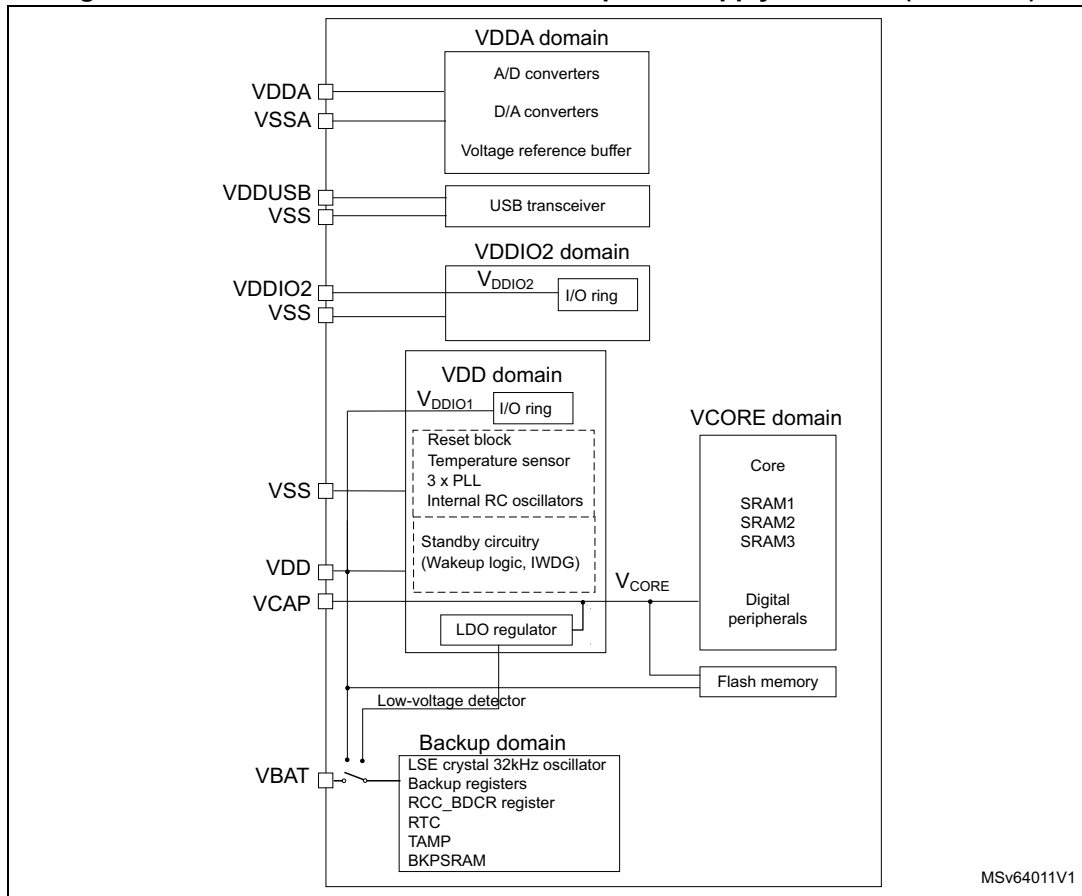


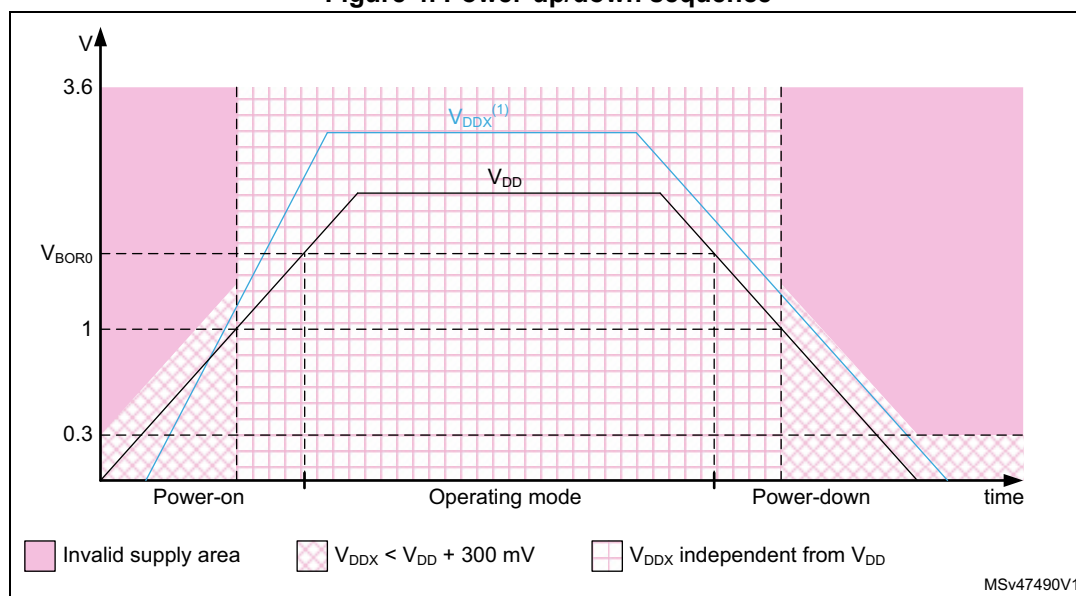
Figure 3. STM32H562xx and STM32H563xx power supply overview (with LDO)



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA} , V_{DDIO2} , V_{DDUSB}) must remain below $V_{DD} + 300$ mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 4. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA} , V_{DDUSB} , and V_{DDIO2} .

3.10.2 Power supply supervisor

The devices have an integrated ultra-low-power brownout reset (BOR) active in all modes; The BOR ensures proper operation of the devices after power on and during power down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes. The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold.

An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor that compares the independent supply voltages V_{DDA} , V_{DDUSB} and V_{DDIO2} to ensure that the peripheral is in its functional supply range.

The devices support dynamic voltage scaling to optimize power consumption in Run mode. The voltage from the main regulator that supplies the logic (V_{CORE}) can be adjusted according to the system maximum operating frequency.

The main regulator operates in the following ranges:

- VOS0 ($V_{CORE} = 1.35$ V) with CPU and peripherals running at up to 250 MHz
- VOS1 ($V_{CORE} = 1.2$ V) with CPU and peripherals running at up to 200 MHz
- VOS2 ($V_{CORE} = 1.1$ V) with CPU and peripherals running at up to 150 MHz
- VOS3 ($V_{CORE} = 1.0$ V) with CPU and peripherals running at up to 100 MHz

Low-power modes

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**

Only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**

This mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the V_{CORE} domain are stopped, the PLL, the CSI, the HSI, the HSI48, and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

The system clock when exiting from Stop mode can be either HSI up to 64 MHz, or CSI (4 MHz), depending on software configuration.
- **Standby mode**

This mode is used to achieve the lowest power consumption with BOR. The PLL, the HSI, the CSI, the HSI48, and the HSE crystal oscillators are also switched off.

The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

The BOR always remains active.

The I/Os state during Standby mode can be retained.

After entering Standby mode, SRAMs and register contents are lost, except for registers and backup SRAM in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a WKUP pin event (configurable rising or falling edge), an RTC event (alarm, periodic wake-up, timestamp), or a tamper detection occurs. The tamper detection can be due to external pins or to an internal failure detection.

The system clock after wake-up is HSI at 32 MHz.

3.10.3 Reset mode

To improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is disabled).

3.10.4 VBAT operation

The VBAT pin allows the device VBAT domain to be powered from an external battery or by an external super-capacitor.

The VBAT pin supplies the RTC with LSE, anti-tamper detection (TAMP), backup registers, and 4-Kbyte backup SRAM. Eight anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from V_{BAT} , neither external interrupts nor RTC alarm/events exit the microcontroller from the VBAT operation.

3.10.5 PWR TrustZone security

When the TrustZone security is activated by the TZEN option bit, the PWR is switched in TrustZone security mode.

The PWR TrustZone security secures the following configuration:

- Low-power mode
- Wake-up (WKUP) pins
- Voltage detection and monitoring
- VBAT mode

Some of the PWR configuration bits security are defined by the security of other peripherals:

- The voltage scaling (VOS) configuration is secure when the system clock selection is secure in RCC.
- The I/O pull-up/pull-down in Standby mode configuration is secure when the corresponding GPIO is secure.
- The backup domain write protection is secure when the RTC is secure.

3.11 Peripheral interconnect matrix

Several peripherals have direct connections between them, for autonomous communication, and to support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run and Sleep modes.

3.12 Reset and clock controller (RCC)

The clock controller distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Clock security system:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals, or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
 - 4 to 50 MHz high-speed external crystal or ceramic resonator (HSE), can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
 - 64 MHz high-speed internal RC oscillator (HSI), trimmable by software, can supply a PLL.
 - 4 MHz low-power internal oscillator (CSI), trimmable by software, can supply a PLL.
 - System PLL, which can be fed by HSE, HSI, or CSI, with a maximum frequency at 250 MHz.

- **RC48 with clock recovery system (HSI48):** internal 48 MHz clock source (HSI48), can be used to drive the USB.
- **UCPD kernel clock,** derived from HSI clock. The HSI RC oscillator must be enabled prior to the UCPD kernel clock use.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
 - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog.
- **Peripheral clock sources:** several peripherals have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, USB, SDMMC, RNG, FDCAN1, OCTOSPI, and the two SAIs.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 32 MHz clock (HSI/2). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock automatically switches to HSI and a software interrupt is generated if enabled. LSE failure can also be detected and generates an interrupt.
- Clock-out capability:
 - **MCO (microcontroller clock output):** it outputs one of the internal clocks for external use by the application.
 - **LSCO (low-speed clock output):** it outputs LSI or LSE in all low-power modes (except VBAT mode).

Several prescalers allow AHB and APB frequencies configuration. The maximum frequency of the AHB and the APB clock domains is 250 MHz.

3.12.1 RCC TrustZone security

When the TrustZone security is activated by the TZEN option bit, the RCC is switched in TrustZone security mode.

The RCC TrustZone security secures some RCC system configuration and peripheral configuration clock from being read or modified by non-secure accesses: when a peripheral is secure, the related peripheral clock, reset, clock source selection and clock enable during low-power modes control bits are secure.

A peripheral is in secure state:

- when its corresponding SEC security bit is set in the TZSC (TrustZone security controller), for securable peripherals.
- when a security feature of this peripheral is enabled through its dedicated bits, for TrustZone-aware peripherals.

3.13 Clock recovery system (CRS)

The devices embed a special block that allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. The trimming is based on the external synchronization signal, derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin, or generated

by user software. For faster lock-in during startup, automatic and manual trimming actions can be combined.

3.14 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

If needed, the I/Os alternate function configuration can be locked following a specific sequence, to avoid spurious writing to the I/Os registers.

Ten I/Os (PD6, PD7, PG9:14, PB8, PB9) can be independently supplied by a dedicated V_{DDIO} supply.

3.14.1 GPIOs TrustZone security

Each I/O pin of GPIO port can be individually configured as secure. When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, I/O data are secure against a non-secure access. The associated registers bit access is restricted to a secure software only. After reset, all GPIO ports are secure.

3.15 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all the masters (CPU, GPDMA1, GPDMA2, SDMMC1, SDMMC2, Ethernet) and the slaves (flash memory, FMC, OCTOSPI, SRAMs, AHB and APB) peripherals. It ensures seamless and efficient operation, even when several high-speed peripherals work simultaneously.

3.16 General purpose direct memory access controller (GPDMA)

The GPDMA controller is a bus master and system peripheral. It used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU. The GPDMA main features are:

- Dual bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
 - Peripheral-to-memory
 - Memory-to-peripheral
 - Memory-to-memory
 - Peripheral-to-peripheral
- Autonomous data transfers during Sleep mode
- Transfers arbitration based on a four-grade programmed priority at a channel level:
 - One high-priority traffic class, for time-sensitive channels (queue 3)
 - Three low-priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)

- Per channel event generation, on any of the following events: transfer complete or half transfer complete or data transfer error or user setting error, and/or update linked-list item error or completed suspension
- Per channel interrupt generation, with separately programmed interrupt enable per event
- Eight concurrent DMA channels:
 - Per channel FIFO for queuing source and destination transfers
 - Intra-channel DMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
 - Intra-channel and inter-channel DMA transfers chaining via programmable DMA input triggers connection to DMA task completion events
- Per linked-list item within a channel:
 - Separately programmed source and destination transfers
 - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
 - Programmable number of data bytes to be transferred from the source, defining the block level
 - 12 channels with linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
 - Four channels with 2D source and destination addressing: programmable signed address offsets between successive burst transfers (non-contiguous addressing within a block, combined with programmable signed address offsets between successive blocks, at a second 2D/repeated block level)
 - Support for scatter-gather (multi-buffer transfers), data interleaving and de-interleaving via 2D addressing
 - Programmable DMA request and trigger selection
 - Programmable DMA half-transfer and transfer complete events generation
 - Pointer to the next linked-list item and its data structure in memory, with automatic update of the DMA linked-list control registers
- Debug:
 - Channel suspend and resume support
 - Channel status reporting including FIFO level and event flags
- TrustZone support:
 - Support for secure and non-secure DMA transfers, independently at a first channel level, and independently at a source/destination and link sub-levels
 - Secure and non-secure interrupts reporting, resulting from any of the respectively secure and non-secure channels
 - TrustZone-aware AHB slave port, protecting any DMA secure resource (register, register field) from a non-secure access
- Privileged/unprivileged support:
 - Support for privileged and unprivileged DMA transfers, independently at a channel level
 - Privileged-aware AHB slave port

3.17 Interrupts and events

3.17.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels and to handle up to 125 maskable interrupt channels plus the 16 interrupt lines of the Cortex-M33.

The NVIC benefits are the following:

- closely coupled NVIC giving low-latency interrupt processing
- interrupt entry vector table address passed directly to the core
- early processing of interrupts
- processing of late arriving higher priority interrupts
- support for tail chaining
- processor state automatically saved
- interrupt entry restored on interrupt exit with no instruction overhead
- TrustZone support: NVIC registers banked across secure and non-secure states

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.17.2 Extended interrupt/event controller (EXTI)

The extended interrupts and event controller (EXTI) manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run modes. The EXTI also includes the EXTI multiplexer IO port selection.

The EXTI main features are the following:

- All event inputs allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
 - Selectable active trigger edge
 - Interrupt pending status register bit independent for the rising and falling edge
 - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt and event generation
 - Software trigger possibility
- TrustZone secure events
 - The access to control and configuration bits of secure input events can be made secure
- EXTI IO port selection

3.18 Cyclic redundancy check calculation unit (CRC)

The CRC is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and that can be stored at a given memory location.

3.19 CORDIC co-processor (CORDIC)

The CORDIC co-processor provides hardware acceleration of certain mathematical functions, notably trigonometric, commonly used in motor control, metering, signal processing and many other applications. It speeds up the calculation of these functions compared to a software implementation, allowing a lower operating frequency, or freeing up processor cycles in order to perform other tasks.

The CORDIC main features are:

- 24-bit CORDIC rotation engine
- Circular and hyperbolic modes
- Rotation and vectoring modes
- Functions: sine, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, natural logarithm
- Programmable precision
- Low-latency AHB slave interface
- Results can be read as soon as ready without polling or interrupt
- DMA read and write channels
- Multiple register read/write by DMA

3.20 Filter math accelerator (FMAC)

The FMAC performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic that allows it to index vector elements held in local memory.

The unit includes support for circular buffers on input and output, which allows digital filters to be implemented. Both finite and infinite impulse response filters can be done.

The unit allows frequent or lengthy filtering operations to be offloaded from the CPU, freeing up the processor for other tasks. In many cases it can accelerate such calculations compared to a software implementation, resulting in a speed-up of time critical tasks.

The FMAC main features are:

- 16 x 16-bit multiplier
- 24 + 2-bit accumulator with addition and subtraction
- 16-bit input and output data

- 256 x 16-bit local memory
- Up to three areas can be defined in memory for data buffers (two input, one output), defined by programmable base address pointers and associated size registers
- Input and output buffers can be circular
- Filter functions: FIR, IIR (direct form 1)
- Vector functions: dot product, convolution, correlation
- AHB slave interface
- DMA read and write data channels

3.21 Flexible memory controller (FMC)

The FMC includes three memory controllers:

- NOR/PSRAM memory controller
- NAND memory controller
- SDRAM memory controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
 - Static random access memory (SRAM)
 - NOR flash memory/OneNAND flash memory
 - PSRAM (four memory banks)
 - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
 - Ferroelectric RAM (FRAM)
- Interface with synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) memories
- 8-, 16- bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO

3.21.1 LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel® 8080 and Motorola® 6800 modes, and is flexible enough to adapt to specific LCD interfaces.

This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

3.21.2 FMC TrustZone security

When the TrustZone security is enabled, the whole FMC banks are secure after reset. Non-secure area can be configured using the TZSC MPCWMx controller.

- The FMC NOR/PSRAM bank:
 - Up to two non-secure area can be configured through the TZSC MPCWM2 controller with a 64-Kbyte granularity
- The FMC NAND bank:

- Can be either configured as fully secure or fully non-secure using the TZSC MPCWM3 controller

The FMC registers can be configured as secure through the TZSC controller.

3.22 Octo-SPI interface (OCTOSPI)

The OCTOSPI supports most external serial memories such as serial PSRAMs, serial NAND and serial NOR flash memories, HyperRAMs™ and HyperFlash™ memories, with the following functional modes:

- Indirect mode: all the operations are performed using the OCTOSPI registers.
- Status-polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting.
- Memory-mapped mode: the external memory is memory mapped and is seen by the system as if it were an internal memory supporting read and write operation.

The OCTOSPI supports the following protocols with associated frame formats:

- the standard frame format with the command, address, alternate byte, dummy cycles and data phase
- the HyperBus™ frame format

The OCTOSPI offers the following features:

- Three functional modes: Indirect, Status-polling, and Memory-mapped
- Read and write support in Memory-mapped mode
- Supports for single, dual, quad and octal communication
- Dual-quad mode, where eight bits can be sent/received simultaneously by accessing two quad memories in parallel.
- SDR (single-data rate) and DTR (double-transfer rate) support
- Data strobe support
- Fully programmable opcode
- Fully programmable frame format
- HyperBus support
- Integrated FIFO for reception and transmission
- 8-, 16-, and 32-bit data accesses allowed
- DMA channel for Indirect mode operations
- Interrupt generation on FIFO threshold, timeout, operation complete, and access error

3.22.1 OCTOSPI TrustZone security

When the TrustZone security is enabled, the whole OCTOSPI bank is secure after reset.

Up to two non-secure area can be configured through the TZSC MPCWM1 controller with a granularity of 64 Kbytes.

The OCTOSPI registers can be configured as secure through the TZSC controller.

3.23 Delay block (DLYB)

The delay block (DLYB) is used to generate an output clock dephased from the input clock. The phase of the output clock must be programmed by the user application. The output clock is then used to clock the data received by another peripheral such as an SDMMC or Octo-SPI interface. The delay is voltage and temperature dependent, that may require the application to re-configure and recenter the output clock phase with the received data.

The delay block main features are:

- Input clock frequency ranging from 25 to 250 MHz
- Up to 12 oversampling phases

3.24 Analog-to-digital converter (ADC1 and ADC2)

The devices embed two successive approximation analog-to-digital converters.

Table 5. ADC features

Mode/feature	ADC1	ADC2
Resolution	12 bit	
Maximum sampling speed	5 Msps (12-bit resolution)	
Dual mode operation	X	
Hardware offset calibration	X	
Hardware linearity calibration	-	
Single-end input	X	
Differential input	X	
Injected channel conversion	X	
Oversampling	Up to x256	
Data register	16 bits	
Data register FIFO depth	3 stages	
DMA support	X	
Parallel data output to ADF	-	
Offset compensation	X	
Gain compensation	-	
Number of analog watchdogs	3	
Option register		X

3.24.1 Analog temperature sensor

This sensor generates a voltage (V_{SENSE}) that varies linearly with temperature. It is internally connected to an ADC input channel used to convert the output voltage into a digital value.

The sensor provides good linearity but it must be calibrated to obtain a good accuracy of the temperature measurement. As the offset depends upon process variation, the uncalibrated internal temperature sensor is suitable for applications that detect only temperature changes.

To improve the measurement accuracy, each device is individually factory-calibrated by ST. The calibration data are stored in the system memory area, accessible in read-only mode.

3.24.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. The V_{REFINT} is internally connected to ADC input channel.

The precise voltage of V_{REFINT} is individually measured for each part during manufacturing, and stored in the system memory area. It is accessible in read-only mode.

3.24.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using ADC or input channel. As the V_{BAT} voltage may be higher than the V_{DDA} , and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by four. As a consequence, the converted digital value is a quarter of the V_{BAT} voltage.

3.25 Digital temperature sensor (DTS)

The devices embeds a sensor that converts the temperature into a square wave, whose frequency is proportional to the temperature. The PCLK or the LSE clock can be used as reference clock for the measurements. Use the formula given in the product reference manual to calculate the temperature according to the measured frequency stored in the DTS_DR register.

3.26 Digital to analog converter (DAC)

The DAC module is a 12-bit voltage output digital-to-analog converter. The DAC can be configured in 8- or 12-bit mode, and can be used in conjunction with the DMA controller. In 12-bit mode, the data can be left- or right-aligned.

The DAC features two output channels, each with its own converter. In dual DAC channel mode, conversions can be done independently or simultaneously when both channels are grouped together for synchronous update operations. An input reference pin, V_{REF+} (shared with others analog peripherals), is available for better resolution. An internal reference can also be set on the same input.

The DAC_OUTx pin can be used as general purpose input/output (GPIO) when the DAC output is disconnected from output pad and connected to on chip peripheral. The DAC output buffer can be optionally enabled to allow a high drive output current. An individual calibration can be applied on each DAC output channel. The DAC output channels support a low power mode, the Sample and hold mode.

The digital interface supports the following features:

- One DAC interface, maximum two output channels
- Left or right data alignment in 12-bit mode

- Synchronized update capability
- Noise-wave and triangular-wave generation
- Sawtooth wave generation
- Dual DAC channel for independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- Double data DMA capability to reduce the bus activity
- External triggers for conversion
- DAC output channel buffered/unbuffered modes
- Buffer offset calibration
- Each DAC output can be disconnected from the DAC_OUTx output pin
- DAC output connection to on chip peripherals
- Sample and Hold mode for low-power operation in Stop mode. The DAC voltage can be changed autonomously with the DMA while the device is in Stop mode.
- Voltage reference input

3.27 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer that can be used as reference for ADCs and DACs, and also as reference for external components through the VREF+ pin.

The internal voltage reference buffer supports three voltages: 1.8 V, 2.048 V, and 2.5 V.

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

3.28 Digital camera interface (DCMI)

DCMI is a synchronous parallel interface able to receive a high-speed data flow from an external 8-, 10-, 12- or 14-bit CMOS camera module, supporting YCbCr4:2:2/RGB565 progressive video and compressed data (JPEG) formats. It can be used with black and white cameras, X24 and X5 cameras (it is assumed that all preprocessing such as resizing is performed in the camera module).

Main features:

- 8-, 10-, 12-, or 14-bit parallel interface
- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature
- Support of the following data formats:
 - 8/10/12/14-bit progressive video: monochrome or raw Bayer
 - YCbCr 4:2:2 progressive video
 - RGB 565 progressive video
 - Compressed data: JPEG

3.29 Parallel synchronous slave interface (PSSI)

The PSSI peripheral and the DCMI (digital camera interface) use the same circuitry. As a result, these two peripherals cannot be used at the same time: when using the PSSI, the DCMI registers cannot be accessed, and vice versa. In addition, the PSSI and the DCMI share the same alternate functions and the same interrupt vector.

The PSSI is a generic synchronous 8-/16-bit parallel data input/output slave interface. It enables the transmitter to send a data valid signal that indicates when the data is valid, and the receiver to output a flow control signal that indicates when it is ready to sample the data.

The PSSI peripheral main features are the following:

- Slave mode operation
- 8-bit or 16-bit parallel data input or output
- 4-word (16-byte) FIFO
- Data enable (PSSI_DE) alternate function input and ready (PSSI_RDY) alternate function output

When selected, these inputs can either enable the transmitter to indicate when the data is valid, or allow the receiver to indicate when it is ready to sample the data, or both.

3.30 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a non-deterministic random bit generator (NDRBG).

The true random generator:

- delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage
- can be used as entropy source to construct a non-deterministic random bit generator (NDRBG)
- produces four 32-bit random samples every 412 AHB clock cycles if $f_{\text{AHB}} < 77$ MHz (256 RNG clock cycles otherwise)
- embeds start-up and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration)
- has an AMBA AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored)

3.31 HASH hardware accelerator (HASH)

The HASH is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-224, SHA-256, SHA-512) and the HMAC (keyed-hash message authentication code) algorithm. HMAC is suitable for applications requiring message authentication.

The HASH computes FIPS (Federal information processing standards) approved digests of length of 160, 224, 256, 512 bits, for messages of up to $(2^{64} - 1)$.

The HASH main features are:

- Suitable for data authentication applications, compliant with:
 - Federal Information Processing Standards Publication FIPS PUB 180-4, *Secure Hash Standard* (SHA-1 and SHA-2 family)
 - Federal Information Processing Standards Publication FIPS PUB 186-4, *Digital Signature Standard* (DSS)
 - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, *HMAC: Keyed-Hashing for Message Authentication* and Federal Information Processing Standards Publication FIPS PUB 198-1, *The Keyed-Hash Message Authentication Code* (HMAC)
- Fast computation of SHA-1, SHA-224, SHA-256 and SHA-512
 - 82 (respectively 66) clock cycles for processing one 512-bit block of data using SHA-1 (respectively SHA-256) algorithm
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
 - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit string
 - Word swapping supported: bits, bytes, half-words and 32-bit words
- Automatic padding to complete the input bit string to fit digest minimum block size of 512 bits (16×32 bits)
- Single 32-bit input register associated to an internal input FIFO of sixteen 32-bit words, corresponding to one block size
- AHB slave peripheral, accessible through 32-bit word accesses only (else an AHB error is generated)
- 8×32 -bit words (H0 to H7) for output message digest
- Automatic data flow control with support of direct memory access (DMA) using one channel. Single or fixed burst of 4 supported.
- Interruptible message digest computation, on a per-32-bit word basis
 - Re-loadable digest registers
 - Hashing computation suspend/resume mechanism, including using DMA

3.32 Public key accelerator (PKA)

The PKA can verify ECDSA signatures, with all needed computation performed within the accelerator. The application CPU is needed only to manage the inputs and the outputs of the operation.

The PKA main features are:

- ECDSA signature verification
- Capability to handle operands up to 640 bits
- AMBA AHB slave peripheral, accessible through 32-bit word single accesses only (otherwise an AHB bus error is generated, and write accesses are ignored)

3.33 Timers and watchdogs

The devices include two advanced control timers, up to seven general-purpose timers, two basic timers, six low-power timers, two watchdog timers and two SysTick timers.

Table 6 compares the features of the advanced control, general-purpose and basic timers.

Table 6. Timer features

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16 bits	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM2, TIM5	32 bits				4	No
	TIM3, TIM4	16 bits				4	No
General purpose	TIM12, TIM15	16 bits	Up			2	1
	TIM13, TIM14, TIM16, TIM17					1	1
Basic	TIM6, TIM7	16 bits	Up			0	No

3.33.1 Advanced-control timers (TIM1, TIM8)

These timers can be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 - 100 %)
- One-pulse mode output

In Debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in the next section) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the *Timer Link* feature for synchronization or event chaining.

3.33.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

The devices embed up to seven synchronizable general-purpose timers (see [Table 6](#)), each of them can be used to generate PWM outputs, or act as a simple time base.

- TIM2 and TIM5
Full-featured general-purpose timers with 32-bit auto-reload up/downcounter and 32-bit prescaler.
These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.
The counters can be frozen in Debug mode.
All have independent DMA request generation and support quadrature encoders.
- TIM3 and TIM4
Full-featured general-purpose timers with 16-bit auto-reload up/downcounter and 16-bit prescaler.
These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output.
They can work together, or with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.
The counters can be frozen in Debug mode. All have independent DMA request generation and support quadrature encoders.
- TIM12, TIM13, TIM14, TIM15, TIM16, and TIM17
General-purpose timers with mid-range features.
They have 16-bit auto-reload upcounters and 16-bit prescalers.
 - TIM12 and TIM15 have two channels and one complementary channel
 - TIM13, TIM14, TIM16, and TIM17 have one channel and one complementary channelAll channels can be used for input capture/output compare, PWM or one-pulse mode output.
The timers can work together via the *Timer Link* feature for synchronization or event chaining. The timers have independent DMA request generation.
The counters can be frozen in Debug mode.

3.33.3 Basic timers (TIM6, TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebase.

3.33.4 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5, LPTIM6)

The devices embed six low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wake up the system from Stop mode.

The low-power timers support the following features:

- 16-bit up counter with 16-bit autoreload register

- 3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock
 - Internal clock sources: LSE, LSI, HSI or APB clock
 - External clock source over LPTIM input (working with no LP oscillator running, used by *Pulse Counter* application)
- 16-bit ARR autoreload register
- 16-bit capture/compare register
- Continuous/One-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity
- Encoder mode (except for LPTIM4)
- Repetition counter
- Up to two independent channels (except for LPTIM4) for:
 - Input capture
 - PWM generation (edge-aligned mode)
 - One-pulse mode output
- Interrupt generation on ten events
- DMA request generation on the following events:
 - Update event
 - Input capture

3.33.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and, as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in Debug mode.

3.33.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

3.33.7 SysTick timer

The Cortex-M33 with TrustZone embeds two SysTick timers.

When TrustZone is activated, two SysTick timer are available:

- SysTick, secure instance
- SysTick, non-secure instance

When TrustZone is disabled, only one SysTick timer is available. This timer (secure or non-secure) is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.34 Real-time clock (RTC), tamper and backup registers

3.34.1 Real-time clock (RTC)

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year, in BCD (binary-coded decimal) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period
- TrustZone support:
 - RTC fully securable
 - Alarm A, alarm B, wake-up timer and timestamp individual secure or non-secure configuration
 - Alarm A, alarm B, wake-up timer and timestamp individual privileged protection

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The RTC clock sources can be one of the following:

- 32.768 kHz external crystal (LSE)
- external resonator or oscillator (LSE)
- internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- high-speed external clock (HSE), divided by a prescaler in the RCC.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes.

All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake up the device from the low-power modes.

3.34.2 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks. 32 32-bit backup registers are retained in all low-power modes and in VBAT mode. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with eight tamper pins and nine internal tampers. The external tamper pins can be configured for edge detection, or level detection with or without filtering, or active tamper that increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- A tamper detection can erase the backup registers, backup SRAM, SRAM2, caches and cryptographic peripherals.
- 32 32-bit backup registers:
 - The backup registers (TAMP_BKPxR) are implemented in the Backup domain that remains powered-on by V_{BAT} when the V_{DD} power is switched off.
- Up to 8 tamper pins for 8 external tamper detection events:
 - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks
 - Flexible active tamper I/O management: from 4 meshes (each input associated to its own exclusive output) to 7 meshes (single output shared for up to 7 tamper inputs)
 - Passive tampers: ultra-low power edge or level detection with internal pull-up hardware management
 - Configurable digital filter

Note: As input, only PC13, PI8, PA0, PA1, and PA2 are functional in Standby and VBAT modes. As output, only PC13, PA1, and PI8 are functional in Standby and VBAT modes.

- Internal tamper events to protect against transient or environmental perturbation attacks
- Each tamper can be configured in two modes:
 - Hardware mode: immediate erase of secrets on tamper detection, including backup registers erase
 - Software mode: erase of secrets following a tamper detection launched by software
- Any tamper detection can generate an RTC time stamp event.
- TrustZone support:
 - Tamper secure or non-secure configuration.
 - Backup registers configuration in 3 configurable-size areas:
 - 1 read/write secure area
 - 1 write secure/read non-secure area
 - 1 read/write non-secure area
 - Secret key, stored in backup registers, protected against read and write access
- Tamper configuration and backup registers privilege protection
- Monotonic counter

3.35 Inter-integrated circuit interface (I2C)

The device embeds four I2C. Refer to [Table 7](#) for the implemented features.

The I²C bus interface handles communications between the microcontroller and the serial I²C bus. It controls all I²C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
 - Slave and Master modes, multimaster capability
 - Standard-mode (Sm), with a bit rate up to 100 Kbit/s
 - Fast-mode (Fm), with a bit rate up to 400 Kbit/s
 - Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
 - 7- and 10-bit addressing modes, multiple 7-bit slave addresses
 - Programmable setup and hold times
 - Optional clock stretching
- System management bus (SMBus) specification rev 3.0 compatibility:
 - Hardware PEC (packet error checking) generation and verification with ACK control
 - Address resolution protocol (ARP) support
 - SMBus alert
- Power system management protocol (PMBus) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming
- Wake-up from Stop capability
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 7. I2C implementation

Feature ⁽¹⁾	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 Kbit/s)	X	X	X	X
Fast-mode (up to 400 Kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wake-up capability	X	X	X	X

1. X: supported

3.36 Improved inter-integrated circuit (I3C)

The I3C interface handles communication between the MCU and others, like sensors and host processor(s), all connected on an I3C bus.

The peripheral implements the required features of the MIPI I3C specification v1.1. It can control I3C bus-specific sequencing, protocol, arbitration and timing, and can act as controller (formerly known as master) or as target (formerly known as slave). When acting as controller the peripheral improves the features of the I2C interface, preserving some backward compatibility: it allows an I2C target to operate on an I3C bus in legacy I2C fast-mode (Fm) or legacy I2C fast-mode plus (Fm+), provided that the latter does not perform clock stretching.

The I3C peripheral can be used with DMA to off-load the CPU.

Table 8. I3C peripheral controller/target features versus MIPI v1.1

Feature	MIPI v1.1	When controller	When target	Comments
I3C SDR message	X	X	X	-
Legacy I ² C message (Fm/Fm+)	X	X	-	Mandatory when controller, and the I3C bus is mixed with (external) legacy I ² C target(s). Optional in MIPI v1.1 when target.
HDR DDR message	X	-	-	Optional in MIPI v1.1
HDR-TSL/TSP, HDR-BT	X	-	-	
Dynamic address assignment	X	X	X	-
Static address	X	X	-	No (intended) support of I3C peripheral as a target on an I ² C bus.
Grouped addressing	X	X	-	Optional in MIPI v1.1
CCCs	X	X	X	Mandatory and some optional CCCs supported.
Error detection and recovery	X	X	X	-
In-band interrupt (with MDB)	X	X	X	-
Secondary controller	X	X	X	-
Hot-join mechanism	X	X	X	-
Target reset	X	X	X	-
Synchronous timing control	X	X	-	Optional in MIPI v1.1
Asynchronous timing control 0	X	X	-	
Asynchronous timing control 1, 2, 3	X	-	-	
Device to device tunneling	X	X	-	
Multi-lane data transfer	X	X	-	
Monitoring device early termination	X	-	-	

3.37 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART)

The devices have six embedded universal synchronous receiver transmitters (USART1/USART2/USART3/USART6/USART10/USART11), six universal asynchronous receiver transmitters (UART4/UART5/UART7/UART8/UART9/UART12), and one low-power universal asynchronous receiver transmitter (LPUART1).

Table 9. USART, UART and LPUART features

Mode/feature ⁽¹⁾	USART 1/2/3/6/10/11	UART 4/5/7/8/9/12	LPUART 1
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode (master/slave)	X	-	-
Smartcard mode	X	-	-
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	-
LIN mode	X	X	-
Dual-clock domain and wake-up from Stop mode	X ⁽²⁾	X ⁽²⁾	X ⁽²⁾
Receiver timeout interrupt	X	X	-
Modbus communication	X	X	-
Auto-baud rate detection	X	X	-
Driver enable	X	X	X
USART data length	7, 8, and 9 bits		
Tx/Rx FIFO	X	X	X
Tx/Rx FIFO size	8 bytes		

1. X = supported.

2. Wake-up supported from Stop mode.

3.37.1 Universal synchronous/asynchronous receiver transmitter (USART/UART)

The USART offers a flexible means to perform full-duplex data exchange with external equipments requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The USART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications up to 20 Mbauds are possible by using the DMA (direct memory access) for multibuffer configuration.

The USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or by 8, to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data
Each FIFO can be enabled/disabled by software and come with a status flag.
- A common programmable transmit and receive baud rate
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Auto baud rate detection
- Programmable data word length (7, 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous Master/Slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
 - Transmits parity bit
 - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from stop capability
- LIN master synchronous break send capability and LIN slave break detection capability
 - 13-bit break generation and 10/11 bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16 bit duration for Normal mode
- Smartcard mode
 - Supports the T=0 and T=1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
 - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
 - Timeout feature
 - CR/LF character recognition

3.37.2 Low-power universal asynchronous receiver transmitter (LPUART)

The LPUART supports bidirectional asynchronous serial communication with minimum power consumption. It also supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher-speed clock can be used to reach higher baud-rates.

The LPUART interface can be served by the DMA controller.

The LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 baud/s to 9600 baud/s using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data
Each FIFO can be enabled/disabled by software and come with status flags for FIFOs states.
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
 - Receive buffer full
 - Transmit buffer empty
 - Busy and end of transmission flags
- Parity control:
 - Transmits parity bit
 - Checks parity of received data byte
- Four error detection flags:
 - Overrun error
 - Noise detection
 - Frame error
 - Parity error
- Interrupt sources with flags

- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Wake-up from Stop capability

3.38 Serial peripheral interface (SPI) / inter-integrated sound interfaces (I2S)

The devices embed six serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices.

The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to setup communication with concrete slave and to assure it handles the data flow properly. The Motorola data format is used by default, but some other specific modes are supported as well.

The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4-bit to 32-bit data size selection or fixed to 8-bit and 16-bit only
- Multi master or multi slave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of PCLK
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in Master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO x MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI formats support
- Hardware CRC feature can secure communication at the end of transaction by:
 - Adding CRC value in Tx mode
 - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun at slave, mode fault at master
- Two 16x or 8x 8-bit embedded Rx and Tx FIFOs with DMA capability
- Programmable number of data in transaction
- Configurable FIFO thresholds (data packing)

- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Wake-up from Stop capability
- Optional status pin RDY signaling the slave device ready to handle the data flow.

Three standard I2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in Master or Slave mode, in full-duplex communication modes, and can be configured to operate with configurable resolution as input or output channel.

I2S main features:

- Full duplex communication
- Simplex communication (only transmitter or receiver)
- Master or slave operations
- 8-bit programmable linear prescaler
- Data length may be 16, 24 or 32 bits
- Channel length can be 16 or 32 in master, any value in slave
- Programmable clock polarity
- Error flags signaling for improved reliability: Underrun, Overrun and Frame Error
- Embedded Rx and Tx FIFOs
- Supported I2S protocols:
 - I2S Philips standard
 - MSB-Justified standard (Left-Justified)
 - LSB-Justified standard (Right-Justified)
 - PCM standard (with short and long frame synchronization)
- Data ordering programmable (LSb or MSb first)
- DMA capability for transmission and reception
- Master clock can be output to drive an external audio component. The ratio is fixed at 256 x FWS (where FWS is the audio sampling frequency)

Table 10. SPI features

Feature	SPI1, SPI2, SPI3 (full feature set instances)	SPI4, SPI5, SPI6 (limited feature set instance)
Data size	Configurable from 4 to 32-bit	8/16-bit
CRC computation	CRC polynomial length configurable from 5 to 33-bit	CRC polynomial length configurable from 9 to 17-bit
Size of FIFOs	16x 8-bit	8x 8-bit
Number of transferred data	Unlimited, expandable	Up to 1024, no data counter
I2S feature	Yes	No

3.39 Serial audio interface (SAI)

The devices embed two SAIs. Refer to [Table 11](#) for the features implementation. The SAI bus interface handles communications between the MCU and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks that can be transmitters or receivers with their respective FIFO
- 8-word integrated FIFOs for each audio sub-block
- Synchronous or Asynchronous mode between the audio sub-blocks
- Master or slave configuration independent for both audio sub-blocks
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit
- Peripheral with large configurability and flexibility, allowing to target the following audio protocols: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF out
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame
- Number of bits by frame may be configurable
- Frame synchronization active level configurable (offset, bit length, level)
- First active bit position in the slot is configurable
- LSB first or MSB first for data transfer
- Mute mode
- Stereo/mono audio frame capability
- Communication clock strobing edge configurable (SCK)
- Error flags with associated interrupts if enabled respectively
 - Overrun and underrun detection
 - Anticipated frame synchronization signal detection in Slave mode
 - Late frame synchronization signal detection in Slave mode
 - Codec not ready for the AC'97 mode in reception
- Interruption sources when enabled:
 - Errors
 - FIFO requests
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 11. SAI implementation

Feature ⁽¹⁾	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO size	X (8 words)	X (8 words)
SPDIF	X	X
PDM	X	-

1. X: supported

3.40 Secure digital input/output and MultiMediaCards interface (SDMMC)

The SD/SDIO, embedded MultiMediaCard (eMMC™) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards, and eMMC devices.

The MultiMediaCard system specifications are available through the MultiMediaCard association website at www.mmca.org, published by the MMCA technical committee.

SD memory card and SD I/O card system specifications are available through the SD card Association website at www.sdcard.org.

The SDMMC features include the following:

- Compliance with Embedded MultiMediaCard System Specification Version 5.1
Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit (HS200 SDMMC_CK speed limited to maximum allowed I/O speed) (HS400 is not supported).
- Full compatibility with previous versions of MultiMediaCards (backward compatibility).
- Full compliance with *SD memory card specifications version 6.0*
(SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Full compliance with *SDIO card specification version 4.0*
Card support for two different databus modes: 1-bit (default) and 4-bit (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Data transfer up to 208 Mbyte/s for the 8-bit mode
(Depending maximum allowed I/O speed).
- Data and command output enable signals to control external bidirectional drivers
- IDMA linked list support

The MultiMediaCard/SD bus connects cards to the host.

The current version of the SDMMC supports only one SD/SDIO/eMMC card at any one time and a stack of eMMC.

Table 12. SDMMC features

Mode/feature ⁽¹⁾	SDMMC1	SDMMC2
Variable delay (SDR104, HS200)	X	X
SDMMC_CKIN	X	X
SDMMC_CD _{IR} , SDMMC_D0 _{DIR}	X	-
SDMMC_D123 _{DIR}	X	-

1. X = supported.

When SDMMC peripherals are used simultaneously:

- Only one can be used in eMMC with 8-bit bus width.
- Usage of SDMMC1 SDIO voltage switch use is mutually exclusive with SDMMC2 eMMC with 8-bit bus width.
- If SDMMC1 must support SDIO UHS-I modes (SDR12, SDR25, SDR50, SDR104, or DDR50), then SDMMC2 cannot support eMMC with 8-bit bus width.
- If SDMMC2 must support eMMC with 8-bit bus width, then SDMMC1 can only support SDIO Default mode and High-speed mode.

3.41 Controller area network (FDCAN)

The controller area network (CAN) subsystem consists of one CAN module, a shared message RAM memory and a configuration block.

The modules (FDCAN) are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 0.8-Kbyte message RAM implements filters, receives FIFOs, transmits event FIFOs and transmits FIFOs.

The FDCAN main features are:

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015, -4
- CAN FD with maximum 64 data bytes supported
- CAN error logging
- AUTOSAR and J1939 support
- Improved acceptance filtering
- 2 receive FIFOs of three payloads each (up to 64 bytes per payload)
- Separate signaling on reception of high priority messages
- Configurable transmit FIFO / queue of three payload (up to 64 bytes per payload)
- Configurable transmit Event FIFO
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains: APB bus interface and CAN core kernel clock
- Power-down support

3.42 USB full speed (USB)

USB main features

- USB specification version 2.0 full-speed compliant
- Host and device functions
- 2048 bytes of dedicated SRAM data buffer memory with 32-bit access
- USB clock recovery
- Configurable number of endpoints from 1 to 8
- Cyclic redundancy check (CRC) generation/checking, non-return-to-zero inverted (NRZI) encoding/decoding and bit-stuffing
- Isochronous transfers support

- Double-buffered bulk/isochronous endpoint support
- USB suspend/resume operations
- Frame-locked clock pulse generation
- USB 2.0 Link power management support
- Battery charging specification revision 1.2 support in device

3.43 USB Type-C/USB Power Delivery controller (UCPD)

The device embeds one controller (UCPD) compliant with USB Type-C Cable and Connector Specification release 2.0 and USB Power Delivery Rev. 3.0 specifications.

The controller uses specific I/Os supporting the USB Type-C and USB power delivery requirements, featuring:

- USB Type-C pull-up (R_p , all values) and pull-down (R_d) resistors
- “Dead battery” support
- USB power delivery message transmission and reception
- FRS (fast role swap) support

The digital controller handles notably:

- USB Type-C level detection with debounce, generating interrupts
- FRS detection, generating an interrupt
- Byte-level interface for USB power delivery payload, generating interrupts (DMA compatible)
- USB power delivery timing dividers (including a clock pre-scaler)
- CRC generation/checking
- 4b5b encode/decode
- Ordered sets (with a programmable ordered set mask at receive)
- Frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB power delivery messages and FRS signaling.

3.44 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for Ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Support of 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation

- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal 2-Kbyte FIFOs to buffer transmit and receive frames
- Support of hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Trigger of interrupt when system time becomes greater than target time

3.45 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The devices embed a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wake up the MCU from Stop mode on data reception.

3.46 Development support

3.46.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.46.2 Embedded Trace Macrocell

The Arm Embedded Trace Macrocell (ETM) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

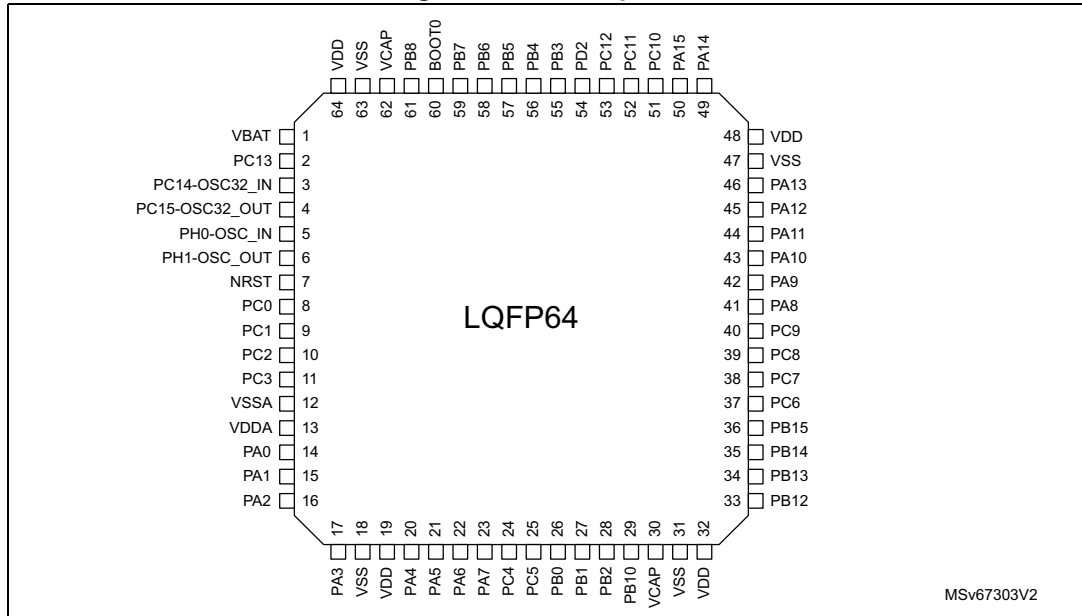
Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The ETM operates with third party debugger software tools.

4 Pinout, pin description and alternate function

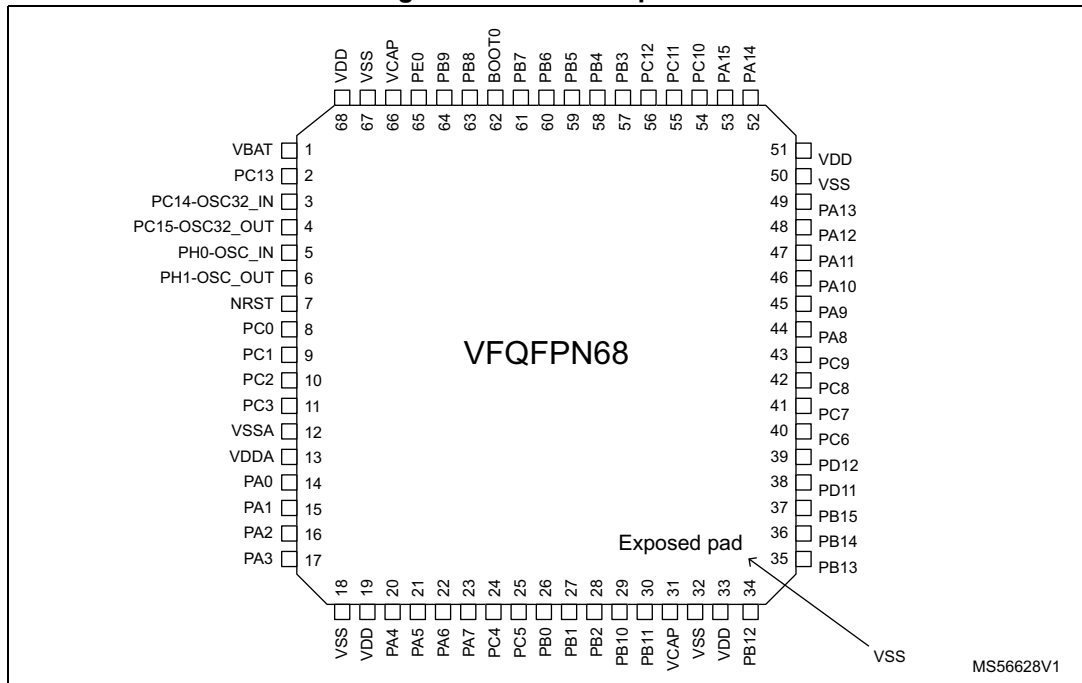
4.1 Pinout/ballout schematics

Figure 5. LQFP64 pinout



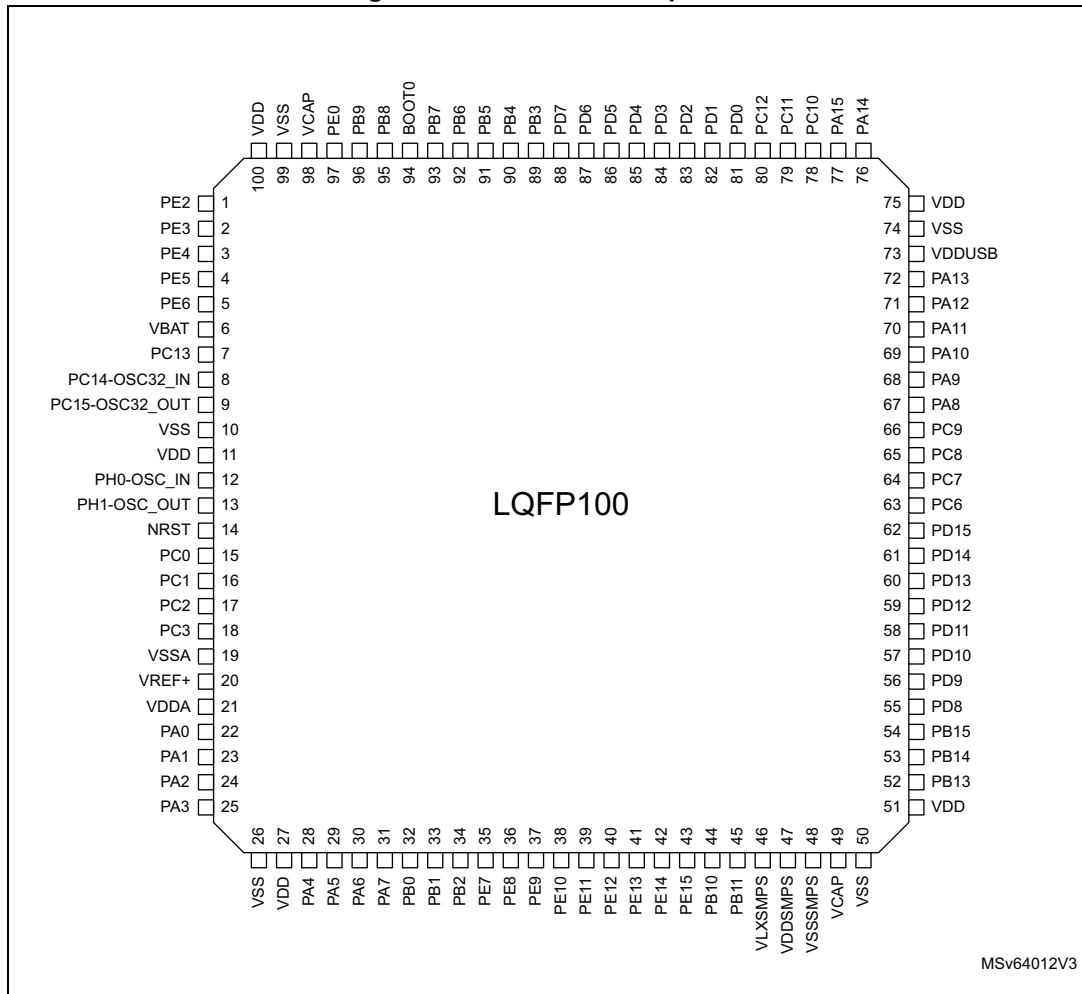
1. The above figure shows the package top view.

Figure 6. VFQFPN68 pinout



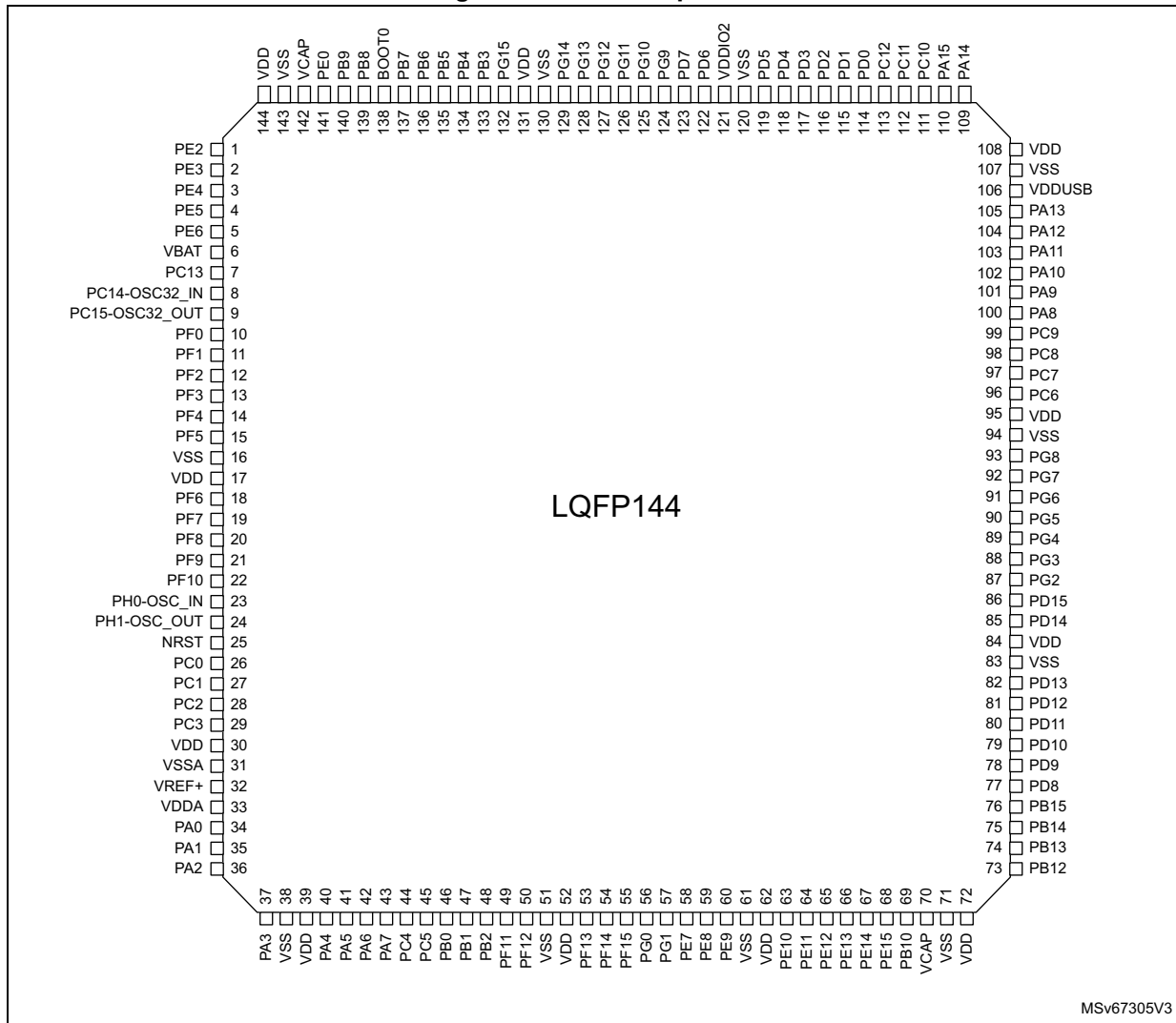
1. The above figure shows the package top view.
2. VSS pads are connected to the exposed pad.

Figure 9. LQFP100 SMPS pinout



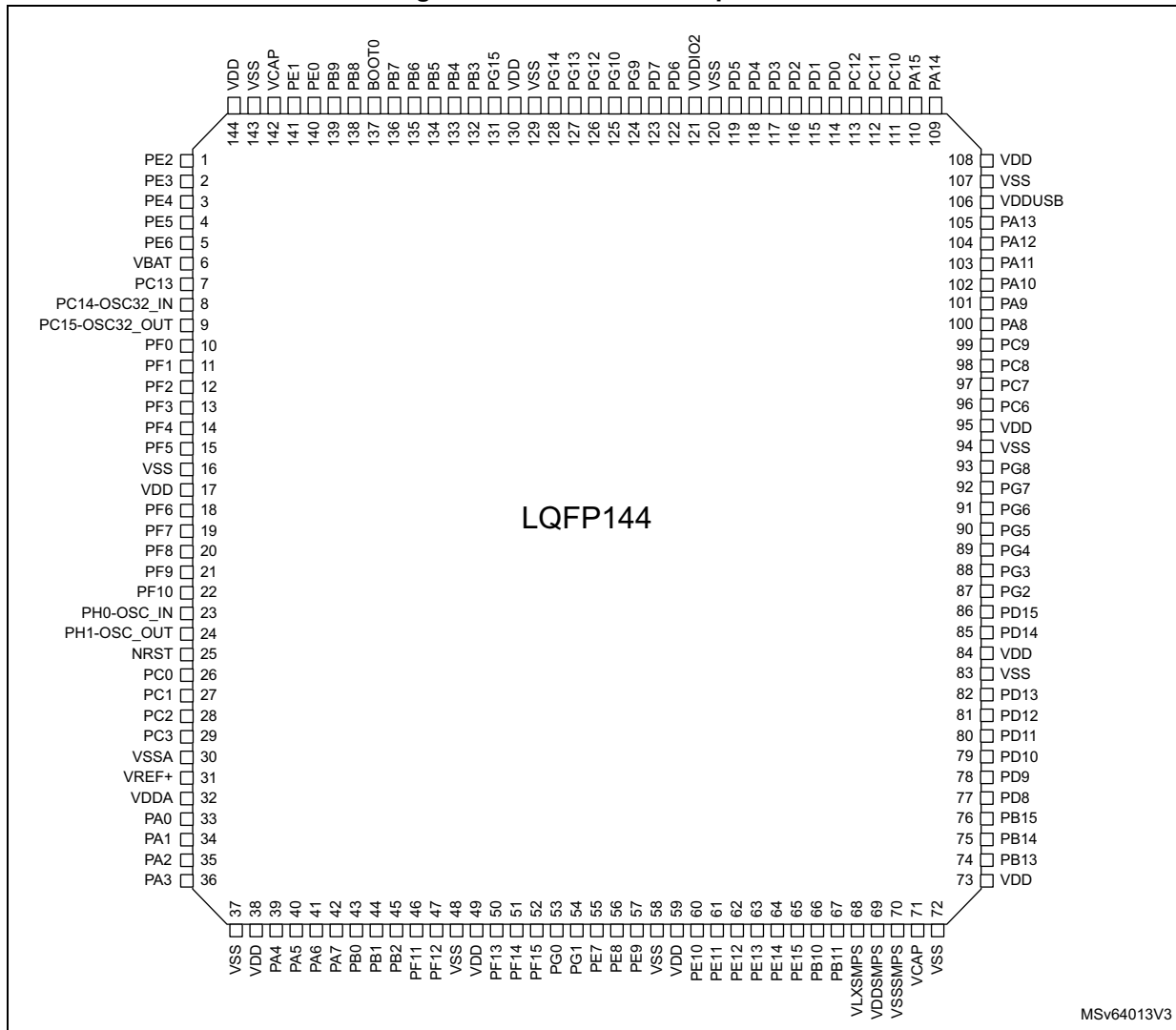
1. The above figure shows the package top view.

Figure 10. LQFP144 pinout



1. The above figure shows the package top view.

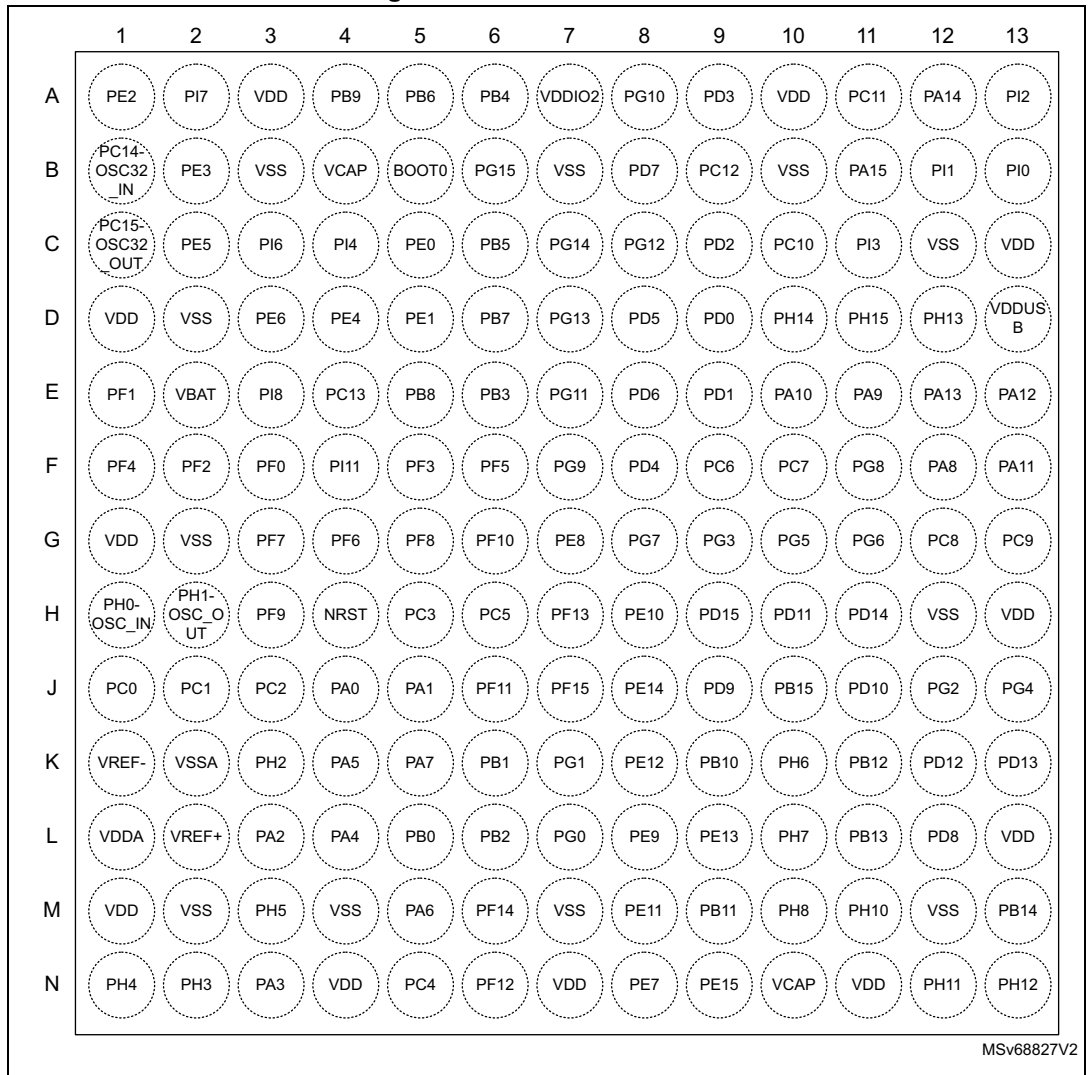
Figure 11. LQFP144 SMPS pinout



MSv64013V3

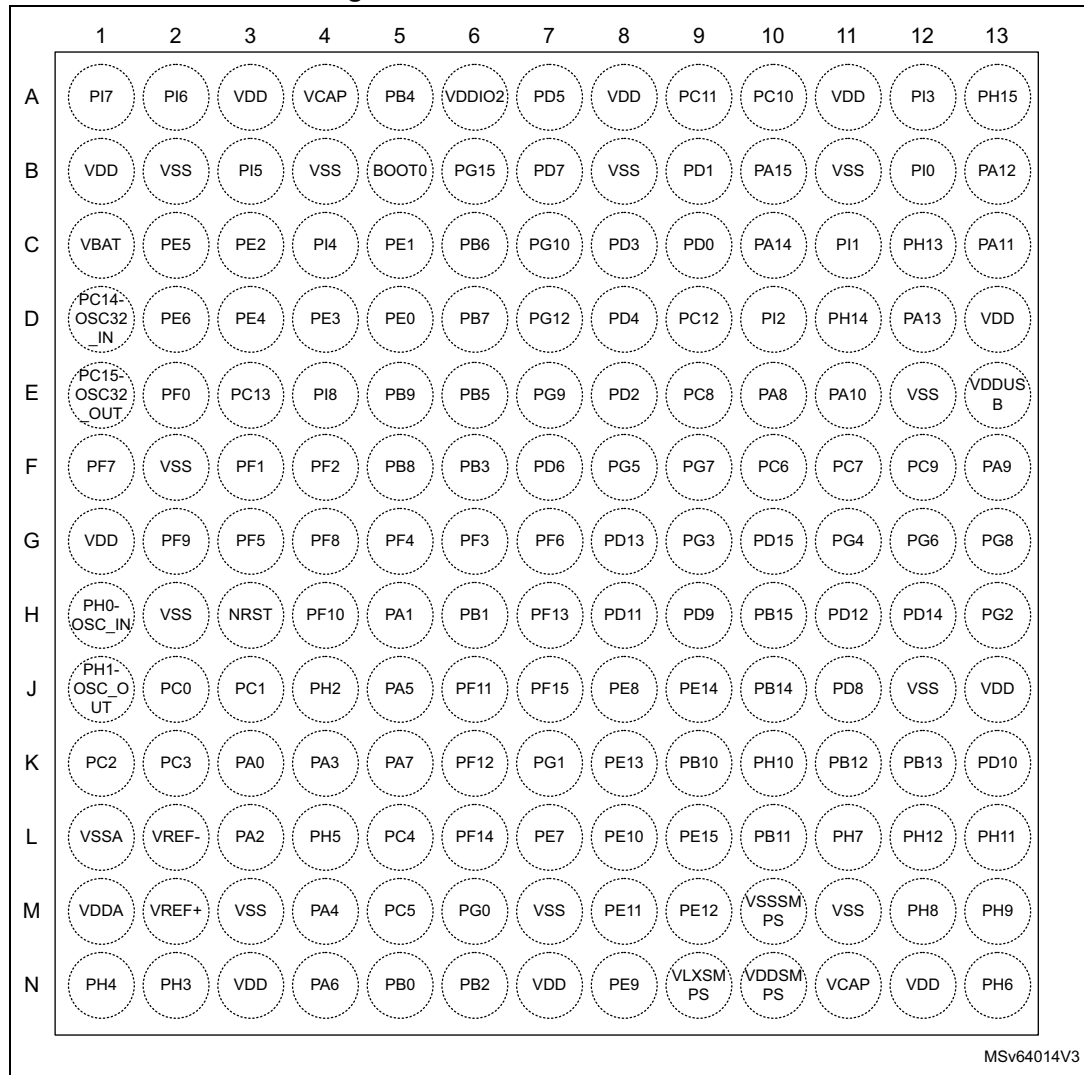
1. The above figure shows the package top view.

Figure 12. UFBGA169 ballout



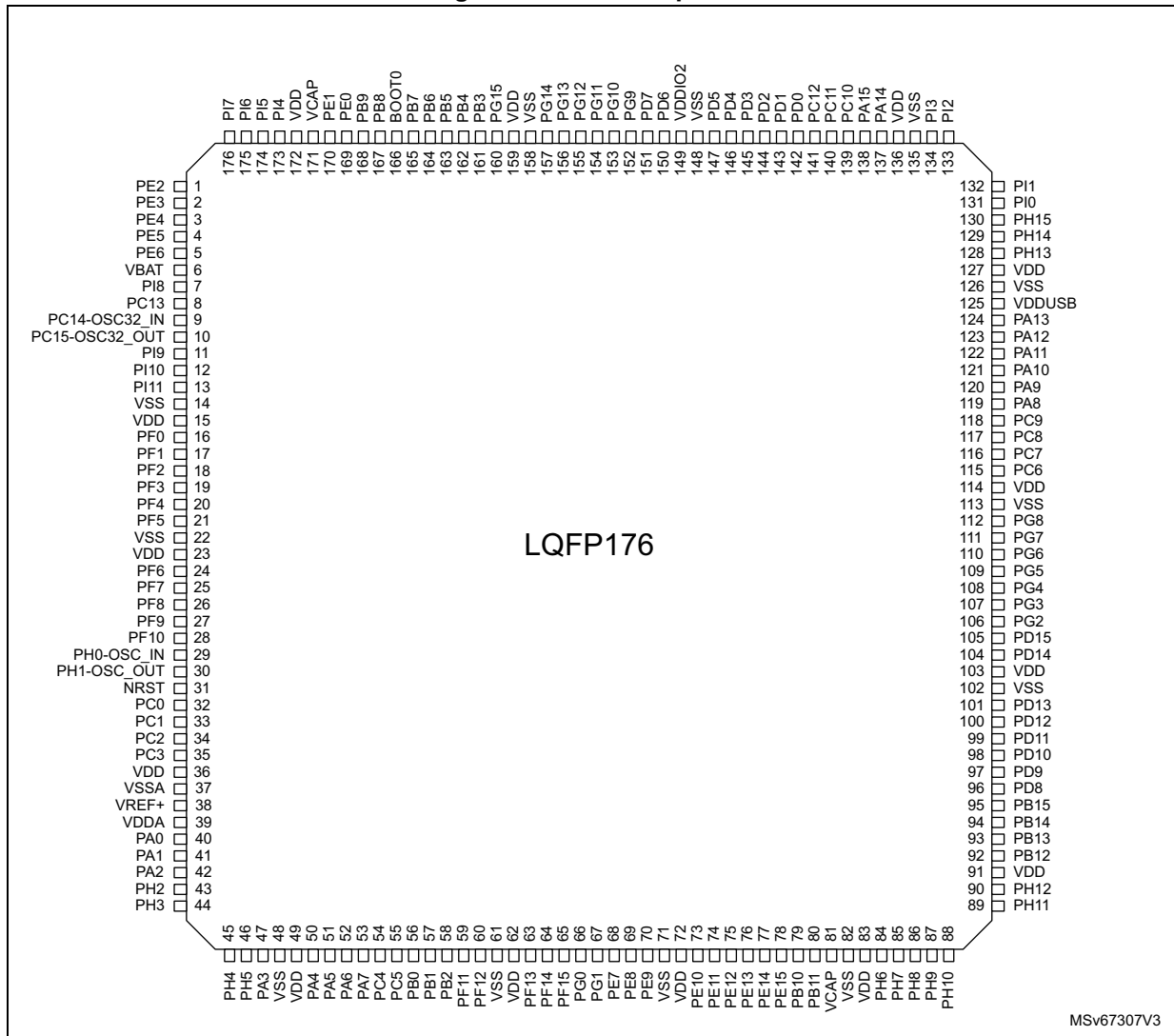
1. The above figure shows the package top view.

Figure 13. UFBGA169 SMPS ballout



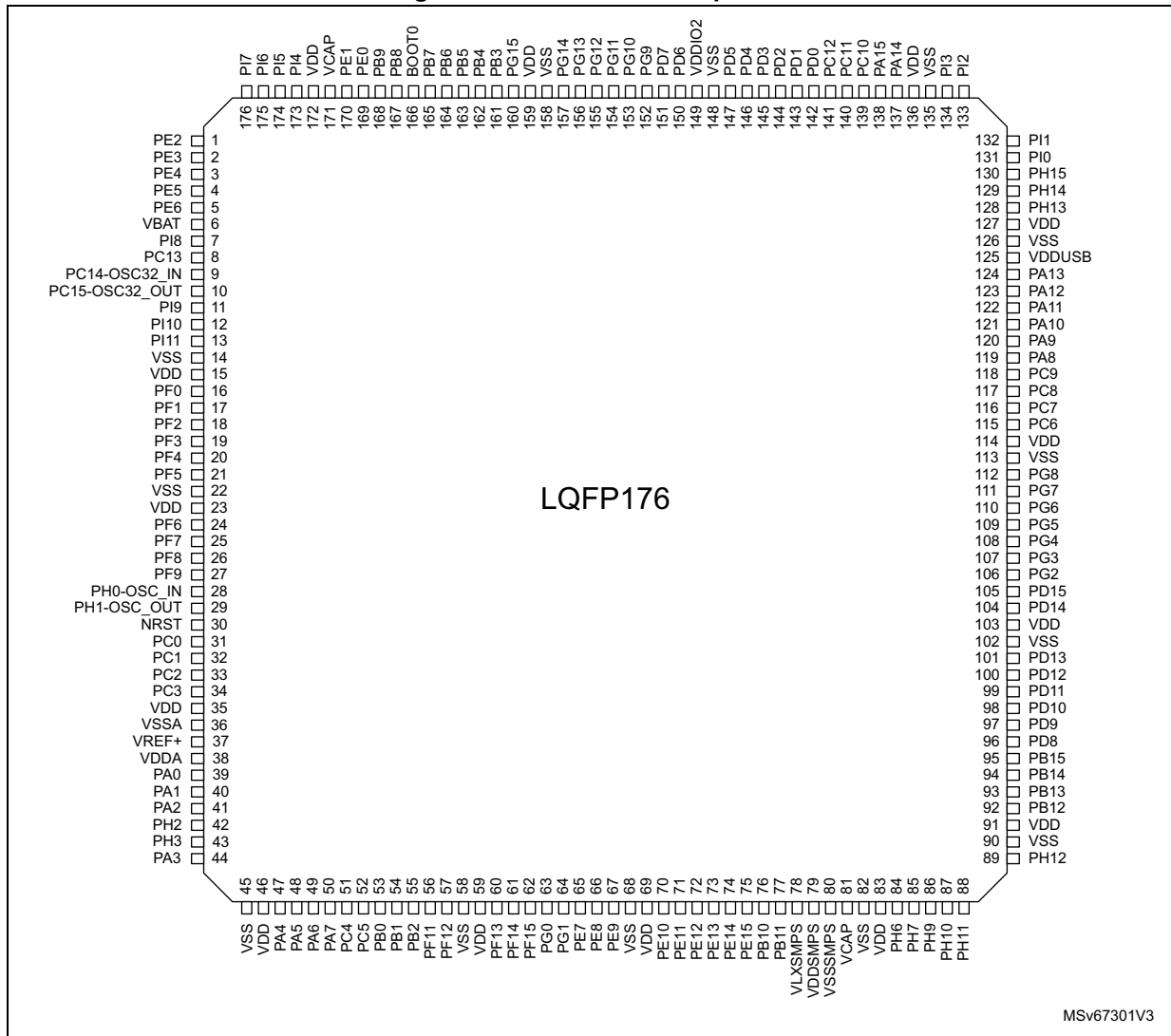
1. The above figure shows the package top view.

Figure 14. LQFP176 pinout



1. The above figure shows the package top view.

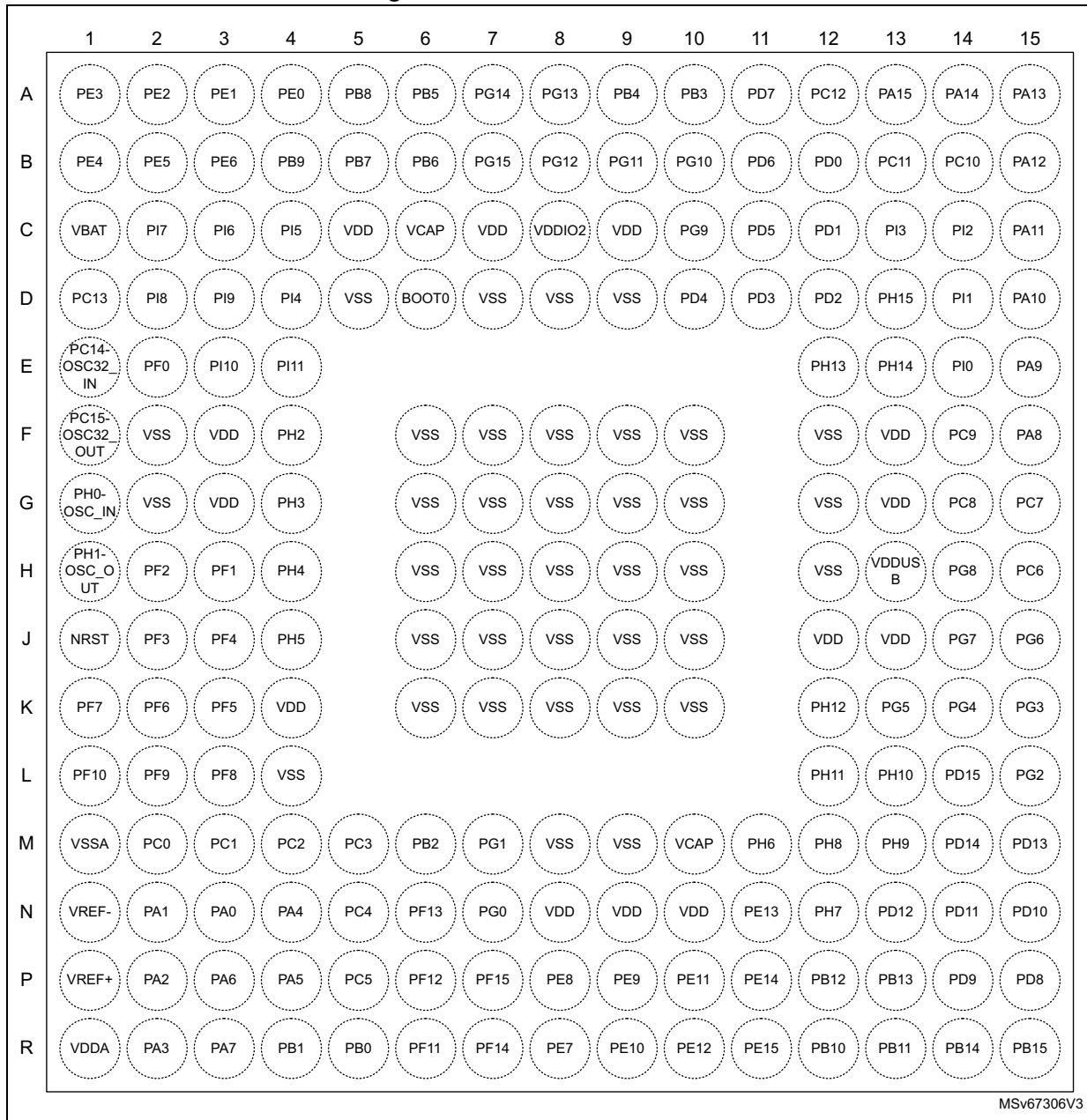
Figure 15. LQFP176 SMPS pinout



MSv67301V3

1. The above figure shows the package top view.

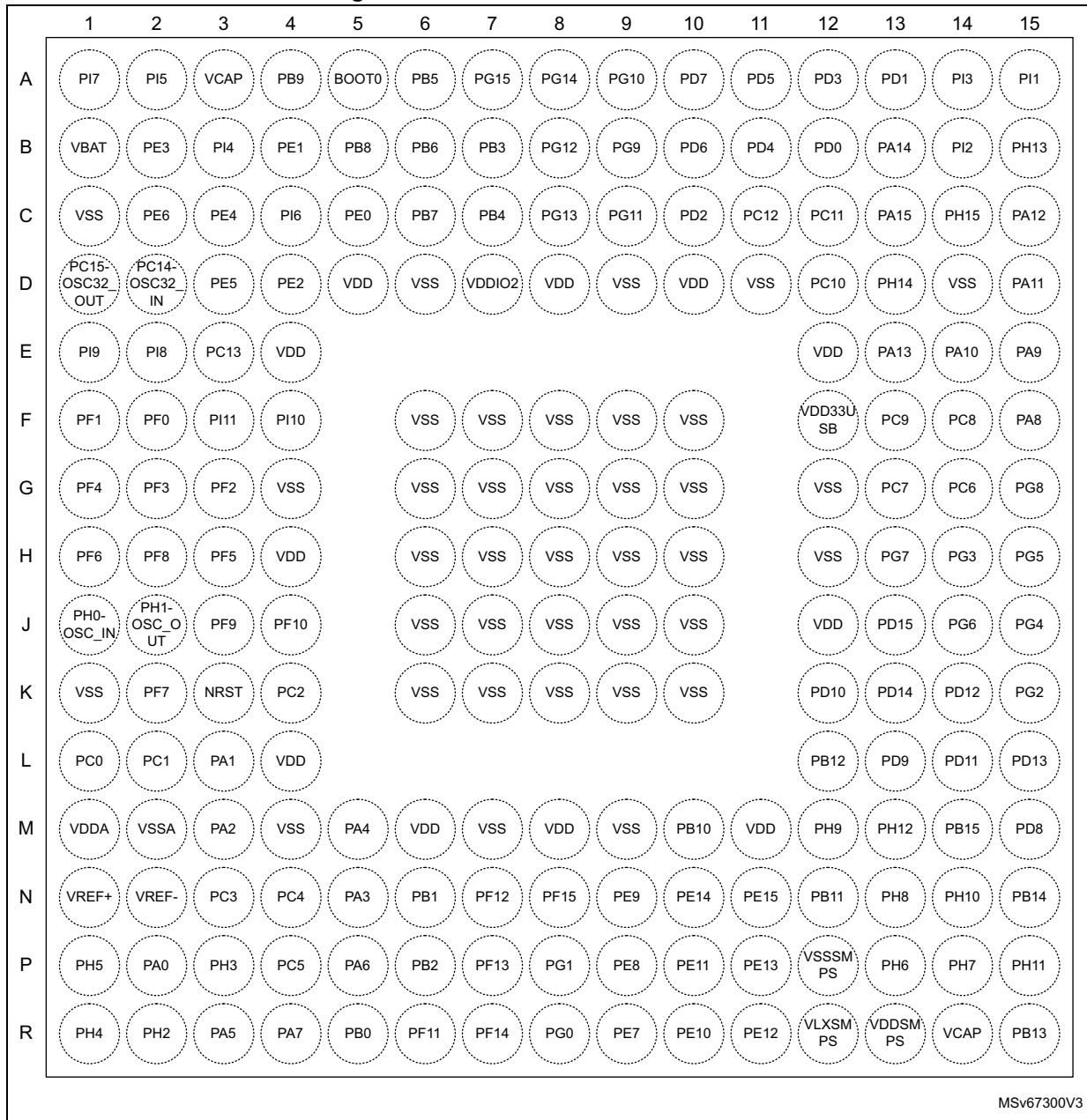
Figure 16. UFBGA176+25 ballout



MSv67306V3

1. The above figure shows the package top view.

Figure 17. UFBGA176+25 SMPS ballout



MSv67300V3

1. The above figure shows the package top view.

4.2 Pin description

Table 13. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/output pin
I/O structure	FT	5 V-tolerant I/O
	TT	3.6 V-tolerant I/O
	RST	Bidirectional reset pin with embedded weak pull-up resistor
	Option for TT or FT I/Os⁽¹⁾	
	_a	I/O, with analog switch function supplied by V _{DDA}
	_c	I/O with USB Type-C power delivery function
	_d	I/O with USB Type-C power delivery dead battery function
	_f	I/O, Fm+ capable
	_h	I/O with high-speed low-voltage mode
	_s	I/O supplied only by V _{DDIO2}
	_t	I/O with tamper function functional in VBAT mode
_u	I/O, with USB function supplied by V _{DDUSB}	
Notes	Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

1. The related I/O structures in the following table are a concatenation of various options. Examples: FT_hat, FT_fs, FT_u, TT_a.

Table 14. STM32H562xx and STM32H563xx pin/ball definition

Pin number ⁽¹⁾⁽²⁾		Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate fu
-	-	-	-	-	-	TRACECLK, LF SAI1_CK1, SAI1_MCLK_A, U SAI1_MCLK_U, UART8_TX, OC ETH_MII_TXD3 DCMI_D3/PSSI_D
-	-	-	-	-	-	TRACED0, TIM SAI1_SD_B, US FMC_A19, EV
-	-	-	-	-	-	TRACED1, S TIM15_CH1N, SAI1_FS_A, F DCMI_D4/PSSI_D
-	-	-	-	-	-	TRACED2, S TIM15_CH1, S SAI1_SCK_A, DCMI_D6/PSSI_D
-	-	-	-	-	-	TRACED3, TIM SAI1_D1, TIM SPI4_MOSI, S SAI2_MCLK_B, DCMI_D7/PSSI_D
A1	-	VDD	S	-	-	
B8	-	VSS	S	-	-	
B10	6	VBAT	S	-	-	
D2	-	VSS	S	-	-	

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate function											
						VLCSP80 SMPs	LQFP100 SMPs	LQFP144 SMPs	UFBGA169 SMPs	LQFP176 SMPs	UFBGA176+25 SMPs	LQFP176	UFBGA176+25	VQFPN68		
-	-	-	-	-	LPTIM3_CH2, L12C2_SMB_A, USART11_CK, LPTIM5_IN1, E	FT_h	I/O	PF2	-	-	-	-	-	-	-	-
-	-	-	-	-	LPTIM3_IN1, USFMC_A3, LPTEVENTC	FT_h	I/O	PF3	-	-	-	-	-	-	-	-
-	-	-	-	-	LPTIM3_ETR, USFMC_A4, EV	FT_h	I/O	PF4	-	-	-	-	-	-	-	-
-	-	-	-	-	LPTIM3_CH1, I3C1_SCL, USART11_CTS/USFMC_A5, LPTEVENTC	FT_fh	I/O	PF5	-	-	-	-	-	-	-	-
H2	-	-	-	-	-	-	S	VSS	-	-	-	-	-	-	-	-
A7	-	-	-	-	-	-	S	VDD	-	-	-	-	-	-	-	-
-	-	-	-	-	TIM16_CH1, SAI1_SD_B, UOCTOSPI1_IO3, IEVENTC	FT_h	I/O	PF6	-	-	-	-	-	-	-	-
-	-	-	-	-	TIM17_CH1, SAI1_MCLK_B, OCTOSPI1_IO2, IEVENTC	FT_h	I/O	PF7	-	-	-	-	-	-	-	-
-	-	-	-	-	TIM16_CH1N, SAI1_SC, UART7_RTS/UTIM13_CH1, OCTOCTOSPI1_IO2, IEVENTC	FT_h	I/O	PF8	-	-	-	-	-	-	-	-



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate function							
						VFQFPN68	UFBGA176+25	LQFP176	UFBGA169	LQFP144	LQFP100	LQFP64
	PF9	I/O	FT_h	-	TIM17_CH1N, SAI1_FS_B, U/TIM14_CH1, OCT/LPTIM5_IN2, EVENTIM16_BKIN, PSSI_D15, OCT/DCMI_D11/P-EVENT							
	PF10	I/O	FT_h	-	TIM16_BKIN, PSSI_D15, OCT/DCMI_D11/P-EVENT							
	PH0-OSC_IN(PH0)	I/O	FT	-	EVENT							
	PH1-OSC_OUT(PH1)	I/O	FT	-	EVENT							
	NRST	I/O	RST	-	-							
	PC0	I/O	FT_a	-	TIM16_BKIN, SAI2_RDY, SAI2_SD_A, SD/OCTOSP11_IO4, FMC_A25, OCT/FMC_SDNWE, TRACED0, SPI2_MOSI/M2SAI1_S							
	PC1	I/O	FT_ah	-	USART11_RTS/USAI2_SD_A, SD/OCTOSP11_IO4, EVENT							
	PC2	I/O	FT_a	-	PWR_CSLEEP, TIM4_CH4, SPI2_M/OCTOSP11_IO5, OETH_MII_TXD2, EVENT							



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Alternate function	Notes	I/O structure	Pin type	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin number ⁽¹⁾⁽²⁾																			
					WLCSP80 SMPs	LQFP100 SMPs	LQFP144 SMPs	UFBGA169 SMPs	LQFP176 SMPs	UFBGA176+25 SMPs	LQFP64	LQFP100	LQFP144	UFBGA169	LQFP176	UFBGA176+25	VQFPN68							
					L9	18	29	29	K2	34	N3	11	18	29	H5	35	M5	11	PC3	I/O	FT_a	-	PWR_CSTOP, LPTIM3, SPI2_MOSI/2, OCTOSPI1_IO6, O ETH_MII_T FMC_SDCKE0,	
					G1	-	-	30	-	35	H4	-	-	30	M1	36	G3	-	VDD	S	-	-	-	
					P2	-	-	-	H2	-	K1	-	-	-	M2	-	G2	-	VSS	S	-	-	-	
					N9	19	30	31	L1	36	M2	12	19	31	K2	37	M1	12	VSSA	S	-	-	-	
					-	-	-	L2	L2	-	N2	-	20	-	K1	-	N1	-	VREF-	S	-	-	-	
					-	20	31	31	M2	37	N1	-	21	32	L2	38	P1	-	VREF+	S	-	-	-	
					P10	21	32	32	M1	38	M1	13	22	33	L1	39	R1	13	VDDA	S	-	-	-	
					K8	22	33	33	K3	39	P2	14	23	34	J4	40	N3	14	PA0	I/O	FT_at	(5)	TIM2_CH1, TIM TIM8_ETR, TIM SPI6_NSS, S USART2_CTS/US UART4_TX, SDN SAI2_SD_B, ET TIM2_ETR, E	
					J7	23	34	34	H5	40	L3	15	24	35	J5	41	N2	15	PA1	I/O	FT_aht	(5)	TIM2_CH2, TIM TIM15_CH1N, L OCTOSPI1 USART2_RTS/US UART4_RX, OC SAI2_MC ETH_MII_RX_CLK/ F_CLK, EVE	



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate f							
						VFQFPN68	UFBGA176+25	LQFP176	UFBGA169	LQFP144	LQFP100	LQFP64
M8	PA2	I/O	FT_hat	(5)	TIM2_CH3, TIM15_CH1, USART2_TX, ETH_MDIO, ETH							
-	PH2	I/O	FT_h	-	LPTIM1_IN2, OCTOSPI1_SCK_B, ETH_SAI2_SCK_B, ETH_FMC_SDCKEO,							
H10	VDD	S	-	-	-							
P8	VSS	S	-	-	-							
-	PH3	I/O	FT_ah	-	OCTOSPI1_IO5, SPI2_NSS/IO5, ETH_MII_COL, ETH_EVENTC							
-	PH4	I/O	FT_fa	-	I2C2_SCL, SPI5_RX, PSSI_D14, ETH_EVENTC							
-	PH5	I/O	FT_fa	-	I2C2_SDA, SPI6_RDY, FMC_EVENTC							
T10	PA3	I/O	FT_ah	-	TIM2_CH4, TIM2_CH3, TIM15_CH1, USART2_RX, ETH_EVENTC							
-	VSS	S	-	-	-							
R1	VDD	S	-	-	-							



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate function	
WLCSP80 SMPs	LQFP100 SMPs	-	-	-	T8	TIM1_CH4N, PSSI_D15, S/ UART12_RTS/U OCTOSPI1 ETH_MII_RXD1/ET , FMC_SDCKE0.
LQFP100 SMPs	LQFP144 SMPs	-	-	-	T8	TIM1_CH4N, PSSI_D15, S/ UART12_RTS/U OCTOSPI1 ETH_MII_RXD1/ET , FMC_SDCKE0.
LQFP100 SMPs	LQFP144 SMPs	-	-	-	T8	TIM1_CH4N, PSSI_D15, S/ UART12_RTS/U OCTOSPI1 ETH_MII_RXD1/ET , FMC_SDCKE0.
LQFP176 SMPs	LQFP176 SMPs	-	-	-	T8	TIM1_CH4N, PSSI_D15, S/ UART12_RTS/U OCTOSPI1 ETH_MII_RXD1/ET , FMC_SDCKE0.
LQFP176 SMPs	LQFP176 SMPs	-	-	-	T8	TIM1_CH4N, PSSI_D15, S/ UART12_RTS/U OCTOSPI1 ETH_MII_RXD1/ET , FMC_SDCKE0.
LQFP176+25 SMPs	LQFP176+25 SMPs	-	-	-	T8	TIM1_CH4N, PSSI_D15, S/ UART12_RTS/U OCTOSPI1 ETH_MII_RXD1/ET , FMC_SDCKE0.
LQFP64	LQFP64	25	26	27	R7	TIM1_CH2N, T TIM8_CH2N, OC USART11_CK, U ETH_MII_RXD2, I EVENTC
LQFP100	LQFP100	34	35	36	P6	TIM1_CH3N, T TIM8_CH3N, OC ETH_MII_RXD3, I EVENTC
LQFP144	LQFP144	45	46	47	L5	RTC_OUT2, TIM8_CH4N, S LPTIM1_CH1, S SPI3_MOSI/M2 OCTOSPI1 OCTOSPI1 SDMMC1_CMD, I EVENTC
LQFP144 SMPs	LQFP144 SMPs	-	43	44	-	SPI5_MOSI, OCTO SAI2_SD_B, FI DCMI_D12/P LPTIM6_CH1, E
LQFP144 SMPs	LQFP144 SMPs	-	43	44	-	SPI5_MOSI, OCTO SAI2_SD_B, FI DCMI_D12/P LPTIM6_CH1, E
LQFP176 SMPs	LQFP176 SMPs	52	53	54	-	FMC_A6, LPT EVENTC
LQFP176+25 SMPs	LQFP176+25 SMPs	P4	R5	N6	-	FMC_A6, LPT EVENTC
UFBGA169 SMPs	UFBGA169 SMPs	M5	N5	H6	-	FMC_A6, LPT EVENTC
UFBGA169	LQFP144	H6	L5	K6	-	FMC_A6, LPT EVENTC
LQFP176	LQFP144	55	46	47	-	FMC_A6, LPT EVENTC
UFBGA176+25	LQFP144	P5	R5	R4	-	FMC_A6, LPT EVENTC
VQFPN68	LQFP144	25	46	47	-	FMC_A6, LPT EVENTC





Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin number ⁽¹⁾⁽²⁾												Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate function	
	WLCSP80 Smps	LQFP100 Smps	LQFP144 Smps	UFBGA169 Smps	LQFP176 Smps	UFBGA176+25 Smps	LQFP64	LQFP100	LQFP144	UFBGA169	LQFP176	UFBGA176+25						VQFPN68
-	-	-	48	M7	58	-	-	51	M7	61	-	-	-	VSS	S	-	-	-
-	-	-	49	N7	59	-	-	52	N7	62	N9	-	-	VDD	S	-	-	-
-	-	-	50	H7	60	P7	-	53	H7	63	N6	-	-	PF13	I/O	FT_ah	-	I2C4_SMBA, LPTIM6_IN1, E
-	-	-	51	L6	61	R7	-	54	M6	64	R7	-	-	PF14	I/O	FT_fah	-	FMC_A8, LPT EVENT
-	-	-	52	J7	62	N8	-	55	J7	65	P7	-	-	PF15	I/O	FT_fh	-	I2C4_SDA, I3C1_S EVENT
-	-	-	53	M6	63	R8	-	56	L7	66	N7	-	-	PG0	I/O	FT_h	-	UART9_RX, F LPTIM4_IN1, E
-	-	-	54	K7	64	P8	-	57	K7	67	M7	-	-	PG1	I/O	FT_h	-	SPI2_MOSI/M2 UART9_TX, F EVENT
T6	35	-	55	L7	65	R9	-	58	N8	68	R8	-	-	PE7	I/O	FT_ah	-	TIM1_E UART12_RTS/U UART7_RX, OC FMC_D4/FMC_AD
N5	36	-	56	J8	66	P9	-	59	G7	69	P8	-	-	PE8	I/O	FT_ah	-	TIM1_CI UART12_CTS/U UART7_TX, OC FMC_D5/FMC_AD
R5	37	-	57	N8	67	N9	-	60	L8	70	P9	-	-	PE9	I/O	FT_ah	-	TIM1_CH1, UA UART7_RTS/U OC TOSPI FMC_D6/FMC_AD
-	-	-	58	-	68	-	-	61	-	71	-	-	-	VSS	S	-	-	-
-	-	-	59	-	69	-	-	62	-	72	-	-	-	VDD	S	-	-	-

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate function							
						VFQFPN68	UFBGA176+25	LQFP176	UFBGA169	LQFP144	LQFP100	LQFP64
M4	PE10	I/O	FT_ah	-	TIM1_CH2N, UART7_CTS, OC_FMC_D7/FMC_AD							
-	PE11	I/O	FT_ah	-	TIM1_CH2, SPI4_NSS, OCT_SAI2_SD_B, FMC_EVENTC							
-	PE12	I/O	FT_h	-	TIM1_CH3N, SAI2_SC FMC_D9/FMC_AD							
-	PE13	I/O	FT_h	-	TIM1_CH3, SAI2_FS FMC_D10/FM EVENTC							
-	PE14	I/O	FT_h	-	TIM1_CH4, SAI2_MC FMC_D11/FM EVENTC							
-	PE15	I/O	FT_h	-	TIM1_BKIN, TIM_USART10 FMC_D12/FM EVENTC							
P4	PB10	I/O	FT_f	-	TIM2_CH3, LP_TIM2_IN1, SPI2_SCK/I2_USART3_TX, OC_ETH_MII_RX_ER							



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾												Pin type	I/O structure	Notes	Alternate function	
	WLSP80 SMPS	LQFP100 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP176 SMPS	UFBGA176+25 SMPS	LQFP64	LQFP100	LQFP144	UFBGA169	LQFP176	UFBGA176+25					VQFPN68
-	-	45	67	L10	77	N12	-	-	-	M9	80	R13	30	I/O	FT_f	-	TIM2_CH4, LP12C2_SDA, SPI2_RUSART3_ETH_MIL_TX_LEN/EN, FMC_NBL1,
T4	46	68	N9	78	R12	-	-	-	-	-	78	R12	-	S	-	-	-
R3	47	69	N10	79	R13	-	-	-	-	-	79	R13	-	S	-	-	-
N3	48	70	M10	80	P12	-	-	-	-	-	80	P12	-	S	-	-	-
T2	49	71	N11	81	R14	30	48	70	N10	N10	81	M10	31	S	-	-	-
-	50	72	M11	82	M9	31	49	71	M12	M9	82	M9	32	S	-	-	-
-	51	73	N12	83	M11	32	50	72	N11	N11	83	N10	33	S	-	-	-
-	-	-	-	N13	P13	-	-	-	K10	M11	84	M11	-	I/O	FT	-	TIM1_CH3N, TIM12C3_SCL_SF_ETH_MIL_RXD3, FDCMI_D9/PSSI_D
-	-	-	L11	85	P14	-	-	-	L10	N12	85	N12	-	I/O	FT_f	-	TIM1_CH3, TIM12C3_SCL_SF_ETH_MIL_RXD3, FDCMI_D9/PSSI_D
-	-	-	M12	-	N13	-	-	-	M10	M12	86	M12	-	I/O	FT_fh	-	TIM1_CH2N, TIM18_CH2, I2C3_SCL_SF_ETH_MIL_RXD3, FDCMI_HSYNCEVENT



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate function							
						VFQFPN68	UFBGA176+25	LQFP176	UFBGA169	LQFP144	LQFP100	LQFP64
	PH9	I/O	FT_h	-	TIM1_CH2, TIM8_CH2N, I2C2_SDA, SPI5_NSS, DCMI_EVENTC							
	PH10	I/O	FT_h	-	TIM1_CH1N, TIM8_CH3, I2C2_SDA, SPI5_RDY, DCMI_EVENTC							
	PH11	I/O	FT_fh	-	TIM1_CH1, TIM8_CH3N, I3C1_SCL, DCMI_EVENTC							
	PH12	I/O	FT_fh	-	TIM1_BKIN, TIM8_BKIN, I3C1_SDA, TIMDCMI_D3/PSSI_D							
	VSS	S	-	-	-							
	VDD	S	-	-	-							
	PB12	I/O	FT_fh	-	TIM1_BKIN, OCT2C2_SDA, SPI2_NUCPD1_FRSTX, FDCAN2_ETH_MIL_TXD0/ETUART5_RX, E							
	L3											
	L12											
	92											
	91											
	90											
	M13											
	M12											
	M11											
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Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate f.
WLCSP80 SMPs	M2				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
LQFP100 SMPs	M2				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
LQFP144 SMPs	M2				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
UFBGA169 SMPs	M2				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
LQFP176 SMPs	M2				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
UFBGA176+25 SMPs	M2				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
LQFP64	34				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
LQFP100	52				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
LQFP144	74				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
UFBGA169	L11				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
LQFP176	93				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
UFBGA176+25	P13				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
VQFPN68	35				TIM1_CH1N, LI LPTIM2_CH1, I2 SPI2_SCK/I2C USART3_CTS/USART3_TX, SPI FDCAN2_TX, SPI UART5_TX, E
L1	N1	I/O	FT_c	(6)	TIM1_CH2N, T TIM8_CH2N, U SPI2_MISO/I USART3_RTS/USART3_TX USART4_RTS/USART4_TX SDMMC2_D0, LI EVENTC
L1	L1	I/O	FT_h	-	RTC_REFIN, T TIM12_CH2, T USART1 SPI2_MOSI/I2C USART11_CTS/USART11_TX USART4_CTS, SPI OCTOSPI1 ETH_MIL_TXD1/ET DCMI_D2/PSSI_D EVENTC
-	-	I/O	FT_h	-	USART3 FMC_D13/FM EVENTC
-	-	S	-	-	-
-	-	I/O	FT_h	-	USART3_RX, F FMC_D14/FM EVENTC



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate function							
						VFQFPN68	UFBGA176+25	LQFP176	UFBGA169	LQFP144	LQFP100	LQFP64
-	PD10	I/O	FT_h	-	LPTIM2_CH2, U FMC_D15/FM EVENTC							
38	PD11	I/O	FT_h	-	SAI1_CK1, LP I2C4_SN USART3_CTS/UA UART4_RX, OC SAI2_S FMC_A16/FMC_CL							
39	PD12	I/O	FT_fh	-	LPTIM1_IN1, T LPTIM2_IN1, I I3C1_SCL, S USART3_RTS/UA UART4_TX, OC SAI2_FS_A, FMC_7 DCMI_D12/P EVENTC							
-	PD13	I/O	FT_fh	-	LPTIM1_CH1, LPTIM2_CH1, I3C1_SDA, OCT SAI2_SC UART9_RTS/UA FMC_A18, DCMI_L LPTIM4_IN1, E							
-	VSS	S	-	-								
-	VDD	S	-	-								
-	PD14	I/O	FT_h	-	TIM4_CH3, UA UART9_RX, FMC EVENTC							



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate function							
						WLCSP80 SMPs	LQFP100 SMPs	LQFP144 SMPs	UFBGA169 SMPs	LQFP176 SMPs	UFBGA176+25 SMPs	LQFP64
J1		I/O	FT_h	-	TIM4_C UART8_RTS/US UART9_TX, FMC_ EVENTC							
-		S	-	-	-							
-	VDD	S	-	-	-							
-	VSS	S	-	-	-							
-	PG2	I/O	FT_h	-	TIM8_BKIN, U FMC_A12, LPT_ EVENTC							
-	PG3	I/O	FT_h	-	TIM8_BKIN2, U FMC_A13, LPT_ EVENTC							
-	PG4	I/O	FT_h	-	TIM1_BK FMC_A14/FM LPTIM4_ETR, E							
-	PG5	I/O	FT_h	-	TIM1_ETR, FMC_ / EVENTC							
-	PG6	I/O	FT_fh	-	TIM17_BKIN, I I2C4_SDA, S OCTOSPI1 UCPD1_FRSTX DCMI_D12/P EVENTC							
-	PG7	I/O	FT_fh	-	SAI1_CK2, I3C1_S SAI1_MCLK, A, L UCPD1_FRSTX DCMI_D13/P EVENTC							



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate function
WLCSP80 SMPS	LQFP100 SMPS	-	-	-	TIM8_ETR, S
LQFP144 SMPS	LQFP144 SMPS	93	94	95	USART16_RTS/US
UFBGA169 SMPS	LQFP176 SMPS	112	113	114	ETH_PPS_OUT, F
UFBGA176+25 SMPS	LQFP176 SMPS	112	113	114	EVENTC
LQFP64	LQFP64	-	-	-	-
LQFP100	LQFP100	-	-	-	-
LQFP144	LQFP144	93	94	95	TIM3_CH1, TI
UFBGA169	LQFP176	F11	113	114	I2S2_MCK, SA
UFBGA176+25	UFBGA176+25	H14	-	-	USART16_TX, SD
VQFPN68	VQFPN68	-	-	-	FMC_NWAIT, S
		PG8	VSS	VDD	OCTOSP11_IO5, S
					DCMI_D0/PSSI_D
J3		PC6			TRGIO, TIM3_CH
K4		PC7			I2S3_MCK, US
J5		PC8			SDMMC1_D123D
F2		PC9			SDMMC2_D7, OC
					SDMMC1
					DCMI_D1/PSSI_D
					TRACED1, TI
					TIM8_CH3, US
					UART5_RTS/US
					FMC_NE2/FMC_N
					FMC_ALE, SDD
					DCMI_D2/PSSI_D
					MCO2, TIM3_CH
					I2C3_SDA, AI
					UART5_CTS, OC
					FMC_CLE, SD
					DCMI_D3/PSSI_D



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾ (2)		Pin name (function after reset) ⁽³⁾ (4)	Pin type	I/O structure	Notes	Alternate f
WLCSP80 SMPS	LQFP100 SMPS	67				
LQFP144 SMPS	LQFP144 SMPS	100				
UFBGA169 SMPS	UFBGA169 SMPS	E10				
LQFP176 SMPS	LQFP176 SMPS	119				
UFBGA176+25 SMPS	UFBGA176+25 SMPS	F15				
LQFP64	LQFP64	41				
LQFP100	LQFP100	67				
LQFP144	LQFP144	100				
UFBGA169	UFBGA169	F12				
LQFP176	LQFP176	119				
UFBGA176+25	UFBGA176+25	F15				
VQFPN68	VQFPN68	44				
		VSS	S	-	-	-
		VDD	S	-	-	-
		PA8	I/O	FT_fh	-	MCO1, TIM1_CH1, I2C3_SCL, SPI2, USART1_CK, UART7_RX, FDCMI, DCMI_D3/PSSI_D
		PA9	I/O	FT_d	-	TIM1_CH2, LPUART1, I2C3_SMBA, SPI2, USART1_TX, ETH, FMC_NWE, DCMI, EVENTOUT
		PA10	I/O	FT_h	-	TIM1_CH3, LPUART1, LPTIM2_IN2, UC, USART1_RX, FDCMI, SDMMC1, DCMI_D1/PSSI_D
		PA11	I/O	FT_u	-	TIM1_CH4, LPUART1, SPI2_NSS/I2S2_W, USART1_CTS/USART1, FDCAN1_RX, EVENTOUT
		PA12	I/O	FT_u	-	TIM1_ENCODER, LPUART1_RTS/LPUART1, SPI2_SCK/I2S2_C, USART1_RTS/USART1, SAI2_FS_B, FE, USB_DP, EV



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾												Pin type	I/O structure	Notes	Alternate function		
	WLCSP80 SMPs	LQFP100 SMPs	LQFP144 SMPs	UFBGA169 SMPs	LQFP176 SMPs	UFBGA176+25 SMPs	LQFP64	LQFP100	LQFP144	UFBGA169	LQFP176	UFBGA176+25					VQFPN68	
F4	72	105	D12	124	E13	46	72	105	E12	124	A15	49	PA13 (JTMS/SWDIO)	I/O	FT	(7)	JTMS/SWDIO	
-	74	107	E12	126	D14	47	74	107	C12	126	F12	50	VSS	S	-	-	-	-
-	75	108	D13	127	E12	48	75	108	C13	127	F13	51	VDD	S	-	-	-	-
B2	73	106	E13	125	F12	-	73	106	D13	125	H13	-	VDDUSB	S	-	-	-	-
-	-	-	C12	128	B15	-	-	-	D12	128	E12	-	PH13	I/O	FT_h	-	-	LPTIM1_IN2, TIM8_CH2N, UART8_TX, UART8_RX, FDCAN1_TX, DCM1_EVENTC
-	-	-	D11	129	D13	-	-	-	D10	129	E13	-	PH14	I/O	FT_h	-	-	TIM8_CH2N, FDCAN1_DCM1_D4/PSSI_D
-	-	-	A13	130	C14	-	-	-	D11	130	D13	-	PH15	I/O	FT_h	-	-	TIM8_CH2N, FDCAN1_DCM1_D4/PSSI_D
-	-	-	B12	131	-	-	-	-	B13	131	E14	-	PI0	I/O	FT_h	-	-	TIM5_CH4, SPI2_I2C1, DCMI_D13/PSSI_D
-	-	-	C11	132	A15	-	-	-	B12	132	D14	-	PI1	I/O	FT_h	-	-	TIM8_CH4, SPI2_I2C1, DCMI_D8/PSSI_D
-	-	-	D10	133	B14	-	-	-	A13	133	C14	-	PI2	I/O	FT_h	-	-	TIM8_CH4, SPI2_I2C1, DCMI_D9/PSSI_D
-	-	-	A12	134	A14	-	-	-	C11	134	C13	-	PI3	I/O	FT_h	-	-	TIM8_CH4, SPI2_I2C1, DCMI_D10/PSSI_D



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾		Pin type	I/O structure	Notes	Alternate f
	Package	Pin				
WLCSP80 SMPs	-	-	-	-	-	-
LQFP100 SMPs	-	-	-	-	-	-
LQFP144 SMPs	-	-	-	-	-	-
UFBGA169 SMPs	B8	A8	S	-	-	-
LQFP176 SMPs	135	136	S	-	-	-
UFBGA176+25 SMPs	D9	D8	S	-	-	-
LQFP64	-	-	I/O	FT	(7)	JTCK/SWCLK, JTDI, TIM2_CH1, HDMI_CEC, SPI1, SPI3_NSS/I2S3_V, UART4_RTS/USART7_TX, FTDCMI_D11/PSSI_D
LQFP100	76	77	I/O	FT	(7)	LPTIM3, SPI3_SCK/I2S3_TX, USART3_TX, L, OCTOSPI1, ETH_MII_TXD0/ETSDMMC1, DCMI_D8/PSSI_D
LQFP144	109	110	I/O	FT_h	-	LPTIM3, SPI3_MISO/I, USART3_RX, L, OCTOSPI1_NCS, DCMI_D4/PSSI_D
UFBGA169	B10	A10	I/O	FT_h	-	LPTIM3, SPI3_MISO/I, USART3_RX, L, OCTOSPI1_NCS, DCMI_D4/PSSI_D
LQFP176	135	136	I/O	FT_h	-	TRACED3, TIM, SPI6_S, SPI3_MOSI/I2S3_TX, USART3_CK, L, SDMMC1, DCMI_D9/PSSI_D
UFBGA176+25	D9	C9	I/O	FT_h	-	TRACED3, TIM, SPI6_S, SPI3_MOSI/I2S3_TX, USART3_CK, L, SDMMC1, DCMI_D9/PSSI_D
VQFPN68	-	-	I/O	FT_h	-	TRACED3, TIM, SPI6_S, SPI3_MOSI/I2S3_TX, USART3_CK, L, SDMMC1, DCMI_D9/PSSI_D



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin number ⁽¹⁾⁽²⁾												Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate f	
	WLCSP80 SMPS	LQFP100 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP176 SMPS	UFBGA176+25 SMPS	LQFP64	LQFP100	LQFP144	UFBGA169	LQFP176	UFBGA176+25						VQFPN68
-	-	-	-	B11	-	-	D11	-	-	-	-	-	-	VSS	S	-	-	-
-	-	-	A11	A11	-	-	D10	-	-	-	-	-	-	VDD	S	-	-	-
A3	81	114	C9	C9	142	B12	B12	81	114	D9	142	B12	-	PD0	I/O	FT_h	-	TIM8_CH4N, U FDCAN1_RX, U FMC_D2/FMC_AD
B4	82	115	B9	B9	143	A13	A13	82	115	E9	143	C12	-	PD1	I/O	FT_h	-	UART4_TX, FC FMC_D3/FMC_AD
A5	83	116	E8	E8	144	C10	C10	83	116	C9	144	D12	-	PD2	I/O	FT_h	-	TRACED2, TI TIM15_BKIN, U SDMMC1_1 DCMI_D11/P LPTIM4_ETR, E
-	84	117	C8	C8	145	A12	A12	84	117	A9	145	D11	-	PD3	I/O	FT_h	-	SPI2_SCK/I2 USART2_CTS/U FMC_CLK, DCMI, EVENTC
-	85	118	D8	D8	146	B11	B11	85	118	F8	146	D10	-	PD4	I/O	FT_h	-	USART2_RTS/U OCTOSPI1_IO4, EVENTC
-	86	119	A7	A7	147	A11	A11	86	119	D8	147	C11	-	PD5	I/O	FT_h	-	TIM1_CH4N, S USART2_TX, FI OCTOSPI1_IO5, EVENTC
-	-	120	-	-	148	-	-	-	120	B7	148	D8	-	VSS	S	-	-	-
-	-	121	A6	A6	149	D7	D7	-	121	A7	149	C8	-	VDDIO2	S	-	-	-



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾		Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate f
WLCSP80 SMPs	-					
LQFP100 SMPs	87					SAI1_D1, SPI3_MC SAI1_SD_A, US OCTOSP11_IO6, S FMC_NV DCMI_D10/P EVENTC
LQFP144 SMPs	122					SPI1_MOSI/2 USART2_CK, OC SDMMC2 FMC_NE1/FM LPTIM4_OUT, E
UFBGA169 SMPs	F7					
LQFP176 SMPs	150					
UFBGA176+25 SMPs	B10					
LQFP64	-					
LQFP100	87					
LQFP144	122					
UFBGA169	E8					
LQFP176	150					
UFBGA176+25	B11					
VQFPN68	-					
		PD6	I/O	FT_sh	-	
		PD7	I/O	FT_sh	-	
		VSS	S	-	-	
		PG9	I/O	FT_sh	-	SPI1_MISO/I USART6_RX, OC SAI2_FS_B, SD FMC_NE2/FM DCMI_VSYNCR EVENTC
		PG10	I/O	FT_sh	-	SPI1_NSS/I2S1_W SDMMC2_D1, DCMI_D2/PSSI_D
		PG11	I/O	FT_sh	-	LPTIM1_IN2, SPI1_ USART1C USART11_RTS/U SDMMC2 ETH_MII_TX_ENE EN, DCMI_D3 EVENTC

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾		Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate f
WLCSP80 SMPs	-					LPTIM1_IN1, F SPI6_MISO, US USART6_RTS/U SDMMC2 ETH_MIL_TXD1/ET FMC_NE4, DCMI_L LPTIM5_CH1, F
LQFP100 SMPs	-					TRACED0, LP SPI6_S USART10_CTS/U USART6_CTS/U SDMMC2 ETH_MIL_TXD0/ET FMC_A24, LP EVENTC
LQFP144 SMPs	126					TRACED1, LP LPTIM1_CH2, S LPTIM1_RTS/U USART10_TX, OC SDMMC2 ETH_MIL_TXD1/ET FMC_A25, LP EVENTC
LQFP100 SMPs	-					
LQFP144 SMPs	127					
UFBGA169 SMPs	D7					
LQFP176 SMPs	155					
UFBGA176+25 SMPs	B8					
LQFP64	-					
LQFP100	-					
LQFP144	127					
UFBGA169	C8					
LQFP176	155					
UFBGA176+25	B8					
VQFPN68	-					
		PG12	I/O	FT_sh	-	
		PG13	I/O	FT_sh	-	
		PG14	I/O	FT_sh	-	
		VSS	S	-	-	
		VDD	S	-	-	
		PG15	I/O	FT_h	-	SPI4_RDY, US USART6_CTS/U FMC_NC DCMI_D13/P EVENTC



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate function
WLCSP80 SMPS	LQFP100 SMPS	89	C5		JTDO/TRACESW I2C2_SDA, SPI1_S I2C2_SCK, SPI3_SCK/I2 S13_SCK, SD UART12_CTS/UART1 SPI6_SCK, SD CRS_SYNC, U LPTIM6_ETR, F
LQFP144 SMPS	LQFP144 SMPS	132	F6		
UFBGA169 SMPS	LQFP176 SMPS	161	B7		
UFBGA176+25 SMPS	LQFP64	55			
LQFP100	LQFP100	89			
LQFP144	LQFP144	133			
UFBGA169	LQFP176	161			
UFBGA176+25	UFBGA176+25	A10			
VQFPN68	VQFPN68	57			
B6	B6		B6		
D6	D6		D6		
E7	E7		E7		
B6	B6		B6		
B6	B6		B6		
A5	A5		A5		
A6	A6		A6		
C6	C6		C6		
A6	A6		A6		
A9	A9		A9		
58	58		58		
59	59		59		
FT_h	FT_h		FT_h		
FT_h	FT_h		FT_h		
FT_f	FT_f		FT_f		



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾ (2)	Pin name (function after reset) ⁽³⁾ (4)	Pin type	I/O structure	Notes	Alternate f
WLCSP80 SMPs	LQFP100 SMPs	93	93	94	DCMI_VSYNC/ EVENT0
LQFP144 SMPs	LQFP144 SMPs	136	136	137	DCMI_VSYNC/ EVENT0
UFBGA169 SMPs	LQFP176 SMPs	165	165	166	DCMI_VSYNC/ EVENT0
UFBGA176+25 SMPs	LQFP176 SMPs	165	165	166	DCMI_VSYNC/ EVENT0
LQFP64	LQFP64	59	59	60	DCMI_VSYNC/ EVENT0
LQFP100	LQFP100	93	93	94	DCMI_VSYNC/ EVENT0
LQFP144	LQFP144	137	137	138	DCMI_VSYNC/ EVENT0
UFBGA169	LQFP144	D6	D6	B5	DCMI_VSYNC/ EVENT0
LQFP176	LQFP176	165	165	166	DCMI_VSYNC/ EVENT0
UFBGA176+25	UFBGA176+25	B5	B5	D6	DCMI_VSYNC/ EVENT0
VQFPN68	VQFPN68	61	61	62	DCMI_VSYNC/ EVENT0
		PB7	I/O	FT_fa	
		BOOT0	I	B	
E9					TIM17_CH1N, I3C1_SDA, I2C1_SDA, I2C4_SDA, US LPUART1_RX, F SDMMC2_D5, SD FMC_N DCMI_VSYNC/ EVENT0
					TIM16_CH1, T I3C1_SCL, I2C1_S I2C4_SCL, SD UART4_RX, FC SDMMC2_D4, ET SDMMC1 DCMI_D6/PSSI_D
					TIM17_CH1, T I3C1_SDA, I2C1_S SPI2_NSS/I2S2_V SDMMC1_CDIR, FDCAN1_TX, S SDMMC2_CKIN, S DCMI_D7/PSSI_D
					LPTIM1_ETR, LPTIM2_CH2, LI SPI3_RDY, UA FDCAN1_RX, SA FMC_NBL0, DCMI EVENT0



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

	Pin number ⁽¹⁾⁽²⁾												Pin name (function after reset) ⁽³⁾⁽⁴⁾	Pin type	I/O structure	Notes	Alternate f	
	WLCSP80 SMPs	LQFP100 SMPs	LQFP144 SMPs	UFBGA169 SMPs	LQFP176 SMPs	UFBGA176+25 SMPs	LQFP64	LQFP100	LQFP144	UFBGA169	LQFP176	UFBGA176+25						VQFPN68
-	-	-	141	C5	170	B4	-	-	-	D5	170	A3	-	PE1	I/O	FT_h	-	LPTIM1_IN2, L FDCAN1_TX, F DCMI_D3/PSSI_D
A9	98	142	A4	A4	171	A3	62	98	142	B4	171	C6	66	VCAP	S	-	-	-
-	99	143	-	-	-	-	63	99	143	B3	-	-	67	VSS	S	-	-	-
-	100	144	-	-	172	-	64	100	144	A3	172	-	68	VDD	S	-	-	-
-	-	-	-	C4	173	B3	-	-	-	C4	173	D4	-	P14	I/O	FT_h	-	TIM8_BKIN, S SAI2_MC DCMI_D5/PSSI_D
-	-	-	-	B3	174	A2	-	-	-	-	174	C4	-	P15	I/O	FT_h	-	TIM8_CH1, SA DCMI_VSYNC/ EVENT
-	-	-	-	A2	175	C4	-	-	-	C3	175	C3	-	P16	I/O	FT_h	-	TIM8_CH2, SA/ DCMI_D6/PSSI_D
-	-	-	-	A1	176	A1	-	-	-	A2	176	C2	-	P17	I/O	FT_h	-	TIM8_CH3, SA/ DCMI_D7/PSSI_D
-	-	-	-	-	-	F6	-	-	-	-	-	F6	-	VSS	S	-	-	-
-	-	-	-	-	-	F7	-	-	-	-	-	F7	-	VSS	S	-	-	-
-	-	-	-	-	-	F8	-	-	-	-	-	F8	-	VSS	S	-	-	-
-	-	-	-	-	-	F9	-	-	-	-	-	F9	-	VSS	S	-	-	-
-	-	-	-	-	-	F10	-	-	-	-	-	F10	-	VSS	S	-	-	-
-	-	-	-	-	-	G6	-	-	-	-	-	G6	-	VSS	S	-	-	-
-	-	-	-	-	-	G7	-	-	-	-	-	G7	-	VSS	S	-	-	-
-	-	-	-	-	-	G8	-	-	-	-	-	G8	-	VSS	S	-	-	-



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continue)

Pin number ⁽¹⁾⁽²⁾	Pin name (function after reset) ⁽³⁾⁽⁴⁾												Pin type	I/O structure	Notes	Alternate f	
	WLCSP80 SMPS	LQFP100 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP176 SMPS	UFBGA176+25 SMPS	LQFP64	LQFP100	LQFP144	UFBGA169	LQFP176	UFBGA176+25					VQFPN68
-	-	-	-	-	-	-	-	-	-	-	-	-	-	S	-	-	-
-	-	-	-	-	-	-	G9	-	-	-	-	G9	-	S	-	-	-
-	-	-	-	-	-	-	G10	-	-	-	-	G10	-	S	-	-	-
-	-	-	-	-	-	-	H6	-	-	-	-	H6	-	S	-	-	-
-	-	-	-	-	-	-	H7	-	-	-	-	H7	-	S	-	-	-
-	-	-	-	-	-	-	H8	-	-	-	-	H8	-	S	-	-	-
-	-	-	-	-	-	-	H9	-	-	-	-	H9	-	S	-	-	-
-	-	-	-	-	-	-	H10	-	-	-	-	H10	-	S	-	-	-
-	-	-	-	-	-	-	J6	-	-	-	-	J6	-	S	-	-	-
-	-	-	-	-	-	-	J7	-	-	-	-	J7	-	S	-	-	-
-	-	-	-	-	-	-	J8	-	-	-	-	J8	-	S	-	-	-
-	-	-	-	-	-	-	J9	-	-	-	-	J9	-	S	-	-	-
-	-	-	-	-	-	-	J10	-	-	-	-	J10	-	S	-	-	-
-	-	-	-	-	-	-	K6	-	-	-	-	K6	-	S	-	-	-
-	-	-	-	-	-	-	K7	-	-	-	-	K7	-	S	-	-	-
-	-	-	-	-	-	-	K8	-	-	-	-	K8	-	S	-	-	-
-	-	-	-	-	-	-	K9	-	-	-	-	K9	-	S	-	-	-
-	-	-	-	-	-	-	K10	-	-	-	-	K10	-	S	-	-	-

1. The devices with SMPS correspond to commercial code STM32H5631xxQ.

2. A non-connected I/O in a given package is configured as an output tied to VSS. When VREF+ pad is not available on a package, the (VREFBUF) is not available and must be kept disabled.

3. PC13, PC14 and PC15 are supplied through the power switch (by VSM). This switch sinks a limited amount of current, hence the use is limited: The speed must not exceed 2 MHz with a maximum load of 30 pF. These GPIOs must not be used as current sources (for



4.3

Alternate functions

Table 15. Alternate function AF0 to AF7⁽¹⁾

Port	AF0	AF1	AF2	AF3	AF4	AF5
	SYS	LPTIM1/ TIM1/2/16/17	LPTIM3/ PDM_SAI1/ TIM3/4/5/12/15	I3C1/LPTIM2/3/ LPUART1/ OCTOSPI/TIM1/8	CEC/DCMI/ I2C1/2/3/4/ LPTIM1/2/SPI1/ I2S1/TIM15/ USART1	CEC/I3C1/LPTIM1/ SPI1/I2S1/SPI2/I2S3/ SPI3/I2S3/SPI4/5/6
PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	TIM15_BKIN	SPI6_NSS
PA1	-	TIM2_CH2	TIM5_CH2	-	TIM15_CH1N	LPTIM1_IN1
PA2	-	TIM2_CH3	TIM5_CH3	-	TIM15_CH1	LPTIM1_IN2
PA3	-	TIM2_CH4	TIM5_CH4	OCTOSPI1_CLK	TIM15_CH2	SPI2_NSS/I2S2_WS
PA4	-	-	TIM5_ETR	LPTIM2_CH1	-	SPI1_NSS/I2S1_WS
PA5	-	TIM2_CH1	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK
PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO/I2S1_SD
PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SD
PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	SPI1_RDY
PA9	-	TIM1_CH2	-	LPUART1_TX	I2C3_SMBA	SPI2_SCK/I2S2_CK
PA10	-	TIM1_CH3	-	LPUART1_RX	LPTIM2_IN2	-
PA11	-	TIM1_CH4	-	LPUART1_CTS	-	SPI2_NSS/I2S2_WS
PA12	-	TIM1_ETR	-	LPUART1_RTS/ LPUART1_DE	-	SPI2_SCK/I2S2_CK
PA13	JTMS/SWDIO	-	-	-	-	-
PA14	JTCK/SWCLK	-	-	-	-	-
PA15	JTDI	TIM2_CH1	LPTIM3_IN2	-	HDMI_CEC	SPI1_NSS/I2S1_WS

Port A





Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5
	SYS	LPTIM1/ TIM1/2/16/17	LPTIM3/ PDM_SAI1/ TIM3/4/5/12/15	I3C1/LPTIM2/3/ LPUART1/ OCTOSPI/TIM1/8	CEC/DCMI/ I2C1/2/3/4/ LPTIM1/2/SPI1/ I2S1/TIM15/ USART1	CEC/I3C1/LPTIM1/ SPI1/I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/5/6
PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-
PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-
PB2	RTC_OUT2	-	SAI1_D1	TIM8_CH4N	SPI1_RDY	LPTIM1_CH1
PB3	JTDO/TRACE SWO	TIM2_CH2	-	-	I2C2_SDA	SPI1_SCK/I2S1_CK
PB4	NJTRST	TIM16_BKIN	TIM3_CH1	OCTOSPI1_CLK	LPTIM1_CH2	SPI1_MISO/I2S1_SD
PB5	-	TIM17_BKIN	TIM3_CH2	OCTOSPI1_NCLK	I2C1_SMBA	SPI1_MOS/I2S1_SD
PB6	-	TIM16_CH1N	TIM4_CH1	I3C1_SCL	I2C1_SCL	HDMI_CEC
PB7	-	TIM17_CH1N	TIM4_CH2	I3C1_SDA	I2C1_SDA	-
PB8	-	TIM16_CH1	TIM4_CH3	I3C1_SCL	I2C1_SCL	SPI4_RDY
PB9	-	TIM17_CH1	TIM4_CH4	I3C1_SDA	I2C1_SDA	SPI2_NSS/I2S2_WS
PB10	-	TIM2_CH3	LPTIM3_CH1	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK
PB11	-	TIM2_CH4	-	LPTIM2_ETR	I2C2_SDA	SPI2_RDY
PB12	-	TIM1_BKIN	-	OCTOSPI1_NCLK	I2C2_SDA	SPI2_NSS/I2S2_WS
PB13	-	TIM1_CH1N	LPTIM3_IN1	LPTIM2_CH1	I2C2_SMBA	SPI2_SCK/I2S2_CK
PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/I2S2_SD
PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOS/I2S2_SD

Port B

Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5
	SYS	LPTIM1/ TIM1/2/16/17	LPTIM3/ PDM_SAI1/ TIM3/4/5/12/15	I3C1/LPTIM2/3/ LPUART1/ OCTOSPI/TIM1/8	CEC/DCMI/ I2C1/2/3/4/ LPTIM1/2/SPI1/ I2S1/TIM15/ USART1	CEC/I3C1/LPTIM1/ SPI1/I2S1/SPI2/I2S3/ SPI3/I2S3/SPI4/5/6
PC0	-	TIM16_BKIN	-	-	-	-
PC1	TRACED0	-	SAI1_D1	-	-	SPI2_MOS/I2S2_SD
PC2	PWR_CSLEEP	TIM17_CH1	TIM4_CH4	-	-	SPI2_MISO/I2S2_SD
PC3	PWR_CSTOP	-	SAI1_D3	LPTIM3_CH1	-	SPI2_MOS/I2S2_SD
PC4	-	TIM2_CH4	SAI1_CK1	LPTIM2_ETR	-	I2S1_MCK
PC5	-	TIM1_CH4N	SAI1_D3	-	PSSI_D15	-
PC6	-	-	TIM3_CH1	TIM8_CH1	-	I2S2_MCK
PC7	TRGIO	-	TIM3_CH2	TIM8_CH2	-	-
PC8	TRACED1	-	TIM3_CH3	TIM8_CH3	-	-
PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	AUDIOCLK
PC10	-	-	LPTIM3_ETR	-	-	-
PC11	-	-	LPTIM3_IN1	-	-	-
PC12	TRACED3	-	TIM15_CH1	-	-	SPI6_SCK
PC13	-	-	-	-	-	-
PC14	-	-	-	-	-	-
PC15	-	-	-	-	-	-

Port C





Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5
	SYS	LPTIM1/ TIM1/2/16/17	LPTIM3/ PDM_SAI1/ TIM3/4/5/12/15	I3C1/LPTIM2/3/ LPUART1/ OCTOSPI/TIM1/8	CEC/DCMI/ I2C1/2/3/4/ LPTIM1/2/SPI1/ I2S1/TIM15/ USART1	CEC/I3C1/LPTIM1/ SPI1/I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/5/6
Port D						
PD0	-	-	-	TIM8_CH4N	-	-
PD1	-	-	-	-	-	-
PD2	TRACED2	-	TIM3_ETR	-	TIM15_BKIN	-
PD3	-	-	-	-	-	SPI2_SCK/I2S2_CK
PD4	-	-	-	-	-	-
PD5	-	TIM1_CH4N	-	-	-	SPI2_RDY
PD6	-	-	SAI1_D1	-	-	SPI3_MOSI/I2S3_SD
PD7	-	-	-	-	-	SPI1_MOSI/I2S1_SD
PD8	-	-	-	-	-	-
PD9	-	-	-	-	-	-
PD10	-	-	-	LPTIM2_CH2	-	-
PD11	-	-	SAI1_CK1	LPTIM2_IN2	I2C4_SMBA	-
PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	I2C4_SCL	I3C1_SCL
PD13	-	LPTIM1_CH1	TIM4_CH2	LPTIM2_CH1	I2C4_SDA	I3C1_SDA
PD14	-	-	TIM4_CH3	-	-	-
PD15	-	-	TIM4_CH4	-	-	-

Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5
	SYS	LPTIM1/ TIM1/2/16/17	LPTIM3/ PDM_SAI1/ TIM3/4/5/12/15	I3C1/LPTIM2/3/ LPUART1/ OCTOSPI/TIM1/8	CEC/DCMI/ I2C1/2/3/4/ LPTIM1/2/SPI1/ I2S1/TIM15/ USART1	CEC/I3C1/LPTIM1/ SPI1/I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/5/6
PE0	-	LPTIM1_ETR	TIM4_ETR	LPTIM2_CH2	LPTIM2_ETR	-
PE1	-	LPTIM1_IN2	-	-	-	-
PE2	TRACECLK	LPTIM1_IN2	SAI1_CK1	-	-	SPI4_SCK
PE3	TRACED0	-	-	-	TIM15_BKIN	-
PE4	TRACED1	-	SAI1_D2	-	TIM15_CH1N	SPI4_NSS
PE5	TRACED2	-	SAI1_CK2	-	TIM15_CH1	SPI4_MISO
PE6	TRACED3	TIM1_BKIN2	SAI1_D1	-	TIM15_CH2	SPI4_MOSI
PE7	-	TIM1_ETR	-	-	-	-
PE8	-	TIM1_CH1N	-	-	-	-
PE9	-	TIM1_CH1	-	-	-	-
PE10	-	TIM1_CH2N	-	-	-	-
PE11	-	TIM1_CH2	-	-	SPI1_RDY	SPI4_NSS
PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK
PE13	-	TIM1_CH3	-	-	-	SPI4_MISO
PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI
PE15	-	TIM1_BKIN	-	TIM1_CH4N	-	-

Port E





Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5
	SYS	LPTIM1/ TIM1/2/16/17	LPTIM3/ PDM_SAI1/ TIM3/4/5/12/15	I3C1/LPTIM2/3/ LPUART1/ OCTOSPI/TIM1/8	CEC/DCMI/ I2C1/2/3/4/ LPTIM1/2/SPI1/ I2S1/TIM15/ USART1	CEC/I3C1/LPTIM1/ SPI1/I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/5/6
PF0	-	-	-	-	I2C2_SDA	-
PF1	-	-	-	-	I2C2_SCL	-
PF2	-	-	LPTIM3_CH2	LPTIM3_IN2	I2C2_SMBA	-
PF3	-	-	LPTIM3_IN1	-	-	-
PF4	-	-	LPTIM3_ETR	-	-	-
PF5	-	-	LPTIM3_CH1	-	I2C4_SCL	I3C1_SCL
PF6	-	TIM16_CH1	-	-	-	SPI5_NSS
PF7	-	TIM17_CH1	-	-	-	SPI5_SCK
PF8	-	TIM16_CH1N	-	-	-	SPI5_MISO
PF9	-	TIM17_CH1N	-	-	-	SPI5_MOSI
PF10	-	TIM16_BKIN	SAI1_D3	-	PSSI_D15	-
PF11	-	-	-	-	-	SPI5_MOSI
PF12	-	-	-	-	-	-
PF13	-	-	-	-	I2C4_SMBA	-
PF14	-	-	-	-	-	-
PF15	-	-	-	-	I2C4_SDA	I3C1_SDA

Port F

Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5
	SYS	LPTIM1/ TIM1/2/16/17	LPTIM3/ PDM_SAI1/ TIM3/4/5/12/15	I3C1/LPTIM2/3/ LPUART1/ OCTOSPI/TIM1/8	CEC/DCMI/ I2C1/2/3/4/ LPTIM1/2/SPI1/ I2S1/TIM15/ USART1	CEC/I3C1/LPTIM1/ SPI1/I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/5/6
PG0	-	-	-	-	-	-
PG1	-	-	-	-	-	-
PG2	-	-	-	TIM8_BKIN	-	-
PG3	-	-	-	TIM8_BKIN2	-	-
PG4	-	TIM1_BKIN2	-	-	-	-
PG5	-	TIM1_ETR	-	-	-	-
PG6	-	TIM17_BKIN	-	I3C1_SDA	I2C4_SDA	SPI1_RDY
PG7	-	-	SAI1_CK2	I3C1_SCL	I2C4_SCL	-
PG8	-	-	-	TIM8_ETR	-	SPI6_NSS
PG9	-	-	-	-	-	SPI1_MISO/I2S1_SD
PG10	-	-	-	-	-	SPI1_NSS/I2S1_WS
PG11	-	LPTIM1_IN2	-	-	-	SPI1_SCK/I2S1_Ck
PG12	-	LPTIM1_IN1	-	-	PSSI_D15	SPI6_MISO
PG13	TRACED0	LPTIM1_CH1	-	-	-	SPI6_SCK
PG14	TRACED1	LPTIM1_ETR	-	-	LPTIM1_CH2	SPI6_MOSI
PG15	-	-	-	-	-	SPI4_RDY

Port G





Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5
	SYS	LPTIM1/ TIM1/2/16/17	LPTIM3/ PDM_SAI1/ TIM3/4/5/12/15	I3C1/LPTIM2/3/ LPUART1/ OCTOSPI/TIM1/8	CEC/DCMI/ I2C1/2/3/4/ LPTIM1/2/SPI1/ I2S1/TIM15/ USART1	CEC/I3C1/LPTIM1/ SPI1/I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/5/6
PH0	-	-	-	-	-	-
PH1	-	-	-	-	-	-
PH2	-	LPTIM1_IN2	-	-	-	-
PH3	-	-	-	-	-	-
PH4	-	-	-	-	I2C2_SCL	SPI5_RDY
PH5	-	-	-	-	I2C2_SDA	SPI5_NSS
PH6	-	TIM1_CH3N	TIM12_CH1	TIM8_CH1	I2C2_SMBA	SPI5_SCK
PH7	-	TIM1_CH3	-	TIM8_CH1N	I2C3_SCL	SPI5_MISO
PH8	-	TIM1_CH2N	TIM5_ETR	TIM8_CH2	I2C3_SDA	SPI5_MOSI
PH9	-	TIM1_CH2	TIM12_CH2	TIM8_CH2N	I2C3_SMBA	SPI5_NSS
PH10	-	TIM1_CH1N	TIM5_CH1	TIM8_CH3	I2C4_SMBA	SPI5_RDY
PH11	-	TIM1_CH1	TIM5_CH2	TIM8_CH3N	I2C4_SCL	I3C1_SCL
PH12	-	TIM1_BKIN	TIM5_CH3	TIM8_BKIN	I2C4_SDA	I3C1_SDA
PH13	-	LPTIM1_IN2	-	TIM8_CH1N	-	-
PH14	-	-	-	TIM8_CH2N	-	-
PH15	-	-	-	TIM8_CH3N	-	-

Port H

Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5
	SYS	LPTIM1/ TIM1/2/16/17	LPTIM3/ PDM_SAI1/ TIM3/4/5/12/15	I3C1/LPTIM2/3/ LPUART1/ OCTOSPI/TIM1/8	CEC/DCMI/ I2C1/2/3/4/ LPTIM1/2/SPI1/ I2S1/TIM15/ USART1	CEC/I3C1/LPTIM1/ SPI1/I2S1/SPI2/I2S2/ SPI3/I2S3/SPI4/5/6
Pi0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS
Pi1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK
Pi2	-	-	-	TIM8_CH4	-	SPI2_MISO/I2S2_SD
Pi3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SD
Pi4	-	-	-	TIM8_BKIN	-	-
Pi5	-	-	-	TIM8_CH1	-	-
Pi6	-	-	-	TIM8_CH2	-	-
Pi7	-	-	-	TIM8_CH3	-	-
Pi8	-	-	-	-	-	-
Pi9	-	-	-	-	-	-
Pi10	-	-	-	-	-	-
Pi11	-	-	-	-	-	-

1. Refer to the next table for AF8 to AF15.



Table 16. Alternate function AF8 to AF15(1)

Port	AF8	AF9	AF10	AF11	AF12	AF13
	LPUART1/SAI2 /SDMMC1/SPI6 /UART4/5/8	FDCAN1/2/FMC [NAND16]/FMC [NORmux]/FMC [NOR_RAM]/ OCTOSPI/SDMM C2/TIM13/14	CRS/FMC[NAND 16]/OCTOSPI/S AI2/SDMMC2/ TIM8/USB_PD	ETH[MII/RMII]/ FMC[NAND16]/ OCTOSPI/ SDMMC2/ UART7/9/USB_PD	FMC[NAND16]/ FMC[NORmux]/ FMC[NOR_RAM]/ FMC[SDRAM_16bit] /SDMMC1	DCMI/FMC[N FMC[NOR FMC[NOR_ LPTIM
PA0	UART4_TX	SDMMC2_CMD	SAI2_SD_B	ETH_MII_CRS	-	-
PA1	UART4_RX	OCTOSPI1_IO3	SAI2_MCLK_B	ETH_MII_RX_CLK /ETH_RMII_REF_ CLK	-	-
PA2	SAI2_SCK_B	-	-	ETH_MDIO	-	-
PA3	-	-	-	ETH_MII_COL	-	-
PA4	SPI6_NSS	-	-	-	-	DCMI_HS PSSI_L
PA5	SPI6_SCK	-	-	ETH_MII_TX_EN/ ETH_RMII_TX_EN	-	PSSI_D
PA6	SPI6_MISO	TIM13_CH1	-	-	-	DCMI_PIX PSSI_PD
PA7	SPI6_MOSI	TIM14_CH1	OCTOSPI1_IO2	ETH_MII_RX_DV/ ETH_RMII_CRS_ DV	FMC_SDNWE	FMC_N
PA8	-	-	USB_SOF	UART7_RX	FMC_NOE	DCMI_D3/P
PA9	-	-	-	ETH_MII_TX_ER	FMC_NWE	DCMI_D0/P
PA10	-	FDCAN2_TX	-	-	SDMMC1_D0	DCMI_D1/P
PA11	-	FDCAN1_RX	USB_DM	-	-	-
PA12	SAI2_FS_B	FDCAN1_TX	USB_DP	-	-	-
PA13	-	-	-	-	-	-
PA14	-	-	-	-	-	-
PA15	UART4_RTS/ UART4_DE	-	-	UART7_TX	FMC_NBL1	DCMI_D11/P

Port A

Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port	AF8	AF9	AF10	AF11	AF12	AF13
	LPUART1/SAI2 /SDMMC1/SPI6 /UART4/5/8	FDCAN1/2/FMC [NAND16]/FMC [NORmux]/FMC [NOR_RAM]/ OCTOSPI/SDMM C2/TIM13/14	CRS/FMC[NAND 16]/OCTOSPI/S AI2/SDMMC2/ TIM8/USB_PD	ETH[MII/RMII]/ FMC[NAND16]/ OCTOSPI/ SDMMC2/ UART7/9/USB_PD	FMC[NAND16]/ FMC[NORmux]/ FMC[NOR_RAM]/ FMC[SDRAM_16bit] /SDMMC1	DCMI/FMC[N FMC[NOR FMC[NOR_ LPTIM
PB0	UART4_CTS	-	-	ETH_MII_RXD2	-	-
PB1	-	-	-	ETH_MII_RXD3	-	-
PB2	-	OCTOSPI1_CLK	OCTOSPI1_DQS	-	SDMMC1_CMD	LPTIM5
PB3	SPI6_SCK	SDMMC2_D2	CRS_SYNC	UART7_RX	-	-
PB4	SPI6_MISO	SDMMC2_D3	-	UART7_TX	-	DCMI_D7/P
PB5	SPI6_MOSI	FDCAN2_RX	-	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10/P
PB6	LPUART1_TX	FDCAN2_TX	OCTOSPI1_NCS	-	FMC_SDNE1	DCMI_D5/P
PB7	LPUART1_RX	FDCAN1_TX	SDMMC2_D5	SDMMC2_CKIN	FMC_NL	DCMI_VS PSSI_R
PB8	UART4_RX	FDCAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC1_D4	DCMI_D6/P
PB9	UART4_TX	FDCAN1_TX	SDMMC2_D5	SDMMC2_CKIN	SDMMC1_D5	DCMI_D7/P
PB10	-	OCTOSPI1_NCS	-	ETH_MII_RX_ER	-	-
PB11	-	-	-	ETH_MII_TX_EN/ ETH_RMII_TX_EN	FMC_NBL1	-
PB12	-	FDCAN2_RX	-	ETH_MII_TXD0/ ETH_RMII_TXD0	-	-
PB13	-	FDCAN2_TX	-	-	SDMMC1_D0	-
PB14	UART4_RTS/ UART4_DE	SDMMC2_D0	-	-	-	-
PB15	UART4_CTS	SDMMC2_D1	OCTOSPI1_CLK	ETH_MII_TXD1/ ETH_RMII_TXD1	-	DCMI_D2/P





Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port	AF8	AF9	AF10	AF11	AF12	AF13
	LPUART1/SAI2/SDMMC1/SPI6/UART4/5/8	FDCAN1/2/FMC[NAND16]/FMC[NORMux]/FMC[NOR_RAM]/OCTOSPI/SDMMC2/TIM13/14	CRS/FMC[NAND16]/OCTOSPI/S AI2/SDMMC2/TIM8/USB_PD	ETH[MII/RMII]/FMC[NAND16]/OCTOSPI/SDMMC2/UART7/9/USB_PD	FMC[NAND16]/FMC[NORMux]/FMC[NOR_RAM]/FMC[SDRAM_16bit]/SDMMC1	DCMI/FMC[NOR_FMC[NOR_LPTIM
PC0	SAI2_FS_B	FMC_A25	OCTOSPI1_IO7	-	FMC_SDNWE	-
PC1	SAI2_SD_A	SDMMC2_CK	OCTOSPI1_IO4	ETH_MDC	-	-
PC2	-	OCTOSPI1_IO2	-	ETH_MII_TXD2	FMC_SDNE0	-
PC3	-	OCTOSPI1_IO0	-	ETH_MII_TX_CLK	FMC_SDCKE0	-
PC4	-	-	-	ETH_MII_RXD0/ ETH_RMII_RXD0	FMC_SDNE0	-
PC5	-	-	OCTOSPI1_DQS	ETH_MII_RXD1/ ETH_RMII_RXD1	FMC_SDCKE0	-
PC6	SDMMC1_D0DIR	FMC_NWAIT	SDMMC2_D6	OCTOSPI1_IO5	SDMMC1_D6	DCMI_D0/P
PC7	SDMMC1_D123DIR	FMC_NE1	SDMMC2_D7	OCTOSPI1_IO6	SDMMC1_D7	DCMI_D1/P
PC8	UART5_RTS/ UART5_DE	FMC_NE2/ FMC_NCE	FMC_INT	FMC_ALE	SDMMC1_D0	DCMI_D2/P
PC9	UART5_CTS	OCTOSPI1_IO0	-	FMC_CLE	SDMMC1_D1	DCMI_D3/P
PC10	UART4_TX	OCTOSPI1_IO1	-	ETH_MII_TXD0/ ETH_RMII_TXD0	SDMMC1_D2	DCMI_D8/P
PC11	UART4_RX	OCTOSPI1_NCS	-	-	SDMMC1_D3	DCMI_D4/P
PC12	UART5_TX	-	-	-	SDMMC1_CK	DCMI_D9/P
PC13	-	-	-	-	-	-
PC14	-	-	-	-	-	-
PC15	-	-	-	-	-	-

Port C

Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port	AF8	AF9	AF10	AF11	AF12	AF13
	LPUART1/SAI2 /SDMMC1/SPI6 /UART4/5/8	FDCAN1/2/FMC [NAND16]/FMC [NORmux]/FMC [NOR_RAM]/ OCTOSPI/SDMM C2/TIM13/14	CRS/FMC[NAND 16]/OCTOSPI/S AI2/SDMMC2/ TIM8/USB_PD	ETH[MII/RMII]/ FMC[NAND16]/ OCTOSPI/ SDMMC2/ UART7/9/USB_PD	FMC[NAND16]/ FMC[NORmux]/ FMC[NOR_RAM]/ FMC[SDRAM_16bit] /SDMMC1	DCMI/FMC[N FMC[NOR FMC[NOR_ LPTIM
PD0	UART4_RX	FDCAN1_RX	-	UART9_CTS	FMC_D2/FMC_AD2	-
PD1	UART4_TX	FDCAN1_TX	-	-	FMC_D3/FMC_AD3	-
PD2	UART5_RX	-	-	-	SDMMC1_CMD	DCMI_D11/P
PD3	-	-	-	-	FMC_CLK	DCMI_D5/P
PD4	-	-	OCTOSPI1_IO4	-	FMC_NOE	-
PD5	-	FDCAN1_TX	OCTOSPI1_IO5	-	FMC_NWE	-
PD6	-	-	OCTOSPI1_IO6	SDMMC2_CK	FMC_NWAIT	DCMI_D10/P
PD7	-	-	OCTOSPI1_IO7	SDMMC2_CMD	FMC_NE1/ FMC_NCE	-
PD8	-	-	-	-	FMC_D13/ FMC_AD13	-
PD9	-	FDCAN2_RX	-	-	FMC_D14/ FMC_AD14	-
PD10	-	-	-	-	FMC_D15/ FMC_AD15	-
PD11	UART4_RX	OCTOSPI1_IO0	SAI2_SD_A	-	FMC_A16/FMC_CLE	-
PD12	UART4_TX	OCTOSPI1_IO1	SAI2_FS_A	-	FMC_A17/FMC_ALE	DCMI_D12/P
PD13	-	OCTOSPI1_IO3	SAI2_SCK_A	UART9_RTS/ UART9_DE	FMC_A18	DCMI_D13/P
PD14	UART8_CTS	-	-	UART9_RX	FMC_D0/FMC_AD0	-
PD15	UART8_RTS/ UART8_DE	-	-	UART9_TX	FMC_D1/FMC_AD1	-

Port D



Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port	AF8	AF9	AF10	AF11	AF12	AF13
	LPUART1/SAI2 /SDMMC1/SPI6 /UART4/5/8	FDCAN1/2/FMC [NAND16]/FMC [NORmux]/FMC [NOR_RAM]/ OCTOSPI/SDMM C2/TIM13/14	CRS/FMC[NAND 16]/OCTOSPI/S AI2/SDMMC2/ TIM8/USB_PD	ETH[MII/RMII]/ FMC[NAND16]/ OCTOSPI/ SDMMC2/ UART7/9/USB_PD	FMC[NAND16]/ FMC[NORmux]/ FMC[NOR_RAM]/ FMC[SDRAM_16bit] /SDMMC1	DCMI/FMC[N FMC[NOR FMC[NOR_ LPTIM
PE0	UART8_RX	FDCAN1_RX	SAI2_MCLK_A	-	FMC_NBL0	DCMI_D2/P
PE1	UART8_TX	FDCAN1_TX	-	-	FMC_NBL1	DCMI_D3/P
PE2	UART8_TX	OCTOSPI1_IO2	-	ETH_MII_TXD3	FMC_A23	DCMI_D3/P
PE3	-	-	-	-	FMC_A19	-
PE4	-	-	-	-	FMC_A20	DCMI_D4/P
PE5	-	-	-	-	FMC_A21	DCMI_D6/P
PE6	-	-	SAI2_MCLK_B	-	FMC_A22	DCMI_D7/P
PE7	-	-	OCTOSPI1_IO4	-	FMC_D4/FMC_AD4	-
PE8	-	-	OCTOSPI1_IO5	-	FMC_D5/FMC_AD5	-
PE9	-	-	OCTOSPI1_IO6	-	FMC_D6/FMC_AD6	-
PE10	-	-	OCTOSPI1_IO7	-	FMC_D7/FMC_AD7	-
PE11	-	-	SAI2_SD_B	-	FMC_D8/FMC_AD8	-
PE12	-	-	SAI2_SCK_B	-	FMC_D9/FMC_AD9	-
PE13	-	-	SAI2_FS_B	-	FMC_D10/ FMC_AD10	-
PE14	-	-	SAI2_MCLK_B	-	FMC_D11/ FMC_AD11	-
PE15	-	-	-	-	FMC_D12/ FMC_AD12	-

Port F

Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port	AF8	AF9	AF10	AF11	AF12	AF13
	LPUART1/SAI2 /SDMMC1/SPI6 /UART4/5/8	FDCAN1/2/FMC [NAND16]/FMC [NORmux]/FMC [NOR_RAM]/ OCTOSPI/SDMM C2/TIM13/14	CRS/FMC{NAND 16}/OCTOSPI/S AI2/SDMMC2/ TIM8/USB_PD	ETH{MII/RMII}/ FMC{NAND16}/ OCTOSPI/ SDMMC2/ UART7/9/USB_PD	FMC{NAND16}/ FMC{NORmux}/ FMC{NOR_RAM}/ FMC{SDRAM_16bit} /SDMMC1	DCMI/FMC{N FMC{NOR FMC{NOR_ LPTIM5
PF0	-	-	-	-	FMC_A0	LPTIM5_
PF1	-	-	-	-	FMC_A1	LPTIM5_
PF2	-	-	-	-	FMC_A2	LPTIM5_
PF3	-	-	-	-	FMC_A3	LPTIM5_
PF4	-	-	-	-	FMC_A4	-
PF5	-	-	-	-	FMC_A5	-
PF6	-	-	OCTOSPI1_IO3	-	-	LPTIM5_
PF7	-	-	OCTOSPI1_IO2	-	-	LPTIM5_
PF8	-	TIM13_CH1	OCTOSPI1_IO0	-	-	LPTIM5_
PF9	-	TIM14_CH1	OCTOSPI1_IO1	-	-	LPTIM5_
PF10	-	OCTOSPI1_CLK	-	-	-	DCMI_D11/P
PF11	-	OCTOSPI1_NCLK	SAI2_SD_B	-	FMC_NRAS	DCMI_D12/P
PF12	-	-	-	-	FMC_A6	-
PF13	-	-	-	-	FMC_A7	-
PF14	-	-	-	-	FMC_A8	-
PF15	-	-	-	-	FMC_A9	-

Port F





Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port	AF8	AF9	AF10	AF11	AF12	AF13
	LPUART1/SAI2 /SDMMC1/SPI6 /UART4/5/8	FDCAN1/2/FMC [NAND16]/FMC [NORmux]/FMC [NOR_RAM]/ OCTOSPI/SDMM C2/TIM13/14	CRS/FMC[NAND 16]/OCTOSPI/S AI2/SDMMC2/ TIM8/USB_PD	ETH[RMII/RMII]/ FMC[NAND16]/ OCTOSPI/ SDMMC2/ UART7/9/USB_PD	FMC[NAND16]/ FMC[NORmux]/ FMC[NOR_RAM]/ FMC[SDRAM_16bit] /SDMMC1	DCMI/FMC[N FMC[NOR FMC[NOR_ LPTIM5_
PG0	-	-	-	UART9_RX	FMC_A10	-
PG1	-	-	-	UART9_TX	FMC_A11	-
PG2	-	-	-	-	FMC_A12	-
PG3	-	-	-	-	FMC_A13	LPTIM5_
PG4	-	-	-	-	FMC_A14/FMC_BA0	-
PG5	-	-	-	-	FMC_A15/FMC_BA1	-
PG6	-	-	OCTOSPI1_NCS	UCPD1_FRSTX	FMC_NE3	DCMI_D12/P
PG7	-	-	-	UCPD1_FRSTX	FMC_INT	DCMI_D13/P
PG8	-	-	-	ETH_PPS_OUT	FMC_SDCLK	-
PG9	-	OCTOSPI1_IO6	SAI2_FS_B	SDMMC2_D0	FMC_NE2/ FMC_NCE	DCMI_VS PSSI_R
PG10	-	-	SAI2_SD_B	SDMMC2_D1	FMC_NE3	DCMI_D2/P
PG11	-	-	SDMMC2_D2	ETH_MII_TX_EN/ ETH_RMII_TX_EN	-	DCMI_D3/P
PG12	-	-	SDMMC2_D3	ETH_MII_TXD1/ ETH_RMII_TXD1	FMC_NE4	DCMI_D11/P
PG13	-	-	SDMMC2_D6	ETH_MII_TXD0/ ETH_RMII_TXD0	FMC_A24	LPTIM5_
PG14	-	OCTOSPI1_IO7	SDMMC2_D7	ETH_MII_TXD1/ ETH_RMII_TXD1	FMC_A25	LPTIM5_
PG15	-	-	-	-	FMC_NCAS	DCMI_D13/P

Port G

Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port	AF8	AF9	AF10	AF11	AF12	AF13
	LPUART1/SAI2 /SDMMC1/SPI6 /UART4/5/8	FDCAN1/2/FMC [NAND16]/FMC [NORmux]/FMC [NOR_RAM]/ OCTOSPI/SDMM C2/TIM13/14	CRS/FMC[NAND 16]/OCTOSPI/S AI2/SDMMC2/ TIM8/USB_PD	ETH[MII/RMII]/ FMC[NAND16]/ OCTOSPI/ SDMMC2/ UART7/9/USB_PD	FMC[NAND16]/ FMC[NORmux]/ FMC[NOR_RAM]/ FMC[SDRAM_16bit] /SDMMC1	DCMI/FMC[N FMC[NOR FMC[NOR_ LPTIM
PH0	-	-	-	-	-	-
PH1	-	-	-	-	-	-
PH2	-	OCTOSPI1_IO4	SAI2_SCK_B	ETH_MII_CRG	FMC_SDCKE0	-
PH3	-	OCTOSPI1_IO5	SAI2_MCLK_B	ETH_MII_COL	FMC_SDNE0	-
PH4	-	-	-	-	-	PSSI_D
PH5	-	-	-	-	FMC_SDNWE	-
PH6	-	-	-	ETH_MII_RXD2	FMC_SDNE1	DCMI_D8/P
PH7	-	-	-	ETH_MII_RXD3	FMC_SDCKE1	DCMI_D9/P
PH8	-	-	-	-	-	DCMI_HS PSSI_L
PH9	-	-	-	-	-	DCMI_D0/P
PH10	-	-	-	-	-	DCMI_D1/P
PH11	-	-	-	-	-	DCMI_D2/P
PH12	-	-	TIM8_CH4N	-	-	DCMI_D3/P
PH13	UART4_TX	FDCAN1_TX	-	-	-	DCMI_D3/P
PH14	UART4_RX	FDCAN1_RX	-	-	-	DCMI_D4/P
PH15	-	-	-	-	-	DCMI_D11/P

Port H





Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port	AF8	AF9	AF10	AF11	AF12	AF13
	LPUART1/SAI2 /SDMMC1/SPI6 /UART4/5/8	FDCAN1/2/FMC [NAND16]/FMC [NORMUX]/FMC [NOR_RAM]/ OCTOSPI/SDMM C2/TIM13/14	CRS/FMC[NAND 16]/OCTOSPI/S AI2/SDMMC2/ TIM8/USB_PD	ETH[MII/RMII]/ FMC[NAND16]/ OCTOSPI/ SDMMC2/ UART7/9/USB_PD	FMC[NAND16]/ FMC[NORMUX]/ FMC[NOR_RAM]/ FMC[SDRAM_16bit] /SDMMC1	DCMI/FMC[N FMC[NOR FMC[NOR_] LPTIM
P10	-	-	-	-	-	DCMI_D13/P
P11	-	-	-	-	-	DCMI_D8/P
P12	-	-	-	-	-	DCMI_D9/P
P13	-	-	-	-	-	DCMI_D10/P
P14	-	-	SAI2_MCLK_A	-	-	DCMI_D5/P
P15	-	-	SAI2_SCK_A	-	-	DCMI_VS PSSI_R
P16	-	-	SAI2_SD_A	-	-	DCMI_D6/P
P17	-	-	SAI2_FS_A	-	-	DCMI_D7/P
P18	-	-	-	-	-	-
P19	UART4_RX	FDCAN1_RX	-	-	-	-
P110	-	FDCAN1_RX	-	ETH_MII_RX_ER	-	PSSI_D
P111	-	-	-	-	-	PSSI_D

1. Refer to the previous table for AF0 to AF7.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_J = 25\text{ °C}$ and $T_J = T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes, and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_J = 25\text{ °C}$, $V_{DD} = V_{DDA} = 3.3\text{ V}$ (for the $1.71 \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

5.1.3 Typical curves

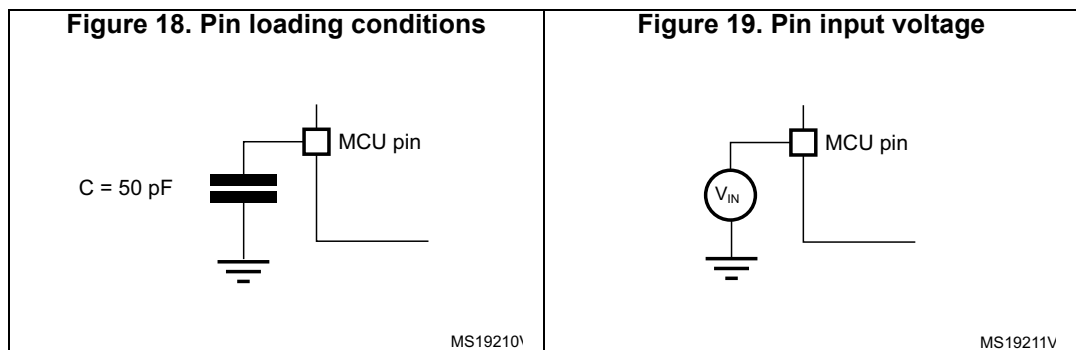
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 18](#).

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 19](#).



5.1.6 Power supply scheme

Figure 20. Power supply scheme with SMPS

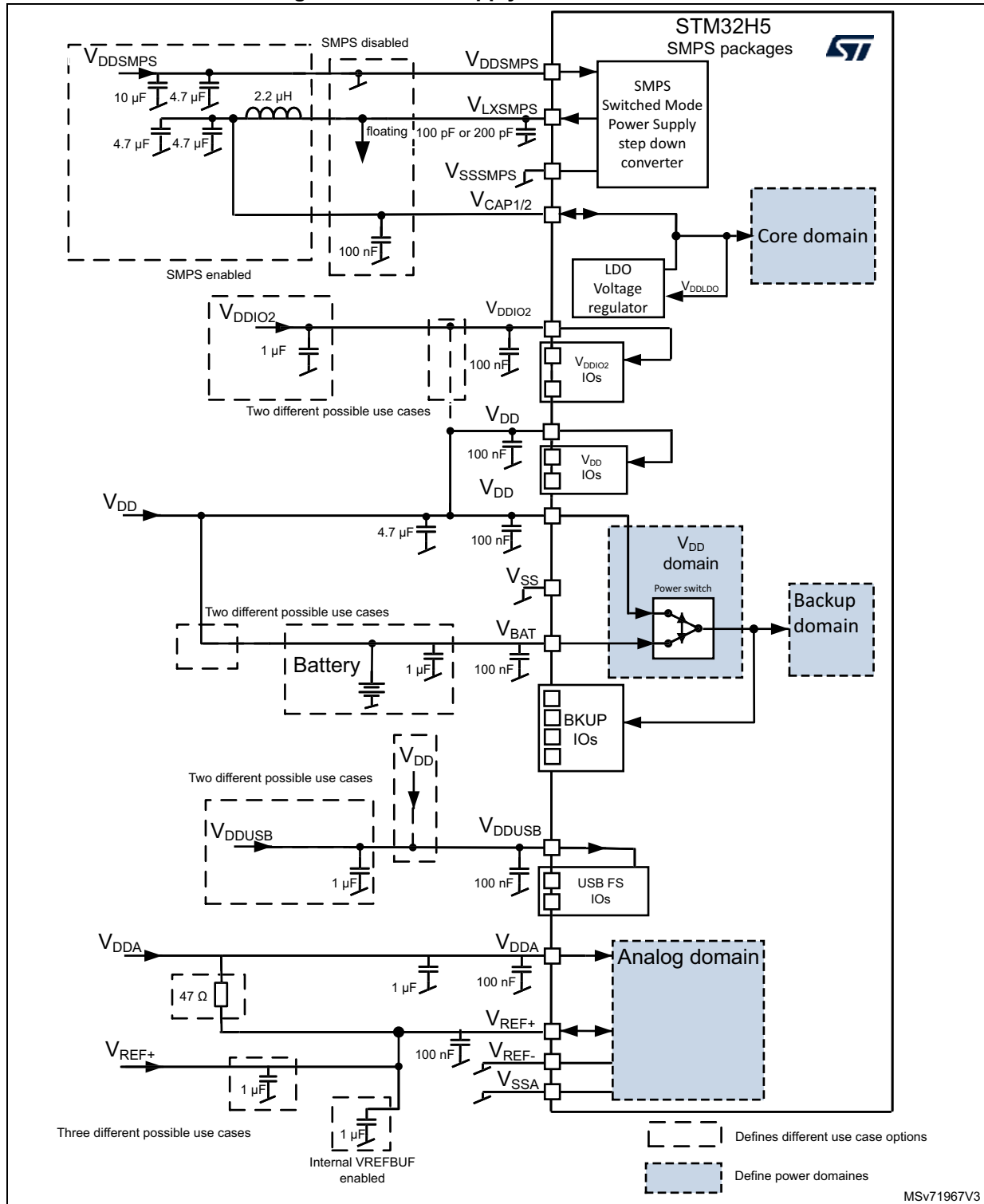
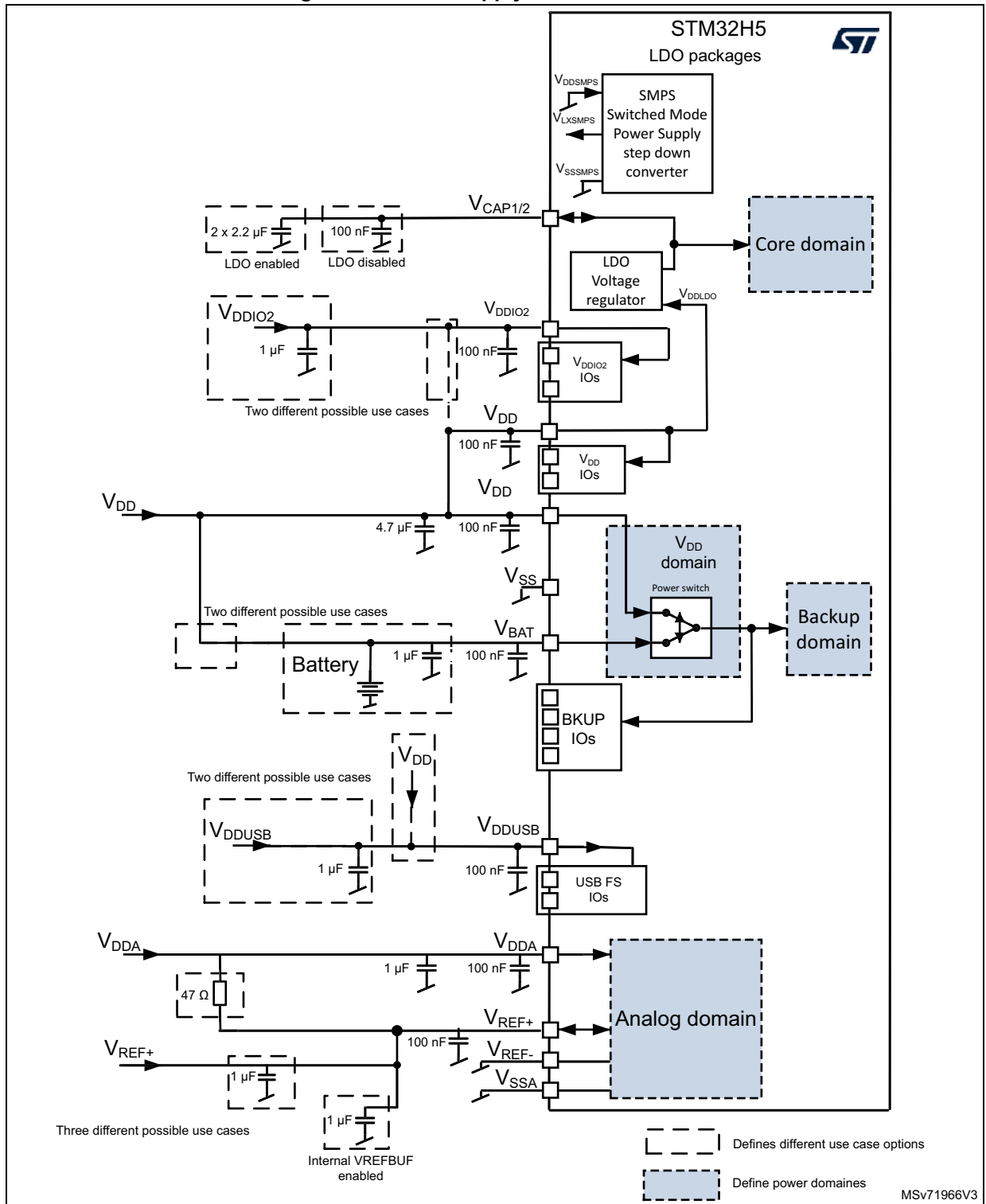


Figure 21. Power supply scheme with LDO



Note: Refer to “Getting started with STM32H5 Series hardware development” (AN5711) for more details.

Caution: Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 17](#), [Table 18](#), and [Table 19](#) may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 17. Voltage characteristics⁽¹⁾

Symbol	Ratings	Min	Max	Unit
$V_{DDx} - V_{SS}$	External main supply voltage (including $V_{DDSMPS}^{(2)}$, V_{DDA} , V_{DDUSB} , $V_{DDIO2}^{(2)(3)(4)}$, V_{BAT} , and V_{REF+})	-0.3	4.0	V
$V_{DDIOx}^{(4)} - V_{SS}$	I/O supply when HSLV ⁽²⁾ = 0	-0.3	4.0	V
	I/O supply when HSLV ⁽²⁾ = 1	-0.3	2.75	
$V_{IN}^{(5)}$	Input voltage on FT_XXX pins except FT_c pins	$V_{SS} - 0.3$	$\min(\min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0, 6.0 \text{ V})^{(6)(7)}$	V
	Input voltage on FT_t in V_{BAT} mode	$V_{SS} - 0.3$	$\min(\min(V_{BAT}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0 \text{ V}, 6.0 \text{ V})$	
	Input voltage on TT_xx pins	$V_{SS} - 0.3$	4.0	
	Input voltage on BOOT0 pin	V_{SS}	$\min(\min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0, 6.0 \text{ V})^{(6)}$	
	Input voltage on FT_c pins	$V_{SS} - 0.3$	5.5	
	Input voltage on any other pins	$V_{SS} - 0.3$	4.0	
$V_{REF+} - V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	
$ \Delta V_{DDx} $	Variations between different V_{DDx} power pins of the same domain	-	50.0	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	-	50.0	

1. All main power (V_{DD} , V_{DDA} , V_{DDUSB} , V_{DDIO2} , V_{REF+} , V_{DDSMPS} , V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. HSLV = High-speed low-voltage mode. Refer to General-purpose I/Os (GPIO) section of RM0481.
3. If HSLV = 0.
4. V_{DDIO1} or V_{DDIO2} . $V_{DDIO1} = V_{DD}$.
5. V_{IN} maximum must always be respected. Refer to the maximum allowed injected current values.
6. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
7. This formula must be applied on power supplies related to the I/O structure described by the pin definition table.

Table 18. Current characteristics

Symbol	Ratings	Max	Unit
$\Sigma I_{V_{DD}}$	Total current into sum of all V_{DD} power lines (source) ⁽¹⁾	350	mA
$\Sigma I_{V_{SS}}$	Total current out of sum of all V_{SS} ground lines (sink) ⁽¹⁾	350	
$I_{V_{DD}}$	Maximum current into each V_{DD} power pin (source) ⁽¹⁾	100	
$I_{V_{SS}}$	Maximum current out of each V_{SS} ground pin (sink) ⁽¹⁾	100	
$I_{I/O(PIN)}$	Output current sunk/sourced by any I/O and control pin	20	
$\Sigma I_{I/O(PIN)}$	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	140	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	140	
$I_{INJ(PIN)}^{(3)(4)}$	Injected current on FT_xxx, TT_xx, NRST pins	-5 / 0	
$\Sigma I_{INJ(PIN)} $	Total injected current (sum of all I/Os and control pins) ⁽⁵⁾	±25	

1. All main power (V_{DD} , V_{DDA} , V_{DDIO2} , and V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supplies, in the allowed range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os, and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 17](#) for the minimum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma |I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 19. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	130 ⁽¹⁾	°C

1. The junction temperature is limited to 105 °C in the VOS0 voltage range.

5.3 Operating conditions

5.3.1 General operating conditions

Table 20. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	HSLV ⁽¹⁾ = 0	1.71 ⁽²⁾	-	3.6	V
		HSLV ⁽¹⁾ = 1	1.71 ⁽²⁾	-	2.7	
V_{DDSMPS}	Supply voltage for the internal SMPS step-down converter	V_{DD}	V_{DD}	-	V_{DD}	V

Table 20. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V _{DDIO2}	PB8, PB9, PD6, PD7, PG[9:14] I/Os supply voltage	At least one I/O in PB8, PB9, PD6, PD7, PG[9:14] is used, HSLV ⁽¹⁾ = 0	1.08	-	3.6	V
		At least one I/O in PB8, PB9, PD6, PD7, PG[9:14] is used, HSLV ⁽¹⁾ = 1	1.08	-	2.7	
		PB8, PB9, PD6, PD7, PG[9:14] are not used	0	-	3.6	
V _{DDUSB}	USB supply voltage	USB is used	3.0	-	3.6	V
		USB is not used	0	-	3.6	
V _{DDA}	Analog supply voltage	ADC is used	1.62	-	3.6	V
		DAC is used	1.8	-		
		VREFBUF is used	2.1	-		
		ADC, DAC, and VREFBUF are not used	0	-		
V _{BAT}	Backup domain supply voltage	-	1.2	-	3.6	V
V _{IN}	I/O input voltage	All I/Os except FT_c and TT_xx	-0.3	-	min (min (V _{DD} , V _{DDA} , V _{DDUSB} , V _{DDIO2}) + 3.6V, 5.5 V) (3)(4)	V
		Input voltage on FT_t in VBAT mode	-0.3	-	min (min (V _{BAT} , V _{DDA} , V _{DDUSB} , V _{DDIO2}) + 3.6 V, 5.5 V) (3)(4)	
		FT_c I/O	-0.3	-	5.0	
		TT_xx I/O	-0.3	-	V _{DDIOx} + 0.3	

Table 20. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V _{CORE}	Internal regulator ON	VOS0 ⁽⁵⁾ (max frequency for AHB and APB: 250 MHz)	1.30	1.35	1.40	V
		VOS1 (max frequency for AHB and APB: 200 MHz)	1.15	1.20	1.26	
		VOS2 (max frequency for AHB and APB: 150 MHz)	1.05	1.10	1.15	
		VOS3 (max frequency for AHB and APB: 100 MHz)	0.95	1.00	1.05	
	Regulator OFF: external V _{CORE} voltage must be supplied from external regulator on VCAP pins	VOS0 ⁽⁵⁾	1.32	1.35	1.40	V
		VOS1	1.17	1.20	1.26	
		VOS2	1.07	1.10	1.15	
		VOS3	0.97	1.00	1.05	
	Stop mode	SVOS3	-	1.0	-	V
		SVOS4	-	0.9	-	
SVOS5		-	0.74	-		
f _{HCLK}	AHB clock frequency	VOS0 ⁽⁵⁾	-	-	250	MHz
		VOS1	-	-	200	
		VOS2	-	-	150	
		VOS3	-	-	100	
f _{PCLKx} (x=1,2,3)	APB1, APB2, APB3 clock frequency	VOS0 ⁽⁵⁾	-	-	250	MHz
		VOS1	-	-	200	
		VOS2	-	-	150	
		VOS3	-	-	100	
P _D	Power dissipation at T _A = 85 °C for suffix 6 version ⁽⁶⁾	LQFP64	See Table 140 for appropriate thermal resistance and package. Power dissipation is calculated according to ambient temperature (T _A), maximum junction temperature (T _J), and selected thermal resistance.			mW
		LQFP100				
		LQFP144				
		LQFP176				
		UFBGA169				
		UFBGA176				
		VFQFPN68				
		WLCSP80				

Table 20. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
P _D	Power dissipation at T _A = 125 °C for suffix 3 version ⁽⁶⁾	LQFP100	See Table 140 for appropriate thermal resistance and package. Power dissipation is calculated according to ambient temperature (T _A), maximum junction temperature (T _J), and selected thermal resistance.			mW
		LQFP144				
		LQFP176				
		UFBGA169				
		UFBGA176				
		WLCSP80				
T _A	Ambient temperature for the suffix 3 version	Maximum power dissipation	-40	-	125	°C
	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	-	85	
		In LDO bypass mode	-40	-	125	
T _J	Junction temperature range	VOS0	-40	-	105	°C
		VOS1, VOS2, and VOS3	-40	-	130	

1. HSLV = High-speed low-voltage mode. Refer to General-purpose I/Os (GPIO) section of RM0481.
2. When RESET is released functionality is guaranteed down to BOR level 0 minimum voltage.
3. This formula must be applied on power supplies related to the I/O structure described by the pin definition table. Maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}, V_{DDIO2}) + 3.6 V and 5.5 V.
4. For operation with voltages higher than min (V_{DD}, V_{DDA}, V_{DDIO2}) + 0.3V, the internal pull-up and pull-down resistors must be disabled.
5. In VOS0 mode the max T_J is 105 °C.
6. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see [Table 19](#)).

Table 21. Maximum allowed clock frequencies

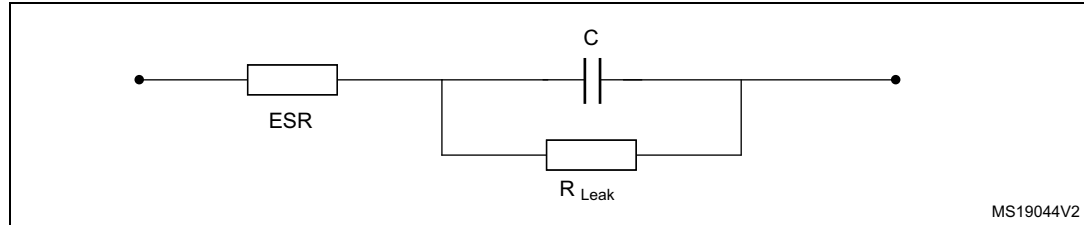
Symbol ⁽¹⁾⁽²⁾	Parameter	VOS0	VOS1	VOS2	VOS3	Unit
f _{CPU}	CPU	250	200	150	100	MHz
f _{HCLK}	AHB	250	200	150	100	
f _{PCLK}	APB	250	200	150	100	
-	FMC	250	200	150	100	
f _{octospi_ker_ck}	OCTOSPI[1:2]	250	200	150	100	
f _{sdmmc_ker_ck}	SDMMC[1:2]	250	200	150	100	
-	HDMI_CEC	4	4	4	4	
f _{fdcan_ker_ck}	FDCAN	250	200	150	100	
f _{I2C_ker_ck}	I2C[1:4]	250	200	150	100	
f _{I3C_ker_ck}	I3C	250	200	150	100	
f _{lptim_ker_ck}	LPTIM[1:6]	250	200	150	100	
f _{tim_ker_ck}	TIM[1:8], TIM[12:17]	250	200	150	100	
	TIM6/17	64	64	64	64	
f _{rng_clk}	RNG	50	50	50	50	
f _{sai_a_ker_ck}	SAI1/2	250	200	150	100	
f _{sai_b_ker_ck}						
f _{spi_ker_ck}	SPI(I2S)1,2,3	125	100	75	50	
	SPI4,5,6	125	100	75	50	
f _{lpuart_ker_ck}	LPUART1	250	200	150	100	
f _{usart_ker_ck}	USART/UART	250	200	150	100	
f _{usb_ker_ck}	USB FS	50	50	50	50	
f _{adc_ker_ck_input}	ADC/DAC	125	100	75	50	
f _{dac_pclk}	DAC	250	200	150	100	
f _{usb_ker_ck}	USBPD	64	64	64	64	
f _{rtc_ker_ck}	RTC	1	1	1	1	
-	DCMI	250	200	150	100	

1. Specified by design - Not tested in production.
2. The maximum kernel clock frequencies can be limited by the maximum peripheral clock frequency (refer to each peripheral electrical characteristics).

5.3.2 VCAP external capacitor

Stabilization for the embedded LDO regulator is achieved by connecting an external capacitor C_{EXT} to the VCAPx (one or two pins, depending upon the package). C_{EXT} is specified in [Table 22](#). VCAP operating conditions. Two external capacitors must be connected to VCAP pins (refer to AN5711 “STM32H5 Series hardware development”).

Figure 22. External capacitor C_{EXT}



MS19044V2

Table 22. Supply voltage and maximum frequency configuration

Symbol	Parameter	Conditions
C_{EXT}	External capacitor for LDO enabled	2.2 $\mu\text{F}^{(1)}$
ESR	Equivalent series resistance of the external capacitor	< 100 m Ω

1. This value corresponds to C_{EXT} typical value. A variation of $\pm 20\%$ is tolerated

5.3.3 SMPS step-down converter

The devices embed a high power efficiency SMPS step-down converter requiring external components.

Table 23. Characteristics of SMPS step-down converter external components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{in}	Capacitance of external capacitor on VDDSMPS pins	-	-	4.7 ⁽¹⁾	-	μF
	ESR of external capacitor	2.4 MHz	-	-	10	m Ω
C_{filt}	Capacitance of external capacitor on VLXSMPS pin	-	-	220	-	pF
C_{OUT}	Capacitance of external capacitor on VCAP pin	-	-	10 ⁽¹⁾	-	μF
	ESR of external capacitor	2.4 MHz	-	-	20	m Ω
L	Inductance of external Inductor on VLXSMPS pin	-	-	2.2 ⁽¹⁾	-	μH
	Series DC resistance	All packages	-	-	150	m Ω
		WLCSP80 package, $V_{DDSMPS} > 3\text{ V}$	-	-	300	
I_{SAT}	DC current at which the inductance drops 30% from the value without current	-	1	-	-	A
I_{RMS}	Average current for which the temperature of the inductor is raised 40 °C by the DC current	-	1	-	-	

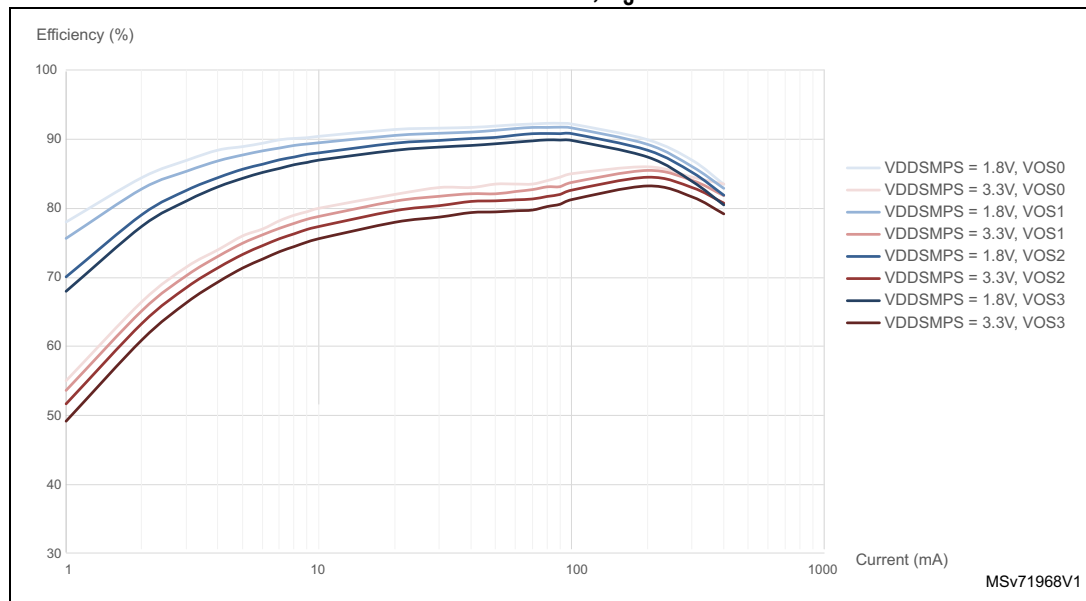
1. Tolerance: -50% and + 30% for all conditions.

The SMPS current consumption can be determined using the following formula based on the maximum LDO current consumption provided in [Section 5.3.7](#):

$$I_{DDSMPS} = I_{DDLDO} \times V_{CORE} / (V_{DD} \times \text{efficiency})$$

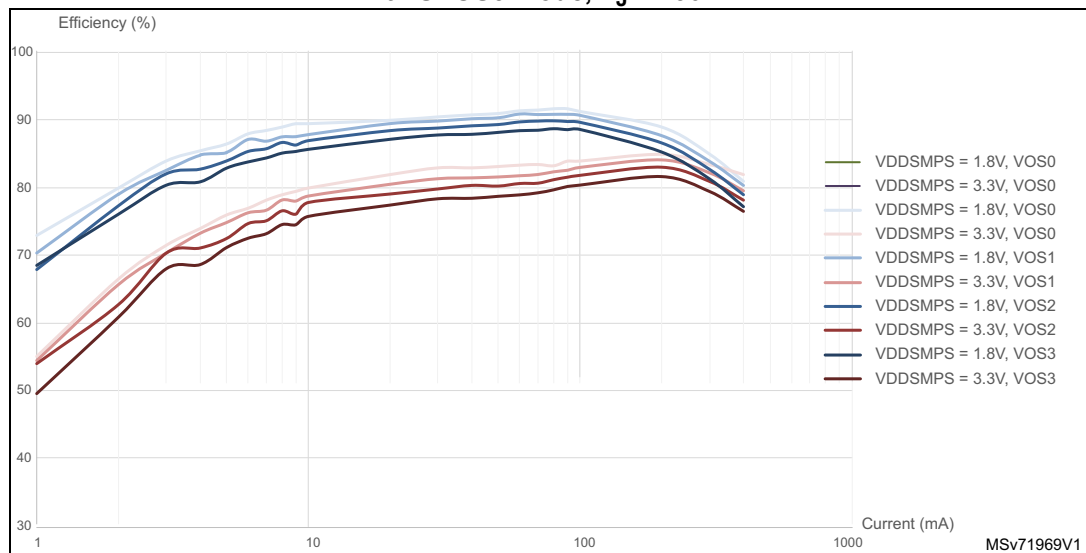
I_{DDLDO} is the current in LDO configuration given in the following tables, V_{CORE} is the digital core supply (VCAP), and efficiency is defined in the following curves.

Figure 23. SMPS efficiency versus load current in Run, Sleep and Stop modes with SVOS3 mode, $T_J = 30\text{ }^\circ\text{C}$



Note: SVOS3 is equivalent to VOS3 in Run and Sleep modes.

Figure 24. SMPS efficiency versus load current in Run, Sleep and Stop modes with SVOS3 mode, $T_J = 130\text{ }^\circ\text{C}$



Note: SVOS3 is equivalent to VOS3 in Run and Sleep modes.

Figure 25. SMPS efficiency versus load current in stop SVOV4, SVOS5, $T_J = 30\text{ }^\circ\text{C}$

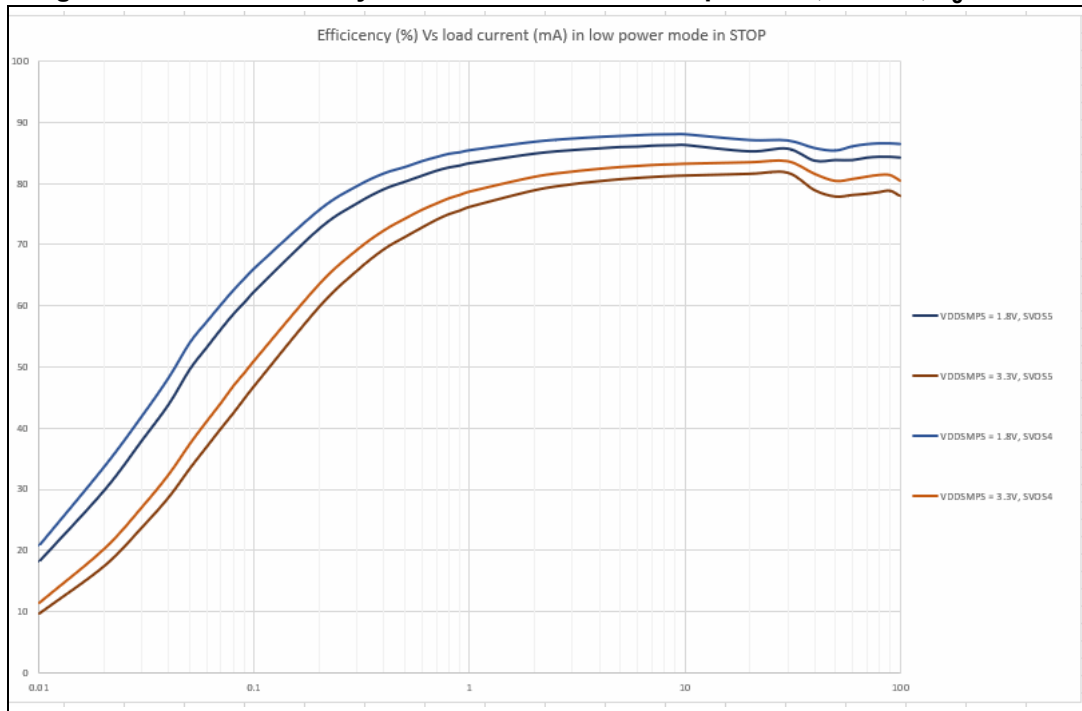
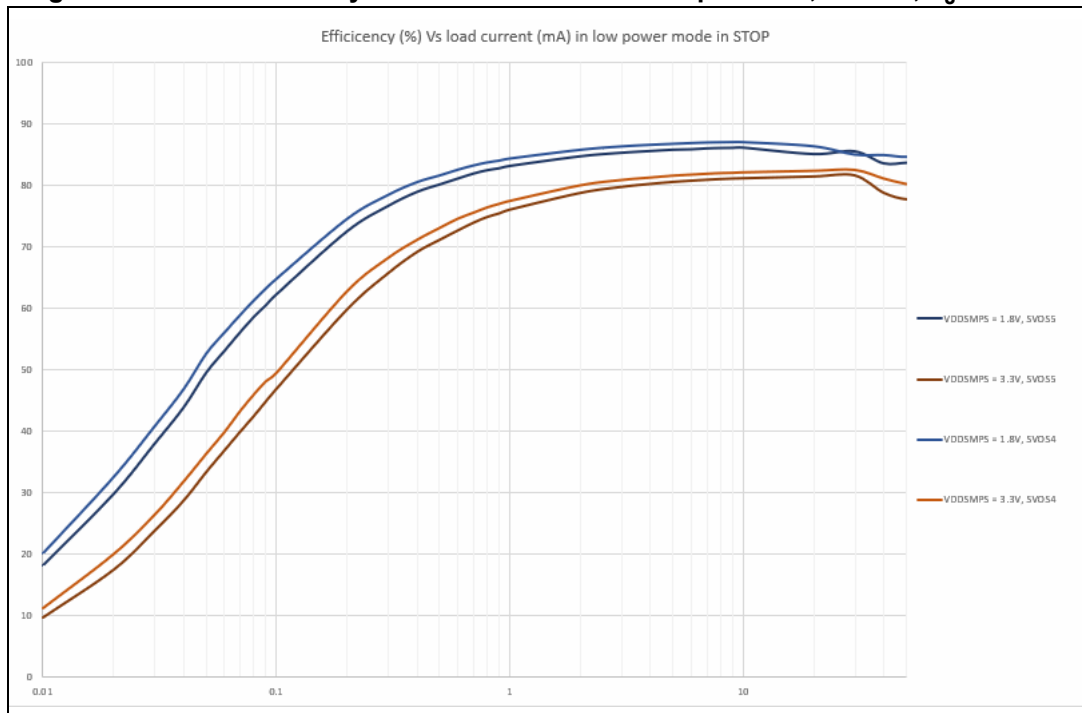


Figure 26. SMPS efficiency versus load current in stop SVOV4, SVOS5, $T_J = 130\text{ }^\circ\text{C}$



5.3.4 Operating conditions at power-up/down

Subject to general operating conditions for T_A .

Table 24. Operating conditions at power-up/down (regulator ON)

Symbol	Parameter	Min	Max	Unit
T_{VDD}	V_{DD} rise time rate	0	∞	$\mu\text{s/V}$
	V_{DD} fall time rate	10	∞	
T_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
T_{VDDUSB}	T_{VDDUSB} rise time rate	0	∞	
	T_{VDDUSB} fall time rate	10	∞	
T_{VDDIO2}	T_{VDDIO2} rise time rate	0	∞	
	T_{VDDIO2} fall time rate	10	∞	
T_{VBAT}	T_{VBAT} rise time rate	0	∞	
	T_{VBAT} fall time rate	10	∞	

5.3.5 Embedded reset and power control block characteristics

The parameters given in [Table 25](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

Table 25. Embedded reset and power control block characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}^{(2)}$	Reset temporization after BOR0 detection	V_{DD} rising	-	377	550	μs
$V_{POR/PDR}$	Power-on/down reset threshold (BORH_EN =0)	Rising edge	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brownout reset threshold 1 (BORH_EN =1)	Rising edge	2.04	2.10	2.15	V
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brownout reset threshold 2 (BORH_EN =1)	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brownout reset threshold 3 (BORH_EN =1)	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	

Table 25. Embedded reset and power control block characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V _{PVD0}	PVD threshold 0	Rising edge	1.90	1.96	2.01	V	
		Falling edge	1.81	1.86	1.91		
V _{PVD1}	PVD threshold 1	Rising edge	2.05	2.10	2.16		
		Falling edge	1.96	2.01	2.06		
V _{PVD2}	PVD threshold 2	Rising edge	2.19	2.26	2.32		
		Falling edge	2.10	2.15	2.21		
V _{PVD3}	PVD threshold 3	Rising edge	2.35	2.41	2.47		
		Falling edge	2.25	2.31	2.37		
V _{PVD4}	PVD threshold 4	Rising edge	2.49	2.56	2.62		
		Falling edge	2.39	2.45	2.51		
V _{PVD5}	PVD threshold 5	Rising edge	2.64	2.71	2.78		
		Falling edge	2.55	2.61	2.68		
V _{PVD6}	PVD threshold 6	Rising edge	2.78	2.86	2.94		
		Falling edge	2.69	2.76	2.83		
V _{POR/PDR}	Hysteresis for power-on/down reset	Hysteresis in Run mode	-	43	-	mV	
V _{hyst_BOR_PVD}	Hysteresis voltage of BOR (unless BORH_EN = 0) and PVD	-	-	100	-		
I _{DD_BOR_PVD} ⁽²⁾	BOR and PVD consumption from V _{DD}	-	-	-	0.630	μA	
I _{DD_POR_PDR}	POR and PDR consumption from V _{DD}	-	0.8	-	1.2		
V _{AVD0}	V _{DDA} voltage monitor 0 threshold	Rising edge	1.66	1.71	1.76	V	
		Falling edge	1.56	1.61	1.66		
V _{AVD1}	V _{DDA} voltage monitor 1 threshold	Rising edge	2.06	2.12	2.19		
		Falling edge	1.96	2.02	2.08		
V _{AVD2}	V _{DDA} voltage monitor 2 threshold	Rising edge	2.42	2.50	2.58		
		Falling edge	2.35	2.42	2.49		
V _{AVD3}	V _{DDA} voltage monitor 3 threshold	Rising edge	2.74	2.83	2.91		
		Falling edge	2.64	2.72	2.80		
V _{IO2VM}	V _{DDIO2} voltage monitor threshold	-	-	0.9	-		V
V _{hyst_AVD}	Hysteresis of V _{DDA} voltage monitor	-	-	100	-		mV
I _{DD_AVD_IO2VM} ⁽²⁾	Power voltage detector consumption from V _{DD} (AVD, IO2VM)	-	-	-	0.25	μA	
I _{DD_AVD_A} ⁽²⁾	V _{DDA} analog voltage detector consumption from V _{DDA} (resistor bridge)	-	-	-	0.25		

1. Evaluated by characterization and not tested in production, unless otherwise specified.
2. Specified by design - Not tested in production

5.3.6 Embedded reference voltage

The parameters given in [Table 26](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20](#).

Table 26. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT}^{(1)}$	Internal reference voltage	$-40\text{ °C} < T_J < +130\text{ °C}$	1.180	1.216	1.255	V
$t_{S_vrefint}^{(2)(3)}$	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	μs
t_{S_vbat}	V_{BAT} sampling time when reading the internal V_{BAT} voltage	-	9	-	-	
$t_{start_vrefint}^{(3)}$	Start time of reference voltage buffer when the ADC is enabled	-	-	-	4.4	
$I_{refbuf}^{(3)}$	Reference buffer consumption for ADC	$V_{DD} = 3.3\text{ V}$	9	13.5	23	μA
$\Delta V_{REFINT}^{(3)}$	Internal reference voltage spread over the temperature range	$-40\text{ °C} < T_J < +130\text{ °C}$	-	5	15	mV
T_{Ccoeff}	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$	Average voltage coefficient	$3.0\text{ V} < V_{DD} < 3.6\text{ V}$	-	10	1370	ppm/V
$V_{REFINT_DIV1}^{(3)}$	1/4 reference voltage	-	-	25	-	% V_{REFINT}
$V_{REFINT_DIV2}^{(3)}$	1/2 reference voltage		-	50	-	
$V_{REFINT_DIV3}^{(3)}$	3/4 reference voltage		-	75	-	

- V_{REFINT} does not take into account package and soldering effects.
- The shortest sampling time for the application can be determined by multiple iterations.
- Specified by design - Not tested in production.

Table 27. Internal reference voltage calibration value

Symbol	Parameter	Memory address
V_{REFINT_CAL}	Raw data acquired at 30 °C, $V_{DDA} = 3.3\text{ V}$	0x08FF F810 - 0x08FF F811

5.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.

- All peripherals are disabled except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait-state number, depending on the f_{HCLK} frequency (refer to the tables “FLASH recommended number of wait states and programming delay” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency and the APB clock frequency is AHB frequency.

The parameters given in the following tables are derived from tests performed under supply voltage conditions summarized in [Table 20](#), and, unless otherwise specified, at ambient temperature.

The maximum current consumption is given for LDO regulator ON.

Table 28. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 2-way instruction cache ON, PREFETCH ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ LDO	Typ SMPS	Max ⁽¹⁾⁽²⁾				Unit	
						T _J = 25 °C	T _J = 85 °C	T _J = 105 °C	T _J = 130 °C		
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled	VOS0	250	32.1	17.5	37	65	87	-	mA
				215	27.9	15.0	32	60	82	-	
				200	25.7	13.8	30	59	81	-	
			VOS1	200	22.1	11.0	25	45	62	93	
				180	20.3	10.1	23	43	59	90	
				168	18.8	9.3	21	42	58	89	
			VOS2	150	16.9	8.5	20	40	56	88	
				150	15.4	7.4	17	33	47	73	
				100	10.8	5.2	13	28	41	68	
			VOS3	100	9.8	4.5	11	23	34	55	
				60	6.4	3.0	8.0	20	30	52	
				25	3.2	1.7	5.0	17	27	49	
		All peripherals enabled	VOS0	250	86.8	49.8	90	118	140	-	
				215	75.0	43.2	78	107	128	-	
				200	69.5	40.1	72	102	123	-	
			VOS1	200	60.7	31.7	62	82	99	130	
				180	55.1	28.5	56	76	92	124	
				150	45.8	23.4	47	68	84	116	
			VOS2	150	41.9	20.0	43	59	72	98	
				100	28.5	13.8	30	45	58	85	
				100	25.9	11.7	27	39	49	71	
			VOS3	60	16.2	7.5	17	29	40	61	
				25	7.5	3.8	9.0	21	31	53	

1. Evaluated by characterization - Not tested in production.
2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

Table 29. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 1-way instruction cache ON, PREFETCH ON

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ LDO	Typ SMPS	Max ⁽¹⁾⁽²⁾				Unit	
						T _J = 25 °C	T _J = 85 °C	T _J = 105 °C	T _J = 130 °C		
I _{DD} (Run)	Supply current in Run mode	All peripherals disabled	VOS0	250	29.2	15.9	34	62	84	-	mA
				200	23.3	12.5	28	56	78	-	
			VOS1	200	20.1	10.0	23	43	59	91	
				180	18.5	9.2	21	41	57	89	
			VOS2	150	15.4	7.8	18	38	54	86	
				150	14.0	6.7	16	32	45	71	
			VOS3	100	9.8	4.8	12	27	40	67	
				100	8.9	4.2	10	22	33	54	
			25	3.0	1.6	4.0	17	27	49		

1. Evaluated by characterization - Not tested in production.
2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

Table 30. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 1-way

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ LDO	Typ SMPS	Max ⁽¹⁾⁽²⁾				Unit	
						T _J = 25 °C	T _J = 85 °C	T _J = 105 °C	T _J = 130 °C		
I _{DD} (Run)	Supply current in Run mode	All peripherals disabled	VOS0	250	27.8	15.5	32	61	82	-	mA
				215	24.1	13.4	29	57	79	-	
				200	22.1	12.3	27	55	77	-	
			VOS1	200	19.1	9.9	22	42	58	90	
				180	17.6	9.1	20	40	56	88	
			VOS2	150	14.6	7.6	22	42	58	90	
				150	13.3	6.6	17	37	53	85	
			VOS3	100	9.4	4.7	11	27	40	66	
				100	8.5	4.1	10	22	33	54	
			VOS3	60	5.6	2.8	7	19	30	51	
				25	2.9	1.6	4	16	27	48	

1. Evaluated by characterization - Not tested in production.
2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

Table 31. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 2-way

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ LDO	Typ SMPS	Max ⁽¹⁾⁽²⁾				Unit	
						T _J = 25 °C	T _J = 85 °C	T _J = 105 °C	T _J = 130 °C		
I _{DD(Run)}	Supply current in Run mode	All peripherals disabled	VOS0	250	30.8	17.2	35	64	86	-	mA
				215	26.7	14.4	31	60	81	-	
				200	24.6	13.3	29	58	80	-	
			VOS1	200	21.2	10.5	24	44	61	93	
				180	19.5	9.7	22	42	58	90	
				168	18.0	9.0	21	41	57	89	
			VOS2	150	16.2	8.4	19	39	55	87	
				150	14.8	7.2	17	33	46	72	
			VOS3	100	10.3	5.1	12	28	41	67	
				100	9.4	4.5	11	23	33	55	
				60	6.1	2.9	8.0	20	30	52	
						25	3.2	1.7	5.0	17	

1. Evaluated by characterization - Not tested in production.
2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

Table 32. Typical consumption in Run mode with CoreMark running from flash memory and SRAM⁽¹⁾

Symbol	Parameter	Conditions		f _{HCLK} (MHz)	Typ LDO	Typ SMPS	Unit	Typ LDO	Typ SMPS	Unit
		Peripheral	Code							
I _{DD(Run)}	Supply current in Run mode	All peripherals disabled, instruction cache 2-way, prefetch ON	FLASH	250	32.1	17.5	mA	128.6	70.1	μA/MHz
				200	22.1	10.97		110.7	54.8	
				168	18.8	9.3		111.8	55.6	
				150	15.4	8.5		102.7	56.9	
				100	9.8	4.5		97.9	45.3	
		All peripherals disabled, instruction cache 1-way, prefetch ON	FLASH	250	29.2	15.9		116.6	63.8	
				200	20.1	12.5		100.4	62.7	
				150	14.0	10.0		93.3	66.4	
				100	8.9	4.2		88.9	41.7	
		All peripherals disabled, instruction cache 2-way	SRAM	250	30.8	17.2		123.3	68.7	
				200	21.2	10.5		106.2	52.6	
				168	18.0	9.0		107.3	53.4	
				150	14.8	7.2		98.5	48.2	
				100	9.4	4.5		94.1	44.6	
		All peripherals disabled, instruction cache 1-way	SRAM	250	27.8	15.5		111.1	61.9	
				200	19.1	9.9		95.4	49.3	
				150	13.3	6.6		88.9	43.8	
				100	8.5	4.1		84.9	40.7	

1. Evaluated by characterization - Not tested in production.

Table 33. Typical consumption in Run mode with SecureMark running from flash memory and SRAM⁽¹⁾

Symbol	Parameter	Conditions		f _{HCLK} (MHz)	Typ LDO	Typ SMPS	Unit	Typ LDO	Typ SMPS	Unit
		Peripheral	Code							
I _{DD(Run)}	Supply current in Run mode	All peripherals disabled, instruction cache 2-way, prefetch ON	FLASH	250	34.1	17.9	mA	136.3	71.8	µA/MHz
				180	21.8	10.6		120.9	58.8	
				168	20.1	9.8		119.7	58.5	
				150	24.9	7.7		166.2	51.2	
				100	10.6	4.8		106.0	47.6	
		All peripherals disabled, instruction cache 1-way, prefetch ON	FLASH	250	31.3	16.6		125.2	66.3	
				180	20.1	9.8		111.6	54.5	
				168	18.5	9.1		110.4	54.2	
				150	18.8	7.2		125.1	47.7	
				100	9.8	4.5		98.3	44.5	

1. Evaluated by characterization - Not tested in production.

Table 34. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ LDO	Typ SMPS	Max ^{(1) (2)}				Unit	
						T _J = 25°C	T _J = 85°C	T _J = 105°C	T _J = 130°C		
I _{DD(sleep)}	Supply current in sleep mode	All peripherals disabled	VOS0	250	7.3	4.2	12	40	61	-	mA
				200	5.8	3.3	10	38	60	-	
			VOS1	200	4.8	2.6	8	27	43	75	
				180	4.8	2.6	8	27	43	75	
				168	4.3	2.3	7	26	42	74	
			VOS2	150	3.9	2.2	7	26	42	74	
				150	3.5	1.9	6	21	34	60	
			VOS3	100	2.8	1.6	5	20	33	59	
				100	2.5	1.4	4	16	26	48	
			60	2.0	1.2	4	15	26	47		

1. Evaluated by characterization - Not tested in production.

2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

Table 35. Typical and maximum current consumption in Stop mode

Symbol	Parameter	Conditions		Typ LDO	Typ SMPS	Max ^{(1) (2)}				Unit
						T _J = 25 °C	T _J = 85 °C	T _J = 105 °C	T _J = 130 °C	
I _{DD(stop)}	Supply current in Stop	Flash memory in low power mode, SRAMs ON	SVOS3	0.37	0.09	2.00	13.98	24.00	44.39	mA
			SVOS4	0.27	0.07	1.40	10.48	18.37	34.76	
			SVOS5	0.19	0.06	0.86	7.08	12.88	25.31	
		Flash memory in normal mode, SRAMs ON	SVOS3	0.38	0.10	2.02	14.01	24.06	44.55	
			SVOS4	0.29	0.09	1.42	10.52	18.46	34.88	
		Flash memory in low power mode, SRAMs OFF except SRAM2 16 Kbytes ON	SVOS3	0.34	0.09	1.93	13.28	22.75	41.99	
			SVOS4	0.25	0.07	1.35	9.87	17.33	32.65	
			SVOS5	0.17	0.05	0.81	6.46	11.68	22.86	
		Flash memory in low power mode, SRAMs OFF except SRAM2 ON	SVOS3	0.35	0.10	1.95	13.45	23.02	42.52	
			SVOS4	0.26	0.08	1.36	10.01	17.52	33.10	
			SVOS5	0.17	0.08	0.82	6.59	11.92	23.37	

1. Evaluated by characterization - Not tested in production.
2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

Table 36. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions		Typ ⁽¹⁾				Max ⁽¹⁾				Unit
		Backup RAM	RTC and LSE ⁽²⁾	1.8 V	2.4 V	3 V	3.3 V	T _J = 25 °C	T _J = 85 °C	T _J = 105 °C	T _J = 130 °C	
I _{DD(standby)}	Supply current in standby mode, IWDG OFF	OFF	OFF	2.58	2.78	3.01	3.19	4.3	8.8	16.5	42.6	µA
		ON	OFF	3.79	4.05	4.38	4.63	6.0	17.0	30.0	75.0	
		OFF	ON	2.91	3.15	3.47	3.67	-	-	-	-	
		ON	ON	4.16	4.46	4.85	5.12	-	-	-	-	

1. Evaluated by characterization - Not tested in production.
2. LSE is in medium-low drive mode.

Table 37. Typical and maximum current consumption in VBAT mode

Symbol	Parameter	Conditions		Typ ⁽¹⁾				Max ⁽¹⁾				Unit
		Backup RAM	RTC and LSE ⁽²⁾	1.8 V	2.4 V	3 V	3.3 V	T _J = 25 °C	T _J = 85 °C	T _J = 105 °C	T _J = 130 °C	
I _{DD(VBAT)}	Supply current in V _{BAT} mode	OFF	OFF	0.01	0.01	0.02	0.02	0.2	2.0	4.9	14.9	µA
		ON	OFF	1.11	1.14	1.17	1.29	3	14	27	62	
		OFF	ON	0.45	0.46	0.48	0.59	-	-	-	-	
		ON	ON	1.56	1.57	1.62	1.84	-	-	-	-	

1. Evaluated by characterization - Not tested in production.

2. LSE is in medium-low drive mode.

I/O system current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 58](#).

To estimate the current consumption for the output pins, consider also external pull-downs or loads.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this current consumption can be avoided by configuring the I/Os in analog mode. This is notably the case of ADC input pins, to be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done by using pull-up/down resistors, or by configuring the pins in output mode.

In addition to the internal peripheral current consumption, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: C = C_{INT} + C_{EXT} + C_S

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration
- All peripherals are disabled unless otherwise mentioned
- The I/O compensation cell is enabled
- f_{HCLK} is the CPU clock, $f_{PCLK} = f_{rcc_cpu_ck}$, and $f_{HCLK} = f_{rcc_cpu_ck}$.

The given value is calculated by measuring the difference of current consumption:

- with all peripherals clocked off
- with only one peripheral clocked on
- $f_{rcc_cpu_ck} = 250$ MHz (Scale 0), $f_{rcc_cpu_ck} = 200$ MHz (Scale 1), $f_{rcc_cpu_ck} = 150$ MHz (Scale 2), $f_{rcc_cpu_ck} = 100$ MHz (Scale 3)
- the ambient operating temperature is 25 °C and $V_{DD} = 3.0$ V

Table 38. Peripheral current consumption in Sleep mode

Bus	Peripheral	I _{DD} (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB1	SRAM1	0.9	0.85	0.78	0.7	µA/MHz
	BKPRAM	0.95	0.89	0.82	0.74	
	CORDIC	0.5	0.45	0.42	0.4	
	CRC	0.22	0.21	0.18	0.18	
	DCACHE	0.66	0.59	0.55	0.51	
	ETH	11.33	10	9.13	8.32	
	FLASH	10.19	8.87	8.09	7.35	
	FMAC	2.07	1.84	1.68	1.56	
	GPDMA1	0.62	0.55	0.51	0.45	
	GPDMA2	0.45	0.43	0.38	0.35	
	GTZC1	1.19	1.05	0.97	0.9	
	ICACHE	0.86	0.81	0.75	0.67	
	RAMCFG	0.88	0.79	0.71	0.67	
	AHB1	1.09	0.94	0.86	0.79	

Table 38. Peripheral current consumption in Sleep mode (continued)

Bus	Peripheral	I _{DD} (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB2	ADC12	2.35	2.1	1.9	1.74	μA/MHz
	DAC1	1.35	1.19	1.07	0.98	
	DCMI	3.49	3.09	2.83	2.55	
	GPIOA	0.1	0.08	0.07	0.08	
	GPIOB	0.07	0.06	0.05	0.05	
	GPIOC	0.08	0.05	0.04	0.04	
	GPIOD	0.09	0.06	0.05	0.04	
	GPIOE	0.09	0.09	0.08	0.05	
	GPIOF	0.06	0.08	0.08	0.05	
	GPIOG	0.07	0.07	0.06	0.04	
	GPIOH	0.07	0.07	0.05	0.06	
	GPIOI	0.07	0.07	0.06	0.04	
	HASH1	1.37	1.2	1.1	1	
	PKA	5.43	4.78	4.37	3.98	
	RNG1	1.12	0.99	0.9	0.82	
	SRAM2	1.33	1.18	1.06	0.96	
	SRAM3	1.5	1.33	1.22	1.1	
AHB2	1.59	1.39	1.29	1.16		
AHB4	FMC	9.73	8.48	7.69	6.95	uA/MHz
	OSPI1	2.88	2.54	2.29	2.08	
	SDMMC1	8.71	7.64	6.98	6.36	
	SDMMC2	8.46	7.45	6.82	6.2	
	AHB4	0.36	0.32	0.32	0.28	

Table 38. Peripheral current consumption in Sleep mode (continued)

Bus	Peripheral	I _{DD} (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
APB1	CEC	0.15	0.15	0.14	0.11	μA/MHz
	CRS	0.22	0.23	0.20	0.19	
	FDCAN1	6.37	5.63	5.14	4.70	
	I2C1	0.57	0.5	0.49	0.42	
	I2C2	0.57	0.52	0.5	0.46	
	I3C1	0.28	0.27	0.28	0.25	
	LPTIM2	0.91	0.81	0.75	0.69	
	SPI2	1.04	0.93	0.89	0.78	
	SPI3	1.00	0.92	0.85	0.76	
	TIM12	1.41	1.26	1.18	1.06	
	TIM13	0.92	0.82	0.77	0.70	
	TIM14	0.89	0.78	0.75	0.66	
	TIM2	2.86	2.51	2.30	2.11	
	TIM3	2.52	2.21	2.03	1.87	
	TIM4	2.43	2.15	1.96	1.79	
	TIM5	2.79	2.48	2.26	2.06	
	TIM6	0.54	0.49	0.45	0.42	
	TIM7	0.56	0.5	0.48	0.43	
	UART12	1.17	1.06	0.95	0.88	
	UART4	1.12	0.98	0.93	0.83	
	UART5	1.09	0.99	0.93	0.84	
	UART7	1.28	1.14	1.05	0.93	
	UART8	1.17	1.06	0.94	0.86	
	UART9	1.12	1.00	0.90	0.84	
	UCPD1	1.1	1.00	0.90	0.84	
	USART10	1.35	1.22	1.14	1.02	
	USART11	1.24	1.11	1.04	0.94	
	USART2	1.42	1.29	1.19	1.07	
	USART3	1.35	1.24	1.14	1.02	
	USART6	1.19	1.08	1.02	0.92	
WWDG1	0.39	0.35	0.35	0.30		
APB1	1.85	1.61	1.49	1.34		

Table 38. Peripheral current consumption in Sleep mode (continued)

Bus	Peripheral	I _{DD} (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
APB2	SAI1	1.13	0.99	0.93	0.82	μA/MHz
	SAI2	1.06	0.9	0.85	0.75	
	SPI1	1.03	0.91	0.85	0.75	
	SPI4	1.03	0.89	0.83	0.73	
	SPI6	1.03	0.9	0.85	0.74	
	TIM1	4.35	3.86	3.52	3.2	
	TIM15	2.08	1.84	1.69	1.54	
	TIM16	1.43	1.26	1.16	1.05	
	TIM17	1.44	1.25	1.17	1.05	
	TIM8	4.33	3.82	3.5	3.18	
	USART1	1.24	1.11	1.02	0.91	
	USBFS	2.53	2.22	2.04	1.84	
	APB2	1.04	0.92	0.84	0.77	
APB3	I2C3	2.43	2.14	1.93	1.76	uA/MHz
	I2C4	2.37	2.08	1.89	1.73	
	LPTIM1	0.92	0.82	0.75	0.67	
	LPTIM3	0.88	0.77	0.71	0.65	
	LPTIM4	0.49	0.45	0.41	0.37	
	LPTIM5	0.84	0.76	0.69	0.63	
	LPTIM6	0.93	0.82	0.76	0.70	
	LPUART1	0.84	0.74	0.66	0.63	
	RTCAPB	1.93	1.70	1.54	1.38	
	SBS	0.45	0.41	0.38	0.34	
	SPI5	1.05	0.93	0.84	0.75	
	VREFBUF	0.08	0.08	0.07	0.05	
	APB3	0.64	0.57	0.53	0.48	

Wake-up time from low-power modes

The times given in [Table 39](#) are measured starting from the wake-up event trigger up to the first instruction executed by the CPU:

- for Stop or Sleep modes: the wake-up event is WFE.
- WKUP (PA1) pin is used to wake-up from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} = 3.0 V.

Table 39. Low-power mode wake-up timings⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
t _{WUSLEEP}	Wake-up time from Sleep mode	Instruction cache enabled	15	16	CPU clock cycles
		Instruction cache disabled	15	16	
t _{WUSTOP}	Wake-up time from Stop mode	SVOS3, HSI 64 MHz, flash memory in normal mode	4.0	4.8	μs
		SVOS3, HSI 64 MHz, flash memory in low-power mode	7.9	11.5	
		SVOS4, HSI 64 MHz, flash memory in normal mode	13.8	16.0	
		SVOS4, HSI 64 MHz, flash memory in low-power mode	17.7	21.9	
		SVOS5, HSI 64 MHz, flash memory in low-power mode	31.4	36.8	
		SVOS3, CSI 4 MHz, flash memory in normal mode	25.5	31.0	
		SVOS3, CSI 4 MHz, flash memory in low power mode	27.7	34.2	
		SVOS4, CSI 4 MHz, flash memory in normal mode	35.3	40.8	
		SVOS4, CSI 4 MHz, flash memory in low-power mode	37.5	44.0	
		SVOS5, CSI 4 MHz, flash memory in low-power mode	51.2	58.9	
t _{WUSTBY}	Wake-up time from Standby mode	VCAP capacitors discharged	506.0	653.6	

1. Evaluated by characterization - Not tested in production.

5.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal must respect the [Table 40](#) in addition to [Table 58](#). The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0481).

Table 40. High-speed external user clock characteristics⁽¹⁾

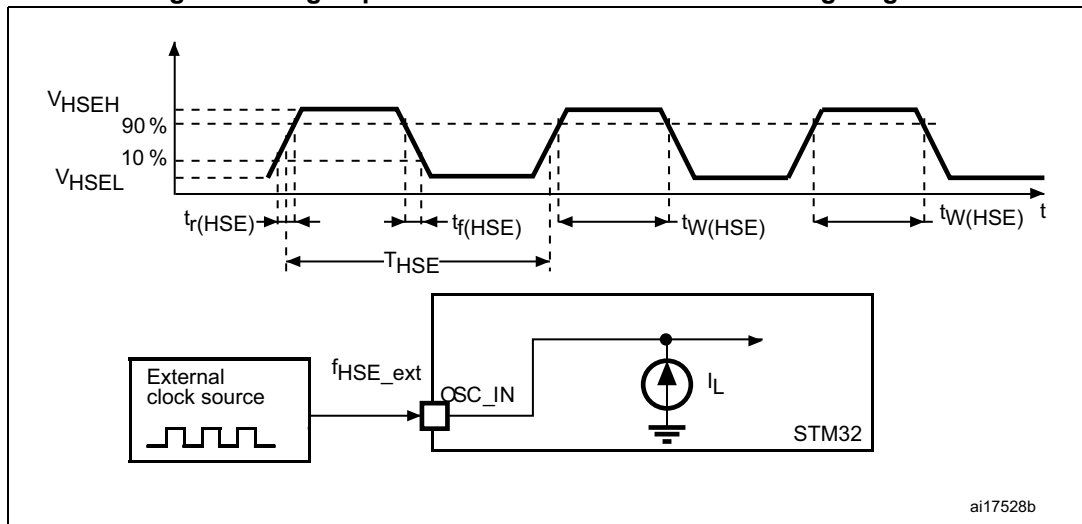
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{HSE_ext}	User external clock source frequency	External digital/analog clock	4	25	50	MHz
V _{HSEH}	Digital OSC_IN input high-level voltage	External digital clock	0.7 V _{DD}	-	V _{DD}	V
V _{HSEL}	Digital OSC_IN input low-level voltage		V _{SS}	-	0.3 V _{DD}	
t _{w(HSEH)} /t _{w(HSEL)} ⁽²⁾	Digital OSC_IN input high or low time	External digital clock	7	-	-	ns

Table 40. High-speed external user clock characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isw(HSEH)}$ $(V_{HSEH} - V_{HSEL})^{(3)}$	Analog low-swing OSC_IN peak-to-peak amplitude	External analog low swing clock	0.2	-	$2/3 V_{DD}$	V
$DuCy_{HSE}$	Analog low-swing OSC_IN duty cycle		45	50	55	%
$t_{r(HSE)}/t_{f(HSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low swing clock, 10% to 90%	$0.05 / f_{HSE_ext}$	-	$0.3 / f_{HSE_ext}$	ns

1. Specified by design - Not tested in production..
2. The rise and fall times for a digital input signal are not specified, but the V_{HSEH} and V_{HSEL} conditions must be fulfilled anyway.
3. The DC component of the signal must ensure that the signal peaks are located between V_{DD} and V_{SS} .

Figure 27. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal must respect the [Table 41](#) in addition to [Table 58](#). The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0481).

Table 41. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	External digital/analog clock	-	32.768	1000	kHz
V_{LSEH}	Digital OSC32_IN input high-level voltage	External digital clock	$0.7 V_{DD}$	-	V_{DD}	V
V_{LSEL}	Digital OSC32_IN input low-level voltage		V_{SS}	-	$0.3 V_{DD}$	

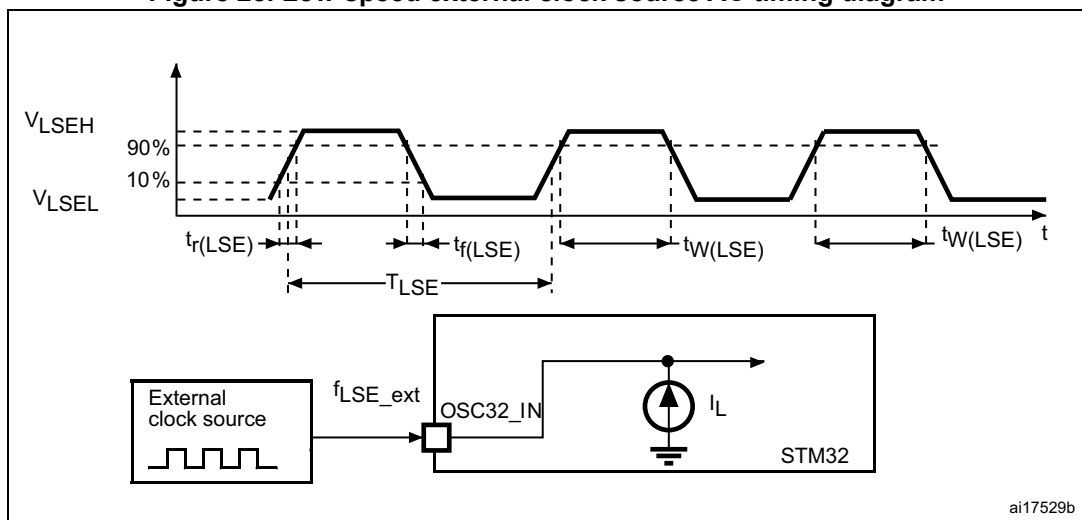
Table 41. Low-speed external user clock characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(LSEH)}/t_{w(LSEL)}$	Digital OSC_IN input high or low time	External digital clock	250	-	-	ns
V_{isw_H}	Analog low-swing OSC_IN high-level voltage	External analog low swing clock	0.6	-	1.225	V
V_{isw_L}	Analog low-swing OSC_IN low-level voltage		0.35	-	0.8	
V_{iswLSE} ($V_{LSEH} - V_{LSEL}$)	Analog low-swing OSC_IN peak-to-peak amplitude		0.5	-	0.875	
DuCyLSE	Analog low-swing OSC_IN duty cycle		45	50	55	
$t_{r(LSE)}/t_{f(LSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low swing clock, 10% to 90%	-	100	200	ns

1. Specified by design - Not tested in production.

Note: For information on selecting the crystal, refer to AN2867 “Oscillator design guide for ST microcontrollers” available from www.st.com.

Figure 28. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 50 MHz crystal/ceramic resonator oscillator.

All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 42](#). In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 42. 4-50 MHz HSE oscillator characteristics⁽¹⁾

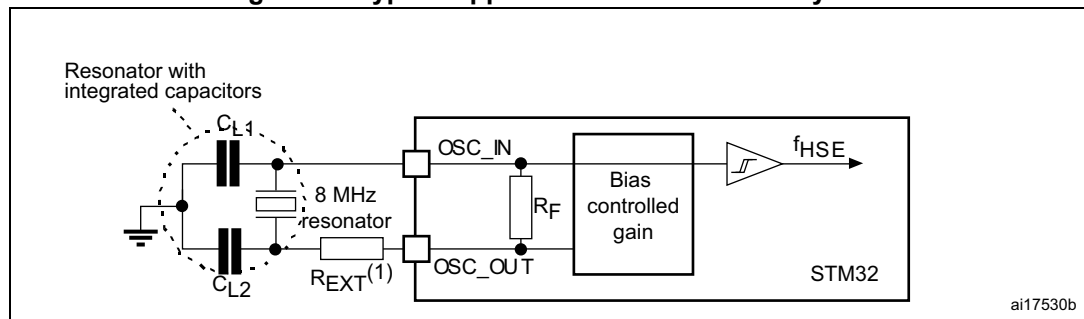
Symbol	Parameter	Operating conditions ⁽²⁾	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	50	MHz
R _F	Feedback resistor	-	-	200	-	kΩ
I _{DD(HSE)}	HSE current consumption	During startup ⁽³⁾	-	-	10	mA
		V _{DD} = 3 V, R _m = 20 Ω, C _L = 10 pF at 4 MHz	-	0.44	-	
		V _{DD} = 3 V, R _m = 20 Ω, C _L = 10 pF at 8 MHz	-	0.44	-	
		V _{DD} = 3 V, R _m = 20 Ω, C _L = 10 pF at 16 MHz	-	0.55	-	
		V _{DD} = 3 V, R _m = 20 Ω, C _L = 10 pF at 32 MHz	-	0.67	-	
V _{DD} = 3 V, R _m = 20 Ω, C _L = 10 pF at 48 MHz	-	1.17	-			
G _{m_{critmax}}	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
t _{SU(HSE)} ⁽⁴⁾	Startup time	V _{DD} is stabilized	-	2	-	ms

1. Evaluated by design - Not tested in production.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the t_{SU(HSE)} startup time
4. t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 to 20 pF range (typical), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 29](#)). C_{L1} and C_{L2} usually have the same size. The crystal manufacturer typically specifies a load capacitance, which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate for the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to AN2867 “Oscillator design guide for ST microcontrollers”, available from www.st.com.

Figure 29. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph is based on design simulation results obtained with typical external components specified in [Table 43](#). In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

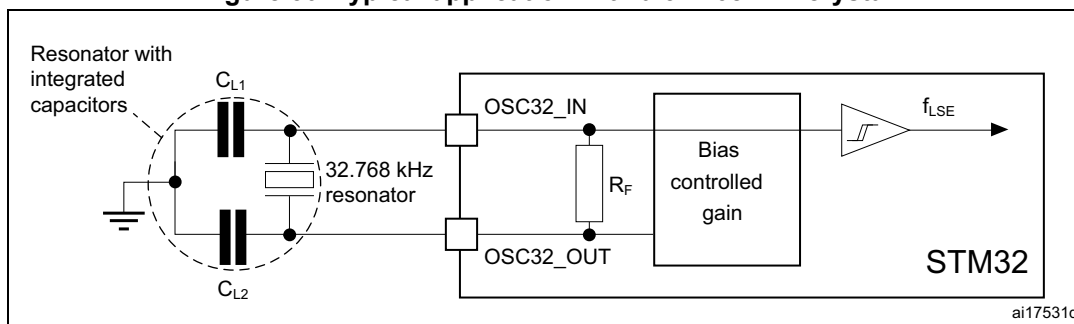
Table 43. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I _{DD}	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	246	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	333	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	462	-	
		LSEDRV[1:0] = 11 High drive capability	-	747	-	
G _m _{critmax}	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	μA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
t _{SU(LSE)} ⁽³⁾	Startup time	V _{DD} is stabilized	-	2	-	s

1. Specified by design - Not tested in production.
2. Refer to the note and caution paragraphs below the table, and to AN2867 "Oscillator design guide for ST microcontrollers".
3. t_{SU(LSE)} is the startup time measured from the moment it is enabled (by software) to when a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to AN2867 "Oscillator design guide for ST microcontrollers", available from www.st.com.

Figure 30. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

5.3.9 Internal clock source characteristics

The parameters given in Table 44 to Table 47 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 20.

48 MHz high-speed internal RC oscillator (HSI48)

Table 44. HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{HSI48}	HSI48 frequency	V _{DD} = 3.3 V, T _J = 30 °C	47.5 ⁽¹⁾	48	48.5 ⁽¹⁾	MHz
TRIM ⁽³⁾	User trimming step	-	-	0.175	0.250	%
USER TRIM COVERAGE ⁽²⁾	User trimming coverage	±32 steps	±4.70	±5.6	-	
DuCy(HSI48) ⁽³⁾	Duty cycle	-	45	-	55	%
ACCCHSI48_REL ⁽³⁾	Accuracy of the HSI48 oscillator over temperature (reference is 30 °C)	T _J = -40 to 130 °C	-4.5	-	4	%
ΔV _{DD} (HSI48)	HSI48 oscillator frequency drift with V _{DD} (reference is 3.3 V)	V _{DD} = 3.0 to 3.6 V	-	0.025	0.05	%
		V _{DD} = 1.71 to 3.6 V	-	0.05	0.1	
t _{su} (HSI48) ⁽³⁾	HSI48 oscillator start-up time	-	-	2.1	4.0	μs
I _{DD} (HSI48) ⁽³⁾	HSI48 oscillator power consumption	-	-	350	400	μA
N _T jitter ⁽³⁾	Next transition jitter accumulated jitter on 28 cycles	-	-	±0.15	-	ns
P _T jitter ⁽³⁾	Paired transition jitter accumulated jitter on 56 cycles ⁽⁴⁾	-	-	±0.25	-	

1. Calibrated during manufacturing tests.
2. Evaluated by characterization - Not tested in production.
3. Specified by design - Not tested in production.
4. Jitter measurements are performed without clock sources activated in parallel.

64 MHz high-speed internal RC oscillator (HSI)

Table 45. HSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{HSI}	Frequency	V _{DD} = 3.3 V, T _J = 30 °C	63.7 ⁽²⁾	64.0 ⁽²⁾	64.3 ⁽²⁾	MHz
TRIM	User trimming step	Trimming is not a multiple of 32 ⁽³⁾	-	0.24	0.32	%
		Trimming is 128, 256, and 384 ⁽³⁾	-5.2	-1.8	-	
		Trimming is 64, 192, 320, and 488 ⁽³⁾	-1.4	-0.8	-	
		Other trimmings are multiples of 32 (not including multiples of 64 and 128) ⁽³⁾	-0.6	-0.25	-	
DuCy(HSI)	Duty cycle	-	45	-	55	%
ΔV _{DD} (HSI)	Frequency drift with V _{DD} (reference is 3.3 V)	V _{DD} = 1.71 to 3.6 V	-0.12	-	0.03	%
ΔTEMP(HSI)	Frequency drift with V _{DD} (reference is 64 MHz)	T _J = -20 to 105 °C	-1 ⁽⁴⁾	-	1 ⁽⁴⁾	
		T _J = -40 to 130 °C	-2 ⁽⁴⁾	-	1 ⁽⁴⁾	
t _{su} (HSI)	Start-up time	-	-	1.4	2.0	μs
t _{stab} (HSI)	Stabilization time	At 1% of target frequency	-	4	8	μs
		At 1% of target frequency	-	-	4	
I _{DD} (HSI)	Power consumption	-	-	300	450	μA

1. Specified by design - Not tested in production, unless otherwise specified.
2. Calibrated during manufacturing tests.
3. Trimming value of HSICAL[8:0].
4. Guaranteed by characterization - Not tested in production.

4 MHz low-power internal RC oscillator (CSI)

Table 46. CSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{CSI}	Frequency	V _{DD} = 3.3 V, T _J = 30 °C	3.96 ⁽²⁾	4	4.04 ⁽²⁾	MHz
TRIM	User trimming step	Trimming is not a multiple of 16	-	0.40	0.75	%
		Trimming is not a multiple of 32	-4.75	-2.75	0.75	
		Other trimmings are a multiple of 32 (not including multiples of 64 and 128)	-0.43	0.00	0.75	
DuCy(CSI)	Duty cycle	-	45	-	55	%
ΔTEMP(CSI)	Frequency drift over temperature	T _J = 0 to 85 °C	-3.7 ⁽³⁾	-	4.5 ⁽³⁾	%
		T _J = -40 to T _J = 130 °C	-11 ⁽³⁾	-	7.5 ⁽³⁾	%
ΔV _{DD} (CSI)	Frequency drift over V _{DD}	V _{DD} = 1.71 to 3.6 V	-0.06	-	0.06	%
t _{su} (CSI)	Start-up time	-	-	1	2	μs

Table 46. CSI oscillator characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{stab} (CSI)	Stabilization time (to reach ± 3% of f _{CSI})	-	-	-	4	cycle
I _{DD} (CSI)	Power consumption	-	-	23	30	µA

1. Specified by design - Not tested in production, unless otherwise specified.
2. Calibrated during manufacturing tests.
3. Evaluated by characterization - Not tested in production.

Low-speed internal (LSI) RC oscillator

Table 47. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{LSI}	Frequency	V _{DD} = 3.3 V, T _J = 25 °C	31.4 ⁽¹⁾	32	32.6 ⁽¹⁾	kHz
		T _J = -40 to 110 °C, V _{DD} = 1.71 to 3.6 V	29.76 ⁽²⁾	-	33.6 ⁽²⁾	
		T _J = -40 to 130 °C, V _{DD} = 1.71 to 3.6 V	29.4 ⁽²⁾	-	33.6 ⁽²⁾	
t _{su} (LSI) ⁽³⁾	Start-up time	-	-	80	130	µs
t _{stab} (LSI) ⁽³⁾	Stabilization time (5% of final value)	-	-	120	170	
I _{DD} (LSI) ⁽³⁾	Power consumption	-	-	130	280	

1. Calibrated during manufacturing tests.
2. Evaluated by characterization - Not tested in production.
3. Specified by design - Not tested in production.

5.3.10 PLL characteristics

The parameters given in [Table 48](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

Table 48. PLL characteristics (wide VCO frequency range)⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{PLL_IN}	PLL input clock	-	2	-	16	MHz
	PLL input clock duty cycle	-	10	-	90	%
f _{PLL_P_OUT}	PLL multiplier output clock P, Q, R	VOS0	1	-	250 ⁽²⁾	MHz
		VOS1	1	-	200 ⁽²⁾	
		VOS2	1	-	150 ⁽²⁾	
		VOS3	1	-	100 ⁽²⁾	
f _{VCO_OUT}	PLL VCO output	-	128	-	560 ⁽²⁾	
t _{LOCK}	PLL lock time	Normal mode	-	45	100 ⁽³⁾	µs
		Sigma-delta mode (f _{PLL_IN} ≥ 8 MHz)	-	60	120 ⁽³⁾	

Table 48. PLL characteristics (wide VCO frequency range)⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Jitter	Cycle-to-cycle jitter	$f_{VCO_OUT} = 128$ MHz	-	60	-	±ps	
		$f_{VCO_OUT} = 200$ MHz	-	50	-		
		$f_{VCO_OUT} = 400$ MHz	-	20	-		
		$f_{VCO_OUT} = 560$ MHz	-	15	-		
	Long term jitter	Normal mode ($f_{PLL_IN} = 2$ MHz), $f_{VCO_OUT} = 560$ MHz	-	±0.2	-	%	
		Normal mode ($f_{PLL_IN} = 16$ MHz), $f_{VCO_OUT} = 560$ MHz	-	±0.8	-		
		Sigma-delta mode ($f_{PLL_IN} = 2$ MHz), $f_{VCO_OUT} = 560$ MHz	-	±0.2	-		
		Sigma-delta mode ($f_{PLL_IN} = 16$ MHz), $f_{VCO_OUT} = 560$ MHz	-	±0.8	-		
$I_{DD}(PLL)$	PLL power consumption on V_{DD}	$f_{VCO_OUT} = 560$ MHz	V_{DD}	-	330	420	µA
			V_{CORE}	-	630	-	
		$f_{VCO_OUT} = 128$ MHz	V_{DD}	-	155	230	
			V_{CORE}	-	170	-	

1. Specified by design - Not tested in production, unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.
3. Evaluated by characterization - Not tested in production.

Table 49. PLL characteristics (medium VCO frequency range)

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
f_{PLL_IN}	PLL input clock	-	1	-	2	MHz
	PLL input clock duty cycle	-	10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS0	1.17	-	210	MHz
		VOS1	1.17	-	210	
		VOS2	1.17	-	160 ⁽²⁾	
		VOS3	1.17	-	88 ⁽²⁾	
f_{VCO_OUT}	PLL VCO output	-	150	-	420	
t_{LOCK}	PLL lock time	Normal mode	-	45	80 ⁽³⁾	µs
		Sigma-delta mode	Forbidden			

Table 49. PLL characteristics (medium VCO frequency range) (continued)

Symbol	Parameter	Conditions		Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
Jitter	Cycle-to-cycle jitter	$f_{VCO_OUT} = 150 \text{ MHz}$	-	-	60	-	±ps
		$f_{VCO_OUT} = 200 \text{ MHz}$	-	-	40	-	
		$f_{VCO_OUT} = 400 \text{ MHz}$	-	-	18	-	
		$f_{VCO_OUT} = 420 \text{ MHz}$	-	-	15	-	
	Period jitter	$f_{VCO_OUT} = 150 \text{ MHz}$	$f_{PLL_OUT} = 50 \text{ MHz}$	-	75	-	
		$f_{VCO_OUT} = 400 \text{ MHz}$		-	25	-	
Long term jitter	Normal mode $f_{VCO_OUT} = 400 \text{ MHz}$		-	±0.2	-	%	
$I_{DD(PLL)}$	PLL power consumption on V_{DD}	$f_{VCO_OUT} = 420 \text{ MHz}$	V_{DD}	-	275	360	µA
			V_{CORE}	-	450	-	
		$f_{VCO_OUT} = 150 \text{ MHz}$	V_{DD}	-	160	240	
			V_{CORE}	-	165	-	

1. Specified by design - Not tested in production, unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.
3. Evaluated by characterization - Not tested in production.

5.3.11 Memory characteristics

Flash memory

The characteristics are given at $T_J = -40$ to $130 \text{ }^\circ\text{C}$ unless otherwise specified.

The devices are shipped to customers with the flash memory erased.

Table 50. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
I_{DD}	Supply current	Word program ⁽²⁾	-	2.5	3.6	mA
		Sector erase	-	1.8	4	
		Mass erase	-	2.0	4	

1. Specified by design - Not tested in production
2. Data are evaluated with a write of 50% of the programmed bits equal to 0.

Table 51. Flash memory programming⁽¹⁾

Symbol	Parameter	Conditions	Min ⁽²⁾	Typ	Max ⁽¹⁾	Unit
t_{prog}	Word program time	128 bits (user area)	-	31	-	µs
		16 bits (OTP area)	-	31	-	
t_{ERASE}	Sector erase time (8 Kbytes)	-	-	2	10.5	ms
t_{ME}	Mass erase time	-	-	2	2.68	s
V_{prog}	Programming voltage	-	1.71	-	3.6	V

1. Data are valid for program memory and high-cycling data memory.

2. Specified by design - Not tested in production.

Table 52. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit
N _{PEND}	Endurance program memory	T _J = -40 to +130 °C	10	kcycles
N _{DEND}	Endurance data memory	T _J = -40 to +130 °C	100	
t _{PRET}	Program memory, data retention	1 kcycle at T _A = 125 °C	10	Years
		1 kcycles at T _A = 85 °C	30	
		10 kcycles at T _A = 55 °C	30	
t _{DRET}	Data retention for data memory	100 kcycle at T _A = 125 °C	1	
		100 kcycles at T _A = 85 °C	10	
		100 kcycles at T _A = 55 °C	10	

1. Evaluated by characterization - Not tested in production, unless otherwise specified.

5.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)**, positive and negative, is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows to resume normal operation.

The test results are given in [Table 53](#). They are based on the EMS levels and classes defined in AN1709 “EMC design guide for STM8, STM32 and legacy MCUs”.

Table 53. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V _{FESD}	Voltage limits to apply on any I/O pin to induce a functional disturbance	V _{DD} = 3.3 V, T _A = 25 °C, LQFP176-SMPS, f _{rcc_cpu_ck} = 250 MHz, conform to IEC 61000-4-2	2B
V _{FTB}	Fast transient voltage burst limits to apply through 100 pF on V _{DD} and V _{SS} pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ), located as close as possible to the MCU, to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. Note that good EMC performance is highly dependent upon the user application, and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for its application.

Software recommendations

The software flow must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (such as control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or on the oscillator pins for 1 s.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015 “Software techniques for improving microcontrollers EMC performance”).

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard, which specifies the test board and the pin loading.

Table 54. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f _{HSE} /f _{CPU}]	Unit
				25/250 MHz	
S _{EMI}	Peak level ⁽¹⁾	V _{DD} = 3.6 V, T _A = 25 °C, LQFP176-SMPS package, conforming to IEC61967-2	0.1 to 30 MHz	21	dBμV
			30 to 130 MHz	22	
			130 MHz to 1 GHz	29	
			1 GHz to 2 GHz	21	
			EMI level	4	-

1. Refer to the EMI radiated test chapter of application note AN1709 “EMC design guide for STM8, STM32 and legacy MCUs” available from the ST website www.st.com.

5.3.13 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive pulse followed by a negative one) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 55. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = 25 °C conforming to ANSI/ESDA/JEDEC JS-001	Packages with SMPS	1C	1000 ⁽²⁾	V
			Packages without SMPS	2	2000	
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All packages	C2a	500	V

1. Evaluated by characterization - Not tested in production.
2. The electrostatic discharge is 2000 V for all pins, except V_{FBSMPS}, for which the test fails at 2000 V and passes at 1600 V.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with the JESD78 IC latch-up standard.

Table 56. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T _J = 130 °C, conforming to JESD78	II level A

5.3.14 I/O current injection characteristics

As a general rule, avoid current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) during the normal product operation. To give an indication of the device robustness when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the characterization.

Functional susceptibility to I/O current injection

While a simple application is executed, the device is stressed by injecting current into the I/O pins (one at the time) programmed in floating input mode, and checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain

limit (higher than 5 LSB TUE), out of conventional limits (-5 / +0 µA range) of induced leakage current on adjacent pins, or other functional failures (such as reset, oscillator frequency deviation).

Table 57 shows I/Os current injection susceptibility data. Negative/positive induced leakage currents are caused, respectively, by negative/positive injection.

Table 57. I/O current injection susceptibility⁽¹⁾

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I _{INJ}	Injected current on pins PA4, PA5, PB2, PB12, PC14, PC15, PD8, and PH2	0	0	mA
	Injected current on all other pins	5	N/A	

1. Evaluated by characterization - Not tested in production.

5.3.15 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 58 are derived from tests performed under the conditions summarized in Table 20. All I/Os are CMOS and TTL compliant (except for BOOT0).

Note: For information on GPIO configuration, refer to AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption”, available on www.st.com.

Table 58. I/O static characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IL}	I/O input low level voltage except BOOT0	1.08 V < V _{DD} < 3.6 V	-	-	0.3 V _{DDIOx} ⁽²⁾	V
	I/O input low level voltage except BOOT0		-	-	0.4 V _{DDIOx} - 0.1 ⁽³⁾	
	BOOT0 I/O input low level voltage		-	-	0.19 V _{DDIOx} + 0.1 ⁽³⁾	
V _{IH}	I/O input high level voltage except BOOT0	1.08 V < V _{DD} < 3.6 V	0.7 V _{DDIOx} ⁽²⁾	-	-	V
	I/O input high level voltage except BOOT0		0.52 V _{DDIOx} + 0.18 ⁽³⁾	-	-	
	BOOT0 I/O input high level voltage		0.17 V _{DDIOx} + 0.6 ⁽³⁾	-	-	
V _{HYS} ⁽³⁾	TT_xx, FT_xxx and NRST I/O input hysteresis	1.08 V < V _{DD} < 3.6 V	-	250	-	mV
	BOOT0 I/O input hysteresis	1.71 V < V _{DD} < 3.6 V	-	200	-	

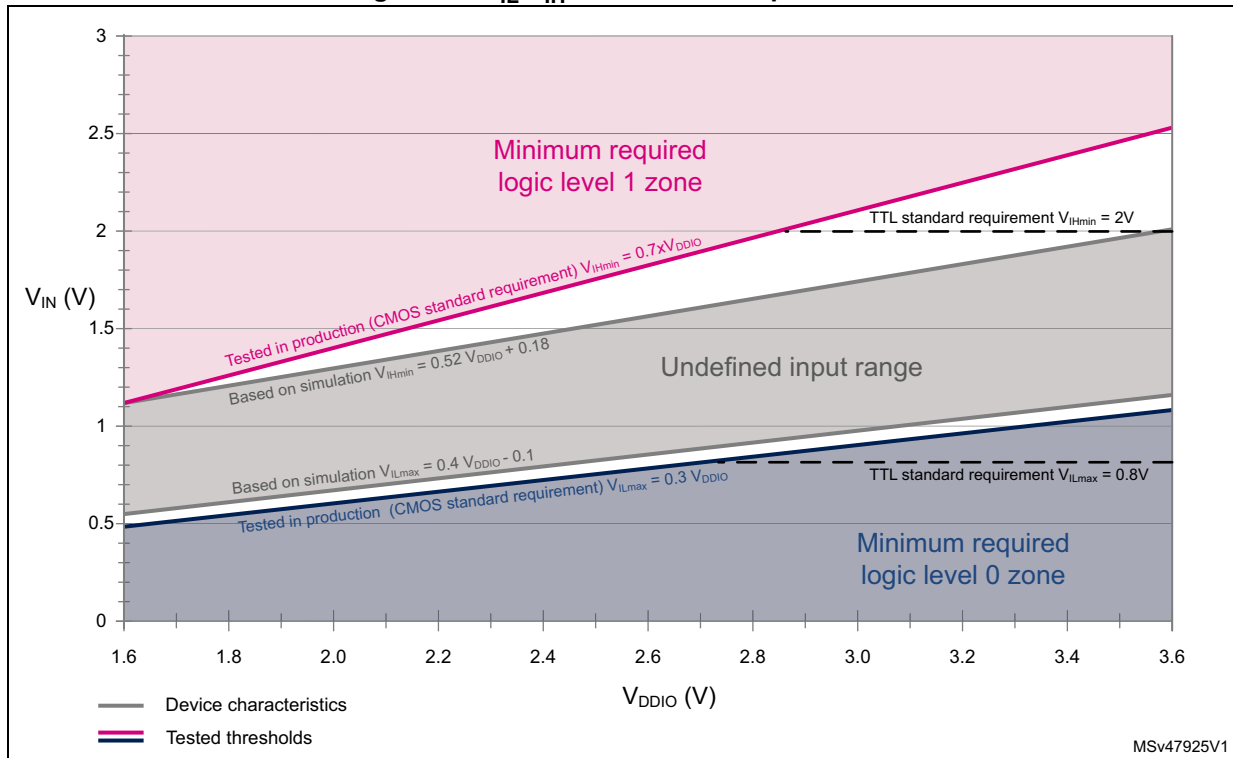
Table 58. I/O static characteristics⁽¹⁾ (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{leak} ⁽⁴⁾	FT_xx input leakage current ⁽³⁾	$0 < V_{IN} \leq \text{Max}(V_{DDXXX})^{(7)}$	-	-	±200	nA
		$\text{Max}(V_{DDXXX}) < V_{IN} \leq \text{Max}(V_{DDXXX}) + 1 \text{ V}^{(5)(7)}$	-	-	2500	
		$\text{Max}(V_{DDXXX}) < V_{IN} \leq 5.5 \text{ V}^{(5)(7)}$	-	-	750	
	TT_xx Input leakage current	$0 < V_{IN} \leq \text{Max}(V_{DDXXX})^{(7)}$	-	-	±200	
	BOOT0	$0 < V_{IN} \leq V_{DDOX}$	-	-	15	
R _{PU}	Weak pull-up equivalent resistor ⁽⁶⁾	$V_{IN} = V_{SS}$	30	40	50	kΩ
R _{PD}	Weak pull-down equivalent resistor ⁽⁶⁾	$V_{IN} = V_{DD}^{(7)}$	30	40	50	
C _{IO}	I/O pin capacitance	-	-	5	-	pF

- V_{DDIOx} represents V_{DD} or V_{DDIO2}.
- Compliant with CMOS requirements.
- Specified by design - Not tested in production.
- This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: I_{Total_leak_max} = 10 μA + [number of I/Os where V_{IN} is applied on the pad] × I_{lkg(Max)}.
- V_{IN} must be lower than Max(V_{DDXXX}) + 3.6 V.
- The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10%).
- Max(V_{DDXXX}) is the maximum value of all the I/O supplies.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in [Figure 31](#).

Figure 31. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#). In particular:

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 18](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 18](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 59](#) and [Table 61](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#). All I/Os are CMOS and TTL compliant.

Table 59. Output voltage characteristics for all I/Os except PC13, PC14, PC15, and PI8

Symbol	Parameter	Conditions ⁽¹⁾	Min	Max	Unit
V _{OL}	Output low level voltage	CMOS port ⁽²⁾ , I _{IO} = 8 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	-	0.4	V
V _{OH}	Output high level voltage	CMOS port ⁽²⁾ , I _{IO} = -8 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	V _{DD} - 0.4	-	
V _{OL} ⁽³⁾	Output low level voltage	TTL port ⁽²⁾ , I _{IO} = 8 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
V _{OH} ⁽³⁾	Output high level voltage	TTL port ⁽²⁾ , I _{IO} = -8 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	2.4	-	
V _{OL} ⁽³⁾	Output low level voltage	I _{IO} = 20 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	-	1.3	
V _{OH} ⁽³⁾	Output high level voltage	I _{IO} = -20 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	V _{DD} - 1.3	-	
V _{OL} ⁽³⁾	Output low level voltage	I _{IO} = 4 mA 1.71 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
V _{OH} ⁽³⁾	Output high level voltage	I _{IO} = -4 mA 1.71 V ≤ V _{DD} < 3.6 V	V _{DD} - 0.4	-	
V _{OL} ⁽³⁾	Output low level voltage	I _{IO} = 2 mA 1.08 V ≤ V _{DD} ≤ 1.32 V	-	0.3 V _{DDIO2}	
V _{OH} ⁽³⁾	Output high level voltage	I _{IO} = -2 mA 1.71 V ≤ V _{DD} < 1.32 V	0.7 V _{DDIO2}	-	
V _{OLFM+} ⁽³⁾	Output low level voltage for an FTf I/O pin in (FT I/O with "f" option)	I _{IO} = 20 mA 2.3 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
		I _{IO} = 10 mA 1.71 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
		I _{IO} = 4.5 mA 1.08 V ≤ V _{DD} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 17](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Table 60. Output voltage characteristics for FT_c I/Os

Symbol	Parameter	Conditions ⁽¹⁾	Min	Max	Unit
V _{OL}	Output low level voltage	CMOS port ⁽²⁾ , I _{IO} = 2 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	-	0.4	V
V _{OH}	Output high level voltage	CMOS port ⁽²⁾ , I _{IO} = -2 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	V _{DD} - 0.4	-	
V _{OL} ⁽³⁾	Output low level voltage	TTL port ⁽²⁾ , I _{IO} = 2 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
V _{OH} ⁽³⁾	Output high level voltage	TTL port ⁽²⁾ , I _{IO} = -2 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	2.4	-	
V _{OL} ⁽³⁾	Output low level voltage	I _{IO} = 1 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
V _{OH} ⁽³⁾	Output high level voltage	I _{IO} = -1 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	V _{DD} - 0.4	-	
V _{OL} ⁽³⁾	Output low level voltage	I _{IO} = 0.1 mA 1.71 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
V _{OH} ⁽³⁾	Output high level voltage	I _{IO} = -0.1 mA 1.71 V ≤ V _{DD} < 3.6 V	V _{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 17](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Table 61. Output voltage characteristics for PC13 and PI8⁽¹⁾

Symbol	Parameter	Conditions ⁽³⁾	Min	Max	Unit
V _{OL}	Output low level voltage	CMOS port ⁽²⁾ , I _{IO} = 3 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	-	0.4	V
V _{OH}	Output high level voltage	CMOS port ⁽²⁾ , I _{IO} = -3 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	V _{DD} - 0.4	-	
V _{OL} ⁽³⁾	Output low level voltage	TTL port ⁽²⁾ , I _{IO} = 3 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
V _{OH} ⁽³⁾	Output high level voltage	TTL port ⁽²⁾ , I _{IO} = -3 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	2.4	-	
V _{OL} ⁽³⁾	Output low level voltage	I _{IO} = 1.5 mA 1.71 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
V _{OH} ⁽³⁾	Output high level voltage	I _{IO} = -1.5 mA 1.71 V ≤ V _{DD} ≤ 3.6 V	V _{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 17](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Table 62. Output voltage characteristics for PC14 and PC15⁽¹⁾

Symbol	Parameter	Conditions ⁽³⁾	Min	Max	Unit
V _{OL}	Output low level voltage	CMOS port ⁽²⁾ , I _{IO} = 0.5 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	-	0.4	V
V _{OH}	Output high level voltage	CMOS port ⁽²⁾ , I _{IO} = -0.5 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	V _{DD} - 0.4	-	
V _{OL} ⁽³⁾	Output low level voltage	TTL port ⁽²⁾ , I _{IO} = 0.5 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
V _{OH} ⁽³⁾	Output high level voltage	TTL port ⁽²⁾ , I _{IO} = -0.5 mA 2.7 V ≤ V _{DD} ≤ 3.6 V	2.4	-	
V _{OL} ⁽³⁾	Output low level voltage	I _{IO} = 0.25 mA 1.71 V ≤ V _{DD} ≤ 3.6 V	-	0.4	
V _{OH} ⁽³⁾	Output high level voltage	I _{IO} = -0.25 mA 1.71 V ≤ V _{DD} ≤ 3.6 V	V _{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 17](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of GPIOx_HSLVR register can be used to optimize the I/O speed when the voltage is below 2.7 V.

Table 63. Output timing characteristics (HSLV OFF)⁽¹⁾

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F _{max} ⁽²⁾⁽³⁾	Maximum frequency	C = 50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	8	MHz
			C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	5	
			C = 40 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	10	
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	5	
			C = 30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	12	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	5	
			C = 20 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	14	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	5	
			C = 10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	16	
	C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	5			
	t _r /t _f ⁽⁴⁾⁽⁵⁾	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	18.0	ns
			C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	36.0	
			C = 40 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	17.0	
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	34.0	
			C = 30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	15.5	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	32.0	
			C = 20 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	14.2	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	30.0	
			C = 10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	12.2	
C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V			-	27		

Table 63. Output timing characteristics (HSLV OFF)⁽¹⁾ (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	F _{max} ⁽²⁾⁽³⁾	Maximum frequency	C = 50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V		40	MHz
			C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	12	
			C = 40 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	45	
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	14	
			C = 30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	50	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	16	
			C = 20 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	55	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	18	
			C = 10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	60	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	20	
	t _r /t _f ⁽⁴⁾⁽⁵⁾	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	6.2	ns
			C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	11.4	
			C = 40 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	5.7	
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	10.5	
			C = 30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	5.1	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	9.5	
			C = 20 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	4.5	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V		8.4	
			C = 10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V		3.7	
C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V		7.0				

Table 63. Output timing characteristics (HSLV OFF)⁽¹⁾ (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	F _{max} ⁽²⁾⁽³⁾	Maximum frequency	C = 50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	80	MHz
			C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	30	
			C = 40 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	90	
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	35	
			C = 30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	100	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	40	
			C = 20 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	110	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	45	
			C = 10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	133	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	50	
	t _r /t _f ⁽⁴⁾⁽⁵⁾	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	3.8	ns
			C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	7.5	
			C = 40 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	3.4	
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	6.6	
			C = 30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	2.9	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	5.7	
			C = 20 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	2.5	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	4.7	
			C = 10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	1.9	
C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	3.7				

Table 63. Output timing characteristics (HSLV OFF)⁽¹⁾ (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
11	F _{max} ⁽²⁾⁽³⁾	Maximum frequency	C = 50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	100	MHz
			C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	40	
			C = 40 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	120	
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	50	
			C = 30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	140	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	60	
			C = 20 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	166	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	70	
			C = 10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	200	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	80	
	t _r /t _f ⁽⁴⁾⁽⁵⁾	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	3.3	ns
			C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	6.3	
			C = 40 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	2.8	
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	5.5	
			C = 30 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	2.3	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	4.6	
			C = 20 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	1.9	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	3.7	
			C = 10 pF, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	1.4	
C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	3				

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the conditions (t_r + t_f) ≤ 2/3 T, Skew ≤ 1/20 T, and 45% < Duty cycle < 55%.
3. When 2 V < V_{DD} < 2.7 V the maximum frequency is between values given for V_{DD} = 1.98 V and V_{DD} = 2.7 V.
4. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
5. When 2 V < V_{DD} < 2.7 V the maximum t_{rise}/t_{fall} is between values given for V_{DD} = 1.98 V and V_{DD} = 2.7 V.

Output buffer timing characteristics (HSLV option enabled)

Table 64. Output timing characteristics (HSLV ON)⁽¹⁾

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F _{max} ⁽²⁾	Maximum frequency	C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	8	MHz
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	10	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	12	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	14	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	16	
	t _r /t _f ⁽³⁾	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	17.8	ns
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	15.8	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	14.4	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	13.1	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	11.4	
01	F _{max} ⁽²⁾	Maximum frequency	C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	40	MHz
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	45	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	50	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	55	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	60	
	t _r /t _f ⁽³⁾⁽⁴⁾	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	7.2	ns
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	6.5	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	5.6	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	4.8	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	3.8	
10	F _{max} ⁽²⁾⁽⁴⁾	Maximum frequency	C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	60	MHz
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	70	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	90	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	110	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	140	
	t _r /t _f ⁽³⁾⁽⁴⁾	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	5.3	ns
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	4.6	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	3.8	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	3.0	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	2.2	

Table 64. Output timing characteristics (HSLV ON)⁽¹⁾ (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
11	F _{max} ⁽²⁾⁽⁴⁾	Maximum frequency	C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	67	MHz
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	100	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	120	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	155	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	200	
	t _r /t _f ⁽³⁾⁽⁴⁾	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	5.0	ns
			C = 40 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	4.1	
			C = 30 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	3.3	
			C = 20 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	2.5	
			C = 10 pF, 1.71 V ≤ V _{DD} ≤ 2 V	-	1.8	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the conditions: (t_r+t_f) ≤ 2/3 T, Skew ≤ 1/20 T, 45% < Duty cycle < 55%.
3. The fall and rise times are defined, respectively, between 90 and 10% and between 10 and 90% of the output waveform.
4. Compensation system enabled.

Table 65. Output timing characteristics V_{DDIO2} 1.2 V range (HSLV OFF)⁽¹⁾

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F _{max} ⁽²⁾	Maximum frequency	C = 50 pF, 1.08 V ≤ V _{DDIO2} ≤ 1.32 V	-	1	MHz
			C = 40 pF, 1.08 V ≤ V _{DDIO2} ≤ 1.32 V	-	1	
			C = 30 pF, 1.08 V ≤ V _{DDIO2} ≤ 1.32 V	-	1	
			C = 20 pF, 1.08 V ≤ V _{DDIO2} ≤ 1.32 V	-	1	
			C = 10 pF, 1.08 V ≤ V _{DDIO2} ≤ 1.32 V	-	1	
	t _r /t _f ⁽³⁾	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ V _{DDIO2} ≤ 1.32 V	-	83.0	ns
			C = 40 pF, 1.08 V ≤ V _{DDIO2} ≤ 1.32 V	-	79.0	
			C = 30 pF, 1.08 V ≤ V _{DDIO2} ≤ 1.32 V	-	46.0	
			C = 20 pF, 1.08 V ≤ V _{DDIO2} ≤ 1.32 V	-	72.0	
			C = 10 pF, 1.08 V ≤ V _{DDIO2} ≤ 1.32 V	-	68.0	

Table 65. Output timing characteristics V_{DDIO2} 1.2 V range (HSLV OFF)⁽¹⁾ (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	$F_{max}^{(2)}$	Maximum frequency	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5	MHz
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5	
	$t_r/t_f^{(3)}$	Output high to low level fall time and output low to high level rise time	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	24.5	ns
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	22.2	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	20.0	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	17.8	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	15.0	
10	$F_{max}^{(2)}$	Maximum frequency	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	10	MHz
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	10	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	10	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	10	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	10	
	$t_r/t_f^{(3)}$	Output high to low level fall time and output low to high level rise time	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	16.2	ns
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	14.3	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	12.2	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	10.0	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	7.9	
11	$F_{max}^{(2)(4)}$	Maximum frequency	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	20	MHz
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	23	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	25	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	28	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	30	
	$t_r/t_f^{(3)(4)}$	Output high to low level fall time and output low to high level rise time	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	14.0	ns
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	12.0	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	10.0	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	8.0	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	6.0	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the conditions $(t_r + t_f) \leq 2/3 T$, $Skew \leq 1/20 T$, $45\% < \text{Duty cycle} < 55\%$.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Table 66. Output timing characteristics V_{DDIO2} 1.2 V (HSLV ON)⁽¹⁾

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	$F_{\max}^{(2)}$	Maximum frequency	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5	MHz
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5	
	$t_r/t_f^{(3)}$	Output high to low level fall time and output low to high level rise time	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	32.5	ns
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	30.0	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	27.5	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	25.0	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	22.5	
01	$F_{\max}^{(2)}$	Maximum frequency	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	15.0	MHz
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	17.5	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	20.0	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	22.5	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	25.0	
	$t_r/t_f^{(3)}$	Output high to low level fall time and output low to high level rise time	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	14.6	ns
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	12.9	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	11.2	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	9.3	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	7.3	
10	$F_{\max}^{(2)(4)}$	Maximum frequency	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	25	MHz
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	30	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	33	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	44	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	55	
	$t_r/t_f^{(3)(4)}$	Output high to low level fall time and output low to high level rise time	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	11.6	ns
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	9.7	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	7.8	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	6.1	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	4.3	

Table 66. Output timing characteristics V_{DDIO2} 1.2 V (HSLV ON)⁽¹⁾ (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
11	$F_{max}^{(2)(4)}$	Maximum frequency	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	30	MHz
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	35	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	44	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	55	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	77	
	$t_r/t_f^{(3)(4)}$	Output high to low level fall time and output low to high level rise time	$C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	11.1	ns
			$C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	9.2	
			$C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	7.2	
			$C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	5.4	
			$C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$	-	3.6	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the conditions $(t_r + t_f) \leq 2/3 T$, $Skew \leq 1/20 T$, $45\% < \text{Duty cycle} < 55\%$.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Table 67. Output timing characteristics for FT_c I/Os (PB13/PB14)⁽¹⁾⁽²⁾

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F_{max}	Maximum frequency	$C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{DDIO} \leq 3.6 \text{ V}$	-	2	MHz
			$C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{DDIO} < 2.7 \text{ V}$	-	1	
	t_r/t_f	Output rise and fall time	$C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{DDIO} < 3.6 \text{ V}$	-	166	ns
			$C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{DDIO} < 2.7 \text{ V}$	-	330	
01	F_{rmax}	Maximum frequency	$C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{DDIO} < 3.6 \text{ V}$	-	10	MHz
			$C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{DDIO} < 2.7 \text{ V}$	-	4	
	t_r/t_f	Output rise and fall time	$C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{DDIO} < 3.6 \text{ V}$	-	33	ns
			$C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{DDIO} < 2.7 \text{ V}$	-	65	

1. Specified by design - Not tested in production.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the product reference manual for a description of GPIO port configuration register.

5.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 58](#)).

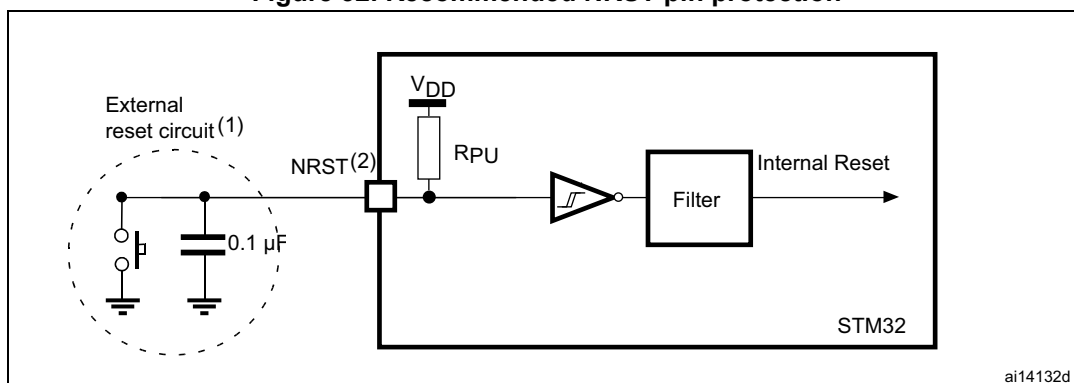
Unless otherwise specified, the parameters in [Table 68](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

Table 68. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{PU}^{(2)}$	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
$V_{F(NRST)}^{(2)}$	NRST input filtered pulse	$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	50	ns
$V_{NF(NRST)}^{(2)}$	NRST input not filtered pulse	$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	350	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. The PMOS contribution to the series resistance is minimum (~10 % order).
2. Specified by design - Not tested in production.

Figure 32. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 58](#), otherwise the reset is not taken into account by the device.

5.3.17 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length to ensure its detection by the event controller.

Table 69. EXTI input characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Specified by design - Not tested in production.

5.3.18 FMC characteristics

Unless otherwise specified, the parameters given in tables [70](#) to [83](#) are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 11$
- Measurement points are done at CMOS levels: $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7\text{ V}$
- VOS level set to VOS0

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics.

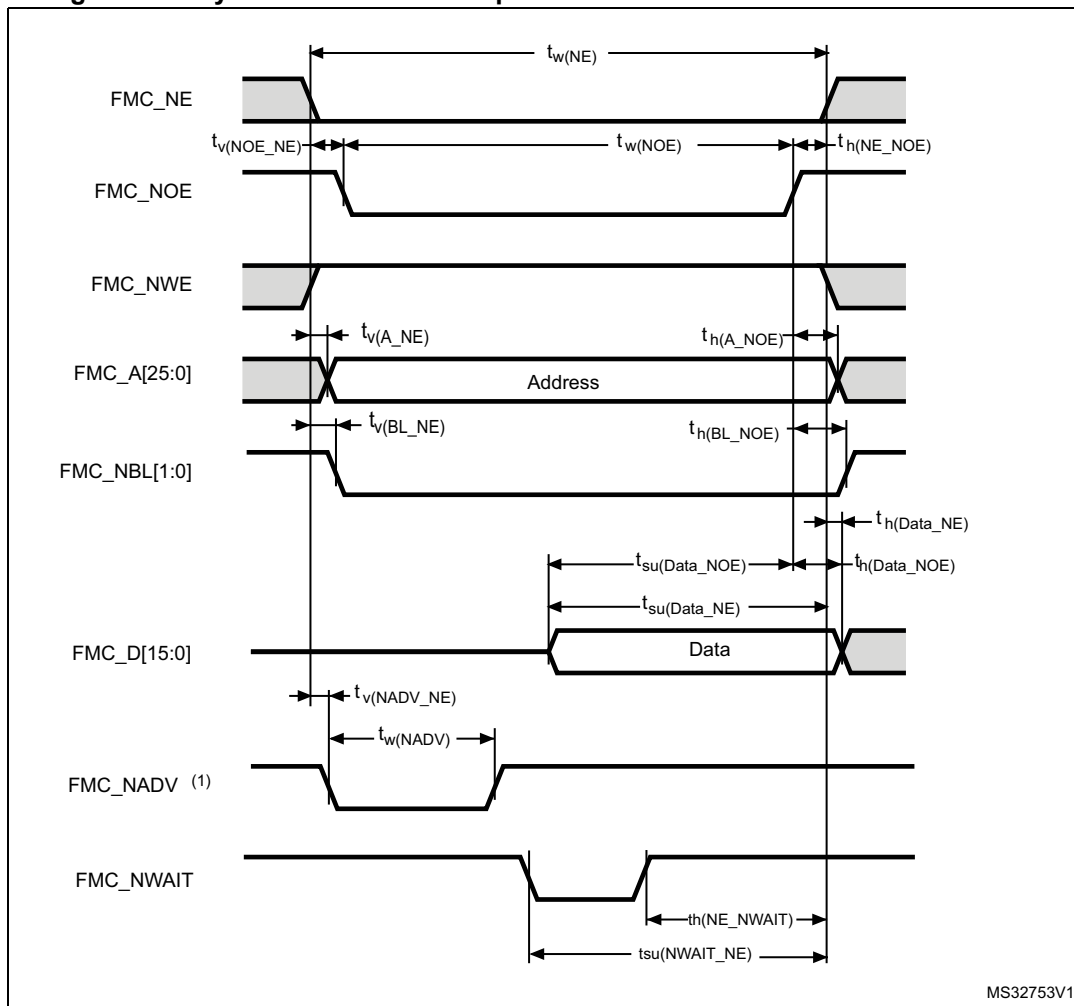
Asynchronous waveforms and timings

Figures 33 through 35 represent asynchronous waveforms, tables 70 through 77 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load $C_L = 30 \text{ pF}$

In all timing tables, the $T_{fmc_ker_ck}$ is the f_{HCLK} clock period.

Figure 33. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 70. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3 T_{fmc_ker_ck} - 1$	$3 T_{fmc_ker_ck} + 1$	ns
$t_{v(NO_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2 T_{fmc_ker_ck} - 1$	$2 T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$2 T_{fmc_ker_ck} - 1.5$	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} + 10$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	9	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck} + 1$	

1. Evaluated by characterization - Not tested in production.

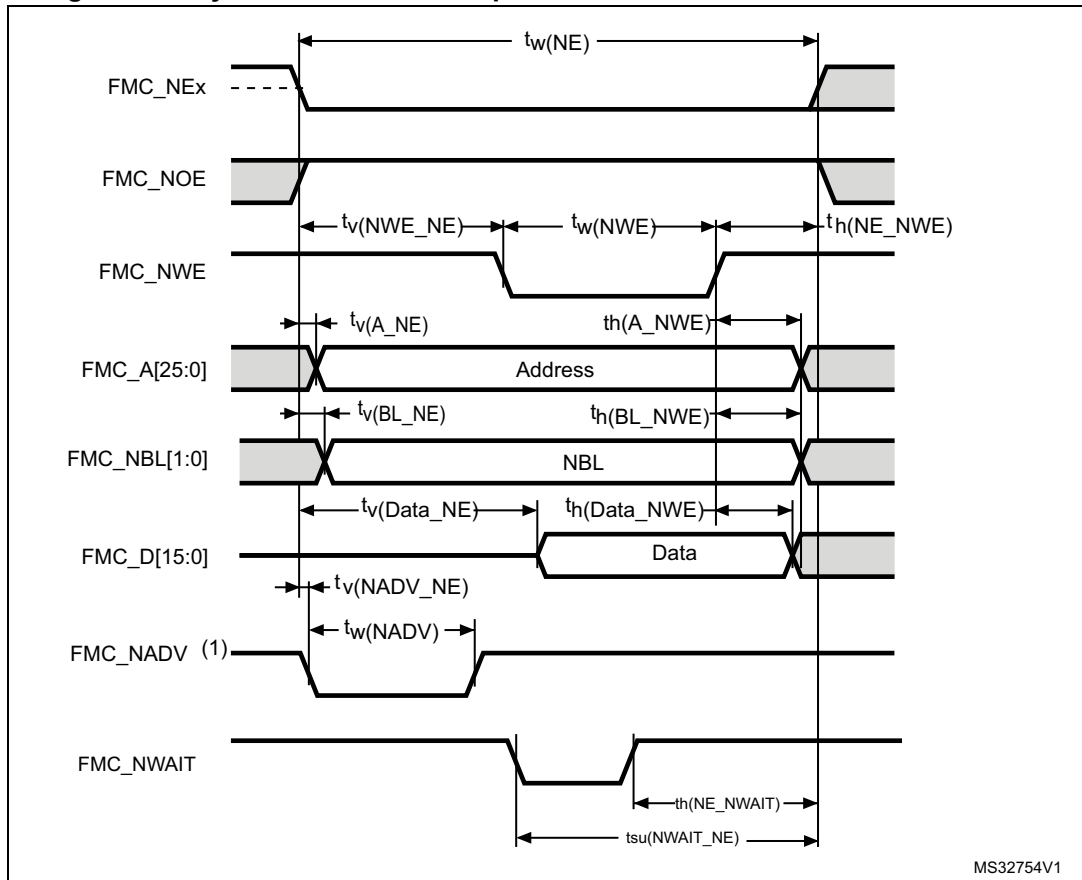
Table 71. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8 T_{fmc_ker_ck} - 1$	$8 T_{fmc_ker_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$7 T_{fmc_ker_ck} - 1$	$7 T_{fmc_ker_ck} + 1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc_ker_ck} - 0.5$	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5 T_{fmc_ker_ck} + 10$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4 T_{fmc_ker_ck} + 10$	-	

1. Evaluated by characterization - Not tested in production.

2. N_{WAIT} pulse width is equal to one fmc_ker_ck cycle.

Figure 34. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



MS32754V1

1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3 T_{fmc_ker_ck} - 1$	$3 T_{fmc_ker_ck} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 1$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck} - 1$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_NBL valid	-	0.5	
$t_{h(BL_NWE)}$	FMC_NBL hold time after FMC_NWE high	$T_{fmc_ker_ck} - 1$	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{fmc_ker_ck} + 1$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck}$	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck} + 1$	

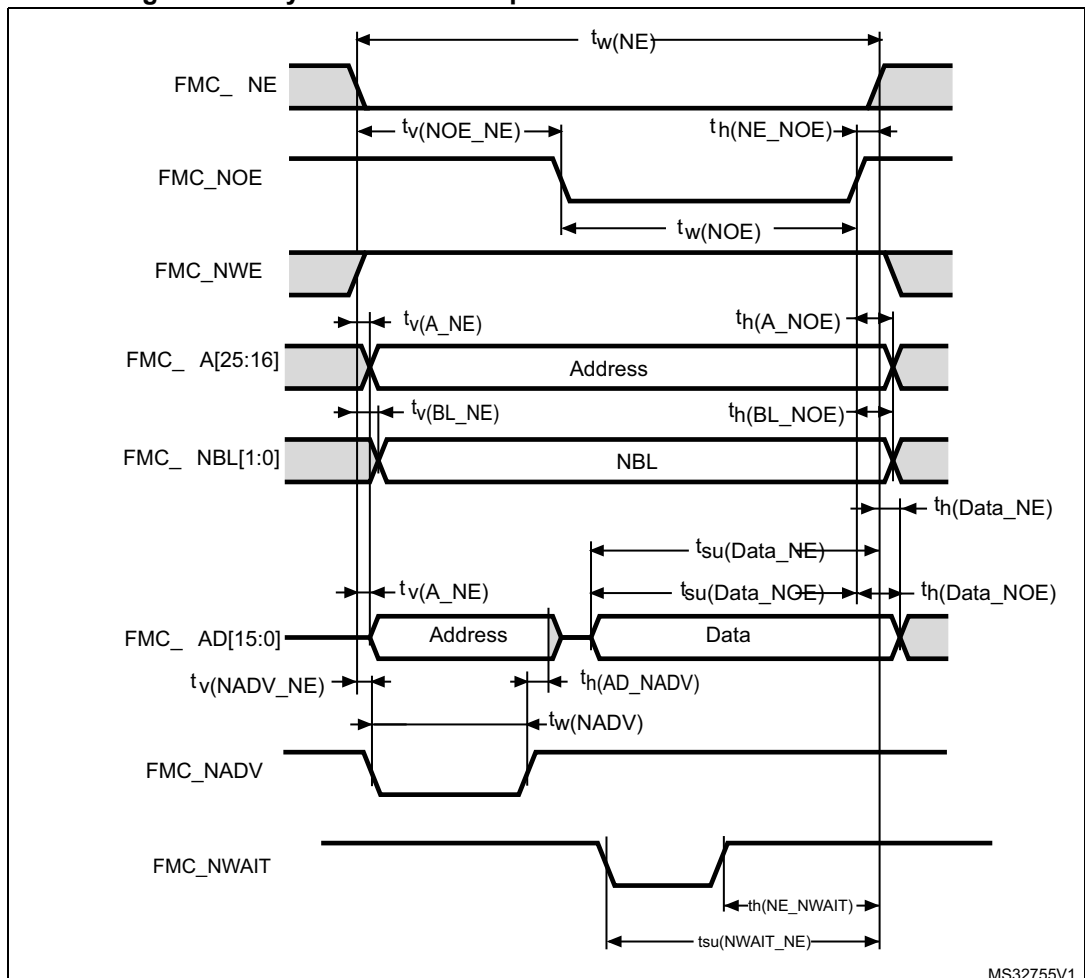
1. Evaluated by characterization - Not tested in production.

Table 73. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8 T_{fmc_ker_ck} - 1$	$8 T_{fmc_ker_ck} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6 T_{fmc_ker_ck} - 1$	$6 T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5 T_{fmc_ker_ck} + 10$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4 T_{fmc_ker_ck} + 10$	-	

1. Evaluated by characterization - Not tested in production.
2. N_{WAIT} pulse width is equal to one fmc_ker_ck cycle.

Figure 35. Asynchronous multiplexed PSRAM/NOR read waveforms



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Table 74. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4 T_{fmc_ker_ck} - 1$	$4 T_{fmc_ker_ck} + 1$	ns
$t_{v(NO_NE)}$	FMC_NEx low to FMC_NOE low	$2 T_{fmc_ker_ck} - 1$	$2 T_{fmc_ker_ck} + 0.5$	
$t_{tw(NO_E)}$	FMC_NOE low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$2 T_{fmc_ker_ck} - 0.5$	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} + 10$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	9	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Evaluated by characterization - Not tested in production.

Table 75. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings^{(1) (2)}

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9 T_{fmc_ker_ck} - 1$	$9 T_{fmc_ker_ck} + 1$	ns
$t_{w(NO_E)}$	FMC_NOE low time	$7 T_{fmc_ker_ck} - 1$	$7 T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4 T_{fmc_ker_ck} + 10$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$3 T_{fmc_ker_ck} + 10$	-	

1. Evaluated by characterization - Not tested in production.

2. NWAIT pulse width is equal to one fmc_ker_ck cycle.

Figure 36. Asynchronous multiplexed PSRAM/NOR write waveforms

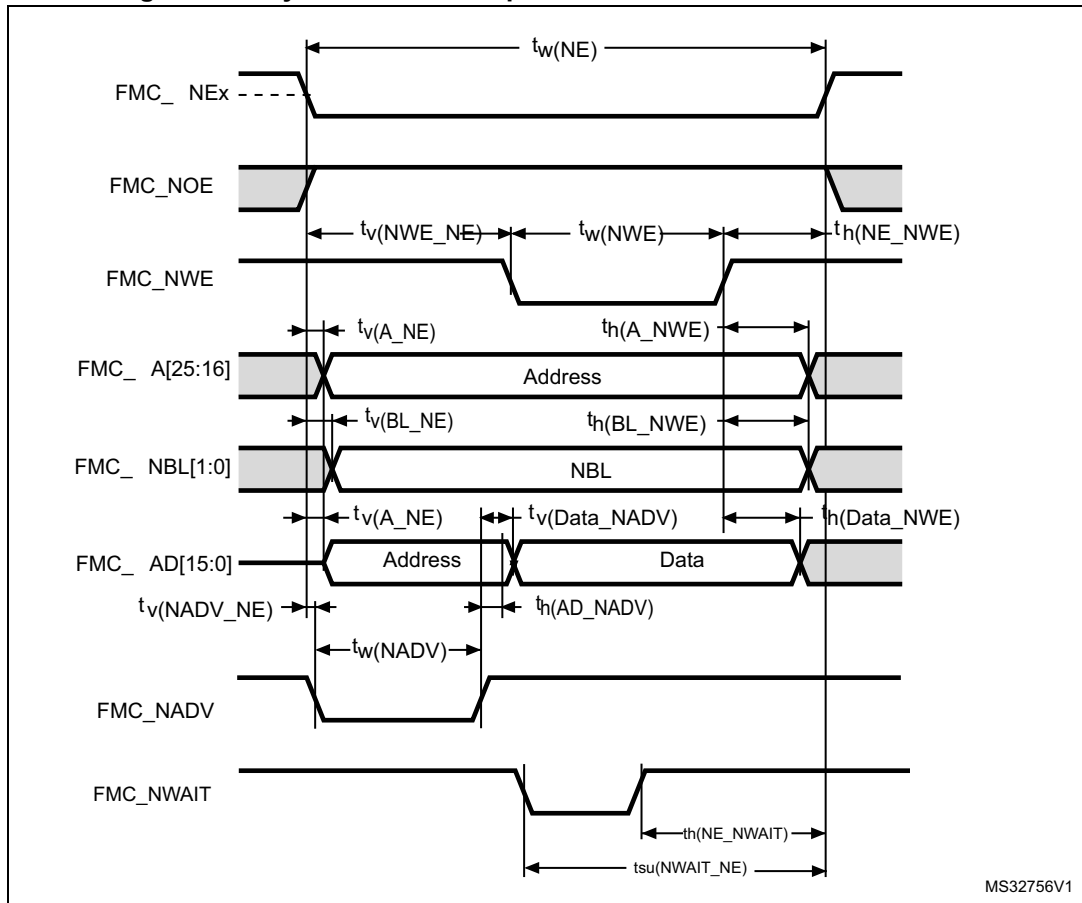


Table 76. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4 T_{fmc_ker_ck} - 1$	$4 T_{fmc_ker_ck} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2 T_{fmc_ker_ck} - 1$	$2 T_{fmc_ker_ck} + 1$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck} - 1$	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck} - 1$	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck} - 1$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc_ker_ck} + 0.5$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck} - 0.5$	-	

1. Evaluated by characterization - Not tested in production.

Table 77. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9 T_{fmc_ker_ck} - 1$	$9 T_{fmc_ker_ck} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7 T_{fmc_ker_ck} - 1$	$7 T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5 T_{fmc_ker_ck} + 10$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4 T_{fmc_ker_ck} + 10$	-	

1. Evaluated by characterization - Not tested in production.

2. N_{WAIT} pulse width is equal to one fmc_ker_ck cycle.

Synchronous waveforms and timings

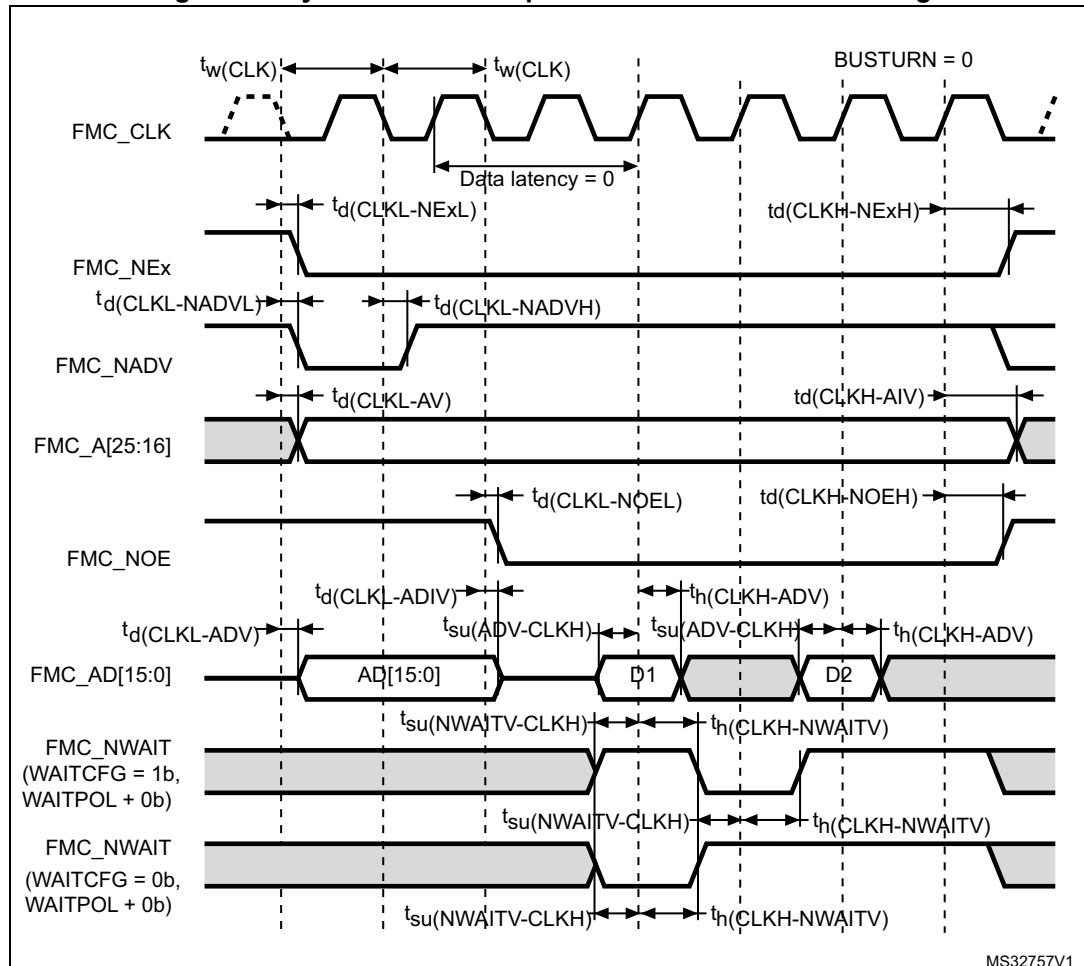
Figures 37 through 40 represent synchronous waveforms, tables 78 through 81 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash, DataLatency = 0 for PSRAM.
- With capacity load $C_L = 30$ pF

In all the timing tables, the $T_{fmc_ker_ck}$ is the $f_{fmc_ker_ck}$ clock period, with the following FMC_CLK maximum values:

- For $2.7\text{ V} < V_{DD} < 3.6\text{ V}$: maximum FMC_CLK = 100 MHz at $C_L = 20$ pF
- For $1.71\text{ V} < V_{DD} < 1.8\text{ V}$: maximum FMC_CLK = 95 MHz at $C_L = 20$ pF
- For $1.71\text{ V} < V_{DD} < 1.8\text{ V}$: maximum FMC_CLK = 100 MHz at $C_L = 15$ pF

Figure 37. Synchronous multiplexed NOR/PSRAM read timings



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Table 78. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{CLK})$	FMC_CLK period	$2T_{\text{fmc_ker_ck}} - 0.5$	-	ns
$t_d(\text{CLKL-NExL})$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	1	
$t_d(\text{CLKH-NExH})$	FMC_CLK high to FMC_NEx high (x = 0..2)	$T_{\text{fmc_ker_ck}} - 1$	-	
$t_d(\text{CLKL-NADVl})$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_d(\text{CLKL-NADVh})$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_d(\text{CLKL-AV})$	FMC_CLK low to FMC_Ax valid (x = 16...25)	-	1	
$t_d(\text{CLKH-AIV})$	FMC_CLK high to FMC_Ax invalid (x = 16...25)	$T_{\text{fmc_ker_ck}} - 1$	-	
$t_d(\text{CLKL-NOEL})$	FMC_CLK low to FMC_NOE low	-	1	
$t_d(\text{CLKH-NOEH})$	FMC_CLK high to FMC_NOE high	$T_{\text{fmc_ker_ck}} + 0.5$	-	
$t_d(\text{CLKL-ADV})$	FMC_CLK low to FMC_AD[15:0] valid	-	3.5	
$t_d(\text{CLKL-ADIV})$	FMC_CLK low to FMC_AD[15:0] invalid	0.5	-	
$t_{\text{su}}(\text{ADV-CLKH})$	FMC_A/D[15:0] valid data before FMC_CLK high	3.5	-	
$t_h(\text{CLKH-ADV})$	FMC_A/D[15:0] valid data after FMC_CLK high	1.5	-	
$t_{\text{su}}(\text{NWAIT-CLKH})$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_h(\text{CLKH-NWAIT})$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Evaluated by characterization - Not tested in production.

Figure 38. Synchronous multiplexed PSRAM write timings

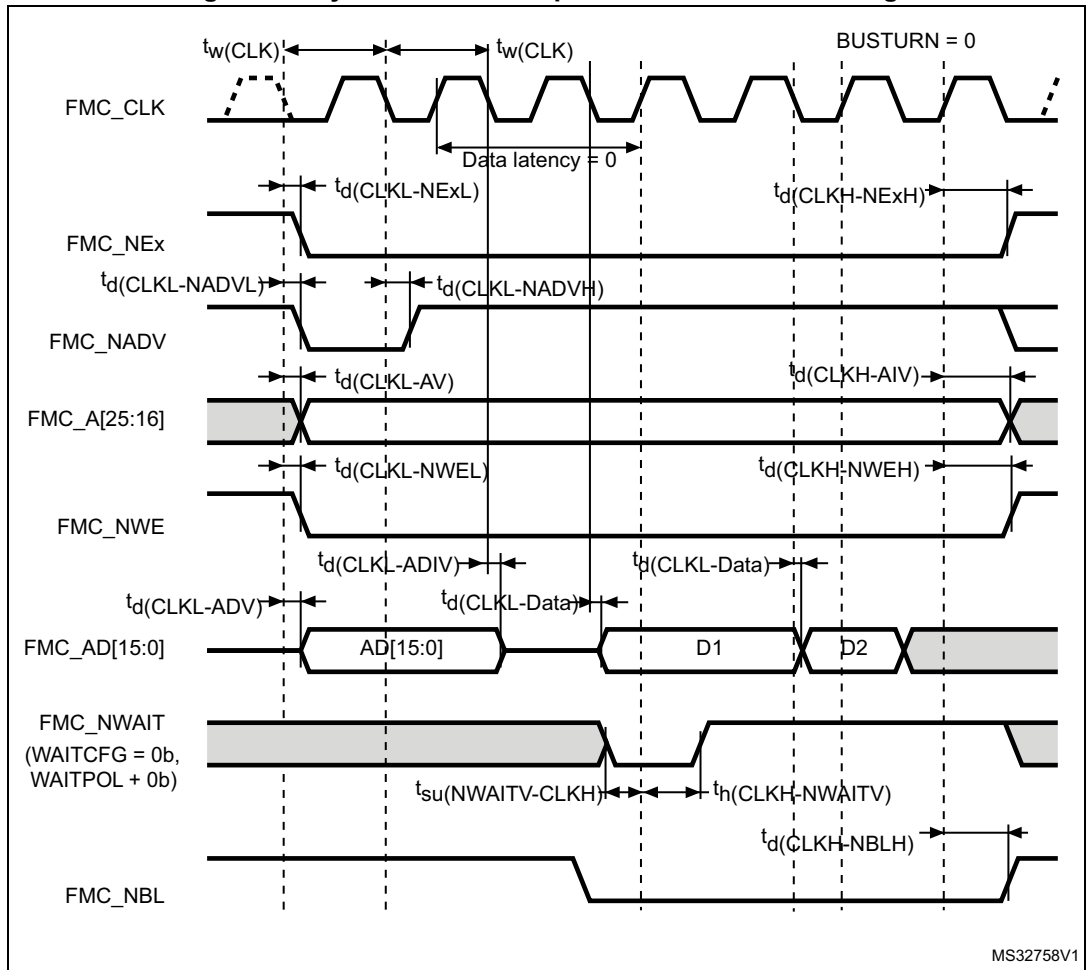


Table 79. Synchronous multiplexed PSRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, $V_{DD} = 2.7$ to 3.6 V	$2T_{fmc_ker_ck} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low ($x = 0..2$)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high ($x = 0..2$)	$T_{fmc_ker_ck} - 1$	-	
$t_{d(CLKL-NADVl)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVh)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid ($x = 16..25$)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid ($x = 16..25$)	$T_{fmc_ker_ck} - 1$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	1	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	1	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	1	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc_ker_ck}$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_h(CLKH-NWAIT)$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Evaluated by characterization - Not tested in production.

Figure 39. Synchronous non-multiplexed NOR/PSRAM read timings

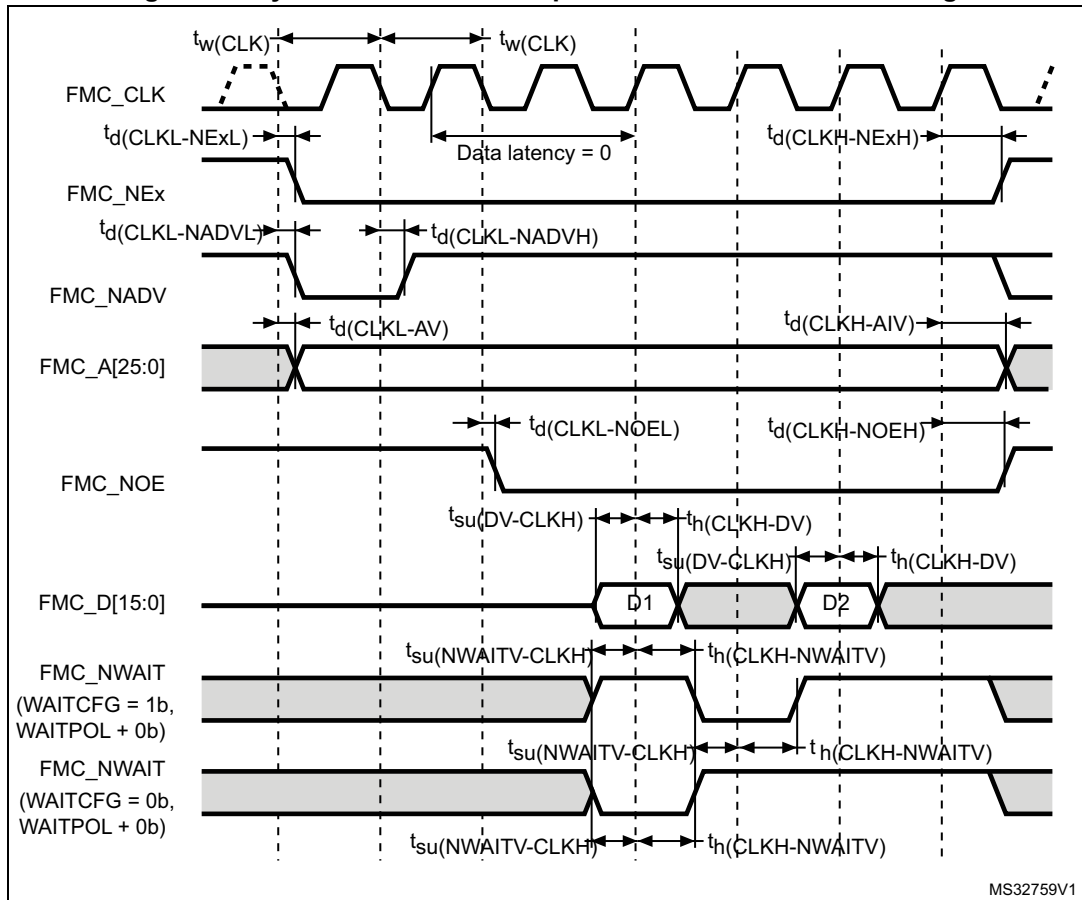
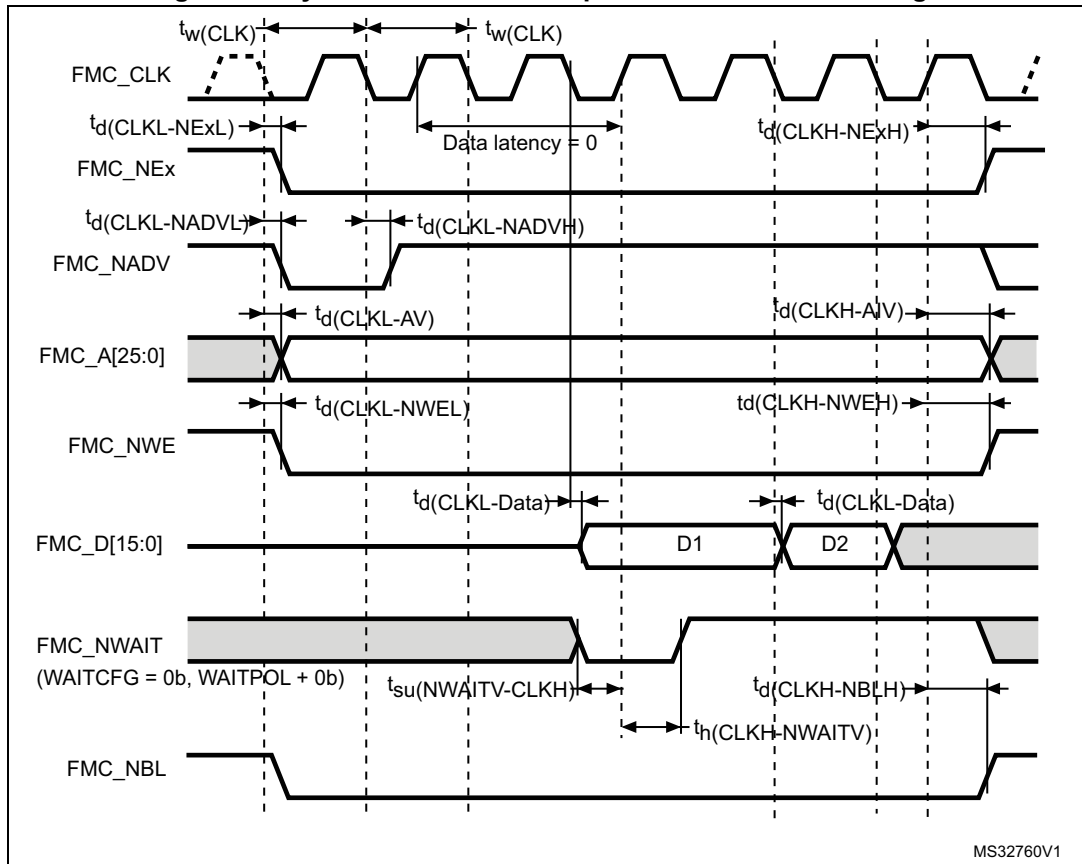


Table 80. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{CLK})$	FMC_CLK period	$2T_{\text{fmc_ker_ck}} - 0.5$	-	ns
$t_{\text{d}}(\text{CLKL-NExL})$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	1	
$t_{\text{d}}(\text{CLKH-NExH})$	FMC_CLK high to FMC_NEx high (x = 0..2)	$T_{\text{fmc_ker_ck}} - 1$	-	
$t_{\text{d}}(\text{CLKL-NADV})$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{\text{d}}(\text{CLKL-NADVH})$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{\text{d}}(\text{CLKL-AV})$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	1	
$t_{\text{d}}(\text{CLKH-AIV})$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	$T_{\text{fmc_ker_ck}} - 1$	-	
$t_{\text{d}}(\text{CLKL-NOEL})$	FMC_CLK low to FMC_NOE low	-	1	
$t_{\text{d}}(\text{CLKH-NOEH})$	FMC_CLK high to FMC_NOE high	$T_{\text{fmc_ker_ck}} + 0.5$	-	
$t_{\text{su}}(\text{DV-CLKH})$	FMC_D[15:0] valid data before FMC_CLK high	3.5	-	
$t_{\text{h}}(\text{CLKH-DV})$	FMC_D[15:0] valid data after FMC_CLK high	1.5	-	
$t_{\text{su}}(\text{NWAITV-CLKH})$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_{\text{h}}(\text{CLKH-NWAITV})$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Evaluated by characterization - Not tested in production.

Figure 40. Synchronous non-multiplexed PSRAM write timings



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Table 81. Synchronous non-multiplexed PSRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	1	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0...2)	$T_{fmc_ker_ck} - 0.5$	-	
$t_{d(CLKL-NADV)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16...25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16...25)	$T_{fmc_ker_ck} + 0.5$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	1.5	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Evaluated by characterization - Not tested in production.

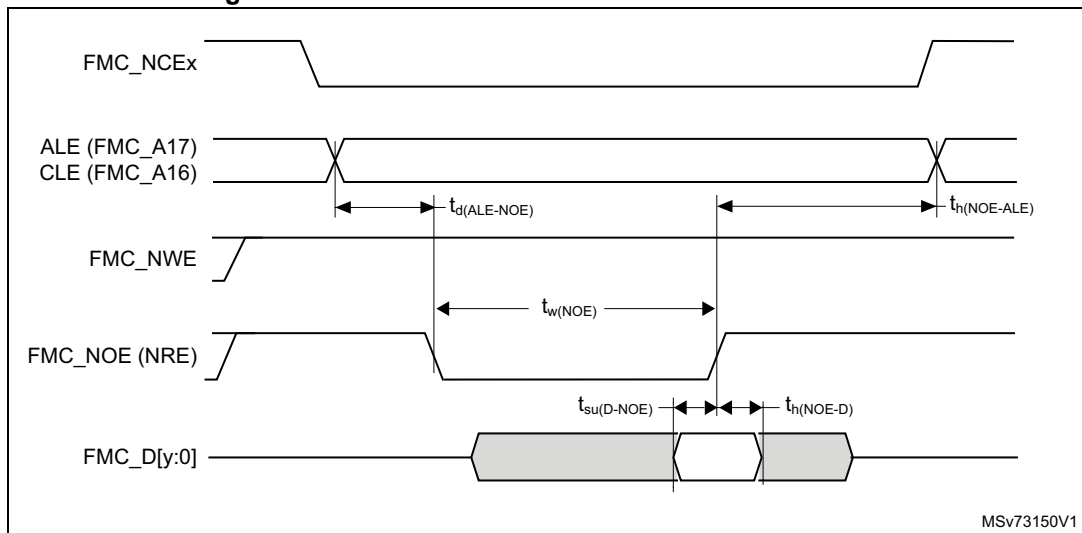
NAND controller waveforms and timings

Figures 41 through 44 represent synchronous waveforms, tables 82 and 83 provide the corresponding timings. The results are obtained with the following FMC configuration and a capacitive load (C_L) of 30 pF:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- Capacitive load $C_L = 30$ pF

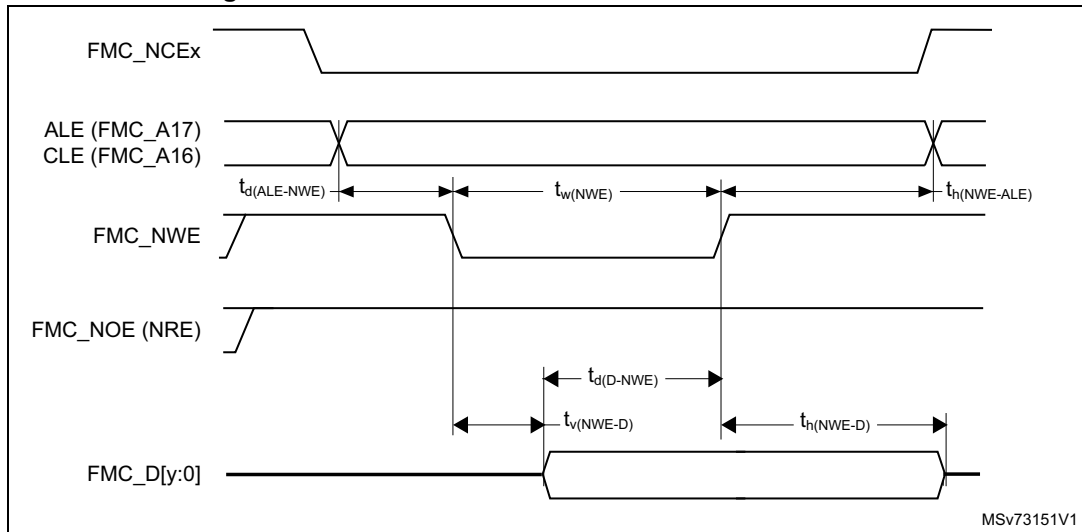
In all timing tables, $T_{fmc_ker_ck}$ is the HCLK clock period.

Figure 41. NAND controller waveforms for read access



1. $y = 7$ or 15 , depending upon the NAND flash memory interface.

Figure 42. NAND controller waveforms for write access



1. $y = 7$ or 15 , depending upon the NAND flash memory interface.

Figure 43. NAND controller waveforms for common memory read access

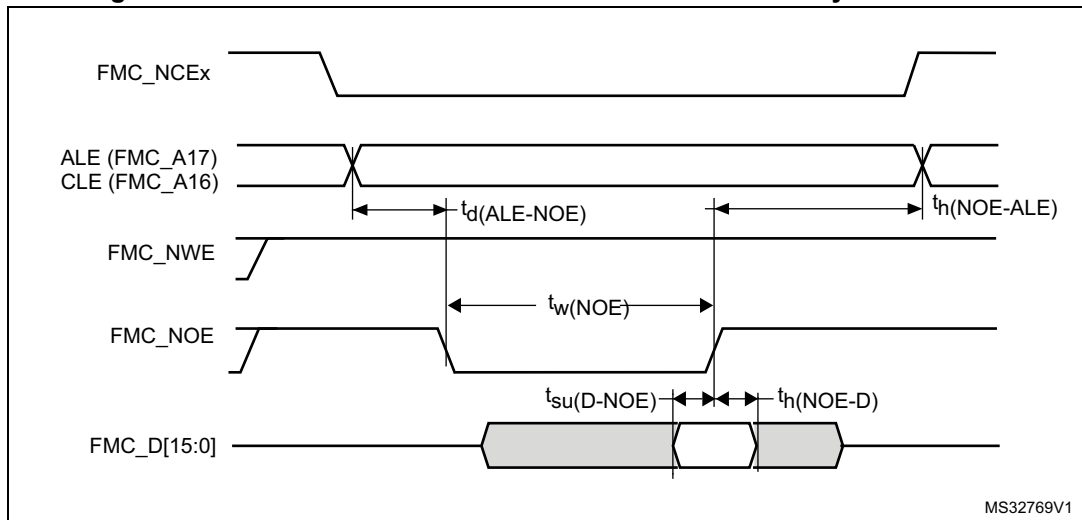


Figure 44. NAND controller waveforms for common memory write access

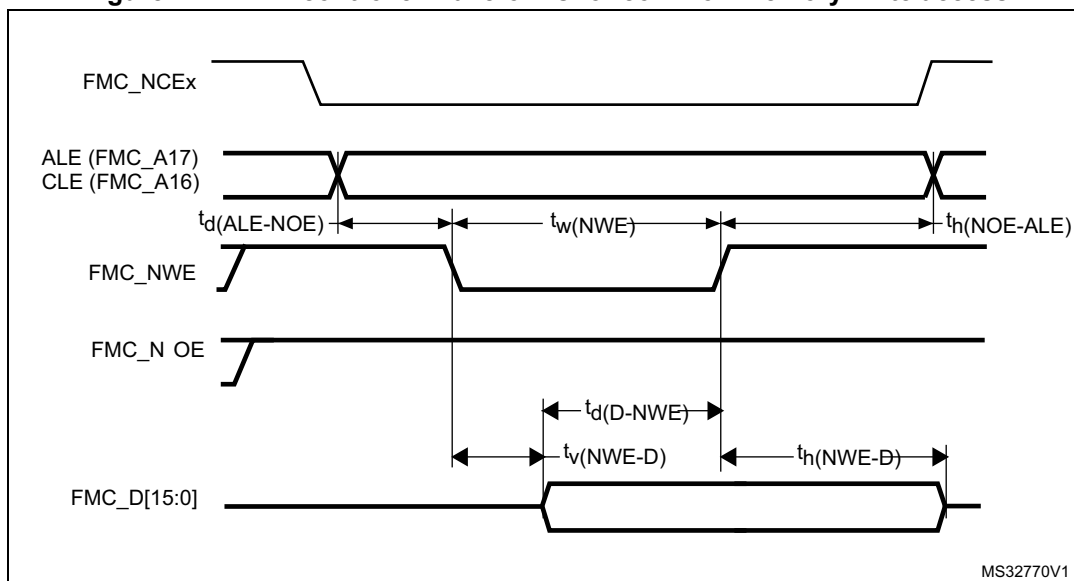


Table 82. Switching characteristics for NAND flash read cycles⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FMC_NOE low width	$4T_{fmc_ker_ck} - 0.5$	$4T_{fmc_ker_ck} + 0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	11	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc_ker_ck} + 0.5$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{fmc_ker_ck} - 1.5$	-	

1. Evaluated by characterization - Not tested in production.

Table 83. Switching characteristics for NAND flash write cycles⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc_ker_ck} - 0.5$	$4T_{fmc_ker_ck} + 0.5$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc_ker_ck} + 0.5$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc_ker_ck} - 2.5$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc_ker_ck} + 0.5$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc_ker_ck} - 1$	-	

1. Evaluated by characterization - Not tested in production.

SDRAM waveforms and timings

In all timing tables, the $t_{fmc_ker_ck}$ is the f_{HCLK} clock period, with the following FMC_SDCLK maximum values:

- For $2.7\text{ V} < V_{DD} < 3.6\text{ V}$: maximum FMC_SDCLK = 95 MHz at 20 pF (100 MHz for $V_{DD} > 3.0\text{ V}$)
- For $1.71\text{ V} < V_{DD} < 1.8\text{ V}$: maximum FMC_SDCLK = 95 MHz at 15 pF
- For $1.71\text{ V} < V_{DD} < 1.8\text{ V}$: maximum FMC_SDCLK = 90 MHz at 20 pF

Figure 45. SDRAM read access waveforms (CL = 1)

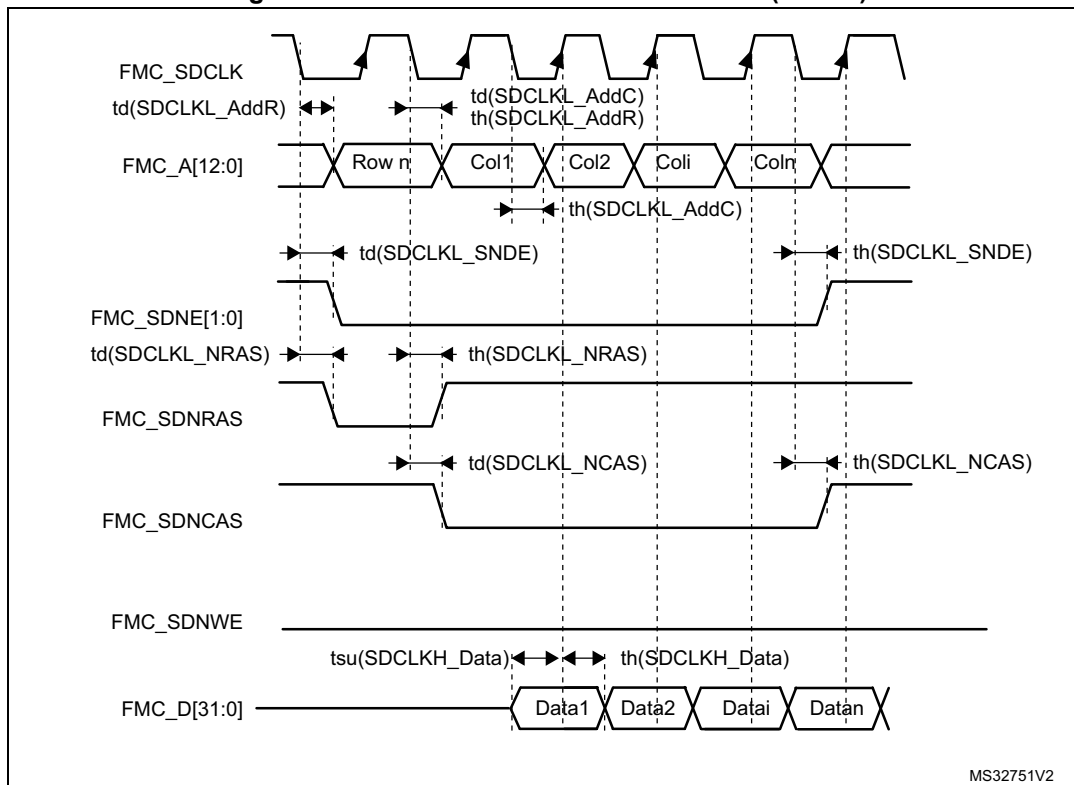


Table 84. SDRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 0.5$	$2T_{fmc_ker_ck} + 0.5$	ns
$t_{su}(\text{SDCLKH_Data})$	Data input setup time	3	-	
$t_h(\text{SDCLKH_Data})$	Data input hold time	0.5	-	
$t_d(\text{SDCLKL_Add})$	Address valid time	-	1.5	
$t_d(\text{SDCLKL_SDNE})$	Chip select valid time	-	1.5	
$t_h(\text{SDCLKL_SDNE})$	Chip select hold time	0	-	
$t_d(\text{SDCLKL_SDNRAS})$	SDNRAS valid time	-	1.5	
$t_h(\text{SDCLKL_SDNRAS})$	SDNRAS hold time	0	-	
$t_d(\text{SDCLKL_SDNCAS})$	SDNCAS valid time	-	1	
$t_h(\text{SDCLKL_SDNCAS})$	SDNCAS hold time	0	-	

1. Evaluated by characterization - Not tested in production.

Table 85. LPSDR SDRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 0.5$	$2T_{fmc_ker_ck} + 0.5$	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	3	-	
$t_h(SDCLKH_Data)$	Data input hold time	0.5	-	
$t_d(SDCLKL_Add)$	Address valid time	-	1.5	
$t_d(SDCLKL_SDNE)$	Chip select valid time	-	1.5	
$t_h(SDCLKL_SDNE)$	Chip select hold time	0	-	
$t_d(SDCLKL_SDNRAS)$	SDNRAS valid time	-	1.5	
$t_h(SDCLKL_SDNRAS)$	SDNRAS hold time	0	-	
$t_d(SDCLKL_SDNCAS)$	SDNCAS valid time	-	1	
$t_h(SDCLKL_SDNCAS)$	SDNCAS hold time	0	-	

1. Evaluated by characterization - Not tested in production.

Figure 46. SDRAM write access waveforms

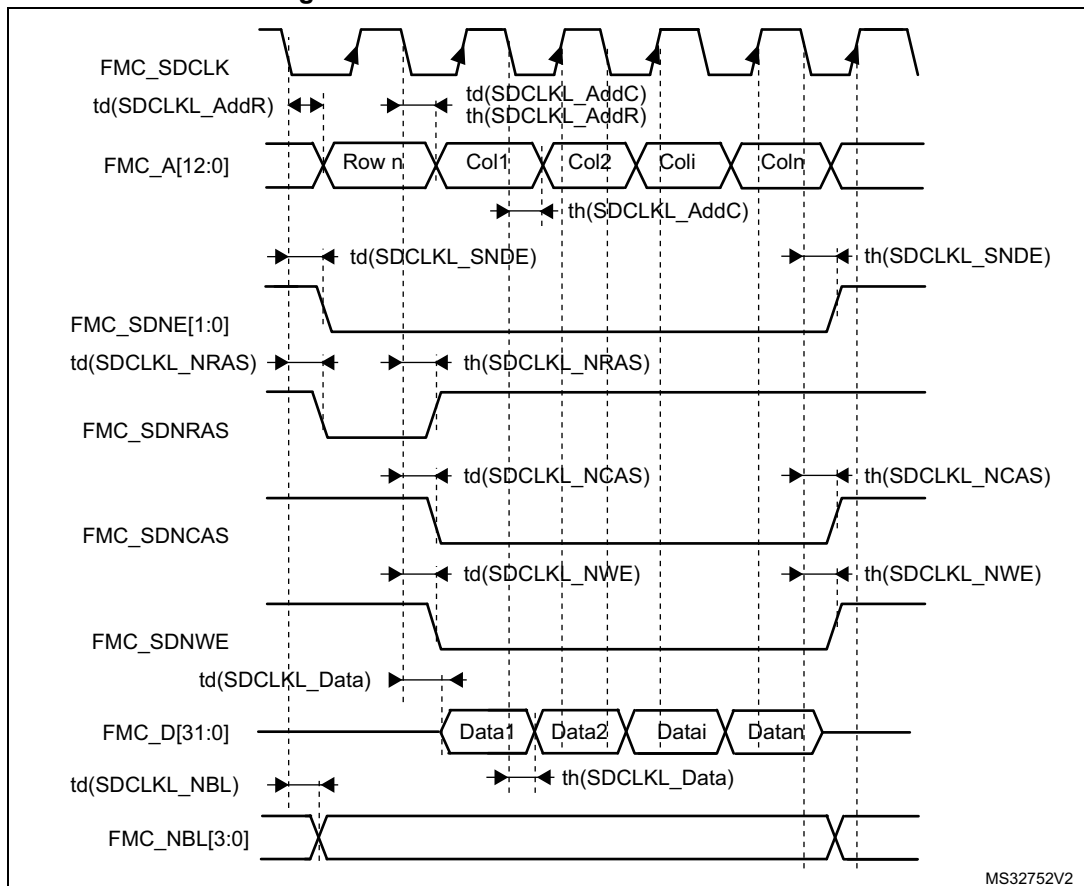


Table 86. SDRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{\text{fmc_ker_ck}} - 0.5$	$2T_{\text{fmc_ker_ck}} + 0.5$	ns
$t_d(\text{SDCLKL_Data})$	Data output valid time	-	1	
$t_h(\text{SDCLKL_Data})$	Data output hold time	0	-	
$t_d(\text{SDCLKL_Add})$	Address valid time	-	2	
$t_d(\text{SDCLKL_SDNWE})$	SDNWE valid time	-	1	
$t_h(\text{SDCLKL_SDNWE})$	SDNWE hold time	0	-	
$t_d(\text{SDCLKL_SDNE})$	Chip select valid time	-	1	
$t_h(\text{SDCLKL_SDNE})$	Chip select hold time	0	-	
$t_d(\text{SDCLKL_SDNRAS})$	SDNRAS valid time	-	1.5	
$t_h(\text{SDCLKL_SDNRAS})$	SDNRAS hold time	0	-	
$t_d(\text{SDCLKL_SDNCAS})$	SDNCAS valid time	-	1	
$t_d(\text{SDCLKL_SDNCAS})$	SDNCAS hold time	0	-	

1. Evaluated by characterization - Not tested in production.

Table 87. LPSDR SDRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{\text{fmc_ker_ck}} - 0.5$	$2T_{\text{fmc_ker_ck}} + 0.5$	ns
$t_d(\text{SDCLKL_Data})$	Data output valid time	-	1	
$t_h(\text{SDCLKL_Data})$	Data output hold time	0	-	
$t_d(\text{SDCLKL_Add})$	Address valid time	-	2	
$t_d(\text{SDCLKL-SDNWE})$	SDNWE valid time	-	1	
$t_h(\text{SDCLKL-SDNWE})$	SDNWE hold time	0	-	
$t_d(\text{SDCLKL-SDNE})$	Chip select valid time	-	1.5	
$t_h(\text{SDCLKL-SDNE})$	Chip select hold time	0	-	
$t_d(\text{SDCLKL-SDNRAS})$	SDNRAS valid time	-	1.5	
$t_h(\text{SDCLKL-SDNRAS})$	SDNRAS hold time	0	-	
$t_d(\text{SDCLKL-SDNCAS})$	SDNCAS valid time	-	1	
$t_d(\text{SDCLKL-SDNCAS})$	SDNCAS hold time	0	-	

1. Evaluated by characterization - Not tested in production.

5.3.19 Octo-SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 88](#) and [Table 89](#) are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 11$
- Measurement points are done at CMOS levels: $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7 V$
- VOS level set to VOS0

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics.

Table 88. OCTOSPI characteristics in SDR mode⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max ⁽³⁾	Unit
$F_{(CLK)}$	OCTOSPI clock frequency	$1.71 V < V_{DD} < 1.9 V$, $C_L = 15 pF$	-	-	110	MHz
		$1.7 V < V_{DD} < 3.6 V$, $C_L = 15 pF$	-	-	150	
$t_{w(CLKH)}$	OCTOSPI clock high and low time, even division	PRESCALER[7:0] = n (= 0, 1, 3, 5, ..., 255)	$t_{(CLK)}/2 - 0.5$	-	$t_{(CLK)}/2 + 0.5$	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2 - 0.5$	-	$t_{(CLK)}/2 + 0.5$	
$t_{w(CLKH)}$	OCTOSPI clock high and low time, odd division	PRESCALER[7:0] = n (= 2, 4, 6, ..., 254)	$(n/2) * t_{(CLK)} / (n + 1) - 0.5$	-	$(n/2) * t_{(CLK)} / (n + 1) + 0.5$	
$t_{w(CLKL)}$			$(n/2 + 1) * t_{(CLK)} / (n + 1) - 0.5$	-	$(n/2 + 1) * t_{(CLK)} / (n + 1) + 0.5$	
$t_{s(IN)}$	Data input setup time	-	4	-	-	
$t_{h(IN)}$	Data input hold time	-	1	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	0.5	1	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

1. All values apply to Octal and Quad-SPI mode.
2. Evaluated by characterization - Not tested in production.
3. At VOS1 these values are degraded by up to 5%.

Figure 47. OCTOSPI SDR read/write timing diagram

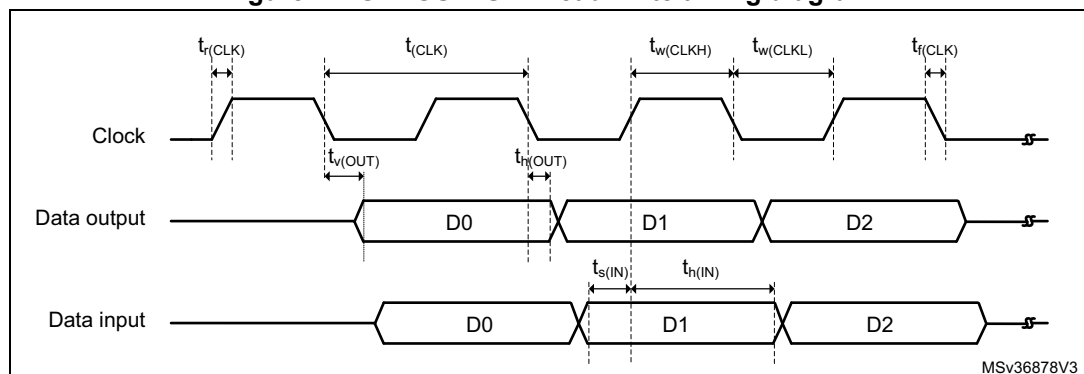


Table 89. OCTOSPI characteristics in DTR mode (no DQS)⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F _{CLK}	OCTOSPI clock frequency	1.71 V < V _{DD} < 3.6 V, C _L = 15 pF	-	-	100 ⁽⁴⁾	MHz
		1.7 V < V _{DD} < 3.6 V, C _L = 15 pF	-	-	125 ⁽⁴⁾	
t _{w(CLKH)}	OCTOSPI clock high and low time	PRESCALER[7:0] = n (= 0, 1, 3, 5, ..., 255)	t _{(CLK)/2} - 0.5	-	t _{(CLK)/2} + 0.5	ns
t _{w(CLKL)}			t _{(CLK)/2} - 0.5	-	t _{(CLK)/2} + 0.5	
t _{w(CLKH)}	OCTOSPI clock high and low time	PRESCALER[7:0] = n (= 2, 4, 6, 8, ..., 254)	(n/2) * t _{(CLK)/} (n + 1) - 0.5	-	(n/2) * t _{(CLK)/} (n + 1) + 0.5	ns
t _{w(CLKL)}			(n/2 + 1) * t _{(CLK)/} (n + 1) - 0.5	-	(n/2 + 1) * t _{(CLK)/} (n + 1) + 0.5	
t _{v(CLK)}	Clock valid time	-	-	-	t _(CLK) + 0.5	ns
t _{sr(IN),} t _{sf(IN)}	Data input setup time	-	4	-	-	ns
t _{hr(IN),} t _{hf(IN)}	Data input hold time	-	1.5	-	-	
t _{vr(OUT)} t _{vf(OUT)}	Data output valid time	DHQC = 0	-	2.5	3.5	
		DHQC = 1, Prescaler [7:0] = 1, 2...	-	t _{(CLK)/4} + 0.5	t _{(CLK)/4} + 1	
t _{hr(OUT)} t _{hf(OUT)}	Data output hold time	DHQC = 0	1.5	-	-	
		DHQC = 1, Prescaler [7:0] = 1, 2...	t _{(CLK)/4} - 1	-	-	

1. All values apply to Octal and Quad-SPI mode.
2. Evaluated by characterization - Not tested in production.
3. Delay block bypassed.
4. DHQC must be set to reach the mentioned frequency.

Table 90. OCTOSPI characteristics in DTR mode (with DQS) / hyperbus⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F _{CLK}	OCTOSPI clock frequency	1.71 V < V _{DD} < 3.6 V, C _L = 15 pF	-	-	125 ⁽³⁾⁽⁴⁾	MHz
		1.7 V < V _{DD} < 3.6 V, C _L = 15 pF	-	-	125 ⁽³⁾⁽⁵⁾	
t _w (CLKH)	OCTOSPI clock high and low time	PRESCALER[7:0] = n = (0, 1, 3, 5, ..., 255)	t _{(CLK)/2} - 0.5	-	t _{(CLK)/2} + 0.5	ns
t _w (CLKL)			t _{(CLK)/2} - 0.5	-	t _{(CLK)/2} + 0.5	
t _w (CLKH)	OCTOSPI clock high and low time	PRESCALER[7:0] = n = (2, 4, 6, 8, ..., 254)	(n/2)*t _{(CLK)/} (n+1) - 0.5	-	(n/2)*t _{(CLK)/} (n+1) + 0.5	ns
t _w (CLKL)			(n/2+1)*t _{(CLK)/} (n+1) - 0.5	-	(n/2+1)*t _{(CLK)/} (n+1) + 0.5	
t _v (CLK)	Clock valid time	-	-	-	t _(CLK) + 2	
t _h (CLK)	Clock hold time	-	t _{(CLK)/2} - 1	-	-	
t _{ODr} (₍₅₎ CLK)	CLK, NCLK crossing level on CLK rising edge	V _{DD} = 1.8 V	890	-	1300	mV
t _{ODf} (₍₅₎ CLK)	CLK, NCLK crossing level on CLK falling edge	V _{DD} = 1.8 V	790	-	1080	mV
t _w (CS)	Chip select high time	-	3 * t _(CLK)	-	-	ns
t _v (DQ)	Data input valid time	-	3	-	-	
t _v (DS)	Data strobe input valid time	-	1	-	-	
t _h (DS)	Data strobe input hold time	-	0	-	-	
t _v (RWDS)	Data strobe output valid time	-	-	-	3 * t _(CLK)	
t _{sr} (DQ), t _{sf} (DQ)	Data input setup time	-	-0.5	-	-	ns
t _{hr} (DQ), t _{hf} (DQ)	Data input hold time	-	2	-	-	
t _{vr} (OUT) t _{vf} (OUT)	Data output valid time	DHQC = 0	-	2.5	3.5	
		DHQC = 1, all prescaler values (except 0)	-	t _{(CLK)/4} + 0.5	t _{(CLK)/4} + 1	
t _{hr} (OUT) t _{hf} (OUT)	Data output hold time	DHQC = 0	1.5	-	-	
		DHQC = 1, all prescaler values (except 0)	t _{(CLK)/4} - 1	-	-	

1. Evaluated by characterization - Not tested in production.
2. Delay block activated.
3. Maximum frequency value are given for a maximum RWDS to DQ skew of ± 1.0 ns.
4. DHQC must be set to reach the mentioned frequency.
5. PF10/PB5, PB4/PB5 and PA3/PB5 are recommended to be in line with crossing specification.

Figure 48. OCTOSPI timing diagram - DTR mode

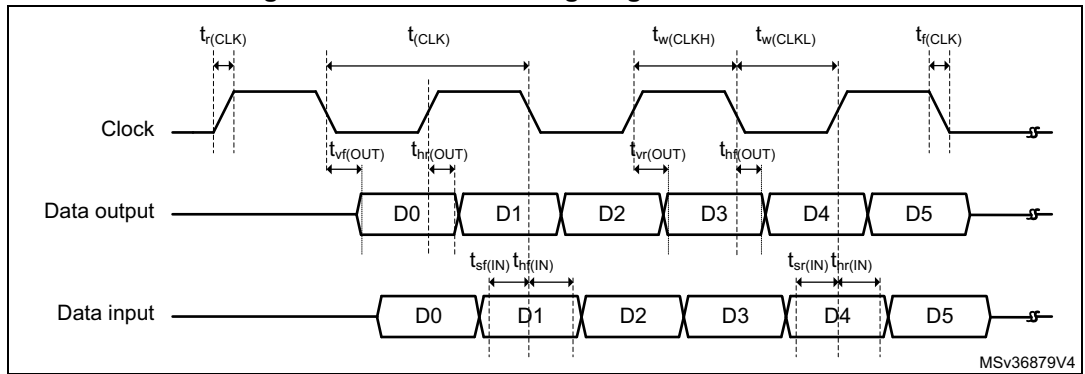


Figure 49. OCTOSPI hyperbus clock

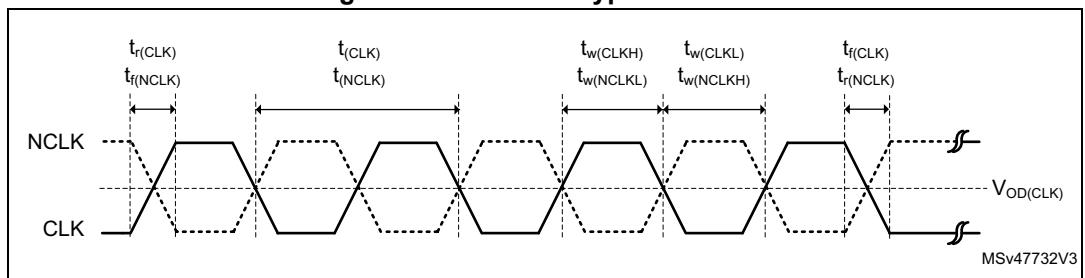


Figure 50. OCTOSPI hyperbus read

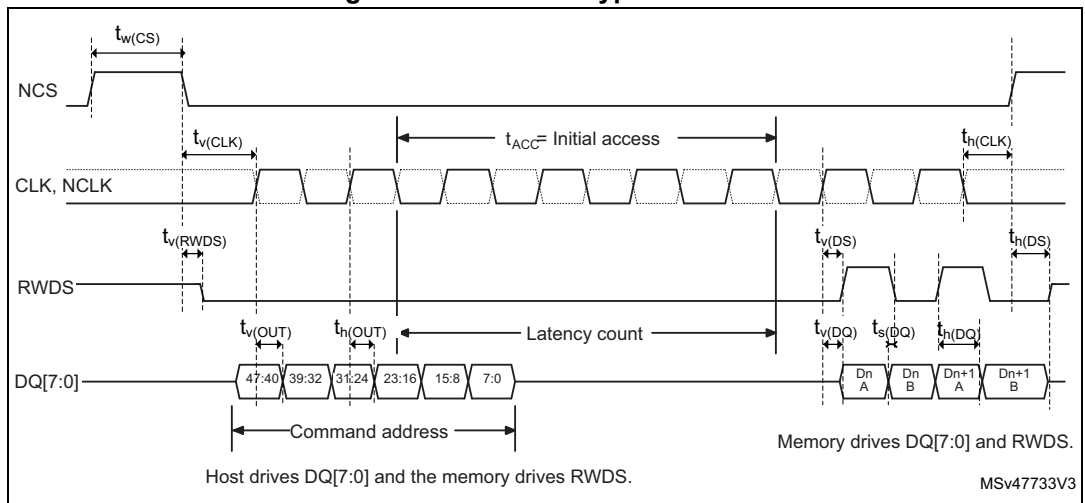
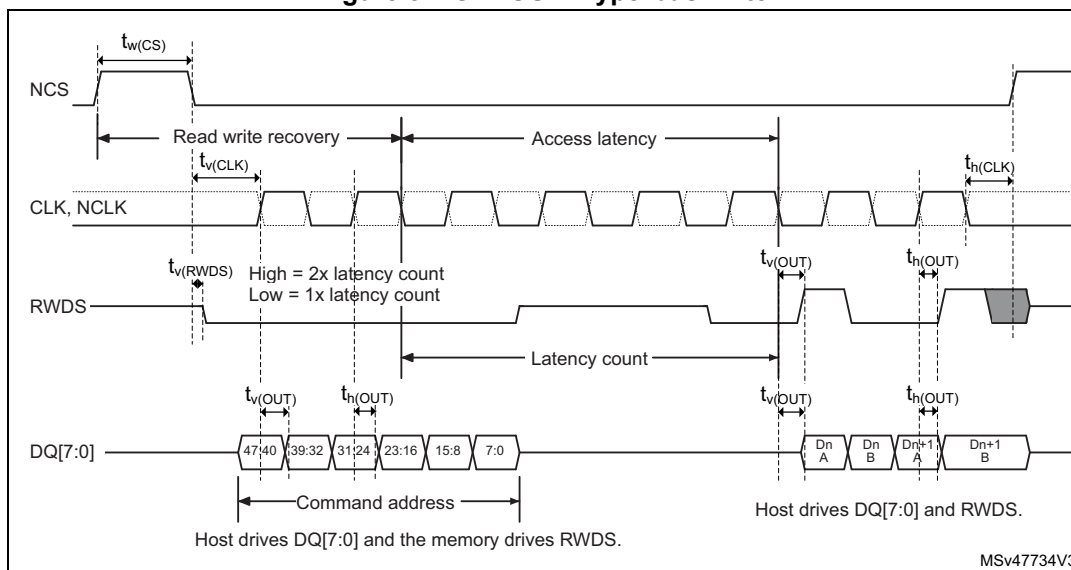


Figure 51. OCTOSPI hyperbus write



5.3.20 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in [Table 91](#) are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 20](#), with the following configuration:

Table 91. Delay block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	750	1100	1700	ps
t_{Δ}	Unit delay	-	38	44	54	ps

5.3.21 DCMI interface characteristics

Unless otherwise specified, the parameters given in [Table 92](#) are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 20](#), with the following configuration:

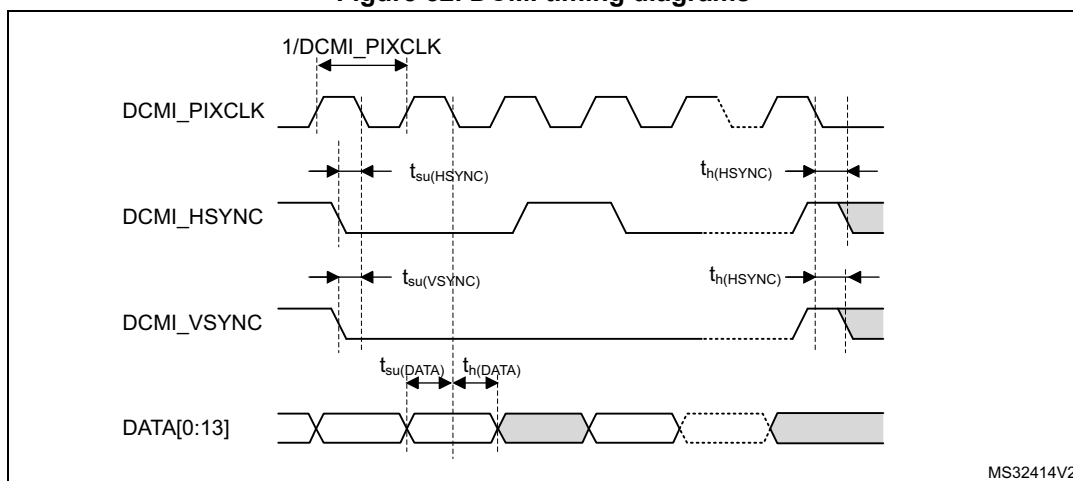
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load $C_L = 30$ pF
- Measurement points done at CMOS levels: $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Voltage scaling VOS0 selected

Table 92. DCMI characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/fHCLK	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	100	MHz
D _{PIXEL}	Pixel clock input duty cycle	30	70	%
t _{su} (DATA)	Data input setup time	2.5	-	ns
t _h (DATA)	Data hold time	2	-	
t _{su} (HSYNC), t _{su} (VSYNC)	DCMI_HSYNC and DCMI_VSYNC input setup times	2.5	-	
t _h (HSYNC), t _h (VSYNC)	DCMI_HSYNC and DCMI_VSYNC input hold times	1.5	-	

1. Evaluated by characterization - Not tested in production.

Figure 52. DCMI timing diagrams



MS32414V2

5.3.22 PSSI interface characteristics

Unless otherwise specified, the parameters given in [Table 92](#) and [Table 93](#) are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 20](#) and [Section 5.3.1](#), with the following configuration:

- PSSI_PDCK polarity: falling
- PSSI_RDY and PSSI_DE polarity: low
- Bus width: 16 lines
- DATA width: 32 bits
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V
- Voltage scaling VOS0 selected

Table 93. PSSI transmit characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
-	Frequency ratio PSSI_PDCK/f _{HCLK}	-	-	0.4	-
PSSI_PDCK	PSSI clock input	2.7 V ≤ V _{DD} ≤ 3.6 V	-	90 ⁽²⁾	MHz
		1.71 V ≤ V _{DD} ≤ 3.6 V	-	86	
D _{pixel}	PSSI clock input duty cycle		30	70	%
t _{ov} (DATA)	Data output valid time	2.7 V ≤ V _{DD} ≤ 3.6 V	-	11	ns
		1.71 V ≤ V _{DD} ≤ 3.6 V	-	11.5	
t _{oh} (DATA)	Data output hold time	1.71 V ≤ V _{DD} ≤ 3.6 V	5.5	-	
t _{ov} (DE)	DE output valid time		-	11.5	
t _{oh} (DE)	DE output hold time		5.5	-	
tsu(RDY)	RDY input setup time		0.5	-	
th(RDY)	RDY input hold time		0.5	-	

1. Evaluated by characterization - Not tested in production.
2. This maximal frequency does not consider receiver setup and hold timings.

Table 94. PSSI receive characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
-	Frequency ratio PSSI_PDCK/f _{HCLK}		-	0.4	-
PSSI_PDCK	PSSI clock input	1.71 V ≤ V _{DD} ≤ 3.6 V	-	100	MHz
D _{pixel}	PSSI clock input duty cycle	-	30	70	%
t _{su} (DATA)	Data input setup time	1.71 V ≤ V _{DD} ≤ 3.6 V	2	-	ns
t _h (DATA)	Data input hold time		2.5	-	
t _{su} (DE)	DE input setup time		1.5	-	
t _h (DE)	DE input hold time		2	-	
t _{ov} (RDY)	RDY output valid time		-	16.5	
t _{oh} (RDY)	RDY output hold time		5.5	-	

1. Evaluated by characterization - Not tested in production.

Figure 53. PSSI transmit timing diagram

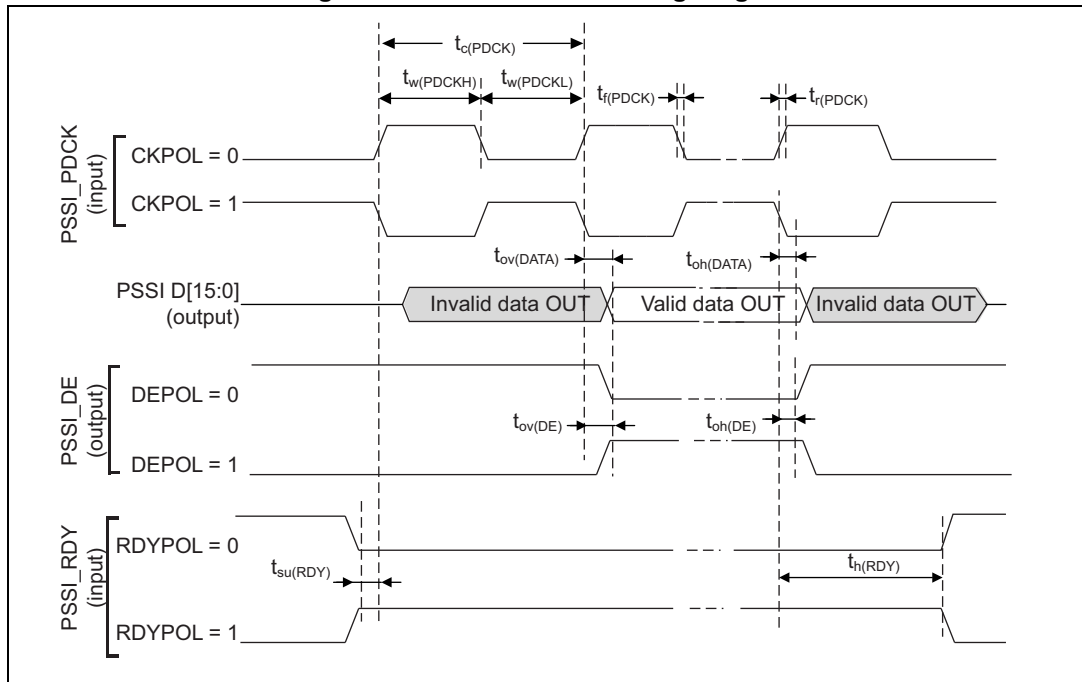
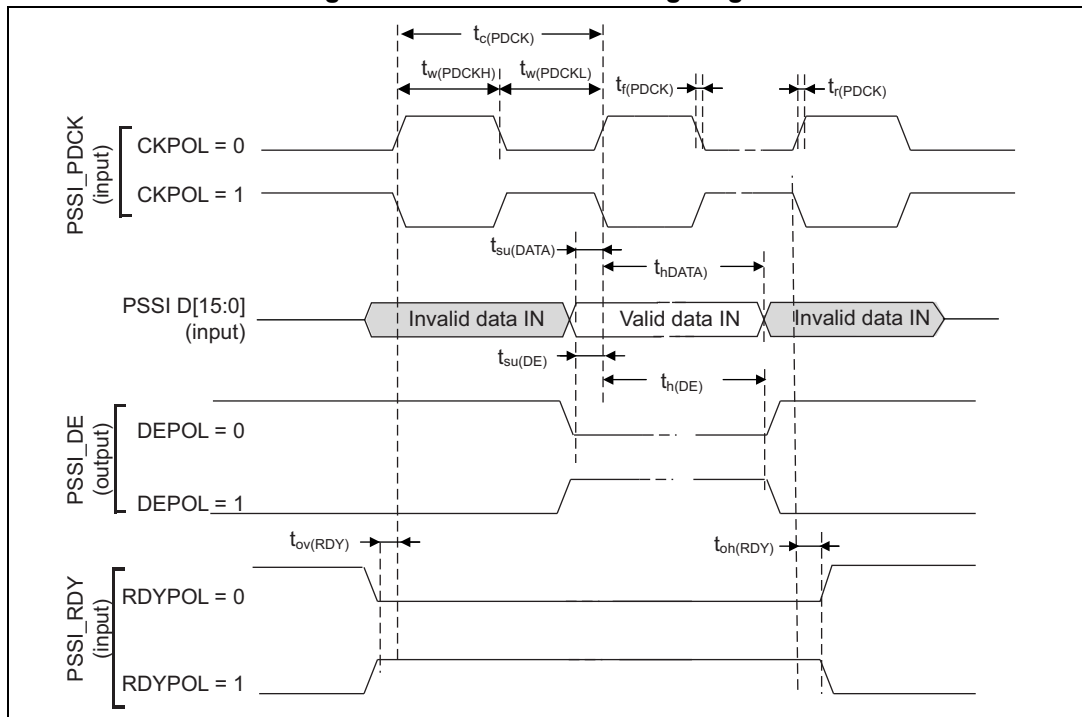


Figure 54. PSSI receive timing diagram



5.3.23 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 95](#) are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DDA} supply voltage conditions summarized in [Table 20](#).

Table 95. 12-bit ADC characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions				Min	Typ	Max	Unit		
V_{DDA}	Analog supply voltage for ADC ON	-				1.62	-	3.6	V		
V_{REF+}	Positive reference voltage	-				1.62	-	V_{DDA}	V		
V_{REF-}	Negative reference voltage	-				V_{SSA}					
f_{ADC}	ADC clock frequency	$1.62\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$				1.5	-	75	MHz		
$f_S^{(3)}$ with $R_{AIN} = 47\ \Omega$ and $C_{PCB} = 22\ \text{pF}$	Sampling rate for fast channels (VIN[0:5])	Resolution = 12 bits	Continuous mode	$1.8\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$	$-40^\circ\text{C} \leq T_J \leq 130^\circ\text{C}$	$f_{ADC} = 75\text{ MHz}$	SMP = 2.5	-	5.00	-	MSPS
				$1.6\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$		$f_{ADC} = 70\text{ MHz}$		-	4.66		
			Single or Discontinuous mode	$2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$		$f_{ADC} = 60\text{ MHz}$		-	4.00		
				$1.6\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$		$f_{ADC} = 50\text{ MHz}$		-	3.33		
		Resolution = 10 bits	Continuous mode	$1.6\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$		$f_{ADC} = 75\text{ MHz}$		-	5.77	-	
				Single or Discontinuous mode		$2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$		$f_{ADC} = 75\text{ MHz}$	-	5.77	
	$1.6\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$	$f_{ADC} = 65\text{ MHz}$	-		5.00						
	Resolution = 8 bits	All modes	$1.6\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$	$f_{ADC} = 75\text{ MHz}$	-	6.82	-				
			$1.6\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$	$f_{ADC} = 75\text{ MHz}$	-	8.33					
	Resolution = 6 bits	All modes	$1.6\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$	$-40^\circ\text{C} \leq T_J \leq 130^\circ\text{C}$	$f_{ADC} = 35\text{ MHz}$	SMP = 2.5	-	2.30	-		
					$f_{ADC} = 35\text{ MHz}$		-	2.70			
					$f_{ADC} = 50\text{ MHz}$		-	4.50			
$f_{ADC} = 50\text{ MHz}$					-		5.50				
t_{TRIG}	External trigger period	Resolution = 12 bits				-	-	15	$1/f_{ADC}$		

Table 95. 12-bit ADC characteristics⁽¹⁾⁽²⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{AIN}^{(2)}$	Conversion voltage range	-	0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-	$V_{REF/2-10\%}$	$V_{REF/2}$	$V_{REF/2+10\%}$	
$R_{AIN}^{(5)}$	External input impedance	Resolution = 12 bits, $T_J = 130^\circ\text{C}$ (tolerance 4 LSBs)	-	-	321	Ω
		Resolution = 12 bits, $T_J = 125^\circ\text{C}$	-	-	220	
		Resolution = 10 bits, $T_J = 130^\circ\text{C}$	-	-	1039	
		Resolution = 10 bits, $T_J = 125^\circ\text{C}$	-	-	2100	
		Resolution = 8 bits, $T_J = 130^\circ\text{C}$	-	-	6327	
		Resolution = 8 bits, $T_J = 125^\circ\text{C}$	-	-	12000	
		Resolution = 6 bits, $T_J = 130^\circ\text{C}$	-	-	47620	
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
$t_{ADCVREG_STUP}$	ADC LDO startup time	-	-	5	10	μs
t_{STAB}	ADC power-up time	LDO already started	1	-	-	conversion cycle
t_{OFF_CAL}	Offset calibration time	-	1335			
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.5	
		CKMODE = 10	-	-	2.5	
		CKMODE = 11	-	-	2.25	
t_{LATRIJ}	Trigger conversion latency for regular and injected channels when a regular conversion is aborted	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.5	
		CKMODE = 10	-	-	3.5	
		CKMODE = 11	-	-	3.25	
t_S	Sampling time	-	2.5	-	640.5	
t_{CONV}	Total conversion time (including sampling time)	N-bits resolution	$t_S + 0.5 + N$			

Table 95. 12-bit ADC characteristics⁽¹⁾⁽²⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DDA_D(ADC)}	ADC consumption on V _{DDA} and V _{REF-} . Differential mode	fs = 5 MSPS	-	600	-	µA
		fs = 1 MSPS	-	190	-	
		fs = 0.1 MSPS	-	50	-	
I _{DDA_SE(ADC)}	ADC consumption on V _{DDA} and V _{REF-} . Single-ended mode	fs = 5 MSPS	-	500	-	
		fs = 1 MSPS	-	150	-	
		fs = 0.1 MSPS	-	50	-	
I _{DD(ADC)}	ADC consumption on V _{DD}	f _{ADC} = 75 MHz	-	265	-	
		f _{ADC} = 50 MHz	-	175	-	
		f _{ADC} = 25 MHz	-	90	-	
		f _{ADC} = 12.5 MHz	-	45	-	
		f _{ADC} = 6.25 MHz	-	22	-	
		f _{ADC} = 3.125 MHz	-	11	-	

1. Specified by design - Not tested in production.
2. The voltage booster on ADC switches must be used for V_{DDA} < 2.7 V (embedded I/O switches).
3. These values are valid on BGA packages.
4. Depending on the package, V_{REF+} can be internally connected to V_{DDA} and V_{REF-} to V_{SSA}.
5. The tolerance is two LSBs for 12-bit, 10-bit and 8-bit resolutions, otherwise specified.

Table 96. Minimum sampling time versus R_{AIN}⁽¹⁾⁽²⁾

Resolution	R _{AIN} (Ω)	Minimum sampling time (s)	
		Fast channel	Slow channel ⁽³⁾
12 bits	47	3.75E-08	6.12E-08
	68	3.94E-08	6.25E-08
	100	4.36E-08	6.51E-08
	150	5.11E-08	7.00E-08
	220	6.54E-08	7.86E-08
	330	8.80E-08	9.57E-08
	470	1.17E-07	1.23E-07
	680	1.60E-07	1.65E-07

Table 96. Minimum sampling time versus $R_{AIN}^{(1)(2)}$ (continued)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channel	Slow channel ⁽³⁾
10 bits	47	3.19E-08	5.17E-08
	68	3.35E-08	5.28E-08
	100	3.66E-08	5.45E-08
	150	4.35E-08	5.83E-08
	220	5.43E-08	6.50E-08
	330	7.18E-08	7.89E-08
	470	9.46E-08	1.00E-07
	680	1.28E-07	1.33E-07
	1000	1.81E-07	1.83E-07
	1500	2.63E-07	2.63E-07
	2200	3.79E-07	3.76E-07
8 bits	3300	5.57E-07	5.52E-07
	47	2.64E-08	4.17E-08
	68	2.76E-08	4.24E-08
	100	3.02E-08	4.39E-08
	150	3.51E-08	4.66E-08
	220	4.27E-08	5.13E-08
	330	5.52E-08	6.19E-08
	470	7.17E-08	7.72E-08
	680	9.68E-08	1.00E-07
	1000	1.34E-07	1.37E-07
	1500	1.93E-07	1.94E-07
	2200	2.76E-07	2.74E-07
	3300	4.06E-07	4.01E-07
	4700	5.73E-07	5.62E-07
	6800	8.21E-07	7.99E-07
10000	1.20E-06	1.17E-06	
15000	1.79E-06	1.74E-06	

Table 96. Minimum sampling time versus $R_{AIN}^{(1)(2)}$ (continued)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channel	Slow channel ⁽³⁾
6 bits	47	2.14E-08	3.16E-08
	68	2.23E-08	3.21E-08
	100	2.40E-08	3.31E-08
	150	2.68E-08	3.52E-08
	220	3.13E-08	3.87E-08
	330	3.89E-08	4.51E-08
	470	4.88E-08	5.39E-08
	680	6.38E-08	6.79E-08
	1000	8.70E-08	8.97E-08
	1500	1.23E-07	1.24E-07
	2200	1.73E-07	1.73E-07
	3300	2.53E-07	2.49E-07
	4700	3.53E-07	3.45E-07
	6800	5.04E-07	4.90E-07
	10000	7.34E-07	7.11E-07
15000	1.09E-06	1.05E-06	

1. Specified by design - Not tested in production.
2. Data valid up to 130 °C, with a 22 pF PCB capacitor, and $V_{DDA} = 1.6$ V.
3. Slow channels correspond to all ADC inputs except for the fast channels.

Figure 55. ADC conversion timing diagram

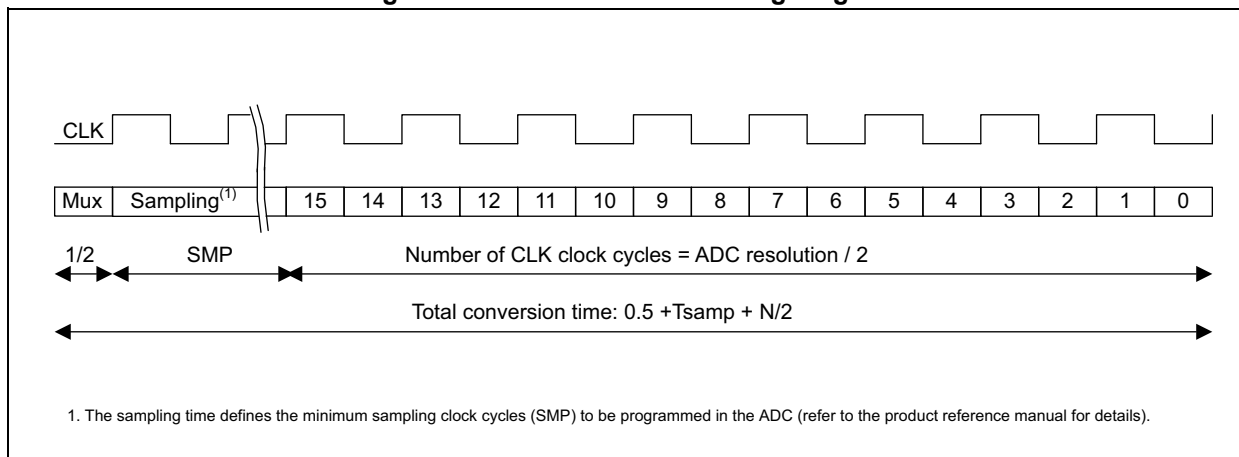


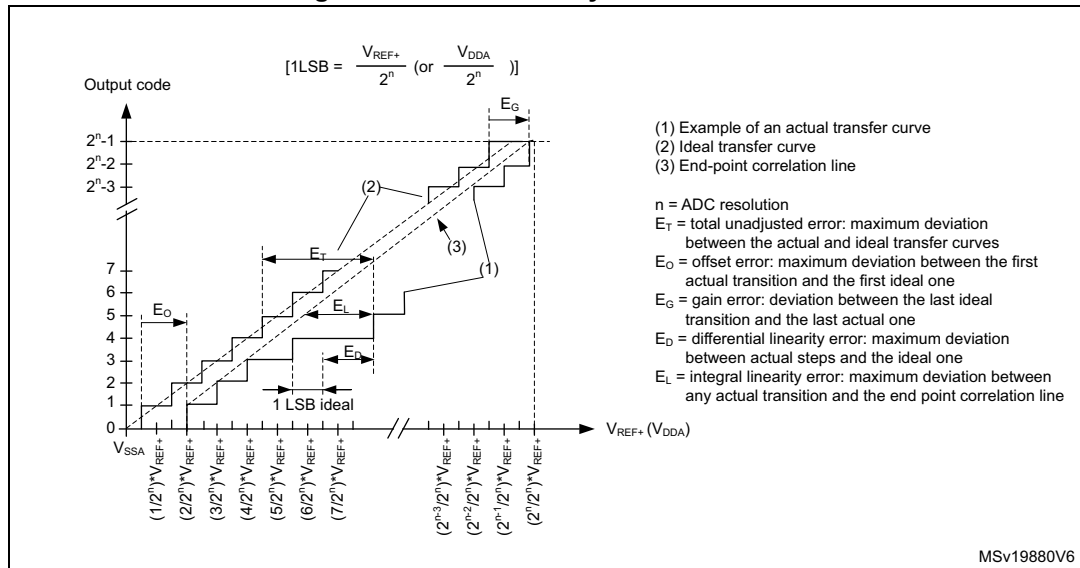
Table 97. ADC accuracy⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit	
ET	Total unadjusted error	Fast and slow channels	Single ended	-	±3.5	±12	LSB	
			Differential	-	±2.5	±7.5		
EO	Offset error	-	Single ended	-	±3	±5.5		
		-	Differential	-	±2	±3.5		
EG	Gain error	-	Single ended	-	±3.5	±11		
		-	Differential	-	±2.5	±7		
ED	Differential linearity error	-	Single ended	-	±0.75	+2/-1		
		-	Differential	-	±0.75	+2/-1		
EL	Integral linearity error	Fast and slow channels	Single ended	-	±2	±6.5		
			Differential	-	±1	±4		
ENOB	Effective number of bits	Single ended		-	10.8	-		Bits
		Differential		-	11.5	-		
SINAD	Signal-to-noise and distortion ratio	Single ended		-	68	-	dB	
		Differential		-	71	-		
SNR	Signal-to-noise ratio	Single ended		-	70	-		
		Differential		-	72	-		
THD	Total harmonic distortion	Single ended		-	-70	-		
		Differential		-	-80	-		

1. Evaluated by characterization for BGA packages. The values for LQFP package can differ. Not tested in production.
2. ADC DC accuracy values are measured after internal calibration in continuous mode.

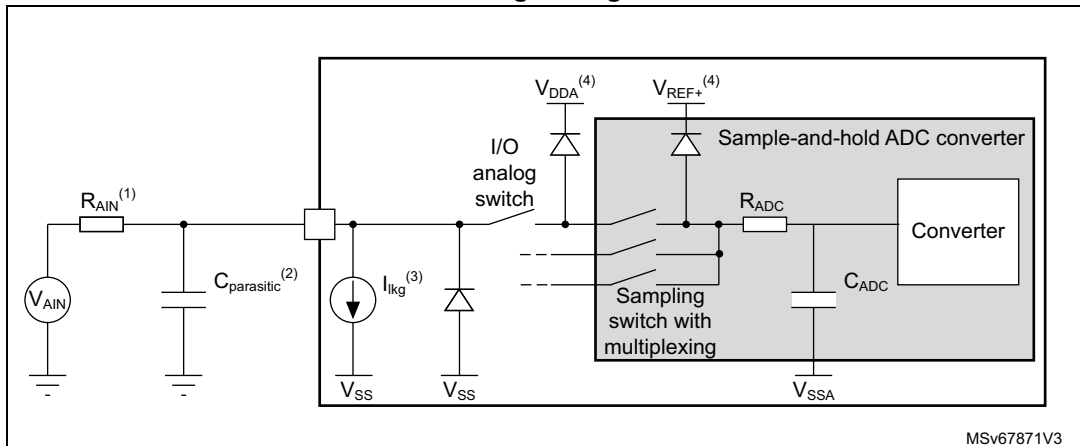
Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins, which may potentially inject negative currents.

Figure 56. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
5. E_O = Offset error: deviation between the first actual transition and the first ideal one.
6. E_G = Gain error: deviation between the last ideal transition and the last actual one.
7. E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
8. E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 57. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function

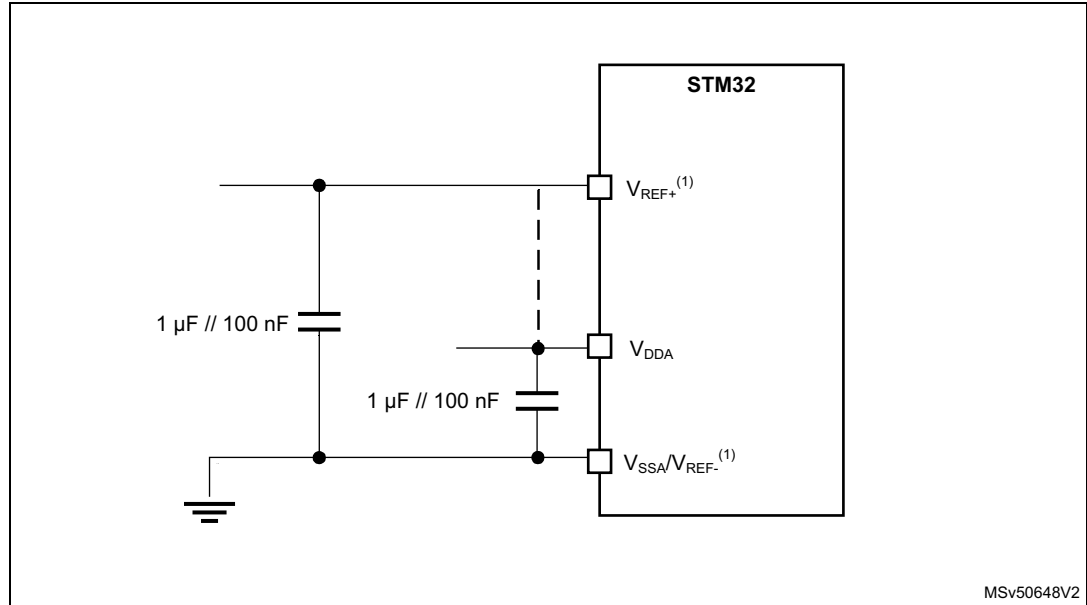


1. Refer to [Table 95](#) for the values of R_{AIN} , and C_{ADC} .
2. $C_{\text{parasitic}}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to [Table 58](#)). A high $C_{\text{parasitic}}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to [Table 58](#) for the value of I_{lkg} .
4. Refer to [Figure 20](#).

General PCB design guidelines

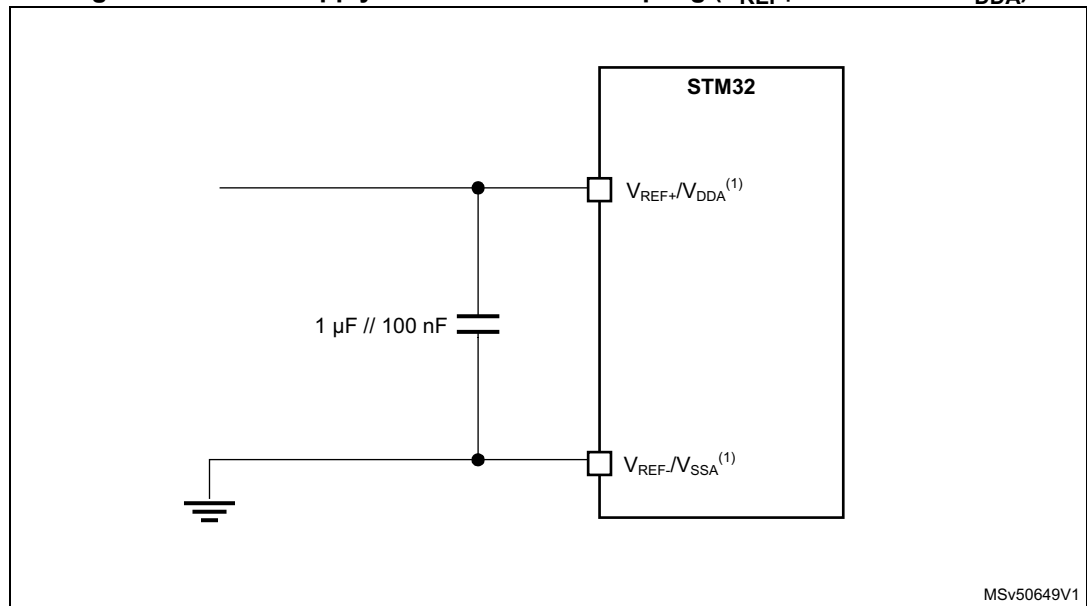
It is recommended to perform power supply decoupling as shown in [Figure 58](#) or [Figure 59](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors must be ceramic (good quality), and placed as close as possible to the chip.

Figure 58. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is not available on all packages (refer to [Table 14](#)), V_{REF-} is available only on UFBGA176+25, UFBGA169 with SMPS, LQFP100, UFBGA169, and UFBGA176+25 packages. When V_{REF+} is not available, it is internally connected to V_{SSA} .

Figure 59. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is not available on all packages (refer to [Table 14](#)), V_{REF-} is available only on UFBGA176+25, UFBGA169 with SMPS, LQFP100, UFBGA169, and UFBGA176+25 packages. When V_{REF-} is not available, it is internally connected to V_{SSA} . If V_{REF-} is available and connected to V_{DDA} , refer to [Figure 20](#) for more details.

5.3.24 DAC characteristics

Table 98. DAC characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{DDA}	Analog supply voltage	-	1.8	3.3	3.6	V	
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}		
V_{REF-}	Negative reference voltage	-	-	V_{SSA}	-		
R_L	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	k Ω
			Connected to V_{DDA}	25	-	-	
R_O	Output impedance	DAC output buffer OFF	10.3	13	16		
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	$V_{DD} = 2.7$ V	-	-	1.6	k Ω
			$V_{DD} = 2.0$ V	-	-	2.6	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	$V_{DD} = 2.7$ V	-	-	17.8	k Ω
			$V_{DD} = 2.0$ V	-	-	18.7	
C_L	Capacitive load	DAC output buffer OFF	-	-	50	pF	
C_{SH}		Sample and Hold mode	-	0.1	1	μ F	
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON	0.2	-	$V_{DDA} - 0.2$	V	
		DAC output buffer OFF	0	-	V_{REF+}		
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ± 0.5 LSB, ± 1 LSB, ± 2 LSB, ± 4 LSB, ± 8 LSB)	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ k Ω	± 0.5 LSB	-	2.05	3	μ s
			± 1 LSB	-	1.97	2.87	
			± 2 LSB	-	1.67	2.84	
			± 4 LSB	-	1.66	2.78	
			± 8 LSB	-	1.65	2.7	
		Normal mode, DAC output buffer OFF, ± 1 LSB $C_L = 10$ pF	-	1.7	2		
$t_{WAKEUP}^{(2)}$	Wake-up time from off state (setting the ENx bit in the DAC control register) until the final value of ± 1 LSB is reached	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L = 5$ k Ω	-	5	7.5	μ s	
		Normal mode, DAC output buffer OFF, $C_L \leq 10$ pF	-	2	5		
PSRR	DC V_{DDA} supply rejection ratio	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L = 5$ k Ω	-	-80	-28	dB	

Table 98. DAC characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
t _{SAMP}	Sampling time in Sample and Hold mode C _L = 100 nF (code transition between the lowest and the highest input code when DAC_OUT reaches the ±1LSB final value)	MODE<2:0>_V12 = 100/101 (BUFFER ON)	-	0.7	2.6	ms	
		MODE<2:0>_V12 = 110 (BUFFER OFF)	-	11.5	18.7		
		MODE<2:0>_V12=111 ⁽³⁾ (INTERNAL BUFFER OFF)	-	0.3	0.6	µs	
I _{leak}	Output leakage current	-	-	-	⁽⁴⁾	nA	
C _{lint}	Internal sample and hold capacitor	-	1.8	2.2	2.6	pF	
t _{TRIM}	Middle code offset trim time	Minimum time to verify each code	50	-	-	µs	
V _{offset}	Middle code offset for 1 trim code step	V _{REF+} = 3.6 V	-	850	-	µV	
		V _{REF+} = 1.8 V	-	425	-		
I _{DDA(DAC)}	DAC quiescent consumption from V _{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	360	-	µA
			No load, worst code (0xF1C)	-	490	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	20	-	
		Sample and Hold mode, C _{SH} = 100 nF	-	360*T _{ON} / (T _{ON} +T _{OFF}) ⁽⁵⁾	-		
I _{DDV(DAC)}	DAC consumption from V _{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	170	-	µA
			No load, worst code (0xF1C)	-	170	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	160	-	
		Sample and Hold mode, buffer ON, C _{SH} = 100 nF (worst code)	-	170*T _{ON} / (T _{ON} +T _{OFF}) ⁽⁵⁾	-		
		Sample and Hold mode, buffer OFF, C _{SH} = 100 nF (worst code)	-	160*T _{ON} / (T _{ON} +T _{OFF}) ⁽⁵⁾	-		

1. Specified by design - Not tested in production, unless otherwise specified.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).
3. DACx_OUT pin is not connected externally (internal connection only).
4. Refer to [Table 58](#).

5. T_{ON} is the refresh phase duration, T_{OFF} is the hold phase duration. Refer to the reference manual for more details.

Table 99. DAC accuracy⁽¹⁾

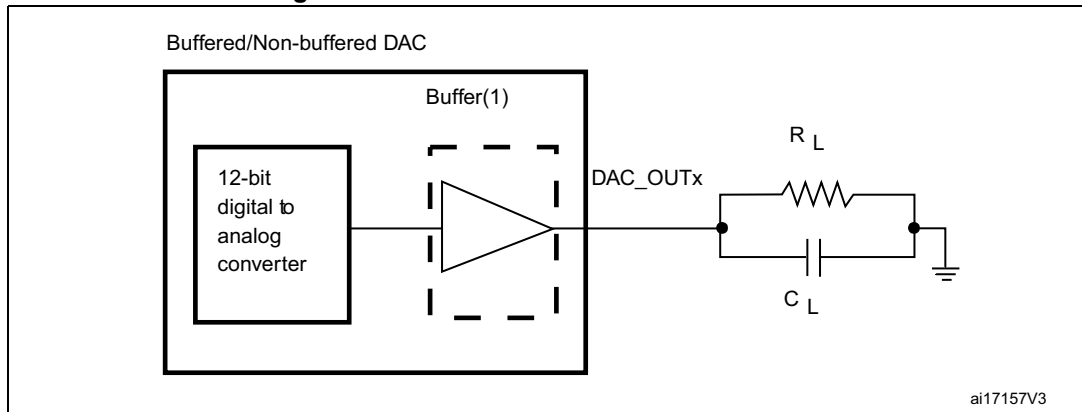
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential non linearity ⁽²⁾	DAC output buffer ON	-2	-	2	LSB
		DAC output buffer OFF	-2	-	2	
-	Monotonicity	10 bits	-	-	-	-
INL	Integral non linearity ⁽³⁾	DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$	-4	-	4	
		DAC output buffer OFF, $C_L \leq 50 \text{ pF}$, no R_L	-4	-	4	
Offset	Offset error at code 0x800 ⁽³⁾	DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$, $V_{REF+} = 3.6 \text{ V}$	-	-	± 12	LSB
		DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$, $V_{REF+} = 1.8 \text{ V}$	-	-	± 25	
		DAC output buffer OFF, $C_L \leq 50 \text{ pF}$, no R_L	-	-	± 8	
Offset1	Offset error at code 0x001 ⁽⁴⁾	DAC output buffer OFF, $C_L \leq 50 \text{ pF}$, no R_L	-	-	± 5	
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$, $V_{REF+} = 3.6 \text{ V}$	-	-	± 5	
		DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$, $V_{REF+} = 1.8 \text{ V}$	-	-	± 7	
Gain	Gain error ⁽⁵⁾	DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$	-	-	± 1	%
		DAC output buffer OFF, $C_L \leq 50 \text{ pF}$, no R_L	-	-	± 1	
TUE	Total unadjusted error	DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$	-	-	± 30	LSB
		DAC output buffer OFF, $C_L \leq 50 \text{ pF}$, no R_L			± 12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$	-	-	± 23	
SNR	Signal-to-noise ratio ⁽⁶⁾	DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$, 1 kHz, BW = 500 kHz	-	67.8	-	
		DAC output buffer OFF, $C_L \leq 50 \text{ pF}$, no R_L , 1 kHz, BW = 500 kHz	-	67.8	-	
THD	Total harmonic distortion ⁽⁶⁾	DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$, 1 kHz	-	-78.6	-	dB
		DAC output buffer OFF, $C_L \leq 50 \text{ pF}$, no R_L , 1 kHz	-	-78.6	-	
SINAD	Signal-to-noise and distortion ratio ⁽⁶⁾	DAC output buffer ON, $C_L \leq 50 \text{ pF}$, $R_L \geq 5 \text{ k}\Omega$, 1 kHz	-	67.5	-	
		DAC output buffer OFF, $C_L \leq 50 \text{ pF}$, no R_L , 1 kHz	-	67.5	-	

Table 99. DAC accuracy⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ k Ω , 1 kHz	-	10.9	-	bits
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L , 1 kHz	-	10.9	-	

1. Evaluated by characterization - Not tested in production.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFFF when the buffer is OFF, and from code giving 0.2 V and ($V_{REF+} - 0.2$ V) when the buffer is ON.
6. Signal is -0.5 dBFS with $F_{sampling} = 1$ MHz.

Figure 60. 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly, without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.25 Analog temperature sensor characteristics

Table 100. Analog temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature (from V_{SENSOR} voltage)	-	-	3	$^{\circ}C$
	V_{SENSE} linearity with temperature (from ADC counter)	-	-	3	
Avg_Slope ⁽²⁾	Average slope (from V_{SENSOR} voltage)	-	2	-	mV/ $^{\circ}C$
	Average slope (from ADC counter)	-	2	-	
$V_{30}^{(3)}$	Voltage at 30 $^{\circ}C \pm 5$ $^{\circ}C$	-	0.62	-	V
t_{start_run}	Startup time in Run mode (buffer startup)	-	-	25.2	μs
$t_{S_temp}^{(1)}$	ADC sampling time when reading the temperature	9	-	-	
$I_{sens}^{(1)}$	Sensor consumption	-	0.18	0.31	μA
$I_{sensbuf}^{(1)}$	Sensor buffer consumption	-	3.8	6.5	

1. Specified by design - Not tested in production.
2. Evaluated by characterization - Not tested in production.
3. Measured at $V_{DDA} = 3.3 \text{ V} \pm 10 \text{ mV}$. The V_{30} ADC conversion result is stored in the TS_CAL1 bytes.

Table 101. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, $V_{DDA} = 3.3 \text{ V}$	0x08FF F814 - 0x08FF F815
TS_CAL2	Temperature sensor raw data acquired value at 130 °C, $V_{DDA} = 3.3 \text{ V}$	0x08FF F818 - 0x08FF F819

5.3.26 Digital temperature sensor characteristics

Table 102. Digital temperature sensor characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DTS}^{(2)}$	Output clock frequency	-	500	750	1150	kHz
$T_{LC}^{(2)}$	Temperature linearity coefficient	VOS2	1660	2100	2750	Hz/°C
$T_{TOTAL_ERROR}^{(2)}$	Temperature offset measurement, all VOS	$T_J = -40 \text{ to } 30 \text{ °C}$	-13	-	4	°C
		$T_J = 30 \text{ °C to } T_{Jmax}$	-7	-	2	
T_{VDD_CORE}	Additional error due to supply variation	VOS2	0	-	0	°C
		VOS0, VOS1, VOS3	-1	-	1	
t_{TRIM}	Calibration time	-	-	-	2	ms
t_{WAKE_UP}	Wake-up time from off state until DTS ready bit is set	-	-	67	116	µs
I_{DDCORE_DTS}	DTS consumption on V_{DD_CORE}	-	8.5	30	70	µA

1. Specified by design - Not tested in production, unless otherwise specified.
2. Evaluated by characterization - Not tested in production.

5.3.27 V_{CORE} monitoring characteristics

Table 103. V_{CORE} monitoring characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
T_{S_VCORE}	ADC sampling time when reading the V_{CORE} voltage	1	-	-	µs

1. Specified by design - Not tested in production.

5.3.28 Temperature and V_{BAT} monitoring

Table 104. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V _{BAT}	-	4 x 26	-	kΩ
Q	Ratio on V _{BAT} measurement	-	4	-	-
Er ⁽¹⁾	Error on Q	-10	-	+10	%
t _{S_vbat} ⁽¹⁾	ADC sampling time when reading V _{BAT} input	9	-	-	μs
V _{BAThigh}	High supply monitoring	3.50	3.575	3.63	V
V _{BATlow}	Low supply monitoring	-	1.36	-	
I _{VBATbuf}	Sensor buffer consumption	-	3.8	6.5	μA

1. Specified by design - Not tested in production.

Table 105. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R _{BC}	Battery charging resistor	VBRS in PWR_CR3 = 0	-	5	-	kΩ
		VBRS in PWR_CR3 = 1	-	1.5	-	

Table 106. Temperature monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
TEMP _{high}	High temperature monitoring	-	126	-	°C
TEMP _{low}	Low temperature monitoring	-	-37	-	

5.3.29 Voltage booster for analog switch

Table 107. Voltage booster for analog switch characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{DD}	Supply voltage	-	1.71	2.6	3.6	V
t _{SU(BOOST)}	Booster startup time	-	-	-	50	μs
I _{DD(BOOST)}	Booster consumption	1.71 V ≤ V _{DD} ≤ 2.7 V	-	-	125	μA
		2.7 V < V _{DD} < 3.6 V	-	-	250	

1. Evaluated by characterization - Not tested in production.

5.3.30 V_{REFBUF} characteristicsTable 108. V_{REFBUF} characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode at $V_{\text{DDA}} = 3.3 \text{ V}$	VRS = 000	2.8	3.3	3.6	V
			VRS = 001	2.4	-	3.6	
			VRS = 010	2.1	-	3.6	
		Degraded mode ⁽²⁾	VRS = 000	1.62	-	2.80	
			VRS = 001	1.62	-	2.40	
			VRS = 010	1.62	-	2.10	
$V_{\text{REFBUF_OUT}}$	Voltage reference buffer output	Normal mode at $30 \text{ }^\circ\text{C}$, $I_{\text{LOAD}} = 100 \text{ }\mu\text{A}$	VRS = 000	2.498 ⁽³⁾	2.5000	2.5035 ⁽³⁾	V
			VRS = 001	2.0460	2.0490	2.0520	
			VRS = 010	1.8010	1.8040	1.8060	
		Degraded mode ⁽²⁾	VRS = 000	$V_{\text{DDA}} - 150 \text{ mV}$	-	2.5035	
			VRS = 001	$V_{\text{DDA}} - 150 \text{ mV}$	-	2.0520	
			VRS = 010	$V_{\text{DDA}} - 150 \text{ mV}$	-	1.8060	
TRIM	Trim step resolution	-	-	-	± 0.05	± 0.1	%
C_{L}	Load capacitor	-	-	0.5	1	1.50	μF
esr	Equivalent serial resistor of C_{L}	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
$I_{\text{line_reg}}$	Line regulation	$2.8 \text{ V} \leq V_{\text{DDA}} \leq 3.6 \text{ V}$	$I_{\text{load}} = 500 \text{ }\mu\text{A}$	-	200	-	ppm/ V
			$I_{\text{load}} = 4 \text{ mA}$	-	100	-	
$I_{\text{load_reg}}$	Load regulation	$500 \text{ }\mu\text{A} \leq I_{\text{load}} \leq 4 \text{ mA}$	Normal mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	$-40 \text{ }^\circ\text{C} < T_{\text{J}} < +130 \text{ }^\circ\text{C}$	-	-	-	100	ppm/ $^\circ\text{C}$
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100 kHz	-	-	40	-	
t_{START}	Start-up time	$C_{\text{L}} = 0.5 \text{ }\mu\text{F}$	-	-	300	-	μs
		$C_{\text{L}} = 1 \text{ }\mu\text{F}$	-	-	500	-	
		$C_{\text{L}} = 1.5 \text{ }\mu\text{F}$	-	-	650	-	

Table 108. V_{REFBUF} characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I _{INRUSH}	Control of maximum DC current drive on V _{REFBUF_OUT} during startup phase ⁽⁴⁾⁽⁴⁾	-		-	8	-	mA
I _{DDA(VREFBUF)}	VREFBUF consumption from VDDA	I _{LOAD} = 0 μA	-	-	15	25	μA
		I _{LOAD} = 500 μA	-	-	16	30	
		I _{LOAD} = 4 mA	-	-	32	50	

1. Specified by design - Not tested in production, unless otherwise specified.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}-drop voltage).
3. Evaluated by characterization - Not tested in production.
4. To properly control V_{REFBUF} I_{INRUSH} current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 2.1 V - 3.6 V, 2.4 V - 3.6 V and 2.8 V - 3.6 V for VRS = 010, 001, and 000, respectively.

5.3.31 Timer characteristics

The parameters given in [Table 109](#) are guaranteed by design.

Refer to [Section 5.3.15](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 109. TIMx characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions ⁽³⁾	Min	Max	Unit
t _{res(TIM)}	Timer resolution time	AHB/APBx prescaler = 1, 2, or 4, f _{TIMxCLK} = 250 MHz	1	-	t _{TIMxCLK}
		AHB/APBx prescaler > 4, f _{TIMxCLK} = 125 MHz	1	-	t _{TIMxCLK}
f _{EXT}	Timer external clock frequency on CH1 to CH4	f _{TIMxCLK} = 250 MHz	0	f _{TIMxCLK} / 2	MHz
Res _{TIM}	Timer resolution		-	16 / 32	bit
t _{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	t _{TIMxCLK}

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Specified by design - Not tested in production.
3. The maximum timer frequency on APB1 or APB2 is up to 250 MHz, by setting the TIMPRE bit in the RCC_CFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = rcc_hclk1, otherwise TIMxCLK = 4 × F_{rcc_pclkx1} or TIMxCLK = 4 × F_{rcc_pclkx2}.

5.3.32 Low-power timer characteristics

Table 110. LPTIMx characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	250	MHz
f_{EXT}	Timer external clock frequency on Input1 and Input2	0	$f_{LPTIMxCLK}/2$	
Res _{TIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{TIMxCLK}$

1. LPTIMx is used as a general term for LPTIM1 to LPTIM6 timers.
2. Specified by design - Not tested in production.

5.3.33 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are specified by design, not tested in production, when the I²C peripheral is properly configured (refer to the product reference manual)

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to [Section 5.3.15](#) for the I²C I/Os characteristics

All I²C SDA and SCL I/Os embed an analog filter, refer to [Table 111](#) for its characteristics.

Table 111. I²C analog filter characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes suppressed by analog filter	50 ⁽³⁾	160 ⁽⁴⁾	ns

1. Evaluated by characterization - Not tested in production.
2. Measurement points are done at 50% V_{DD}.
3. Spikes with widths below $t_{AF(min)}$ are filtered.
4. Spikes with widths above $t_{AF(max)}$ are not filtered.

USART interface characteristics

Unless otherwise specified, the parameters given in [Table 112](#) are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load $C_L = 30$ pF
- Measurement points are done at CMOS levels: $0.5 V_{DD}$
- I/O compensation cell activated
- VOS level set to VOS0
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 112. USART characteristics⁽¹⁾

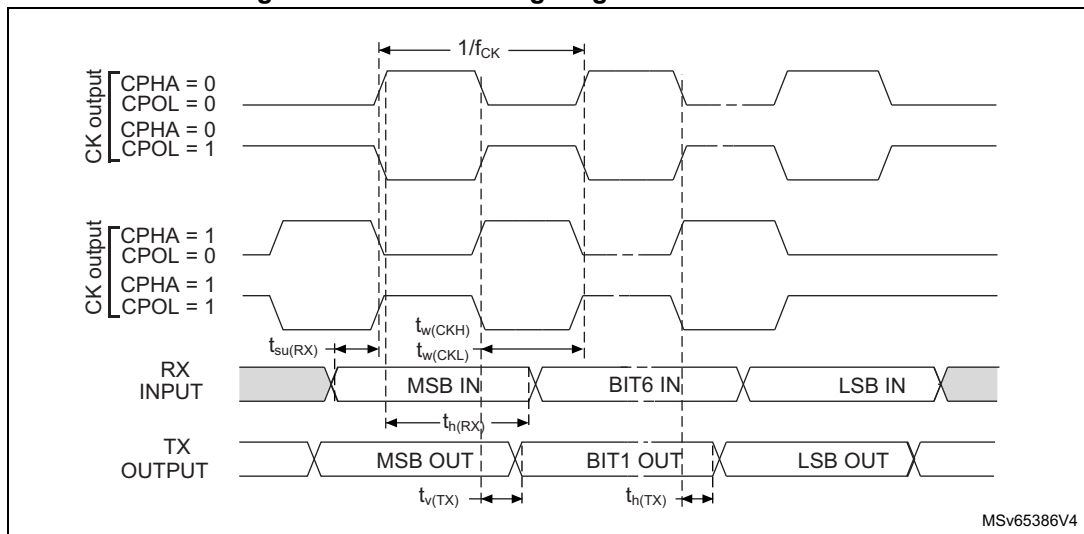
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master receiver $1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	31	MHz
		Master transmitter $1.71\text{ V} < V_{DD} < 3.6\text{ V}$			$31/6^{(2)}$	
		Master transmitter $2.7\text{ V} < V_{DD} < 3.6\text{ V}$			$31/6^{(2)}$	
		Slave receiver $1.71\text{ V} < V_{DD} < 3.6\text{ V}$			83	
		Slave transmitter $1.71\text{ V} < V_{DD} < 3.6\text{ V}$			$32/6^{(2)}$	
		Slave transmitter $2.7\text{ V} < V_{DD} < 3.6\text{ V}$			$35/6^{(2)}$	
$t_{su(NSS)}$	NSS setup time	Slave mode	$t_{ker}^{(3)} + 3.5$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2.5	-	-	
$t_w(SCKH)$ $t_w(SCKL)$	CK high and low time	Master mode	$1/f_{ck}/2 - 1$	$1/f_{ck}/2$	$1/f_{ck}/2 + 1$	
		Master mode	13	-	-	
$t_{su(RX)}$	Data input setup time	Slave mode	3.5	-	-	
		Slave mode	0.5	-	-	
$t_{h(RX)}$	Data input hold time	Slave mode	1.5	-	-	
		Slave mode	-	11.5	$15.5/71^{(2)}$	
$t_{v(TX)}$	Data output valid time	Slave mode, $1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	11.5	$14/35^{(2)}$	
		Slave mode, $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-		$3/52^{(2)}$	
		Slave mode, $1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	2.5	$3/22^{(2)}$	
		Slave mode, $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-		$3/22^{(2)}$	

Table 112. USART characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(TX)}$	Data output hold time	Slave mode	7.5	-	-	ns
		Master mode	0	-	-	

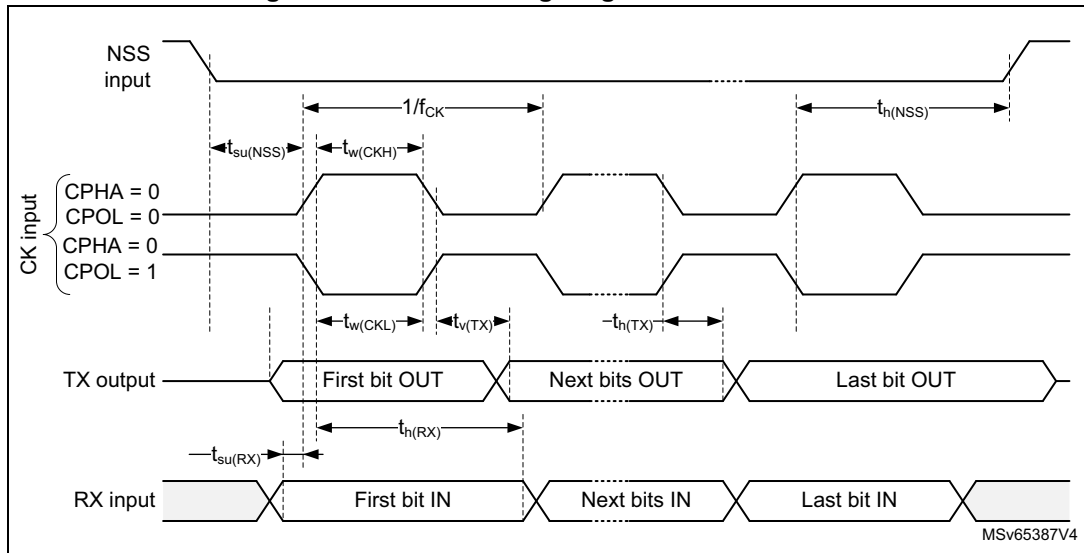
1. Evaluated by characterization - Not tested in production.
2. For PB14 with OSPEEDRy[1:0] = 01.
3. T_{ker} is the usart_ker_ck_pres clock period.

Figure 61. USART timing diagram in Master mode



1. Measurement points are done at 0.5V_{DD} and with external C_L = 30 pF.

Figure 62. USART timing diagram in Slave mode



I3C interface characteristics

The I3C interface meets the timings requirements of the MIPI® I3C specification v1.1.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

The parameters given in [Table 113](#) are obtained with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0

The timings are in line with MIPI specification, except for the ones given in [Table 113](#) and [Table 114](#). For t_{SU_OD} and t_{SU_PP} this can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register. For t_{SCO} this can be mitigated by enabling and adjusting the clock stall time both on the address ACK phase and on the data read Tbit phase in the I3C_TIMINGR2 register. This can also be mitigated by increasing the SCL low duration in the I3C_TIMINGR0 register. For further details refer to AN5879.

Table 113. I3C open-drain measured timing

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements	Unit
			Min	Max		
t_{SU_OD}	SDA data setup time during open drain mode	Controller $1.71\text{ V} < V_{DD} < 3.6\text{ V}$	3	-	16.5	ns

Table 114. I3C push-pull measured timing

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements	Unit
			Min	Max		
t_{SU_PP}	SDA signal data setup in push-pull mode	Controller $1.71\text{ V} < V_{DD} < 3.6\text{ V}$	3	-	12	ns

SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 115](#) are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load $C_L = 30$ pF
- Measurement points are done at CMOS levels: $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V

- VOS level set to VOS0

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 115. SPI characteristics⁽¹⁾

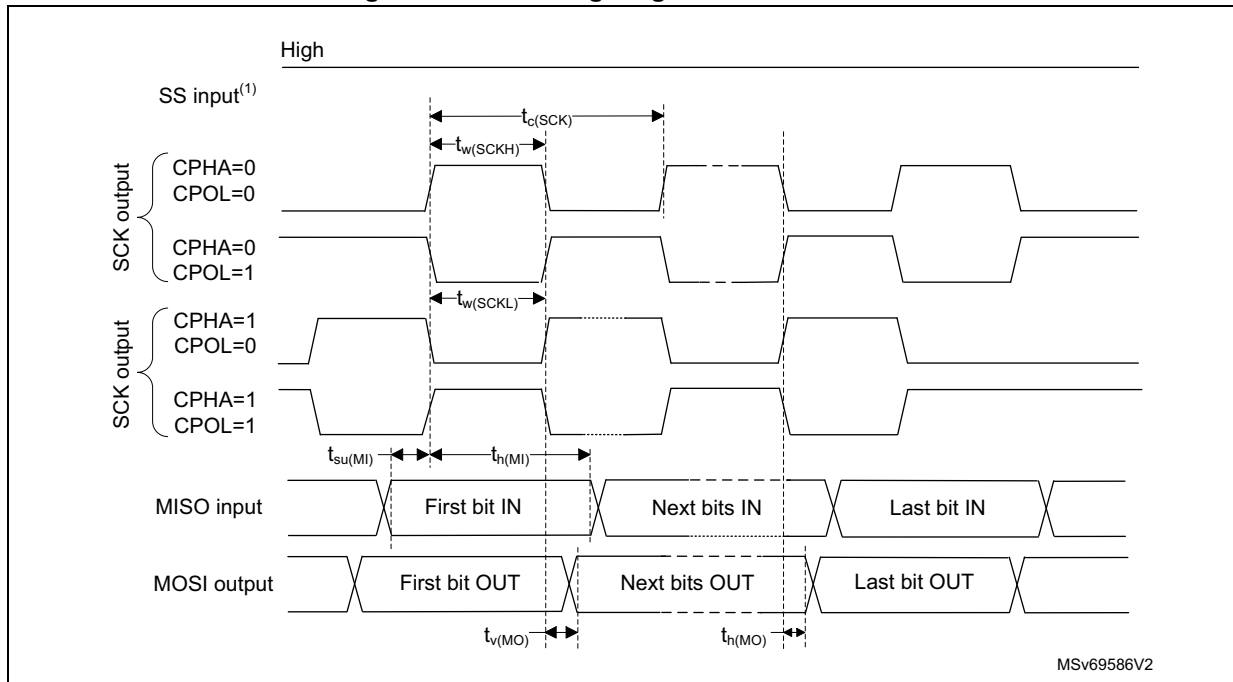
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{SCK} 1/t _{SCK}	SPI clock frequency	Master receiver mode 2.7 V < V _{DD} < 3.6 V	-	-	135/3 ⁽²⁾	MHz
		Master receiver mode 1.71 V < V _{DD} < 2.7 V	-	-	120/3 ⁽²⁾	
		Master transmitter mode 2.7 V < V _{DD} < 3.6 V	-	-	135/3 ⁽²⁾	
		Master transmitter mode 1.71 V < V _{DD} < 3.6 V	-	-	120/3 ⁽²⁾	
		Slave receiver mode 1.71 V < V _{DD} < 3.6 V	-	-	120	
		Slave transmitter mode 2.7 V < V _{DD} < 3.6 V	-	-	43/6 ⁽³⁾	
		Slave transmitter mode 1.71 V < V _{DD} < 2.7 V	-	-	41/6 ⁽³⁾	
t _{su(NSS)}	NSS setup time	Slave mode	3.5	-	-	ns
t _{h(NSS)}	NSS hold time	Slave mode	4.5	-	-	ns
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode	(t _{SCK} /2) - 1	(t _{SCK} /2)	(t _{SCK} /2) + 1	ns
t _{su(MI)}	Data input setup time	Master mode	3.5	-	-	ns
t _{su(SI)}		Slave mode	2	-	-	
t _{h(MI)}	Data input hold time	Master mode	1	-	-	ns
t _{h(SI)}		Slave mode	1.5	-	-	
t _{a(SO)}	Data output access time	Slave mode	6.5	-	15	ns
t _{dis(SO)}	Data output disable time	Slave mode	7.5	-	18	ns
t _{v(SO)}	Data output valid time	Slave mode, 2.7 V < V _{DD} < 3.6 V	-	8.5/25 ⁽³⁾	11.5/33 ⁽³⁾	ns
		Slave mode, 1.71 V < V _{DD} < 3.6 V	-	10/59 ⁽³⁾	12/76 ⁽³⁾	
t _{v(MO)}		Master mode	-	1.5	2	
t _{h(SO)}	Data output hold time	Slave mode, 1.71 V < V _{DD} < 3.6 V	6.5/20.5 ⁽³⁾	-	-	ns
t _{h(MO)}		Master mode	0	-	-	

1. Evaluated by characterization - Not tested in production.

2. When using PB13.

3. When using PB14.

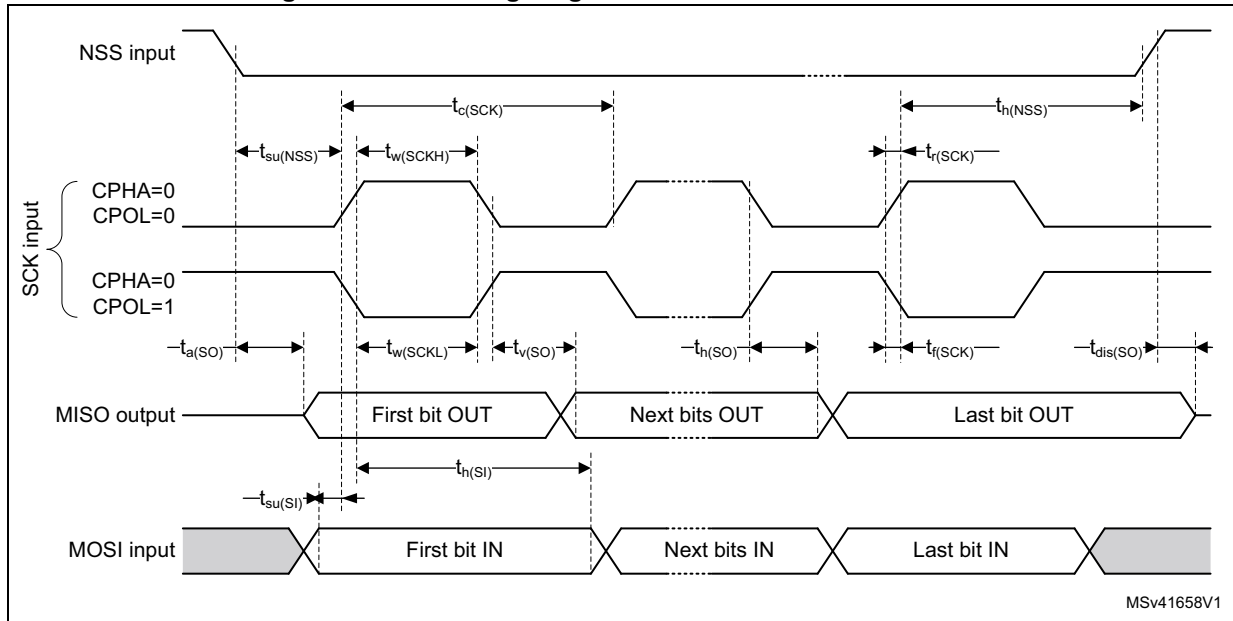
Figure 63. SPI timing diagram - Master mode



MSv69586V2

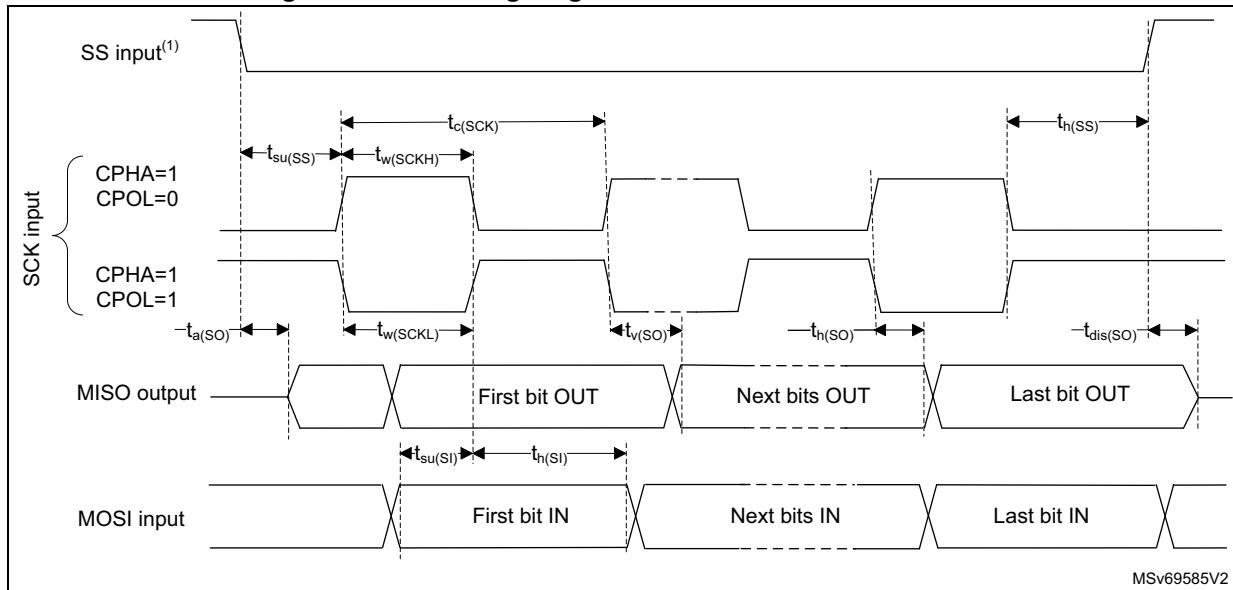
1. The SS input can be configured to active low or active high.

Figure 64. SPI timing diagram - Slave mode and CPHA = 0



MSv41658V1

Figure 65. SPI timing diagram - Slave mode and CPHA = 1



1. The SS input can be configured to active low or active high.

I²S Interface characteristics

Unless otherwise specified, the parameters given in [Table 116](#) are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 11$
- Capacitive load $C_L = 30$ pF
- Measurement points are done at CMOS levels: $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics (CK,SD,WS).

Table 116. I²S dynamic characteristics⁽¹⁾

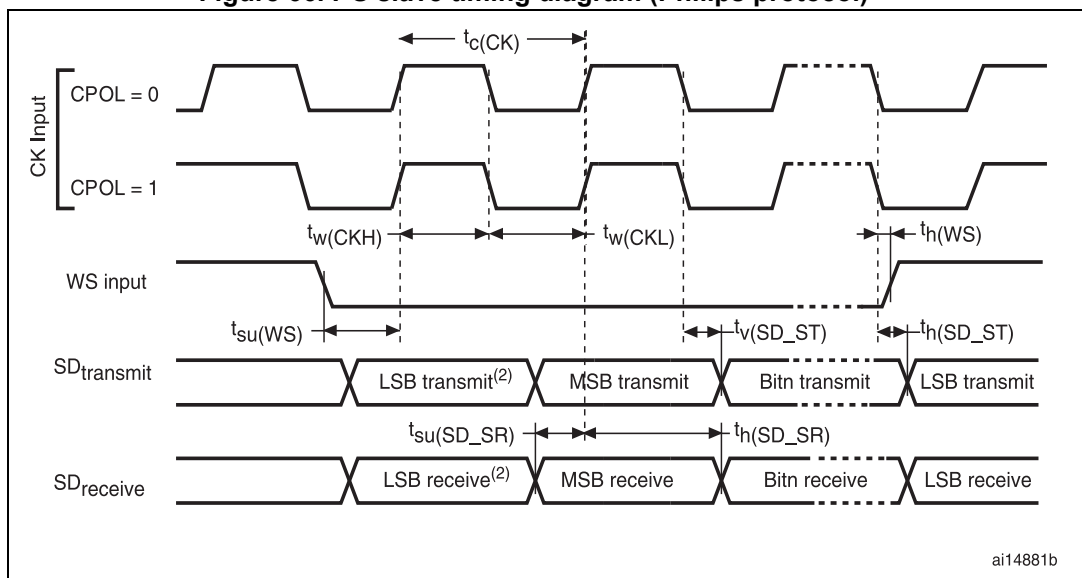
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I ² S main clock output	-	-	50	MHz
f_{CK}	I ² S clock output	Master transmitter	-	50	
		Slave transmitter (TX)	-	21	
		Slave receiver (RX)	-	50	

Table 116. I²S dynamic characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(WS)}$	WS valid time	Master mode	-	2	ns
$t_{h(WS)}$	WS hold time		0.5	-	
$t_{su(WS)}$	WS setup time	Slave mode	3	-	
$t_{h(WS)}$	WS hold time		1.5	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	4	-	
$t_{su(SD_SR)}$		Slave receiver	2	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	1	-	
$t_{h(SD_SR)}$		Slave receiver	1.5	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	14	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	1	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5.5	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	

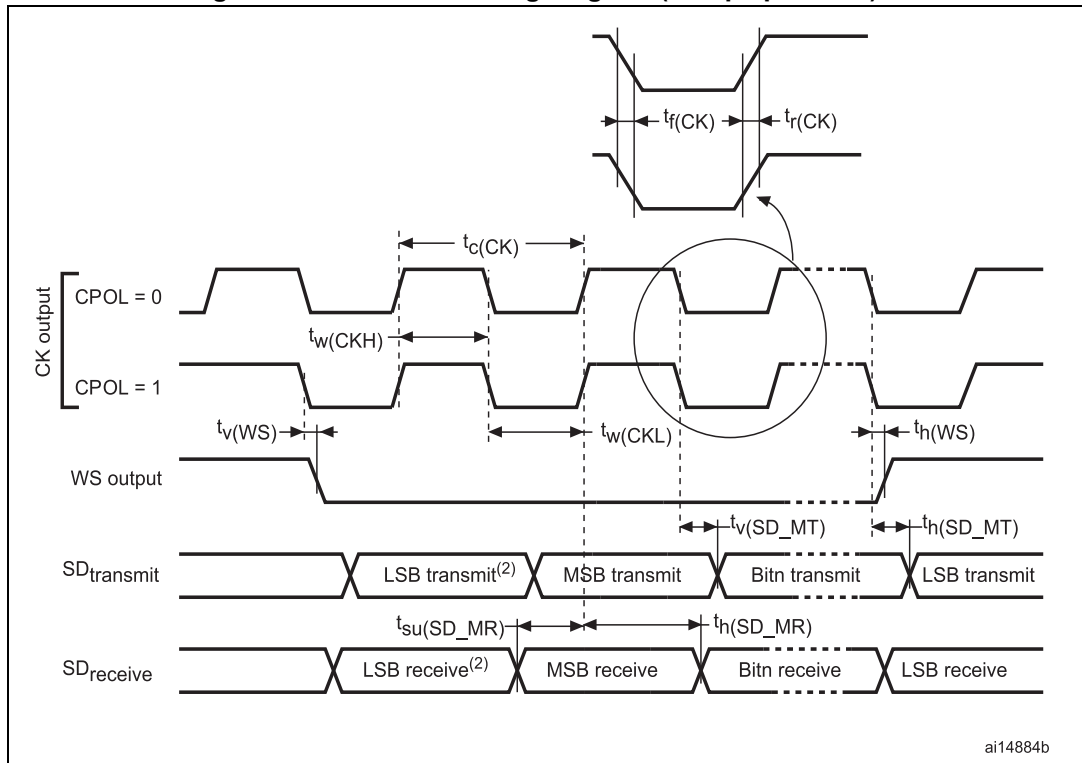
1. Evaluated by characterization - Not tested in production.

Figure 66. I²S slave timing diagram (Philips protocol)⁽¹⁾



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 67. I²S master timing diagram (Philips protocol)⁽¹⁾



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB full speed (FS) characteristics

The USB interface is fully compliant with the USB specification version 2.0.

Table 117. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
V _{DD}	USB full speed transceiver operating voltage	-	3.0 ⁽²⁾	-	3.6	V
V _{DI} ⁽³⁾	Differential input sensitivity	Over V _{CM} range	0.2	-	-	V
V _{CM} ⁽³⁾	Differential input common mode range	Includes V _{DI} range	0.8	-	2.5	
V _{SE} ⁽³⁾	Single ended receiver input threshold	-	0.8	-	2.0	
V _{OL}	Static output level low	R _L of 1.5 kΩ to 3.6 V ⁽⁴⁾	-	-	0.3	V
V _{OH}	Static output level high	R _L of 15 kΩ to V _{SS} ⁽⁴⁾	2.8	-	3.6	
R _{PD} ⁽³⁾	Pull down resistor on PA11, PA12 (USB_DP/DM)	V _{IN} = V _{DD}	14.25	-	24.8	kΩ
R _{PU} ⁽³⁾	Pull-up resistor on PA12 (USB_DP)	V _{IN} = V _{SS} , during idle	0.9	1.25	1.575	
	Pull-up resistor on PA12 (USB_DP)	V _{IN} = V _{SS} during reception	1.425	2.25	3.09	

1. All the voltages are measured from the local ground potential.
2. The USB full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics, which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Specified by design - Not tested in production.

4. R_L is the load connected on the USB full speed drivers.

Figure 68. USB timings - definition of data signal rise and fall time

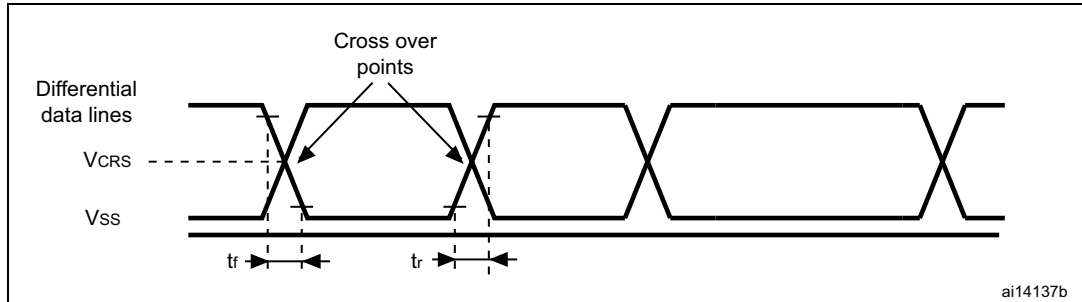


Table 118. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}^{(1)}$	USB transceiver startup time	1	μs

1. Specified by design - Not tested in production.

Table 119. USB electrical characteristics⁽¹⁾

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_{rLS}	Rise time in LS ⁽²⁾	$C_L = 200$ to 600 pF	75	300	ns
t_{fLS}	Fall time in LS ⁽²⁾	$C_L = 200$ to 600 pF	75	300	ns
t_{rfmLS}	Rise/fall time matching in LS	t_r/t_f	80	125	%
t_{rFS}	Rise time in FS ⁽²⁾	$C_L = 50$ pF	4	20	ns
t_{fFS}	Fall time in FS ⁽²⁾	$C_L = 50$ pF	4	20	ns
t_{rfmFS}	Rise/fall time matching in FS	t_r/t_f	90	111	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	1.3	2.0	V
Z_{DRV}	Output driver impedance ⁽³⁾	Driving high or low	28	44	Ω

- Specified by design - Not tested in production.
- Measured from 10% to 90% of the data signal. For more detailed information, refer to USB specification - chapter 7 (version 2.0).
- No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 120. USB BCD DC electrical characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	-	-	300	μA
	Secondary detection mode consumption	-	-	-	300	
R_{DAT_LKG}	Data line leakage resistance	-	300	-	-	k Ω
V_{DAT_LKG}	Data line leakage voltage	-	0.0	-	3.6	V

Table 120. USB BCD DC electrical characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RDCP_DAT	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
VLGC_HI	Logic high	-	2.0	-	3.6	V
VLGC_LOW	Logic low	-	-	-	0.8	
VLGC	Logic threshold	-	0.8	-	2.0	
VDAT_REF	Data detect voltage	-	0.25	-	0.4	
VDP_SRC	D+ source voltage	-	0.5	-	0.7	
VDM_SRC	D- source voltage	-	0.5	-	0.7	
IDP_SINK	D+ sink current	-	25	-	175	μA
IDM_SINK	D- sink current	-	25	-	175	

1. Specified by design - Not tested in production.

SAI characteristics

Unless otherwise specified, the parameters given in [Table 121](#) are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load $C_L = 30$ pF
- I/O compensation cell activated
- Measurement points are done at CMOS levels: $0.5 V_{DD}$
- VOS level set to VOS0

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics (SCK, SD, WS).

Table 121. SAI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency	Master transmitter, $2.7 V \leq V_{DD} \leq 3.6 V$	-	38	
		Master transmitter, $1.71 V \leq V_{DD} \leq 3.6 V$	-	38	
		Master receiver, $1.71 V \leq V_{DD} \leq 3.6 V$	-	38	
		Slave transmitter, $2.7 V \leq V_{DD} \leq 3.6 V$	-	34	
		Slave transmitter, $1.71 V \leq V_{DD} \leq 3.6 V$	-	33	
		Slave receiver, $1.71 V \leq V_{DD} \leq 3.6 V$	-	50	

Table 121. SAI characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
t _{v(FS)}	F _S valid time	Master mode, 2.7 V ≤ V _{DD} ≤ 3.6 V	-	13	ns
		Master mode, 1.71 V ≤ V _{DD} ≤ 3.6 V	-	13	
t _{su(FS)}	F _S setup time	Slave mode	3	-	
t _{h(FS)}	F _S hold time	Master mode	5	-	
		Slave mode	2	-	
t _{su(SD_A_MR)}	Data input setup time	Master receiver	4	-	
t _{su(SD_B_SR)}		Slave receiver	3.5	-	
t _{h(SD_A_MR)}	Data input hold time	Master receiver	1.5	-	
t _{h(SD_B_SR)}		Slave receiver	0.5	-	
t _{v(SD_B_ST)}	Data output valid time	Slave transmitter (after enable edge), 2.7 V ≤ V _{DD} ≤ 3.6 V	-	14.5	
		Slave transmitter (after enable edge), 1.71 V ≤ V _{DD} ≤ 3.6 V	-	15	
t _{h(SD_B_ST)}	Data output hold time	Slave transmitter (after enable edge)	7	-	
t _{v(SD_A_MT)}	Data output valid time	Master transmitter (after enable edge), 2.7 V ≤ V _{DD} ≤ 3.6 V	-	13	
		Master transmitter (after enable edge), 1.71 V ≤ V _{DD} ≤ 3.6 V	-	13	
t _{h(SD_A_MT)}	Data output hold time	Master transmitter (after enable edge)	5.5	-	

1. Evaluated by characterization - Not tested in production.

Figure 69. SAI master timing waveforms

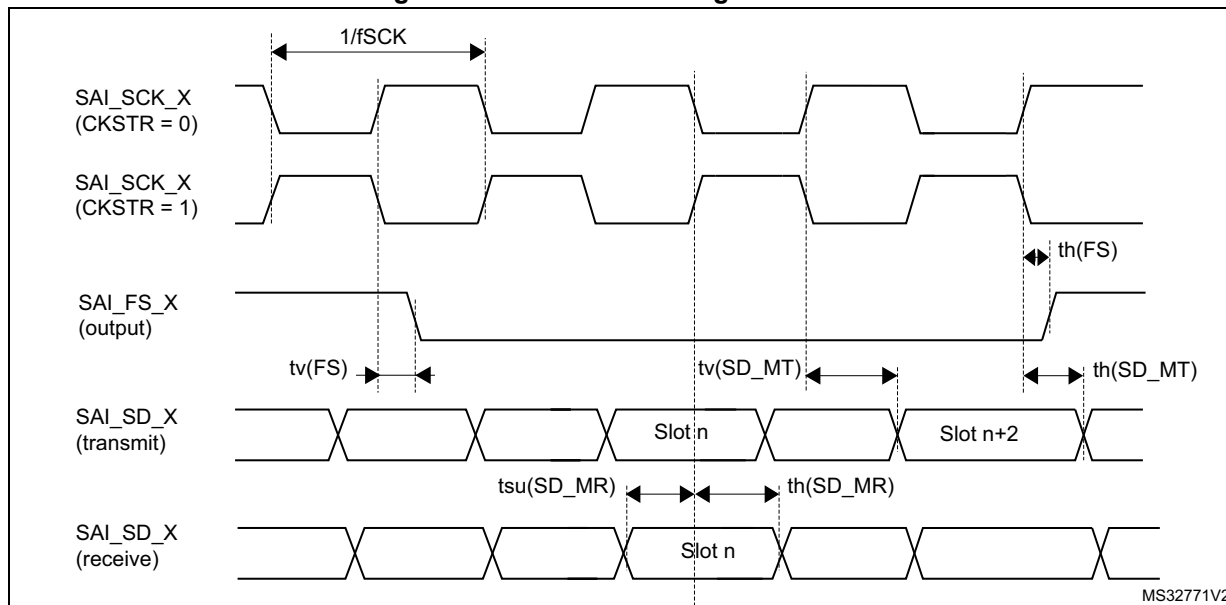
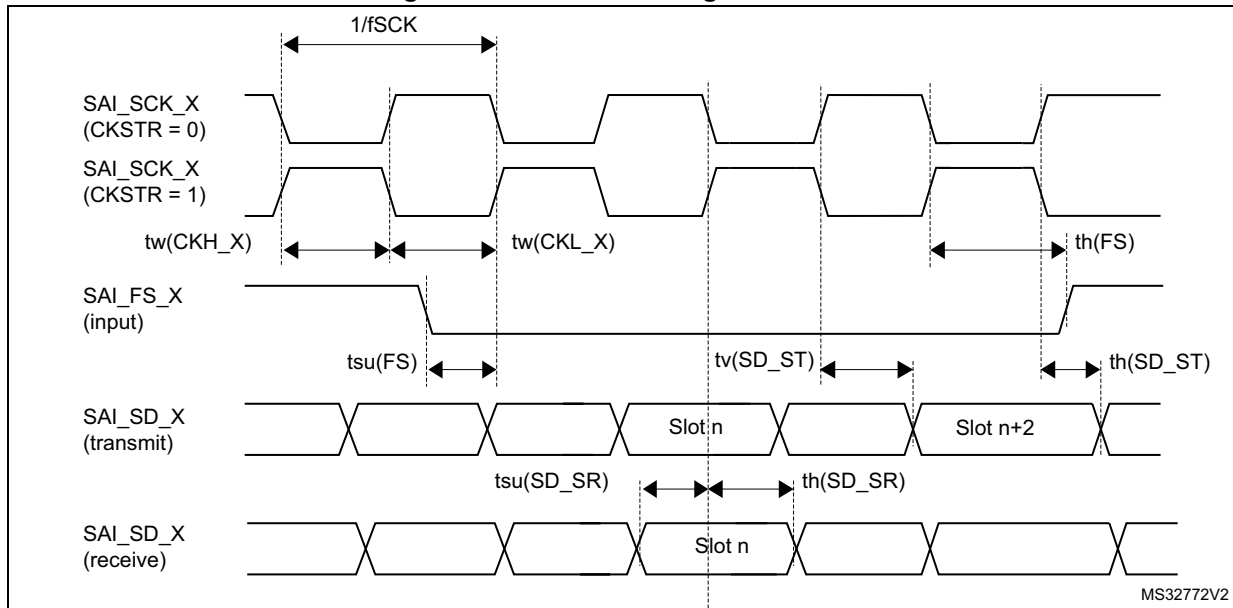


Figure 70. SAI slave timing waveforms



SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in [Table 122](#) and [Table 123](#) are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in [Table 20](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load $C_L = 30$ pF
- Measurement points are done at CMOS levels: $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to [Section 5.3.15](#) for more details on the input/output characteristics.

Table 122. Dynamic characteristics: SD/MMC, $V_{DD} = 2.7$ to 3.6 V⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	$130^{(2)}/6^{(3)}$	MHz
$t_{W(CKL)}$	Clock low time	$f_{PP} = 52$ MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR⁽⁴⁾/DDR⁽⁴⁾ mode						
t_{ISU}	Input setup time HS	-	3	-	-	ns
t_{IH}	Input hold time HS	-	1	-	-	
$t_{IDW}^{(5)}$	Input valid window (variable window)	-	4.5	-	-	
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR⁽⁴⁾/DDR⁽⁴⁾ mode						
t_{OV}	Output valid time HS	-	-	5	$5.5/38^{(3)}$	ns
t_{OH}	Output hold time HS	-	3	-	-	

Table 122. Dynamic characteristics: SD/MMC, $V_{DD} = 2.7$ to 3.6 V⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	2.5		-	ns
t_{IHD}	Input hold time SD	-	1.5		-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	0.5	1/33 ⁽³⁾	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. Evaluated by characterization - Not tested in production.
2. C_L applied is 20 pF.
3. When using PB13 and PB14.
4. For SD 1.8 V support, an external voltage converter is needed.
5. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Table 123. Dynamic characteristics: eMMC, $V_{DD} = 1.71$ to 1.9 V⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	110 ⁽²⁾ /6 ⁽³⁾	MHz
$t_{W(CKL)}$	Clock low time	$f_{PP} = 52$ MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	-	1.5	-	-	ns
t_{IHD}	Input hold time HS	-	1.5	-	-	
$t_{IDW}^{(4)}$	Input valid window (variable window)	-	4	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	-	-	5.5	6/75 ⁽³⁾	ns
t_{OH}	Output hold time HS	-	3	-	-	

1. Evaluated by characterization - Not tested in production.
2. $C_L = 20$ pF.
3. When using PB13 and PB14.
4. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Figure 71. SDIO high-speed/eMMC timing

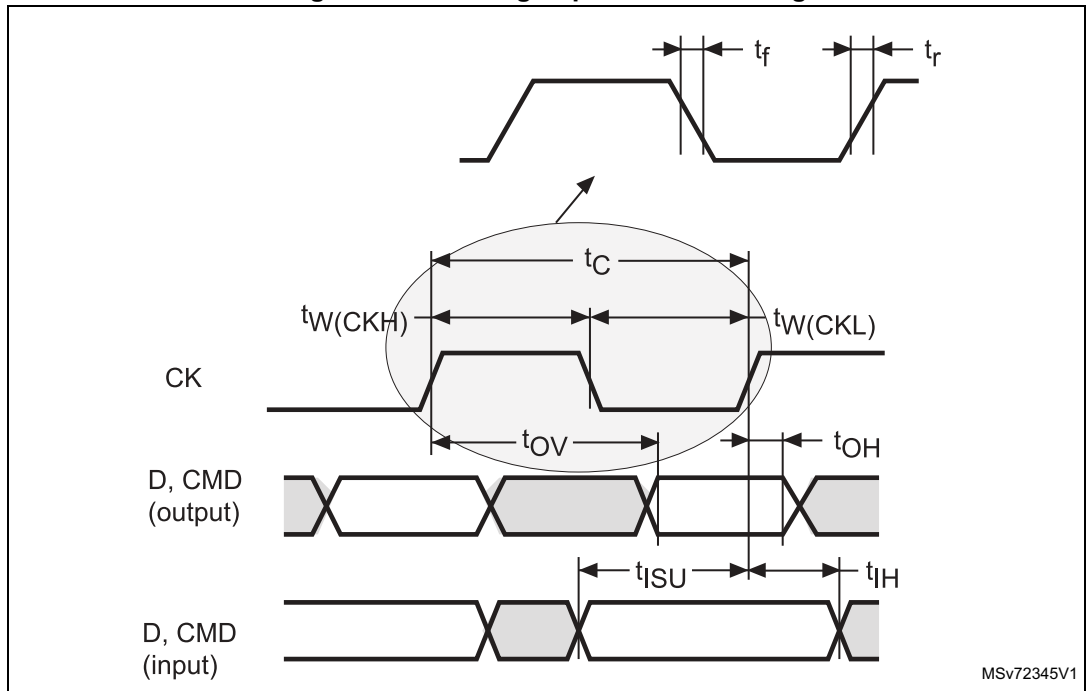


Figure 72. SD default speed timings

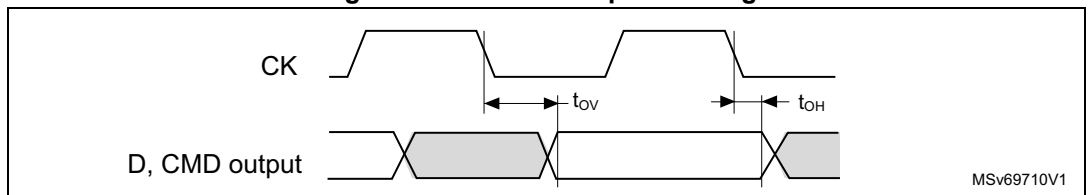
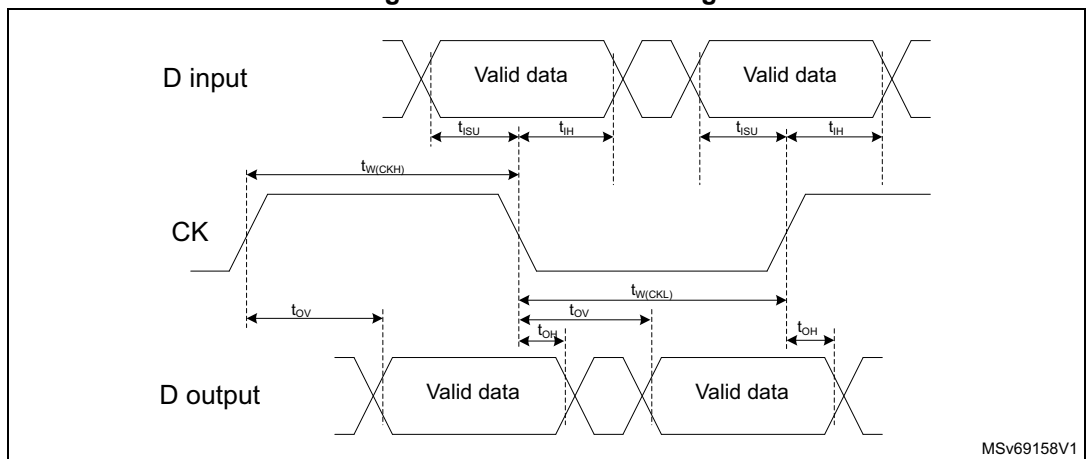


Figure 73. DDR mode timings



Ethernet interface characteristics

Unless otherwise specified, the parameters given in [Table 124](#), [Table 125](#), and [Table 126](#) are derived from tests performed under the ambient temperature, $f_{\text{rcc_c_ck}}$ frequency and V_{DD} supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load $C_L = 20$ pF
- Measurement points are done at CMOS levels: $0.5 V_{\text{DD}}$
- I/O compensation cell activated
- HSLV activated when $V_{\text{DD}} \leq 2.5$ V

Refer to [Section 5.3.15](#) for more details on the input/output characteristics.

Table 124. Dynamic characteristics: Ethernet MAC signals for SMI ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (2.5 MHz)	400	400	403	ns
$T_{\text{d(MDIO)}}$	Write data valid time	0	0.5	1	
$t_{\text{su(MDIO)}}$	Read data setup time	12.5	-	-	
$t_{\text{h(MDIO)}}$	Read data hold time	0	-	-	

1. Evaluated by characterization - Not tested in production.

Table 125. Dynamic characteristics: Ethernet MAC signals for RMII ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{su(RXD)}}$	Receive data setup time	3	-	-	ns
$t_{\text{h(RXD)}}$	Receive data hold time	1	-	-	
$t_{\text{su(CRS)}}$	Carrier sense setup time	2	-	-	
$t_{\text{h(CRS)}}$	Carrier sense hold time	1	-	-	
$t_{\text{d(TXEN)}}$	Transmit enable valid delay time	7.5	9.5	15	
$t_{\text{d(TXD)}}$	Transmit data valid delay time	7.5	10	15.5	

1. Evaluated by characterization - Not tested in production.

Table 126. Dynamic characteristics: Ethernet MAC signals for MII ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su}(RXD)$	Receive data setup time	3	-	-	ns
$t_{ih}(RXD)$	Receive data hold time	1.5	-	-	
$t_{su}(DV)$	Data valid setup time	2	-	-	
$t_{ih}(DV)$	Data valid hold time	1	-	-	
$t_{su}(ER)$	Error setup time	3	-	-	
$t_{ih}(ER)$	Error hold time	1	-	-	
$t_d(TXEN)$	Transmit enable valid delay time	7.5	10	16	
$t_d(TXD)$	Transmit data valid delay time	8	10.5	16.5	

1. Evaluated by characterization - Not tested in production.

Figure 74. Ethernet RMII timing diagram

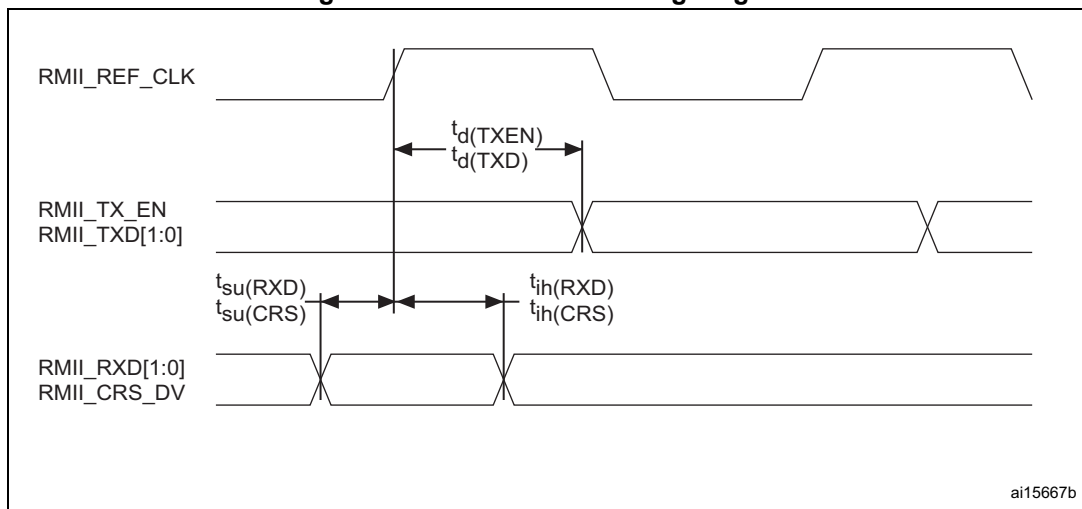


Figure 75. Ethernet MII timing diagram

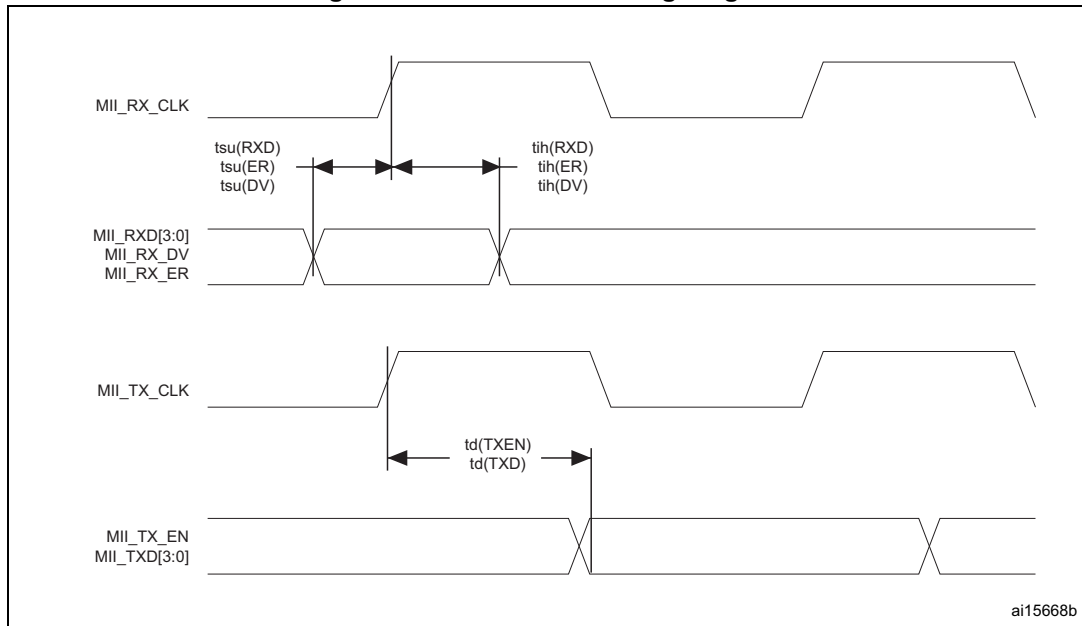
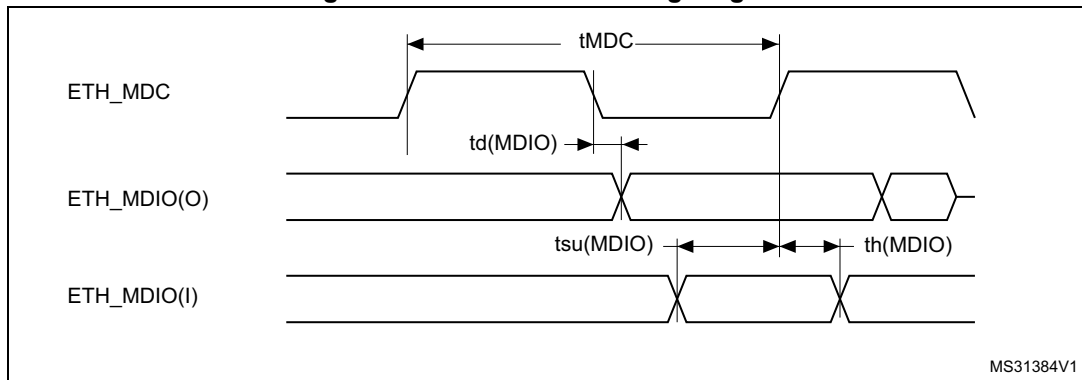


Figure 76. Ethernet SMI timing diagram



JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in [Table 127](#) and [Table 128](#) for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage summarized in [Table 20](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load $C_L = 30$ pF
- HSLV activated when $V_{DD} \leq 2.7$ V
- Measurement points are done at CMOS levels: $0.5 V_{DD}$

Refer to [Section 5.3.15](#) for more details on the input/output characteristics:

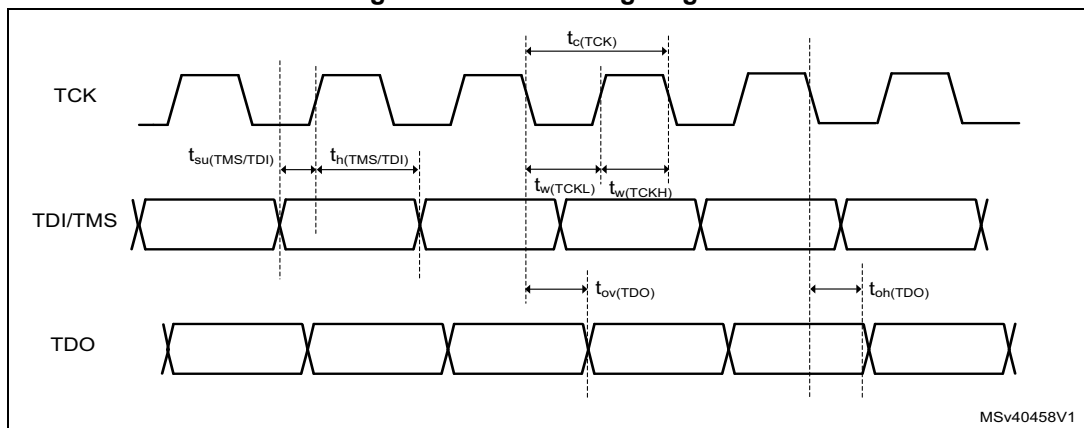
Table 127. Dynamic JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{TCK}	T_{CK} clock frequency	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	50	MHz
$1/t_{c(TCK)}$		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	45	
$t_{i_{su}(TMS)}$	TMS input setup time	-	2	-	-	ns
$t_{i_{h}(TMS)}$	TMS input hold time	-	1.5	-	-	
$t_{i_{su}(TDI)}$	TDI input setup time	-	1.5	-	-	
$t_{i_{h}(TDI)}$	TDI input hold time	-	1.5	-	-	
$t_{ov}(TDO)$	TDO output valid time	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	8	10	
		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	8	11	
$t_{oh}(TDO)$	TDO output hold time	-	6.5	-	-	

Table 128. Dynamic SWD characteristics

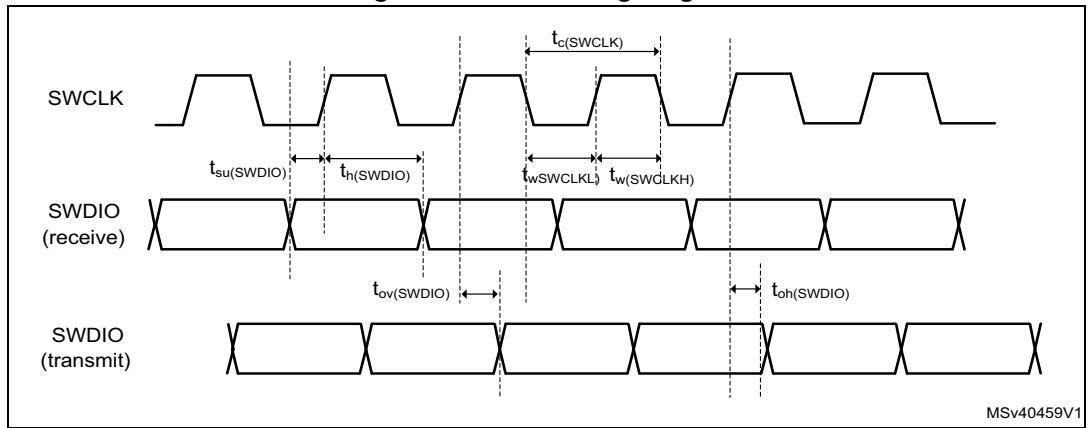
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{SWCLK}	SWCLK clock frequency	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	80	MHz
$1/t_{c(SWCLK)}$		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	71	
$t_{i_{su}(SWDIO)}$	SWDIO input setup time	-	1.5	-	-	ns
$t_{i_{h}(SWDIO)}$	SWDIO input hold time	-	1.5	-	-	
$t_{ov}(SWDIO)$	SWDIO output valid time	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	10.5	12.5	
		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	10.5	14.0	
$t_{oh}(SWDIO)$	SWDIO output hold time	-	8.5	-	-	

Figure 77. JTAG timing diagram



MSv40458V1

Figure 78. SWD timing diagram



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Device marking

Refer to “*Reference device marking schematics for STM32 microcontrollers and microprocessors*” (TN1433), available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

6.2 LQFP64 package information (5W)

This LQFP is 64-pin, 10 x 10 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 79. LQFP64 - Outline⁽¹⁵⁾

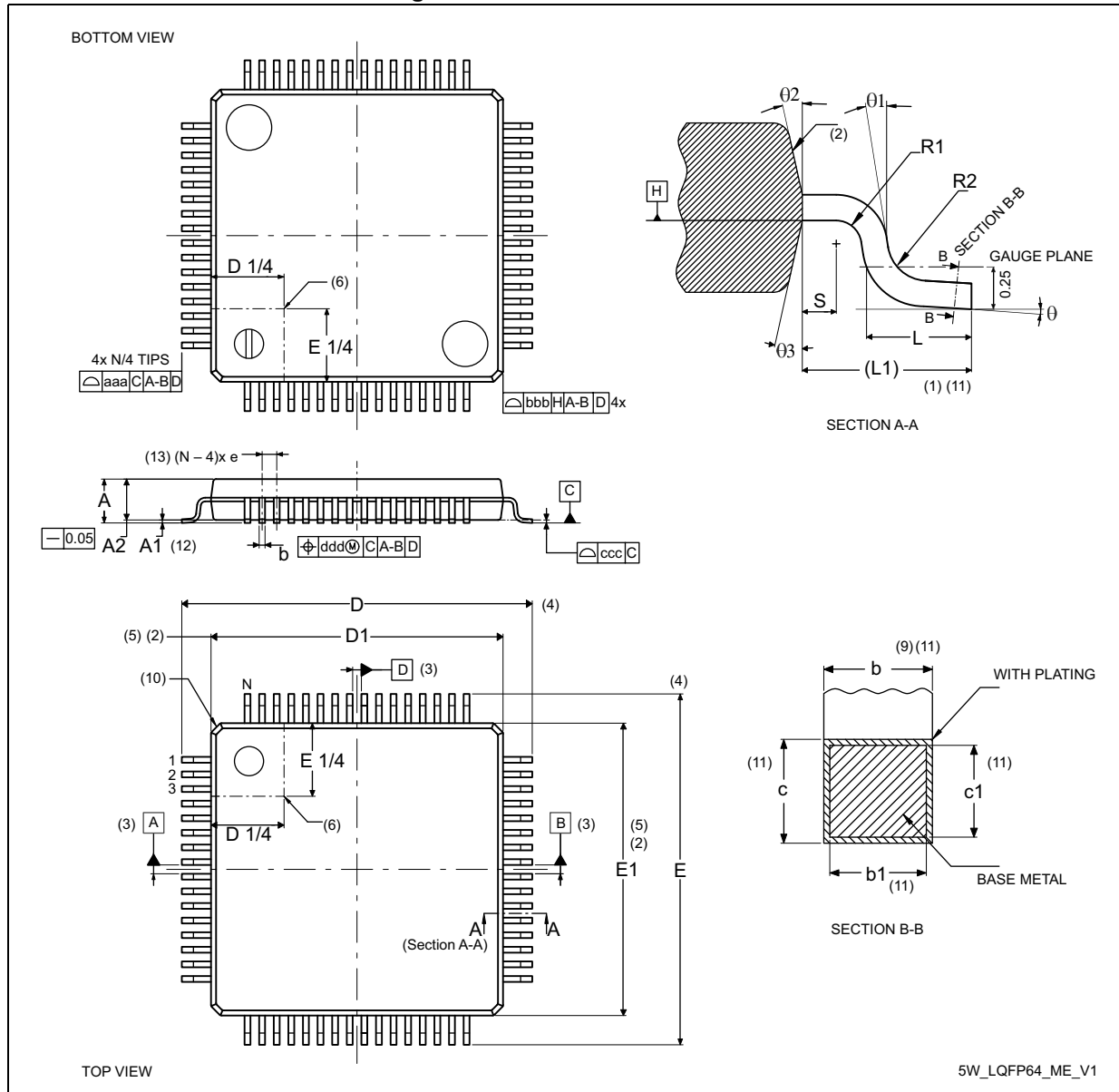


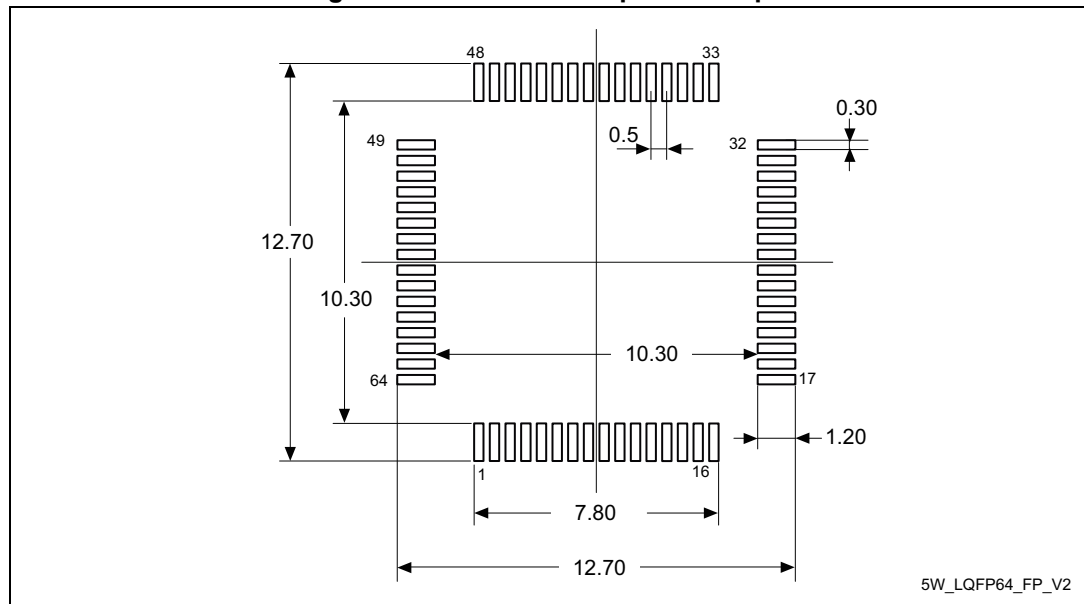
Table 129. LQFP64 - Mechanical data

Symbol	millimeters			inches ⁽¹⁴⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1 ⁽¹²⁾	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b ⁽⁹⁾⁽¹¹⁾	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1 ⁽¹¹⁾	0.17	0.20	0.23	0.0067	0.0079	0.0091
c ⁽¹¹⁾	0.09	-	0.20	0.0035	-	0.0079
c1 ⁽¹¹⁾	0.09	-	0.16	0.0035	-	0.0063
D ⁽⁴⁾	12.00 BSC			0.4724 BSC		
D1 ⁽²⁾⁽⁵⁾	10.00 BSC			0.3937 BSC		
E ⁽⁴⁾	12.00 BSC			0.4724 BSC		
E1 ⁽²⁾⁽⁵⁾	10.00 BSC			0.3937 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N ⁽¹³⁾	64					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa ⁽¹⁾	0.20			0.0079		
bbb ⁽¹⁾	0.20			0.0079		
ccc ⁽¹⁾	0.08			0.0031		
ddd ⁽¹⁾	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. "N" is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 80. LQFP64 - Footprint example

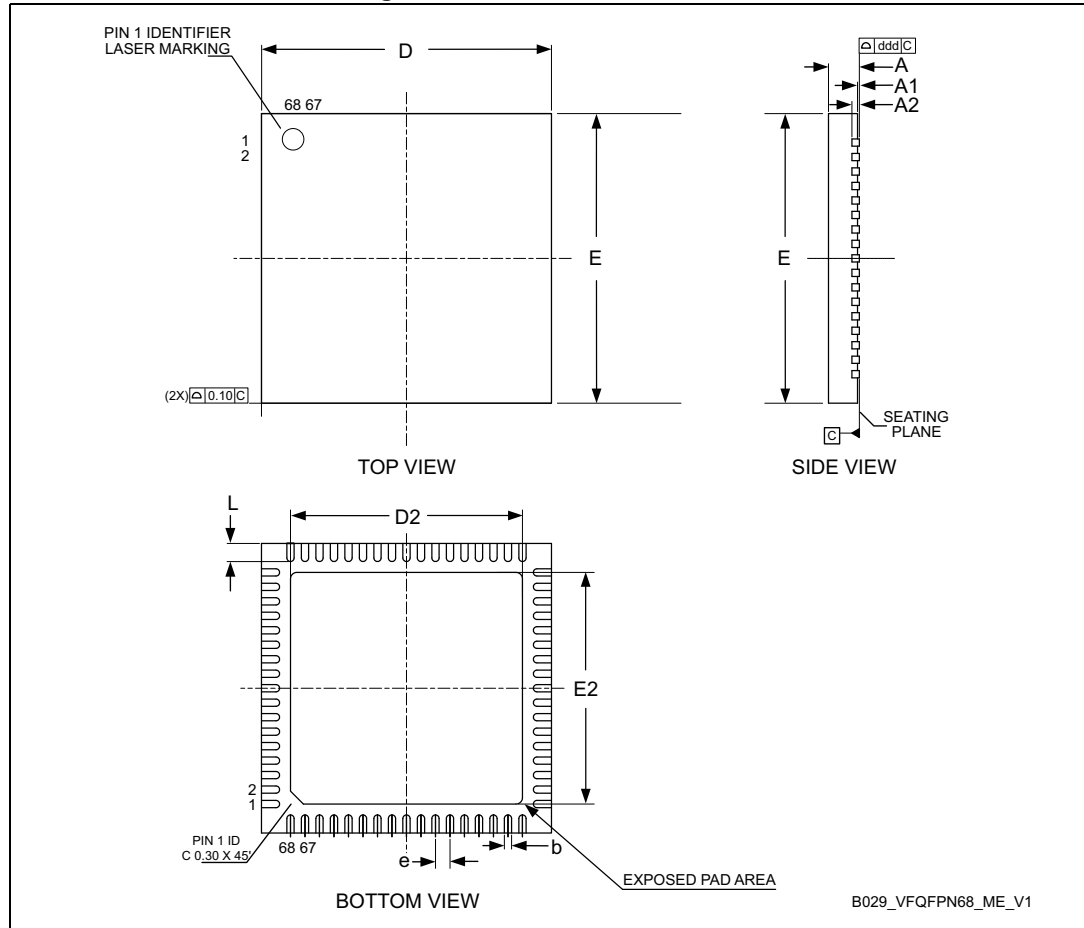


1. Dimensions are expressed in millimeters.

6.3 VFQFPN68 package information (B029)

This VFQFPN is a 68 pins, 8 x 8 mm, 0.4 mm pitch, very thin fine pitch quad flat package.

Figure 81. VFQFPN68 - Outline



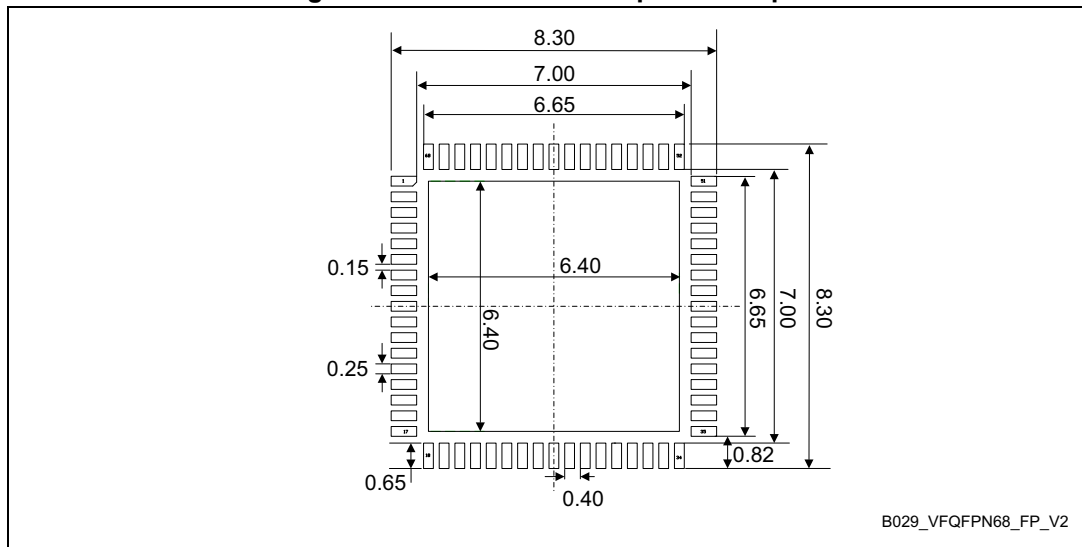
1. VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Packages No lead. Sawed version. Very thin profile: $0.80 < A \leq 1.00\text{mm}$.
2. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature is optional.

Table 130. VFQFPN68 - Mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05	0	0.0008	0.0020
A3	-	0.20	-	-	0.0008	-
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
D	7.85	8.00	8.15	0.3091	0.3150	0.3209
D2	6.30	6.40	6.50	0.2480	0.2520	0.2559
E	7.85	8.00	8.15	0.3091	0.3150	0.3209
E2	6.30	6.40	6.50	0.2480	0.2520	0.2559
e	-	0.40	-	-	0.0157	-
L	0.40	0.50	0.60	0.0157	0.0197	0.0236
ddd	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. VFQFPN68 - Footprint example

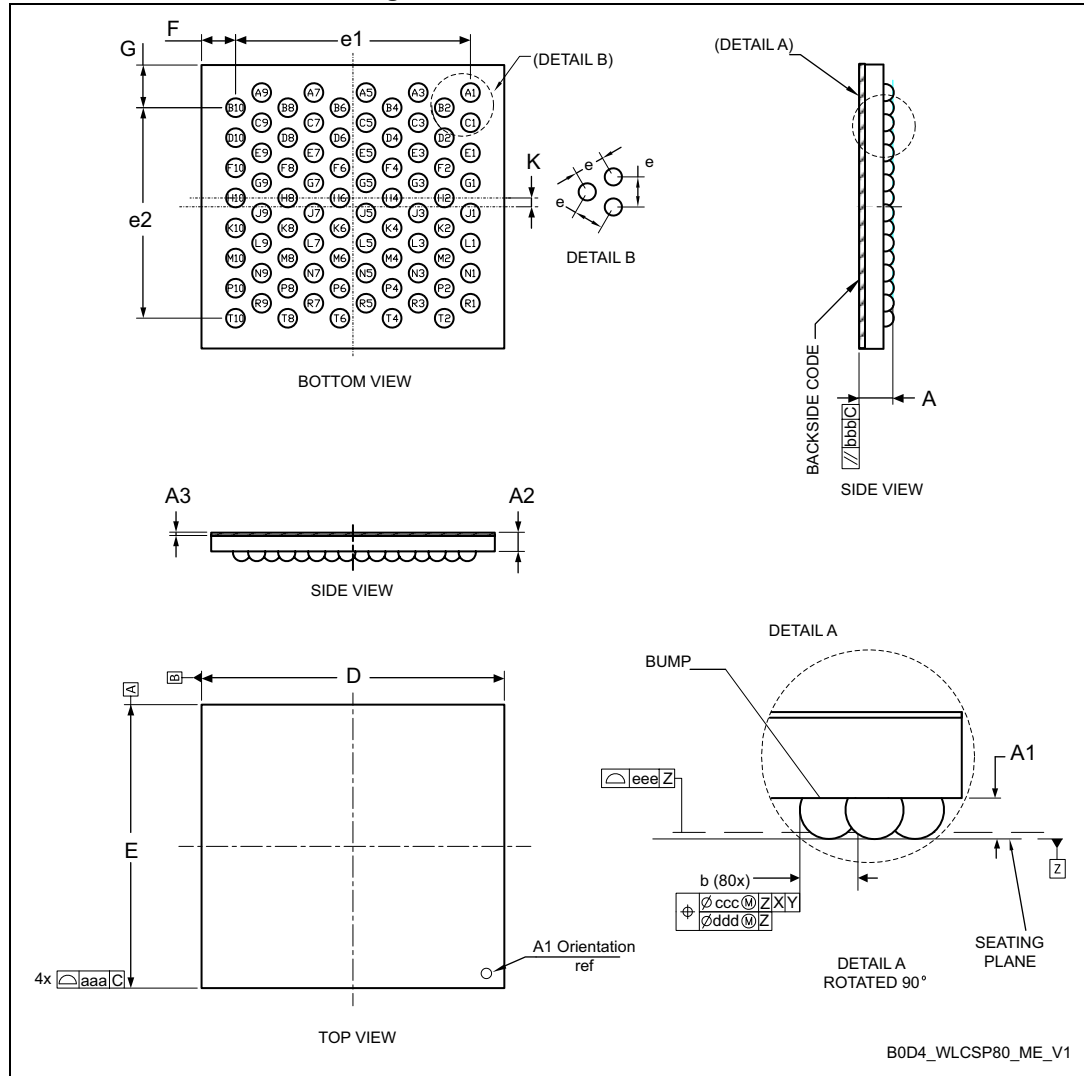


1. Dimensions are expressed in millimeters.

6.4 WLCSP80 package information (B0D4)

This WLCSP is a 80 ball, 3.50 x 3.27 mm, 0.35 mm pitch, wafer level chip scale package.

Figure 83. WLCSP80 - Outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.

Table 131. WLCSP80 - Mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A ⁽²⁾	-	-	0.58	-	-	0.228
A1	-	0.17	-	-	0.0067	-
A2	-	0.38	-	-	0.0150	-
A3 ⁽³⁾	-	0.025	-	-	0.0098	-
b	0.22	0.24	0.27	0.0087	0.0094	0.0106
D	3.47	3.50	3.52	0.1366	0.1378	0.1386
E	3.25	3.27	3.30	0.1279	0.1287	0.1299
e	-	0.35	-	-	0.138	-
e1	-	2.73	-	-	0.1075	-
e2	-	2.45	-	-	0.0964	-
F ⁽⁴⁾	-	0.384	-	-	0.0151	-
G ⁽⁴⁾	-	0.484	-	-	0.0190	-
H	-	0.1025	-	-	0.0040	-
aaa	-	-	0.10	-	-	0.0039
bbb	-	-	0.10	-	-	0.0039
ccc ⁽⁵⁾	-	-	0.10	-	-	0.0039
ddd ⁽⁶⁾	-	-	0.05	-	-	0.0020
eee	-	-	0.05	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Back side coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability.
4. Calculated dimensions are rounded to the 3rd decimal place
5. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.
6. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone ddd perpendicular to datum Z and located on true position as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone. Each tolerance zone ddd in the array is contained entirely in the respective zone ccc above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 84. WLCSP80 - Footprint example

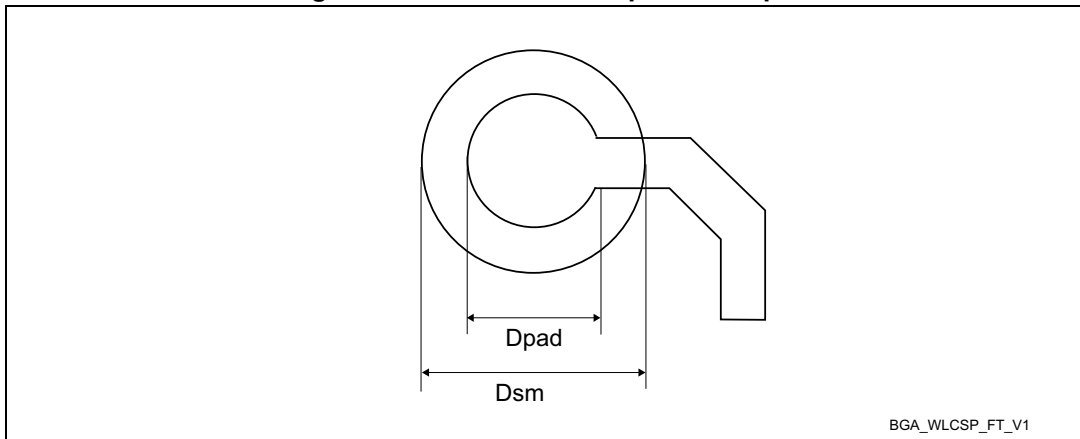


Table 132. WLCSP80 - Example of PCB design rules

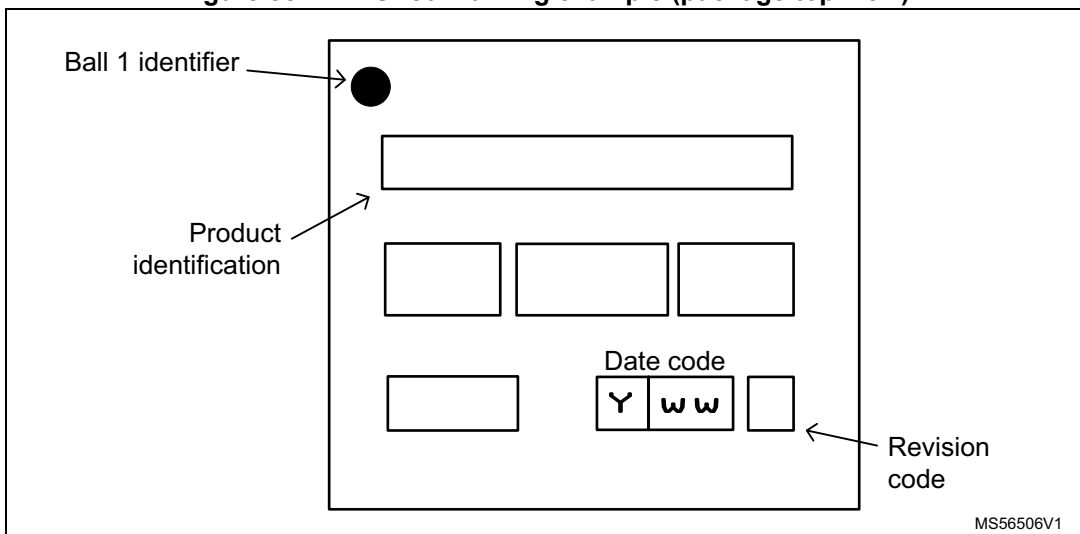
Dimension	Values
Pitch	0.35 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.235 mm
Stencil thickness	0.080 mm

Example of device marking for WLCSP80

The following figure gives an example of the locations and orientation of the marking areas versus ball A1, and allows engineering samples to be identified.

With the device text markings oriented as in the figure, ball A1 is always located at top left.

Figure 85. WLCSP80 marking example (package top view)



6.5 LQFP100 package information (1L)

This LQFP is 100 lead, 14 x 14 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 86. LQFP100 - Outline⁽¹⁵⁾

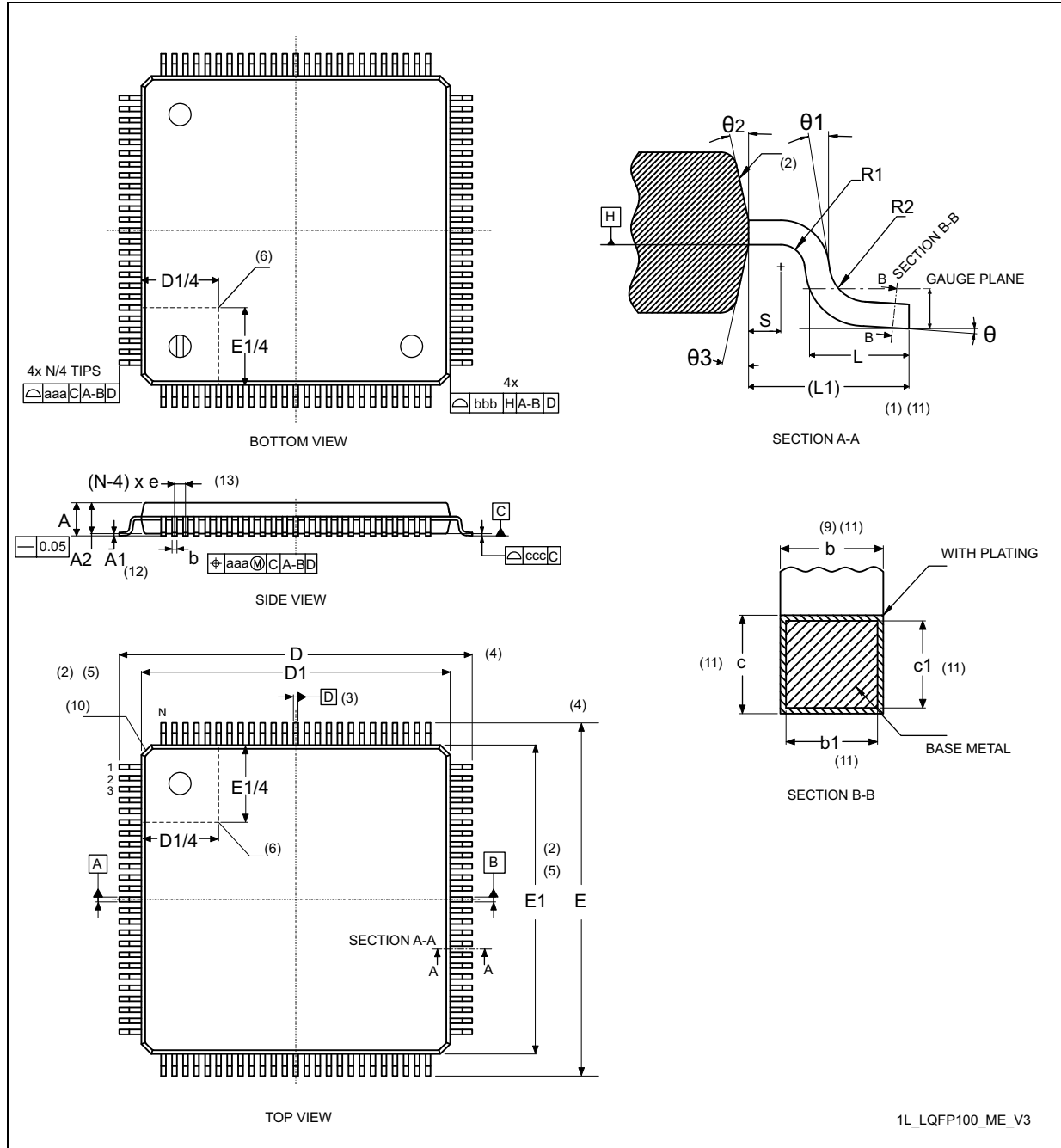


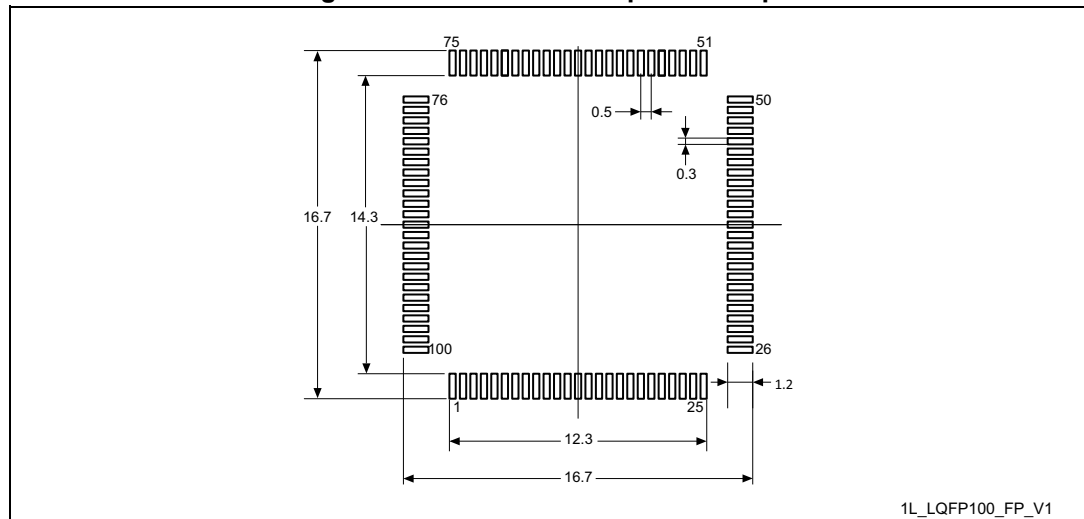
Table 133. LQFP100 - Mechanical data

Symbol	millimeters			inches ⁽¹⁴⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	1.50	1.60	-	0.0590	0.0630
A1 ⁽¹²⁾	0.05	-	0.15	0.0019	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b ⁽⁹⁾⁽¹¹⁾	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1 ⁽¹¹⁾	0.17	0.20	0.23	0.0067	0.0079	0.0090
c ⁽¹¹⁾	0.09	-	0.20	0.0035	-	0.0079
c1 ⁽¹¹⁾	0.09	-	0.16	0.0035	-	0.0063
D ⁽⁴⁾	16.00 BSC			0.6299 BSC		
D1 ⁽²⁾⁽⁵⁾	14.00 BSC			0.5512 BSC		
E ⁽⁴⁾	16.00 BSC			0.6299 BSC		
E1 ⁽²⁾⁽⁵⁾	14.00 BSC			0.5512 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.177	0.0236	0.0295
L1 ⁽¹⁾⁽¹¹⁾	1.00			-	0.0394	-
N ⁽¹³⁾	100					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa ⁽¹⁾	0.20			0.0079		
bbb ⁽¹⁾	0.20			0.0079		
ccc ⁽¹⁾	0.08			0.0031		
ddd ⁽¹⁾	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. "N" is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 87. LQFP100 - Footprint example



1. Dimensions are expressed in millimeters.

6.6 LQFP144 package information (1A)

This LQFP is a 144-pin, 20 x 20 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 88. LQFP144 - Outline⁽¹⁵⁾

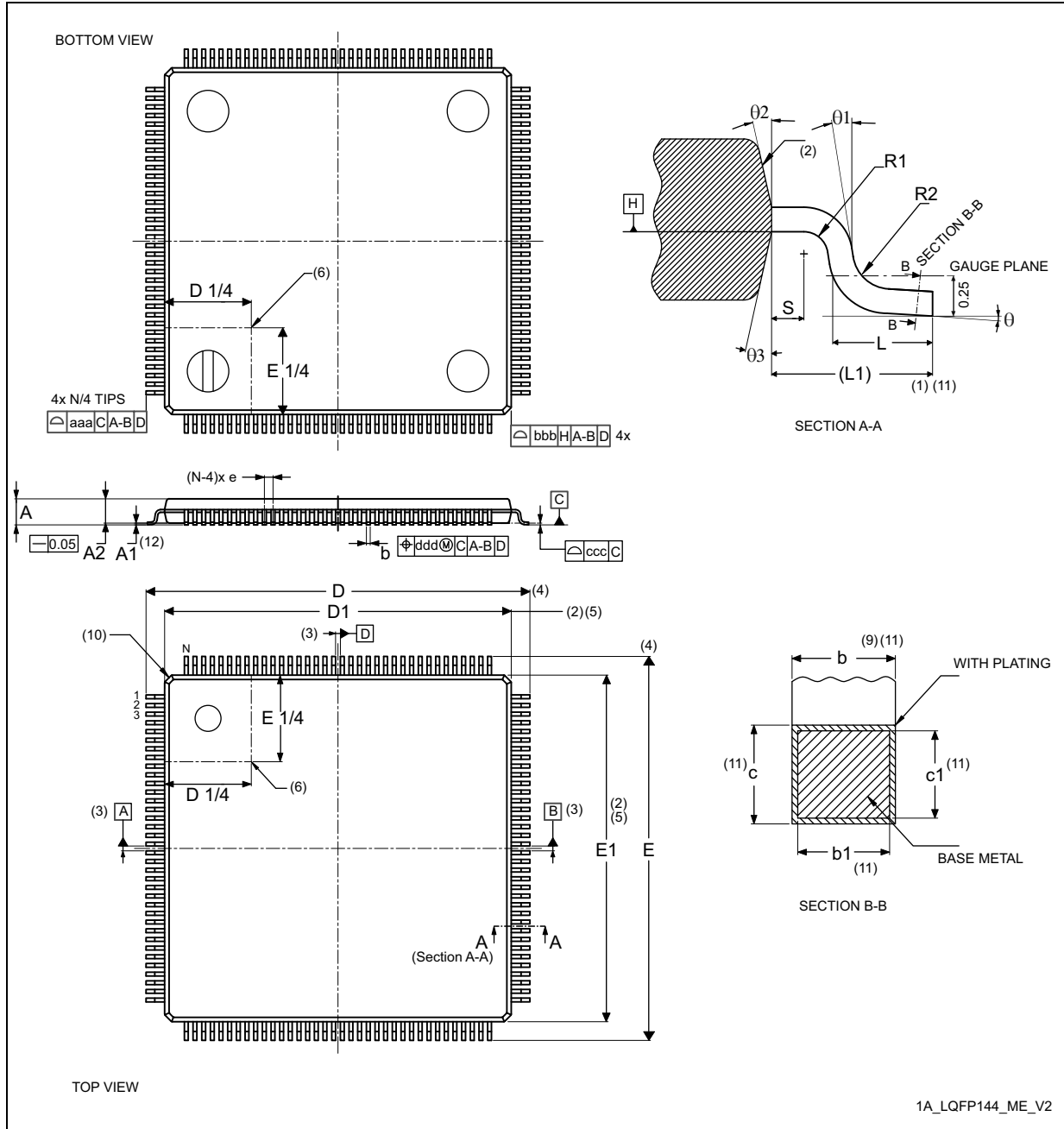


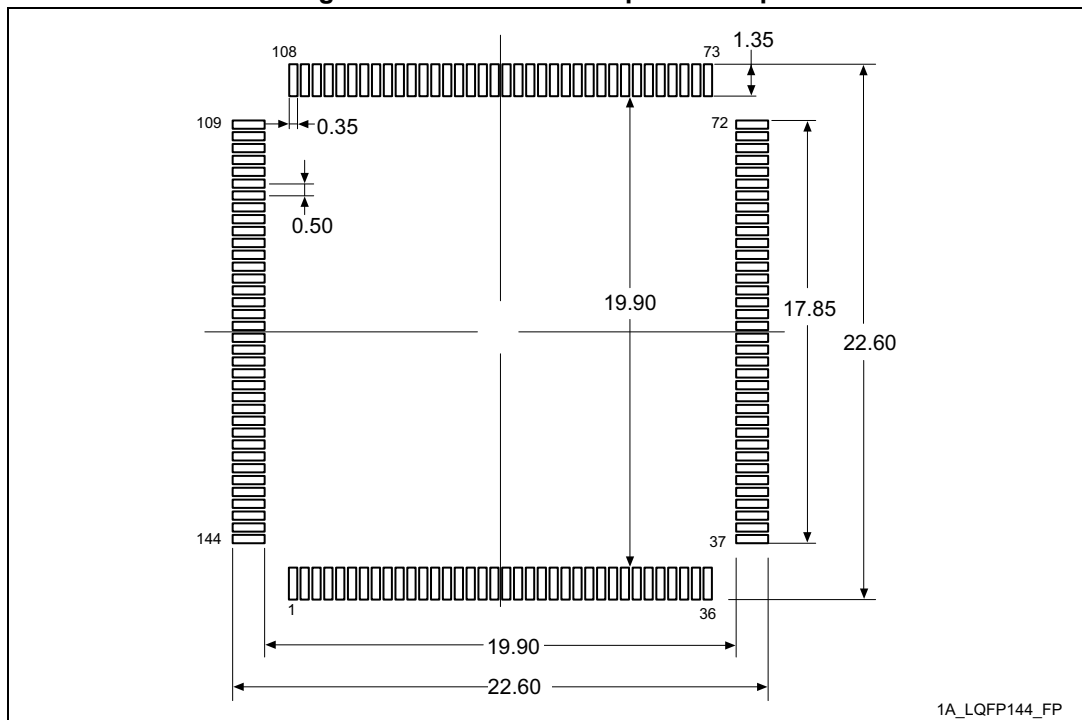
Table 134. LQFP144 - Mechanical data

Symbol	millimeters			inches ⁽¹⁴⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1 ⁽¹²⁾	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b ⁽⁹⁾⁽¹¹⁾	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1 ⁽¹¹⁾	0.17	0.20	0.23	0.0067	0.0079	0.0090
c ⁽¹¹⁾	0.09	-	0.20	0.0035	-	0.0079
c1 ⁽¹¹⁾	0.09	-	0.16	0.0035	-	0.0063
D ⁽⁴⁾	22.00 BSC			0.8661 BSC		
D1 ⁽²⁾⁽⁵⁾	20.00 BSC			0.7874 BSC		
E ⁽⁴⁾	22.00 BSC			0.8661 BSC		
E1 ⁽²⁾⁽⁵⁾	20.00 BSC			0.7874 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N ⁽¹³⁾	144					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. "N" is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 89. LQFP144 - Footprint example

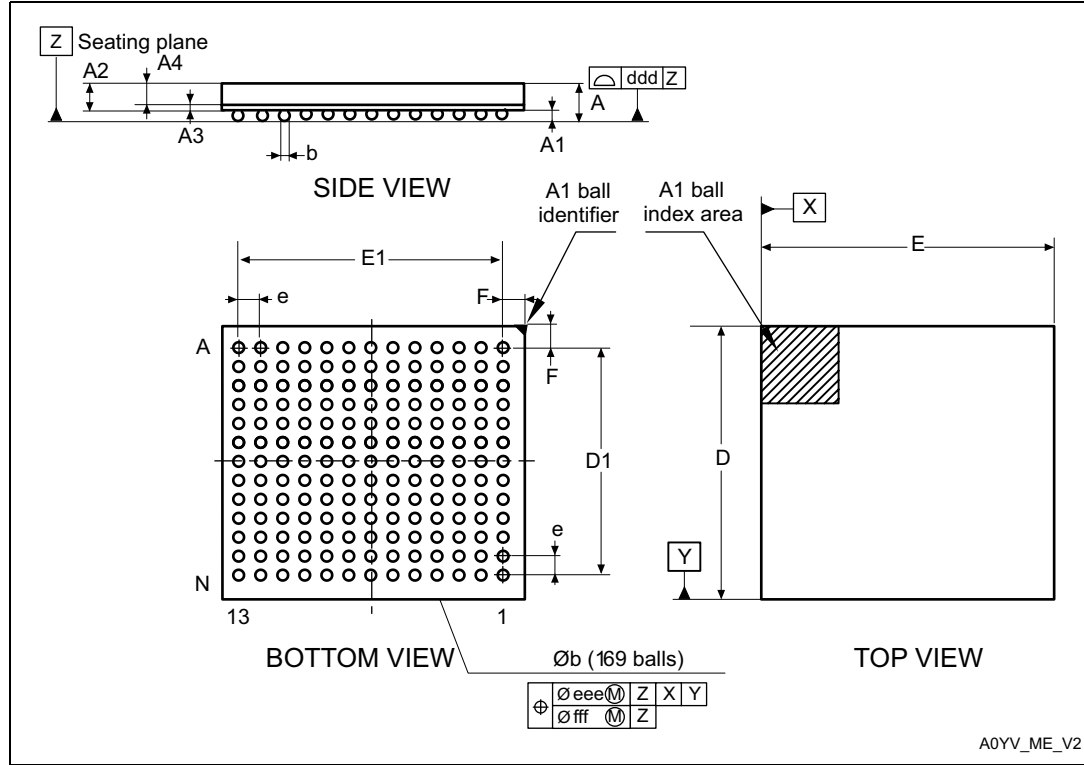


1. Dimensions are expressed in millimeters.

6.7 UFBGA169 package information (A0YV)

This UFBGA is a 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Figure 90. UFBGA169 - Outline



1. Drawing is not to scale.

Table 135. UFBGA169 - Mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-
F	0.450	0.500	0.550	0.0177	0.0197	0.0217

Table 135. UFBGA169 - Mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 91. UFBGA169 - Footprint example

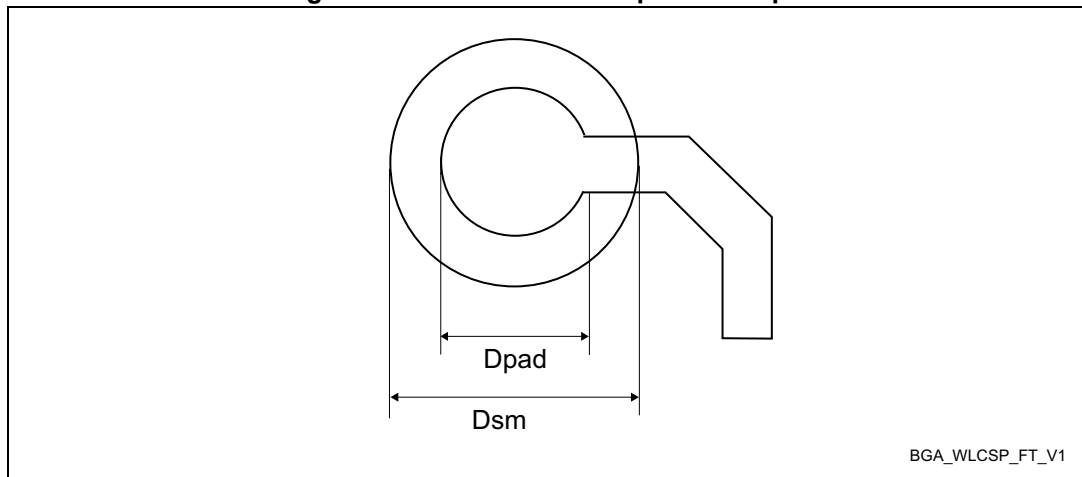


Table 136. UFBGA169 - Example of PCB design rules (0.5 mm pitch BGA)

Dimension	Values
Pitch	0.5 mm
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non-solder mask defined (NSMD) pads are recommended.

Note: 4 to 6 mils solder paste screen printing process.

6.8 LQFP176 package information (1T)

This LQFP is a 176-pin, 24 x 24 mm, 0.5 mm pitch, low profile quad flat package.

Note: See list of notes in the notes section.

Figure 92. LQFP176 - Outline⁽¹⁵⁾

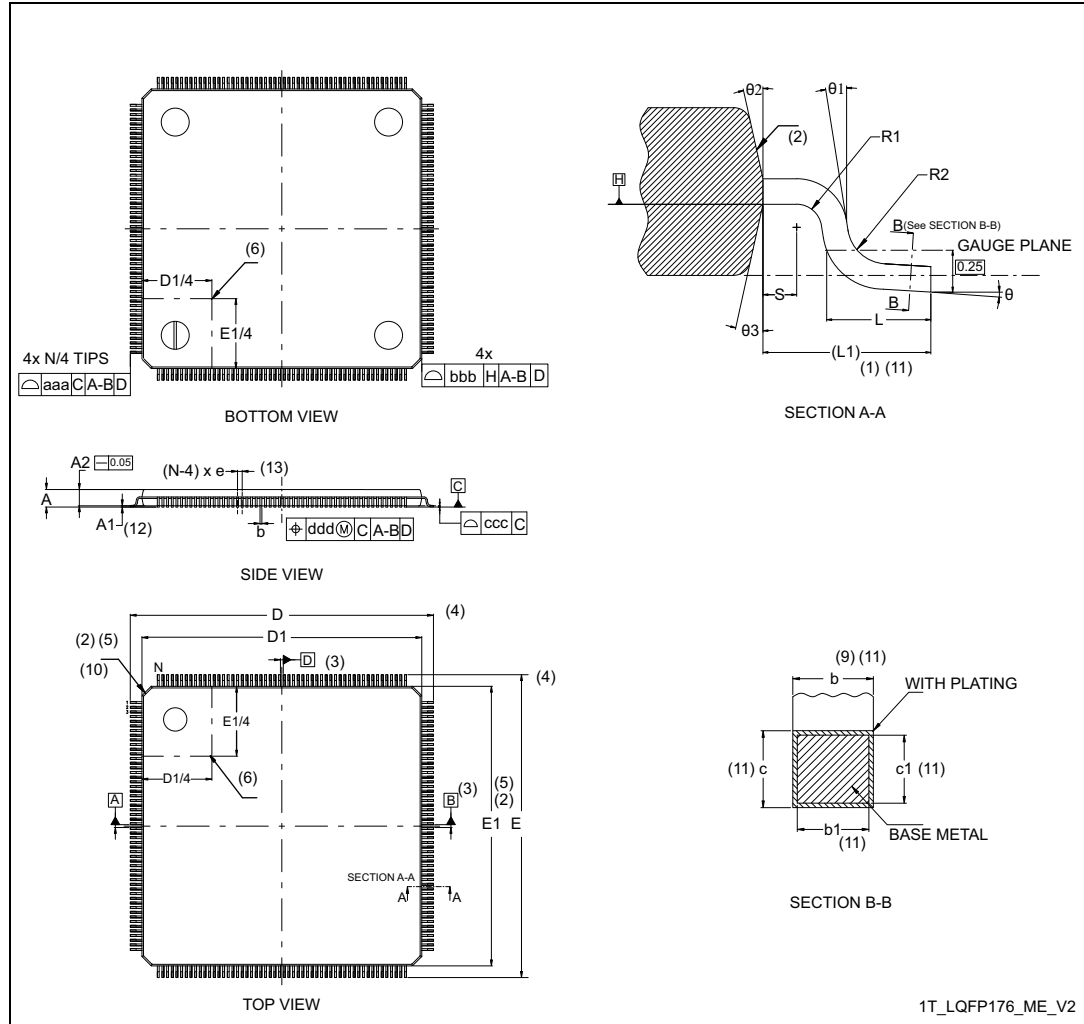


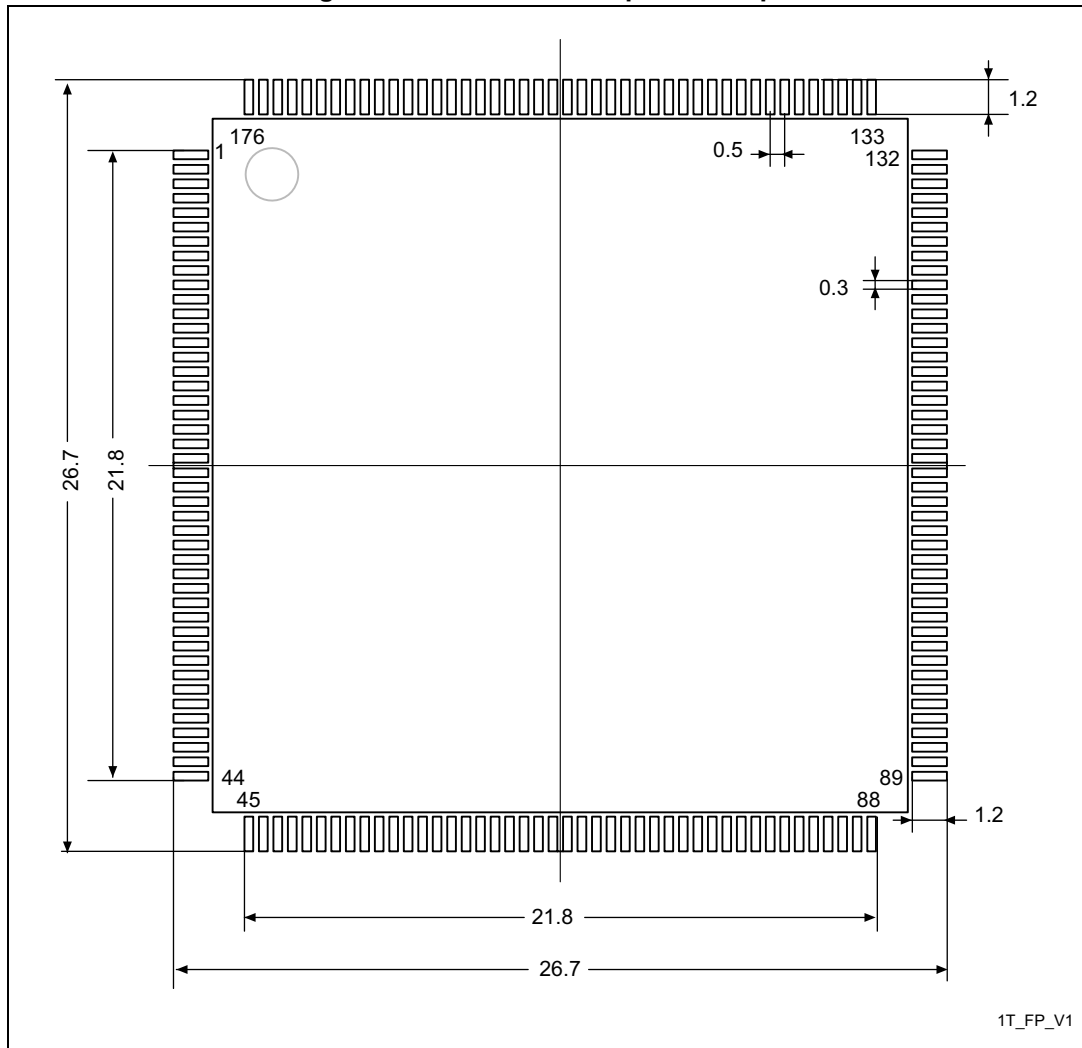
Table 137. LQFP176 - Mechanical data

Symbol	millimeters			inches ⁽¹⁴⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1 ⁽¹²⁾	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b ⁽⁹⁾⁽¹¹⁾	0.170	0.220	0.270	0.0067	0.0087	0.0106
b1 ⁽¹¹⁾	0.170	0.200	0.230	0.0067	0.0079	0.0091
c ⁽¹¹⁾	0.090	-	0.200	0.0035	-	0.0079
c1 ⁽¹¹⁾	0.090	-	0.160	0.0035	-	0.063
D ⁽⁴⁾	26.000			1.0236		
D1 ⁽²⁾⁽⁵⁾	24.000			0.9449		
E ⁽⁴⁾	26.000			0.0197		
E1 ⁽²⁾⁽⁵⁾	24.000			0.9449		
e	0.500			0.1970		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1 ⁽¹⁾⁽¹¹⁾	1			0.0394 REF		
N ⁽¹³⁾	176					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.080	-	-	0.0031	-	-
R2	0.080	-	0.200	0.0031	-	0.0079
S	0.200	-	-	0.0079	-	-
aaa ⁽¹⁾	0.200			0.0079		
bbb ⁽¹⁾	0.200			0.0079		
ccc ⁽¹⁾	0.080			0.0031		
ddd ⁽¹⁾	0.080			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. "N" is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 93. LQFP176 - Footprint example

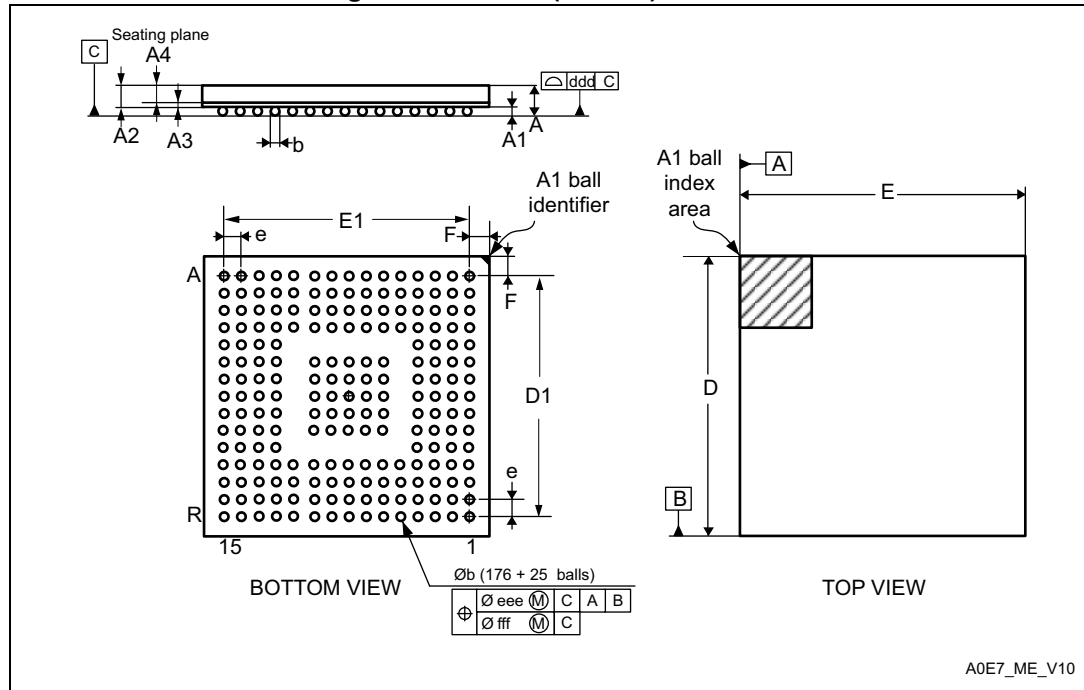


1. Dimensions are expressed in millimeters.

6.9 UFBGA(176+25) package information (A0E7)

This UFBGA is a 176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package.

Figure 94. UFBGA(176+25) - Outline



1. Drawing is not to scale.

Table 138. UFBGA(176+25) - Mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
F	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 138. UFBGA(176+25) - Mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 95. UFBGA(176+25) - Footprint example

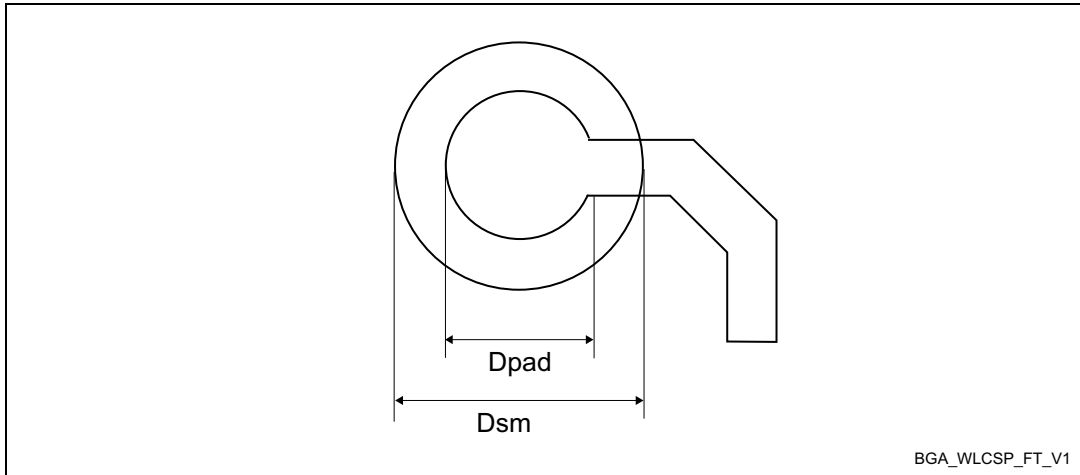


Table 139. UFBGA(176+25) - Example of PCB design rules (0.65 mm pitch BGA)

Dimension	Values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

6.10 Package thermal characteristics

The maximum chip-junction temperature, T_{Jmax} in degrees Celsius, can be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins:

$$P_{I/Omax} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 140. Package thermal characteristics

Symbol	Definition	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	LQFP64 (10 x 10 mm)	48.1	°C/W
		VFQFPN68 (8 x 8 mm)	24.2	
		WLCSP80 (3.50 x 3.27 mm)	47.3	
		LQFP100 (14 x 14 mm)	35.9	
		LQFP144 (20 x 20 mm)	37.5	
		LQFP176 (24 x 24 mm)	38.3	
		UFBGA169 (7 x 7 mm)	40.6	
		UFBGA176 (10 x 10 mm)	39.1	
Θ_{JB}	Thermal resistance junction-board	LQFP64 (10 x 10 mm)	24.1	°C/W
		VFQFPN68 (8 x 8 mm)	9.4	
		WLCSP80 (3.50 x 3.27 mm)	23.0	
		LQFP100 (14 x 14 mm)	21.9	
		LQFP144 (20 x 20 mm)	26.3	
		LQFP176 (24 x 24 mm)	28.3	
		UFBGA169 (7 x 7 mm)	26.4	
		UFBGA176 (10 x 10 mm)	27.0	

Table 140. Package thermal characteristics (continued)

Symbol	Definition	Parameter	Value	Unit
Θ_{JC}	Thermal resistance junction-case	LQFP64 (10 x 10 mm)	10.3	°C/W
		VFQFPN68 (8 x 8 mm)	10.8	
		WLCSP80 (3.50 x 3.27 mm)	2.3	
		LQFP100 (14 x 14 mm)	8.5	
		LQFP144 (20 x 20 mm)	8.6	
		LQFP176 (24 x 24 mm)	9.1	
		UFBGA169 (7 x 7 mm)	11.2	
		UFBGA176 (10 x 10 mm)	10.9	

6.10.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.
- For information on thermal management, refer to AN5036 “*Guidelines for thermal management on STM32 applications*”, available from www.st.com.

7 Ordering information

Example:	STM32	H	563	V	I	T	6	Q	TR
Device family									
STM32 = Arm based 32-bit microcontroller									
Product type									
H = high performance									
Device subfamily									
562 = STM32H562xx devices without Ethernet 563 = STM32H563xx devices									
Pin count									
R = 64 pins / 68 pins M = 80 pins V = 100 pins Z = 144 pins A = 169 balls I = 176 pins									
Flash memory size									
G = 1 Mbyte I = 2 Mbytes									
Package									
V = VFQFPN T = LQFP I = UFBGA (7 x 7 mm) K = UFBGA (10 x 10) Y = WLCSP									
Temperature range									
6 = Temperature range, -40 to 85 °C (130 °C junction) 3 = Industrial temperature range, -40 to 125 °C (130 °C junction)									
Dedicated pinout									
Q = Dedicated pinout supporting SMPS step-down converter									
Packing									
TR = tape and reel xxx = programmed parts									

For a list of available options (such as speed or package) or for further information on any aspect of this device, contact the nearest ST sales office.

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9 Revision history

Table 141. Document revision history

Date	Revision	Changes
06-Mar-2023	1	Initial release.
20-Oct-2023	2	<p>Updated Features and Section 3.10.1: Power supply schemes. Updated Table 2: STM32H56xxx features and peripheral counts, Table 18: Current characteristics, Table 20: General operating conditions, tables 30 to 32, tables 34 to 35, Table 58: I/O static characteristics, and Table 64: Output timing characteristics (HSLV ON). Updated Figure 7: WLCSP80 SMPS ballout, Figure 41: NAND controller waveforms for read access, Figure 42: NAND controller waveforms for write access, Figure 63: SPI timing diagram - Master mode, Figure 65: SPI timing diagram - Slave mode and CPHA = 1, Figure 69: SAI master timing waveforms, and Figure 70: SAI slave timing waveforms. Added Section 3.32: Public key accelerator (PKA), Section 6.1: Device marking, and Example of device marking for WLCSP80. Minor text edits across the whole document.</p>
28-May-2024	3	<p>Updated Figure 1: STM32H562xx and STM32H563xx block diagram, Figure 6: VFQFPN68 pinout, Figure 17: UFBGA176+25 SMPS ballout, Figure 31: VIL/VIH for all I/Os except BOOT0, and Figure 63: SPI timing diagram - Master mode. Updated Table 14: STM32H562xx and STM32H563xx pin/ball definition, Table 15: Alternate function AF0 to AF7, Table 21: Maximum allowed clock frequencies, Table 23: Characteristics of SMPS step-down converter external components, Table 30: Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 1-way, Table 45: HSI oscillator characteristics, tables 53 to 55, Table 122: Dynamic characteristics: SD/MMC, VDD = 2.7 to 3.6 V, and Table 123: Dynamic characteristics: eMMC, VDD = 1.71 to 1.9 V. Updated Section 3.24.1: Analog temperature sensor. Added Section 3.25: Digital temperature sensor (DTS), Section 5.3.14: I/O current injection characteristics, and USB full speed (FS) characteristics. Added Table 60: Output voltage characteristics for FT_c I/Os and Table 67: Output timing characteristics for FT_c I/Os (PB13/PB14). Added Figure 36: Asynchronous multiplexed PSRAM/NOR write waveforms. Minor text edits across the whole document.</p>

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