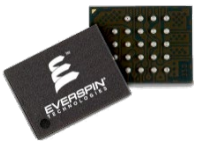
THE DATASHEET OF

EM016LXQADG13IS1T

EXpanded Serial Peripheral Interface (xSPI) Industrial STT-MRAM Persistent Memory

1.8V, 200MHz Octal SPI interface (STR & DTR) with SPI, DSPI and QSPI



Features

- Expanded SPI bus interface supporting
  - Octal, Quad, Dual and Single SPI protocol
- Up to 200MHz single and double transfer rate (STR/DTR) for Octal SPI
- Up to 133MHz, SPI, DSPI, QSPI
- Data endurance: Unlimited read, write and erase operations for supported life of product
- Data retention: 10 Years minimum across temperature
- JEDEC compliant: JESD251, JESD251-1
- Byte level writes and reads with no erase required as persistent memory
- Data integrity: No external ECC required.
- Low Power Modes:
  - Standby < 350µA (64Mb)
  - Deep power down 50µA
- SPI compatibility: NVSRAM, FRAM, NOR, Toggle MRAM
- SPI, xSPI Commands for Program/Erase emulated NOR compatible Execute-in-place (XIP)
- Volatile and nonvolatile configuration settings
  - Nonvolatile settings are not reflow protected
- Dedicated 256-byte OTP area outside main memory
  - Readable and user-lockable
  - Permanent lock with WRITE OTP command
  - Not reflow protected
- Erase capability
  - Chip / bulk erase and sector erase
  - Subsector erase 4KB, 32KB granularity
- Voltage
  - 1.65–2.0V (1.8V)
- Density
  EM008LX 8Mb, EM016LX 16Mb,
  EM032LX 32Mb, EM064LX 64Mb
- 400MBps sustained throughput with OSPI at 200MHz , DTR, for reads and writes
- Boot mode configurations
  - Boot in x1, x2, x4, x8
- Software reset and hardware reset pin available
- 3-byte and 4-byte address modes
- Sequential (burst) read and writes
- Electronic signature
  - JEDEC-standard 3-byte signature
- JEDEC standard, RoHS compliant packages:
  - 24-ball BGA, 6mm x 8mm (5 x 5 array)
  - 8-pin DFN, 6mm x 8mm
- Operating temperature range
  - Commercial: From 0°C to +70°C
  - Industrial: From -40°C to +85°C
- Security and write protection
  - 16 configurable hardware write protected regions plus top/bottom select
  - Program/erase protection during power-up CRC command to detect accidental changes to user data

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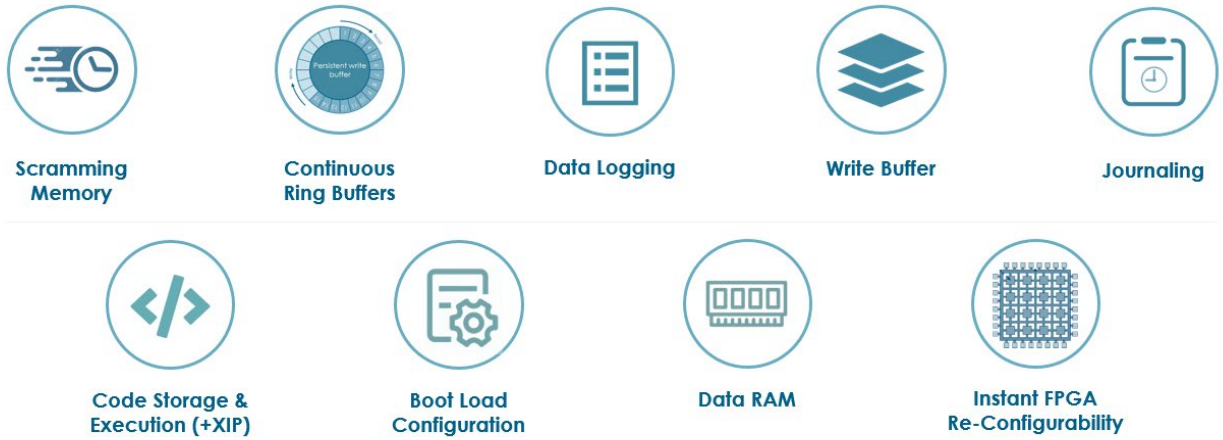
Device Description

The EMxxLX is the industry's first xSPI serial interface persistent memory based on Everspin's unique industrial STT MRAM technology. It is a high-performance, multiple I/O, SPI-compatible MRAM device featuring a high-speed, low pin count SPI compatible bus interface with a clock frequency of up to 200 MHz and a single 1.8V power supply. The EMxxLX delivers up to 400MBps reads and writes via eight I/O signals with a clock frequency of 200MHz.

The **EMxxLX** brings a new era of universal memory applications, replacing products such as SRAM, BBSRAM, NVSRAM and over-provisioned NOR devices and targets applications in Industrial Automation, Datacenter, Engineering Emulation, Automotive and Transportation, and Gaming. It is a great choice for the following application usage models:



Block Diagram

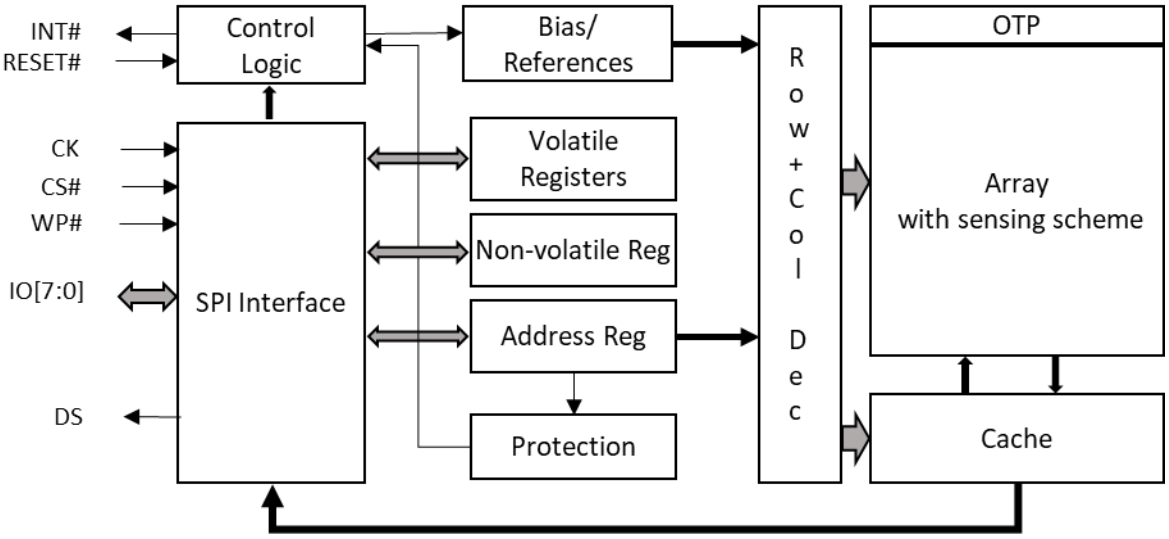
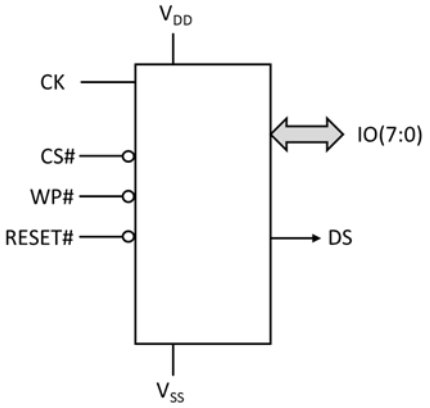
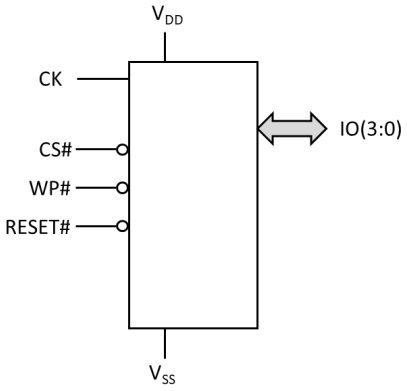


Figure 1

Logic Diagram



OSPI, QSPI, DSPI, xSPI (24-pin BGA)



QSPI, DSPI, SPI (8-pin DFN)

Figure 2

2. Device Pin Assignments

2.1 24 BALL BGA, 5 X 5 (BALLS DOWN)

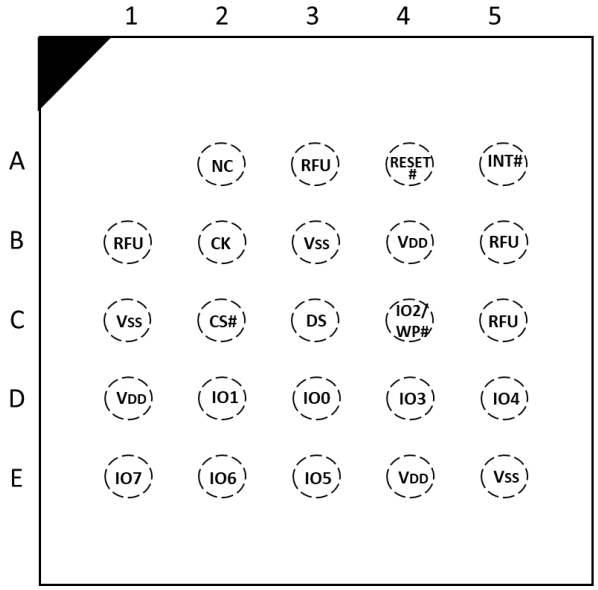


Figure 3a *Octal SPI with Quad, Dual and Single SPI modes*

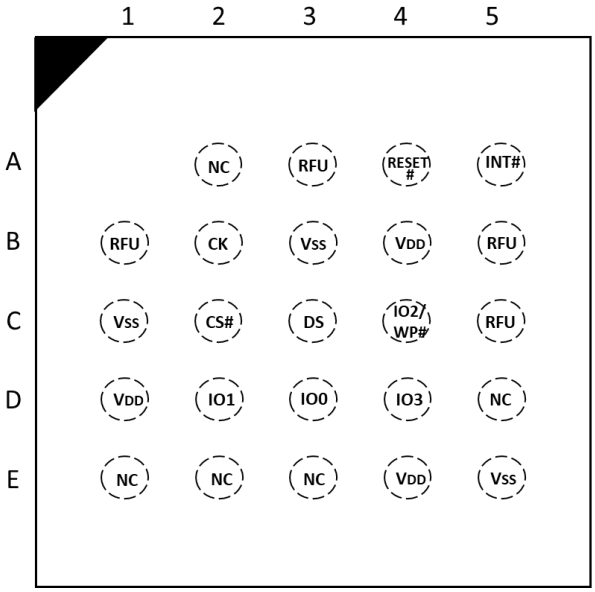


Figure 3b *Quad SPI with Single SPI mode*

2.2 Signal Ball Assignment

Table 1: 24 Ball BGA xSPI, Octal, Quad, Dual and Single SPI Modes

Ball Location	xSPI Signal	Ball Location	xSPI Signal
A1	No Ball	**C4**	IO2 / WP#
A2	NC	**C5**	RFU
A3	RFU	**D1**	V_{DD}
A4	RESET#	**D2**	IO1
A5	INT#	**D3**	IO0
B1	RFU	**D4**	IO3
B2	CK	**D5**	IO4
B3	V_{SS}	**E1**	IO7
B4	V_{DD}	**E2**	IO6
B5	RFU	**E3**	IO5
C1	V_{SS}	**E4**	V_{DD}
C2	CS#	**E5**	V_{SS}
C3	DS		

Notes:

- The signals which show a "/" indicates that the pin or ball is dual function
- For C4 pin, the write protect feature (WP#) can only be used when device is in single SPI mode
- See WP# signal description for detail
- Signals IO4, IO5, IO6, IO7 are NC on Quad SPI part number options

Table 1

2.3 8-Pin DFN Package

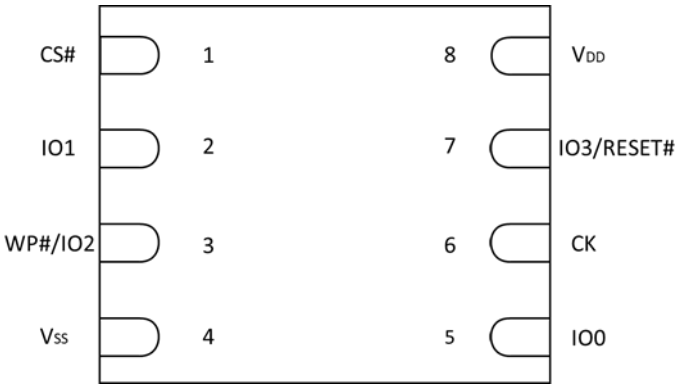


Figure 4

2.4 Signal Pinout in DFN Package

Table 2: Quad, Dual and Single SPI Modes

Pin Location	Signal
1	CS#
2	IO1
3	WP#/IO2
4	VSS
5	IO0
6	CK
7	IO3/RESET#
8	VDD

Note:
1. Pin 7 will be IO3 in Quad SPI mode and RESET# in SPI mode or Dual SPI mode.
2. When using SPI and Dual SPI commands, IO3 must be driven high before CS# goes high to avoid an unintended reset.

Table 2

3. Signal Descriptions

Signal Name	Type	Description
CS#	Input	**Chip Select.** Bus transactions are initiated with a HIGH to LOW transition. Bus transactions are terminated with a LOW to HIGH transition.
CK	Input	**Clock.** Command, Address and Data information is transferred from controller to memory with respect to the rising or falling edge of the CK. The clock is not required to be free running.
IO[7:0]	Input / Output	**Data Input/Output.** Command, Address, and Data information is transferred on these signals during Read and Write transactions.
DS	Output	**Data Strobe.** Strobe signal to capture read data sent by the memory. DS is used by a limited set of xSPI commands.
V_{DD}	Power Supply	**Power.**
V_{SS}	Power Supply	**Ground.**
RESET#	Input	**Hardware Reset.** When LOW, the memory will self-initialize and return the device to the ready state. DS and IO[7:0] are placed into the High-Z state when RESET# is LOW. The RESET# signal should not be allowed to float ; an external pull-up should be used on the PCB for a BGA package. IO3 and RESET# share Pin 7 in the DFN package. See section 18.2 for more detail.
INT#	Output (Open Drain)	**Interrupt**. When LOW, the memory is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output.
WP#	Input	**Write Protect**. Locks the status register in conjunction with the enable/disable bit [7] of the status register. This signal does not have internal pull-ups, it cannot be left floating and must be driven, even if neither of WP#/IO2 function is used.
RFU	Undefined	**Reserved for Future Use.** The package terminal may be connected to a circuit in the device. The function of the terminal is not currently defined or may be used for an optional signal. It is recommended to leave the terminal open and unconnected to external circuits.
NC	No Connection	**No Connection.** The package terminal has no connection to circuits in the device.
DNU	Undefined	**Do Not Use.** The package terminal must remain open and unconnected to external circuits.

Table 3

4. xSPI Signal Protocol

During the time that CS# is active (LOW) the clock signal (CK) is toggled while command information is first transferred on the data (IO) signals. The clock must be active during any period required for information access or transfer to the memory. The clock continues active during the transfer of read data from the memory to the controller or write data from the controller to the memory. When the controller has transferred the desired amount of data, CS# is driven inactive (HIGH). The period during which CS# is active is called a transaction on the bus.

While CS# is inactive, the CK is not required to toggle. CK may stop toggling when CS# is LOW as a means of lowering power consumption or inserting delay within a transaction for flow control. CK must always complete at least one rising edge and one falling edge before stopping at LOW. This requirement for a minimum of one rising and falling edge in turn requires that DTR transfers always occur in two transfer increments, e.g., two bytes (word) for 8-bit wide transfers in 8D mode. STR transfers must occur in one byte increments.

There are up to four phases of activity within each transaction:

- **Command transfer** from controller to memory
- **Command Modifier** (Address) transfer from controller to memory
- **Initial Access Latency** (also used for IO signal direction turn around in a read transaction)
- **Data transfer** (memory to controller in a read transaction or controller to memory in a write transaction)

The command transfer occurs at the beginning of every transaction. The command modifier, initial access latency, and data transfer phases are optional, and their presence depends on the protocol mode or command transferred.
The number of parallel IO signals used during the command modifier and data phases depends on the current protocol mode or command transferred. The initial access latency phase does not use the IO signals for information transfer. The protocol mode options are described by the data rate and the IO width (number of IO signals) used during the command, command modifier (address), and data phases in the following nomenclature (format):

WR-WR-WR where:
The first *WR* is the command bit width and rate
The second *WR* is the command modifier (address) bit width and rate
The third *WR* is the data bit width and rate.

The bit width *W* value may be 1, 2, 4 or 8. R has a value of S for STR, or D for DTR. STR has the same transfer value during the rising and falling edge of a clock cycle. DTR may have different transfer values during the rising and falling edges of each clock.

1S-1S-1S means that the command is 1-bit wide STR, the command modifier is 1-bit wide STR, and the data is one bit wide STR. 8D-8D-8D means that the command, the command modifier, and data transfers are always 8 bits wide DTR. The EMxxLX allows the option to repeat the command opcode which makes an 8D command look like an 8S command, but it is not required to repeat the command opcode.

Example protocol modes supported for the EMxxLX are:
1S-1S-1S; 1S-1D-1D
2S-2S-2S; 2S-2D-2D
4S-4S-4S; 4S-4D-4D
8S-8S-8S; 8D-8D-8D

Note: For full list of opcodes and modes supported by EMxxLX, please refer to section "xSPI Command Opcodes and Modes".

The EMxxLX must be configured during the factory initialization to select the mode in which the device will boot following Power-On-Reset (POR). Supported boot modes are x1, x2, x4 or x8. For example, 8D-8D-8D mode can be made the default

mode if so desired. The controller must determine the default protocol mode of the memory after POR. This may be done through prior knowledge of the system design. The controller may later reconfigure the memory to use other supported modes.

A protocol mode phase using single bit transfer uses IO[0] to transfer information from controller to memory and IO[1] to transfer information from memory to controller. On each IO, information is placed on the IO line in Most Significant bit (MSb) to Least Significant bit (LSb) order within each u. Sequential command modifier bytes are transferred in highest order to lowest order sequence. Sequential data bytes are transferred in lowest address to highest address order.

Table 4: 1S-1S-1S Bit Positions for 4 (and 3) Byte addressing

IO	Command Bits	Address Bits	Latency	Data Byte 0	Data Byte 1
0	7, 6, 5, 4, 3, 2, 1, 0	31 (23), 30 (22), … 1, 0	X …	X …	X …
1	X …	X …	X …	7, 6, 5, 4, 3, 2, 1, 0	7, 6, 5, 4, 3, 2, 1, 0
2	X …	X …	X …	X …	X …
3	X …	X …	X …	X …	X …
4	X …	X …	X …	X …	X …
5	X …	X …	X …	X …	X …
6	X …	X …	X …	X …	X …
7	X …	X …	X …	X …	X …

Table 4

A protocol mode phase using two IO signals uses IO[1:0], four IO signals using IO[3:0] and eight IO signals uses IO[7:0]. The LSb of each byte is placed on IO[0] with each higher order bit on the successively higher numbered IO signals. Sequential command modifier bytes are transferred in highest order to lowest order sequence. Sequential data bytes in STR are transferred in lowest address to highest address order. While in 8D mode, sequential data bytes in DTR are transferred only in byte pairs (words) where the byte order depends on the order in which the bytes are written or programmed in that protocol mode. Sequential data bytes are transferred in lowest address to highest address order. In 8D mode, the starting address must be even.

Table 5: 8D-8D-8D Bit Positions for 4 (and 3) Byte addressing

IO	Command Bits		Address Bits				Latency	Data Word 0		Data Word 1	
0	0	0	24	16	8	0	X …	0	0	0	0
1	1	1	25	17	9	1	X …	1	1	1	1
2	2	2	26	18	10	2	X …	2	2	2	2
3	3	3	27	19	11	3	X …	3	3	3	3
4	4	4	28	20	12	4	X …	4	4	4	4
5	5	5	29	21	13	5	X …	5	5	5	5
6	6	6	30	22	14	6	X …	6	6	6	6
7	7	7	31	23	15	7	X …	7	7	7	7

Table 5

IO signals not in use in a particular phase are undefined and may or may not be driven by the controller or memory, i.e., these signals may be in a high impedance state (floating and indicated by X in the bit position tables).

Note:

- In single and dual bit transfers the IO[7:2] signals may be high impedance, unless they are dual purpose such as WP# or RESET# in the DFN package

- In quad bit transfers the IO[7:4] signals may be high impedance

During the data transfer period of a read memory transaction, the Data Strobe (DS) signal is driven by the memory device and transitions edge aligned with the IO signal data transitions. DS is used as an additional output signal with the same timing characteristics as other data outputs but with the guarantee of transitioning with every data bit transferred. The DS signal transitions can be received and internally phase shifted by the controller to be used as an internal read clock/strobe to capture each data bit transferred. Data Strobe is the return of the clock, CK. It is available in all modes and makes it easier to achieve higher clock frequencies. It is required to achieve the maximum clock frequencies. DS goes low when CS# is driven low by the host controller and is driven until CS# is pulled high. DS stays low while the device is receiving command, address, and data. DS will toggle while the device is transmitting data out.

5. Registers

The EMxxLX supports various status and configuration registers for device status updates and configuration settings. These registers and their access details are discussed in the following sections.

5.1 Status Register

Read Status Register or Write Status Register commands are used to read from or write to the Status Register bits, respectively. When the status register enable/disable bit (bit 7) is set to 1 and WP# is driven LOW, the status register nonvolatile bits become read-only and the Write Status Register operation will not execute. This hardware-protected mode is exited by driving WP# high.

	Table 6: Status Register				
Bit	**Name**	**Settings**	**Description**	**Type**	**Notes**
0	WIP: Write in progress	0 = Ready 1 = Busy	Status bit to determine if a Write Status Register, Write Nonvolatile Configuration Register, Write (Program), CRC, or Erase operation is in progress. This bit is Read Only.	Volatile	2
1	WEL: Write enable latch	0 = Clear (Default) 1 = Set	The device powers up with the Write enable latch (WEL) cleared to prevent inadvertent Write (Program), or Erase operations. To enable these operations, the Write Enable command must be executed to set this bit. The Write Disable command clears this bit. This bit is Read Only.	Volatile	
2	BP[0]	Refer to Protected Area tables	Defines memory area to be software protected against Write (Program) or Erase operations. When one or more block protect bits are set to 1, a designated memory area is protected. This bit is writable.	Non-volatile	1
3	BP[1]	Refer to Protected Area tables	Defines memory area to be software protected against Write (Program) or Erase operations. When one or more block protect bits are set to 1, a designated memory area is protected. This bit is writable.	Non-volatile	1
4	BP[2]	Refer to Protected Area tables	Defines memory area to be software protected against Write (Program) or Erase operations. When one or more block protect bits are set to 1, a designated memory area is protected. This bit is writable.	Non-volatile	1

5	Top/Bottom	0 = Top (Default) 1 = Bottom	Determines whether the top or bottom of the memory array is where the protected area as defined by the block protect bits starts from. This bit is writable.	Non-volatile	
6	BP[3]	Refer to Protected Area tables	Defines memory area to be software protected against Write (Program) or Erase operations. When one or more block protect bits are set to 1, a designated memory area is protected. This bit is writable.	Non-volatile	1
7	Status Register Write Enable/Disable	0 = Enabled (Default) 1 = Disabled	Used with WP# to enable or disable writing to the status register. This bit is writable.	Non-volatile	
Notes 1. All BP bits must be set to 0 for the Bulk Erase command execution 2. Bit 0 is the inverse of Flag Status Register Bit 7					

Table 6

Status Register Write Enable/Disable Bit [7]

This bit enables write protect for the Status register when set to '1' and the write protect (WP#) pin is driven LOW. In this mode, any instruction that changes the status register content is ignored, effectively locking the state of the device. If SR Bit [7] is set to '0', irrespective of the WP# status (LOW or HIGH), status register write protection remains disabled. Refer to Table 7 for the memory and status register protection options.

Top/ Bottom Protection Bit [5]

This bit defines the operation of the Block Protection bits BP3, BP2, BP1, and BP0. This bit controls the starting point of the memory array (from top or bottom) that gets protected by the Block protection bits.

Block Protection (BP3, BP2, BP1 and BP0) [6,4:2]

These bits define the memory array to be write-protected against memory write commands. When one or more of the BP bits is set to '1', the respective memory address is protected from writes. The Block Protect bits (BP3, BP2, BP1, and BP0) in combination with the T/B bit can be used to protect an address or sector range of the memory array. The size of the range is determined by the value of the BP bits and the upper or lower starting point of the range which is selected by the T/B. Table xx shows EMxxLX protected address range for BP[3:0] bits setting.

Write Enable Latch (WEL) Bit [1]

The WEL bit must be set to 1 to enable write operations to the memory array or registers, as shown in Table xx. This bit is set to '1' only by executing the Write Enable (WREN) command. The WEL bit (SR1[1]) automatically clears to '0' after a Write Disable (04h) command is executed. Write (Program) commands will not reset WEL at the completion of the command allowing for back-to-back writes to memory without loading the WREN command again. The WEL bit is volatile and returns to its default '0' state after POR, software RESET, and hardware RESET (via the RESET# pin when available).

5.2 HARDWARE WRITE PROTECTION

Designated protected blocks as set by SR Bits [6:2], (BP3:0 and TB) are hardware protected with the WP# pin. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven LOW, the status register nonvolatile bits become read-only and the Write Status Register command (01h) operation will not execute. During the extended-SPI protocol with Quad Output Fast Read, Quad IO Fast Read, Octal Output Fast Read, Octal IO Fast Read commands, and with Quad SPI and Octal SPI protocols, this pin function is an input/output with IO2 functionality. Table 7 below explains how the Write Protection is enabled or disabled with the Status register write enable/disable bit 7, the WEL bit 1 and the WP# signal.

Table 7: Write Protection

SR Bit[7]	WP#	WEL Bit [1]	Protected Blocks	Unprotected Blocks	Status Register
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable

1	Low	1	Protected	Writable	Protected
1	High	1	Protected	Writable	Writable

Table 7

Block Protection Settings

Sectors can be protected from Program and Erase operations by setting the TB and BP[3:0] bits corresponding to those sectors as shown in Table 8. If the address of a Write(Program) command is within a protected area, the Write will not execute. Writing will not resume until a new write command is issued with an address in an unprotected area. In other words, a write operation will not skip over a protected area and resume in the next unprotected area. A new Write command is required once an ongoing write aborts.

Table 8: Block Protection- Protected Areas

					Protected 64KB Sectors for given part density (Mb)			
Top/Bottom	**BP3**	**BP2**	**BP1**	**BP0**	**64**	**32**	**16**	**8**
0	0	0	0	0	**None**	**None**	**None**	**None**
0	0	0	0	1	127:127	63:63	31:31	15:15
0	0	0	1	0	127:126	63:62	31:30	15:14
0	0	0	1	1	127:125	63:61	31:29	15:13
0	0	1	0	0	127:124	63:60	31:28	15:12
0	0	1	0	1	127:123	63:59	31:27	15:11
0	0	1	1	0	127:122	63:58	31:26	15:10
0	0	1	1	1	127:121	63:57	31:25	15:9
0	1	0	0	0	127:120	63:56	31:24	15:8
0	1	0	0	1	127:112	63:48	31:16	15:0
0	1	0	1	0	127:96	63:32	31:0	15:0
R0	1	0	1	1	127:64	63:0	31:0	15:0
0	1	1	0	0	127:0	63:0	31:0	15:0
0	1	1	0	1	127:0	63:0	31:0	15:0
0	1	1	1	0	127:0	63:0	31:0	15:0
0	1	1	1	1	127:0	63:0	31:0	15:0
1	**0**	**0**	**0**	**0**	**None**	**None**	**None**	**None**
1	0	0	0	1	0:0	0:0	0:0	0:0
1	0	0	1	0	1:0	1:0	1:0	1:0
1	0	0	1	1	2:0	2:0	2:0	2:0
1	0	1	0	0	3:0	3:0	3:0	3:0
1	0	1	0	1	4:0	4:0	4:0	4:0
1	0	1	1	0	5:0	5:0	5:0	5:0
1	0	1	1	1	6:0	6:0	6:0	6:0
1	1	0	0	0	7:0	7:0	7:0	7:0

1	1	0	0	1	15:0	15:0	15:0	15:0
1	1	0	1	0	31:0	31:0	31:0	15:0
1	1	0	1	1	63:0	63:0	31:0	15:0
1	1	1	0	0	127:0	63:0	31:0	15:0
1	1	1	0	1	127:0	63:0	31:0	15:0
1	1	1	1	0	127:0	63:0	31:0	15:0
1	1	1	1	1	127:0	63:0	31:0	15:0

Table 8

5.3 FLAG STATUS REGISTER

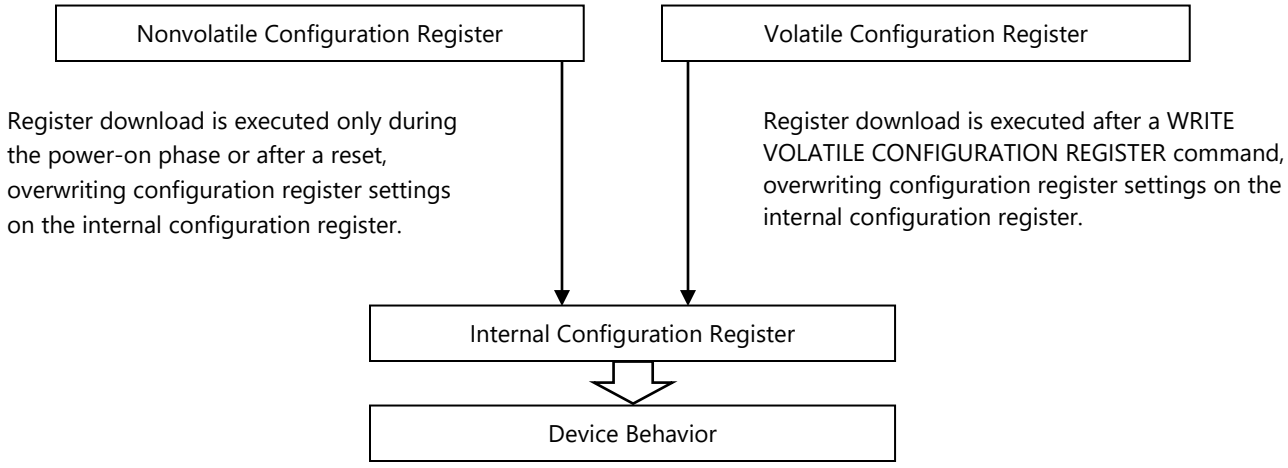
The Read Flag Status Register command is used to read the Flag status register bits. Flag status registers bits are volatile and are reset to zero on power-up. They are set and reset automatically by the internal controller. Error bits must be cleared through the Clear Flag Status Register command. For Soft Reset, Hardware Reset and Reset with signal sequence, bits 1, 3, 4, and 5 are set to "0"; bit 7 is set to "1". In a Reset with signal sequence, bit 0 is set to "0".

Table 9: Flag Status Register				
Bit	**Name**	**Settings**	**Description**	**Type**
0	Addressing	0 = 3-byte addressing 1 = 4-byte addressing	Indicates whether 3-byte or 4-byte address mode is enabled.	Status
1	Protection	0 = Clear 1 = Protection Error	Indicates whether an Erase or Program operation has attempted to modify the protected array sector as configured by Block Protection, or whether a OTP Write operation has attempted to access the locked OTP space.	Error
2	Reserved			
3	CRC	0 = Clear 1 = Failure	Indicates that the Computed CRC did not match the user provided CRC Code.	Error
4	Write (Program)	0 = Clear 1 = Program Error	Indicates whether a Program operation has succeeded or failed. A PROGRAM or OTP Write operation will fail if WREN is not set.	Error
5	Erase	0 = Clear 1 = Erase Error	Indicates whether an Erase operation has succeeded or failed. An Erase operation will fail if WREN is not set.	Error
6	Reserved			
7	Write (Program) or Erase	0 = Busy 1 = Ready	Indicates whether one of the following command cycles is in progress: Write Status Register, Write Nonvolatile Configuration Register, Write (Program), Erase, or CRC Check.	Status

Table 9

5.4 Configuration Registers

The memory configuration is set by an internal configuration register that is not directly accessible to users. The user can change the default configuration at power up by using the WRITE NONVOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power on or after a reset. The user can change the configuration during device operation using the WRITE VOLATILE CONFIGURATION REGISTER command. Information from the volatile configuration registers overwrite the internal configuration register immediately after the WRITE command completes.



5.5 NONVOLATILE CONFIGURATION REGISTER

Nonvolatile Configuration Register 0					
Address[5]	**0x0000**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	I/O Mode	1111_1111 (0xFF) 1101_1111 (0xDF) 1111_1101 (0xFD) 1101_1101 (0xDD) 1111_1011 (0xFB) 1101_1011 (0xDB) 1110_1011 (0xEB) 1100_1011 (0xCB) 1110_0111 (0xE7) 1100_0111 (0xC7) 1011_0111 (0xB7) 1001_0111 (0x97) Others	SPI with DS (default) SPI w/o DS Dual with DS Dual w/o DS Quad with DS Quad w/o DS Quad DTR with DS Quad DTR w/o DS Octal DTR with DS Octal DTR w/o DS Octal with DS Octal w/o DS SPI with DS (same as default)	6
Nonvolatile Configuration Register 1					
Address	**0x0001**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Dummy Cycle Configuration	0000_0000 0000_0001 0000_0010 . . . 0000_1111 0001_0000 . . . 0001_1110 0001_1111 1111_1111 Others	16 Dummy cycles 1 Dummy cycles 2 Dummy cycles ... 15 Dummy cycles 16 Dummy cycles ... 30 Dummy cycles 31 Dummy cycles 16 Dummy cycles 16 Dummy cycles (default)	
Nonvolatile Configuration Register 2					
Address	**0x0002**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Reserved	TBD		
Nonvolatile Configuration Register 3					
Address	**0x0003**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Driver Strength Configuration	1111_1111 1111_1110 1111_1101 1111_1100 Others	50 Ohm (default) 35 Ohm 25 Ohm 18 Ohm 50 Ohm	
Nonvolatile Configuration Register 4					
Address	**0x0004**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:4	RW	TBD	TBD		
3:0	RW	DS Delay	1111 1110 1101 ... 0000	Zero added DS delay (Default) 100pS added DS delay 200pS added DS delay ... 1500pS added DS delay	7
Nonvolatile Configuration Register 5					

Address	0x0005				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Address Mode	1111_1111 1111_1110 Others	3-Byte Address (default) 4-Byte Address 3-Byte Address	
Nonvolatile Configuration Register 6					
Address	**0x0006**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Execute-in-Place (XIP) Configuration	1111_1111 1111_1110 1111_1100 Others	XIP Disabled (default) XIP Enable- Activated if XIP confirmation bit = 0 during FAST READ XIP BOOT- Activated at boot time XIP Disabled	1
Nonvolatile Configuration Register 7					
Address	**0x0007**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Wrap Configuration	1111_1111 1111_1110 1111_1101 1111_1100 Others	Continuous (default) 64-byte wrap 32-byte wrap 16-byte wrap Continuous	2
Nonvolatile Configuration Register 8					
Address	**0x0008**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7	RW	Erase Bit Value	1 = Erase with '1' (default) 0 = Erase with '0'	Determines data state for Erase operations	
6:2	RW	TBD	TBD		
1	RW	RPE	1 = Reset Pin Enabled (default) 0 = Reset Pin Disabled	When the Reset pin is disabled, the RESET # will be ignored. The device may be reset with Soft Reset or JESD Reset. In the DFN package option, the RESET# signal is disabled automatically when the device is configured in Quad SPI mode (Register 0).	
0	RW	Write mode	1 = Persistent Memory Mode enabled (default) 0 = Persistent memory mode disabled	Persistent Memory mode or NOR Flash like mode is selected with this bit.	3
Nonvolatile Configuration Registers 9,10,11,12					
Address	**0x0009, 0x000A, 0x000B, 0x000C**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Non Volatile user scratch register	1111_1111 (default)	Four 8 bit registers available for storing any user data.	4

Table 10

Notes:

1. Only FAST READ (0Bh) supports XIP operation.
2. Wrap length affects READ commands. WRITE wrap length will depend on the mode selected in Register 8.
3. Used to select the mode for writing to the memory
4. These registers may be used for storing user configuration data that will be used for device recovery if necessary.
5. Register addresses may be either 3-byte or 4-byte depending on user selection
6. When, configuring the I/O mode, the unused IO's, if any, will be left floating. For example, if a user intends to use only the Quad SPI mode in a Octal SPI in a BGA package, IO4-7 will be floating or Hi-Z. These balls may be left unconnected on the PCB if the user never intends to activate Octal SPI. If an Octal SPI BGA device is configured in the Dual SPI mode, IO0 and IO1 will be active and the remaining IO's will be floating except for ball C4 which is dual purpose IO2/WP#. A Quad SPI device in a DFN package which is configured as Dual SPI will use IO2 and IO3 as WP# and RESET# respectively. Similarly, if the same device is configured as SPI mode, IO1 is left floating. Octal configurations in Quad SPI only devices are not valid.
7. Register 4 provides the user a means to tune the DS timing to compensate for PCB layout or system timing offsets to better align with valid data output on the IO's. The amount of delay is configurable. Actual delay can vary +/- 30ps per delay setting, the user should confirm the data strobe timing once it is configured. (Refer to App Note EST 3001 for a tuning sequence)

5.6 VOLATILE CONFIGURATION REGISTER

Volatile Configuration Register 0					
Address[4]	**0x0000**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	I/O Mode	1111_1111 (0xFF) 1101_1111 (0xDF) 1111_1101 (0xFD) 1101_1101 (0xDD) 1111_1011 (0xFB) 1101_1011 (0xDB) 1110_1011 (0xEB) 1100_1011 (0xCB) 1110_0111 (0xE7) 1100_0111 (0xC7) 1011_0111 (0xB7) 1001_0111 (0x97) Others	SPI with DS (default) SPI w/o DS Dual with DS Dual w/o DS Quad with DS Quad w/o DS Quad DTR with DS Quad DTR w/o DS Octal DTR with DS Octal DTR w/o DS Octal with DS Octal w/o DS SPI with DS (same as default)	5
Volatile Configuration Register 1					
Address	**0x0001**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Dummy Cycle Configuration	0000_0000 0000_0001 0000_0010 . . . 0000_1111 0001_0000 . . . 0001_1110 0001_1111 Others	16 Dummy cycles 1 Dummy cycles 2 Dummy cycles ... 15 Dummy cycles 16 Dummy cycles ... 30 Dummy cycles 31 Dummy cycles 16 Dummy cycles	
Volatile Configuration Register 2					
Address	**0x0002**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Reserved	TBD		
Volatile Configuration Register 3					
Address	**0x0003**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Driver Strength Configuration	1111_1111 1111_1110 1111_1101 1111_1100 Others	50 Ohm (default) 35 Ohm 25 Ohm 18 Ohm 50 Ohm	
Volatile Configuration Register 4					
Address	**0x0004**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:4	RW	Reserved	TBD		
3:0	RW	DS Delay	1111 1110 1101 ... 0000	Zero added DS delay (Default) 100pS added DS delay 200pS added DS delay ... 1500pS added DS delay	6
Volatile Configuration Register 5					
Address	**0x0005**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**

7:0	RW	Address Mode	1111_1111 1111_1110 Others	3-Byte Address (default) 4-Byte Address 3-Byte Address	
Volatile Configuration Register 6					
Address	**0x0006**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Execute-in-Place (XIP) Configuration	1111_1111 1111_1110 Others	XIP Disabled (default) XIP Enable- Activated if XIP confirmation bit = 0 during FAST READ XIP Disabled	1
Volatile Configuration Register 7					
Address	**0x0007**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Wrap Configuration	1111_1111 1111_1110 1111_1101 1111_1100 Others	Continuous (default) 64-byte wrap 32-byte wrap 16-byte wrap Continuous	2
Volatile Configuration Register 8					
Address	**0x0008**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7	RW	Erase Bit Value	1 = Erase with '1' (default) 0 = Erase with '0'	Determines data state for Erase operations	
6:3	RW	Reserved			
2	RW	OTP Unlock	1 = OTP Lock Enable (default) 0 = OTP Lock Disable"	When OTP Lock is disabled this will override the OTP Lock Byte setting and unlock the OTP array.	
1	RW	RPE	1 = Reset Pin Enabled (default) 0 = Reset Pin Disabled	When the Reset pin is disabled, the RESET # will be ignored. The device may be reset with Soft Reset or JESD Reset. In the DFN package option, the RESET# signal is disabled automatically when the device is configured in Quad SPI mode (Register 0).	
0	RW	Write mode	1 = Persistent Memory Mode enabled (default) 0 = Persistent memory mode disabled	Persistent Memory mode or NOR Flash like mode is selected with this bit.	3

Table 11

Notes:

1. Only FAST READ (0Bh) supports XIP operation.
2. Wrap length affects READ commands. WRITE wrap length will depend on the mode selected in Register 8.
3. Used to select the mode for writing to the memory
4. Register addresses may be either 3-byte or 4-byte depending on user selection
5. When, configuring the I/O mode, the unused IO's, if any, will be left floating. For example, if a user intends to use only the Quad SPI mode in a Octal SPI in a BGA package, IO4-7 will be floating or Hi-Z. These balls may be left unconnected on the PCB is the user never intends to activate Octal SPI. If an Octal SPI BGA device is configured in the Dual SPI mode, IO0 and IO1 will be active and the remaining IO's will be floating except for ball C4 which is dual purpose IO2/WP#. A Quad SPI device in a DFN package which is configured as Dual SPI will leave IO2 and IO3 as WP# and RESET# respectively. Similarly, if the same device is configured as SPI mode, IO1 is left floating. Octal configurations are not valid in Quad SPI only devices.
6. Default settings are power-on reset defaults.
7. Register 4 provides the user a means to tune the DS timing to compensate for PCB layout or system timing offsets to better align with valid data output on the IO's. The amount of delay is configurable. Actual delay can vary +/- 30ps per delay setting, the user should confirm the data strobe timing once it is configured. (Refer to App Note EST 3001 for a tuning sequence)

5.7 Interrupt Mask and Status Registers, INT# Signal Function

The Interrupt Mask and Status registers are used together to provide the status of certain operations or indicate errors in particular operations as shown in the tables below. The mask register provides the option to receive an interrupt signal on the INT# pin. INT# is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. The INT# is available on the 24-ball BGA, ball A5, but is not available on the 8-DFN package. Power on errors, CRC completion and Erase completion are the operations that generate a status bit. CRC completion and Erase completion result in an output signal, INT#, if the Interrupt Mask register bits 1 and 0 respectively are set to 1 (enabled). The INT# signal will go from a high impedance state to a low state. If a Configuration error occurs, INT# will be enabled regardless of the Interrupt Mask settings. The Interrupt registers are accessed with the Read Volatile Configuration Register and Write Volatile Configuration Register commands.

Interrupt Mask					
Address	**0x000F**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:2	RO	Reserved	0		
1	RW	CRC Done	0 = Masked (default) 1 = Interrupt enabled	Enable interrupt on CRC Check Done	
0	RW	Erase Done	0 = Masked (default) 1 = Interrupt enabled	Enable interrupt on Erase Done 0=Masked – no interrupt is generated	

Table 12

Interrupt Status					
Address	**0x0010**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:3	RO	Reserved	0		
2	RW1C	Power On Error	0 = No error 1 = Error	Read, Write 1 to Clear, Power on error	1,2
1	RW1C	CRC Done	0 = Not done (Reset Value) 1 = Done	Read, Write 1 to Clear	
0	RW1C	Erase Done	0 = Not done (Reset Value) 1 = Done	Read, Write 1 to Clear	

Table 13

Note 1. Bit 2 does not get reset with a hardware reset.

Note 2. For detailed information on the device recovery procedure when a Power On Error is detected, please refer to Everspin Application Note EST 3000, *Device Initialization, Power Cycle, System Reset and Recovery for EMxxLX MRAM*.

5.8 DEVICE FACTORY INITIALIZATION MODE

The EMxxLX device must go through an initialization after system or PCB assembly. This is required to ensure that critical internal device settings are in their proper state after solder reflow processing. Write 6B to enter DFIM mode, write something other than 6B to disable DFIM mode using Write register command.

DFIM Register					
Address		**0x001E**			
Bit		**Name**	**Settings**	**Description**	**Notes**
7:0	RW	DFIM	0 = (Reset Value)	**Device Factory Initialize Mode:** Write 0x6B to enter mode (Manufacturer ID) Read back 0x00 DFIM Not Enabled Read back 0x01 DFIM Enabled	Volatile

Table 14

5.9 TUNING DATA PATTERN REGISTER

TDP Register					
Address	**0x0000 - 0x003F**				
Byte Addr	**Op**	**Name**	**Settings**	**Description**	**Notes**
0x00	RW	TDP Byte 0	0xDE	Power On Reset Value	
0x01	RW	TDP Byte 1	0x7B	Power On Reset Value	
0x02	RW	TDP Byte 2	0x7F	Power On Reset Value	
...	RW	...	...	Power On Reset Value	
0x3E	RW	TDP Byte 62	0x0F	Power On Reset Value	
0x3F	RW	TDP Byte 63	0xFF	Power On Reset Value	

Table 15

Note: For full contents and description of TDP, refer to Everspin Application Note EST 3001.

5.10 Supported Clock Frequencies

The table below specifies the maximum frequency supported for a given number of dummy cycles. The number of dummy cycles is set in the Nonvolatile Configuration Register 1 and the Volatile Configuration Register 1. The frequency supported is shown in the respective tables below for STR and DTR modes. The maximum frequency is f_{CK1}=133MHz for SPI, Dual SPI and Quad SPI mode. The maximum frequency is f_{CK2}=200MHz for Octal SPI mode. There is also a frequency limitation in the DFN package, which is offered for a Quad SPI version of the EMxxLX as a result of not having a data strobe signal available. As a result, the maximum frequency in the DFN package is f_{CK} = 133MHz when configured in for STR operation and f_{CK} = 90MHz when configured for DTR operation.

STR – Frequency (MHz)					
Dummy Clock Cycles	**SPI** 1s-1s-1s 1s-1s-2s 1s-1s-4s 1s-1s-8s	**DUAL** 1s-2s-2s 2s-2s-2s	**QUAD** 1s-4s-4s 4s-4s-4s	**Octal** 1s-8s-8s* 8s-8s-8s	**OpCode**
0	66	~	~	~	READ
1	83	~	~	~	READ FAST
2	100	16	16	~	READ FAST
3	116	33	33	33	READ FAST
4	133	50	50	50	READ FAST
5	133	66	66	66	READ FAST
6	133	83	83	83	READ FAST
7	133	100	100	100	READ FAST
8	133	116	116	116	READ FAST
9	133	133	133	133	READ FAST
10	133	133	133	150	READ FAST
11	133	133	133	166	READ FAST
12	133	133	133	183	READ FAST
13	133	133	133	200	READ FAST
14	133	133	133	200	READ FAST
15	133	133	133	200	READ FAST
16	133	133	133	200	READ FAST

* Limited to 133MHz maximum

Table 16

DTR – Frequency (MHz)					
Dummy Clock Cycles	**SPI** 1s-1d-1d 1s-1d-2d 1s-1d-4d 1s-1d-8d	**DUAL** 1s-2d-2d 2d-2d-2d	**QUAD** 1s-4d-4d 4d-4d-4d	**Octal** 1s-8d-8d* 8d-8d-8d	**OpCode**
0	~	~	~	~	
1	~	~	~	~	
2	16	16	16	~	READ FAST
3	33	33	33	33	READ FAST
4	50	50	50	50	READ FAST
5	66	66	66	66	READ FAST
6	83	83	83	83	READ FAST
7	90	90	90	100	READ FAST
8	90	90	90	116	READ FAST
9	90	90	90	133	READ FAST
10	90	90	90	150	READ FAST
11	90	90	90	166	READ FAST
12	90	90	90	183	READ FAST
13	90	90	90	200	READ FAST
14	90	90	90	200	READ FAST
15	90	90	90	200	READ FAST
16	90	90	90	200	READ FAST

* Limited to 133MHz maximum

Table 17

6. Register Operations

7.1 Read Register Operations

Command	Description	Note
Read Status Register (05h)	Can be read continuously and at any time, including during a PROGRAM, ERASE, or WRITE operation. If one of these operations is in progress, checking the write in progress bit (bit 0 in Status register) or P/E bit (bit 7 in Flag Status register) is recommended before executing a new command.	
Read Flag Status Register (70h)		
Read Nonvolatile Configuration Register (B5h) and Read Volatile Configuration Register (85h)	Register contents of the selected register address will be output on the IO's. If an address is selected beyond the defined address range of the configuration register, the data output will be undefined.	
Read General Purpose Register (96h)	The GPR will contain CRC results. Refer to the CRC Operation section.	

Table 18

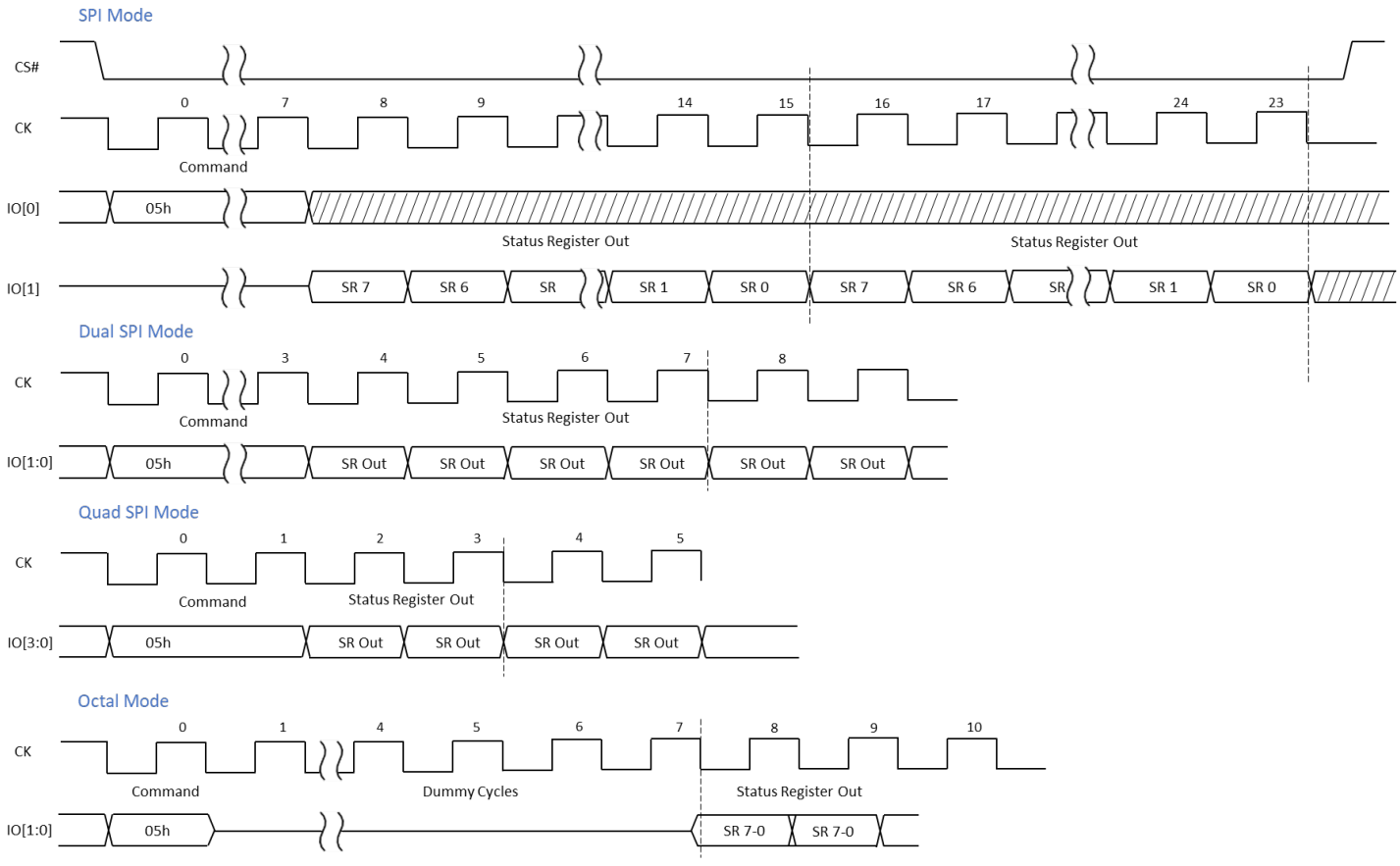


Figure 5: Read Status Register with STR

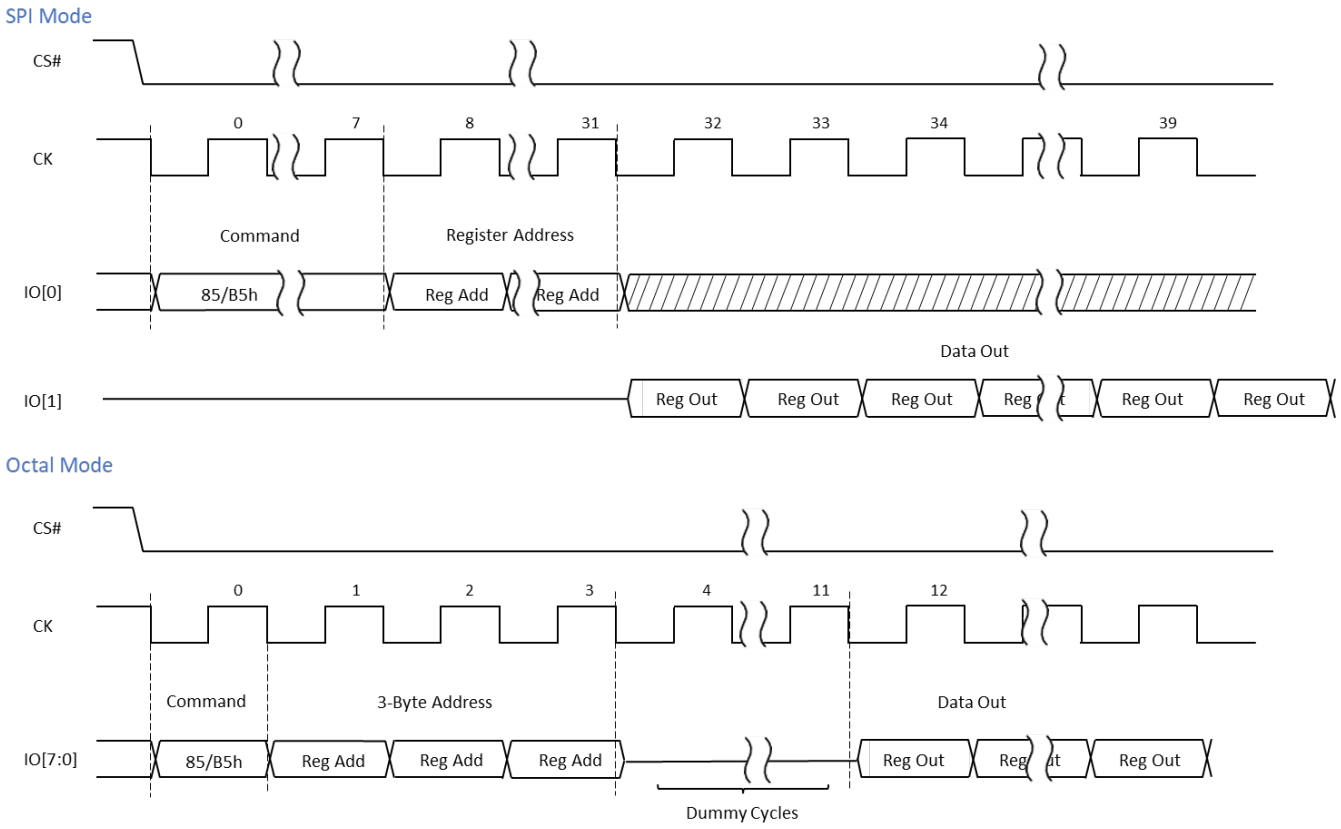


Figure 6: Read Nonvolatile/Volatile Register

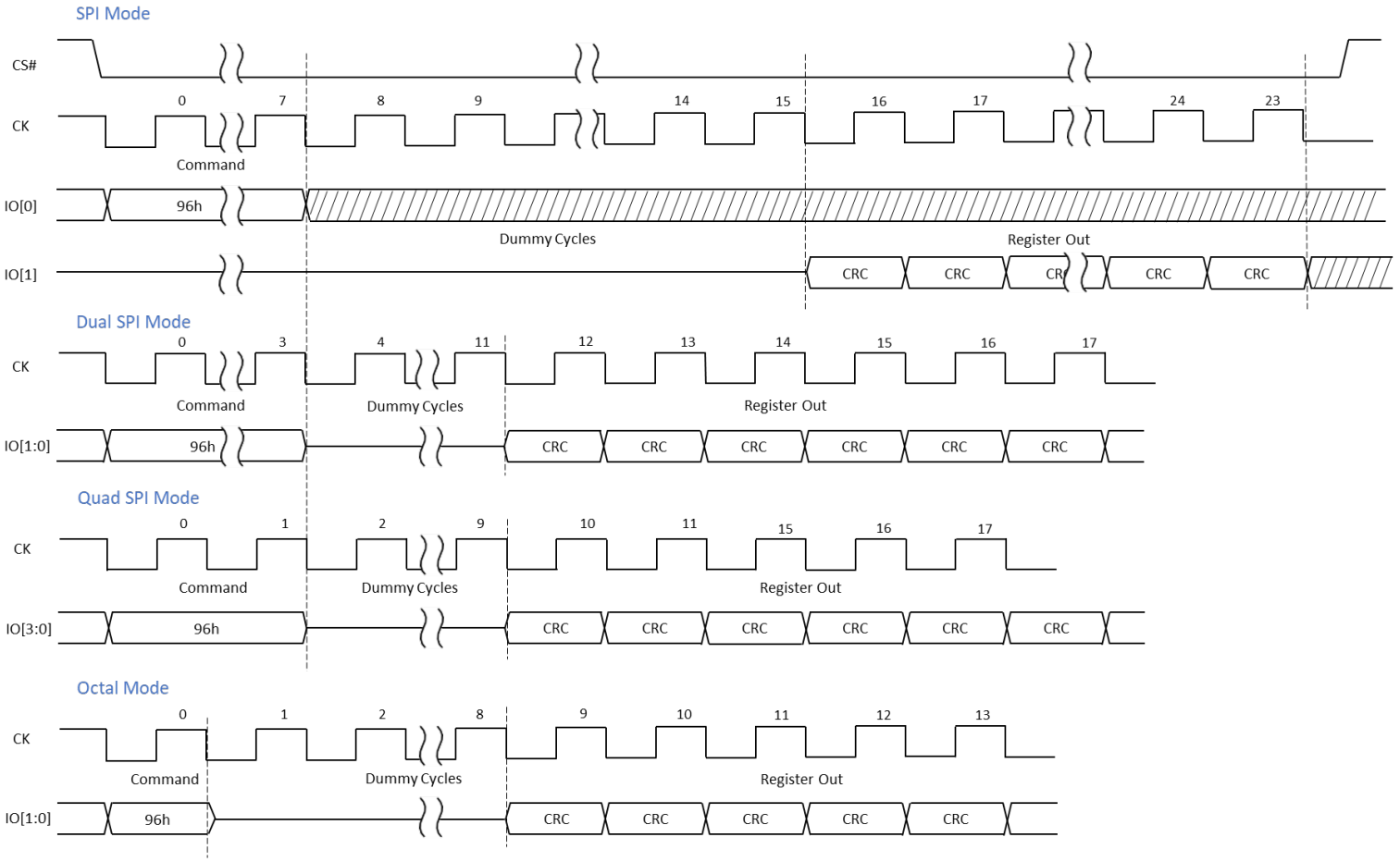


Figure 7: READ General Purpose Register with STR

6.2 Write Register Operations

Command	Description	Note
Write Status Register (01h)	The WRITE STATUS REGISTER command writes new values to status register bits 7:2, enabling software data protection. The status register can also be combined with the WP# signal to provide hardware data protection. This command has no effect on status register bits 1:0. For the WRITE STATUS REGISTER and WRITE NONVOLATILE CONFIGURATION REGISTER commands, when the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is not cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0, whether the operation is successful or not.	1,2
Write Nonvolatile Configuration Register (B1h)		
Write Volatile Configuration Register (81h)	Because register bits are volatile, change to the bits is immediate. Reserved bits are not affected by this command.	2
Clear Flag Status Register (50h)	This command will clear (set to "0") flag status register bits 5, 4,3 and 1 in the Flag Status Register. These are the error status bits.	

Table 19

Notes:

1. The WRITE NONVOLATILE CONFIGURATION REGISTER operation must have input data starting from the least significant byte.
2. When writing to the Status Register or to a single Nonvolatile or Volatile Configuration Register in 8d mode (DTR), the first data byte gets written into the register. When writing to the Nonvolatile and Volatile registers, the register address will increment sequentially if the write operation is continued, and additional bytes will be written. This may be different than some NOR Flash devices in which only one byte of data is accepted. In the case of Nonvolatile and Volatile configuration register writes, in 8d mode, the start address must be even. Single writes with odd addresses are not allowed. In 8d mode, two data bytes will be written, it is not possible to write only one byte.

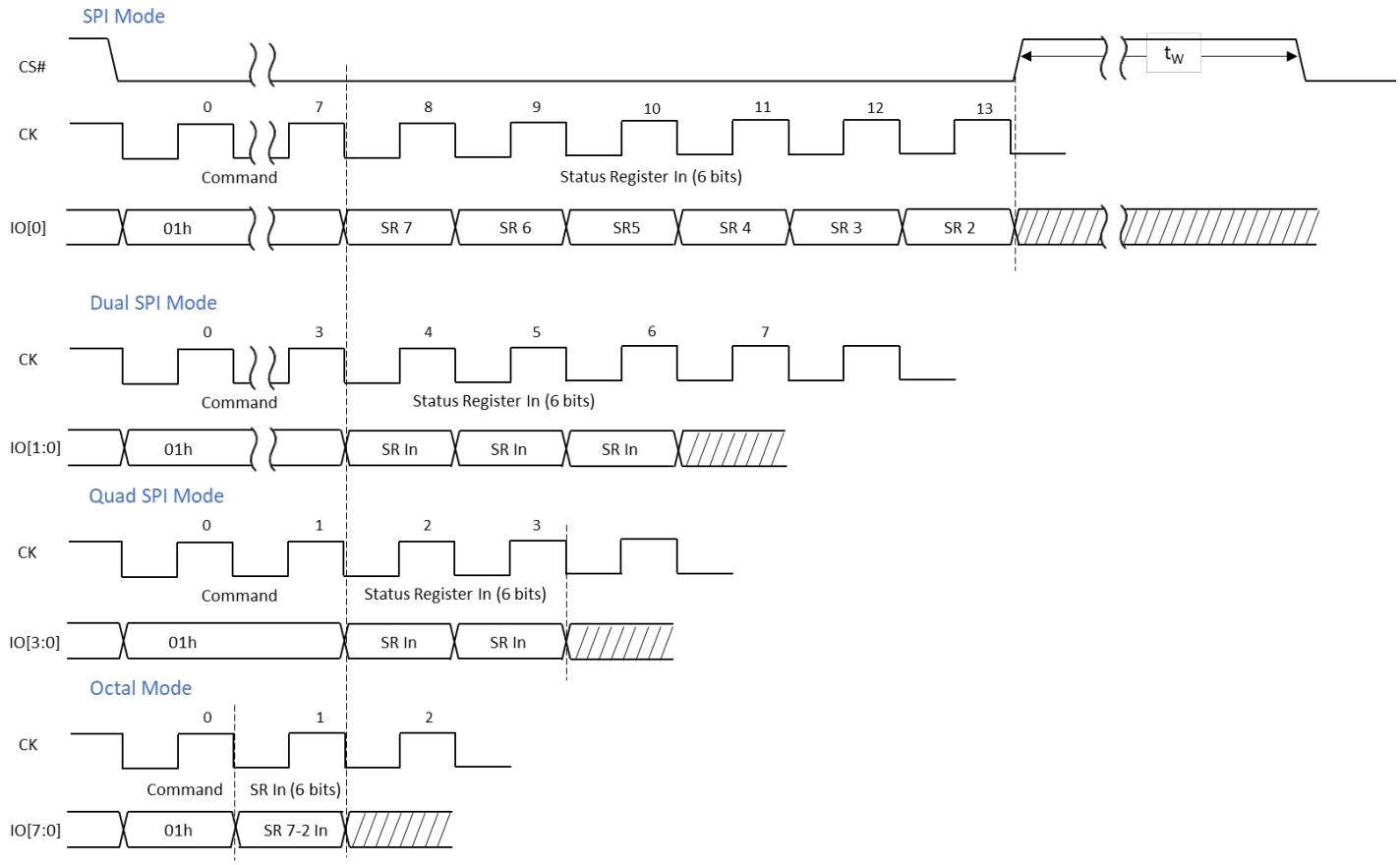


Figure 8: Write Status Register

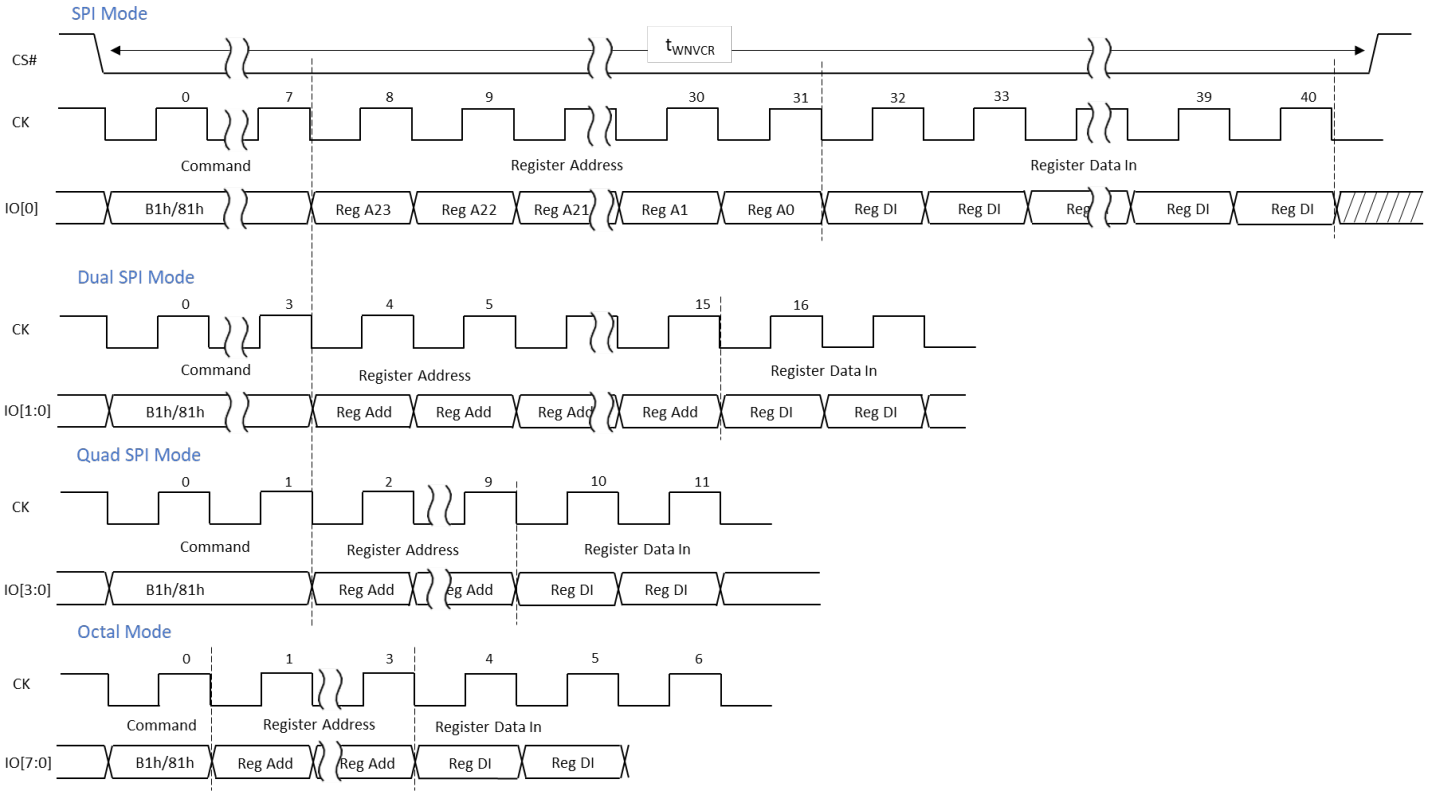


Figure 9: Write Nonvolatile/Volatile Register

8. Memory Organization

Capacity	Sector (64KB)	Subsector (32KB)	Subsector (4KB)	Address Range	
				Start	End
64Mb	127	255	2047	007F F000h	007F FFFFh
			⋮	⋮	⋮
			2040	007F 8000h	007F 8FFFh
		254	2039	007F 7000h	007F 7FFFh
			⋮	⋮	⋮
			2032	007F 0000h	007F 0FFFh
	⋮	⋮	⋮	⋮	⋮
32Mb	63	127	1023	003F 0000h	003F FFFFh
			⋮	⋮	⋮
			1016	003F 8000h	003F 8FFFh
		126	1015	003F 7000h	003F 7FFFh
			⋮	⋮	⋮
			1008	003F 0000h	003F 0FFFh
	⋮	⋮	⋮	⋮	⋮
16Mb	31	63	511	001F F000h	001F FFFFh
			⋮	⋮	⋮
			504	001F 8000h	001F 8FFFh
		62	503	001F 7000h	001F 7FFFh
			⋮	⋮	⋮
			496	001F 0000h	001F 0FFFh
	⋮	⋮	⋮	⋮	⋮
8Mb	15	31	255	000F F000h	000F FFFFh
			⋮	⋮	⋮
			248	000F 8000h	000F 8FFFh
		30	247	000F 7000h	000F 7FFFh
			⋮	⋮	⋮
			240	000F 0000h	000F 0FFFh
	⋮	⋮	⋮	⋮	⋮
	0	1	15	0000 F000h	0000 FFFFh
			⋮	⋮	⋮
			8	0000 8000h	0000 8FFFh
		0	7	0000 7000h	0000 7FFFh
			⋮	⋮	⋮
			0	0000 0000h	0000 0FFFh

Table 20

9. xSPI Command Opcodes and Modes

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of CK after CS# is driven low. Command sequences starts with a one-byte command code. The one-byte command code is shifted into the device on the IO's, and each bit is latched on the rising edges of CK. Depending on the command, this might be followed by address bytes or by data bytes, or by both or neither. CS# must be driven high after the last bit of the command sequence has been completed. For the commands Read, Read Fast, Read Status Register or Deep Power-Down exit, and Read ID, the shifted-in command sequence is followed by a data-out sequence. All read instructions can be completed after any bit of the data-out sequence is being shifted out, then CS# must be driven high to return to deselected status.

Table 21: Instruction Command Table

Instruction Command Set	Opcode (Hex)	SPI Mode	DSPI Mode	QSPI Mode		OSPI Mode		Address Bytes[6]	Latency[4] (Dummy)
				STR	DTR	STR	DTR		
RESET Enable	66	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
RESET Memory	99	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Read ID	9E	1s-0-1s	~	~	~	8s-0-8s	8d-0-8d	0	0,0,0,8
Read ID	9F	1s-0-1s	~	~	~	8s-0-8s	8d-0-8d	0	0,0,0,8
Read ID MIO	AF	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	0,0,0,8
Read	03	1s-1s-1s	~	~	~	~	~	3/4	0
Read Fast (XIP)	0B	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	DCC
Read Fast Dual Output	3B	1s-1s-2s	2s-2s-2s	~	~	~	~	3/4	DCC
Read Fast Dual I/O	BB	1s-2s-2s	2s-2s-2s	~	~	~	~	3/4	DCC
Read Fast Quad Output	6B	1s-1s-4s	~	4s-4s-4s	4s-4d-4d	~	~	3/4	DCC
Read Fast Quad I/O	EB	1s-4s-4s	~	4s-4s-4s	4s-4d-4d	~	~	3/4	DCC
Read Fast DTR	0D	1s-1d-1d	2s-2d-2d	4s-4d-4d	4s-4d-4d	~	~	3/4	DCC
Read Fast Dual Output DTR	3D	1s-1d-2d	2s-2d-2d	~	~	~	~	3/4	DCC
Read Fast Dual I/O DTR	BD	1s-2d-2d	2s-2d-2d	~	~	~	~	3/4	DCC
Read Fast Quad Output DTR	6D	1s-1d-4d	~	4s-4d-4d	4s-4d-4d	~	~	3/4	DCC
Read Fast Quad I/O DTR	ED	1s-4d-4d	~	4s-4d-4d	4s-4d-4d	~	~	3/4	DCC
Read Word Quad I/O (no DTR)	E7	1s-4s-4s	~	4s-4s-4s	~	~	~	3/4	4
Read Fast Octal Output[3]	8B	1s-1s-8s	~	~	~	8s-8s-8s	8d-8d-8d	3/4[5]	DCC
Read Fast Octal I/O[3]	CB	1s-8s-8s	~	~	~	8s-8s-8s	8d-8d-8d	3/4[5]	DCC
Read Fast Octal Output DTR[3]	9D	1s-1d-8d	~	~	~	8d-8d-8d	8d-8d-8d	3/4[5]	DCC
Read Fast Octal I/O DTR[3]	FD	1s-8d-8d	~	~	~	8d-8d-8d	8d-8d-8d	4[5]	DCC
Read 4-byte address	13	1s-1s-1s	~	~	~	~	~	4	0
Read Fast 4-byte address	0C	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	4[5]	DCC
Read Fast Dual Output 4-Byte Address	3C	1s-1s-2s	2s-2s-2s	~	~	~	~	4	DCC
Read Fast Dual I/O 4-byte Address	BC	1s-2s-2s	2s-2s-2s	~	~	~	~	4	DCC
Read Fast Quad Output 4-Byte Address	6C	1s-1s-4s	~	4s-4s-4s	4s-4d-4d	~	~	4	DCC
Read Fast Quad I/O 4-Byte Address	EC	1s-4s-4s	~	4s-4s-4s	4s-4d-4d	~	~	4	DCC
Read Fast DTR 4-Byte Address	0E	1s-1d-1d	2s-2d-2d	4s-4d-4d	4s-4d-4d	~	~	4	DCC
Read Fast Dual I/O DTR 4-Byte Address	BE	1s-2d-2d	2s-2d-2d	~	~	~	~	4	DCC
Read Fast Quad I/O DTR 4-Byte Address	EE	1s-4d-4d	~	4s-4d-4d	4s-4d-4d	~	~	4	DCC
Read Fast Octal Output 4-byte address[3]	7C	1s-1s-8s	~	~	~	8s-8s-8s	8d-8d-8d	4[5]	DCC
Read Fast Octal I/O 4-byte address[3]	CC	1s-8s-8s	~	~	~	8s-8s-8s	8d-8d-8d	4[5]	DCC
Write Enable	06	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0

Instruction Command Set	Opcode (Hex)	SPI Mode	DSPI Mode	QSPI Mode		OSPI Mode		Address Bytes[6]	Latency[4] (Dummy)
				STR	DTR	STR	DTR		
Write Disable	04	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Read Status Register	05	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	0,0,0,8
Read Flag Status Register	70	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	0,0,0,8
Read Nonvolatile Configuration Register	B5	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0,0,0,8
Read Volatile Configuration Register	85	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0,0,0,8
Read General Purpose Register	96	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	8,8,8,8
Write Status Register[1]	01	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	0
Write Nonvolatile Configuration Register[1]	B1	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0
Write Volatile Configuration Register[1]	81	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0
Clear Flag Status Register	50	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Write (Program Page)[1,2]	02	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0
Write (Program) Fast Dual Input[1,2]	A2	1s-1s-2s	2s-2s-2s	~	~	~	~	3/4	0
Write (Program) Fast Dual Input Extended[1,2]	D2	1s-2s-2s	2s-2s-2s	~	~	~	~	3/4	0
Write (Program) Fast Quad Input[1,2]	32	1s-1s-4s	~	4s-4s-4s	4s-4d-4d	~	~	3/4	0
Write (Program) Fast Quad Input Extended[1,2]	38	1s-4s-4s	~	4s-4s-4s	4s-4d-4d	~	~	3/4	0
Write (Program) Fast Octal Input[1,2,3]	82	1s-1s-8s	~	~	~	8s-8s-8s	8d-8d-8d	3/4[5]	0
Write (Program) Fast Octal Input Extended[1,2,3]	C2	1s-8s-8s	~	~	~	8s-8s-8s	8d-8d-8d	3/4[5]	0
Write (Program) 4-byte address[1,2]	12	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	4[5]	0
Write (Program) Fast Quad Input 4-byte[1,2]	34	1s-1s-4s	~	4s-4s-4s	4s-4d-4d	~	~	4	0
Write (Program) Fast Quad Input Ext. 4-byte[1,2]	3E	1s-4s-4s	~	4s-4s-4s	4s-4d-4d	~	~	4	0
Write (Program) Fast Octal Input 4-byte[1,2,3]	84	1s-1s-8s	~	~	~	8s-8s-8s	8d-8d-8d	4[5]	0
Write (Prog) Fast Octal Input Extended 4-byte[1,2,3]	8E	1s-8s-8s	~	~	~	8s-8s-8s	8d-8d-8d	4[5]	0
Erase 32kB[1]	52	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	3/4[5]	0
Erase 4kB[1]	20	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	3/4[5]	0
Erase Sector[1]	D8	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	3/4[5]	0
Erase/Bulk Chip[1]	C7	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Erase/Bulk Chip[1]	60	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Erase Sector 4-byte address[1]	DC	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	4[5]	0
Erase 4kB 4-byte address[1]	21	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	4[5]	0
Erase 32kB 4-byte address[1]	5C	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	4[5]	0
OTP Read	4B	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	DCC
OTP Write[1]	42	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0
4-byte address mode Enter	B7	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
4-byte address mode Exit	E9	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Deep Power Down Enter	B9	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Deep Power Down Exit	AB	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
CRC Operation	9B	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	Note 7,8	0
TDP Write[1]	F0	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0
TDP Read	F1	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	DCC
TDP Read DTR	F2	1s-1d-1d	2s-2d-2d	4s-4d-4d	4s-4d-4d	~	~	3/4	DCC

Table 21

Notes:

1. A Write Enable command is needed to set the WEL bit prior to this command but memory writes only require WREN the first time, subsequent writes do not require a WREN.
2. WREN is only required one time, subsequent writes do not require another WREN command
3. Octal commands are treated as a NOP in part numbers that are QSPI, including QSPI in the DFN package
4. Latency: Positions in this column, A,B,C,D, are defined as: A=SPI, B=Dual, C=Quad, D={8S|8D|4D}
5. Octal SPI with DTR operations or commands all require 4-byte address input. 4-byte addressing does not need to be enabled.
6. A "0" indicates that there is no address byte required.
7. CRC command has a command modifier . The second byte input is a sub-command , not an address.
8. CRC operation on 8Mb, 16Mb and 32Mb part numbers may not be done on the entire memory space using modifier FFh in Byte 3. For those part numbers, a CRC operation may only be done on a specified address range with modifier Feh, however this range can cover the entire memory space if desired. See Sec. 20.

- "~" indicates mode not supported .
- DCC = Dummy Clock Cycles from Configuration Register

xSPI Opcode Timing Representation

Please refer to the modular timing waveform below to understand the full timing for any opcode for EMxxLX shown in section "xSPI Command Opcodes and Modes". Timing of each supported opcode can be decomposed into three key items. Command, Address, and Data as shown below:

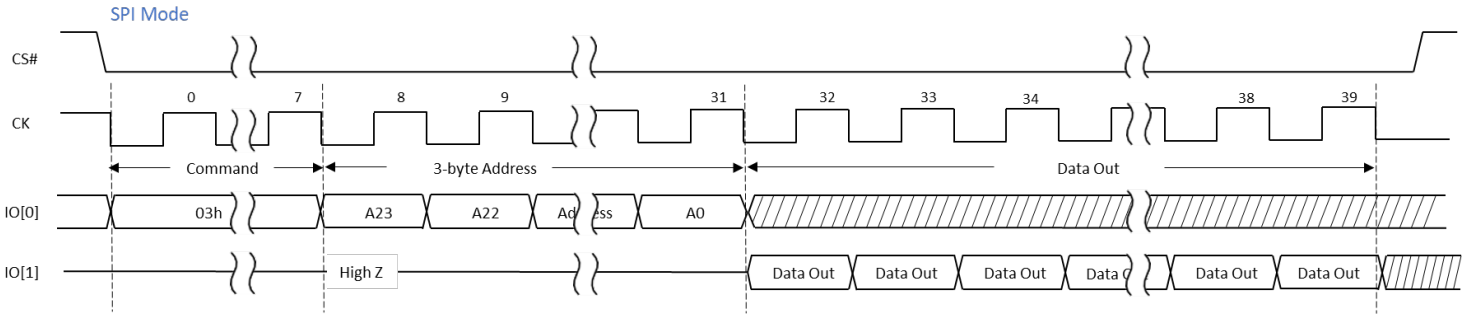


Figure 10: Opcode Timing Diagram

10. Read and Write Operations

The EMxxLX has the unique ability to operate as a persistent memory with random, byte addressability for reads and writes with no erase required, but also follows the JESD 251 conventions for programming and erase operations should the user prefer this mode. Nonvolatile Configuration Register 8 or Volatile Configuration Register 8 (TBD) is designated to select persistent memory operation or xSPI compatible operation.

In persistent memory mode, a write to the array is accomplished with the Write command. Data bytes are written to an internal cache after the command and address bytes are received, and then written to the MRAM array continuously until CS# is driven high (end of Write operation). There is no limit to the number of bytes that can be written. The write address will wrap at the top of memory and will continue incrementing from address 0x00000000. Once CS# is driven high, the Write in Progress bit (WIP) can be read from the Status Register. WIP will indicate "Busy", (WIP=1) for a very short period after the last byte written. Writes to the MRAM array are very fast relative to NOR Flash devices.

11. Read Operations

READ ID

The Read ID command allows the 8-bit manufacturer identification to be read, with two additional device identification bytes following. The device identification indicates the memory type in the second byte, and the memory capacity of the device in the third byte.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The command sequence is shown below. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode.

The Read ID command is not decoded while an Erase or Program cycle is in progress and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

Operation Name	Description/Conditions
Read ID (9Eh/9Fh)	Outputs information shown in the Device ID Data tables. If an ERASE or PROGRAM cycle is in progress when the command is initiated, the command is not decoded and the command cycle in progress is not affected.

Device ID Data

The device ID data in the table below is read by the Read ID and Read ID Multiple IO commands.

Table 22: Device ID Data

Byte #	Description	Value	Byte Address	Assigned By
1	Manufacturer ID	0x6B	0x00	JEDEC
2	Memory Type (Voltage)	0xBB = 1.8V	0x01	Everspin
3	Memory Capacity	0x19 = 256Mb 0x18 = 128Mb 0x17 = 64Mb 0x16 = 32Mb 0x15 = 16Mb 0x14 = 8Mb	0x02	Everspin
4 – 20	Reserved	Reserved	0x04-0x13	Everspin

Table 22

Read ID Diagram

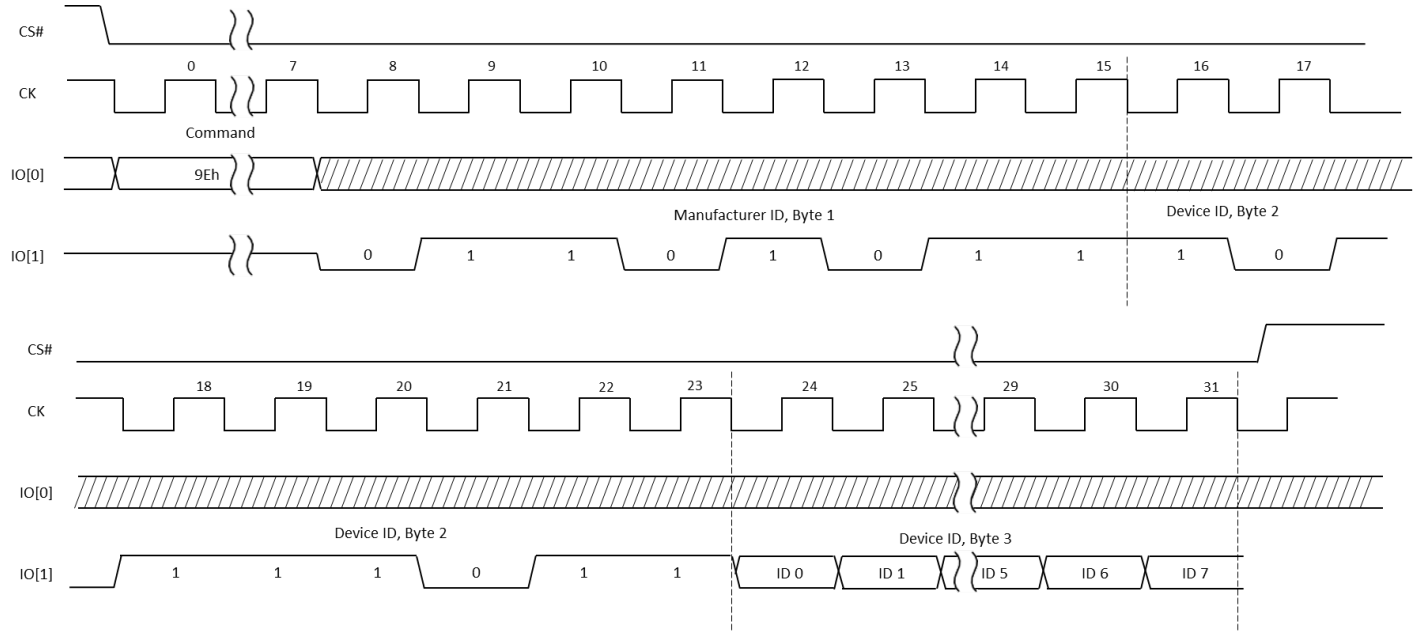


Figure 11

Read ID Diagram (Octal DTR Mode)

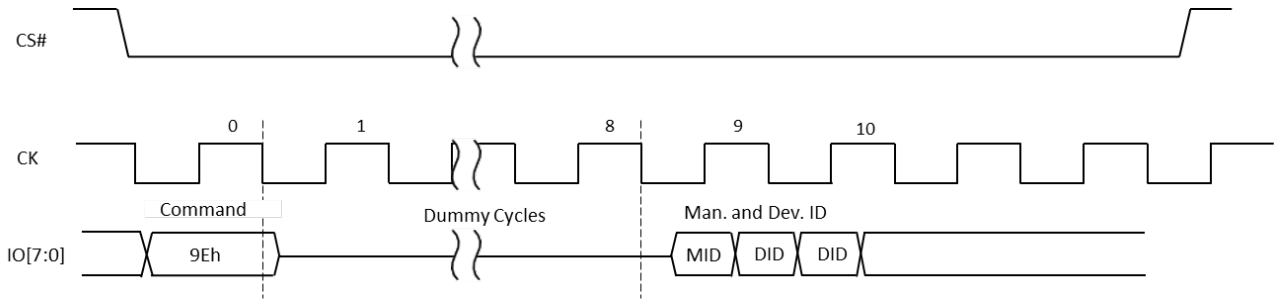


Figure 12

READ ID MULTIPLE IO

Operation Name	Description/Conditions
Read ID Multiple IO (AFh)	Outputs Device ID Data tables on 1, 2, 4 or 8 IO's. If an ERASE or PROGRAM cycle is in progress when the command is initiated, the command is not decoded and the command cycle in progress is not affected.

READ

Operation Name	Description/Conditions
Read (03h)	The device supports 3-byte addressing (default), with A[23:0] input during address cycle. After any READ command is executed, the device will output data from the selected address. After the boundary is reached, the device will start reading again from the beginning address. Each address bit is latched in during the rising edge of the clock. The addressed byte can be at any location, and the address automatically increments to the next address after each byte of data is shifted out; this means the entire array can be read with a single command. READ FAST can operate at a higher frequency (f_{CK}) DTR commands function in DTR protocol regardless of settings in the nonvolatile configuration register or volatile configuration register; other commands function in DTR protocol only after DTR protocol is enabled by the register settings. In DTR, address bits are latched on both edges of the clock. E7h is similar to the READ FAST QUAD I/O command except that the lowest address bit (A0) must equal 0 and only four dummy clocks are required prior to the data output. This command is supported in SPI and Quad SPI protocols, but not in the DTR protocol; it is ignored it in Dual SPI protocol. 4-BYTE commands and DTR 4-BYTE commands function in 4-BYTE and DTR 4-BYTE protocol regardless of settings in the nonvolatile configuration register or volatile configuration register; other commands function in 4-BYTE and DTR protocols only after the specific protocol is enabled by the register settings. The device will ignore address bits that are above the specified range. It is recommended to keep address bits above the specified range at “0”.
Read Fast (0Bh)	
Read Fast Dual Output (3Bh)	
Read Fast Dual Input/Output (BBh)	
Read Fast Quad Output (6Bh)	
Read Fast Quad Input/Output (EBh)	
Read Fast DTR (0Dh)	
Read Fast DTR Dual Output (3Dh)	
Read Fast DTR Dual Input/Output (BDh)	
Read Fast DTR Quad Output (6Dh)	
Read Fast DTR Quad Input/Output (EDh)	
Read Word Quad Input/Output No DTR (E7h)	
Read Fast Octal Output (8Bh)	
Read Fast Octal Input/Output (CBh)	
Read Fast DTR Octal Output (9Dh)	
Read Fast DTR Octal Input/Output (FDh)	

READ Diagram

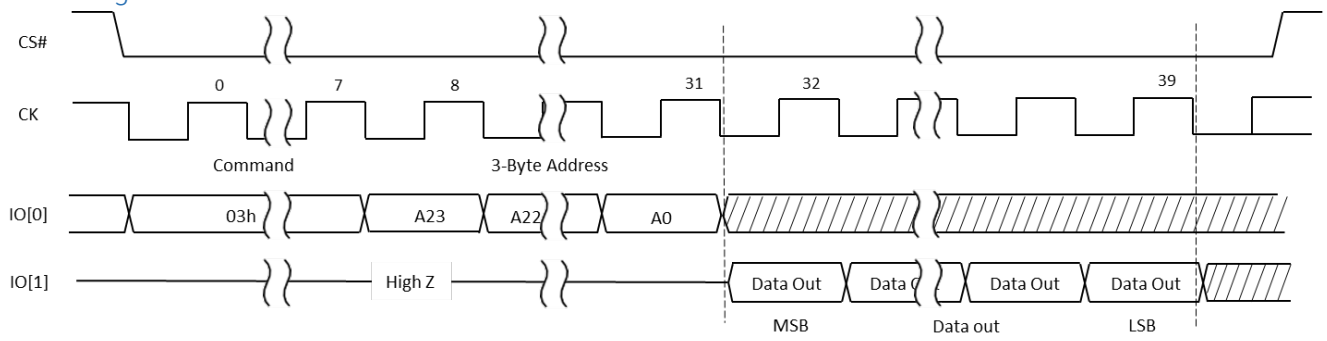


Figure 13

READ FAST Diagram

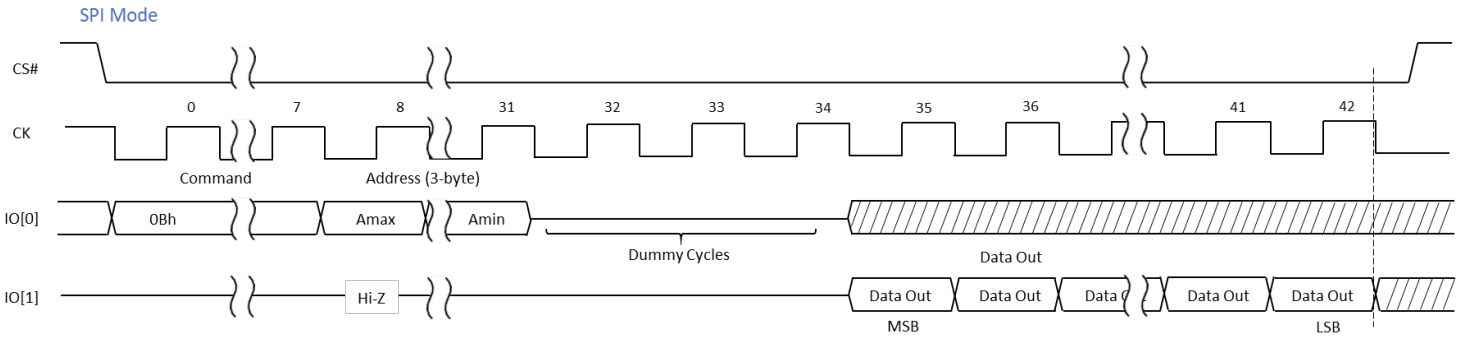


Figure 14

READ FAST Dual Input/Output

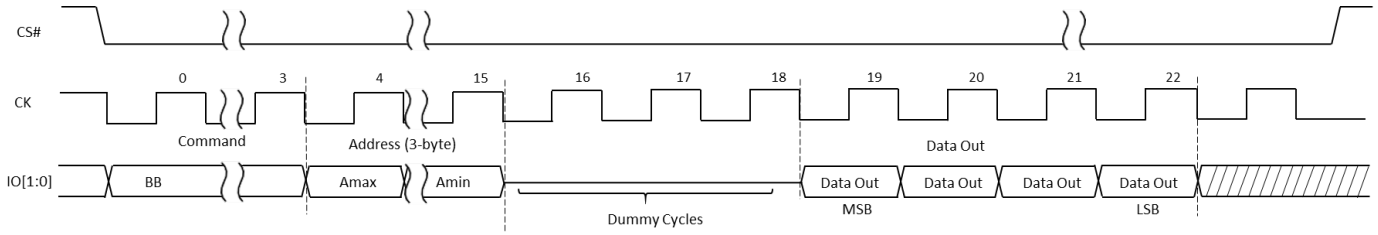


Figure 15

READ FAST Quad Input/Output

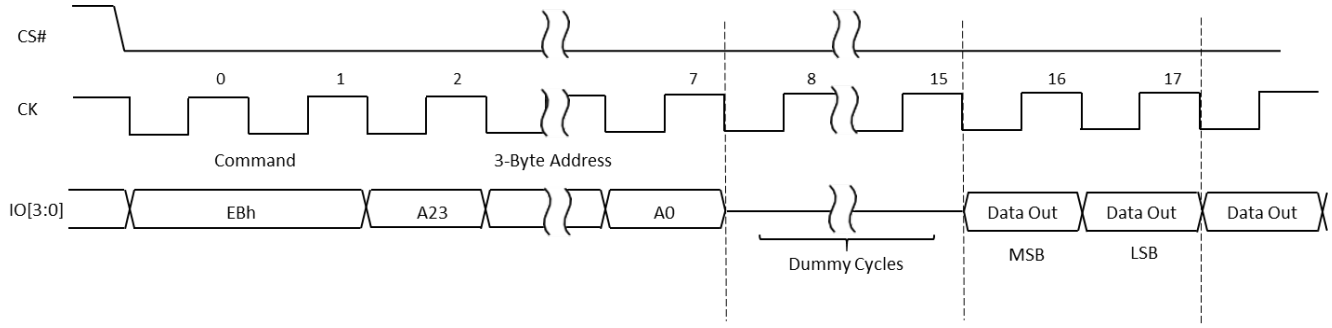
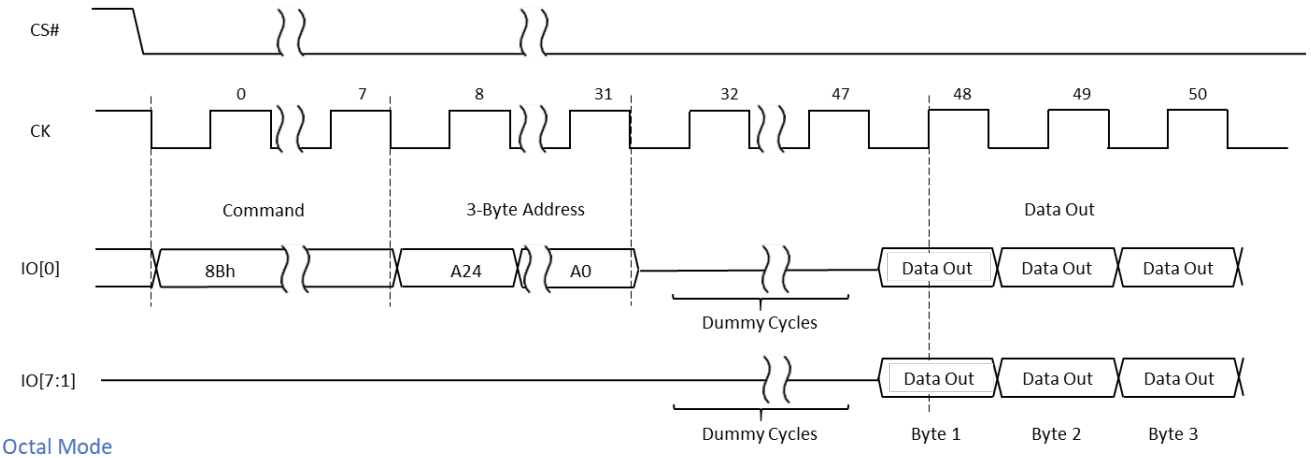


Figure 16

READ FAST Octal Output

SPI Mode



Octal Mode

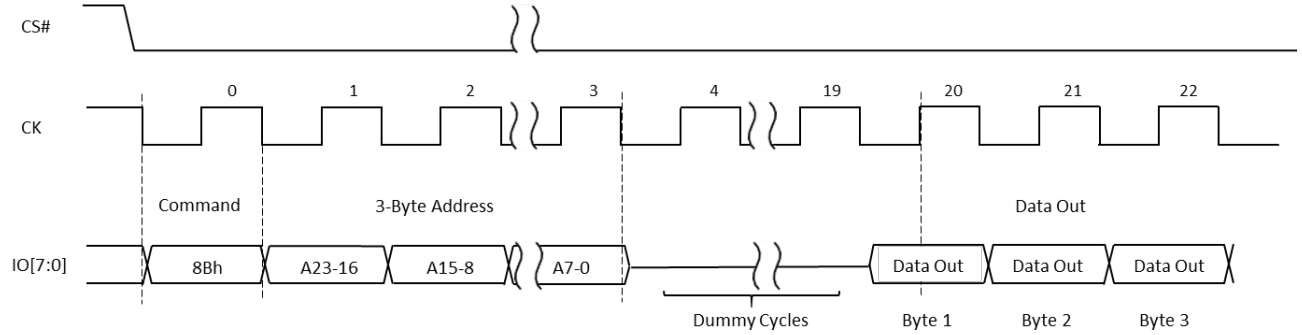


Figure 17

READ FAST Octal Input/Output

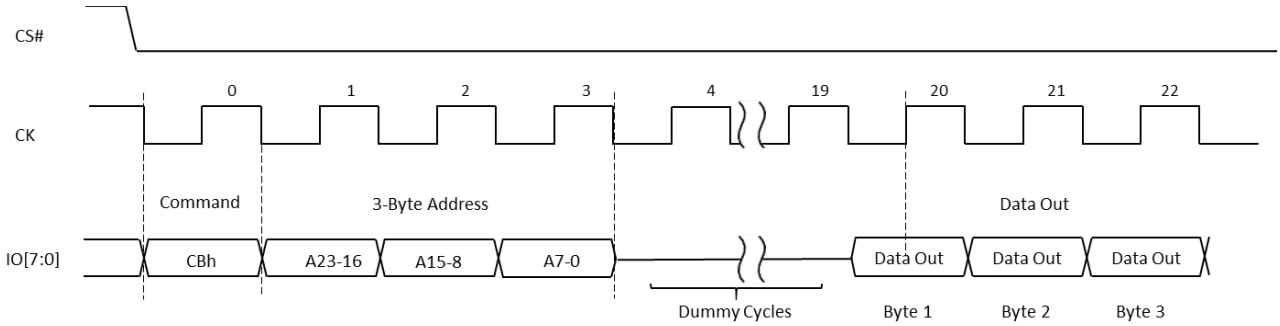


Figure 18

READ FAST DTR SPI, Dual SPI, Quad SPI, Octal SPI

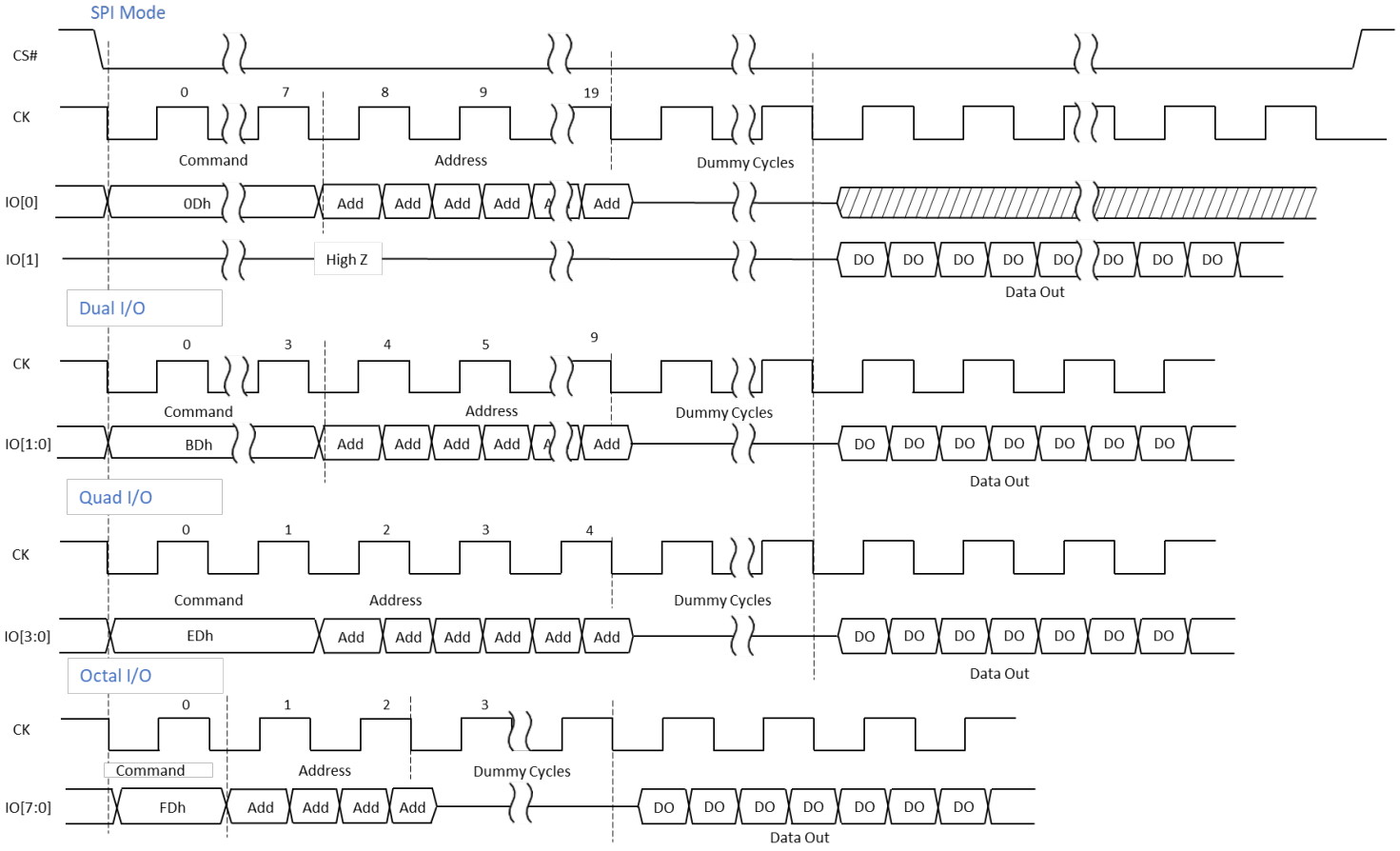


Figure 19

Note: In Octal SPI DTR mode, the address input is always 4-byte.

READ WORD QUAD INPUT/OUTPUT (no DTR) (E7h)

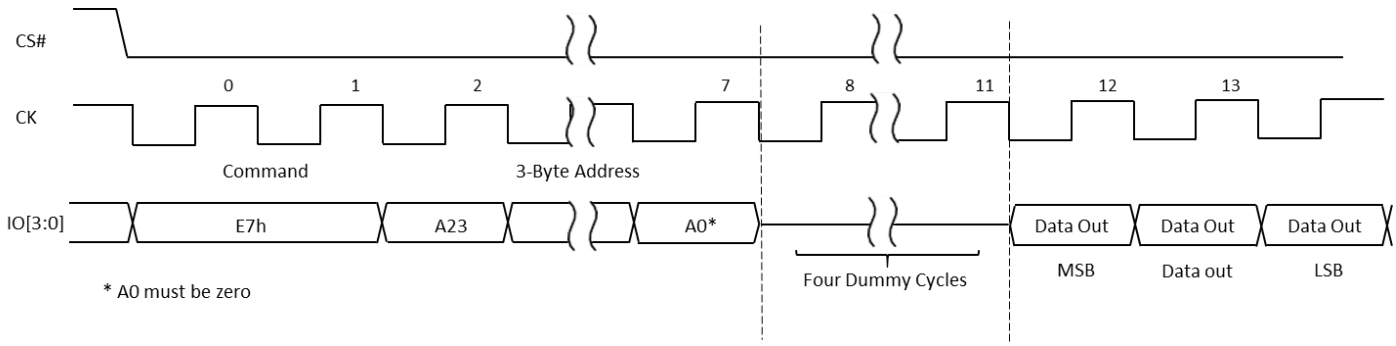


Figure 20

11. Write Operations

The EMxxLX can be configured to be written to as a persistent memory or be programmed similar to a NOR Flash device. The Nonvolatile Configuration Register 8 can be set to have the device operate as persistent memory (Bit 0=1) or to emulate NOR PROGRAM commands (Bit 0=0).

Write Enable/Disable Operations

Operation Name	Description
Write Enable (06h)	Sets the write enable latch bit, WEL. This command is required before each WRITE (Program) and ERASE operation. For subsequent memory write operations, WRITE enable does not need to be loaded, saving cycle overhead for back to back write operations to memory. (For these commands, the WEL bit is not reset at the completion of the write command)
Write Disable (04h)	Clears the write enable latch bit, WEL.

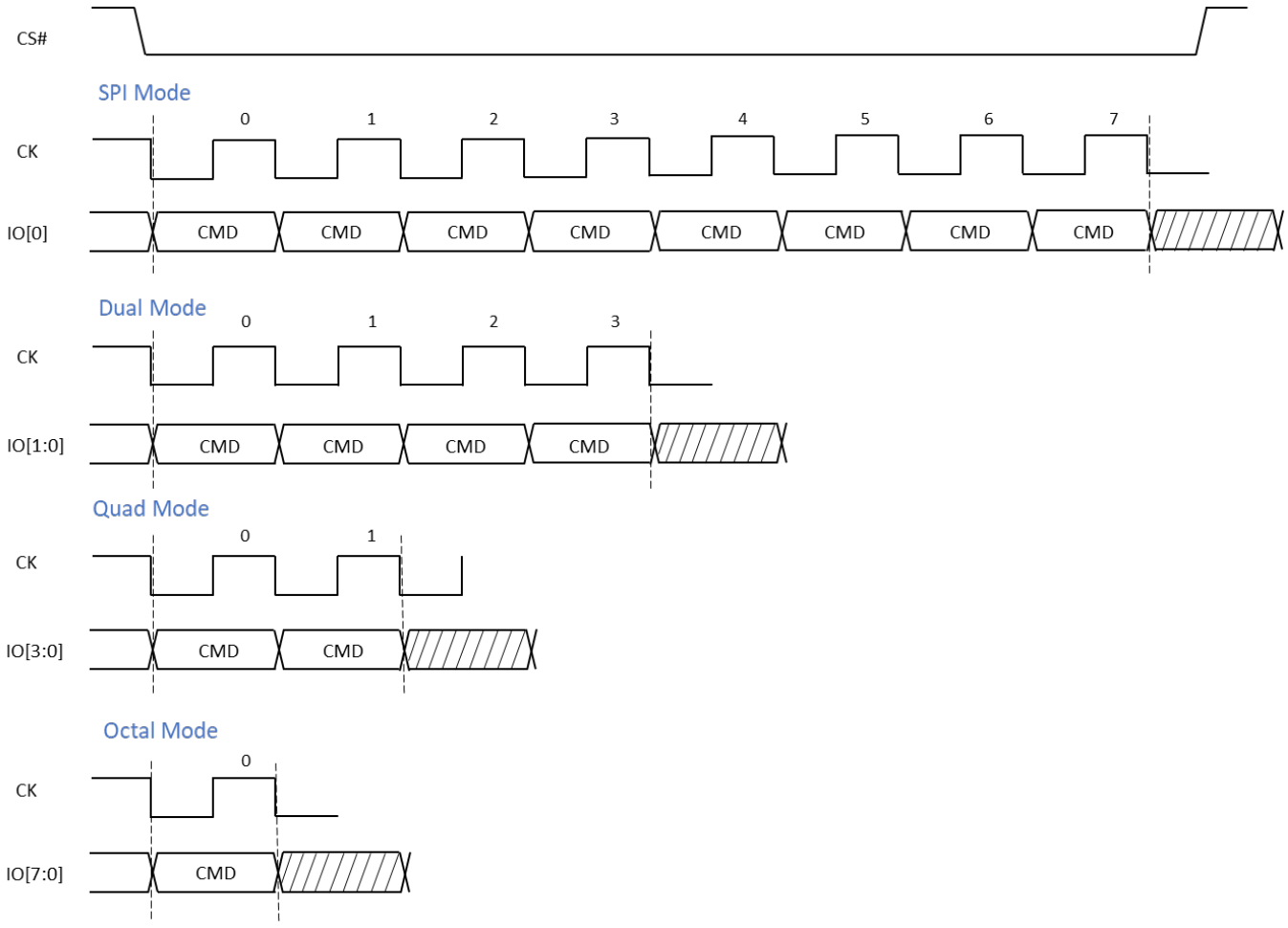
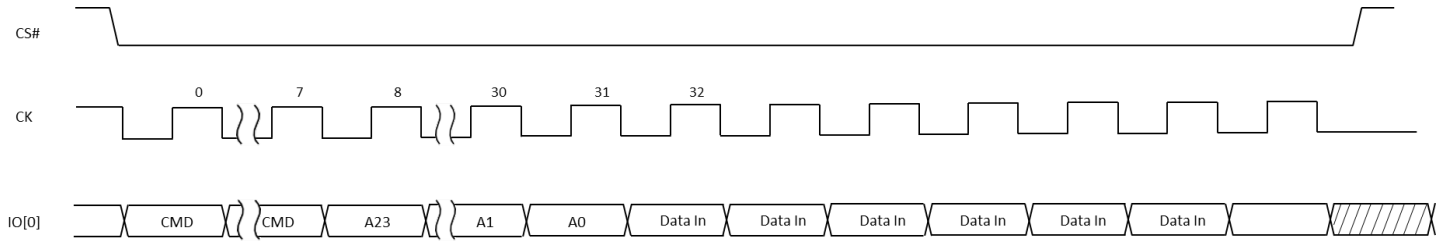


Figure 21

WRITE (PROGRAM) OPERATIONS

Operation Name	Description/Conditions
Write (Program) (02h) Write (Program) FAST Dual Input (A2h) Write (Program) FAST Dual Input Extended (D2h) Write (Program) FAST Quad Input (32h) Write (Program) FAST Quad Input Extended (38h) Write (Program) FAST Octal Input (82h) Write (Program) FAST Octal Input Extended (C2h) Write (Program) 4-byte address (12h) Write (Program) FAST Quad Input 4-byte (34h) Write (Program) FAST Quad Input 4-byte Extended (3Eh) Write (Program) FAST Octal Input 4-byte (84h) Write (Program) FAST Octal Input 4-byte Extended (8Eh)	Write Operations are similar to PROGRAM except that data can change from 1 to 0 or 0 to 1 at any address location. No ERASE is required. There is no limit to the number of bytes that can be written. In persistent memory mode, the write address will wrap at the top of memory and will continue incrementing from address 0x00000000. Unlike NOR Flash, there is no page restriction. In NOR Flash mode, a 256 byte page can be written. Address Control wraps the write address at 0xFF (wrap back to 0, address bits A[31:8] remain unchanged during the write operation). If more than 256 bytes are written, since address wraps, data will be overwritten. The "Write in Progress" WIP status bit, Status Register Bit 0 can be polled to indicate whether or not the write has completed. Writes occur very fast, please refer to the timing specification. The WEL is not reset to "0" after completion of a write. WRITE operations can be extended to a 4-byte address range, with [A31:0] input during address cycle. Selection of the 3-byte or 4-byte address range can be enabled through the ENABLE 4-BYTE ADDRESS MODE/EXIT 4-BYTE ADDRESS MODE commands. 4-BYTE commands and DTR 4-BYTE commands function in 4-BYTE and DTR 4-BYTE protocol regardless of settings in the nonvolatile configuration register or volatile configuration register; other commands function in 4-BYTE and DTR protocols only after the specific protocol is enabled by the register settings. The device will ignore address bits that are above the specified range. It is recommended to keep address bits above the specified range at "0".

Write (Program) (02h)*

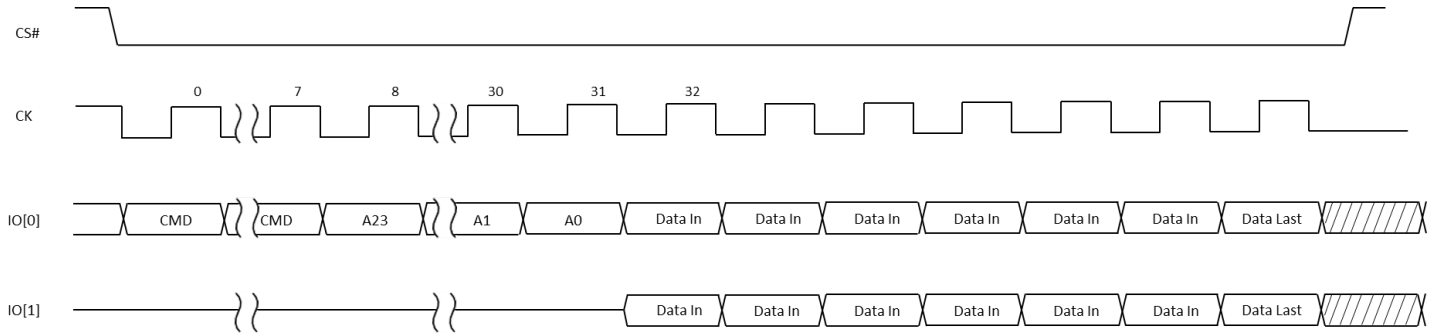


* Persistent memory mode allows writing “0” or “1” to any number of bytes. In Page program mode, writes are confined to the selected 256 byte page and the address wraps within the page. The mode is selected with Bit 0 in the volatile and nonvolatile configuration register 8.

Figure 22

Write Fast Dual Input (A2h)

SPI Mode



Dual SPI Mode

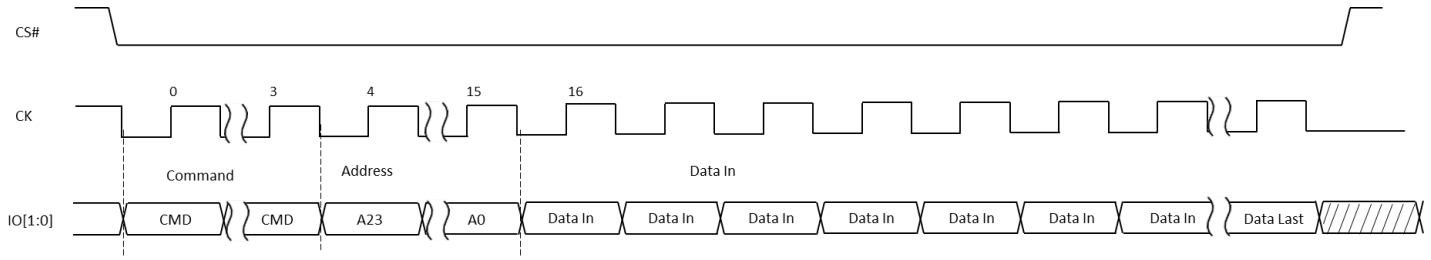
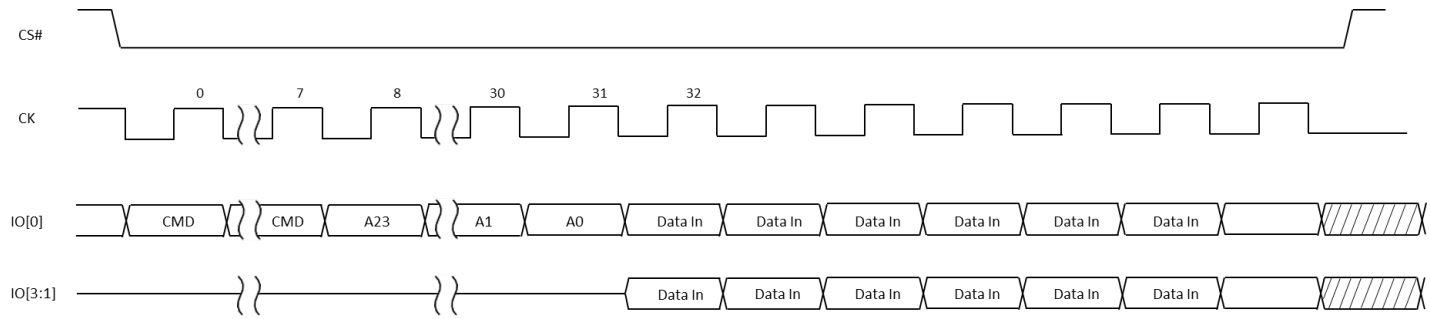


Figure 23

Write Fast Quad Input (32h)

SPI Mode



Quad SPI Mode

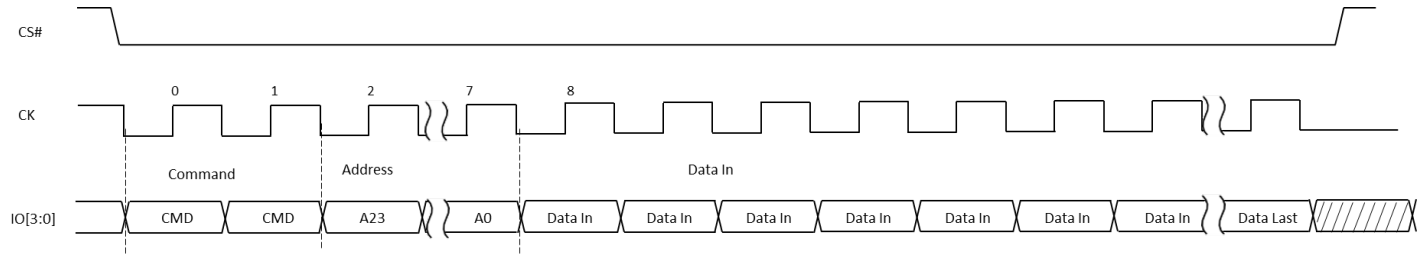
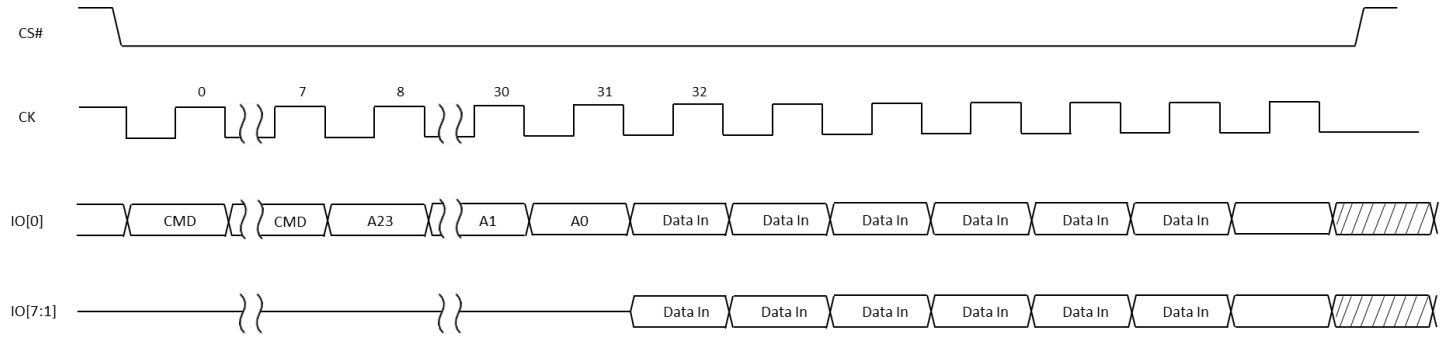


Figure 24

Write Fast Octal Input (82h)

SPI Mode



Octal SPI Mode

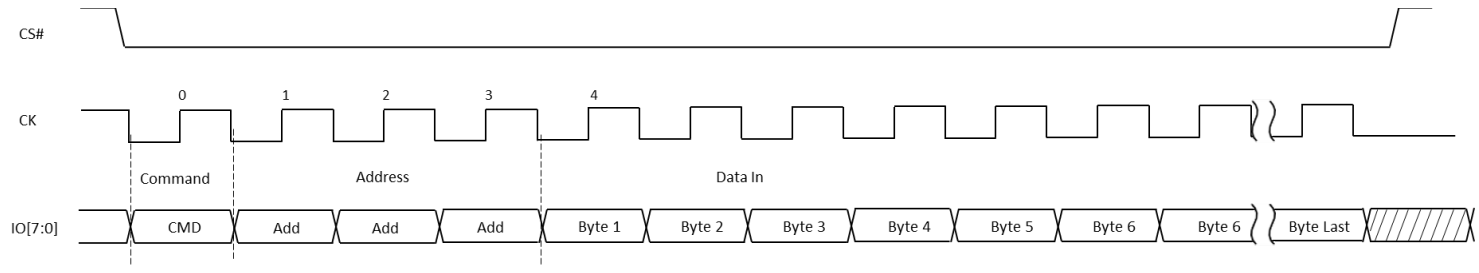
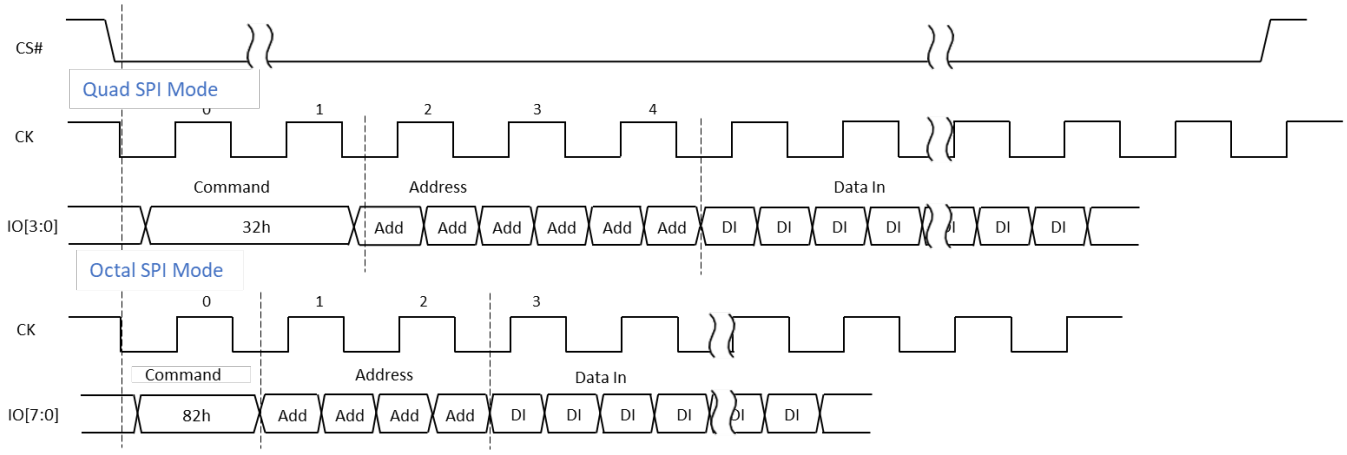


Figure 25

Write Fast with DTR Configured



Note: In Octal SPI DTR mode, the address input is always 4-byte.

Figure 26

12. XIP (Execute-in-Place) Mode

XIP (Execute-in-Place) mode allows the memory to be read by sending an address to the device without a command code and then receives the data on one, two, four or eight pins in parallel, depending on the configuration. XIP mode saves instruction overhead and reduces random access time.

Activate and Terminate XIP Using Volatile Configuration Register

Applications that boot in SPI and then switch to XIP should use the volatile configuration register. XIP provides faster memory read operations by requiring only an address to execute, rather than a command code and an address.

To activate XIP requires two steps. First, enable XIP by setting volatile configuration register address 6 bits [7:0] as shown in the Volatile configuration table. Next, drive the XIP confirmation bit to 0 during the next READ FAST (0Bh) operation. XIP is then active. Once in XIP, READ FAST command (0Bh) that occurs after CS# is toggled requires only address bits to execute; a command code is not necessary. Device operations use the SPI protocol that is enabled. XIP is terminated by driving the XIP confirmation bit to 1 and the device automatically resets volatile configuration register bit 0 to 1.

Activate and Terminate XIP Using Nonvolatile Configuration Register

Applications that must boot directly in XIP use the nonvolatile configuration register. To enable a device to power-up in XIP using this register, set nonvolatile configuration register address 6 bits [7:0] as shown in the Nonvolatile configuration register table. Because the device boots directly in XIP, after the power cycle, no command code is necessary. The XIP confirmation bit is set to 0. XIP is terminated by driving the XIP confirmation bit to 1.

Confirmation Bit Settings Required to Activate or Terminate XIP

The XIP confirmation bit setting activates or terminates XIP after XIP has been enabled in the configuration register. This bit is the value on IO0 during the first dummy clock cycle in the READ FAST operation. In Dual SPI XIP mode, the value of IO1 during the first dummy clock cycle after the addresses is always “Don’t Care.” In Quad SPI XIP mode, the values of IO3, IO2, and IO1 during the first dummy clock cycle after the addresses are always “Don’t Care.” In Octal SPI XIP mode, the values of IO7-1 during the first dummy clock cycle are always “Don’t Care”.

Bit Value	Description
0	Activates XIP: While this bit is 0, XIP remains activated.
1	Terminate XIP: When this bit is set to 1, XIP is terminated, and the device returns to SPI.

Table 23

READ FAST with XIP

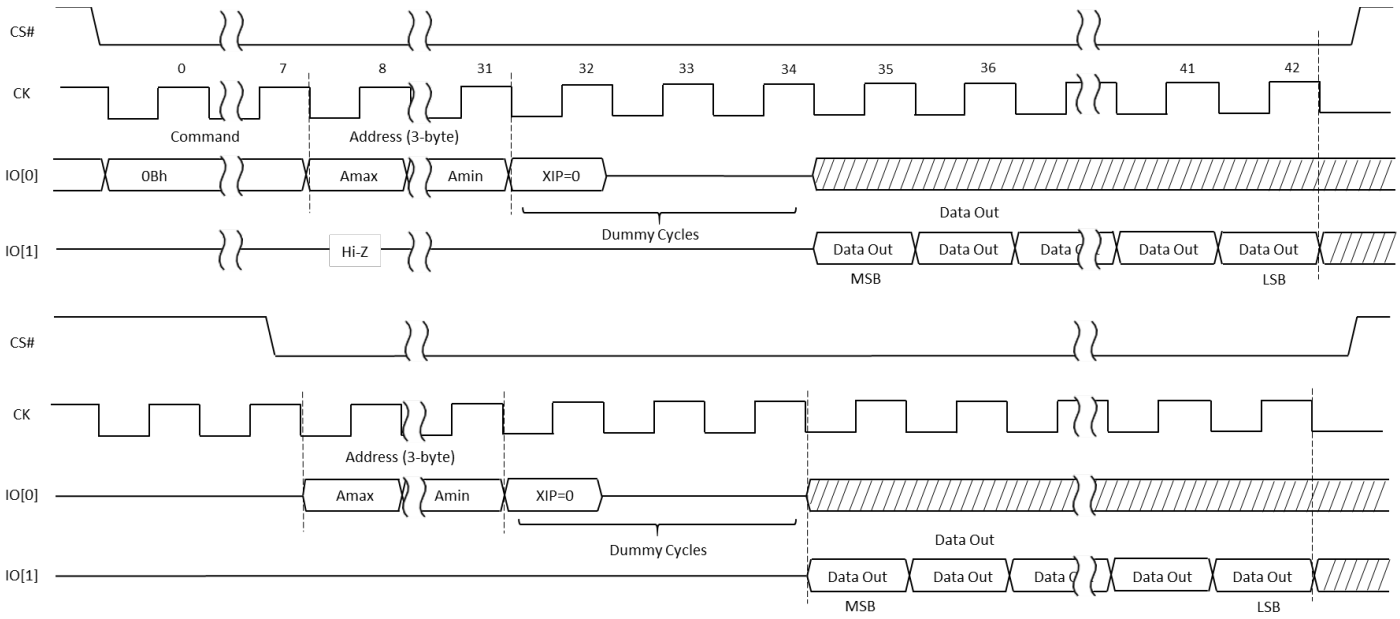


Figure 27

TERMINATING XIP AFTER A MEMORY RESET

A Power-On Reset or Hardware Reset will terminate XIP mode and cause the device to enter the mode configured in the nonvolatile configuration register (including XIP Boot mode). Software Reset is not applicable during XIP mode. A Reset with a signal sequence (JESD252 Reset) will exit XIP mode, but the volatile and nonvolatile configuration registers remain unchanged.

13. ERASE Operations

ERASE operations on the EMxxLX are not required because any bit in the MRAM array can be written to a 1 or 0 at any time regardless of the previous state of the bit. However, for user convenience, the EMxxLX will recognize ERASE opcodes and perform sub sector, sector and chip erase operations. The WRITE ENABLE command must be executed to set the write enable latch bit to 1 before any ERASE command is initiated ; otherwise, the device ignores the command and no error bits are set to indicate operation failure. Erase operations do not reset the write enable latch at the end of the operation.

For ERASE commands, CS# is driven LOW and held LOW until the eighth bit of the last address byte has been latched in, after which it must be driven HIGH. Any address inside the sector is a valid address for the Erase Subsector or Sector command. The operations are self-timed, and duration is tSSE, tSE, or tBE according to the command.

If CS# is not driven HIGH, the command is not executed, flag status register error bits 1 and 5 are not set. No ERASE is performed on a protected subsector. Instead, the write enable latch bit remains set to 1, and flag status register error bits 1 and 5 are set. When an ERASE is in progress, the program or erase status bit 7 of the flag status register is set to 0. In addition, the WIP bit 0 of the status register is set to 1. When the operation completes, the status register bit 0, WIP, is cleared to 0 and the flag status register bit 7 is set to 1 (Ready). The write enable latch bit is not cleared to 0, whether the operation is successful or not. If the operation times out, the erase error bit 5 in the flag status register is set to 1. The status and flag status registers can be polled for the operation status.

For the ERASE Chip command, the sequence is CS# Low, Command bits loaded > CS# High. No Address bits are loaded. CS# must remain high for t_{BE} for the chip erase to complete.

Operation Name	Description
ERASE Subsector 4kB (20h)	Erases the selected subsector or sector bits to 1, or FFh. Any address within the subsector is valid for entry. Each address bit is latched in during the rising edge of the clock.
ERASE Subsector 32kB (52h)	
ERASE Sector 64kB (D8h)	
ERASE Bulk/Chip (C7h/60h)	Erases all the device bits to 1, or FFh. The command is not executed if any sector is locked. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.

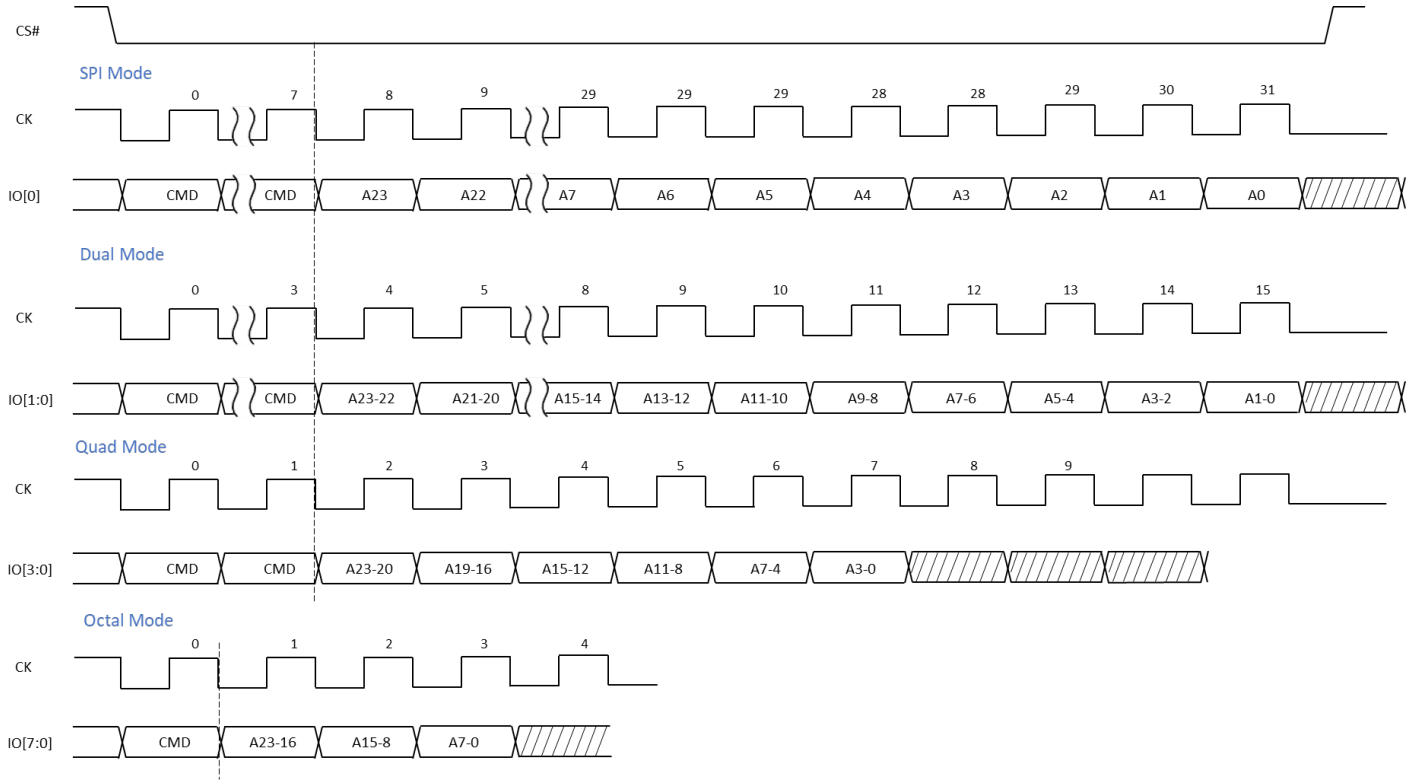


Figure 28 Erase Operations

14. OTP Operation

Operation Name	Description
OTP READ (4Bh)	OTP Data is shifted out on the Ios, beginning from the specified address. The address increments automatically to the next address after each byte of data is shifted out. There is no rollover mechanism; therefore, if read continuously, after location 0x40, the device continues to output data at location 0x40.
OTP WRITE (42h)	The 256 byte OTP data is written to the designated OTP location if the WEL bit is set by the WRITE Enable command.

OTP READ AND WRITE OPERATION

A dedicated area of 256 bytes outside of the memory array is provided to allow specific user information to be stored on a non-volatile basis. To write to the OTP, the WRITE ENABLE command must be issued to set the write enable latch bit to 1. The command code is input on the IO's, followed by address bytes and at least one data byte. There is no rollover mechanism; therefore, after a maximum of 257 bytes are latched in, the subsequent bytes are discarded. The OTP WRITE command writes, at most, 256 bytes to the OTP memory area and one OTP control byte. When the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is not cleared to 0, whether the operation is successful or not, and the status register can be polled for the operation status. When the operation completes, the WIP bit 0 in the status register is cleared to 0. CS# must be driven HIGH to complete the OTP WRITE. When CS# is driven high, the self-timed operation is initiated. The duration of the operation is tPOTP. The operation is considered complete once bit 7 of the flag status register outputs 1 with at least one byte output. The OTP control byte (byte 256) is used to lock the OTP memory array. The OTP will be unlocked during a device recovery sequence and can be reprogrammed if needed. The OTP may also be unlocked by setting Volatile Configuration register 8, bit 2 to "0", which will override the OTP Lock Byte setting and unlock the OTP array for rewriting. Once the OTP has been unlocked and updated, bit 2 should be set to "1" to enable the lock.

OTP WRITE (42h) w/ 3-Byte Address

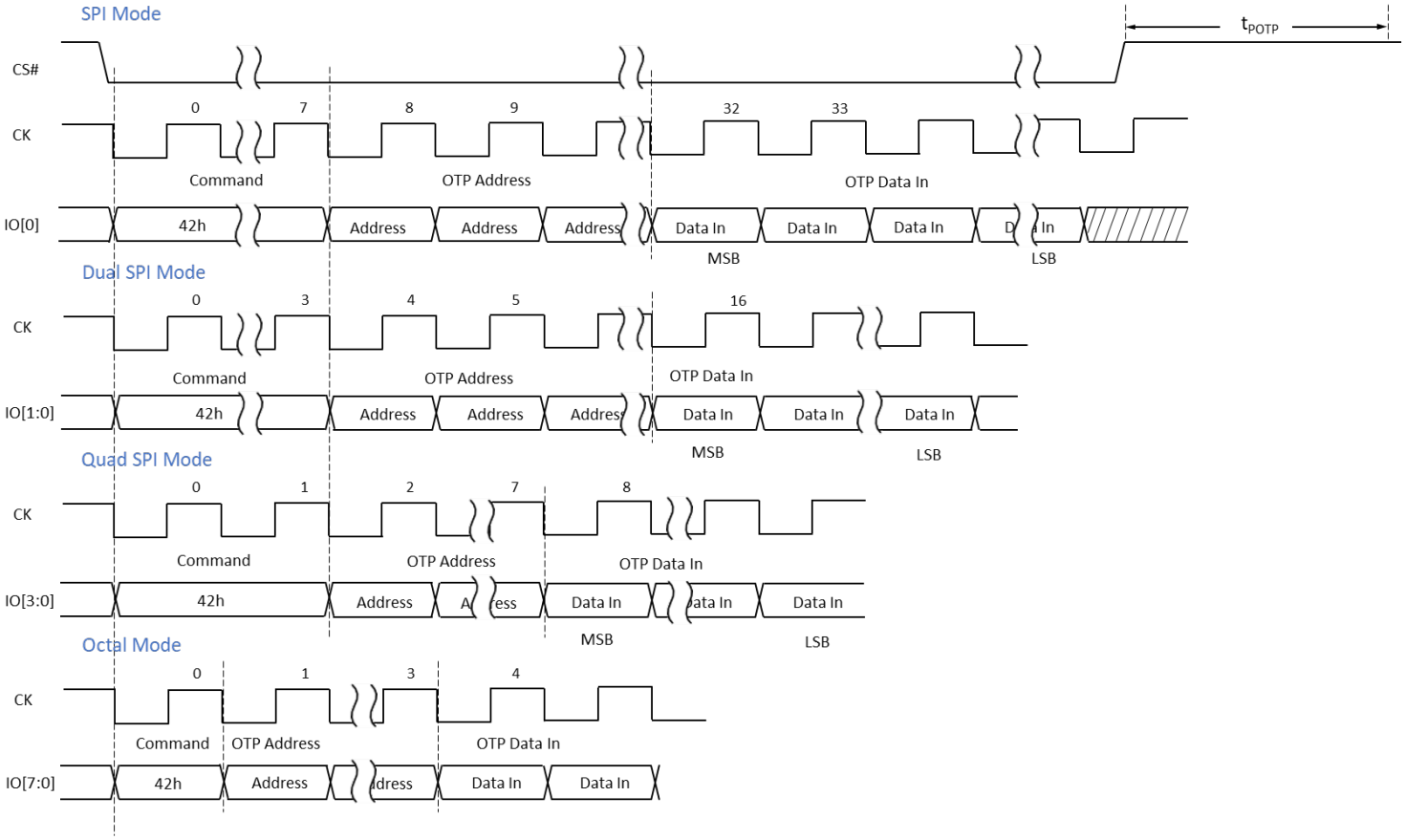


Figure 29

OTP Control Byte

The OTP control byte is used to lock the OTP memory area. It is written with the OTP WRITE command at OTP address 256.

Nonvolatile OTP Control Byte					
Address	**OTP Read/Write Byte 256**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:1	RO	Reserved			
0	RW	Lock Bit	0 = Locked 1 = Unlocked (default)	Used to lock the 256-byte OTP array. When bit 0 = 1, the 256-byte OTP array can be programmed. When bit 0 = 0, the OTP array is read only. Once bit 0 has been programmed to 0, it can no longer be changed to 1. Program OTP array is ignored, the write enable latch bit remains set, and flag status register bits 1 and 4 are set. If there is a need to unlock the OTP, Volatile register 8, bit 2, can be set to "0" to override the OTP control byte lock bit.	

OTP READ (4Bh)

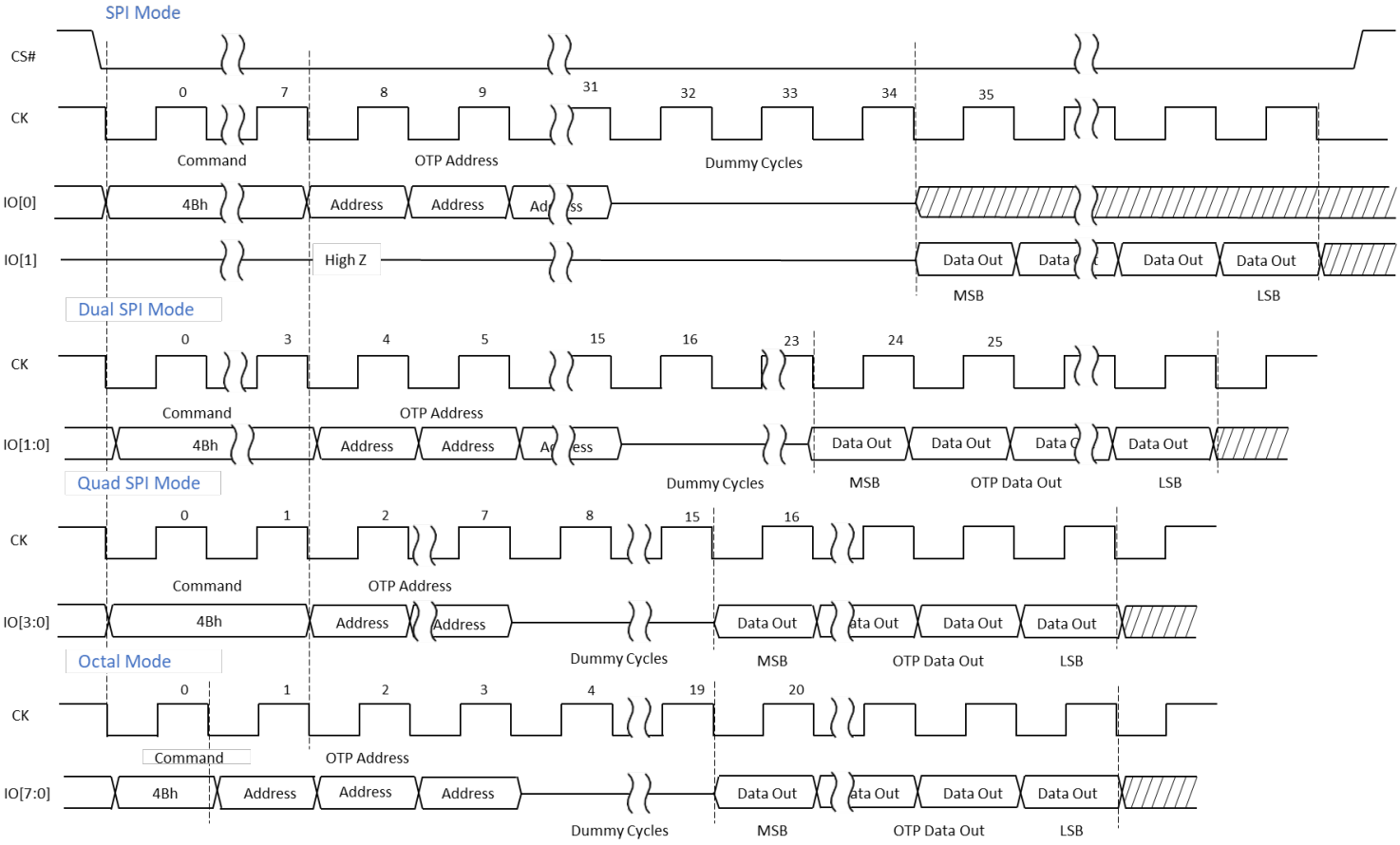


Figure 30

15. Extended Address Operation

Extended Address operation provides an extension of the 3-byte address range [A23: 0] to a 4-byte range [A31:0]. This allows the addressability to be extended from 128Mb to 256Mb. Selection of the 3-byte or 4-byte address range can be enabled in two ways: 1) through the nonvolatile and volatile configuration register or 2), through the 4-BYTE ADDRESS MODE ENTER/EXIT commands. Each address bit is latched in during the rising edge of the clock. The addressed byte can be at any location, and the address automatically increments to the next address after each byte of data is shifted out; With 4-byte enabled, a 256Mb device can be read with a single command.

4-BYTE commands function in 4-BYTE protocol regardless of settings in the nonvolatile configuration register; other commands function in 4-BYTE protocol only after the specific protocol is enabled by the register settings.

WRITE operations can be extended to a 4-byte address range, with [A31:0] input during the address cycle.

Operation Name	Description
4-BYTE MODE ENTER (B7h)	This enables address length of 32 bits for the memory area needed for density larger than 128Mb. The default is 24-bit address mode. The Flag Status register bit 0 will be set to 1 to indicate the 4-byte address mode has been enabled. Once the 4-byte mode is enabled, the address length becomes 32 bits instead of the default 24 bits.
4-BYTE MODE EXIT (E9h)	The 4-byte mode exit will disable 4-byte mode. Reset or Power-off will also disable 4-byte mode. The Flag Status register bit 0 will be reset to 0 to indicate a return to the 3-byte address mode.

4-Byte Mode Enter (B7h)/ Exit (E9h)

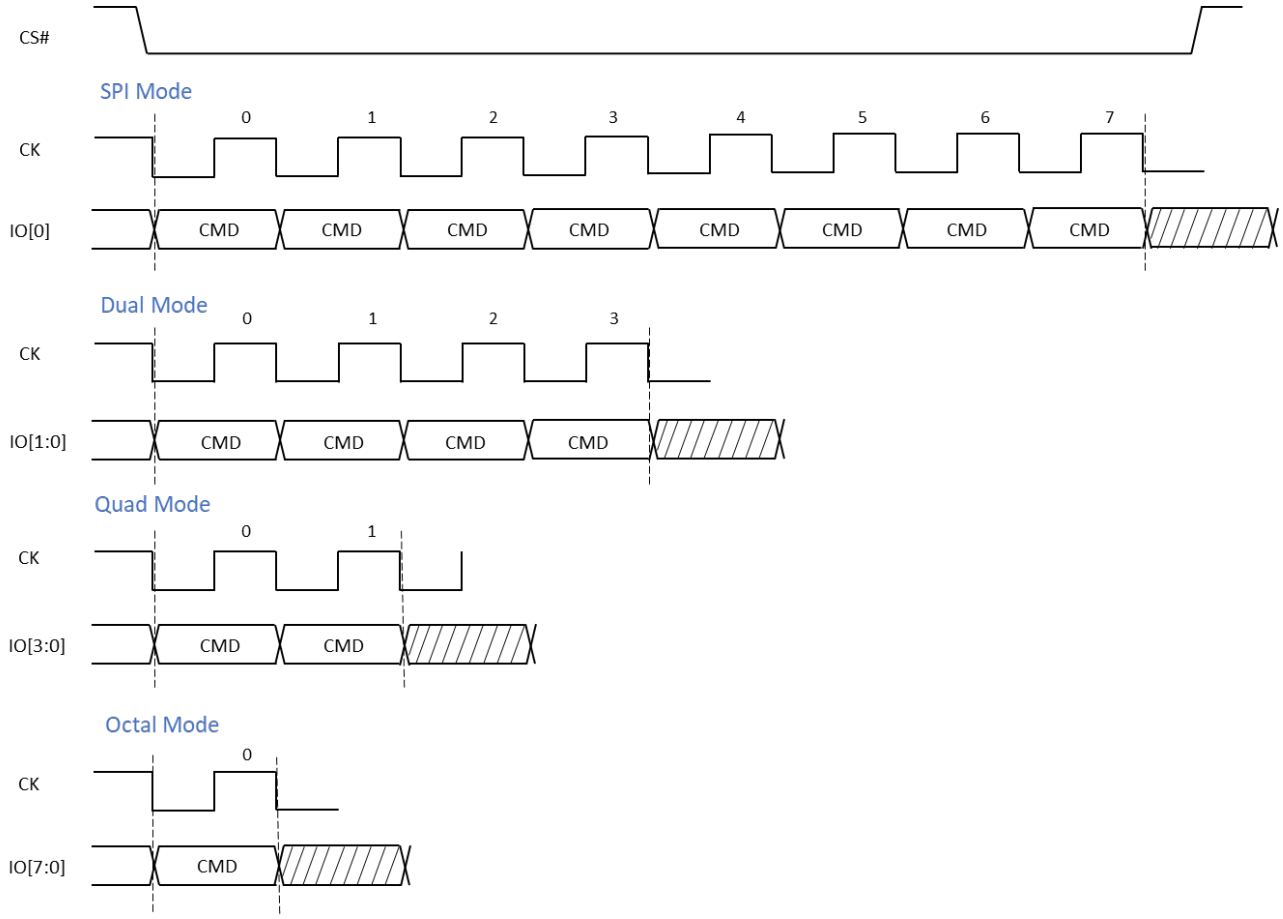


Figure 31 4-BYTE Enter/Exit

4-BYTE COMMANDS

The following commands will enable extended address operation regardless of the Nonvolatile Configuration Register setting. These commands operate in the same manner as their 3-byte mode equivalents, but the address cycle portion of the command input must comprehend the added clock cycles need to accommodate the 4-byte address. Other commands function in the 4-byte mode only after the protocol is enabled by the register setting.

4-BYTE Command	OPCODE (HEX)
Read 4-byte address	13
Read Fast 4-byte address	0C
Read Fast DTR 4-Byte Address	0E
Read Fast Quad I/O DTR 4-Byte Address	EE
Read Fast Octal Output 4-byte address	7C
Read Fast Octal I/O 4-byte address	CC
Write (Program) 4-byte address	12
Write (Program) Fast Quad Input 4-byte	34
Write (Program) Fast Quad Input Extended 4-byte	3E
Write (Program) Fast Octal Input 4-byte	84

Write (Program) Fast Octal Input Extended 4-byte	8E
Erase Sector 4-byte address	DC
Erase 4kB 4-byte address	21
Erase 32kB 4-byte address	5C

READ 4-Byte Address Command - showing the 32 bit address clock timing

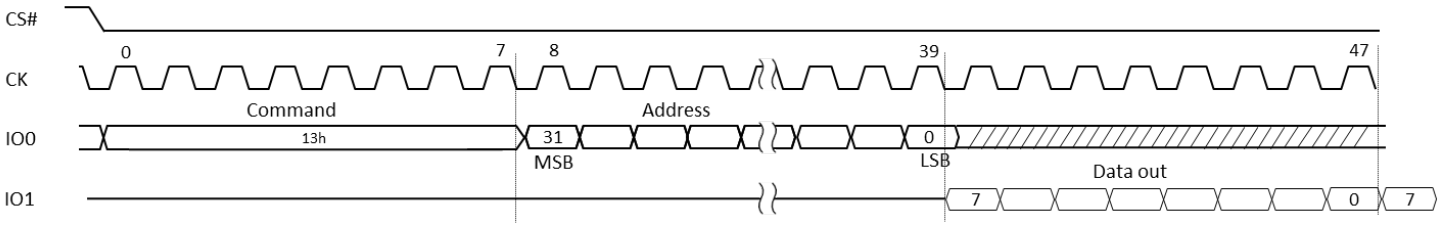


Figure 32

16. Deep Power Down Operation

Executing the Deep Power Down Enter command will put the device in the lowest power consumption mode . In this mode the device ignores all Write (Program) and Erase commands which can serve as a software protection mode while the device is not in use. In Deep Power Down mode all commands are ignored except Deep Power Down Exit, Reset Enable, and Reset. These commands will release the device from Deep Power Down mode.

The Deep Power Down Mode automatically stops at Power-down. The device is in the Standby Mode after Power-up. Any Deep Power-Down (DP) command while an Erase or Write cycle is in progress is rejected without having any effects on the cycle that is in progress.

The Deep Power Down Exit (Abh) is used to release the device from Deep Power down mode. Release from Power Down will take the time duration of tRDP before the device will resume normal operation and other commands are accepted. The CS# pin must remain high during the tRDP time duration. The device is also released from Deep Power mode with a Power-down, a hardware or software Reset.

Operation Name	Description
Deep Power Down Enter (B9h)	This command is used to have the device enter deep power down and reduce the power, after a specified time, tDP, to the level of IDD2.
Deep Power Down Exit (Abh)	This command will cause the device to exit the deep power down mode and return to normal operation after a specified time, tRDP.

Deep Power Down Enter (B9h)

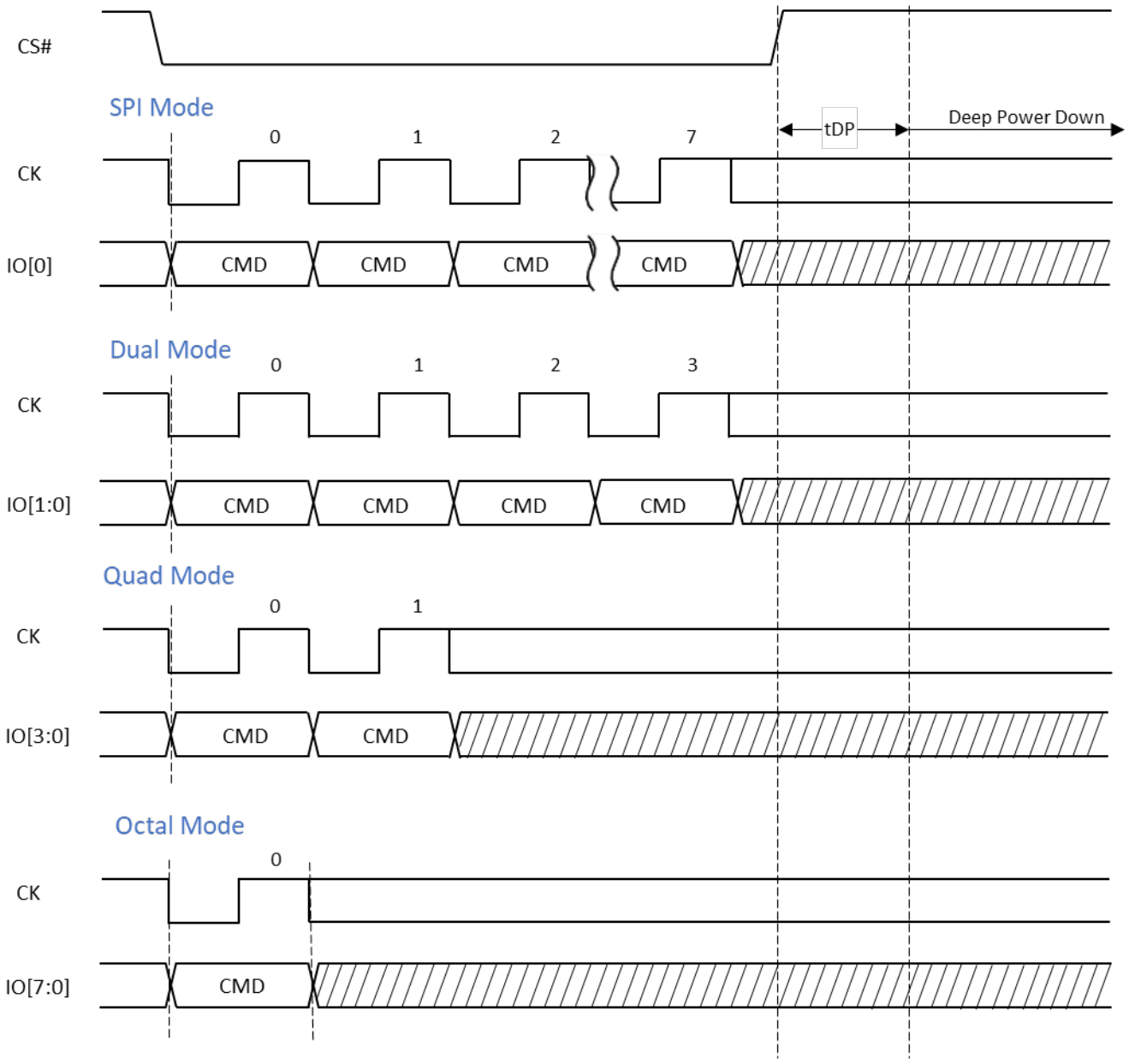


Figure 33 Deep Power Down Enter

Deep Power Down Exit (Abh)

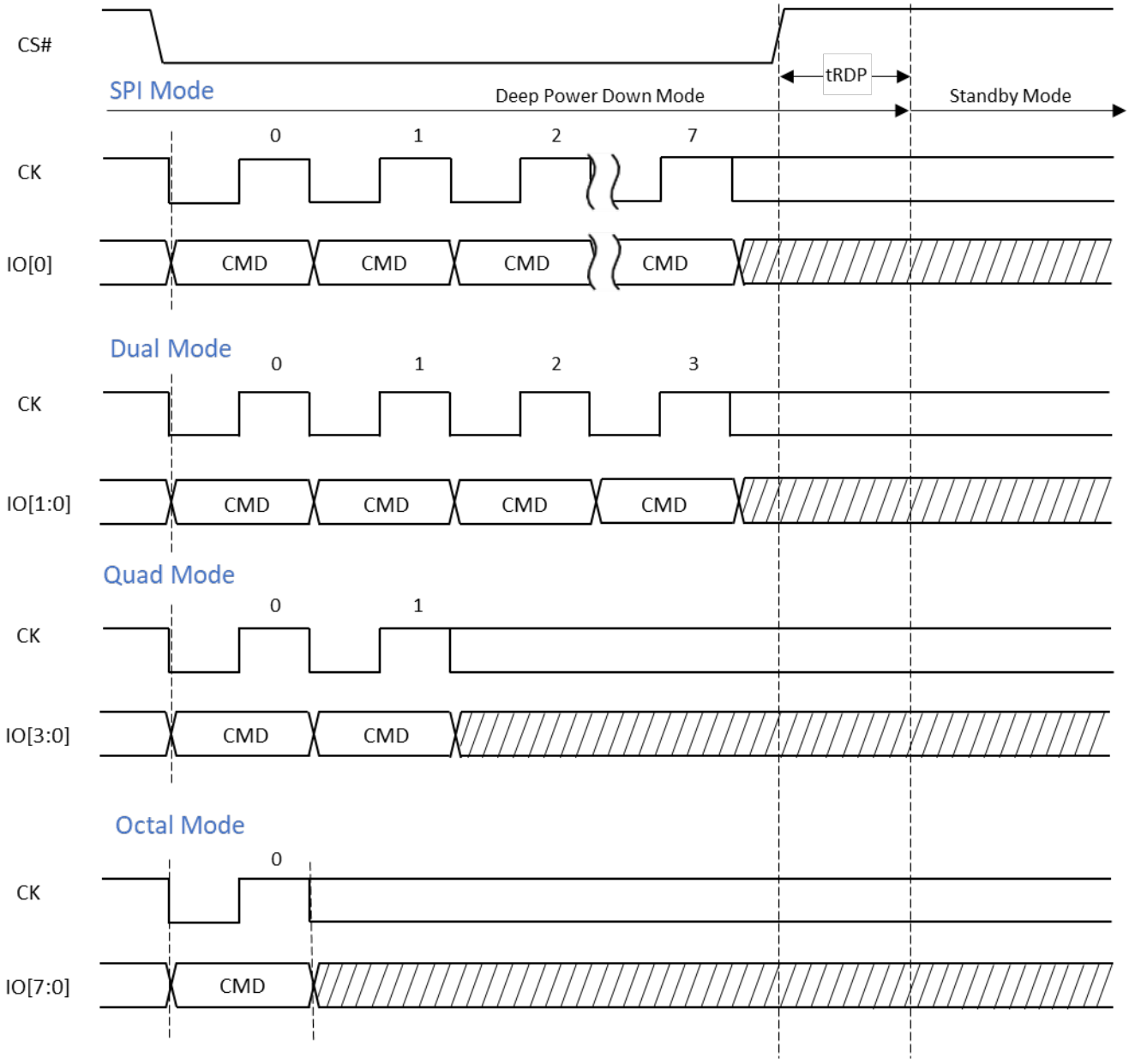


Figure 34

17. Initialization Considerations

Please refer to Everspin Application Note EST 3000, *Device Initialization, Power Cycle, System Reset and Recovery for EMxxLX MRAM.*

18. Reset Operations

The device may be reset in hardware by enabling the RESET# signal or in software by the Reset Enable and Reset Memory commands. As described in section 3, Signal Descriptions, The RESET# signal is available on the 24-BGA package on ball A4 and is a shared signal with IO3 on the 8-DFN package on pin 7. In the 8-DFN package RESET# is available only in SPI or Dual SPI modes since it is shared with IO3. (IO3 is needed as an input/output pin in Quad SPI mode).

18.1 Software Reset

Operation Name	Description
RESET Enable (66h)	To reset the device in software, the **RESET Enable** command is issued, followed by the **RESET Memory** command. The device then enters a power-on reset condition. The CS# deselect time tSHSL3 must be observed between commands. The volatile configuration register, status registers, and CRC are reset to the power-on reset default condition according to nonvolatile configuration register settings. It is recommended to exit XIP mode before executing these two commands. If a reset is initiated while a WRITE, PROGRAM, or ERASE operation is in progress, the operation is aborted, and data may be corrupted. Reset will be effective after the flag status register bit 7 outputs 1 (Ready) . A **RESET Enable** command is not accepted during WRITE STATUS REGISTER and WRITE NONVOLATILE CONFIGURATION REGISTER operations.
RESET Memory (99h)	

Reset Enable and Reset Memory

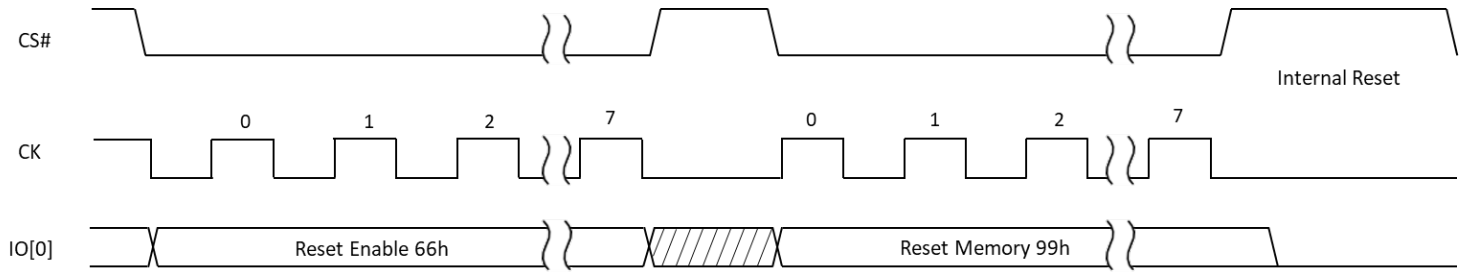


Figure 35 Software Reset

18.2 HARDWARE RESET

A hardware reset is initiated by bringing RESET# low when CS# is high.

Parameter	Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
Hardware RESET	^{t}SHRL		60	–	–	ns	
Hardware RESET recovery time	^{t}RHSL		40	–	–	ns	
Hardware RESET pulse width	^{t}RLRH		100	–	–	ns	

Table 24 Hardware Reset Timing

A hardware reset will reset Volatile configuration registers, extended address register, CRC and status registers, and erase, read, write, or program, and a register write in progress.

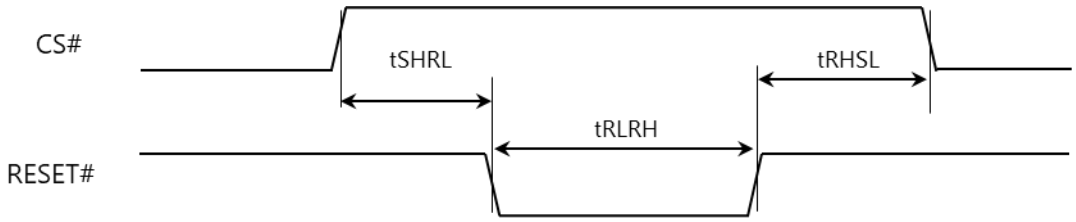


Figure 36 Hardware Reset Timing

Note: A Hardware Reset is only allowed when CS# is high to avoid potential data corruption. IO3 and RESET# share a common pin, Pin 7, in part numbers using the DFN package. Steps should be taken to ensure that data on IO3 does not induce a RESET when CS# is brought high. Under SPI mode configuration, while using a command that changes the mode to Quad SPI "on-the-fly", such as Read Fast Quad Output, a low state on Pin 7 may result, IO3, when CS# is brought high. It is important to ensure that IO3/RESET# is brought high before CS# goes low to avoid an unintended hardware reset.

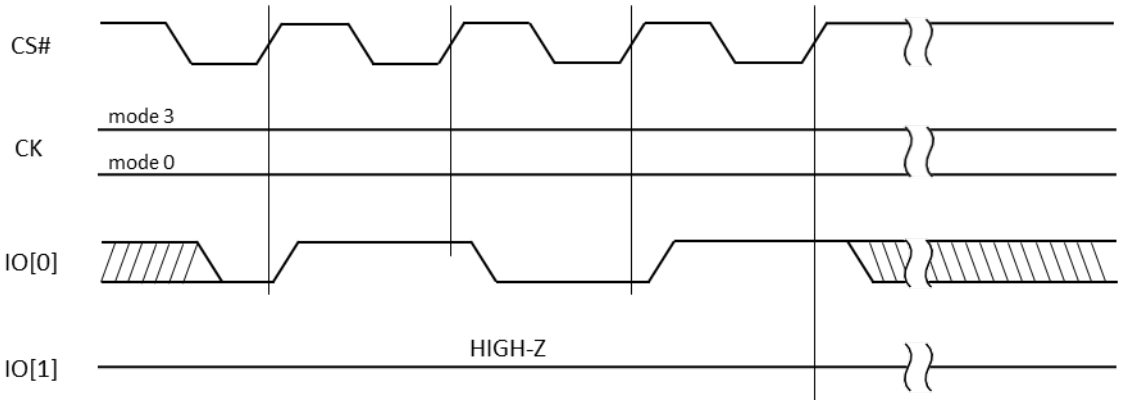
18.3 RESET WITH SIGNAL SEQUENCE

The device may be reset in hardware by sequencing CS#, CK# and IO0 in a specific manner shown below which follows the JESD252 procedure for Serial Flash Reset Signaling Protocol. Use this Reset if the controller and memory device configuration is believed to be out of synchronization. The following items are reset: Device control logic and internal registers are reset. The device will be configured as follows: SPI Mode with DS, 3-Byte Address Mode, DCC setting = 0 (16 dummy cycles), XIP Mode = Off, Wrap = Off, Memory Mode = Persistent Memory Mode, Erase Value = '1'.

The following operations will not be reset:

Erase in progress
CRC check in progress
Non-Volatile or Volatile Registers (left unchanged and user can read out to recover any previously written configuration if so desired)

The Non-Volatile and Volatile Registers should be reconfigured to desired values after JESD Reset. After JESD Reset the device is in a known state and user can issue a Hard or Soft Reset if so desired.



Note: CK should be kept stable high (mode 3) or low (mode 0) to prevent any confusion with commands

Figure 37 Reset with Signal Sequence (JESD 252)

19. Tuning Data Pattern

The EMxxLX provides a tuning technique to align the Data Strobe to ensure IO timing accuracy which is useful for higher speed operation. A fixed tuning data pattern(TDP) is programmed in the device which can be used to tune the system data output receiver with a known pattern. A custom pattern can be written and stored in the device as well. Please refer to Everspin application note EST 3001 for details of using the TDP function.

20. Cyclic Redundancy Check (CRC) Operation

A CYCLIC REDUNDANCY CHECK (CRC) operation is designed to detect accidental changes to user data. The CRC-enabled memory calculates a short, fixed-length binary sequence, known as the CRC code for each block of data. CRC can be a higher performance alternative to reading data directly in order to verify recently programmed data. CRC can be used to periodically check the data integrity of a large block of data against a stored CRC reference over the life of the product. No system hardware changes are required to enable CRC. The CRC-64 operation follows the ECMA standard.

The CRC operation generates the CRC result of the entire memory space or of an address range specified by the operation. The CRC result is then compared with the expected CRC data provided in the sequence. The memory indicates a pass or fail with bit 3 of the Flag Status Register. If the CRC fails, it is possible to take corrective action such as verifying with a normal read mode or by rewriting the array data. CRC operation supports CRC data read back when CRC check fails; the CRC data generated from the target address range or entire device will be stored in the general purpose register (GPR) only when CRC check fails, and it can be read out through the GPR read sequence with command 96h, least significant byte first. GPR is reset to default all 0 at the beginning of the CRC operation, and so the user will read all 0 if CRC operation passes. Note that the GPR is a volatile register. It is cleared to all 0 on power-up and hardware/software reset. Read GPR starts from the first location and when clocked continuously will output 00h after location 64. The CYCLIC REDUNDANCY CHECK operation command sequences are shown in the tables below, for an entire memory space or for a selected address range. In the case of a selected address range, 3 bytes of address, bytes 12, 13, and 14, are sufficient to select a given range. For devices for which there is more than one die in the package and that utilize the Die Select command, the CRC address range works in conjunction with the selected die to check the proper address range.

The CRC is initiated after CS# is driven high at the end of the command sequence. The status of the CRC can be checked in the Interrupt Status register bit 1. Bit 1 = 0 is CRC not complete, 1 = CRC Done. This interrupt is maskable, refer to Bit 1 in the Interrupt Mask register.

CRC operation on 8Mb, 16Mb and 32Mb part numbers may not be done on the entire memory space using modifier FFh in Byte 3 of the command sequence. For those part numbers, a CRC operation may only be done on a specified address range with modifier FEh (as seen in Table 26), however this range can cover the entire memory space if desired.

Command Sequence		Description
Byte#	Data	
1	9Bh	Command code for interface activation
2	27h	Sub-command code for CRC operation
3	FFh	CRC operation option selection (CRC operation on entire device)
4	CRC[7:0]	1st byte of expected CRC value
5–10	CRC[55:8]	2nd to 7th byte of expected CRC value
11	CRC[63:56]	8th byte of expected CRC value
CS# HIGH		Operation sequence confirmed; CRC operation starts

Table 25 Entire Memory Space

Command Sequence		Description
Byte#	**Data**	
1	9Bh	Command code for interface activation
2	27h	Sub-command code for CRC operation
3	FEh	CRC operation option selection (CRC operation on a range)
4	CRC[7:0]	1st byte of expected CRC value
5–10	CRC[55:8]	2nd to 7th byte of expected CRC value
11	CRC[63:56]	8th byte of expected CRC value
12	Start Address [7:0]	Specifies the starting byte address for CRC operation
13–14	Start Address [23:8]	
15	Not used	
16	Stop Address [7:0]	Specifies the ending byte address for CRC operation
17–18	Stop Address [23:8]	
19	Not used	
CS# HIGH		Operation sequence confirmed; CRC operation starts

Table 26 Specific Address Range

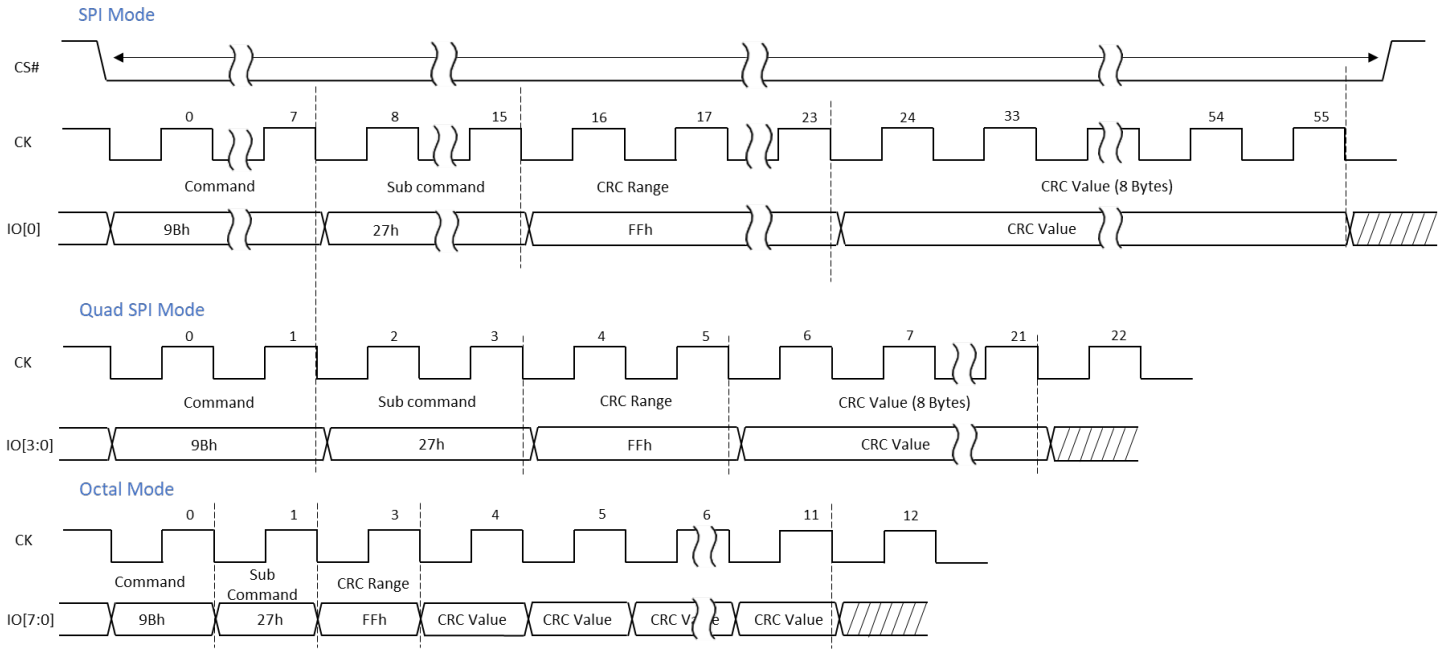
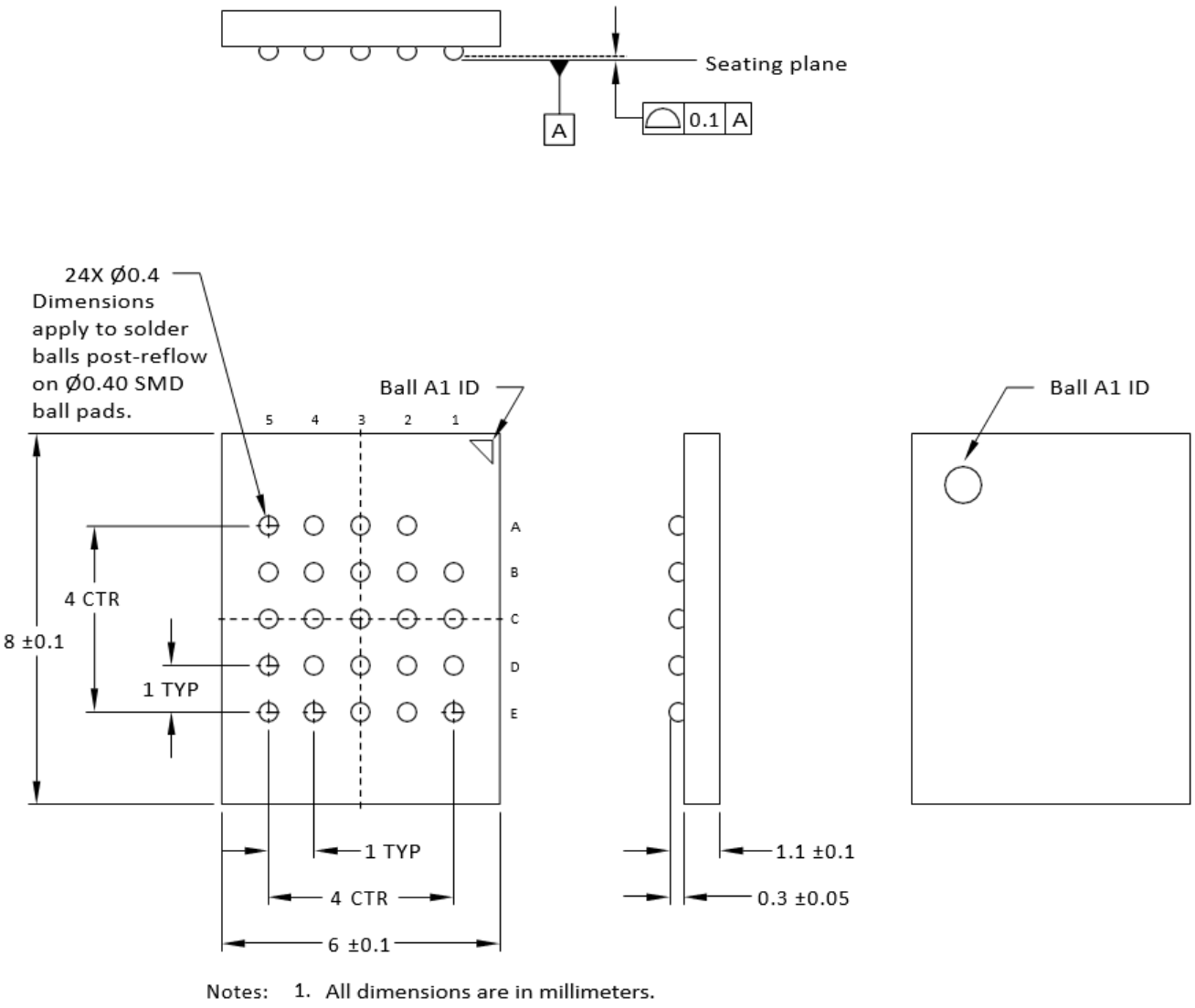


Figure 38 CRC Operation with full range selected (FF) using STR

Notes: 1. Waveform in Fig 38 is for Command 9Bh, full memory CRC using STR timings .Command 9Bh with a selected range requires the input of start and stop addresses to define the CRC range following the CRC Value bytes as described in Table 26.

21. Package Information

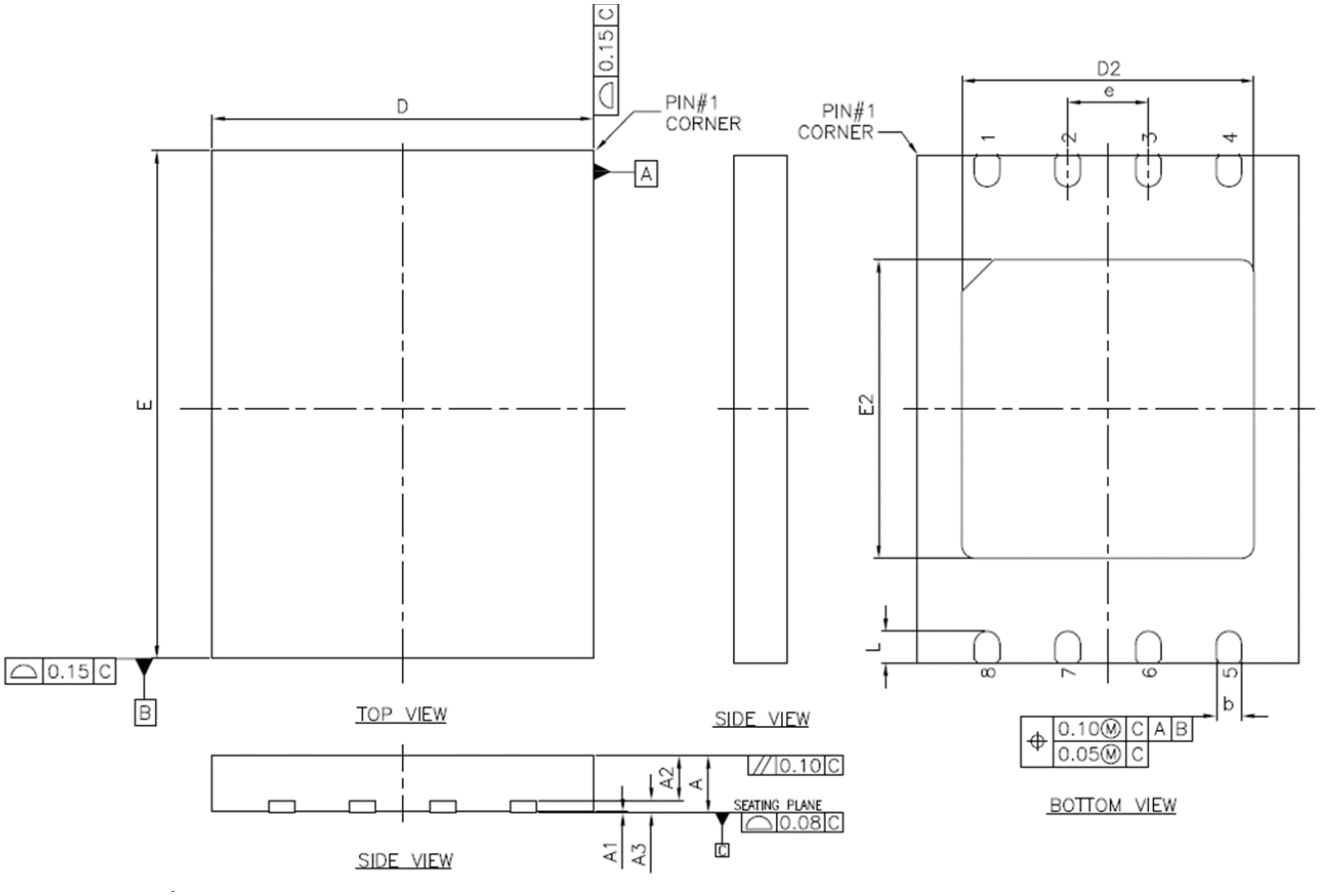
24-Ball TBGA, 5 x 5 ball array



Notes: 1. All dimensions are in millimeters.

Figure 39

8-PIN DFN PACKAGE



	Symbol	Min.	Nom.	Max.
Total thickness	A	0.85	0.90	0.95
Standoff	A1	0.00	0.02	0.05
Mold thickness	A2	0.65	0.70	0.75
Lead thickness	A3		0.20 REF	
Body Size	D	5.90	6.00	6.10
	E	7.90	8.00	8.10
Lead width	b	0.35	0.40	0.48
Exposed pad width	D2	4.55	4.60	4.65
Exposed pad length	E2	4.65	4.70	4.75
Lead pitch	E		1.27 BSC	
Lead length	L	0.45	0.50	0.55
Lead count	N		8L	

THIRD ANGLE PROJECTION	
UNLESS OTHERWISE SPECIFIED DECIMAL: .X ± .XX ± .10 .XXX ± .05	
ANGULAR ± 3°	
SCALE: 15:1	
JEDEC NO.: MO-229(REF.)	
DWG. NO.: PD-PR23 (OSE)	REV.: A

Figure 40

Initial Delivery State

The device is delivered to the customer in the following state

- **Memory array**: entire array is erased with all the bits set to 1 i.e. each byte contains 0xFF
- **Status Registers**: All the status register have value of 0x00
- **Non-Volatile Registers**: All the non-volatile configuration registers are erased and set to 0xFFFF

Important Note: The device is delivered with the memory array erased but after the assembly reflow process the memory array may need to be re-initialized. To ensure a known state of the device, please follow the procedure shown in Application Note EST 3000, *Device Initialization, Power Cycle, System Reset and Recovery for EM064LX MRAM*, at the factory after solder reflow.

22. Electrical Specifications and Operating Conditions

22.1. Power-On Timing

During initial power up or when recovering from brownout or power loss, a power up delay time (tPU) must be added to the time required for voltages to rise to their specified minimum voltages (V_{DD}(min)) before normal operations may commence. This time is required to ensure that device internal voltages have stabilized. Power up time, tPU is measured from the time that V_{DD} has reached the specified minimum voltage. See "Figure xx – Power-Up Timing" for an illustration of the timing.
During initial startup or power loss recovery, the CS# pin should always track V_{DD} or V_{IH}, whichever is lower, and remain high for the total startup time, tPU. In most systems, this means that CS# should be pulled up to V_{DD} with a resistor. Any logic that drives other inputs or Ios should hold the signals at VDD until normal operation can commence. To provide protection for data during initial power up, power loss or brownout, whenever VDD falls below VWI, the device cannot be selected (CS# must remain high), the device is inhibited from Read or Write operations, and a device reset is initiated.

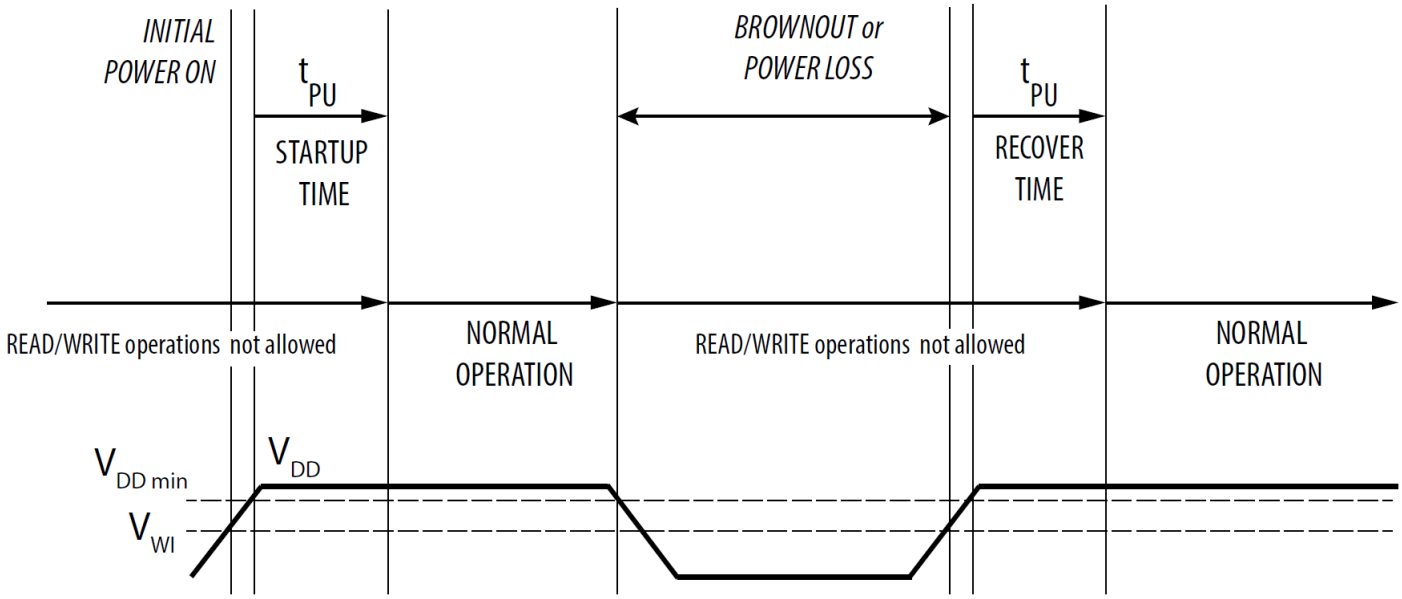


Figure 41

Note: CS# may not be enabled until tPU startup or recover time is met.

Symbol	Parameter	Min	Max	Unit	Notes
V_{WI}	Reset voltage	1.0	1.5	V	-
t_{PU}	V_{DD} (min) to device operation	300		µS	-

Table 27

23.2 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_{STG}	Storage Temperature	-65	150	ºC	-
T_{LEAD}	Storage Temperature	-	See Note 3	ºC	3

V_{IO}	I/O Voltage (reference to ground)	-0.6	V_{DD}+0.6	V	1, 2
V_{DD}	Supply voltage	-0.6	2.4	V	1, 2
V_{ESD}	Electrostatic discharge voltage (human body model)	-2000	+2000	V	1, 2
H_{max}	Maximum Magnetic Field during read/write operation		350	Oe	4,5

Table 28

Notes:
1. All specified voltages are with respect to ground (Vss)
2. JEDEC Standard JESD22-A114A (C1 = 100pF, R1 = 1500Ω, R2 = 500Ω
3. Compliant with JEDEC Standard J-STD-020C (for small-body, Sn-Pb or Pb assembly), RoHS, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
4. Device characterized with a magnet positioned above the package with the magnetic field at 90° to surface for a time of 10 seconds. Magnetic field immunity is affected by many factors such as device operating state, distance from the package surface, length of exposure, and angle of the field. Please refer to Everspin Application Note 3004 for further details.
5. Magnetic field immunity is higher, >1000 Oe, while device is in Standby or Read operations.

23.3 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Supply voltage	1.65	2.0	V	-
T_A	Ambient operating temperature (Commercial range)	0	70	°C	-
T_A	Ambient operating temperature (Industrial range)	–40	85	°C	-

Table 29

23.4 Device Pin Loading

Symbol	Parameter	Min	Max	Unit	Notes
$C_{IN/OUT}$	**I/O capacitance (IO0-IO7)**				
	8Mb to 64Mb	–	8	pF	4
C_{IN}	**Input capacitance (other pins)**				
	8Mb to 64Mb	–	6	pF	4
$C_{IN(CS\#)}$	**Input/Chip select capacitance**				
	8Mb to 64Mb	–	10	pF	4
C_L	**Load capacitance**				
	8Mb to 64Mb	–	12	pF	4

Table 30

Notes:
6. These parameters are verified by design and characterization. The capacitance is measured according to JEP147 ("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)") with V_{DD} and V_{SS} applied and all other pins floating (except the pin under test), VBIAS = V_{DD}/2, TA = 25°C, Frequency = 200 MHz

23.5 AC Timing IO Conditions

A/C Timing I/O conditions

Symbol	Parameter	Min	Max	Unit	Notes
-	Input rise and fall times	–	1.5	ns	-
-	Input pulse voltages	$0.2V_{DD}$ to $0.8V_{DD}$		V	-
-	Input timing reference voltages	$0.3V_{DD}$ to $0.7V_{DD}$		V	-
-	Output timing reference voltages	$V_{DD}/2$		V	

Table 31

Notes:
These parameters are verified by design and characterization

AC Timing Input/Output Reference Levels

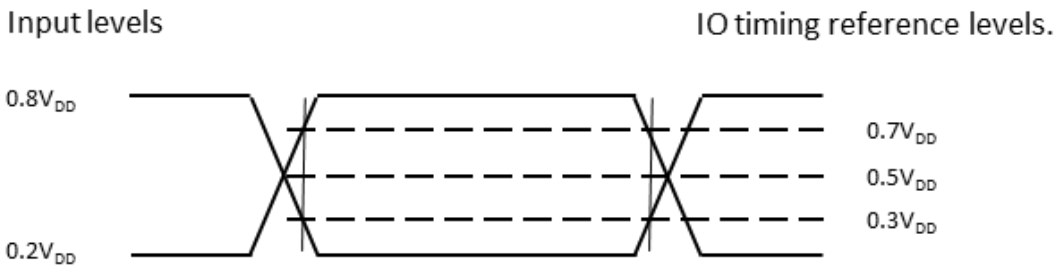


Figure 42

23.6 DC Current Characteristics and Conditions

Symbol	Parameter	Test Conditions	Typ	Max	Unit
I_{LI}	Input Leakage Current			±2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{DD1}	Standby Current	CS#=V_{DD}; V_{In} =V_{DD} or V_{SS}	300	1,330	µA
I_{DD2}	Deep Power-Down Current	CS#=V_{DD}; V_{IN}=V_{DD} or V_{SS}	290	1,210	µA
I_{DD3}	Operating Current (Read)	CK=0.1V_{DD} / 0.9V_{DD} at 200MHz (DTR), IO=Open(*1,*8 I/O)	124	161	mA
		CK=0.1V_{DD} / 0.9V_{DD} at 133MHz, IO=Open(*1,*8 I/O)	50	64	mA
I_{DD4}	Operating Current (Write)	CK=0.1V_{DD} / 0.9V_{DD} at 200MHz (DTR), IO=Open(*1,*8 I/O)	156	199	mA
		CK=0.1V_{DD} / 0.9V_{DD} at 133MHz, IO=Open(*1,*8 I/O)	59	78	mA

I_{DD5}	Operating Current(WRSR)	Execute Write Status Register command, then CS# = V_{DD}	8	13	mA
I_{DD6}	Operating Current (Erase Subsector or Sector)	Execute Erase, then CS# = V_{DD}	35	55	mA
I_{DD7}	Operating Current (Block Erase)	Execute Erase (4Kb, 32kB), then CS# = V_{DD}	29	48	mA
I_{DD8}	Operating Current (Chip Erase)	Execute Erase (Chip), then CS#=V_{DD}	33	50	mA

Table 32

Notes:

1. All currents are RMS unless noted. Typical values at typical V_{DD} (1.8V); V_{IO} = 0V/V_{DD}; T_C = +25°C.
2. Standby current is the average current measured over any time interval 5µs after CS de-assertion (and any internal operations are complete).
3. Deep power-down current is the average current measured over any 5ms time interval, 100µs after the ENTER DEEP POWER-DOWN operation (and any internal operations are complete).
4. All read currents are the average current measured over any 1KB continuous read. No load, checker-board pattern.
5. All write currents are the average current measured over any 256-byte typical data program.

23.7 DC Voltage Characteristics and Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		-0.5		0.2V_{DD}	V
V_{IH}	Input High Voltage		0.7V_{DD}		V_{DD}+0.4	V
V_{OL}	Output Low Voltage	IOL =100uA			0.4	V
V_{OH}	Output High Voltage	IOH =-100µA	V_{DD}-0.2			V

Table 33

23.8 AC Specifications

Parameter	Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
Clock frequency for READ command	^{f}R	STR	1	–	66	MHz	
Clock frequency for other commands SPI, Dual SPI and Quad SPI	$^{f}CK1$	STR	1	–	133	MHz	
		DTR	1		90		
Clock frequency for other commands Octal SPI	$^{f}CK2$	STR	1	–	200	MHz	
		DTR	1	–	200		
Clock HIGH time	^{t}CH	STR	45% (1/fCK)	–	–	ns	1
		DTR	45% (1/fCK)	–	–		
Clock LOW time	^{t}CL	STR	45% (1/fCK)	–	–	ns	1
		DTR	45% (1/fCK)	–	–		
Clock rise time (peak-to-peak)	$^{t}CLCH$	STR/DTR	0.1	–	–	V/ns	2, 3
Clock fall time (peak-to-peak)	$^{t}CHCL$	STR/DTR	0.1	–	–	V/ns	2, 3
CS# active setup time (relative to clock)	$^{t}SLCH$	STR/DTR	4	–	–	ns	
CS# not active hold time (relative to clock)	$^{t}CHSL$	STR/DTR	1	–	–	ns	
Data in setup time	$^{t}DVCH$	STR/DTR	0.5	–	–	ns	
	$^{t}DVCL$	DTR only	0.5	–	–	ns	
Data in hold time	$^{t}CHDX$	STR	0.5	–	–	ns	
		DTR	0.5	–	–	ns	
	$^{t}CLDX$	DTR only	0.5	–	–	ns	
CS# active hold time (relative to clock)	$^{t}CHSH$	STR	2.5	–	–	ns	9
		DTR	4.5	–	–		
CS# not active setup time (relative to clock)	$^{t}SHCH$	STR	2.5	–	–	ns	
		DTR	0.5	–	–	ns	9
CS# deselect time after a READ command	$^{t}SHSL1$	STR/DTR	50	–	–	ns	7
CS# deselect time after an incomplete or aborted command	tSHSL1i	STR/DTR	60	–	–	ns	6
CS# deselect time after a non-READ command	$^{t}SHSL2$	STR/DTR	60	–	–	ns	4,7
CS# deselect time after a Soft or Hard Reset.	$^{t}SHSL3$	STR/DTR	200	–	–	ns	
Output disable time	$^{t}SHQZ$	STR/DTR	–	–	6	ns	2
Data valid window	^{t}DVW	DTR	1.3			ns	
Clock LOW to output valid under 30pF	$^{t}CLQV$	STR/DTR	–	–	7	ns	10
Clock LOW to output valid under 10pF		STR/DTR	–	–	7	ns	
Clock HIGH to output valid under 30pF	$^{t}CHQV$	DTR only	–	–	7	ns	10
Clock HIGH to output valid under 10pF		DTR only	–	–	7	ns	
Output hold time	$^{t}CLQX$	STR/DTR	2	–	–	ns	
Output hold time	$^{t}CHQX$	DTR only	2	–	–	ns	

Parameter	Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
IO hold skew factor (12pF)	^{t}QHS	DTR only	_	_	0.4	ns	
IO valid skew related to DS (12pF)	^{t}DSQ	DTR only	_	_	0.4	ns	
Clock LOW to DS valid	^{t}CLDS	DTR only	-	-	7.5	ns	8
CRC check time: 64 KByte block	^{t}CRC	STR/DTR	–	2	–	ms	
CRC check time: full chip (64Mb)	^{t}CRC	STR/DTR	–	250	–	ms	
Write protect setup time	^{t}WHSL	STR/DTR	20	–	–	ns	5
Write protect hold time	^{t}SHWL	STR/DTR	100	–	–	ns	5
CS# HIGH to deep power-down	^{t}DP	STR/DTR	3	–	–	µs	
CS# HIGH to standby mode (DPD exit time)	^{t}RDP	STR/DTR	350	–	–	µs	
WRITE STATUS REGISTER cycle time	^{t}W	STR/DTR	–	–	1.5	µs	
WRITE NONVOLATILE CONFIGURATION REGISTER cycle time (per Address)	^{t}WNVCR	STR/DTR	–	–	1.5	µs	
PROGRAM OTP cycle time	^{t}POTP	STR/DTR	–	–	1.5	µs	
Sector erase time	^{t}SE	STR/DTR	–	–	960	µs	
4KB subsector erase time	^{t}SSE	STR/DTR	–	–	60	µs	
32KB subsector erase time	^{t}SSE	STR/DTR	–	–	500	µs	
64Mb bulk erase time	^{t}BE	STR/DTR	–	–	125	ms	
Power Up time to device accessible	^{t}PU		350	–	–	µs	

Table 34

Notes:

1. tCH+ tCL must add up to 1/ fCK
2. Value verified by characterization; not 100% tested.
3. Expressed as a slew rate.
4. Any non-READ command
5. Applicable as a constraint for a Write Status Register command when Status Register Write is set to 1.
6. Incomplete command occurs if CS# brought high prior to required timing.
7. tSHSL2 and tSHSL1 = 70ns when device is in Octal SPI, both STR and DTR mode.
8. DS will be driven after the first clock falling edge after CS# low.
9. In Quad SPI DTR mode, tCHSH=5.5ns min , tSHCH=5.5ns minimum
10. These specifications only apply when DS is disabled.

Serial Input Timing STR in SPI Mode

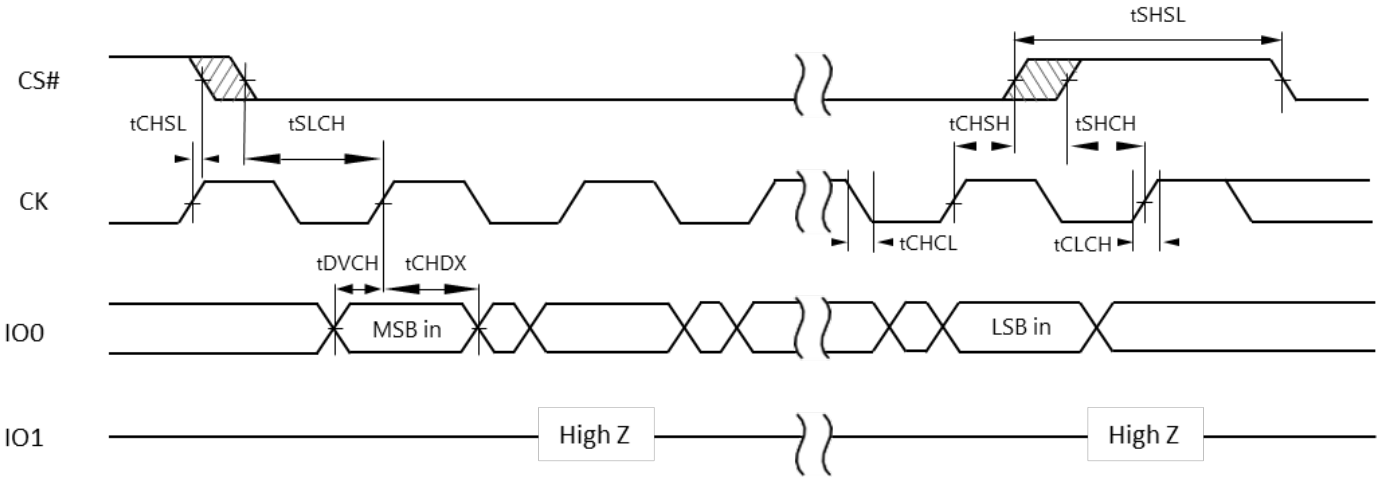


Figure 43

Serial Input Timing STR in Dual, Quad, and Octal SPI Modes

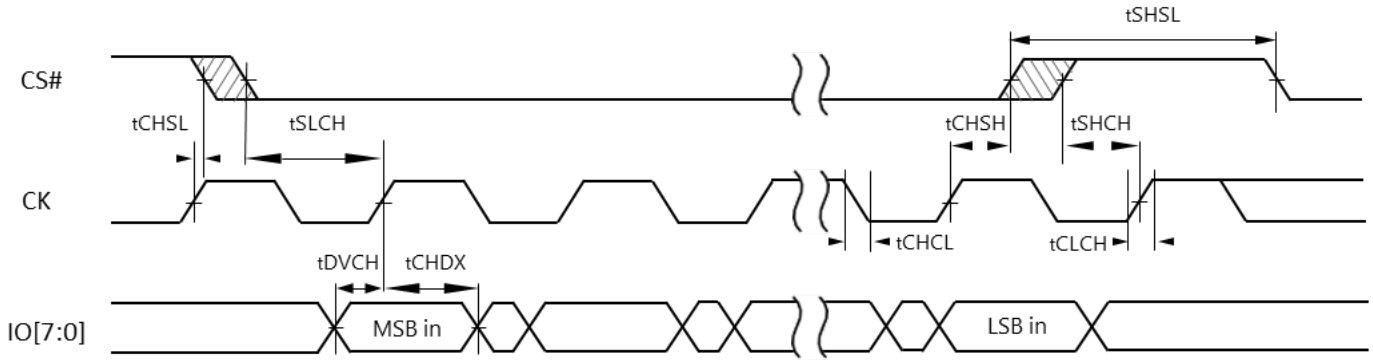


Figure 44

Serial Input Timing DTR in SPI Mode

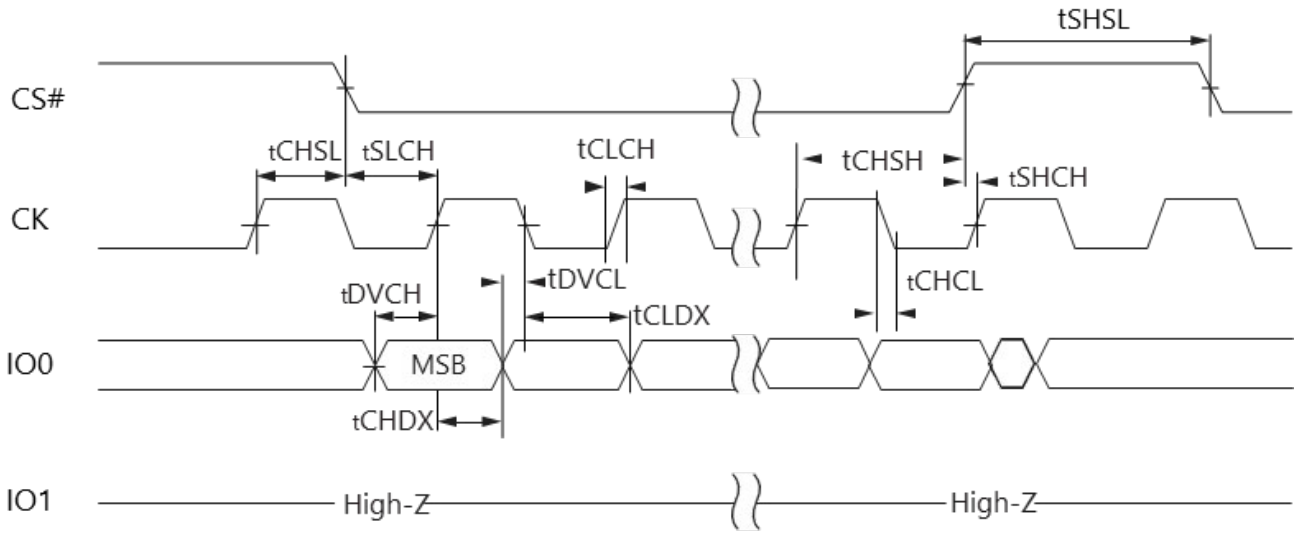


Figure 45

Serial Input Timing DTR in Dual, Quad, or Octal SPI Mode

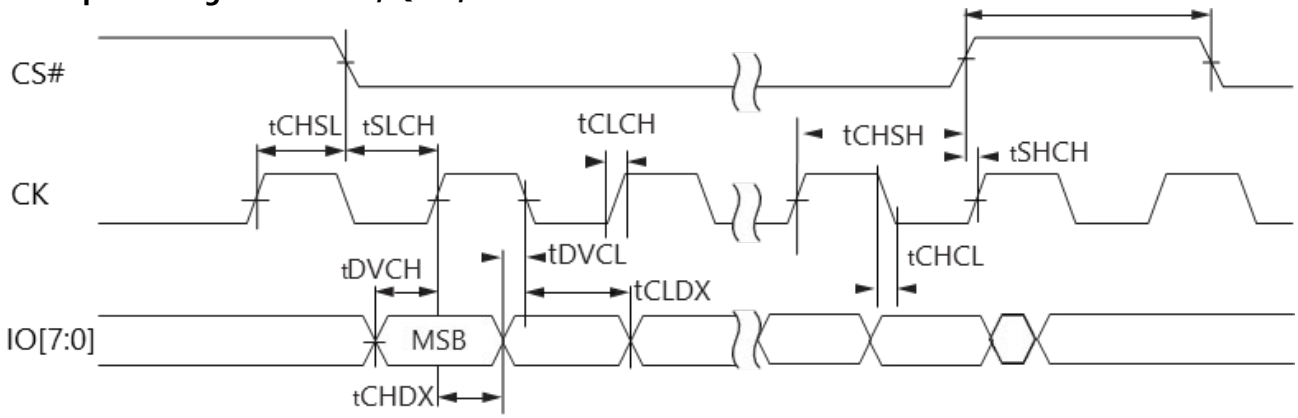


Figure 46

Serial Output Timing STR

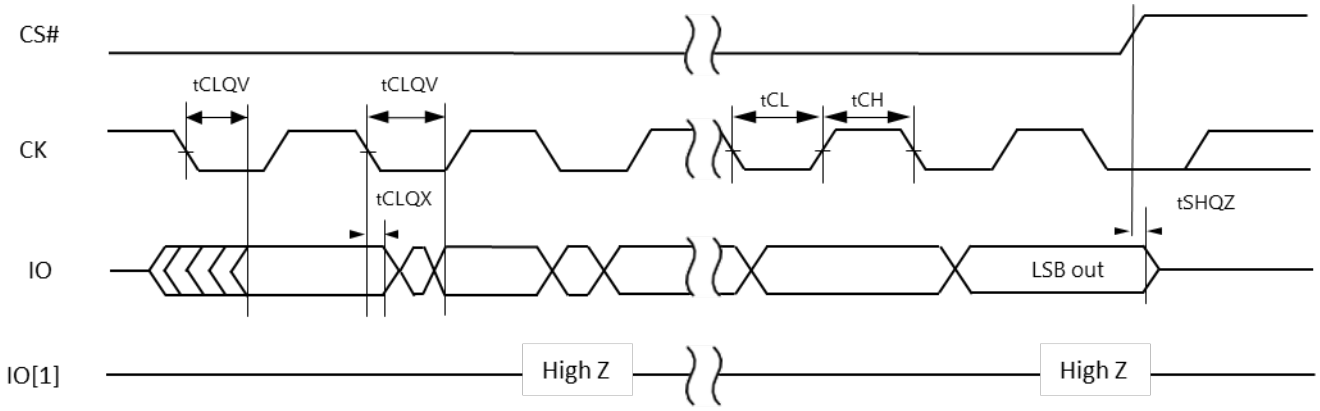


Figure 47

Serial Output Timing DTR

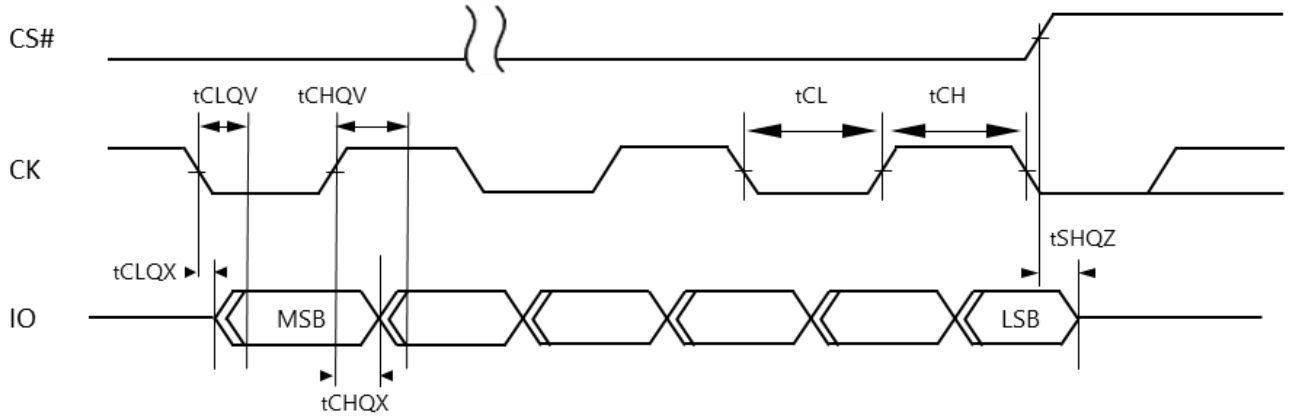


Figure 48

Data Strobe (DS) Timing

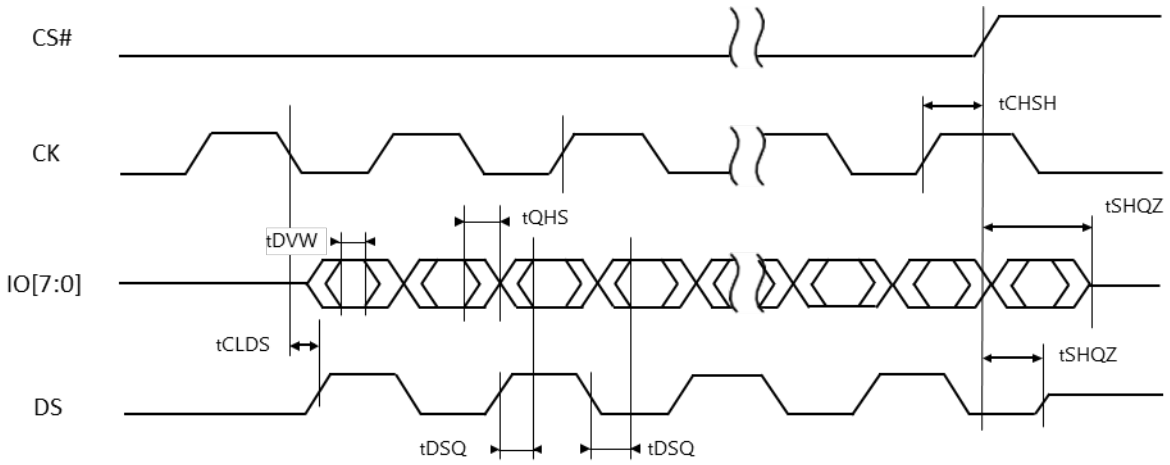


Figure 49

Note: The device should be deselected (CS# brought high) while CK is high to ensure that even counts of data are output. If not, the next IO or DS output may present on the output if CK goes low before CS# is high.

Write Protect Setup and Hold Timing during a Write Status Register Operation

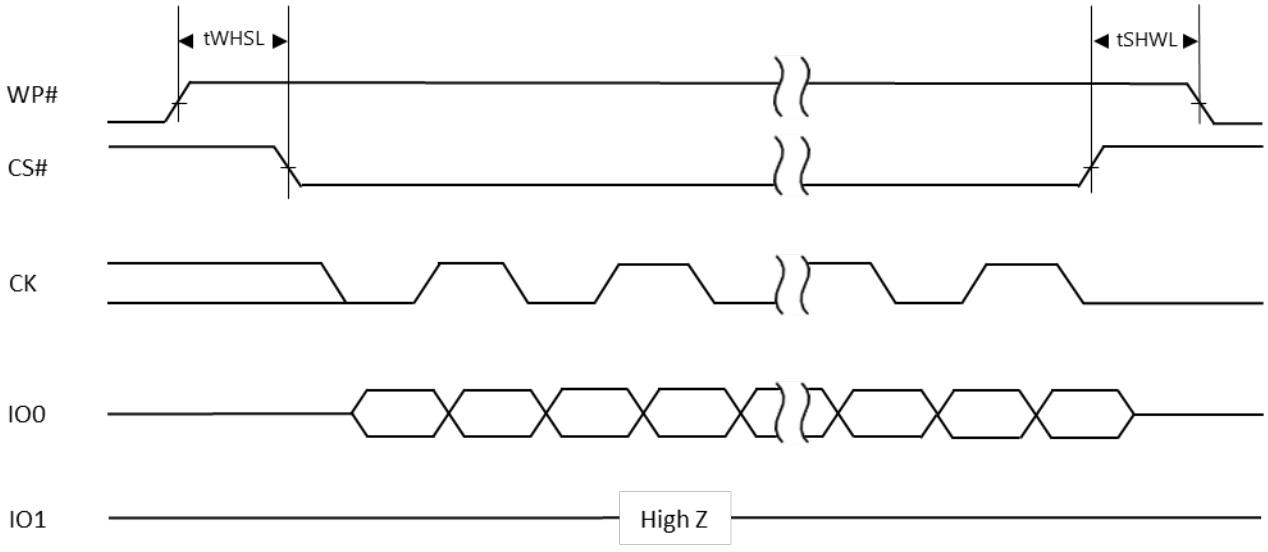


Figure 50

23. Orderable Part Numbers

Density	IO	Package	Temperature	Pack/Ship	OPN
8Mb	Quad	8-DFN	Commercial	Tray	EM008LXQADG13CS1T
				Tape and Reel	EM008LXQADG13CS1R
		24-BGA	Commercial	Tray	EM008LXQAB313CS1T
				Tape and Reel	EM008LXQAB313CS1R
		8-DFN	Industrial	Tray	EM008LXQADG13IS1T
				Tape and Reel	EM008LXQADG13IS1R
		24-BGA	Industrial	Tray	EM008LXQAB313IS1T
				Tape and Reel	EM008LXQAB313IS1R
	Octal	24-BGA	Commercial	Tray	EM008LXOAB320CS1T
				Tape and Reel	EM008LXOAB320CS1R
		24-BGA	Industrial	Tray	EM008LXOAB320IS1T
				Tape and Reel	EM008LXOAB320IS1R
16Mb	Quad	8-DFN	Commercial	Tray	EM016LXQADG13CS1T
				Tape and Reel	EM016LXQADG13CS1R
		24-BGA	Commercial	Tray	EM016LXQAB313CS1T
				Tape and Reel	EM016LXQAB313CS1R
		8-DFN	Industrial	Tray	EM016LXQADG13IS1T
				Tape and Reel	EM016LXQADG13IS1R
		24-BGA	Industrial	Tray	EM016LXQAB313IS1T
				Tape and Reel	EM016LXQAB313IS1R
	Octal	24-BGA	Commercial	Tray	EM016LXOAB320CS1T
				Tape and Reel	EM016LXOAB320CS1R
		24-BGA	Industrial	Tray	EM016LXOAB320IS1T
				Tape and Reel	EM016LXOAB320IS1R
32Mb	Quad	8-DFN	Commercial	Tray	EM032LXQADG13CS1T
				Tape and Reel	EM032LXQADG13CS1R
		24-BGA	Commercial	Tray	EM032LXQAB313CS1T
				Tape and Reel	EM032LXQAB313CS1R
		8-DFN	Industrial	Tray	EM032LXQADG13IS1T
				Tape and Reel	EM032LXQADG13IS1R
		24-BGA	Industrial	Tray	EM032LXQAB313IS1T
				Tape and Reel	EM032LXQAB313IS1R
	Octal	24-BGA	Commercial	Tray	EM032LXOAB320CS1T
				Tape and Reel	EM032LXOAB320CS1R
		24-BGA	Industrial	Tray	EM032LXOAB320IS1T
				Tape and Reel	EM032LXOAB320IS1R
64Mb	Quad	8-DFN	Commercial	Tray	EM064LXQADG13CS1T
				Tape and Reel	EM064LXQADG13CS1R
		24-BGA	Commercial	Tray	EM064LXQAB313CS1T
				Tape and Reel	EM064LXQAB313CS1R
		8-DFN	Industrial	Tray	EM064LXQADG13IS1T
				Tape and Reel	EM064LXQADG13IS1R
		24-BGA	Industrial	Tray	EM064LXQAB313IS1T
				Tape and Reel	EM064LXQAB313IS1R
	Octal	24-BGA	Commercial	Tray	EM064LXOAB320CS1T
				Tape and Reel	EM064LXOAB320CS1R
		24-BGA	Industrial	Tray	EM064LXOAB320IS1T
				Tape and Reel	EM064LXOAB320IS1R

Revision History

Rev	Date	Description
1.0	May 1, 2020	Preliminary datasheet first release.
2.5	April 27, 2022	Updates to Fig 48, DS timings updated, Table 10,11,19, XIP updated, removed Quad IO Entry and Exit command.
2.6	July 15, 2022	Based on WV 2.6 07062022. NDA required. Fig 12 updates. Table 34, AC Timings, updated tCHSH ,tSHCH, removed tCLSH. Fig 44, 45 updated. App note references updated. Fig 38 added for CRC waveform, GPRR renamed to GPR, Table 21 updated for CRC signals. PN EMxxLX used to reflect multiple densities.
2.7	September 9, 2022	Note 7 , Table 34 to include tSHSL2. Table 3 and Section 18.2 updated to advise on IO3/RESET# in DFN package. CRC operation for 8Mb, 16Mb and 32Mb part numbers is restricted, see note 8, Table 21.
2.8	October 1, 2022	Updated Sec.15 4-Byte commands list. Formatting on Read table in sec. 10. Added OPN table in Sec 23. Added Clear Flag Status command added to Sec 6.2. Quad SPI BGA package option added, Fig 3b; Table 1 note added to include NC of Quad SPI BGA option; Notes added in Sec 5.5 and 5.6 to include that Octal configs are not valid in Quad SPI options. Updated Table 32 for IDD1-7 parameters. Table 28 updated with Hmax.
2.9	December 21, 2022	Table 32 IDD values updated. Table 34 erase timings updated; tCRC, tW, tWNVCR, tPOTP updated. Volatile and Nonvolatile configuration register 4, DS delay, added. Table 28 Hmax specification updated.

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