THE DATASHEET OF

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RA2L1 Group
Renesas Microcontrollers

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Ultra low power 48 MHz Arm® Cortex®-M23 core, up to 256-KB code flash memory, 32 KB SRAM, Capacitive Sensing Unit (CTSU2), 12-bit A/D Converter, 12-bit D/A Converter, Security and Safety features.

Features

Arm Cortex-M23 Core

- Armv8-M architecture
- Maximum operating frequency: 48 MHz
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

Memory

- Up to 256-KB code flash memory
- 8-KB data flash memory (100,000 program/erase (P/E) cycles)
- 32 KB SRAM
- Memory protection units
- 128-bit unique ID

Connectivity

- Serial Communications Interface (SCI) × 5
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Simple IIC
  - Simple SPI
  - Smart card interface
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 2
- CAN module (CAN)

Analog

- 12-bit A/D Converter (ADC12)
- 12-bit D/A Converter (DAC12)
- Low-Power Analog Comparator (ACMPLP) × 2
- Temperature Sensor (TSN)

Timers

- General PWM Timer 32-bit (GPT32) × 4
- General PWM Timer 16-bit (GPT16) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

Safety

- ECC in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

Security and Encryption

- AES128/256
- True Random Number Generator (TRNG)

System and Power Management

- Low power modes
- Switching regulator
- Realtime Clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

Human Machine Interface (HMI)

- Capacitive Sensing Unit (CTSU2)

Multiple Clock Sources

- Main clock oscillator (MOSC) （1 to 20 MHz）
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (24/32/48/64 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock out support

Up to 85 pins for general I/O ports

- 5-V tolerance, open drain, input pull-up

Operating Voltage

- VCC: 1.6 to 5.5 V

Operating Temperature and Packages

- Ta = -40°C to +85°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 80-pin LQFP (12 mm × 12 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.50 mm pitch)
  - 48-pin HWQFN (7 mm × 7 mm, 0.50 mm pitch)
- Ta = -40°C to +105°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 80-pin LQFP (12 mm × 12 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.50 mm pitch)
  - 48-pin HWQFN (7 mm × 7 mm, 0.50 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M23 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 256-KB code flash memory
- 32-KB SRAM
- 12-bit A/D Converter (ADC12)
- 12-bit D/A Converter (DAC12)
- Security features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M23 core	• Maximum operating frequency: up to 48 MHz • Arm Cortex-M23 core: – Revision: r1p0-00rel0 – Armv8-M architecture profile – Single-cycle integer multiplier – 19-cycle integer divider • Arm Memory Protection Unit (Arm MPU): – Armv8 Protected Memory System Architecture – 8 protect regions • SysTick timer: – Driven by SYSTICCLK (LOCO) or ICLK

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256 KB of code flash memory.
Data flash memory	8 KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC).

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI boot mode
Resets	The MCU provides 13 resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator (IWDTLOCO) • Clock out support

Table 1.3 System (2 of 2)

Feature	Functional description
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Key Interrupt Function (KINT)	The key interrupt function (KINT) generates the key interrupt by detecting rising or falling edge on the key interrupt input pins.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt or watchdog timer reset.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.6 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 4 channels and a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state
Low power Asynchronous General Purpose Timer (AGT)	The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.

Table 1.6 Timers (2 of 2)

Feature	Functional description
Realtime Clock (RTC)	The RTC has two operation modes, normal operation mode and low-consumption clock mode. In each of the operation mode, the RTC has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.

Table 1.7 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 5 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
I^2C bus interface (IIC)	The I^2C bus interface (IIC) has 2 channels. The IIC module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has 2 channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.
Control Area Network (CAN)	The Controller Area Network (CAN) module uses a message-based protocol to receive and transmit data between multiple slaves and masters in electromagnetically noisy applications. The module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. The CAN module requires an additional external CAN transceiver.

Table 1.8 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter is provided. Up to 19 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
12-bit D/A Converter (DAC12)	A 12-bit D/A converter (DAC12) is provided.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.
Low-Power Analog Comparator (ACMPLP)	The Low-Power Analog Comparator (ACMPLP) compares a reference input voltage with an analog input voltage. Comparator channels ACMPLP0 and ACMPLP1 are independent of each other. The comparison result of the reference input voltage and analog input voltage can be read by software. The comparison result can also be output externally. The reference input voltage can be selected from either an input to the CMPREFi (i = 0, 1) pin or from the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption.

Table 1.9 Human machine interfaces

Feature	Functional description
Capacitive Sensing Unit (CTSU2)	The Capacitive Sensing Unit (CTSU2) measures the electrostatic capacitance of the sensor. Changes in the electrostatic capacitance are determined by software that enables the CTSU to detect whether a finger is in contact with the sensor. The electrode surface of the sensor is usually enclosed with a dielectric film so that a finger does not come into direct contact with the electrode.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows to monitor the access to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated.

Table 1.11 I/O ports

Feature	Functional description
I/O ports	• I/O ports for the 100-pin LQFP – I/O pins: 82 – Input pins: 3 – Pull-up resistors: 82 – N-ch open-drain outputs: 65 – 5-V tolerance: 5 • I/O ports for the 80-pin LQFP – I/O pins: 66 – Input pins: 3 – Pull-up resistors: 66 – N-ch open-drain outputs: 51 – 5-V tolerance: 5 • I/O ports for the 64-pin LQFP – I/O pins: 50 – Input pins: 3 – Pull-up resistors: 50 – N-ch open-drain outputs: 37 – 5-V tolerance: 5 • I/O ports for the 48-pin LQFP/HWQFN – I/O pins: 34 – Input pins: 3 – Pull-up resistors: 34 – N-ch open-drain outputs: 23 – 5-V tolerance: 4

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

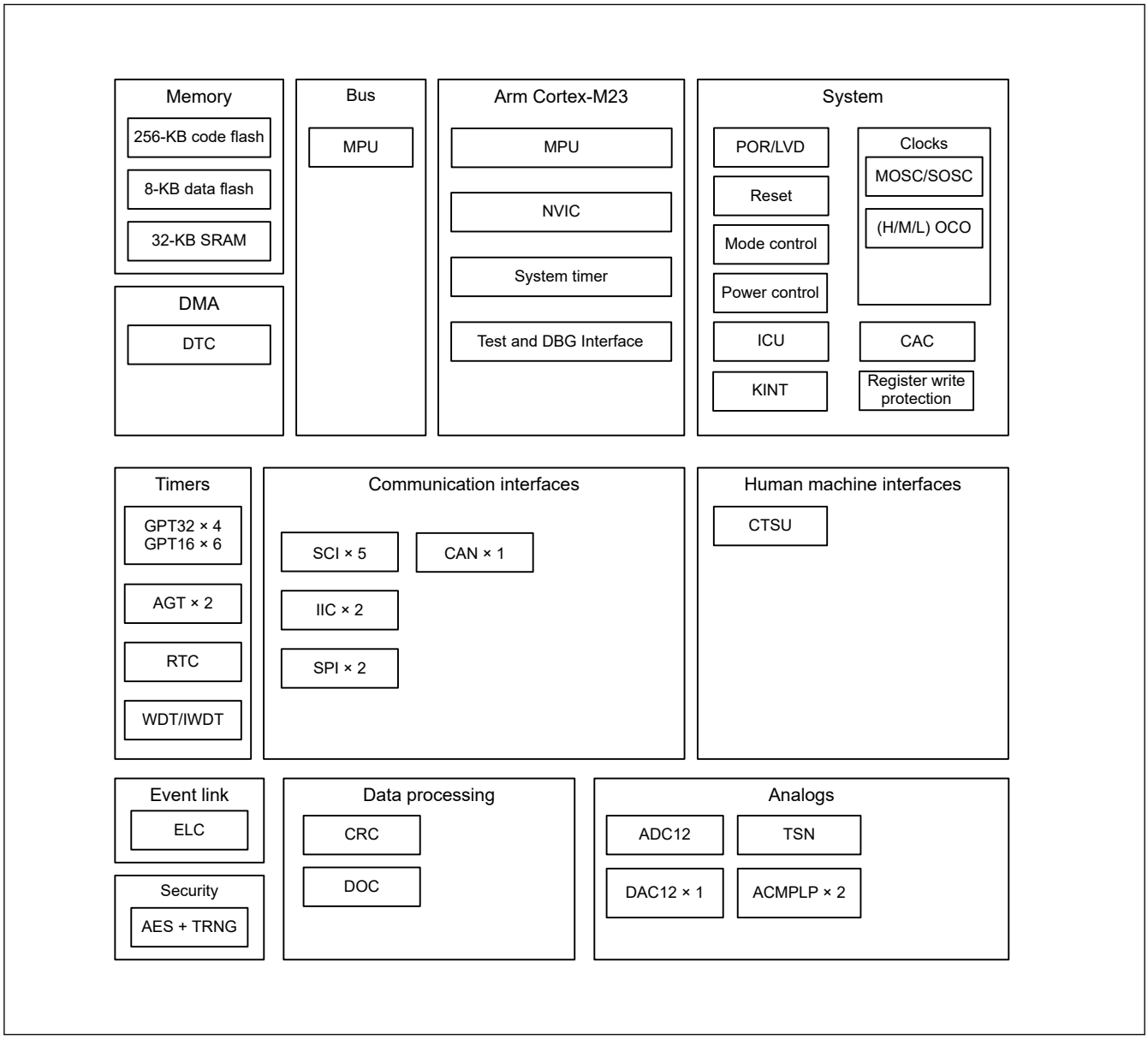


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

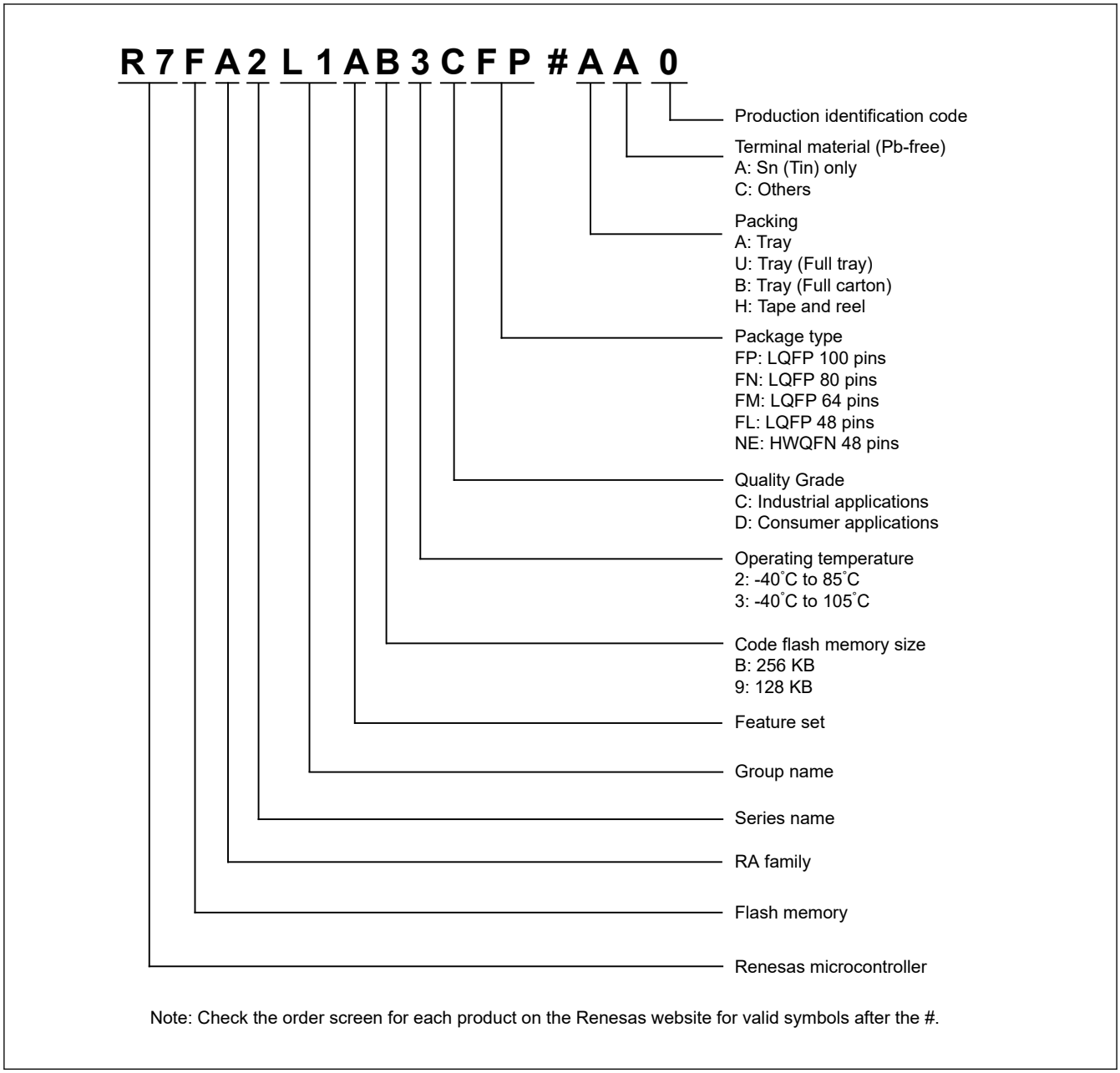


Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA2L1AB3CFP	PLQP0100KB-B	256 KB	8 KB	32 KB	-40 to +105°C
R7FA2L1AB3CFN	PLQP0080KB-B				
R7FA2L1AB3CFM	PLQP0064KB-C PLQP0064KL-A				
R7FA2L1AB3CFL	PLQP0048KB-B PLQP0048KL-A				
R7FA2L1AB3CNE	PWQN0048KC-A				
R7FA2L1AB2DFP	PLQP0100KB-B				-40 to +85°C
R7FA2L1AB2DFN	PLQP0080KB-B				
R7FA2L1AB2DFM	PLQP0064KB-C PLQP0064KL-A				
R7FA2L1AB2DFL	PLQP0048KB-B PLQP0048KL-A				
R7FA2L1AB2DNE	PWQN0048KC-A				
R7FA2L1A93CFP	PLQP0100KB-B	128 KB	8 KB	32 KB	-40 to +105°C
R7FA2L1A93CFN	PLQP0080KB-B				
R7FA2L1A93CFM	PLQP0064KB-C PLQP0064KL-A				
R7FA2L1A93CFL	PLQP0048KB-B PLQP0048KL-A				
R7FA2L1A93CNE	PWQN0048KC-A				
R7FA2L1A92DFP	PLQP0100KB-B				-40 to +85°C
R7FA2L1A92DFN	PLQP0080KB-B				
R7FA2L1A92DFM	PLQP0064KB-C PLQP0064KL-A				
R7FA2L1A92DFL	PLQP0048KB-B PLQP0048KL-A				
R7FA2L1A92DNE	PWQN0048KC-A				

1.4 Function Comparison

Table 1.13 Function comparison

Parts number		R7FA2L1A BxxFP	R7FA2L1A 9xxFP	R7FA2L1A BxxFN	R7FA2L1A 9xxFN	R7FA2L1A BxxFM	R7FA2L1A 9xxFM	R7FA2L1A BxxFL R7FA2L1A BxxNE	R7FA2L1A 9xxFL R7FA2L1A 9xxNE
Pin count		100		80		64		48	
Package		LQFP	LQFP	LQFP	LQFP	LQFP	LQFP	LQFP/QFN	LQFP/QFN
Code flash memory		256 KB	128 KB	256 KB	128 KB	256 KB	128 KB	256 KB	128 KB
Data flash memory		8 KB							
SRAM		32 KB							
	Parity	16 KB							
	ECC	16 KB							
System	CPU clock	48 MHz							
	Sub-clock oscillator	Yes							
	ICU	Yes							
	KINT	8						5	
Event control	ELC	Yes							
DMA	DTC	Yes							
Timers	GPT32	4							
	GPT16	6						3	
	AGT	2							
	RTC	Yes							
	WDT/IWDT	Yes							
Communication	SCI	5							
	IIC	2							
	SPI	2							
	CAN	Yes							
Analog	ADC12	19		17		13		9	
	DAC12	1							
	ACMPLP	2							
	TSN	Yes							
HMI	CTSU	32				30		20	
Data processing	CRC	Yes							
	DOC	Yes							
Security		AES and TRNG							
I/O ports	I/O pins	82		66		50		34	
	Input pins	3		3		3		3	
	Pull-up resistors	82		66		50		34	
	N-ch open-drain outputs	65		51		37		23	
	5-V tolerance	5		5		5		4	

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VCC_DCDC	Input	Switching regulator power supply pin
	VLO	I/O	Switching regulator pin
	VSS_DCDC	Input	Switching regulator ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB	Input	External trigger input pins
	GTIOCnA (n = 0 to 9), GTIOCnB (n = 0 to 9)	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable signals
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Output compare match A output pins
	AGTOB0, AGTOB1	Output	Output compare match B output pins

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
SCI	SCKn (n = 0 to 3, 9)	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn (n = 0 to 3, 9)	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn (n = 0 to 3, 9)	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn (n = 0 to 3, 9)	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	SCLn (n = 0 to 3, 9)	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn (n = 0 to 3, 9)	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn (n = 0 to 3, 9)	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn (n = 0 to 3, 9)	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn (n = 0 to 3, 9)	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn (n = 0 to 3, 9)	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn (n = 0, 1)	I/O	Input/output pins for the clock
	SDAn (n = 0, 1)	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
Analog power supply	AVCC0	Input	Analog voltage supply pin for the ADC12, DAC12
	AVSS0	Input	Analog ground pin for the ADC12, DAC12
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12.
ADC12	AN000 to AN014, AN017 to AN020	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pin for the external trigger signals that start the A/D conversion, active-low.
DAC12	DA0	Output	Output pin for the analog signals processed by the D/A converter.
ACMPLP	VCOUT	Output	Comparator output pin
	CMPREF0, CMPREF1	Input	Reference voltage input pins
	CMPIN0, CMPIN1	Input	Analog voltage input pins
CTSU	TS00, TS02-CFC, TS04 to TS07, TS08-CFC to TS16-CFC, TS17, TS18, TS21 to TS25, TS26-CFC to TS35-CFC	Input	Capacitive touch detection pins (touch pins)
	TSCAP	—	Secondary power supply pin for the touch driver
KINT	KR00 to KR07	Input	Key interrupt input pins

Table 1.14 Pin functions (3 of 3)

Function	Signal	I/O	Description
I/O ports	P000 to P008, P010 to P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201 to P208, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P307	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P505	I/O	General-purpose input/output pins
	P600 to P603, P608 to P610	I/O	General-purpose input/output pins
	P708, P714	I/O	General-purpose input/output pins
	P808, P809	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments from the top view.

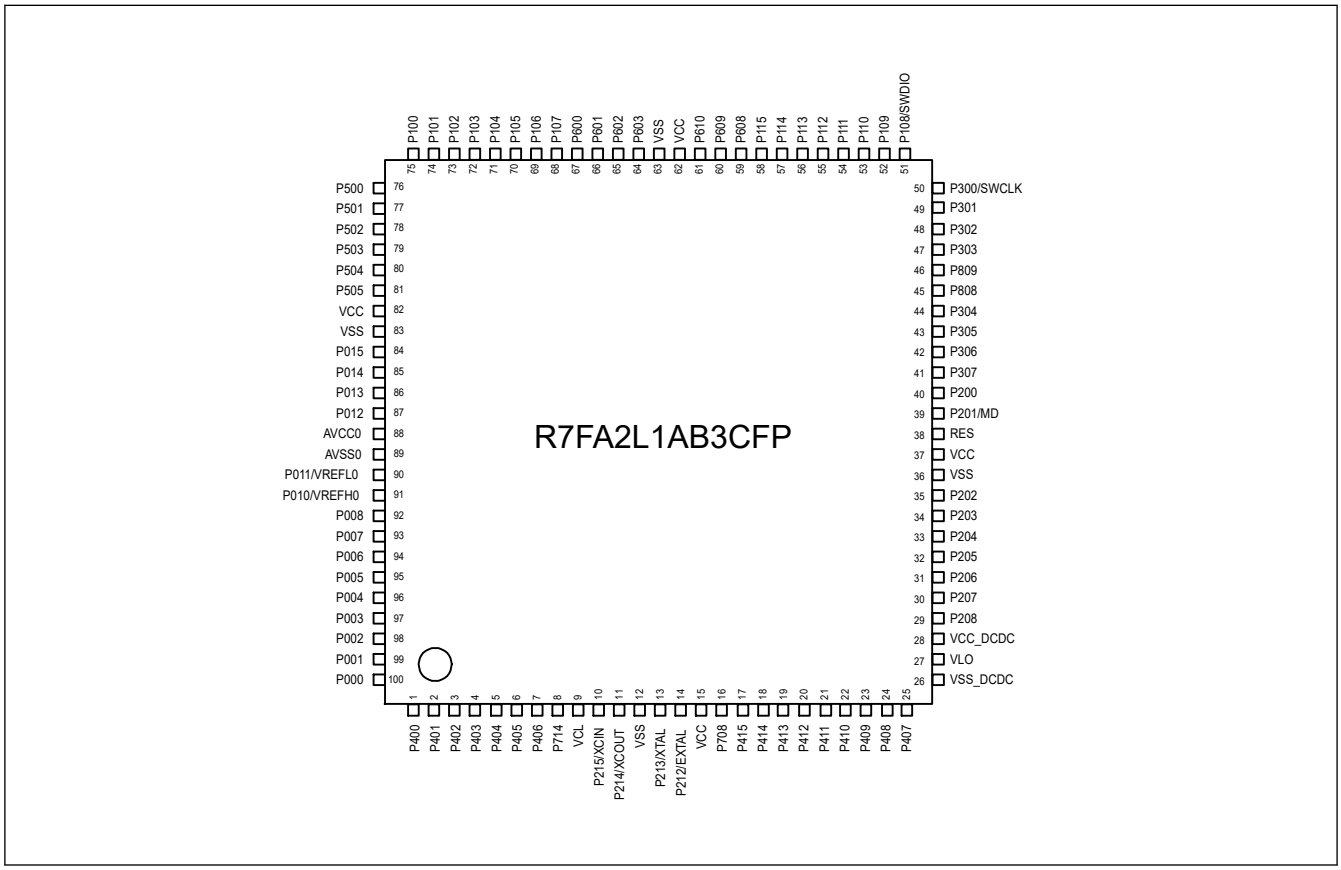


Figure 1.3 Pin assignment for LQFP 100-pin (top view)

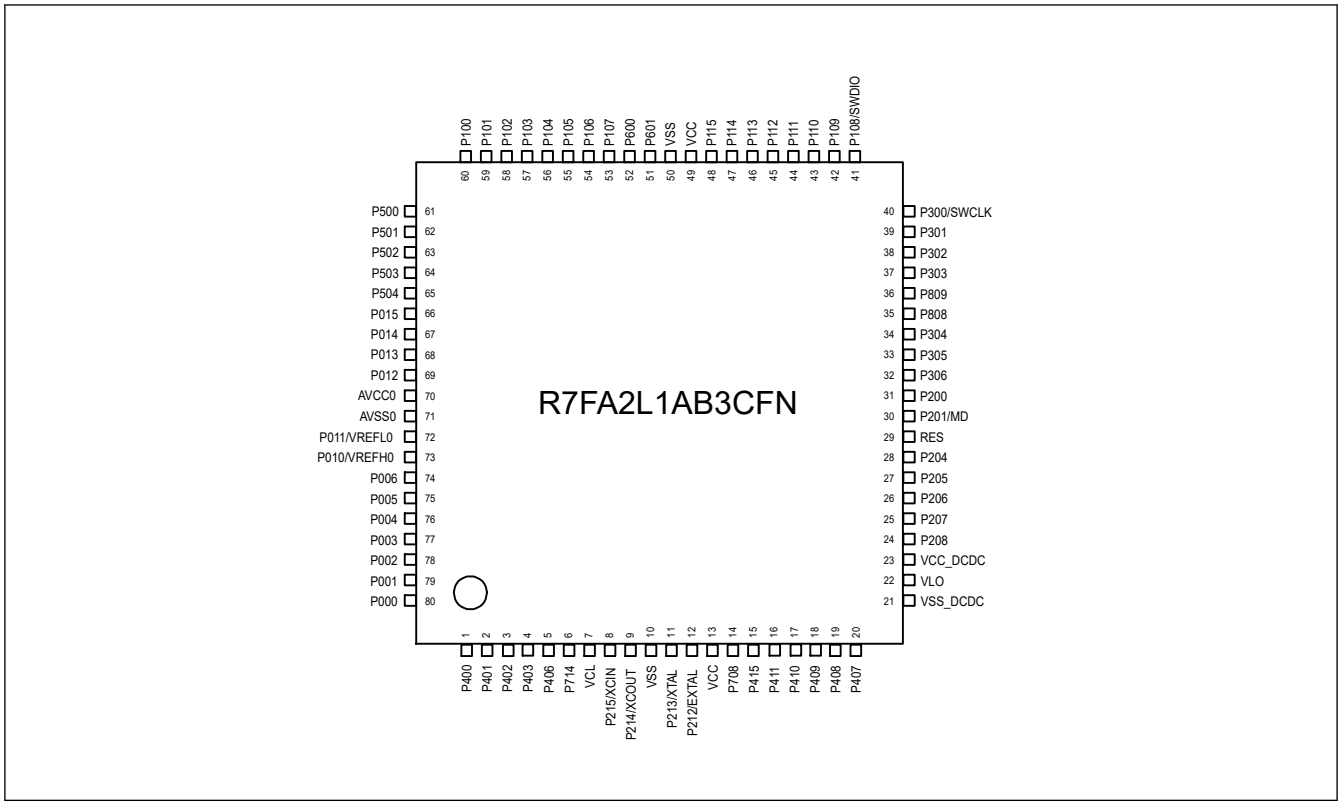


Figure 1.4 Pin assignment for LQFP 80-pin (top view)

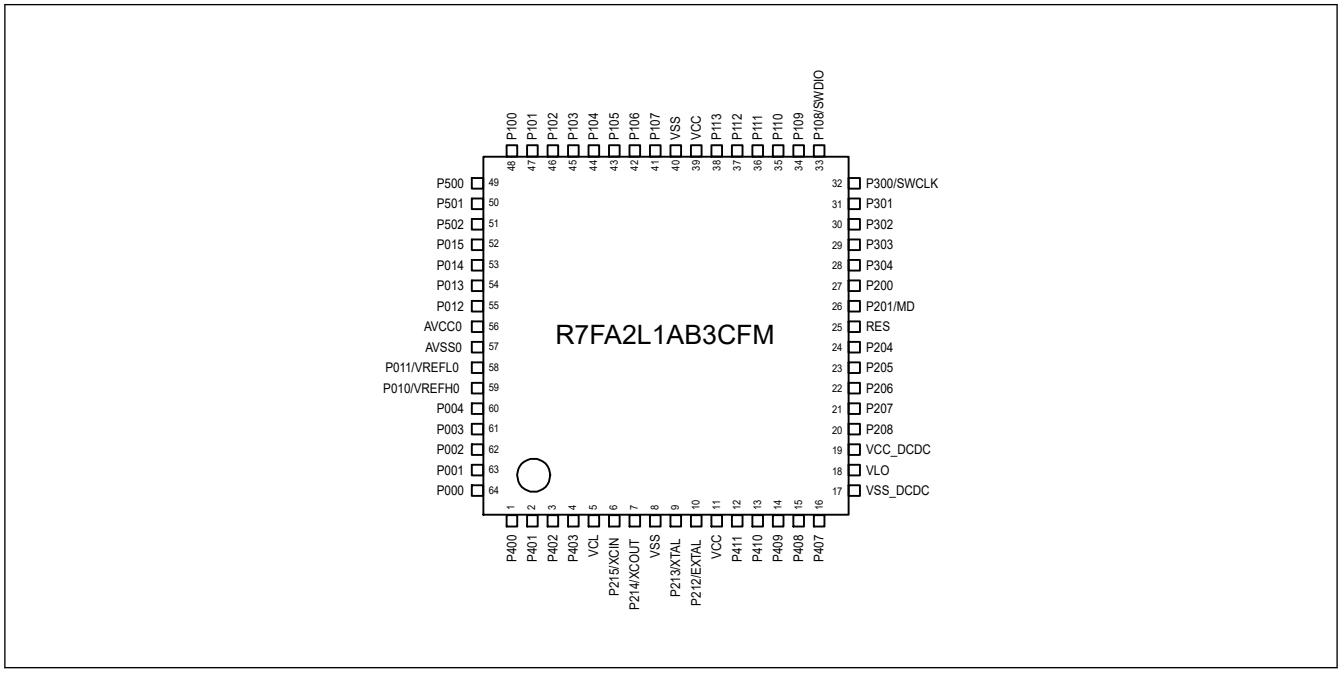


Figure 1.5 Pin assignment for LQFP 64-pin (top view)

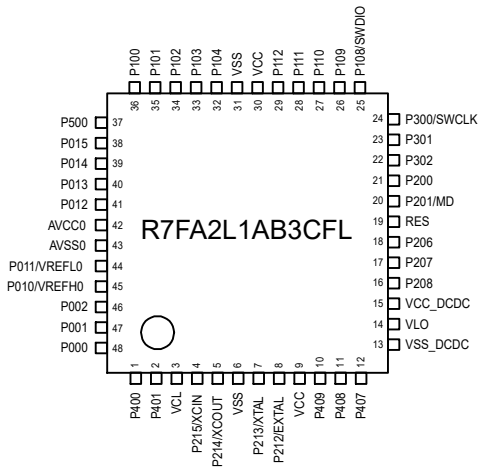
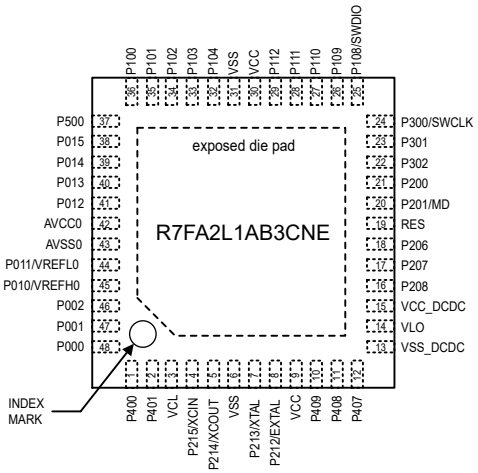


Figure 1.6 Pin assignment for LQFP 48-pin (top view)



Note: Exposed die pad is recommended to connect to VSS or Open.

Figure 1.7 Pin assignment for QFN 48-pin (top view)

1.7 Pin Lists

Table 1.15 Pin list (1 of 4)

Num.						Timers				Communication interfaces				Analogs			HMI	
LQFP100	LQFP80	LQFP64	LQFP48/QFN48	Power, System, Clock, Debug, CAC	I/O ports	AGT	GPT_OPS, POEG	GPT	RTC	CAN	SCI	IIC	SPI	ADC12	DAC12	ACMPLP	CTSU	Interrupt
1	1	1	1	CACREF_C	P400	AGTIO1_C	—	GTIOC6A_A	—	—	SCK0_B/SCK1_B	SCL0_A	—	—	—	—	—	IRQ0_A
2	2	2	2	—	P401	—	GTETRGA_B	GTIOC6B_A	—	CTX0_B	CTS0_RTS0_B/SS0_B/TXD1_B/MOSI1_B/SDA1_B	SDA0_A	—	—	—	—	—	IRQ5
3	3	3	—	—	P402	AGTIO0_E/AGTIO1_D	—	—	—	CRX0_B	RXD1_B/MISO1_B/SCL1_B	—	—	—	—	—	TS18	IRQ4
4	4	4	—	—	P403	AGTIO0_F/AGTIO1_E	—	GTIOC3A_B	—	—	CTS1_RTS1_B/SS1_B	—	—	—	—	—	TS17	—
5	—	—	—	—	P404	—	—	GTIOC3B_B	—	—	—	—	—	—	—	—	—	—
6	—	—	—	—	P405	—	—	GTIOC1A_B	—	—	—	—	—	—	—	—	—	—
7	5	—	—	—	P406	—	—	GTIOC1B_B	—	—	—	—	—	—	—	—	—	—
8	6	—	—	—	P714	—	—	—	—	—	—	—	—	—	—	—	—	—
9	7	5	3	VCL	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10	8	6	4	XCIN	P215	—	—	—	—	—	—	—	—	—	—	—	—	—
11	9	7	5	XCOUT	P214	—	—	—	—	—	—	—	—	—	—	—	—	—
12	10	8	6	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
13	11	9	7	XTAL	P213	—	GTETRGA_D	GTIOC0A_D	—	—	TXD1_A/MOSI1_A/SDA1_A	—	—	—	—	—	—	IRQ2_B
14	12	10	8	EXTAL	P212	AGTEE1	GTETRGB_D	GTIOC0B_D	—	—	RXD1_A/MISO1_A/SCL1_A	—	—	—	—	—	—	IRQ3_B
15	13	11	9	VCC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16	14	—	—	—	P708	—	—	—	—	—	RXD1_D/MISO1_D/SCL1_D	—	SSLA3_B	—	—	—	—	—
17	15	—	—	—	P415	—	—	GTIOC0A_C	—	—	—	—	SSLA2_B	—	—	—	—	—
18	—	—	—	—	P414	—	—	GTIOC0B_C	—	—	—	—	SSLA1_B	—	—	—	—	—
19	—	—	—	—	P413	—	GTOUUP_B	—	—	—	CTS0_RTS0_E/SS0_E	—	SSLA0_B	—	—	—	—	—
20	—	—	—	—	P412	—	GTOULO_B	—	—	—	SCK0_E	—	RSPCKA_B	—	—	—	—	—
21	16	12	—	—	P411	AGTOA1	GTOVUP_B	GTIOC9A_A	—	—	TXD0_B/MOSI0_B/SDA0_B/CTS3_RTS3_A/SS3_A	—	MOSIA_B	—	—	—	TS07	IRQ4_B
22	17	13	—	—	P410	AGTOB1	GTOVLO_B	GTIOC9B_A	—	—	RXD0_B/MISO0_B/SCL0_B/SCK3_A	—	MISOA_B	—	—	—	TS06	IRQ5_B
23	18	14	10	—	P409	—	GTOWUP_B	GTIOC5A_B	—	—	TXD3_A/MOSI3_A/SDA3_A	—	—	—	—	—	TS05	IRQ6_B
24	19	15	11	—	P408	—	GTOWLO_B	GTIOC5B_B	—	—	CTS1_RTS1_D/SS1_D/RXD3_A/MISO3_A/SCL3_A	SCL0_C	—	—	—	—	TS04	IRQ7_B

Table 1.15 Pin list (2 of 4)

Num.				Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication interfaces				Analogs			HMI	
LQFP100	LQFP80	LQFP64	LQFP48/QFN48			AGT	GPT_OPS, POEG	GPT	RTC	CAN	SCI	IIC	SPI	ADC12	DAC12	ACMPLP	CTSU	Interrupt
25	20	16	12	—	P407	AGTIO0_C	—	—	RTCOUT	—	CTS0_RTS0_D/SS0_D	SDA0_B	SSLB3_A	ADTRG0_B	—	—	—	—
26	21	17	13	VSS_DCDC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
27	22	18	14	VLO	—	—	—	—	—	—	—	—	—	—	—	—	—	—
28	23	19	15	VCC_DCDC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
29	24	20	16	—	P208	AGTOB0_A	—	—	—	—	—	—	—	—	—	—	—	—
30	25	21	17	—	P207	—	—	—	—	—	—	—	—	—	—	—	—	—
31	26	22	18	—	P206	—	GTIU_A	—	—	—	RXD0_D/MISO0_D/SCL0_D	SDA1_A	SSLB1_A	—	—	—	—	IRQ0
32	27	23	—	CLKOUT_A	P205	AGTO1	GTIV_A	GTIOC4A_B	—	—	TXD0_D/MOSI0_D/SDA0_D/CTS9_RTS9_A/SS9_A	SCL1_A	SSLB0_A	—	—	—	—	IRQ1
33	28	24	—	CACREF_A	P204	AGTIO1_A	GTIW_A	GTIOC4B_B	—	—	SCK0_D/SCK9_A	SCL0_B	RSPCKB_A	—	—	—	TS00	—
34	—	—	—	—	P203	—	—	—	—	—	CTS2_RTS2_A/SS2_A/TXD9_A/MOSI9_A/SDA9_A	—	MOSIB_A	—	—	—	—	—
35	—	—	—	—	P202	—	—	—	—	—	SCK2_A/RXD9_A/MISO9_A/SCL9_A	—	MISOB_A	—	—	—	—	—
36	—	—	—	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
37	—	—	—	VCC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
38	29	25	19	RES	—	—	—	—	—	—	—	—	—	—	—	—	—	—
39	30	26	20	MD	P201	—	—	—	—	—	—	—	—	—	—	—	—	—
40	31	27	21	—	P200	—	—	—	—	—	—	—	—	—	—	—	—	NMI
41	—	—	—	—	P307	—	—	—	—	—	—	—	—	—	—	—	—	—
42	32	—	—	—	P306	—	—	—	—	—	—	—	—	—	—	—	—	—
43	33	—	—	—	P305	—	—	—	—	—	—	—	—	—	—	—	—	—
44	34	28	—	—	P304	—	—	GTIOC7A_A	—	—	—	—	—	—	—	—	—	—
45	35	—	—	—	P808	—	—	—	—	—	—	—	—	—	—	—	—	—
46	36	—	—	—	P809	—	—	—	—	—	—	—	—	—	—	—	—	—
47	37	29	—	—	P303	—	—	GTIOC7B_A	—	—	—	—	—	—	—	—	TS02-CFC	—
48	38	30	22	—	P302	—	GTOUUP_A	GTIOC4A_A	—	—	TXD2_A/MOSI2_A/SDA2_A	—	SSLB3_B	—	—	—	TS08-CFC	IRQ5_A
49	39	31	23	—	P301	AGTIO0_D	GTOULO_A	GTIOC4B_A	—	—	RXD2_A/MISO2_A/SCL2_A/CTS9_RTS9_D/SS9_D	—	SSLB2_B	—	—	—	TS09-CFC	IRQ6_A
50	40	32	24	SWCLK	P300	—	GTOUUP_C	GTIOC0A_A	—	—	—	—	SSLB1_B	—	—	—	—	—
51	41	33	25	SWDIO	P108	—	GTOULO_C	GTIOC0B_A	—	—	CTS9_RTS9_B/SS9_B	—	SSLB0_B	—	—	—	—	—
52	42	34	26	CLKOUT_B	P109	—	GTOVUP_A	GTIOC1A_A	—	CTX0_A	SCK1_E/TXD9_B/MOSI9_B/SDA9_B	—	MOSIB_B	—	—	—	TS10-CFC	—

Table 1.15 Pin list (3 of 4)

Num.						Timers				Communication interfaces				Analogs			HMI	
LQFP100	LQFP80	LQFP64	LQFP48/QFN48	Power, System, Clock, Debug, CAC	I/O ports	AGT	GPT_OPS, POEG	GPT	RTC	CAN	SCI	IIC	SPI	ADC12	DAC12	ACMPLP	CTSU	Interrupt
53	43	35	27	—	P110	—	GTOVLO_A	GTIOC1B_A	—	CRX0_A	CTS2_RTS2_B/SS2_B/RXD9_B/MISO9_B/SCL9_B	—	MISOB_B	—	—	VCOUT	TS11-CFC	IRQ3_A
54	44	36	28	—	P111	AGTOA0	—	GTIOC3A_A	—	—	SCK2_B/SCK9_B	—	RSPCKB_B	—	—	—	TS12-CFC	IRQ4_A
55	45	37	29	—	P112	AGTOB0	—	GTIOC3B_A	—	—	SCK1_D/TXD2_B/MOSI2_B/SDA2_B	—	SSLB0_C	—	—	—	TSCAP-C	—
56	46	38	—	—	P113	—	—	GTIOC2A_C	—	—	—	—	—	—	—	—	TS27-CFC	—
57	47	—	—	—	P114	—	—	GTIOC2B_C	—	—	—	—	—	—	—	—	TS29-CFC	—
58	48	—	—	—	P115	—	—	GTIOC4A_C	—	—	—	—	—	—	—	—	TS35-CFC	—
59	—	—	—	—	P608	—	—	GTIOC4B_C	—	—	—	—	—	—	—	—	—	—
60	—	—	—	—	P609	—	—	GTIOC5A_C	—	—	—	—	—	—	—	—	—	—
61	—	—	—	—	P610	—	—	GTIOC5B_C	—	—	—	—	—	—	—	—	—	—
62	49	39	30	VCC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
63	50	40	31	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
64	—	—	—	—	P603	—	—	GTIOC7A_B	—	—	CTS9_RTS9_C/SS9_C	—	—	—	—	—	—	—
65	—	—	—	—	P602	—	—	GTIOC7B_B	—	—	TXD9_C/MOSI9_C/SDA9_C	—	—	—	—	—	—	—
66	51	—	—	—	P601	—	—	GTIOC6A_C	—	—	RXD9_C/MISO9_C/SCL9_C	—	—	—	—	—	—	—
67	52	—	—	—	P600	—	—	GTIOC6B_C	—	—	SCK9_C	—	—	—	—	—	—	—
68	53	41	—	—	P107	—	—	GTIOC8A_A	—	—	—	—	—	—	—	—	—	KR07
69	54	42	—	—	P106	—	—	GTIOC8B_A	—	—	—	—	SSLA3_A	—	—	—	—	KR06
70	55	43	—	—	P105	—	GTETRGA_C	GTIOC1A_C	—	—	—	—	SSLA2_A	—	—	—	TS34-CFC	KR05/IRQ0_B
71	56	44	32	—	P104	—	GTETRGB_B	GTIOC1B_C	—	—	RXD0_C/MISO0_C/SCL0_C	—	SSLA1_A	—	—	—	TS13-CFC	KR04/IRQ1_B
72	57	45	33	—	P103	—	GTOWUP_A	GTIOC2A_A	—	CTX0_C	CTS0_RTS0_A/SS0_A	—	SSLA0_A	—	—	CMPREF1	TS14-CFC	KR03
73	58	46	34	—	P102	AGTO0	GTOWLO_A	GTIOC2B_A	—	CRX0_C	SCK0_A/TXD2_D/MOSI2_D/SDA2_D	—	RSPCKA_A	ADTRG0_A	—	CMPIN1	TS15-CFC	KR02
74	59	47	35	—	P101	AGTEE0	GTETRGB_A	GTIOC5A_A	—	—	TXD0_A/MOSI0_A/SDA0_A/CTS1_RTS1_A/SS1_A	SDA1_B	MOSIA_A	—	—	CMPREF0	TS16-CFC	KR01/IRQ1_A
75	60	48	36	—	P100	AGTIO0_A	GTETRGA_A	GTIOC5B_A	—	—	RXD0_A/MISO0_A/SCL0_A/SCK1_A	SCL1_B	MISOA_A	—	—	CMPIN0	TS26-CFC	KR00/IRQ2_A
76	61	49	37	—	P500	—	GTIU_B	GTIOC2A_B	—	—	—	—	—	—	—	—	—	—
77	62	50	—	—	P501	—	GTIV_B	GTIOC2B_B	—	—	TXD1_C/MOSI1_C/SDA1_C	—	—	AN017	—	—	—	—

Table 1.15 Pin list (4 of 4)

Num.						Timers				Communication interfaces				Analogs			HMI	
LQFP100	LQFP80	LQFP64	LQFP48/QFN48	Power, System, Clock, Debug, CAC	I/O ports	AGT	GPT_OPS, POEG	GPT	RTC	CAN	SCI	IIC	SPI	ADC12	DAC12	ACMPLP	CTSU	Interrupt
78	63	51	—	—	P502	—	GTIW_B	GTIOC3B_C	—	—	RXD1_C/MISO1_C/SCL1_C	—	—	AN018	—	—	—	—
79	64	—	—	—	P503	—	GTETRGA_E	—	—	—	SCK1_C	—	—	AN019	—	—	—	—
80	65	—	—	—	P504	—	GTETRGB_E	—	—	—	CTS1_RTS1_C/SS1_C	—	—	AN020	—	—	—	—
81	—	—	—	—	P505	—	—	—	—	—	—	—	—	—	—	—	—	—
82	—	—	—	VCC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
83	—	—	—	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
84	66	52	38	—	P015	—	—	—	—	—	—	—	—	AN010	—	—	TS28-CFC	IRQ7_A
85	67	53	39	—	P014	—	—	—	—	—	—	—	—	AN009	DA0	—	—	—
86	68	54	40	—	P013	—	—	—	—	—	—	—	—	AN008	—	—	TS33-CFC	—
87	69	55	41	—	P012	—	—	—	—	—	—	—	—	AN007	—	—	TS32-CFC	—
88	70	56	42	AVCC0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
89	71	57	43	AVSS0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
90	72	58	44	VREFL0	P011	—	—	—	—	—	—	—	—	AN006	—	—	TS31-CFC	—
91	73	59	45	VREFH0	P010	—	—	—	—	—	—	—	—	AN005	—	—	TS30-CFC	—
92	—	—	—	—	P008	—	—	—	—	—	—	—	—	AN014	—	—	—	—
93	—	—	—	—	P007	—	—	—	—	—	—	—	—	AN013	—	—	—	—
94	74	—	—	—	P006	—	—	—	—	—	—	—	—	AN012	—	—	—	—
95	75	—	—	—	P005	—	—	—	—	—	—	—	—	AN011	—	—	—	—
96	76	60	—	—	P004	—	—	—	—	—	—	—	—	AN004	—	—	TS25	IRQ3
97	77	61	—	—	P003	—	—	—	—	—	—	—	—	AN003	—	—	TS24	—
98	78	62	46	—	P002	—	—	—	—	—	—	—	—	AN002	—	—	TS23	IRQ2
99	79	63	47	—	P001	—	—	—	—	—	—	—	—	AN001	—	—	TS22	IRQ7
100	80	64	48	—	P000	—	—	—	—	—	—	—	—	AN000	—	—	TS21	IRQ6

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E and _F. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC[*1] = AVCC0 = VCC_DCDC[*2] = 1.6 to 5.5 V, VREFH0 = 1.6 V to AVCC0

VSS = AVSS0 = VREFL0 = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.
Note 2. When VCC_DCDC is used. VCC = AVCC0 = VCC_DCDC = 2.4 to 5.5 V.

Figure 2.1 shows the timing conditions.

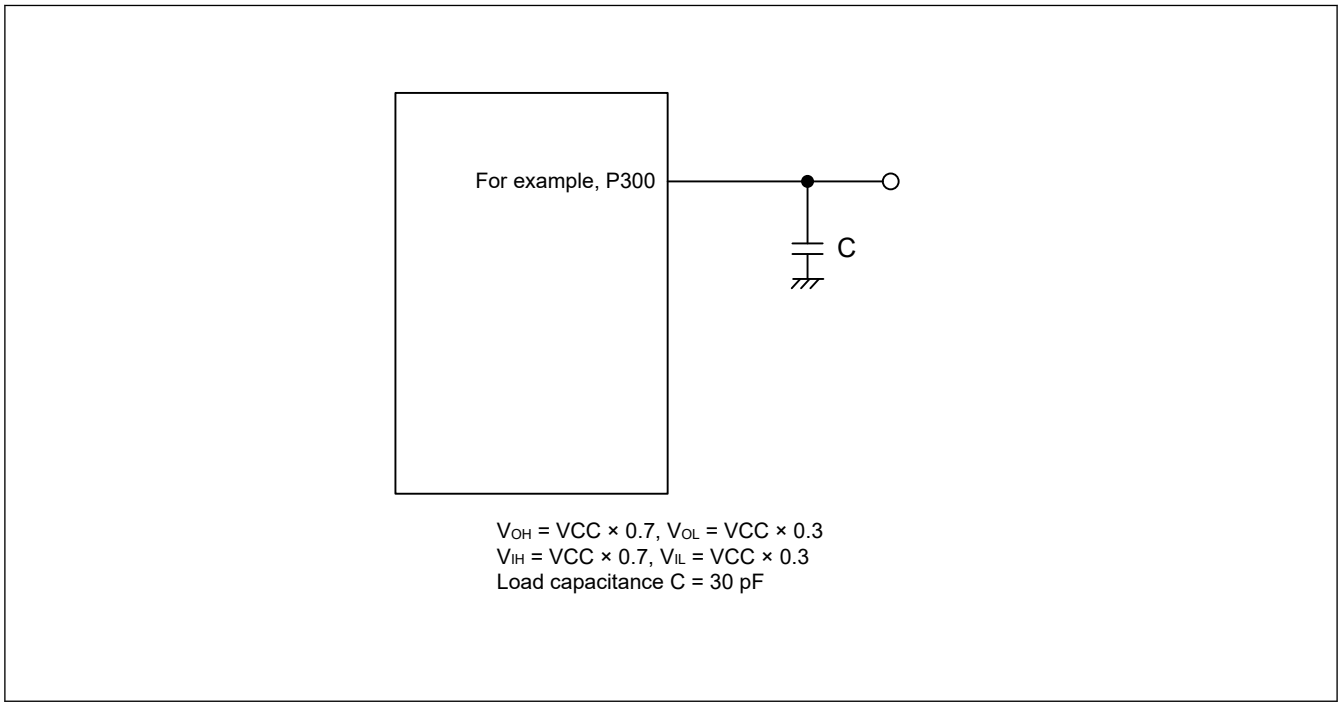


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC characteristics of each function are not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
Input voltage	5V-tolerant ports[*1]	V_{in}	-0.3 to +6.5	V
	P000 to P008, P010 to P015	V_{in}	-0.3 to AVCC0 + 0.3	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +6.5	V
Analog power supply voltage		AVCC0	-0.5 to +6.5	V
Switching regulator power supply voltage		VCC_DCDC	-0.5 to +6.5	V
Analog input voltage	When AN000 to AN014 are used	V_{AN}	-0.3 to AVCC0 + 0.3	V
	When AN017 to AN020 are used		-0.3 to VCC + 0.3	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter	Symbol	Value	Unit
Operating temperature*2 *3 *4	T_{opr}	-40 to +85 -40 to +105	°C
Storage temperature	T_{stg}	-55 to +125	°C

Note 1. Ports P205, P206, P400, P401, and P407 are 5V-tolerant.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.
Note 2. See section 2.2.1. Tj/Ta Definition.
Note 3. Contact Renesas Electronics sales office for information on derating operation under Ta = +85°C to +105°C.
Derating is the systematic reduction of load for improved reliability.
Note 4. The upper limit of the operating temperature is 85°C or 105°C, depending on the product.

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins when VREFH0 is selected as the high potential reference voltage for the ADC12. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:

- **VCC and VSS: about 0.1 µF**
- **AVCC0 and AVSS0: about 0.1 µF**
- **VREFH0 and VREFL0: about 0.1 µF**

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. Connect the VCC_DCDC pin to a VSS_DCDC pin by a 1.0 µF capacitor. Each capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions

Parameter	Symbol		Min	Typ	Max	Unit
Power supply voltages	VCC*1 *2		1.6	—	5.5	V
	VSS		—	0	—	V
Switching regulator power supply voltage	VCC_DCDC	VCC_DCDC = VCC	2.4	—	5.5	V
Analog power supply voltages	AVCC0*1 *2		1.6	—	5.5	V
	AVSS0		—	0	—	V
	VREFH0	When used as ADC12 Reference	1.6	—	AVCC0	V
	VREFL0		—	0	—	V

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 = VCC
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pins.
When powering off the VCC and AVCC0 pins, power them off at the same time or the AVCC0 pin first and then the VCC pins.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (Ta) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	—	125	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.
Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. If the part number shows the operation temperature at 85°C, then the maximum value of Tj is 105°C, otherwise it is 125°C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter	Ports & Functions		Symbol	Min	Max	Unit	Test Conditions
Input voltage	Input ports pins P000 to P008, P010 to P015		V_{IH}	AVCC0 × 0.8	—	V	—
			V_{IL}	—	AVCC0 × 0.2		
	Input ports pins except for P000 to P008, P010 to P015		V_{IH}	VCC × 0.8	—		
			V_{IL}	—	VCC × 0.2		
	EXTAL		V_{IH}	VCC × 0.8	—		
			V_{IL}	—	VCC × 0.2		
	5V-tolerant ports*3		V_{IH}	VCC × 0.8	5.8		
			V_{IL}	—	VCC × 0.2		
	RES, NMI, IRQ		V_{IH}	VCC × 0.8	—		
			V_{IL}	—	VCC × 0.2		
			ΔV_T*5	VCC × 0.10	—		VCC = 2.7 to 5.5 V
				VCC × 0.05	—		VCC = 1.6 to 2.7 V
	Peripheral functions	AGT, GPT, SPI, Others*4	V_{IH}	VCC × 0.8	—		—
			V_{IL}	—	VCC × 0.2		
			ΔV_T*5	VCC × 0.10	—		VCC = 2.7 to 5.5 V
				VCC × 0.05	—		VCC = 1.6 to 2.7 V
		IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	5.8		—
			V_{IL}	—	VCC × 0.3		
			ΔV_T*5	VCC × 0.10	—		VCC = 2.7 to 5.5 V
				VCC × 0.05	—		VCC = 1.6 to 2.7 V
		IIC (SMBus)*2	V_{IH}	2.2	—		VCC = 3.6 to 5.5 V
			V_{IL}	2.0	—		VCC = 2.7 to 3.6 V
			V_{IL}	—	0.8		VCC = 3.6 to 5.5 V
			V_{IL}	—	0.5		VCC = 2.7 to 3.6 V

Note 1. SCL0_A, SDA0_A, SDA0_B, SCL1_A, SDA1_A (total 5 pins)
Note 2. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_B, SCL1_A, SCL1_B, SDA1_A, SDA1_B (total 9 pins)
Note 3. P205, P206, P400, P401, P407 (total 5 pins)
Note 4. See section x.x Peripheral Select Settings for Each Product.
Note 5. I/O Port with ΔVT has Schmitt Trigger capability when PMR = 1 or ISEL = 1. For peripheral selection, see section x.x Peripheral Select Settings for Each Product

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (average value per pin)	Ports P000 to P008, P010 to P015, P205, P206, P212, P213, P400, P401, P407	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	8.0	mA	
	Other output pins*1	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	20.0	mA	

Table 2.5 I/O I_{OH}, I_{OL} (2 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value per pin)	Ports P000 to P008, P010 to P015, P205, P206, P212, P213, P400, P401, P407		I_{OH}	—	—	-4.0	mA	
			I_{OL}	—	—	8.0	mA	
	Other output pins*1		I_{OH}	—	—	-4.0	mA	
			I_{OL}	—	—	20.0	mA	
Permissible output current (max value total pins)*2	Total of ports P000 to P008, P010 to P015		$\Sigma I_{OH\ (max)}$	—	—	-30	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-8	mA	AVCC0 = 1.8 to 2.7 V
				—	—	-4	mA	AVCC0 = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	AVCC0 = 2.7 to 5.5 V
				—	—	4	mA	AVCC0 = 1.8 to 2.7 V
				—	—	2	mA	AVCC0 = 1.6 to 1.8 V
	Total of ports P212, P213		ΣI_{OH}	—	—	-8.0	mA	VCC = 2.7 to 5.5 V
				—	—	-2	mA	VCC = 1.8 to 2.7 V
				—	—	-1	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL}	—	—	16.0	mA	VCC = 2.7 to 5.5 V
				—	—	1.2	mA	VCC = 1.8 to 2.7 V
				—	—	0.6	mA	VCC = 1.6 to 1.8 V
	Total of ports P400 to P415, P708, P714	100 pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V

Table 2.5 I/O I_{OH}, I_{OL} (3 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	Total of ports P201 to P208, P303 to P307, P808, P809	100 pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of ports P108 to P115, P300 to P302, P600 to P603, P608 to P610	100 pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of ports P100 to P107, P500 to P505	100 pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V

Table 2.5 I/O I_{OH}, I_{OL} (4 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	Total of all output pin	100 pin products	$\Sigma I_{OH\ (max)}$	—	—	-100	mA	
			$\Sigma I_{OL\ (max)}$	—	—	100	mA	
	Total of ports P204 to P208, P400 to P403, P406 to P411, P415, P708, P714	80 pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of ports P100 to P115, P201, P300 to P306, P500 to P504, P600, P601, P808, P809	80 pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of all output pin	80 pin products	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	
			$\Sigma I_{OL\ (max)}$	—	—	100	mA	

Table 2.5 I/O I_{OH}, I_{OL} (5 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	Total of ports P204 to P208, P400 to P403, P407 to P411	64 pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of ports P100 to P113, P201, P300 to P304, P500 to P502	64 pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of all output pin	64 pin products	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	
			$\Sigma I_{OL\ (max)}$	—	—	100	mA	

Table 2.5 I/O I_{OH}, I_{OL} (6 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	Total of ports P206 to P208, P400, P401, P407 to P409	48 pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of ports P100 to P104, P108 to P112,P201, P300 to P302, P500	48 pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of all output pin	48 pin products	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	
			$\Sigma I_{OL\ (max)}$	—	—	100	mA	

Note 1. Except for Ports P200, P214, and P215, which are input ports.
Note 2. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OH} = −30.0 mA
Total output current of pins = (−30.0 × 0.7)/(80 × 0.01) ≅ −26.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in Table 2.5.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL} (1)

Conditions: VCC = AVCC0 = 4.0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P008, P010 to P015	V_{OH}	AVCC0 - 0.8	—	—	V	I_{OH} = -4.0 mA
	Output pins except for P000 to P008 and P010 to P015*1	V_{OH}	VCC - 0.8	—	—		I_{OH} = -4.0 mA
	Ports P000 to P008, P010 to P015	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Ports P205, P206, P212, P213, P400, P401, P407	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Output pins except for P000 to P008, P010 to P015, P205, P206, P212, P213, P400, P401, and P407*1	V_{OL}	—	—	1.2		I_{OL} = 20.0 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.7 I/O V_{OH}, V_{OL} (2)

Conditions: VCC = AVCC0 = 2.7 to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P008, P010 to P015	V_{OH}	AVCC0 - 0.8	—	—	V	I_{OH} = -4.0 mA
	Output pins except for P000 to P008 and P010 to P015*1	V_{OH}	VCC - 0.8	—	—		I_{OH} = -4.0 mA
	Ports P000 to P008, P010 to P015	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Output pins except for P000 to P008 and P010 to P015*1	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.8 I/O V_{OH}, V_{OL} (3)

Conditions: VCC = AVCC0 = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P008, P010 to P015	V_{OH}	AVCC0 - 0.5	—	—	V	I_{OH} = -1.0 mA AVCC0 = 1.8 to 2.7 V
			AVCC0 - 0.5	—	—		I_{OH} = -0.5 mA AVCC0 = 1.6 to 1.8 V
	Output pins except for P000 to P008 and P010 to P015*1	V_{OH}	VCC - 0.5	—	—		I_{OH} = -1.0 mA VCC = 1.8 to 2.7 V
			VCC - 0.5	—	—		I_{OH} = -0.5 mA VCC = 1.6 to 1.8 V
	Ports P000 to P008, P010 to P015	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA AVCC0 = 1.8 to 2.7 V
			—	—	0.4		I_{OL} = 0.3 mA AVCC0 = 1.6 to 1.8 V
	Output pins except for P000 to P008 and P010 to P015*1	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA VCC = 1.8 to 2.7 V
			—	—	0.4		I_{OL} = 0.3 mA VCC = 1.6 to 1.8 V

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.9 I/O other characteristics

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, ports P200, P214, P215	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports*1	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports (except for P200, P214, P215, and 5V-tolerant ports)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215)	R_U	10	20	100	kΩ	V_{in} = 0 V
Input capacitance	P200	C_{in}	—	—	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		—	—	15		

Note 1. P205, P206, P400, P401, and P407 (total 5 pins)

2.2.5 Operating and Standby Current

Table 2.10 Operating and standby current (1) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	LDO mode		DCDC mode*12		Unit	Test Conditions
						Typ*10	Max	Typ*10	Max		
Supply current*1	High-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 48 MHz	I_{CC}	5.50	—	3.05	—	mA	*7 *11
				ICLK = 32 MHz		3.65	—	2.20	—		*7
				ICLK = 16 MHz		2.20	—	1.35	—		
				ICLK = 8 MHz		1.45	—	0.90	—		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 48 MHz		—	14.5	—	12.5		*9 *11
		Sleep mode	All peripheral clocks disabled*5	ICLK = 48 MHz		1.05	—	0.65	—		*7
				ICLK = 32 MHz		0.85	—	0.55	—		*7
				ICLK = 16 MHz		0.70	—	0.45	—		
				ICLK = 8 MHz		0.60	—	0.35	—		
			All peripheral clocks enabled*5	ICLK = 48 MHz		4.85	—	2.95	—		*9
				ICLK = 32 MHz		4.68	—	2.85	—		*8
				ICLK = 16 MHz		2.55	—	1.55	—		
				ICLK = 8 MHz		1.50	—	0.95	—		
		Increase during BGO operation*6				2.1	—	1.95	—		—
Supply current*1	Middle-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 24 MHz	I_{CC}	2.80	—	1.65	—	mA	*7
				ICLK = 4 MHz		0.90	—	0.55	—		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 24 MHz		—	10.0	—	8.8		*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 24 MHz		0.70	—	0.45	—		*7
				ICLK = 4 MHz		0.55	—	0.35	—		
			All peripheral clocks enabled*5	ICLK = 24 MHz		3.50	—	2.10	—		*8
				ICLK = 4 MHz		0.95	—	0.60	—		
		Increase during BGO operation*6				2.00	—	1.65	—		—

Table 2.10 Operating and standby current (1) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	LDO mode		DCDC mode*12		Unit	Test Conditions
						Typ*10	Max	Typ*10	Max		
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 2 MHz	I_{CC}	0.33	—	—	—	mA	*7
			All peripheral clocks enabled, code executing from flash*5	ICLK = 2 MHz		—	3.1	—	—		*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 2 MHz		0.13	—	—	—		*7
			All peripheral clocks enabled*5	ICLK = 2 MHz		0.35	—	—	—		*8
	Subosc-speed mode*4	Normal mode	All peripheral clocks enabled, code executing from flash*5	ICLK = 32.768 kHz	I_{CC}	—	540	—	—	μA	*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 32.768 kHz		2.00	—	—	—		*8
			All peripheral clocks enabled*5	ICLK = 32.768 kHz		5.85	—	—	—		*8

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
In LDO mode, the supply current is total current flowing into VCC.
In DCDC mode, the supply current is total current flowing into VCC and VCC_DCDC.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO and A/D operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. PCLKB and PCLKD are set to divided by 64.
Note 8. PCLKB and PCLKD are the same frequency as that of ICLK.
Note 9. PCLKB are set to be divided by 2 and PCLKD is the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.
Note 11. The prefetch is operating.
Note 12. VCC = AVCC0 = VCC_DCDC = 2.4 to 5.5 V

Table 2.11 Operating and standby current (2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Typ*3	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	All SRAMs(0x2000_4000 to 0x2000_7FFF) are on	T_a = 25°C	I_{CC}	0.30	2.2	µA	—
			T_a = 55°C		0.65	5.3		
			T_a = 85°C		2.0	20		
			T_a = 105°C		4.0	70		
		Only 8KB SRAM (0x2000_4000 to 0x2000_5FFF) is on	T_a = 25°C		0.25	2.2		
			T_a = 55°C		0.6	5.3		
			T_a = 85°C		1.8	20		
			T_a = 105°C		3.65	70		
	Increment for RTC operation with low-speed on-chip oscillator*4				0.30	—		—
	Increment for RTC operation in normal operation mode with sub-clock oscillator*4				0.20	—		SOMCR.SODRV[1:0] are 11b (Low power mode 3) RCR4.ROPSEL is 0 (RTC operation in normal operation mode)
					0.95	—		SOMCR.SODRV[1:0] are 00b (normal mode) RCR4.ROPSEL is 0 (RTC operation in normal operation mode)
	Increment for RTC operation in low-consumption clock mode with sub-clock oscillator*4				0.11	—		SOMCR.SODRV[1:0] are 11b (Low power mode 3) RCR4.ROPSEL is 1 (RTC operation in low-consumption clock mode)
					0.90	—		SOMCR.SODRV[1:0] are 00b (normal mode) RCR4.ROPSEL is 1 (RTC operation in low-consumption clock mode)

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state. The supply current is total current flowing into VCC.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.
Note 4. Includes the low-speed on-chip oscillator or sub-oscillation circuit current.

Table 2.12 Operating and standby current (3) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During 12-bit A/D conversion (at high-speed A/D conversion mode)	I_{AVCC0}	—	—	1.44	mA	—
	During 12-bit A/D conversion (at low-power A/D conversion mode)		—	—	0.78	mA	—
	During 12-bit D/A conversion*1		—	—	0.8	mA	—
	Waiting for 12-bit A/D and 12-bit D/A conversion (all units)*2		—	—	1.0	µA	—
Reference power supply current	During 12-bit A/D conversion	I_{REFH0}	—	—	120	µA	—
	Waiting for 12-bit A/D conversion		—	—	60	nA	—
Temperature Sensor (TSN) operating current		I_{TNS}	—	95	—	µA	—

Table 2.12 Operating and standby current (3) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Low-power Analog Comparator (ACMPLP) operating current	Window comparator (high-speed mode)	I_{CMPLP}	—	12	—	μA	—
	Comparator (high-speed mode)		—	6.4	—	μA	—
	Comparator (low-speed mode)		—	1.8	—	μA	—

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 module-stop bit) is in the module-stop state.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.13 Rise and fall gradient characteristics

Conditions: VCC = AVCC0 = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	—	2	ms/V	—
	Voltage monitor 0 reset enabled at startup*1 *2				—		
	SCI boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 2.14 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = AVCC0 = 1.6 to 5.5 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).
When the VCC change exceeds VCC ± 10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ± 10%

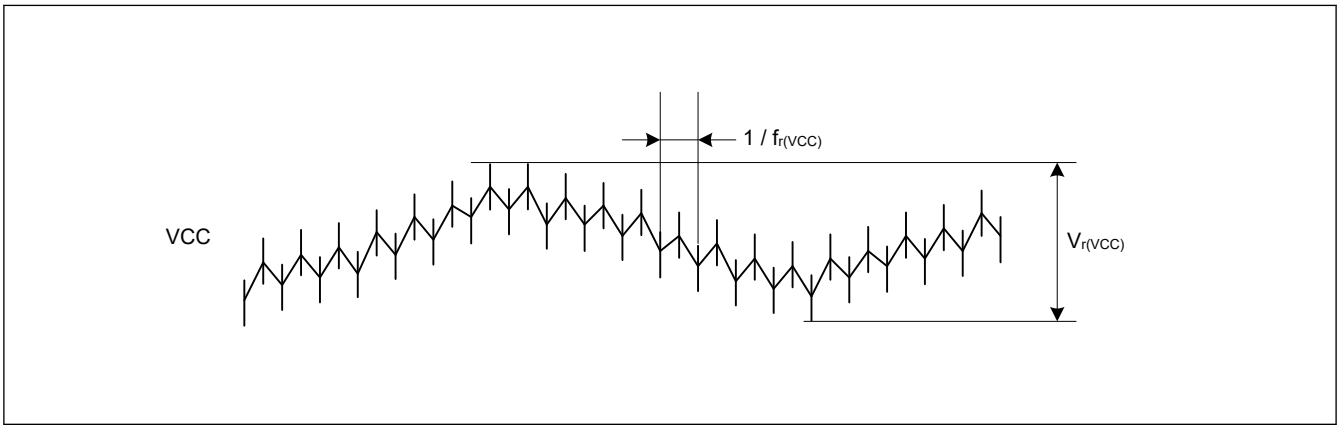


Figure 2.2 Ripple waveform

2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of section 2.2.1. Tj/Ta Definition.

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption

  Tj : Junction temperature (°C)

  Ta : Ambient temperature (°C)

  Tt : Top center case temperature (°C)

  θja : Thermal resistance of "Junction"-to-"Ambient" (°C/W)

  Ψjt : Thermal resistance of "Junction"-to-"Top center case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (IOL × VOL) / Voltage + Σ (|IOH| × |VCC – VOH|) / Voltage
- Dynamic current of IO = Σ IO (Cin + Cload) × IO switching frequency × Voltage

  Cin: Input capacitance

  Cload: Output capacitance

Regarding θja and Ψjt, see Table 2.15.

Table 2.15 Thermal resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal resistance	48-pin HWQFN	θja	18.0	°C/W	JESD 51-2 and 51-7 compliant
	48-pin LQFP		59.7		
	64-pin LQFP		50.8		
	80-pin LQFP		52.0		
	100-pin LQFP		52.2		
	48-pin HWQFN	Ψjt	0.14	°C/W	JESD 51-2 and 51-7 compliant
	48-pin LQFP		1.97		
	64-pin LQFP		1.48		
	80-pin LQFP		1.48		
	100-pin LQFP		1.48		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, see the JEDEC standards.

2.3 AC Characteristics

2.3.1 Frequency

Table 2.16 Operation frequency in high-speed operating mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.8 to 5.5 V	f	0.032768	—	48	MHz
	Peripheral module clock (PCLKB)	1.8 to 5.5 V		—	—	32	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		—	—	64	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.20.

Table 2.17 Operation frequency in middle-speed mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.8 to 5.5 V	f	0.032768	—	24	MHz
		1.6 to 1.8 V		0.032768	—	4	
	Peripheral module clock (PCLKB)	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.20.

Table 2.18 Operation frequency in low-speed mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.6 to 5.5 V	f	0.032768	—	2	MHz
	Peripheral module clock (PCLKB)	1.6 to 5.5 V		—	—	2	
	Peripheral module clock (PCLKD)*3	1.6 to 5.5 V		—	—	2	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ± 1.0% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.20.

Table 2.19 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1	1.6 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB)	1.6 to 5.5 V		—	—	37.6832	
	Peripheral module clock (PCLKD)*2	1.6 to 5.5 V		—	—	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.20 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 2.3
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rising time	t_{Xr}	—	—	5	ns	
EXTAL external clock falling time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	0.3	—	—	μs	—
EXTAL external clock input frequency	f_{EXTAL}	—	—	20	MHz	1.8 ≤ VCC ≤ 5.5

Table 2.20 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
		—	—	4		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	1.8 ≤ VCC ≤ 5.5
		1	—	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	—
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	100	µs	Figure 2.4
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	—
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization time	t_{MOCO}	—	—	1	µs	—
HOCO clock oscillation frequency*5	f_{HOCO24}	23.76	24	24.24	MHz	Ta = -40 to 105°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO32}	31.68	32	32.32		Ta = -40 to 105°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO48}	47.52	48	48.48		Ta = -40 to 105°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO64}	63.36	64	64.64		Ta = -40 to 105°C 1.6 ≤ VCC ≤ 5.5
HOCO clock oscillation stabilization time*3 *4	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	—	1.9	—	µs	Figure 2.5
Sub-clock oscillator oscillation frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	—	0.5	—	s	Figure 2.6

Note 1. Time until the clock can be used after the Main Clock Oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.
Note 3. This is a characteristic when the HOCOCR.HCSTP bit is set to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 µs.
Note 4. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.
Note 5. Accuracy at production test.

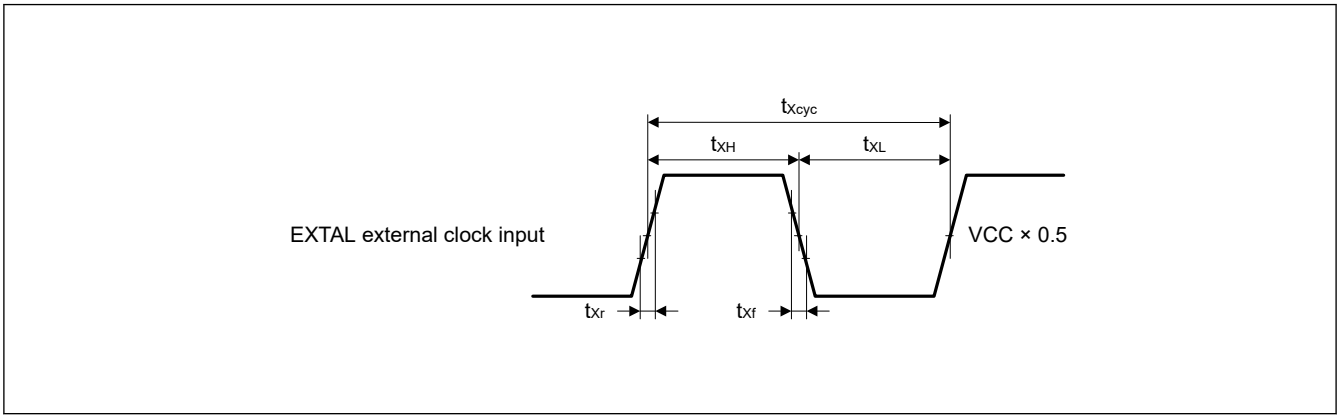


Figure 2.3 EXTAL external clock input timing

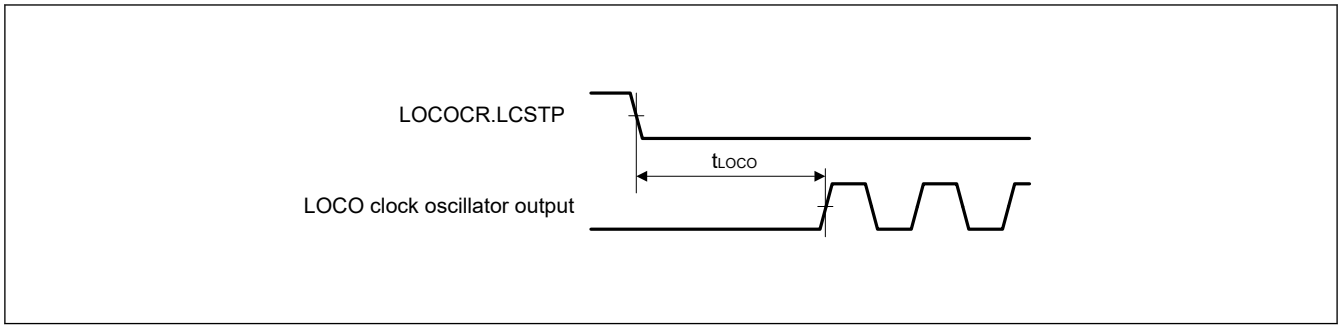


Figure 2.4 LOCO clock oscillation start timing

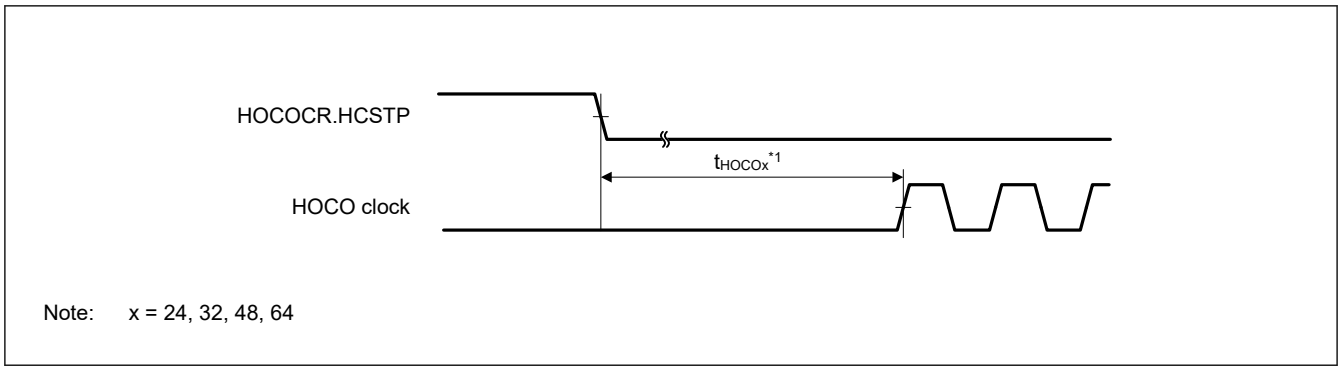


Figure 2.5 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

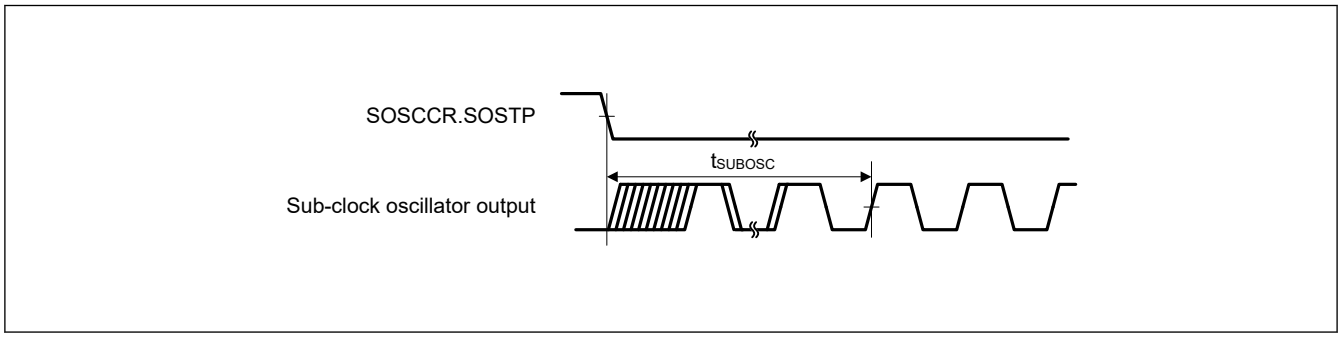


Figure 2.6 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.21 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	10	—	—	ms	Figure 2.7
	Not at power-on	t_{RESW}	30	—	—	μs	Figure 2.8
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	—	0.9	—	ms	Figure 2.7
	LVD0 disabled*2		—	0.2	—		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 2.8
	LVD0 disabled*2		—	0.2	—		
Wait time after internal reset cancellation (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset, software reset)	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 2.9
	LVD0 disabled*2		—	0.15	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

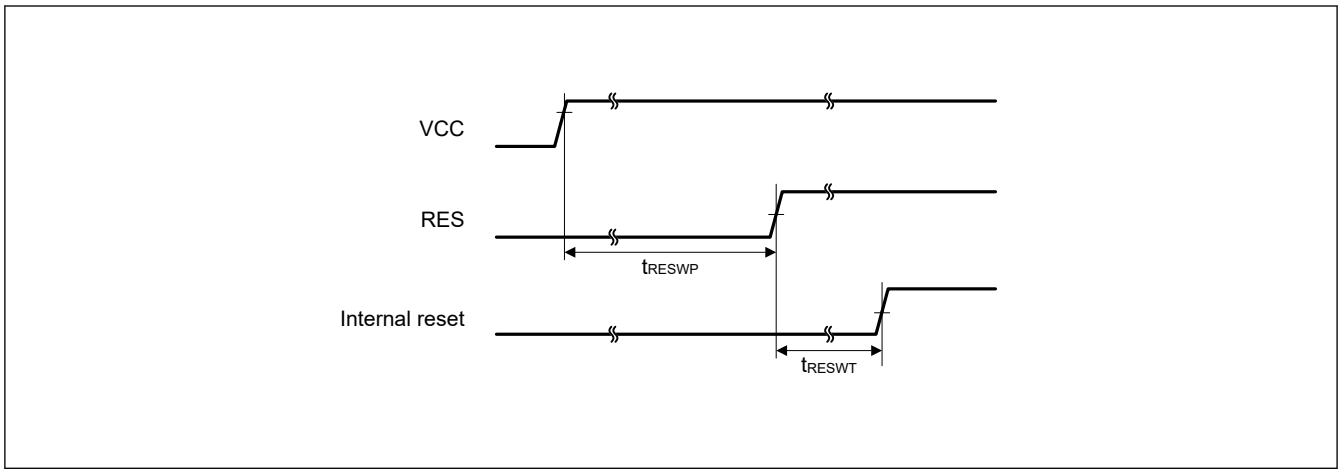


Figure 2.7 Reset input timing at power-on

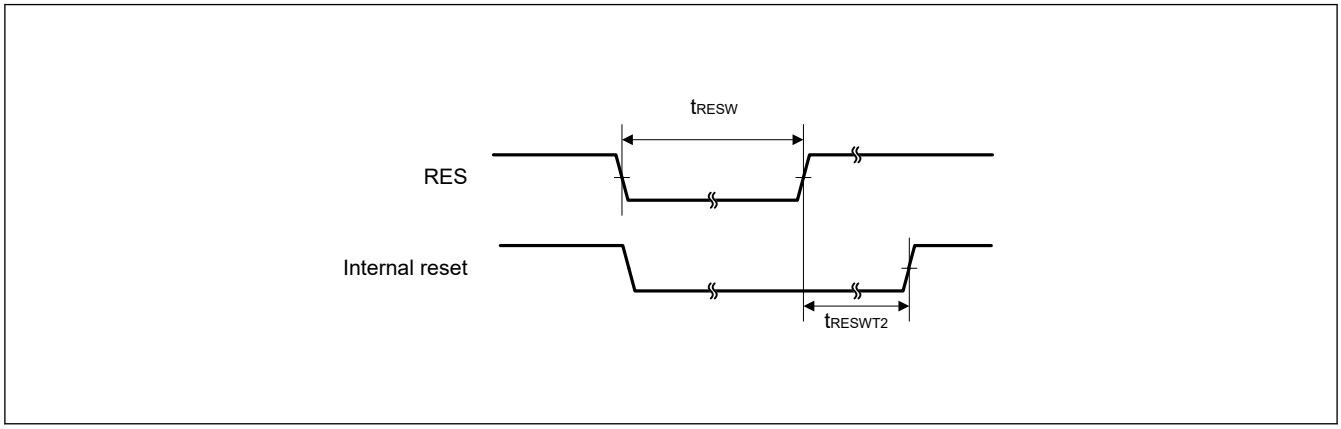


Figure 2.8 Reset input timing (1)

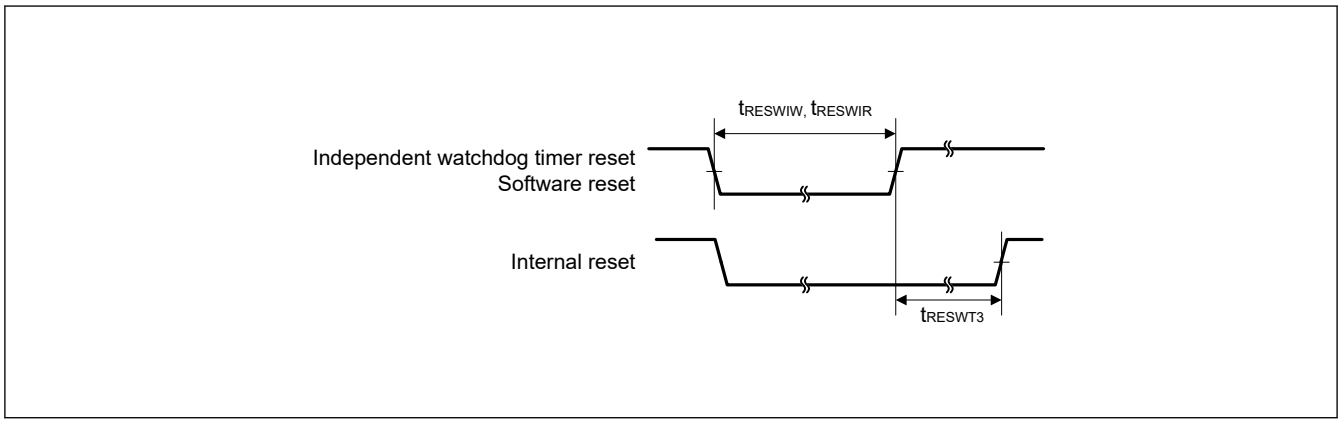


Figure 2.9 Reset input timing (2)

2.3.4 Wakeup Time

Table 2.22 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 2.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t_{SBYEX}	—	2.4	3.1	µs	
		System clock source is HOCO (HOCO clock is 32 MHz)		t_{SBYHO}	—	4.9	6.2	µs	
		System clock source is HOCO (HOCO clock is 48 MHz)		t_{SBYHO}	—	4.8	6	µs	
		System clock source is HOCO (HOCO clock is 64 MHz)		t_{SBYHO}	—	4.9	6.2	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	—	4	5	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

Table 2.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 2.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (4 MHz)*3 VCC = 1.6 V to 1.8 V		—	8.5	9.1		
		System clock source is HOCO	VCC = 1.8 V to 5.5 V*4	t_{SBYHO}	—	5.2	6.5	µs	
			VCC = 1.6 V to 1.8 V		—	13.2	15		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

Table 2.24 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 2.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

Table 2.25 Timing of recovery from low power modes (4)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	—	0.85	1	ms	Figure 2.10
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	—	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

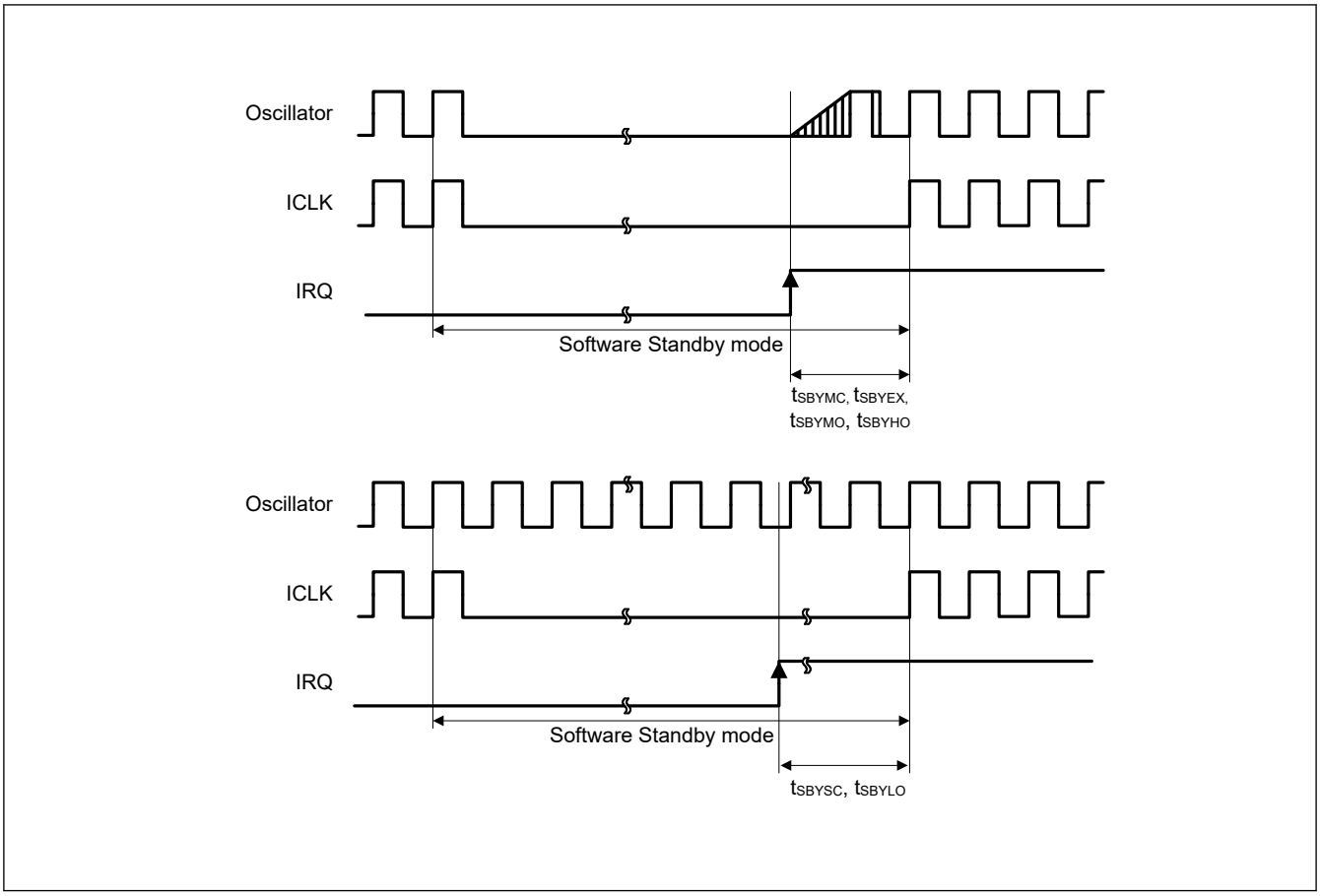
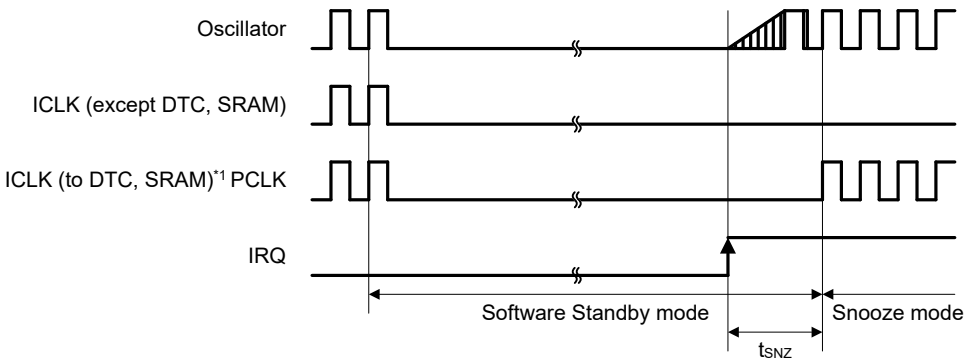


Figure 2.10 Software Standby mode cancellation timing

Table 2.26 Timing of recovery from low power modes (5)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	—	4.1	5.2	µs	Figure 2.11
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.8 V to 5.5 V	t_{SNZ}	—	4.2	5.3	µs	
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.6 V to 1.8 V	t_{SNZ}	—	8.3	10	µs	
	Low-speed mode System clock source is MOCO (2 MHz)	t_{SNZ}	—	6.7	8.0	µs	



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.11 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.27 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is being switched it is needed to add 4 clock cycle of switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

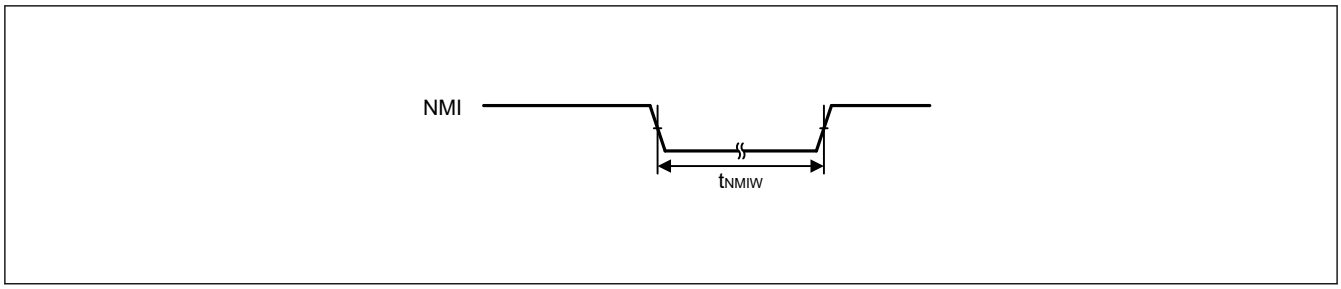


Figure 2.12 NMI interrupt input timing

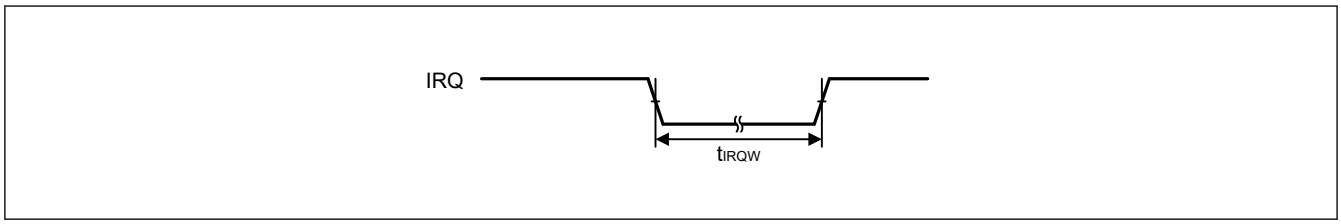


Figure 2.13 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC12 Trigger Timing

Table 2.28 I/O Ports, POEG, GPT, AGT, KINT, and ADC12 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{PRW}	2	—	t_{Pcyc}	Figure 2.14
		2.4 V ≤ VCC < 2.7 V		3			
		1.6 V ≤ VCC < 2.4 V		4			
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.15
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.16
		Dual edge		2.5	—		
AGT	AGTIO, AGTEE input cycle	1.8 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	—	ns	Figure 2.17
		1.6 V ≤ VCC < 1.8 V		2000	—	ns	
	AGTIO, AGTEE input high-level width, low-level width	1.8 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	—	ns	
		1.6 V ≤ VCC < 1.8 V		800	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	—	ns	Figure 2.17
		2.4 V ≤ VCC < 2.7 V		125	—	ns	
		1.8 V ≤ VCC < 2.4 V		250	—	ns	
		1.6 V ≤ VCC < 1.8 V		500	—	ns	
ADC12	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.18
KINT	KRn (n = 00 to 07) pulse width		t_{KR}	250	—	ns	Figure 2.19

Note 1. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

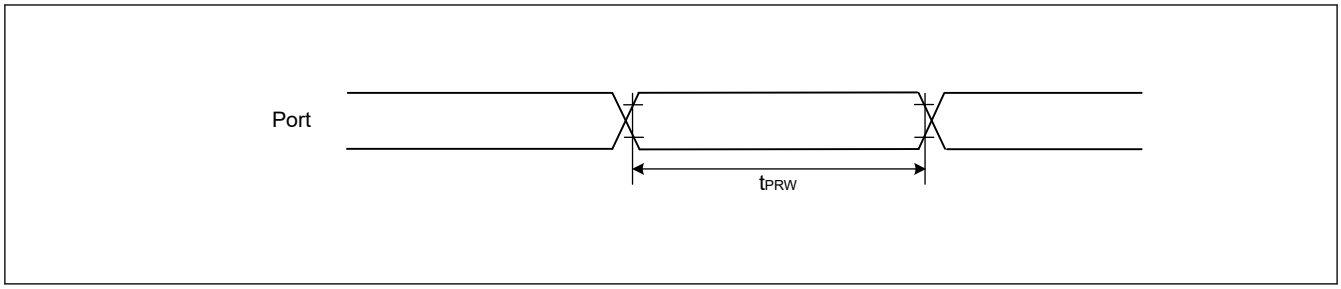


Figure 2.14 I/O ports input timing

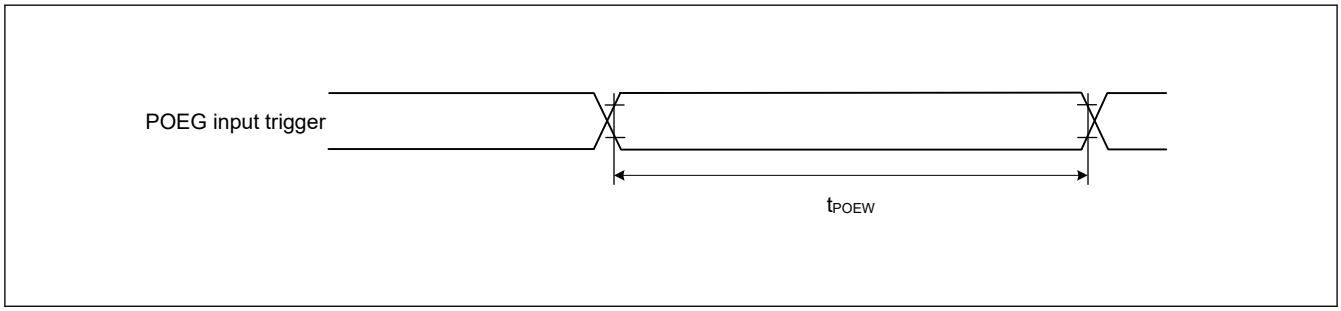


Figure 2.15 POEG input trigger timing

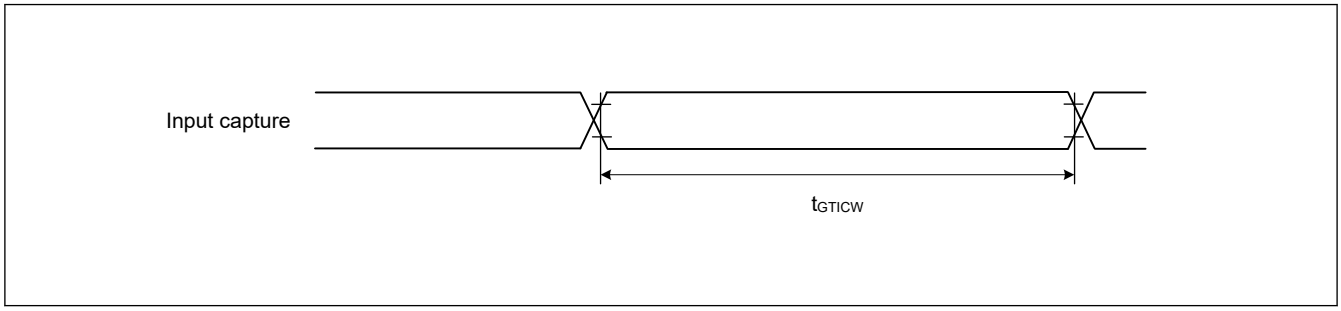


Figure 2.16 GPT input capture timing

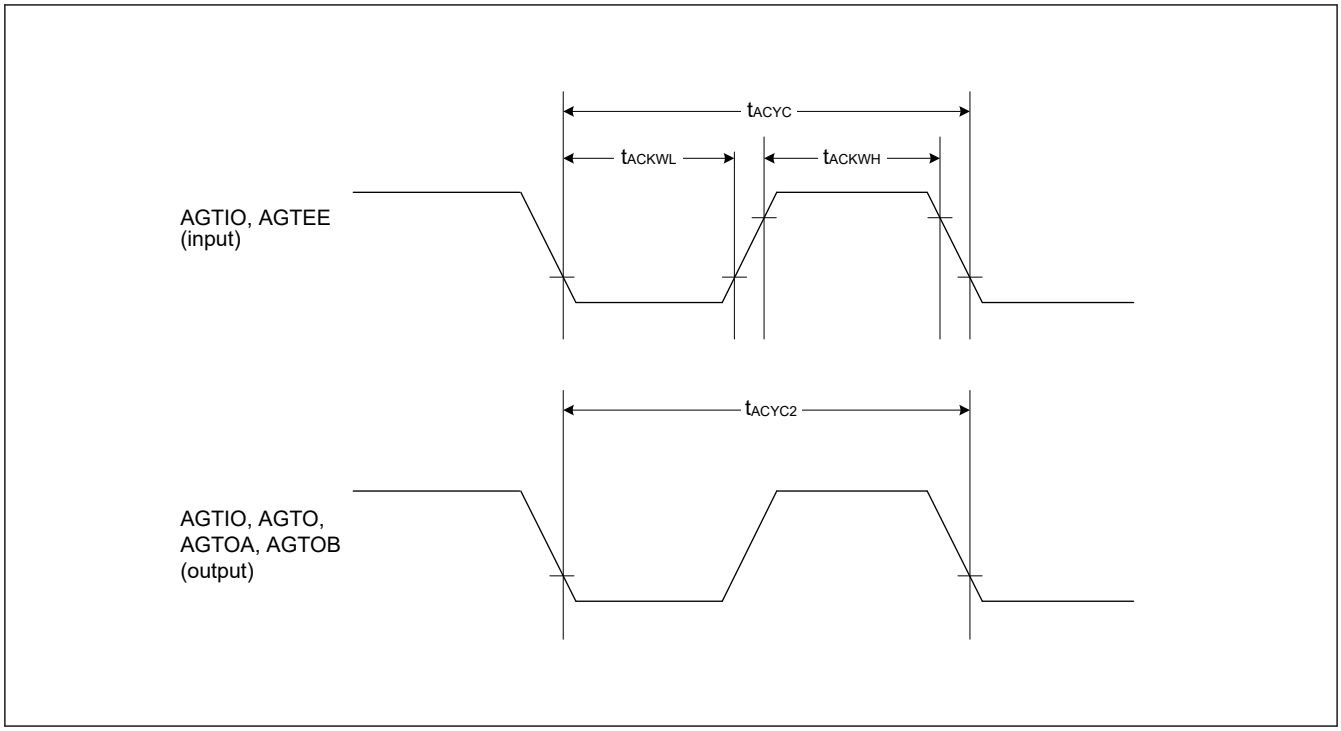


Figure 2.17 AGT I/O timing

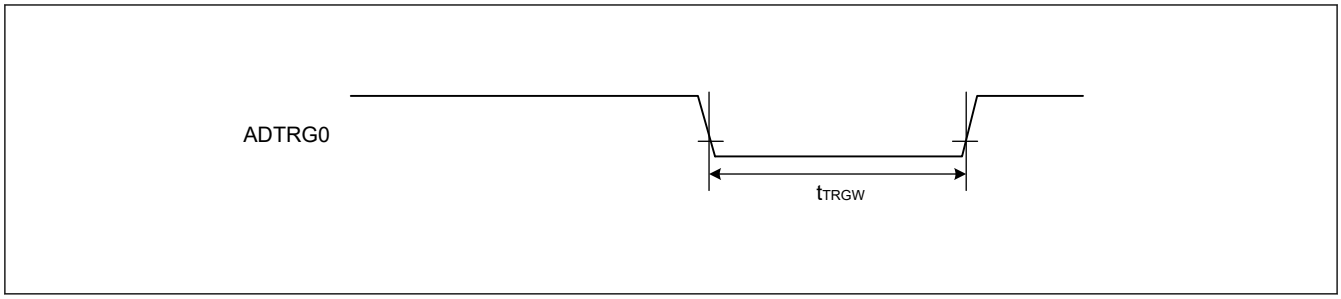


Figure 2.18 ADC12 trigger input timing

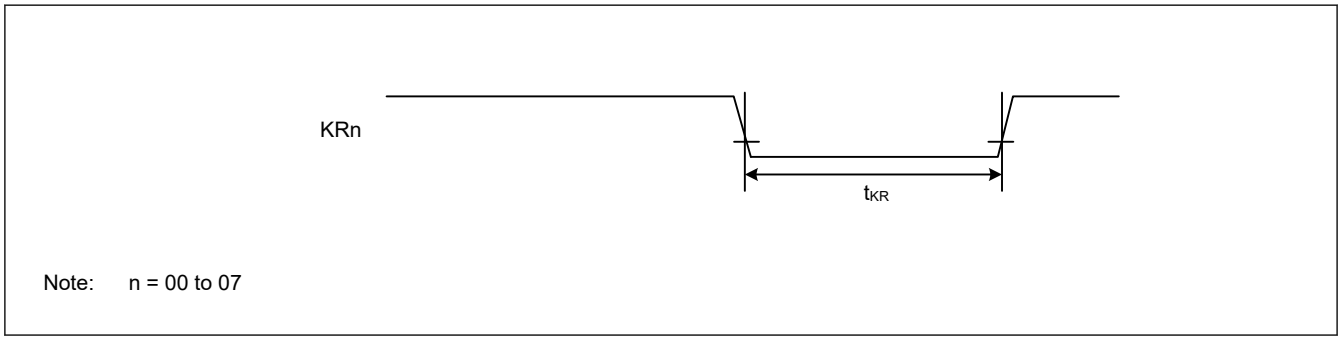


Figure 2.19 Key interrupt input timing

2.3.7 CAC Timing

Table 2.29 CAC timing

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{Pcyc}*1 ≤ t_{CAC}*2	t_{CACREF}	4.5 × t_{CAC} + 3 × t_{Pcyc}	—	—	ns	—
		t_{Pcyc}*1 > t_{CAC}*2		5 × t_{CAC} + 6.5 × t_{Pcyc}	—	—	ns	

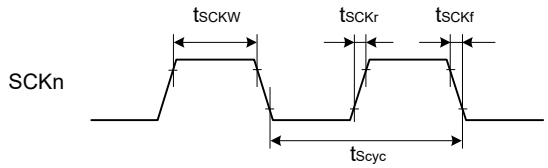
Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. t_{CAC}: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.30 SCI timing (1)

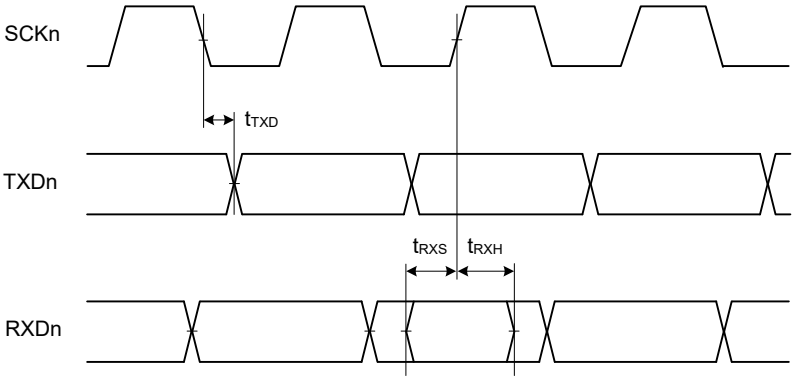
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	125	—	ns	Figure 2.20
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	187.5	—	ns	
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		125	—		
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Output clock fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Transmit data delay time (master)	Clock synchronous	1.8 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	Figure 2.21
			1.6 V ≤ VCC < 1.8 V		—	45		
	Transmit data delay time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		—	55	ns	
			2.4 V ≤ VCC < 2.7 V		—	60		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	—	ns	
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		90	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
	Receive data setup time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		40	—	ns	
			1.6 V ≤ VCC < 2.7 V		45	—		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	—	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	—	ns	



Note: n = 0 to 3, 9

Figure 2.20 SCK clock input timing



Note: n = 0 to 3, 9

Figure 2.21 SCI input/output timing in clock synchronous mode

Table 2.31 SCI timing (2) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

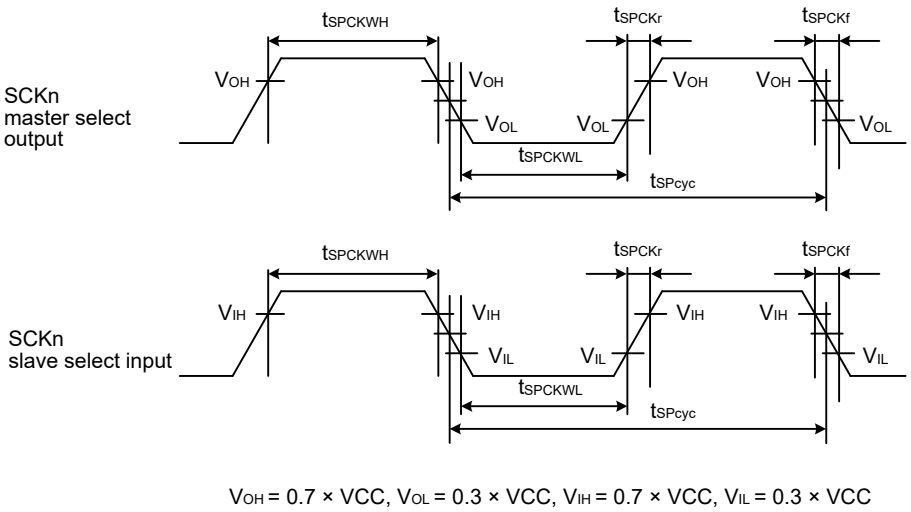
Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	SCK clock cycle output (master)		2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	125	—	ns	Figure 2.22
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	SCK clock cycle input (slave)		2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	45	—	ns	Figure 2.23 to Figure 2.26
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		80	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		40	—		
			1.6 V ≤ VCC < 2.7 V		45	—		
	Data input hold time	Master		t_H	33.3	—	ns	
		Slave			40	—		
	SS input setup time			t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
			1.6 V ≤ VCC < 1.8 V		—	50		
		Slave	2.4 V ≤ VCC ≤ 5.5 V		—	65		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Data output hold time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	-10	—	ns	
			2.4 V ≤ VCC < 2.7 V		-20	—		
			1.8 V ≤ VCC < 2.4 V		-30	—		
			1.6 V ≤ VCC < 1.8 V		-40	—		
		Slave			-10	—		
	Data rise and fall time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
		Slave	1.8 V ≤ VCC ≤ 5.5 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		

Table 2.31 SCI timing (2) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	Slave access time	2.4 V ≤ VCC ≤ 5.5 V		t_{SA}	—	6	t_{Pcyc}	Figure 2.26
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		
	Slave output release time	2.4 V ≤ VCC ≤ 5.5 V		t_{REL}	—	6	t_{Pcyc}	
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		

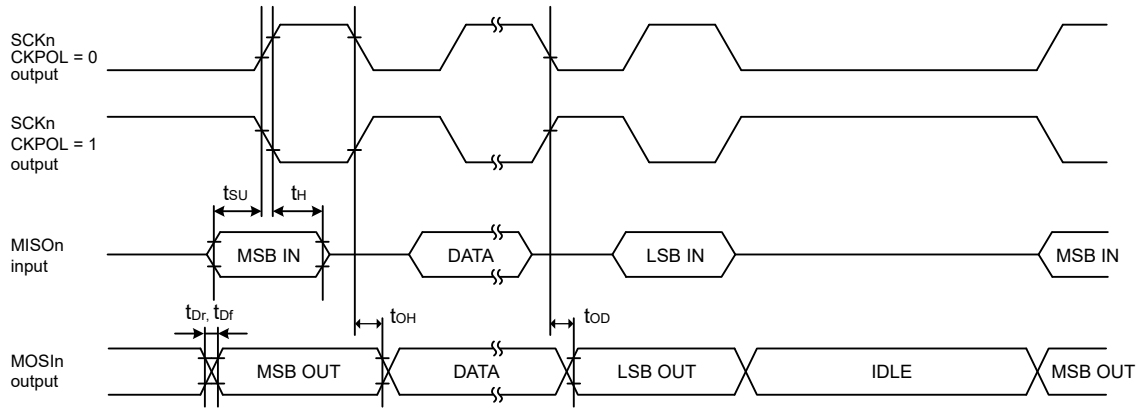
Note 1. t_{Pcyc}: PCLKB cycle.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

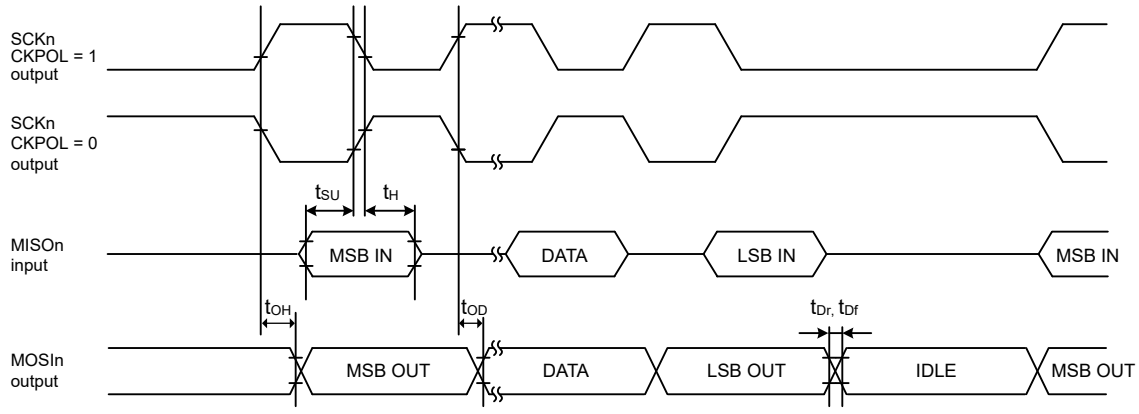
Note: n = 0 to 3, 9

Figure 2.22 SCI simple SPI mode clock timing



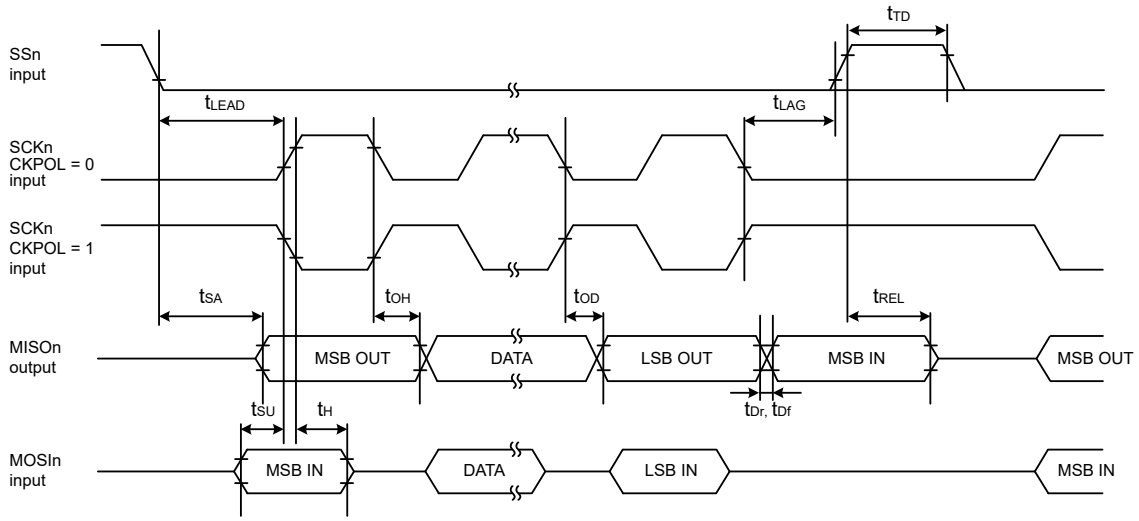
Note: n = 0 to 3, 9

Figure 2.23 SCI simple SPI mode timing (master, CKPH = 1)



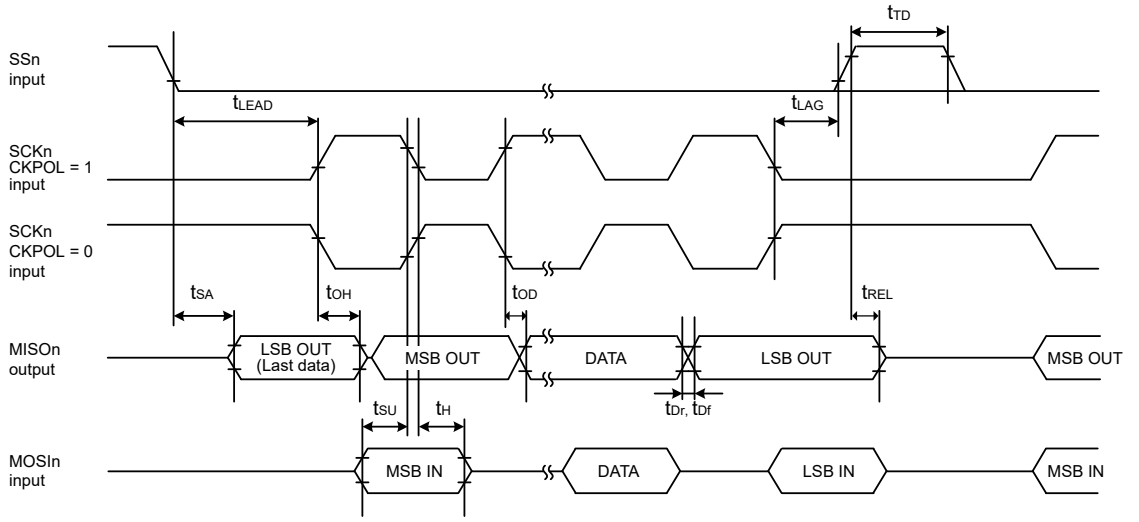
Note: n = 0 to 3, 9

Figure 2.24 SCI simple SPI mode timing (master, CKPH = 0)



Note: n = 0 to 3, 9

Figure 2.25 SCI simple SPI mode timing (slave, CKPH = 1)



Note: n = 0 to 3, 9

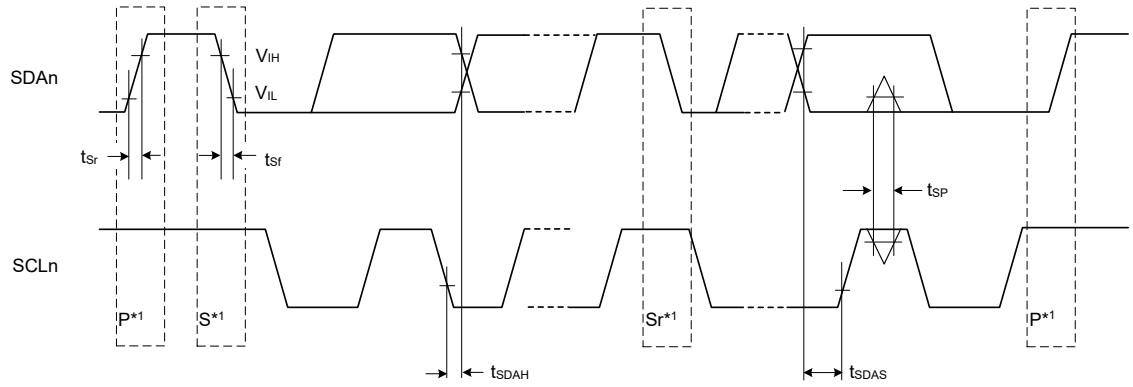
Figure 2.26 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.32 SCI timing (3)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.27
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.27
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	

Note 1. t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.
Note 2. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0 to 3, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.27 SCI simple IIC mode timing

2.3.9 SPI Timing

Table 2.33 SPI timing (1 of 3)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	62.5	—	ns	Figure 2.28 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		125	—		
			1.8 V ≤ VCC < 2.4 V		250	—		
			1.6 V ≤ VCC < 1.8 V		500	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$3 \times t_{Pcyc}$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$3 \times t_{Pcyc}$	—		
	RSPCK clock rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC ≤ 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	0.1	µs/V	

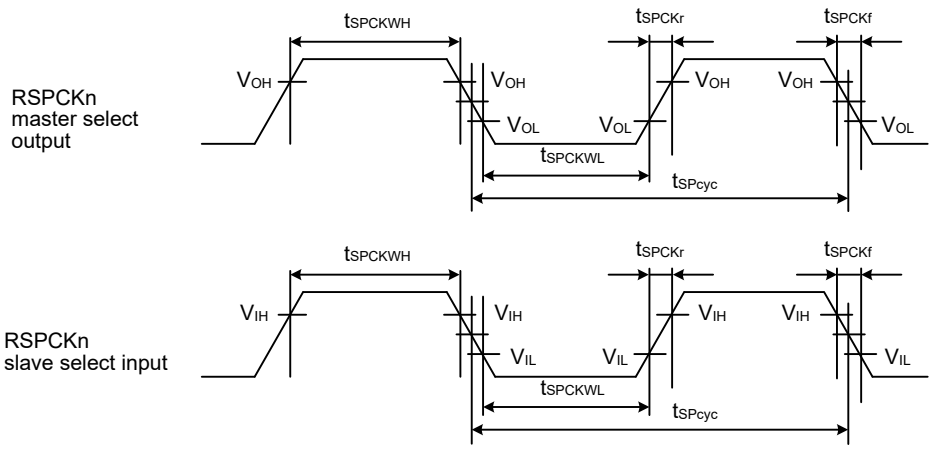
Table 2.33 SPI timing (2 of 3)

Parameter					Symbol	Min	Max	Unit*1	Test conditions
SPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{SU}	10	—	ns	Figure 2.29 to Figure 2.34 C = 30 pF
			2.4 V ≤ VCC < 2.7 V	16 MHz < PCLKB ≤ 32 MHz		30	—		
				PCLKB ≤ 16 MHz		10	—		
			1.8 V ≤ VCC < 2.4 V	16 MHz < PCLKB ≤ 32 MHz		55	—		
				8 MHz < PCLKB ≤ 16 MHz		30	—		
				PCLKB ≤ 8 MHz		10	—		
			1.6 V ≤ VCC < 1.8 V			10	—		
		Slave	2.4 V ≤ VCC ≤ 5.5 V			10	—		
			1.8 V ≤ VCC < 2.4 V			15	—		
			1.6 V ≤ VCC < 1.8 V			20	—		
	Data input hold time	Master (RSPCK is PCLKB/2)			t_{HF}	0	—	ns	
		Master (RSPCK is not PCLKB/2)			t_{H}	t_{Pcyc}	—		
		Slave			t_{H}	20	—		
SPI	SSL setup time	Master	1.8 V ≤ VCC ≤ 5.5 V		t_{LEAD}	-30 + N × t_{SPcyc} *2	—	ns	
			1.6 V ≤ VCC < 1.8 V			-50 + N × t_{SPcyc} *2	—		
		Slave				6 × t_{Pcyc}	—	ns	
	SSL hold time	Master			t_{LAG}	-30 + N × t_{SPcyc} *3	—	ns	
		Slave				6 × t_{Pcyc}	—	ns	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{OD}	—	14	ns	
			2.4 V ≤ VCC < 2.7 V			—	20		
			1.8 V ≤ VCC < 2.4 V			—	25		
			1.6 V ≤ VCC < 1.8 V			—	30		
		Slave	2.7 V ≤ VCC ≤ 5.5 V			—	50		
			2.4 V ≤ VCC < 2.7 V			—	60		
			1.8 V ≤ VCC < 2.4 V			—	85		
			1.6 V ≤ VCC < 1.8 V			—	110		
	Data output hold time	Master			t_{OH}	0	—	ns	
		Slave				0	—		
	Successive transmission delay time	Master			t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave				6 × t_{Pcyc}	—		

Table 2.33 SPI timing (3 of 3)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	MOSI and MISO rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	Figure 2.29 to Figure 2.34 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	SSL rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	Slave access time		2.4 V ≤ VCC ≤ 5.5 V	t_{SA}	—	2 × t_{Pcyc} + 100	ns	Figure 2.33 and Figure 2.34 C = 30 pF
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		
	Slave output release time		2.4 V ≤ VCC ≤ 5.5 V	t_{REL}	—	2 × t_{Pcyc} + 100	ns	
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = A or B

Figure 2.28 SPI clock timing

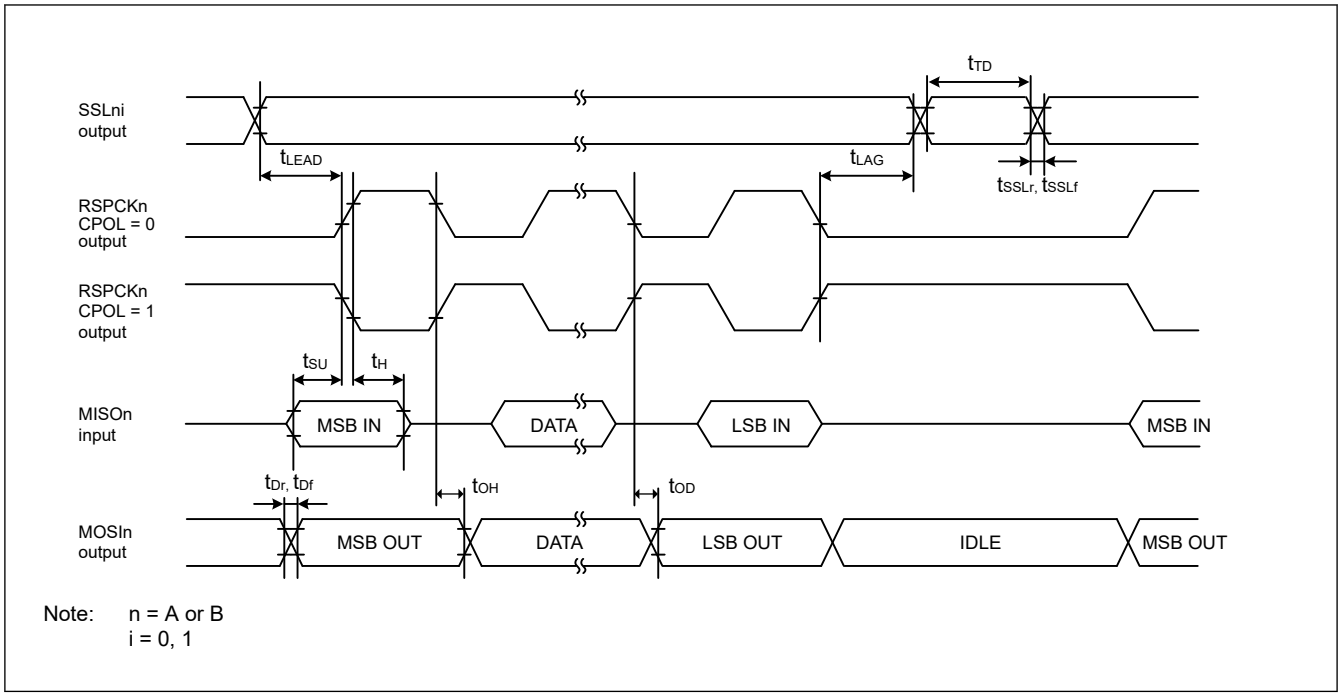


Figure 2.29 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

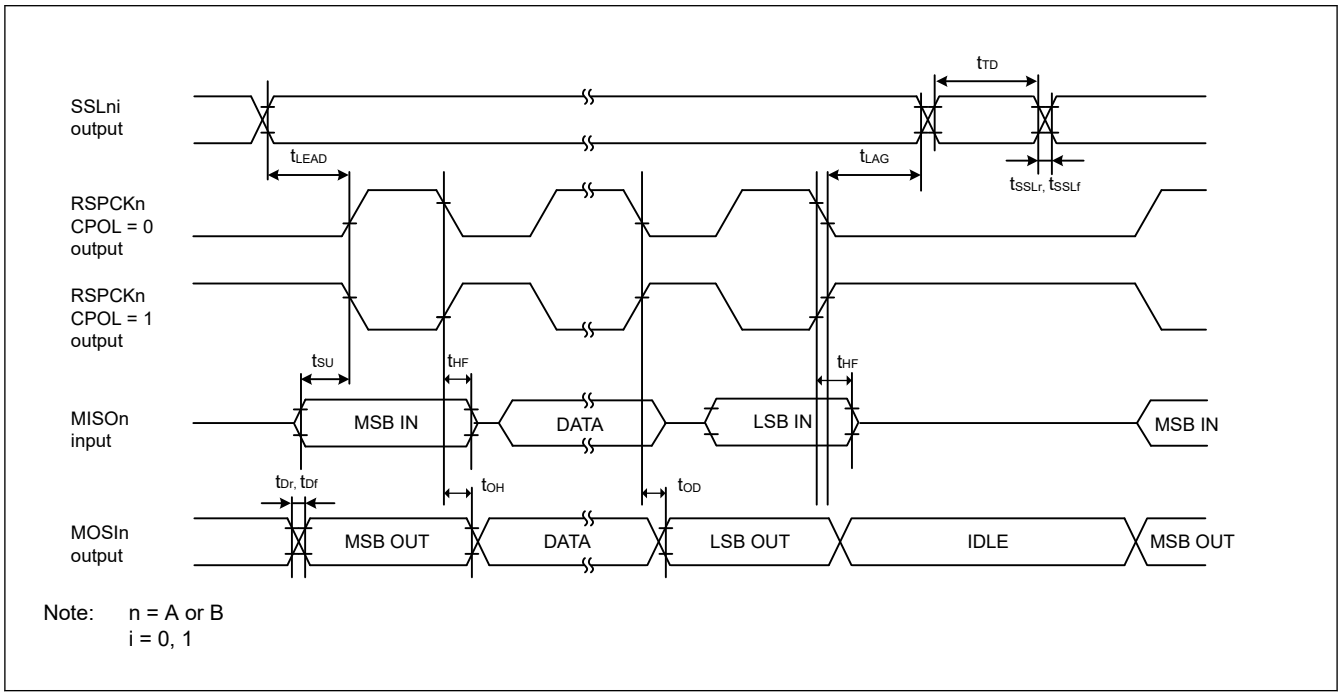
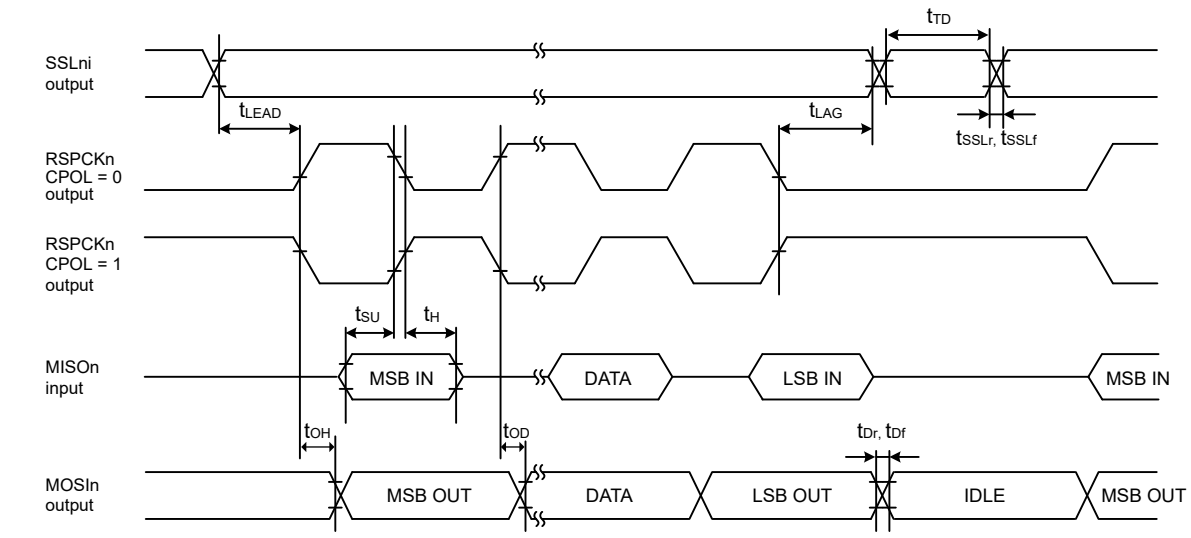
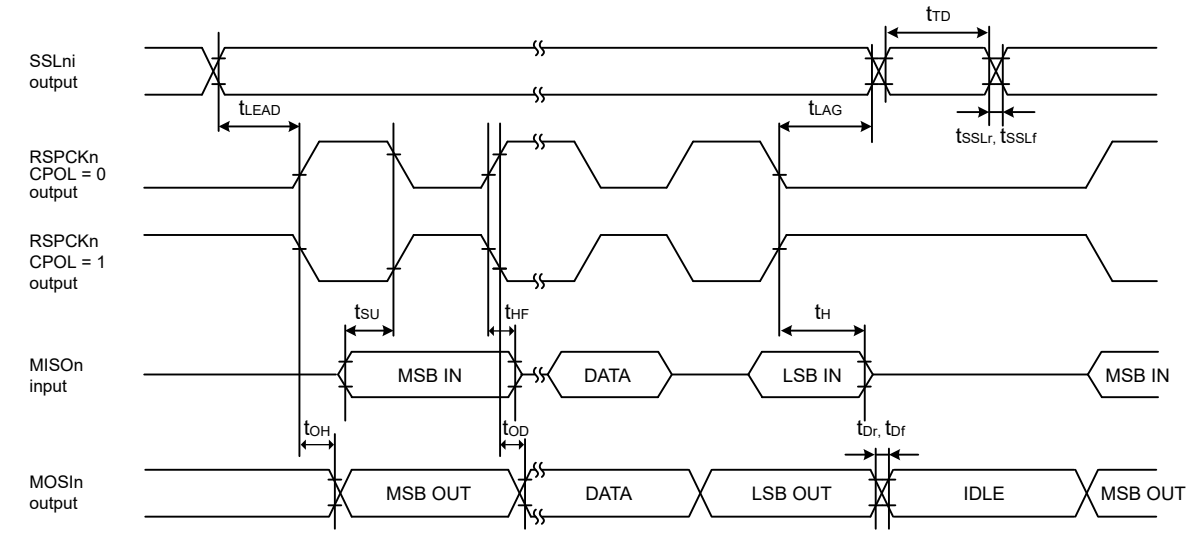


Figure 2.30 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)



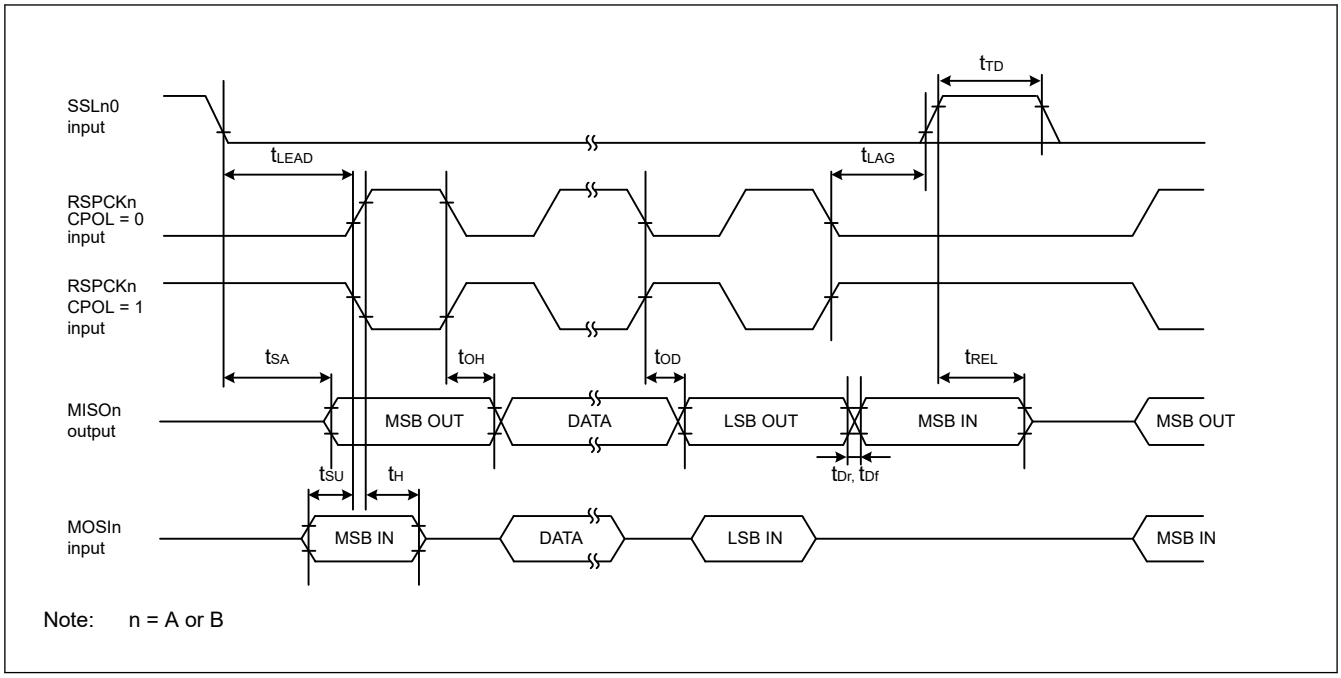
Note: n = A or B
i = 0, 1

Figure 2.31 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)



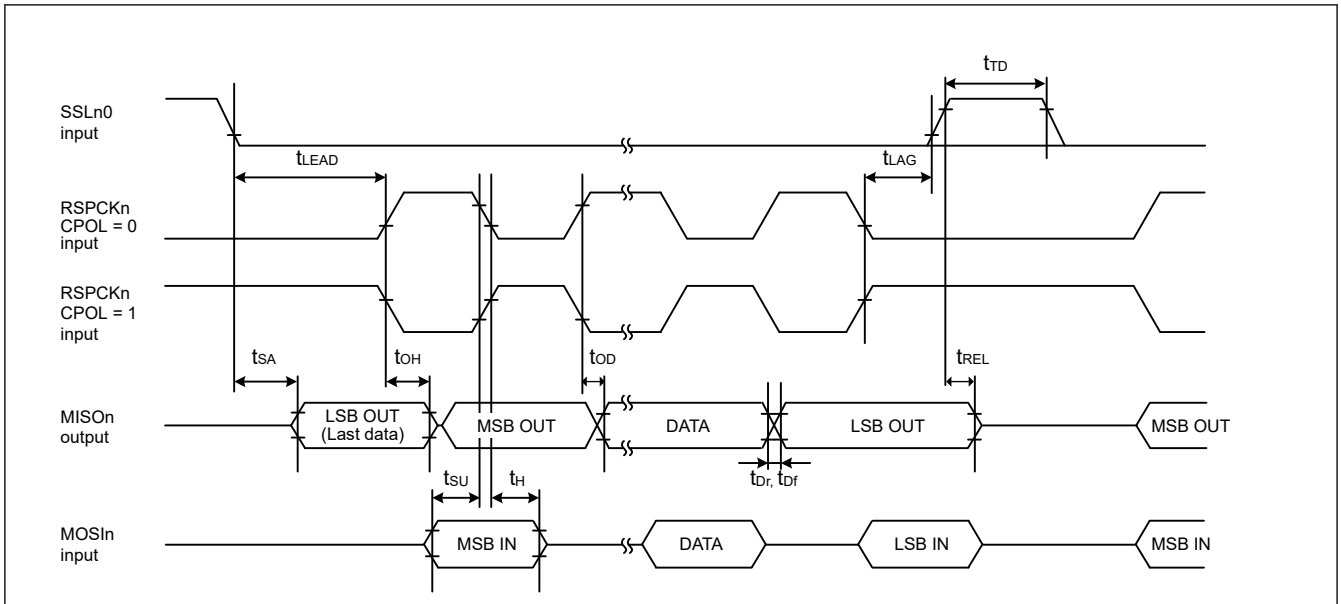
Note: n = A or B
i = 0, 1

Figure 2.32 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)



Note: n = A or B

Figure 2.33 SPI timing (slave, CPHA = 0)



Note: n = A or B

Figure 2.34 SPI timing (slave, CPHA = 1)

2.3.10 IIC Timing

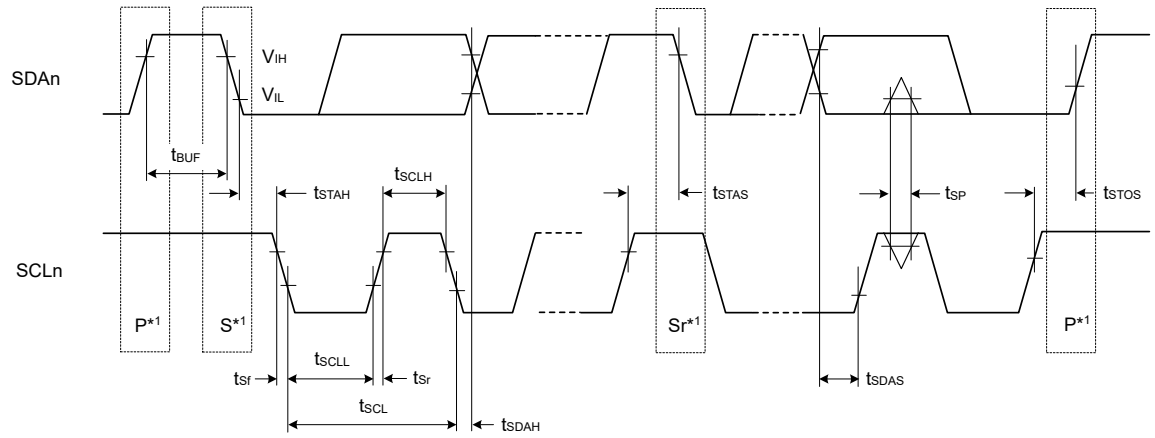
Table 2.34 IIC timing

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.35
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (when wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time (when wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
	START condition input hold time (when wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time (when wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.35
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc}+ 300	—	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.



Note: n = 0, 1
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

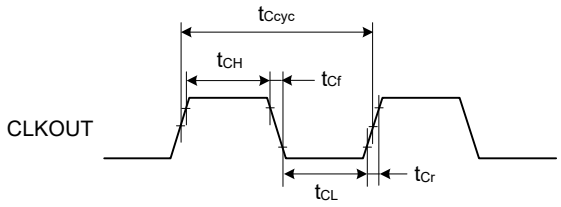
Figure 2.35 I^2C bus interface input/output timing

2.3.11 CLKOUT Timing

Table 2.35 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	Test conditions
CLKOUT	CLKOUT pin output cycle*1	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	—	ns	Figure 2.36
		1.8 V ≤ VCC < 2.7 V		125	—		
		1.6 V ≤ VCC < 1.8 V		250	—		
	CLKOUT pin high pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin low pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin output rise time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		
	CLKOUT pin output fall time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, specifications in Table 2.35 should be satisfied with 45% to 55% of input duty cycle.
Note 2. When MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).



Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 2.36 CLKOUT output timing

2.4 ADC12 Characteristics

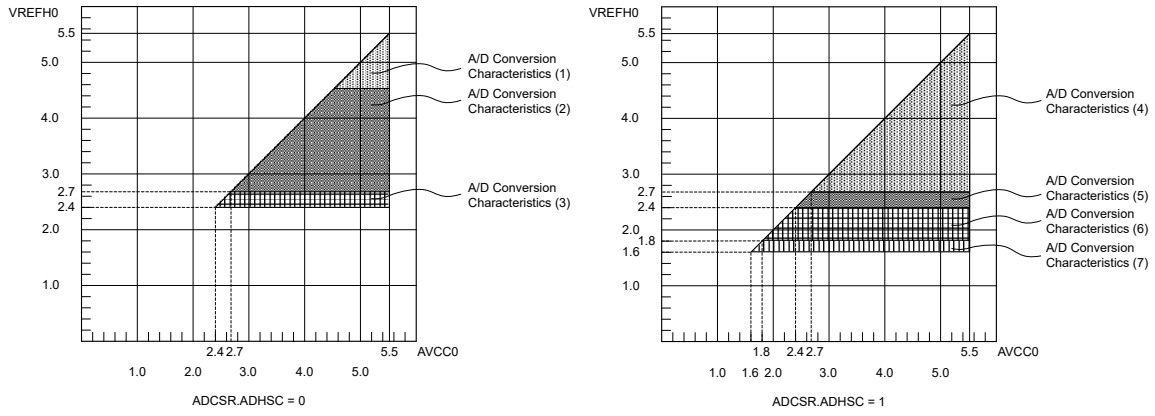


Figure 2.37 AVCC0 to VREFH0 voltage range

Table 2.36 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 4.5 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	64	MHz	ADACSR.ADSAC = 0
				48	MHz	ADACSR.ADSAC = 1
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.3[*3]	kΩ	High-precision channel
		—	—	5.0[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 2.36 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 4.5 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time[*1] (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70 (0.211)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADACSR.ADSAC = 0
		1.34 (0.852)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x36 ADACSR.ADSAC = 0
Conversion time[*1] (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than specified
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.37 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	48	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9[*3]	kΩ	High-precision channel
		—	—	6.0[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 2.37 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time[*1] (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±6.0	LSB	High-precision channel
				±9.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.38 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min		Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	32	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2[*3]	kΩ	High-precision channel
		—	—	7.0[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.00 (0.328)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.94 (1.266)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1

Table 2.38 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min		Max	Unit	Test conditions
Offset error	—	±1.0	±5.5	LSB	High-precision channel
			±7.0	LSB	Other than specified
Full-scale error	—	±1.0	±5.5	LSB	High-precision channel
			±7.0	LSB	Other than specified
Quantization error	—	±0.5	—	LSB	—
Absolute accuracy	—	±2.50	±6.0	LSB	High-precision channel
			±9.0	LSB	Other than specified
DNL differential nonlinearity error	—	±1.0	—	LSB	—
INL integral nonlinearity error	—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.39 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	24	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9[*3]	kΩ	High-precision channel
		—	—	6[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	1.58 (0.438)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		2.0 (0.854)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Full-scale error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—

Table 2.39 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
Absolute accuracy	—	±3.25	±7.0	LSB	High-precision channel
			±10.0	LSB	Other than specified
DNL differential nonlinearity error	—	±1.5	—	LSB	—
INL integral nonlinearity error	—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.40 A/D conversion characteristics (5) in low-power A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	16	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2[*3]	kΩ	High-precision channel
		—	—	7[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	2.38 (0.656)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		3.0 (1.281)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Full-scale error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.25	±7.0	LSB	High-precision channel
				±10.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.5	—	LSB	—
INL integral nonlinearity error		—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.41 A/D conversion characteristics (6) in low-power A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V[*5] (AVCC0 = VCC when VCC < 2.0 V), VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	8	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	6[*3]	kΩ	High-precision channel
		—	—	14[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	4.75 (1.313)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		6.0 (2.563)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±9.5	LSB	High-precision channel
				±13.5	LSB	Other than specified
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

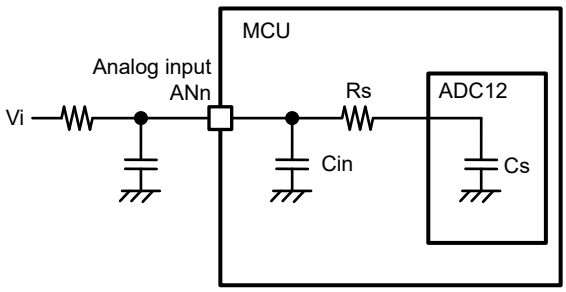
Table 2.42 A/D conversion characteristics (7) in low-power A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 1.6 to 5.5 V[*5] (AVCC0 = VCC when VCC < 2.0 V), VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	4	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	12[*3]	kΩ	High-precision channel
		—	—	28[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	9.5 (2.625)[*4]	—	—	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		12.0 (5.125)[*4]	—	—	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±9.5	LSB	High-precision channel
				±13.5	LSB	Other than specified
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Figure 2.38 shows the equivalent circuit for analog input.



Note: Terminal leakage current is not shown in this figure.

Figure 2.38 Equivalent circuit for analog input

Table 2.43 12-bit A/D converter channel classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN014	AVCC0 = 1.6 to 5.5 V	Pins AN000 to AN014 cannot be used as general I/O, TS transmission, when the A/D converter is in use.
Normal-precision channel	AN017 to AN020		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 1.8 to 5.5 V	—
Temperature sensor input channel	Temperature sensor output	AVCC0 = 1.8 to 5.5 V	—
Input channel from CTSU	CTSU TSCAP voltage	AVCC0 = 1.6 to 5.5 V	—

Table 2.44 A/D internal reference voltage characteristics

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.42	1.48	1.54	V	—
PCLKD (ADCLK) frequency*3	1	—	2	MHz	—
Sampling time*4	5.0	—	—	µs	—

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 1.8 V.
Note 2. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.
Note 3. When the internal reference voltage is selected as the high-potential reference voltage.
Note 4. When the internal reference voltage is converted.

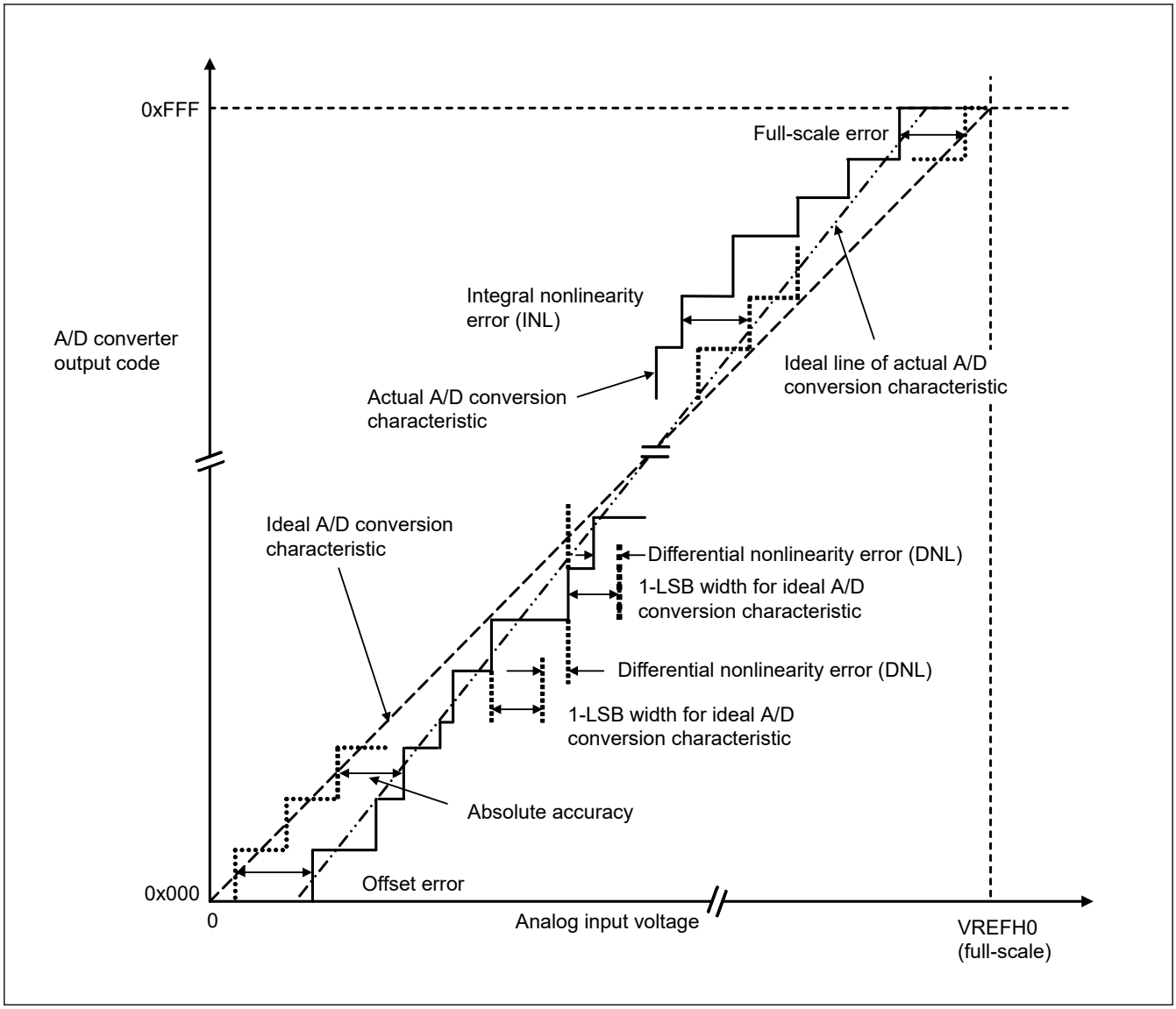


Figure 2.39 Illustration of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

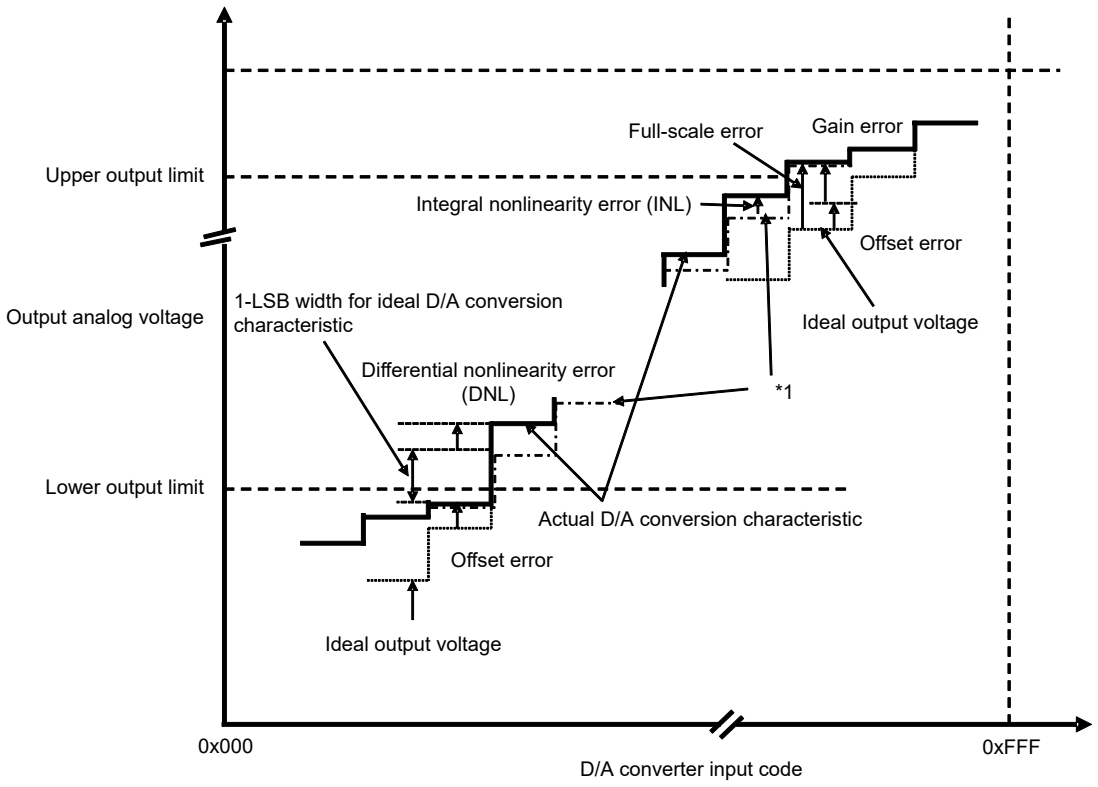
Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.5 DAC12 Characteristics

Table 2.45 12-bit D/A conversion characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V
Reference voltage = AVCC0 or AVSS0 selected

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	bit	—
Resistive load	30	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.35	—	AVCC0-0.47	V	—
DNL differential nonlinearity error	—	±0.5	±2.0	LSB	—
INL integral nonlinearity error	—	±2.0	±8.0	LSB	—
Offset error	—	—	±30	mV	—
Full-scale error	—	—	±30	mV	—
Output impedance	—	5	—	Ω	—
Conversion time	—	—	30	µs	—



Note 1. Ideal D/A conversion output voltage that is adjusted so that offset and full scale errors are zeroed.

Figure 2.40 Illustration of D/A converter characteristic terms

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal output voltage based on the ideal conversion characteristic when the measured offset and full-scale errors are zeroed, and the actual output voltage.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB voltage width based on the ideal D/A conversion characteristics and the width of the actual output voltage.

Offset error

Offset error is the difference between the highest actual output voltage that falls below the lower output limit and the ideal output voltage based on the input code.

Full-scale error

Full-scale error is the difference between the lowest actual output voltage that exceeds the upper output limit and the ideal output voltage based on the input code.

2.6 TSN Characteristics

Table 2.46 TSN characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.5	—	°C	2.4 V or above
		—	± 2.0	—	°C	Below 2.4 V
Temperature slope	—	—	-3.3	—	mV/°C	—
Output voltage (at 25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	—
Sampling time	—	5	—	—	µs	

2.7 OSC Stop Detect Characteristics

Table 2.47 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.41

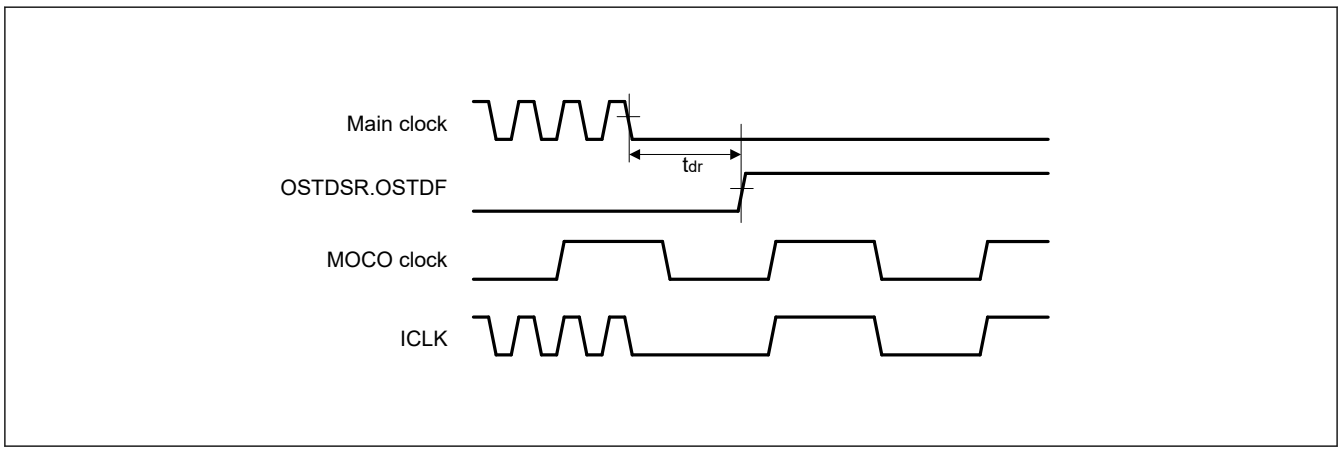


Figure 2.41 Oscillation stop detection timing

2.8 POR and LVD Characteristics

Table 2.48 Power-on reset circuit and voltage detection circuit characteristics (1) (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Power-on reset (POR)	When power supply rise	V_{POR}	1.47	1.51	1.55	V	Figure 2.42
		When power supply fall	V_{PDR}	1.46	1.50	1.54		Figure 2.43
	Voltage detection circuit (LVD0)*2	When power supply rise	V_{det0_0}	3.74	3.91	4.06	V	Figure 2.44 At falling edge VCC
		When power supply fall		3.68	3.85	4.00		
		When power supply rise	V_{det0_1}	2.73	2.9	3.01		
		When power supply fall		2.68	2.85	2.96		
		When power supply rise	V_{det0_2}	2.44	2.59	2.70		
		When power supply fall		2.38	2.53	2.64		
		When power supply rise	V_{det0_3}	1.83	1.95	2.07		
		When power supply fall		1.78	1.90	2.02		
		When power supply rise	V_{det0_4}	1.66	1.75	1.88		
		When power supply fall		1.60	1.69	1.82		
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_0}	4.23	4.39	4.55	V	Figure 2.45 At falling edge VCC
		When power supply fall		4.13	4.29	4.45		
		When power supply rise	V_{det1_1}	4.07	4.25	4.39		
		When power supply fall		3.98	4.16	4.30		
		When power supply rise	V_{det1_2}	3.97	4.14	4.29		
		When power supply fall		3.86	4.03	4.18		
		When power supply rise	V_{det1_3}	3.74	3.92	4.06		
		When power supply fall		3.68	3.86	4.00		
		When power supply rise	V_{det1_4}	3.05	3.17	3.29		
		When power supply fall		2.98	3.10	3.22		
		When power supply rise	V_{det1_5}	2.95	3.06	3.17		
		When power supply fall		2.89	3.00	3.11		
		When power supply rise	V_{det1_6}	2.86	2.97	3.08		
		When power supply fall		2.79	2.90	3.01		
		When power supply rise	V_{det1_7}	2.74	2.85	2.96		
		When power supply fall		2.68	2.79	2.90		

Table 2.48 Power-on reset circuit and voltage detection circuit characteristics (1) (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_8}	2.63	2.75	2.85	V	Figure 2.45 At falling edge VCC
		When power supply fall		2.58	2.68	2.78		
		When power supply rise	V_{det1_9}	2.54	2.64	2.75		
		When power supply fall		2.48	2.58	2.68		
		When power supply rise	V_{det1_A}	2.43	2.53	2.63		
		When power supply fall		2.38	2.48	2.58		
		When power supply rise	V_{det1_B}	2.16	2.26	2.36		
		When power supply fall		2.10	2.20	2.30		
		When power supply rise	V_{det1_C}	1.88	2	2.09		
		When power supply fall		1.84	1.96	2.05		
		When power supply rise	V_{det1_D}	1.78	1.9	1.99		
		When power supply fall		1.74	1.86	1.95		
		When power supply rise	V_{det1_E}	1.67	1.79	1.88		
		When power supply fall		1.63	1.75	1.84		
		When power supply rise	V_{det1_F}	1.65	1.7	1.78		
		When power supply fall		1.60	1.65	1.73		
Voltage detection level*1	Voltage detection circuit (LVD2)*4	When power supply rise	V_{det2_0}	4.20	4.40	4.57	V	Figure 2.46 At falling edge VCC
		When power supply fall		4.11	4.31	4.48		
		When power supply rise	V_{det2_1}	4.05	4.25	4.42		
		When power supply fall		3.97	4.17	4.34		
		When power supply rise	V_{det2_2}	3.91	4.11	4.28		
		When power supply fall		3.83	4.03	4.20		
		When power supply rise	V_{det2_3}	3.71	3.91	4.08		
		When power supply fall		3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.
Note 2. # in the symbol $V_{det0_\#}$ denotes the value of the OFS1.VDSEL0[2:0] bits.
Note 3. # in the symbol $V_{det1_\#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol $V_{det2_\#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 2.49 Power-on reset circuit and voltage detection circuit characteristics (2) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	—	4.3	—	ms	—
	LVD0: disable	t_{POR}	—	3.7	—	ms	—
Wait time after voltage monitor 0, 1, 2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	—	1.4	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.7	—	ms	—
Power-on reset response delay time*3		t_{det}	—	—	500	µs	Figure 2.42, Figure 2.43
LVD0 response delay time*3		t_{det}	—	—	500	µs	Figure 2.44
LVD1 response delay time*3		t_{det}	—	—	350	µs	Figure 2.45
LVD2 response delay time*3		t_{det}	—	—	600	µs	Figure 2.46
Minimum VCC down time		t_{VOFF}	500	—	—	µs	Figure 2.42, VCC = 1.0 V or above
Power-on reset enable time		$t_{W\ (POR)}$	1	—	—	ms	Figure 2.43, VCC = below 1.0 V

Table 2.49 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
LVD1 operation stabilization time (after LVD1 is enabled)	$T_{d\ (E-A)}$	—	—	300	µs	Figure 2.45
LVD2 operation stabilization time (after LVD2 is enabled)	$T_{d\ (E-A)}$	—	—	1200	µs	Figure 2.46
Hysteresis width (POR)	V_{PORH}	—	10	—	mV	—
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	—	60	—	mV	LVD0 selected
		—	110	—		V_{det1_0} to V_{det1_2} selected
		—	70	—		V_{det1_3} to V_{det1_9} selected
		—	60	—		V_{det1_A} to V_{det1_B} selected
		—	50	—		V_{det1_C} to V_{det1_F} selected
		—	90	—		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

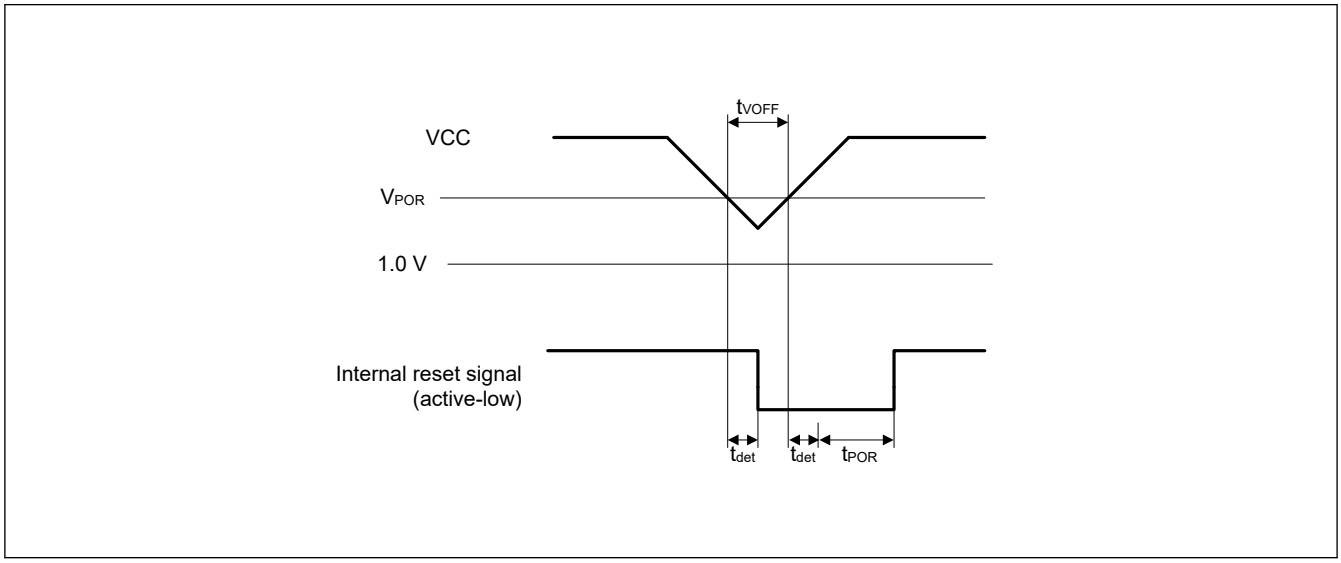
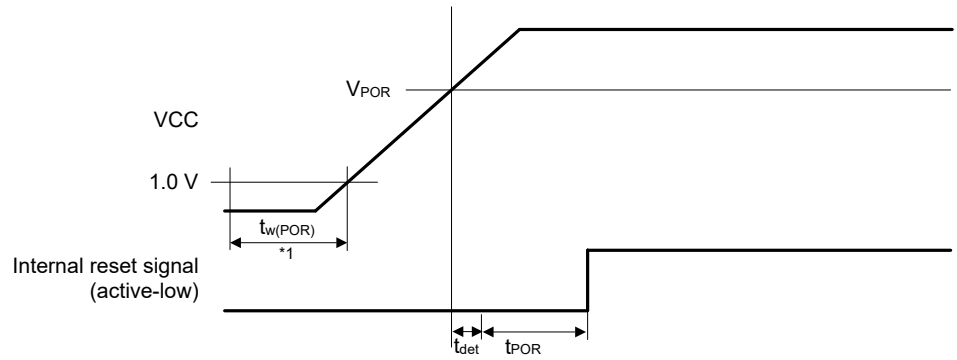


Figure 2.42 Voltage detection reset timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.43 Power-on reset timing

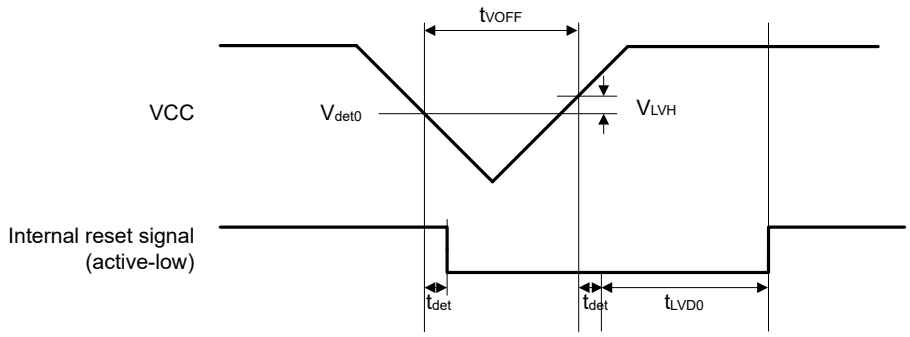


Figure 2.44 Voltage detection circuit timing (V_{det0})

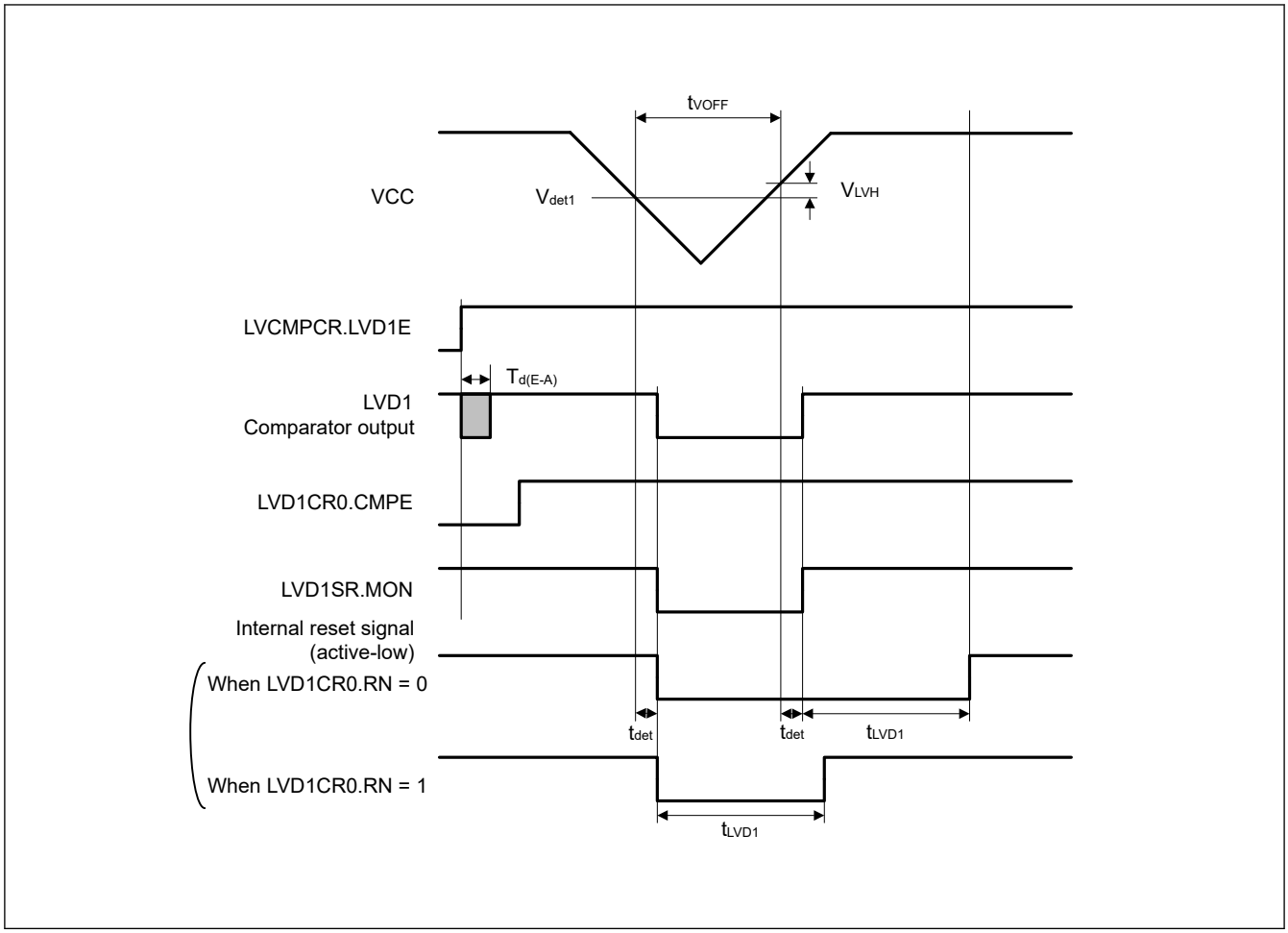


Figure 2.45 Voltage detection circuit timing (V_{det1})

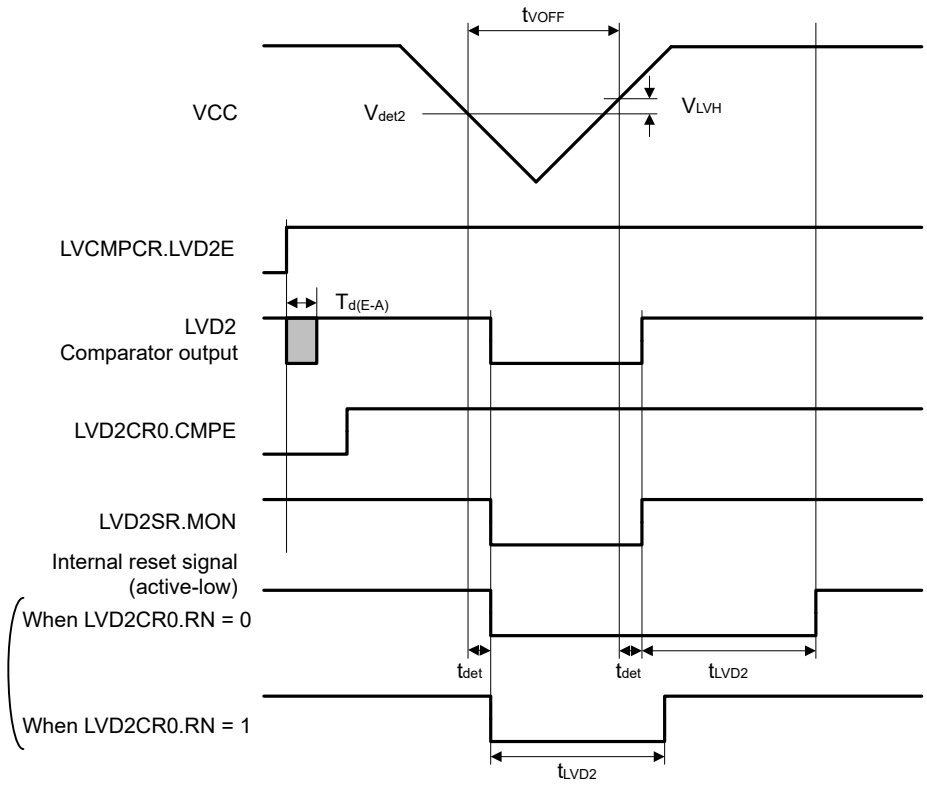


Figure 2.46 Voltage detection circuit timing (V_{det2})

2.9 CTSU Characteristics

Table 2.50 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	—

2.10 Comparator Characteristics

Table 2.51 ACMPLP characteristics (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range		V_{REF}	0	—	VCC-1.4	V	—
Input voltage range		V_I	0	—	VCC	V	—
Internal reference voltage*1		—	1.34	1.44	1.54	V	—
Output delay time	High-speed mode	T_d	—	—	1.2	µs	VCC = 3.0 V
	Low-speed mode		—	—	9	µs	
	Window mode		—	—	2	µs	
Offset voltage	High-speed mode	—	—	—	50	mV	—
	Low-speed mode	—	—	—	40	mV	—
	Window mode	—	—	—	60	mV	—

Table 2.51 ACMPLP characteristics (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Internal reference voltage for window mode		V_{RFH}	—	0.76 × VCC	—	V	—
		V_{RFL}	—	0.24 × VCC	—	V	—
Operation stabilization wait time	High-speed mode	T_{cmp}	100	—	—	µs	—
	Low-speed mode		200	—	—		

Note 1. The internal reference voltage can be selected as ACMPLP reference voltage only when 2.94 V ≤ VCC ≤ 5.50 V.

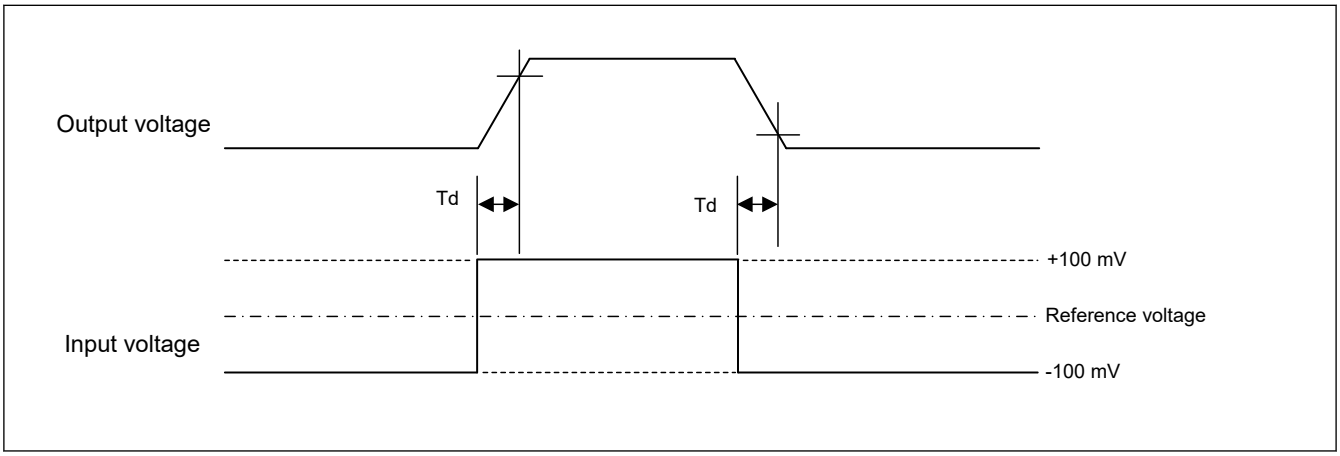


Figure 2.47 Output delay time

2.11 Flash Memory Characteristics

2.11.1 Code Flash Memory Characteristics

Table 2.52 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	—
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20*2 *3	—	—	Year	T_a = +85°C T_a = +105°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.53 Code flash characteristics (2) (1 of 2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	34	321	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	5.6	215	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	8.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	240	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	10.5	µs

Table 2.53 Code flash characteristics (2) (2 of 2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
Access window information program Start-up area selection and security setting time	t_{AWSSAS}	—	21.2	570	—	11.4	423	ms
OCD/serial programmer ID setting time*1	t_{OSIS}	—	84.7	2280	—	45.3	1690	ms
Flash memory mode transition wait time 1	t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2	t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.

Table 2.54 Code flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz*2			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	39	356	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	6.2	227	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	11.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	534	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	11.7	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	12.2	435	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	48.7	1740	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.
Note 2. When 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V

Table 2.55 Code flash characteristics (4) (1 of 2)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	57	502	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	8.8	280	ms

Table 2.55 Code flash characteristics (4) (2 of 2)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	23.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	1841	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	16.2	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	15.9	491	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	63.5	1964	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.

2.11.2 Data Flash Memory Characteristics

Table 2.56 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	—
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2 *3	—	—	Year	Ta = +85°C Ta = +105°C
	After 100000 times of N_{DPEC}		5*2 *3	—	—	Year	
	After 1000000 times of N_{DPEC}		—	1*2 *3	—	Year	Ta = +25°C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,024 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.57 Data flash characteristics (2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 4 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	45	404	—	34	321	µs
Erasure time	1-KB	t_{DE1K}	—	8.8	280	—	6.1	224	ms
Blank check time	1-byte	t_{DBC1}	—	—	15.2	—	—	8.3	µs
	1-KB	t_{DBC1K}	—	—	1832	—	—	466	µs
Suspended time during erasing		t_{DSED}	—	—	13.2	—	—	10.5	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.58 Data flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 4 MHz			ICLK = 8 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	45	404	—	39	356	µs
Erasure time	1-KB	t_{DE1K}	—	8.8	280	—	7.3	248	ms
Blank check time	1-byte	t_{DBC1}	—	—	15.2	—	—	11.3	µs
	1-KB	t_{DBC1K}	—	—	1.84	—	—	1.06	ms
Suspended time during erasing		t_{DSED}	—	—	13.2	—	—	11.7	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. When 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V

Table 2.59 Data flash characteristics (4)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	86	732	—	57	502	µs
Erasure time	1-KB	t_{DE1K}	—	19.7	504	—	12.4	354	ms
Blank check time	1-byte	t_{DBC1}	—	—	46.5	—	—	23.3	µs
	1-KB	t_{DBC1K}	—	—	7.3	—	—	3.66	ms
Suspended time during erasing		t_{DSED}	—	—	22.3	—	—	16.2	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 2 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.11.3 Serial Wire Debug (SWD)

Table 2.60 SWD characteristics (1)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 2.48
SWCLK clock high pulse width	t_{SWCKH}	35	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	16	—	—	ns	Figure 2.49
SWDIO hold time	t_{SWDH}	16	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	70	ns	

Table 2.61 SWD characteristics (2)

Conditions: VCC = AVCC0 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	—	—	ns	Figure 2.48
SWCLK clock high pulse width	t_{SWCKH}	120	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	50	—	—	ns	Figure 2.49
SWDIO hold time	t_{SWDH}	50	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	170	ns	

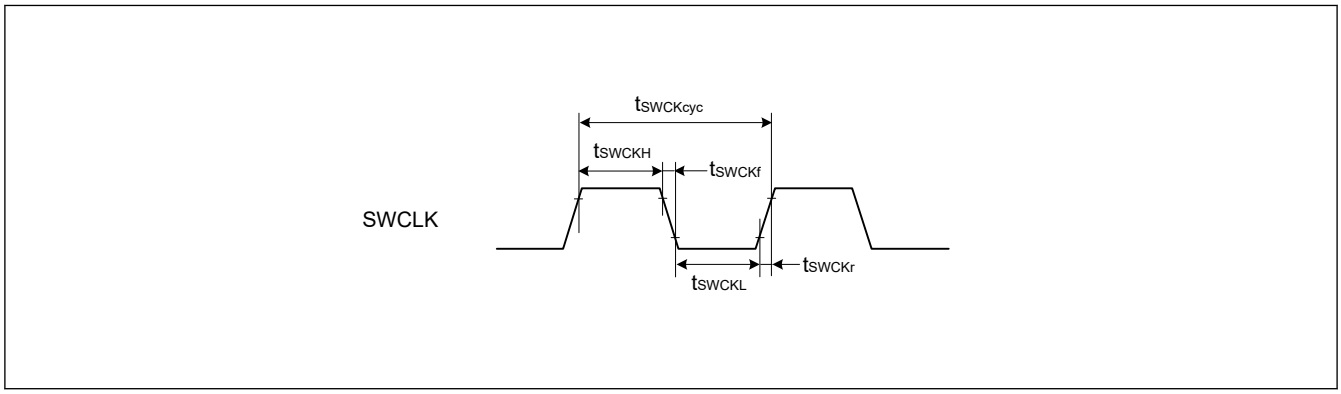


Figure 2.48 SWD SWCLK timing

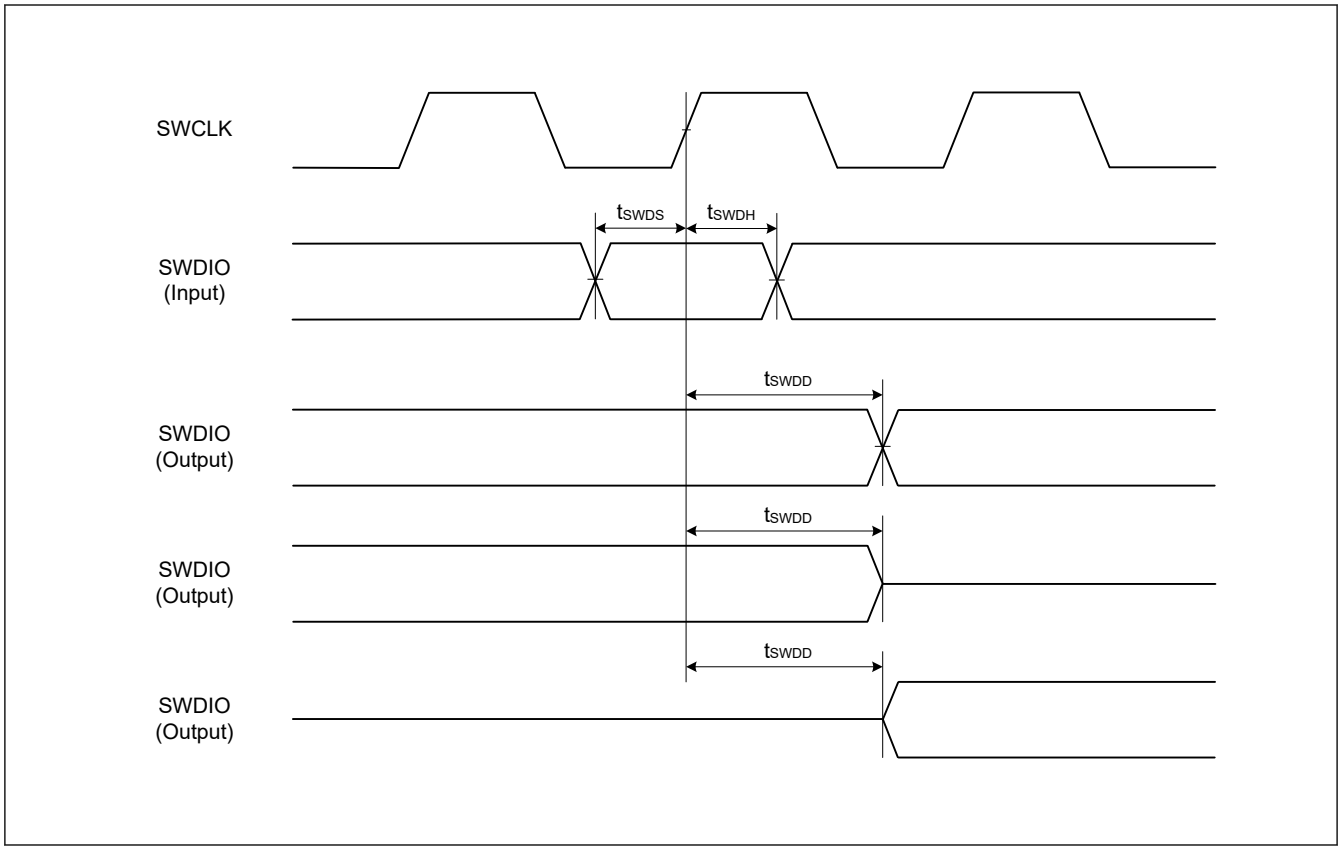


Figure 2.49 SWD input/output timing

2.12 DCDC Characteristics

Table 2.62 DCDC characteristics

Conditions: VCC = AVCC0 = VCC_DCDC = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
DCDC output Voltage	—	1.42	1.50	1.58	V	—
Power switching stabilization time	—	—	—	22	µs	Switch from LDO power to DCDC power
	—	—	—	60	µs	Switch from DCDC power to LDO power
	—	—	—	60	µs	Switch from DCDC power to LDO power in the LC boost mode

Appendix 1. Port States in each Processing Mode

Table 1.1 Port states in each processing mode (1 of 4)

Port name	Reset	Software Standby Mode
P000/AN000/TS21/IRQ6	Hi-Z	Keep-O*1
P001/AN001/TS22/IRQ7	Hi-Z	Keep-O*1
P002/AN002/TS23/IRQ2	Hi-Z	Keep-O*1
P003/AN003/TS24	Hi-Z	Keep-O
P004/AN004/TS25/IRQ3	Hi-Z	Keep-O*1
P005/AN011	Hi-Z	Keep-O
P006/AN012	Hi-Z	Keep-O
P007/AN013	Hi-Z	Keep-O
P008/AN014	Hi-Z	Keep-O
P010/AN005/TS30-CFC	Hi-Z	Keep-O
P011/AN006/TS31-CFC	Hi-Z	Keep-O
P012/AN007/TS32-CFC	Hi-Z	Keep-O
P013/AN008/TS33-CFC	Hi-Z	Keep-O
P014/AN009/DA0	Hi-Z	[DA0 output (DACE0 = 1)] DA0 output retained [Other than the above (DACE0 = 0)] Keep-O
P015/AN010/TS28-CFC/IRQ7_A	Hi-Z	Keep-O*1
P100/CMPIN0/TS26-CFC/AGTIO0_A/GTETRGA_A/GTIOC5B_A/RXD0_A/ MISO0_A/SCL0_A/SCK1_A/SCL1_B/MISOA_A/KRM00/IRQ2_A	Hi-Z	[AGTIO0_A output selected] AGTIO0_A output*2 [Other than the above] Keep-O*1
P101/CMPREF0/TS16-CFC/AGTEE0/GTETRGB_A/GTIOC5A_A/TXD0_A/ MOSI0_A/SDA0_A/CTS1_RTS1_A/SDA1_B/MOSIA_A/KRM01/IRQ1_A	Hi-Z	Keep-O*1
P102/CMPIN1/ADTRG0_A/TS15-CFC/AGTO0/GTOWLO_A/GTIOC2B_A/ CRX0_C /SCK0_A/TXD2_D/MOSI2_D/SDA2_D/RSPCKA_A/KRM02	Hi-Z	[AGTO0 selected] AGTO0 output*2 [Other than the above] Keep-O*1
P103/CMPREF1/TS14-CFC/GTOWUP_A/GTIOC2A_A/CTX0_C/ CTS0_RTS0_A/SSLA0_A/KRM03	Hi-Z	Keep-O*1
P104/TS13-CFC/GTETRGB_B/GTIOC1B_C/RXD0_C/MISO0_C/SCL0_C/ SSLA1_A/KRM04/IRQ1_B	Hi-Z	Keep-O*1
P105/TS34-CFC/GTETRGA_C/GTIOC1A_C/SSLA2_A/KRM05/IRQ0_B	Hi-Z	Keep-O*1
P106/GTIOC8B_A/SSLA3_A/KRM06	Hi-Z	Keep-O*1
P107/GTIOC8A_A/KRM07	Hi-Z	Keep-O*1
P108/SWDIO/GTOULO_C/GTIOC0B_A/CTS9_RTS9_B/SSLB0_B	Pull-up	Keep-O
P109/TS10-CFC/GTOVUP_A/GTIOC1A_A/CTX0_A//SCK1_E/TXD9_B/ MOSI9_B/SDA9_B/MOSIB_B/CLKOUT_B	Hi-Z	[CLKOUT selected] CLKOUT output [Other than the above] Keep-O
P110/TS11-CFC/GTOVLO_A/GTIOC1B_A/CRX0_A/CTS2_RTS2_B/RXD9_B/ MISO9_B/SCL9_B/MISOB_B/IRQ3_A/VCOUT	Hi-Z	[ACMPLP selected] VCOUT output [Other than the above] Keep-O*1

Table 1.1 Port states in each processing mode (2 of 4)

Port name	Reset	Software Standby Mode
P111/TS12-CFC/AGTOA0/GTIOC3A_A/SCK2_B/SCK9_B/RSPCKB_B/ IRQ4_A	Hi-Z	[AGTOA0 selected] AGTOA0 output*2 [Other than the above] Keep-O*1
P112/TSCAP_C/AGTOB0/GTIOC3B_A/TXD2_B/MOSI2_B/SDA2_B/SCK1_D/ SSLB0_C	Hi-Z	[AGTOB0 selected] AGTOB0 output*2 [Other than the above] Keep-O
P113/TS27-CFC/GTIOC2A_C	Hi-Z	Keep-O
P114/TS29-CFC/GTIOC2B_C	Hi-Z	Keep-O
P115/TS35-CFC/GTIOC4A_C	Hi-Z	Keep-O
P200/NMI	Hi-Z	Hi-Z
P201/MD	Pull-up	Keep-O
P202/SCK2_A/RXD9_A/MISO9_A/SCL9_A/MISOB_A	Hi-Z	Keep-O
P203/CTS2_RTS2_A/TXD9_A/MOSI9_A/SDA9_A/MOSIB_A	Hi-Z	Keep-O
P204/CACREF_A/TS0/AGTIO1_A/GTIW_A/GTIOC4B_B/SCK0_D/SCK9_A/ SCL0_B/RSPCKB_A	Hi-Z	[AGTIO1_A output selected] AGTIO1_A output*2 [Other than the above] Keep-O*1
P205/AGTO1/GTIV_A/GTIOC4A_B/TXD0_D/MOSI0_D/SDA0_D/ CTS9_RTS9_A/ SCL1_A/SSLB0_A/IRQ1/CLKOUT_A	Hi-Z	[AGTO1 selected] AGTO1 output*2 [CLKOUT selected] CLKOUT output [Other than the above] Keep-O*1
P206/GTIU_A/RXD0_D/MISO0_D/SCL0_D/SDA1_A/SSLB1_A/IRQ0	Hi-Z	Keep-O*1
P207	Hi-Z	Keep-O
P208/AGTOB0_A	Hi-Z	[AGTOB0_A selected] AGTOB0_A output*2 [Other than the above] Keep-O
P212/EXTAL /AGTEE1/GTETRGB_D/GTIOC0B_D/RXD1_A/MISO1_A/ SCL1_A/IRQ3_B	Hi-Z	Keep-O*1
P213/XTAL /GTETRGA_D/GTIOC0A_D/TXD1_A/MOSI1_A/SDA1_A/IRQ2_B	Hi-Z	Keep-O*1
P214/XCOUT, P215/XCIN	Hi-Z	[Sub-clock Oscillator selected] Sub-clock Oscillator is operating [Other than the above] Hi-Z
P300/SWCLK/GTOUUP_C/GTIOC0A_A/SSLB1_B	Pull-up	Keep-O
P301/TS9-CFC/AGTIO0_D/GTOULO_A/GTIOC4B_A/RXD2_A/MISO2_A/ SCL2_A/CTS9_RTS9_D/SSLB2_B/IRQ6_A	Hi-Z	[AGTIO0_D output selected] AGTIO0_D output*2 [Other than the above] Keep-O*1
P302/TS8-CFC/GTOUUP_A/GTIOC4A_A/TXD2_A/MOSI2_A/SDA2_A/ SSLB3_B/IRQ5_A	Hi-Z	Keep-O*1
P303/TS2-CFC/GTIOC7B_A	Hi-Z	Keep-O
P304/GTIOC7A_A	Hi-Z	Keep-O
P305, P306, P307	Hi-Z	Keep-O

Table 1.1 Port states in each processing mode (3 of 4)

Port name	Reset	Software Standby Mode
P400/CACREF_C/AGTIO1_C/GTIOC6A_A/SCK0_B/SCK1_B/SCL0_A/ IRQ0_A	Hi-Z	[AGTIO1_C output selected] AGTIO1_C output*2 [Other than the above] Keep-O*1
P401/GTETRGA_B/GTIOC6B_A/CTX0_B/CTS0_RTS0_B/TXD1_B/MOSI1_B/ SDA1_B/SDA0_A/IRQ5	Hi-Z	Keep-O*1
P402/TS18/AGTIO0_E/AGTIO1_D/CRX0_B/RXD1_B/MISO1_B/SCL1_B/ IRQ4	Hi-Z	[AGTIO0_E, AGTIO1_D output selected] AGTIO0_E, AGTIO1_D output*2 [Other than the above] Keep-O*1
P403/TS17/AGTIO0_F/AGTIO1_E/GTIOC3A_B/CTS1_RTS1_B	Hi-Z	[AGTIO0_F, AGTIO1_E output selected] AGTIO0_F, AGTIO1_E output*2 [Other than the above] Keep-O*1
P404/GTIOC3B_B, P405/GTIOC1A_B, P406/GTIOC1B_B	Hi-Z	Keep-O
P407/ADTRG0_B/AGTIO0_C/RTCOUT/CTS0_RTS0_D/SDA0_B/SSLB3_A	Hi-Z	[AGTIO0_C output selected] AGTIO0_C output*2 [RTCOUT selected] RTCOUT output [Other than the above] Keep-O*1
P408/TS4/GTOWLO_B/GTIOC5B_B/CTS1_RTS1_D/RXD3_A/MISO3_A/ SCL3_A/SCL0_C/IRQ7_B	Hi-Z	Keep-O*1
P409/TS5/GTOWUP_B/GTIOC5A_B/TXD3_A/MOSI3_A/SDA3_A/IRQ6_B	Hi-Z	Keep-O*1
P410/TS6/AGTOB1/GTOVLO_B/GTIOC9B_A/RXD0_B/MISO0_B/SCL0_B/ SCK3_A/MISOA_B/IRQ5_B	Hi-Z	[AGTOB1 selected] AGTOB1 output*2 [Other than the above] Keep-O*1
P411/TS7/AGTOA1/GTOVUP_B/GTIOC9A_A/TXD0_B/MOSI0_B/SDA0_B/ CTS3_RTS3_A/MOSIA_B/IRQ4_B	Hi-Z	[AGTOA1 selected] AGTOA1 output*2 [Other than the above] Keep-O*1
P412/GTOULO_B/SCK0_E/RSPCKA_B	Hi-Z	Keep-O
P413/GTOUUP_B/CTS0_RTS0_E/SSLA0_B	Hi-Z	Keep-O
P414/GTIOC0B_C/SSLA1_B	Hi-Z	Keep-O
P415/GTIOC0A_C/SSLA2_B	Hi-Z	Keep-O
P500/GTIU_B/GTIOC2A_B	Hi-Z	Keep-O
P501/AN017/GTIV_B/GTIOC2B_B/TXD1_C/MOSI1_C/SDA1_C	Hi-Z	Keep-O
P502/AN018/GTIW_B/GTIOC3B_C/RXD1_C/MISO1_C/SCL1_C	Hi-Z	Keep-O
P503/AN019/GTETRGA_E/SCK1_C	Hi-Z	Keep-O
P504/AN020/GTETRGB_E/CTS1_RTS1_C	Hi-Z	Keep-O
P505	Hi-Z	Keep-O
P600/GTIOC6B_C/SCK9_C	Hi-Z	Keep-O
P601/GTIOC6A_C/RXD9_C/MISO9_C/SCL9_C	Hi-Z	Keep-O
P602/GTIOC7B_B/TXD9_C/MOSI9_C/SDA9_C	Hi-Z	Keep-O
P603/GTIOC7A_B/CTS9_RTS9_C	Hi-Z	Keep-O
P608/GTIOC4B_C	Hi-Z	Keep-O

Table 1.1 Port states in each processing mode (4 of 4)

Port name	Reset	Software Standby Mode
P609/GTIOC5A_C	Hi-Z	Keep-O
P610/GTIOC5B_C	Hi-Z	Keep-O
P708/RXD1_D/MISO1_D/SCL1_D/SSLA3_B	Hi-Z	Keep-O
P714	Hi-Z	Keep-O
P808, P809	Hi-Z	Keep-O

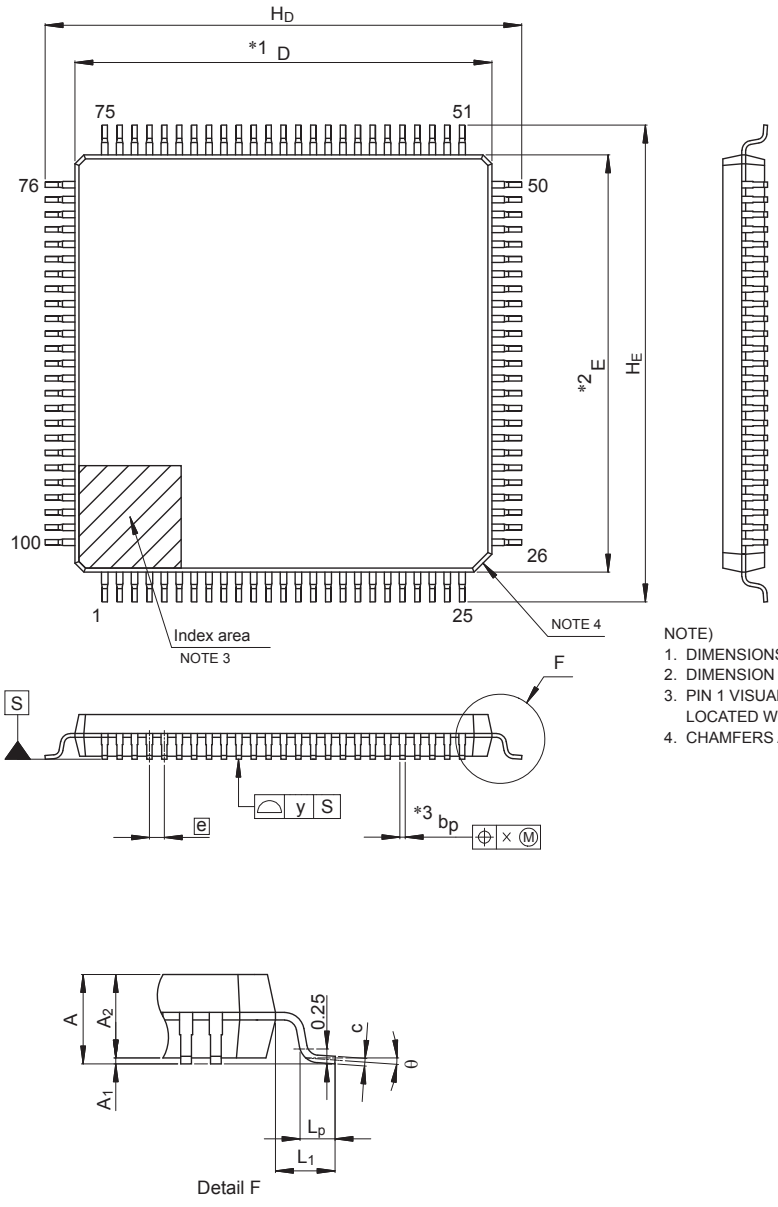
Note: Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins become high-impedance.
Note 1. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 2. AGTIO output is enabled while LOCO or SOSC is selected as a count source.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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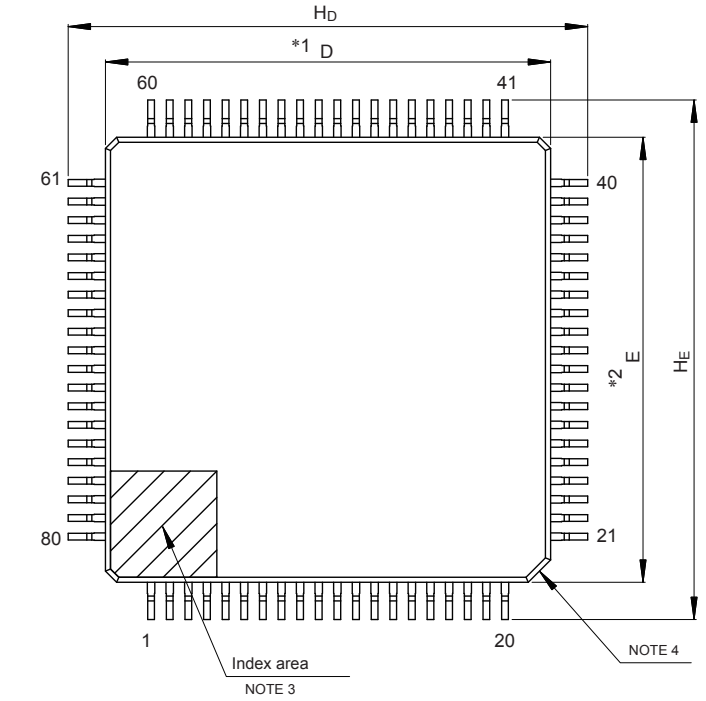
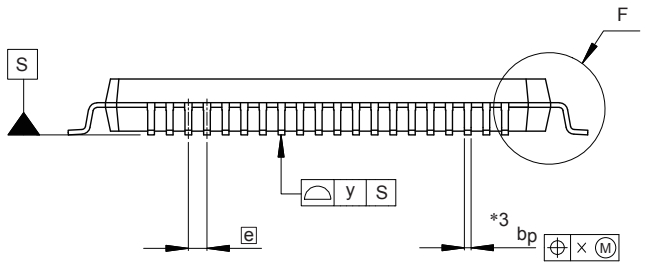
Figure 2.1 LQFP 100-pin

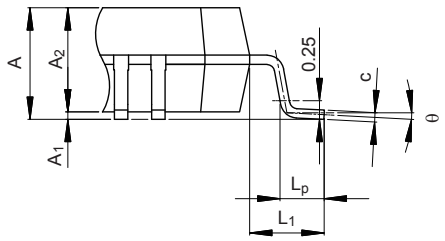
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.





Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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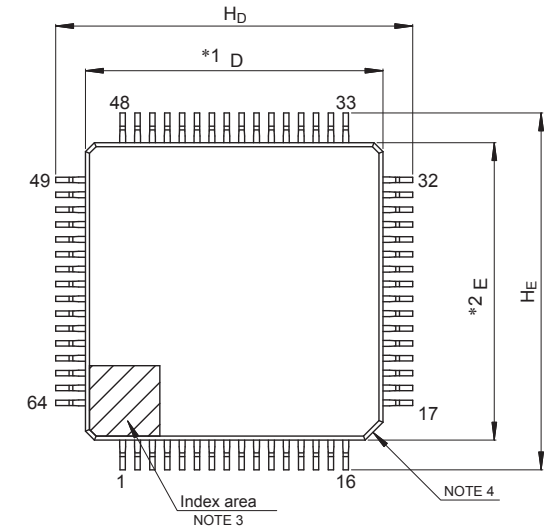
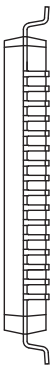
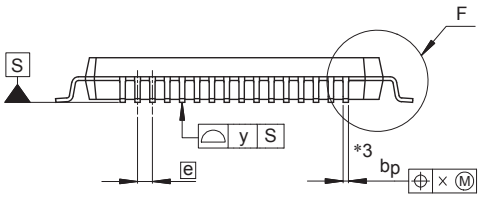
Figure 2.2 LQFP 80-pin

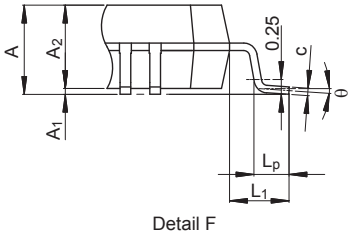
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm









Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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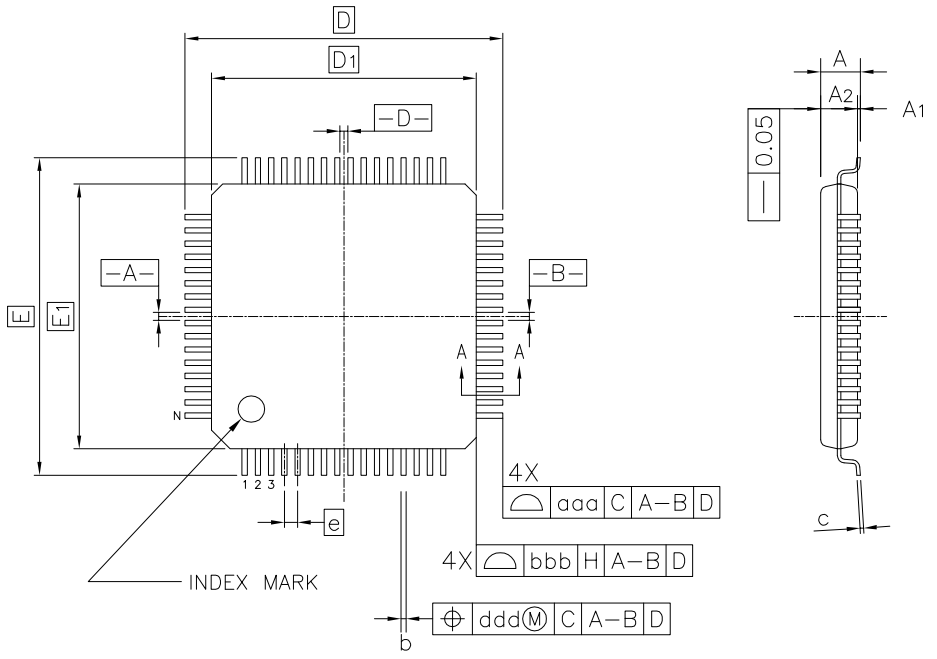
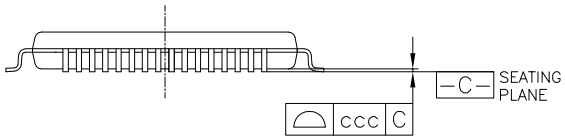
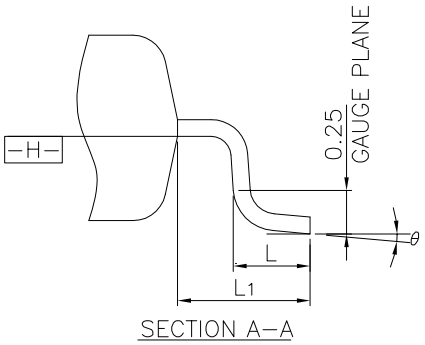
Figure 2.3 LQFP 64-pin (1)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFQFP064-10x10-0.50	PLQP0064KL-A	0.36





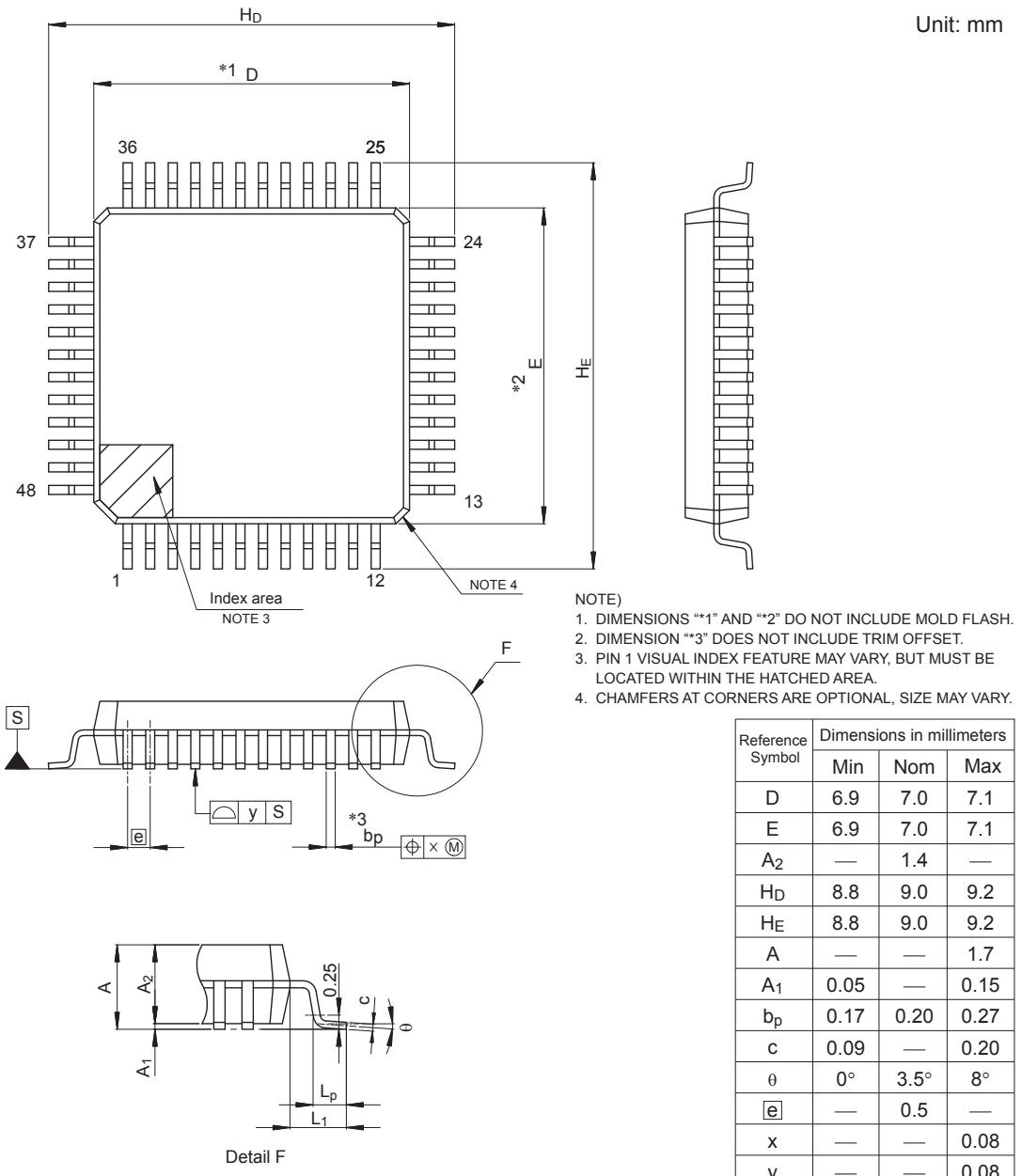


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A_1	0.05	–	0.15
A_2	1.35	1.40	1.45
D	–	12.00	–
D_1	–	10.00	–
E	–	12.00	–
E_1	–	10.00	–
N	–	64	–
e	–	0.50	–
b	0.17	0.22	0.27
c	0.09	–	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L_1	–	1.00	–
aaa	–	–	0.20
bbb	–	–	0.20
ccc	–	–	0.08
ddd	–	–	0.08

Figure 2.4 LQFP 64-pin (2)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm

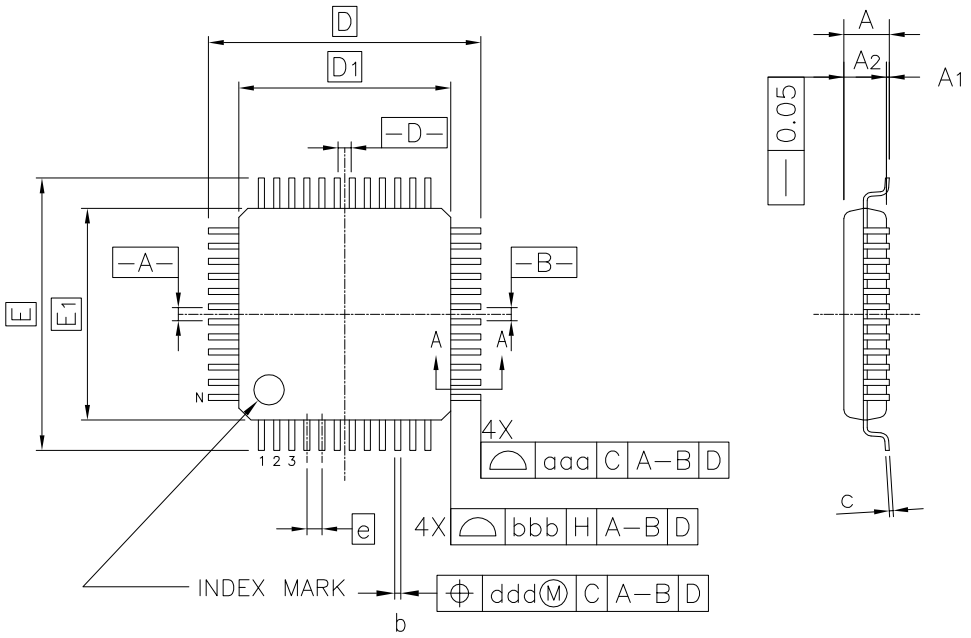


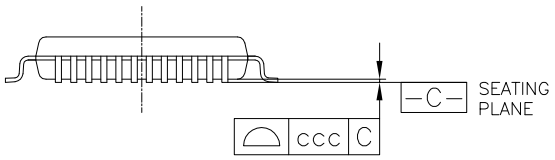
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

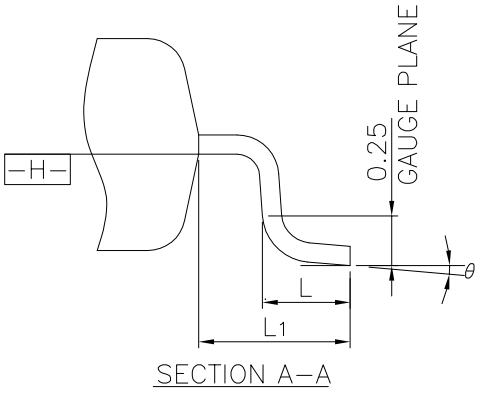
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 2.5 LQFP 48-pin (1)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFQFP48-7x7-0.50	PLQP0048KL-A	0.18



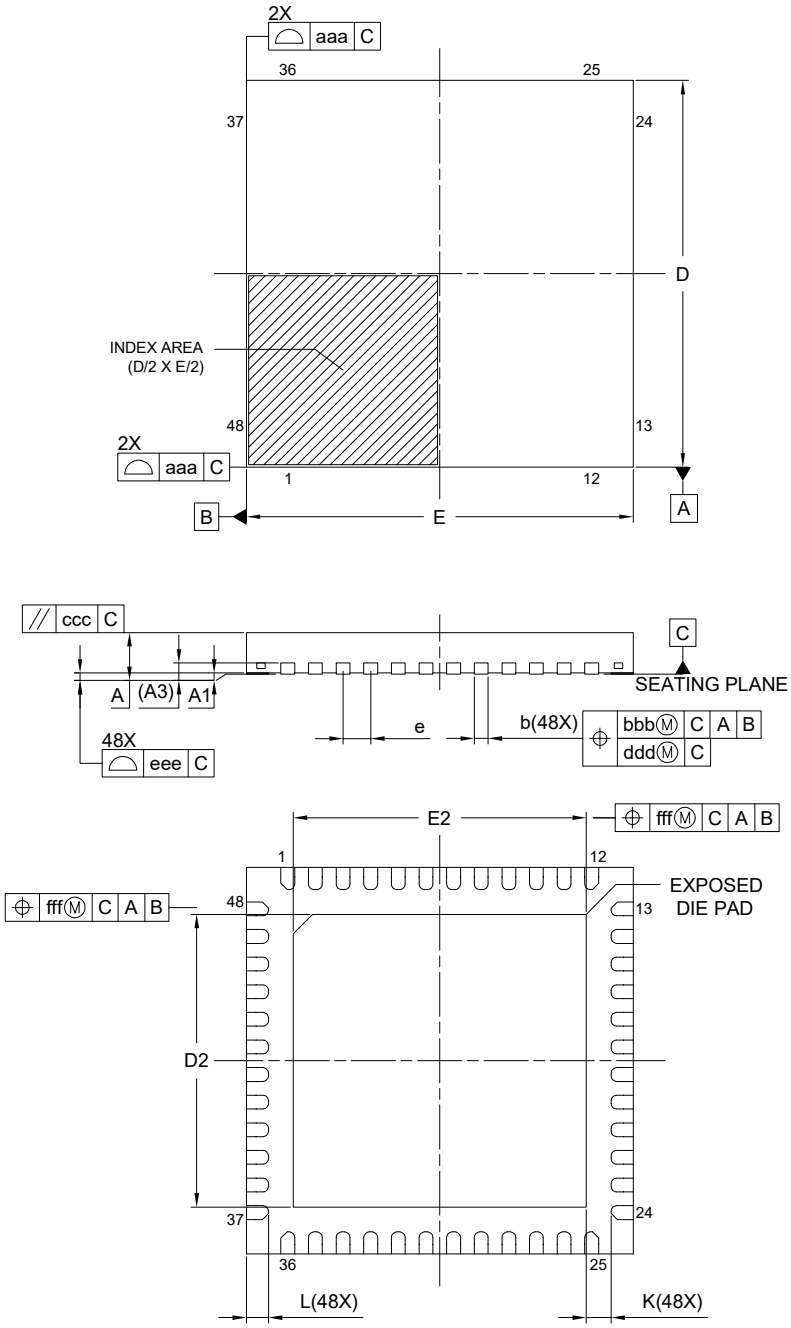




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A_1	0.05	–	0.15
A_2	1.35	1.40	1.45
D	–	9.00	–
D_1	–	7.00	–
E	–	9.00	–
E_1	–	7.00	–
N	–	48	–
e	–	0.50	–
b	0.17	0.22	0.27
c	0.09	–	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L_1	–	1.00	–
aaa	–	–	0.20
bbb	–	–	0.20
ccc	–	–	0.08
ddd	–	–	0.08

Figure 2.6 LQFP 48-pin (2)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.7 HWQFN 48-pin

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
MPU	Memory Protection Unit	0x4000_0000
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
DBG	Debug Function	0x4001_B000
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4004_0000
PORT1	Port 1 Control Registers	0x4004_0020
PORT2	Port 2 Control Registers	0x4004_0040
PORT3	Port 3 Control Registers	0x4004_0060
PORT4	Port 4 Control Registers	0x4004_0080
PORT5	Port 5 Control Registers	0x4004_00A0
PORT6	Port 6 Control Registers	0x4004_00C0
PORT7	Port 7 Control Registers	0x4004_00E0
PORT8	Port 8 Control Registers	0x4004_0100
PFS	Pmn Pin Function Control Register	0x4004_0800
ELC	Event Link Controller	0x4004_1000
POEG	Port Output Enable Module for GPT	0x4004_2000
RTC	Realtime Clock	0x4004_4000
WDT	Watchdog Timer	0x4004_4200
IWDT	Independent Watchdog Timer	0x4004_4400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4004_4600
MSTP	Module Stop Control B, C, D	0x4004_7000
CAN0	CAN0 Module	0x4005_0000
IIC0	Inter-Integrated Circuit 0	0x4005_3000
IIC0WU	Inter-Integrated Circuit 0 Wakeup Unit	0x4005_3014
IIC1	Inter-Integrated Circuit 1	0x4005_3100
DOC	Data Operation Circuit	0x4005_4100
ADC12	12-bit A/D Converter	0x4005_C000
DAC12	12-bit D/A Converter	0x4005_E000
SCI0	Serial Communication Interface 0	0x4007_0000
SCI1	Serial Communication Interface 1	0x4007_0020
SCI2	Serial Communication Interface 2	0x4007_0040
SCI3	Serial Communication Interface 3	0x4007_0060

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
SCI9	Serial Communication Interface 9	0x4007_0120
SPI0	Serial Peripheral Interface 0	0x4007_2000
SPI1	Serial Peripheral Interface 1	0x4007_2100
CRC	CRC Calculator	0x4007_4000
GPT320	General PWM Timer 0 (32-bit)	0x4007_8000
GPT321	General PWM Timer 1 (32-bit)	0x4007_8100
GPT322	General PWM Timer 2 (32-bit)	0x4007_8200
GPT323	General PWM Timer 3 (32-bit)	0x4007_8300
GPT164	General PWM Timer 4 (16-bit)	0x4007_8400
GPT165	General PWM Timer 5 (16-bit)	0x4007_8500
GPT166	General PWM Timer 6 (16-bit)	0x4007_8600
GPT167	General PWM Timer 7 (16-bit)	0x4007_8700
GPT168	General PWM Timer 8 (16-bit)	0x4007_8800
GPT169	General PWM Timer 9 (16-bit)	0x4007_8900
GPT_OPS	Output Phase Switching Controller	0x4007_8FF0
KINT	Key Interrupt Function	0x4008_0000
CTSU	Capacitive Sensing Unit	0x4008_2000
AGT0	Low Power Asynchronous General Purpose Timer 0	0x4008_4000
AGT1	Low Power Asynchronous General Purpose Timer 1	0x4008_4100
ACMPLP	Low-Power Analog Comparator	0x4008_5E00
FLCN	Flash I/O Registers	0x407E_C000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table 3.2:

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

Table 3.2 shows the register access cycles for non-GPT modules.

Table 3.2 Access cycles for non-GPT modules

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MPU, SRAM, BUS, DTC, ICU, DBG	0x4000_2000	0x4001_BFFF	3				ICLK	Memory Protection Unit, SRAM, Buses, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
SYSC	0x4001_E000	0x4001_E6FF	4				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
PORTn, PFS, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	0x4004_0000	0x4004_7FFF	3		2 to 3		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Realtime Clock, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control
CAN0,IICn (n = 0, 1),IIC0WU, DOC, ADC12, DAC12	0x4005_0000	0x4005_EFFF	3		2 to 3		PCLKB	Controller Area Network Module, I^2C Bus Interface, Data Operation Circuit, 12-bit A/D Converter, 12-Bit D/A Converter
SCIn (n = 0*2 to 3, 9)	0x4007_0000	0x4007_0EFF	5		2 to 3		PCLKB	Serial Communications Interface
SPIn (n = 0, 1)*3	0x4007_2000	0x4007_2FFF	5		2 to 3		PCLKB	Serial Peripheral Interface
CRC	0x4007_4000	0x4007_4FFF	3		2 to 3		PCLKB	CRC Calculator
GPT32n (n = 0 to 3), GPT16n (n = 4 to 9), GPT_OPS	0x4007_8000	0x4007_BFFF	See Table 3.3.				PCLKB	General PWM Timer
KINT, CTSU	0x4008_0000	0x4008_2FFF	3		2 to 3		PCLKB	Key interrupt Function, Capacitive Sensing Unit
AGTn	0x4008_4000	0x4008_4FFF	3		2 to 3		PCLKB	Low Power Asynchronous General Purpose Timer
ACMPLP	0x4008_5000	0x4008_6FFF	3		2 to 3		PCLKB	Low-Power Analog Comparator
FLCN	0x407E_C000	0x407E_FFFF	7		7		ICLK	Data Flash, Temperature Sensor, Capacitive Sensing Unit, Flash Control

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.
Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.
Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

Table 3.3 shows register access cycles for GPT modules.

Table 3.3 Access cycles for GPT modules

Frequency ratio between ICLK and PCLK	Number of access cycles		Cycle unit
	Read	Write	
ICLK > PCLKD = PCLKB	5 to 6	3 to 4	PCLKB
ICLK > PCLKD > PCLKB	3 to 4	2 to 3	PCLKB
PCLKD = ICLK = PCLKB	6	4	PCLKB
PCLKD = ICLK > PCLKB	2 to 3	1 to 2	PCLKB
PCLKD > ICLK = PCLKB	4	3	PCLKB
PCLKD > ICLK > PCLKB	2 to 3	1 to 2	PCLKB

3.3 Register Descriptions

This section provides information associated with registers described in this manual.

Table 3.4 shows a list of registers including address offsets, address sizes, access rights, and reset values.

Table 3.4 Register description (1 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
MPU	—	—	—	MMPUCTLA	Bus Master MPU Control Register	0x000	16	R/W	0x0000	0xFFFF
MPU	—	—	—	MMPUPTA	Group A Protection of Register	0x102	16	R/W	0x0000	0xFFFF
MPU	4	0x010	0-3	MMPUACA%s	Group A Region %s access control register	0x200	16	R/W	0x0000	0xFFFF
MPU	4	0x010	0-3	MMPUSA%s	Group A Region %s Start Address Register	0x204	32	R/W	0x00000000	0x00000003
MPU	4	0x010	0-3	MMPUEA%s	Group A Region %s End Address Register	0x208	32	R/W	0x00000003	0x00000003
MPU	—	—	—	SMPUCTL	Slave MPU Control Register	0xC00	16	R/W	0x0000	0xFFFF
MPU	—	—	—	SMPUMBIU	Access Control Register for Memory Bus 1	0xC10	16	R/W	0x0000	0xFFFF
MPU	—	—	—	SMPUFBIU	Access Control Register for Internal Peripheral Bus 9	0xC14	16	R/W	0x0000	0xFFFF
MPU	—	—	—	SMPUSRAM0	Access Control Register for Memory Bus 4	0xC18	16	R/W	0x0000	0xFFFF
MPU	—	—	—	SMPUP0BIU	Access Control Register for Internal Peripheral Bus 1	0xC20	16	R/W	0x0000	0xFFFF
MPU	—	—	—	SMPUP2BIU	Access Control Register for Internal Peripheral Bus 3	0xC24	16	R/W	0x0000	0xFFFF
MPU	—	—	—	SMPUP6BIU	Access Control Register for Internal Peripheral Bus 7	0xC28	16	R/W	0x0000	0xFFFF
MPU	—	—	—	MSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0xD00	16	R/W	0x0000	0xFFFF
MPU	—	—	—	MSPMPUCTL	Stack Pointer Monitor Access Control Register	0xD04	16	R/W	0x0000	0xFEFF
MPU	—	—	—	MSPMPUPT	Stack Pointer Monitor Protection Register	0xD06	16	R/W	0x0000	0xFFFF
MPU	—	—	—	MSPMPUSA	Main Stack Pointer (MSP) Monitor Start Address Register	0xD08	32	R/W	0x00000000	0x00000000
MPU	—	—	—	MSPMPUEA	Main Stack Pointer (MSP) Monitor End Address Register	0xD0C	32	R/W	0x00000000	0x00000000
MPU	—	—	—	PSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0xD10	16	R/W	0x0000	0xFFFF
MPU	—	—	—	PSPMPUCTL	Stack Pointer Monitor Access Control Register	0xD14	16	R/W	0x0000	0xFEFF
MPU	—	—	—	PSPMPUPT	Stack Pointer Monitor Protection Register	0xD16	16	R/W	0x0000	0xFFFF
MPU	—	—	—	PSPMPUSA	Process Stack Pointer (PSP) Monitor Start Address Register	0xD18	32	R/W	0x00000000	0x00000000
MPU	—	—	—	PSPMPUEA	Process Stack Pointer (PSP) Monitor End Address Register	0xD1C	32	R/W	0x00000000	0x00000000
SRAM	—	—	—	PARIOAD	SRAM Parity Error Operation After Detection Register	0x00	8	R/W	0x00	0xFF
SRAM	—	—	—	SRAMPRCR	SRAM Protection Register	0x04	8	R/W	0x00	0xFF
SRAM	—	—	—	ECCMODE	ECC Operating Mode Control Register	0xC0	8	R/W	0x00	0xFF
SRAM	—	—	—	ECC2STS	ECC 2-Bit Error Status Register	0xC1	8	R/W	0x00	0xFF
SRAM	—	—	—	ECC1STSEN	ECC 1-Bit Error Information Update Enable Register	0xC2	8	R/W	0x00	0xFF
SRAM	—	—	—	ECC1STS	ECC 1-Bit Error Status Register	0xC3	8	R/W	0x00	0xFF
SRAM	—	—	—	ECCETST	ECC Test Control Register	0xC4	8	R/W	0x00	0xFF
SRAM	—	—	—	ECCPRCR	ECC Protection Register	0xC4	8	R/W	0x00	0xFF
SRAM	—	—	—	ECCPRCR2	ECC Protection Register 2	0xD0	8	R/W	0x00	0xFF
SRAM	—	—	—	ECCOAD	SRAM ECC Error Operation After Detection Register	0xD8	8	R/W	0x00	0xFF

Table 3.4 Register description (2 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
BUS	—	—	—	BUSMCNTSYS	Master Bus Control Register SYS	0x1008	16	R/W	0x0000	0xFFFF
BUS	—	—	—	BUSMCNTDMA	Master Bus Control Register DMA	0x100C	16	R/W	0x0000	0xFFFF
BUS	—	—	—	BUS3ERRADD	Bus Error Address Register 3	0x1820	32	R	0x00000000	0x00000000
BUS	—	—	—	BUS3ERRSTAT	BUS Error Status Register 3	0x1824	8	R	0x00	0xFE
BUS	—	—	—	BUS4ERRADD	Bus Error Address Register 4	0x1830	32	R	0x00000000	0x00000000
BUS	—	—	—	BUS4ERRSTAT	BUS Error Status Register 4	0x1834	8	R	0x00	0xFE
DTC	—	—	—	DTCCR	DTC Control Register	0x00	8	R/W	0x08	0xFF
DTC	—	—	—	DTCVBR	DTC Vector Base Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
DTC	—	—	—	DTCST	DTC Module Start Register	0x0C	8	R/W	0x00	0xFF
DTC	—	—	—	DTCSTS	DTC Status Register	0x0E	16	R	0x0000	0xFFFF
ICU	8	0x1	0-7	IRQCR%s	IRQ Control Register	0x000	8	R/W	0x00	0xFF
ICU	—	—	—	NMICR	NMI Pin Interrupt Control Register	0x100	8	R/W	0x00	0xFF
ICU	—	—	—	NMIER	Non-Maskable Interrupt Enable Register	0x120	16	R/W	0x0000	0xFFFF
ICU	—	—	—	NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	R/W	0x0000	0xFFFF
ICU	—	—	—	NMISR	Non-Maskable Interrupt Status Register	0x140	16	R	0x0000	0xFFFF
ICU	—	—	—	WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	—	—	—	IELEN	ICU event Enable Register	0x1C0	8	R/W	0x00	0xFF
ICU	—	—	—	SELSR0	SYS Event Link Setting Register	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	R/W	0x00000000	0xFFFFFFFF
DBG	—	—	—	DBGSTR	Debug Status Register	0x00	32	R	0x00000000	0xFFFFFFFF
DBG	—	—	—	DBGSTOPCR	Debug Stop Control Register	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	—	—	—	SBYCR	Standby Control Register	0x00C	16	R/W	0x0000	0xFFFF
SYSC	—	—	—	MSTPCRA	Module Stop Control Register A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	—	—	—	SCKDIVCR	System Clock Division Control Register	0x020	32	R/W	0x04000404	0xFFFFFFFF
SYSC	—	—	—	SCKSCR	System Clock Source Control Register	0x026	8	R/W	0x01	0xFF
SYSC	—	—	—	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	—	—	—	MOSCCR	Main Clock Oscillator Control Register	0x032	8	R/W	0x01	0xFF
SYSC	—	—	—	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	—	—	—	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	—	—	—	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	—	—	—	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	—	—	—	OSTDCR	Oscillation Stop Detection Control Register	0x040	8	R/W	0x00	0xFF
SYSC	—	—	—	OSTDSR	Oscillation Stop Detection Status Register	0x041	8	R/W	0x00	0xFF
SYSC	—	—	—	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x40	0xFF
SYSC	—	—	—	MOCOUTCR	MOCO User Trimming Control Register	0x061	8	R/W	0x00	0xFF
SYSC	—	—	—	HOCOUTCR	HOCO User Trimming Control Register	0x062	8	R/W	0x00	0xFF
SYSC	—	—	—	SNZCR	Snooze Control Register	0x092	8	R/W	0x00	0xFF
SYSC	—	—	—	SNZEDCR0	Snooze End Control Register 0	0x094	8	R/W	0x00	0xFF
SYSC	—	—	—	SNZREQCR0	Snooze Request Control Register 0	0x098	32	R/W	0x00000000	0xFFFFFFFF
SYSC	—	—	—	PSMCR	Power Save Memory Control Register	0x09F	8	R/W	0x00	0xFF
SYSC	—	—	—	OPCCR	Operating Power Control Register	0x0A0	8	R/W	0x01	0xFF
SYSC	—	—	—	MOSCWTCR	Main Clock Oscillator Wait Control Register	0x0A2	8	R/W	0x05	0xFF
SYSC	—	—	—	SOPCCR	Sub Operating Power Control Register	0x0AA	8	R/W	0x00	0xFF

Table 3.4 Register description (3 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SYSC	—	—	—	RSTSR1	Reset Status Register 1	0x0C0	16	R/W	0x0000	0xE0F8
SYSC	—	—	—	LVD1CR1	Voltage Monitor 1 Circuit Control Register	0x0E0	8	R/W	0x01	0xFF
SYSC	—	—	—	LVD1SR	Voltage Monitor 1 Circuit Status Register	0x0E1	8	R/W	0x02	0xFF
SYSC	—	—	—	LVD2CR1	Voltage Monitor 2 Circuit Control Register 1	0x0E2	8	R/W	0x01	0xFF
SYSC	—	—	—	LVD2SR	Voltage Monitor 2 Circuit Status Register	0x0E3	8	R/W	0x02	0xFF
SYSC	—	—	—	PRCR	Protect Register	0x3FE	16	R/W	0x0000	0xFFFF
SYSC	—	—	—	SYOCDCR	System Control OCD Control Register	0x040E	8	R/W	0x00	0xFF
SYSC	—	—	—	RSTSR0	Reset Status Register 0	0x410	8	R/W	0x00	0xF0
SYSC	—	—	—	RSTSR2	Reset Status Register 2	0x411	8	R/W	0x00	0xFE
SYSC	—	—	—	MOMCR	Main Clock Oscillator Mode Oscillation Control Register	0x413	8	R/W	0x00	0xFF
SYSC	—	—	—	LVCMPCR	Voltage Monitor Circuit Control Register	0x417	8	R/W	0x00	0xFF
SYSC	—	—	—	LVDLVLR	Voltage Detection Level Select Register	0x418	8	R/W	0x07	0xFF
SYSC	—	—	—	LVD1CR0	Voltage Monitor 1 Circuit Control Register 0	0x41A	8	R/W	0x80	0xF7
SYSC	—	—	—	LVD2CR0	Voltage Monitor 2 Circuit Control Register 0	0x41B	8	R/W	0x80	0xF7
SYSC	—	—	—	DCDCCTL	DCDC/LDO Control Register	0x440	8	R/W	0xC0	0xFF
SYSC	—	—	—	VCCSEL	Voltage Level Selection Control Register	0x441	8	R/W	0x00	0xFF
SYSC	—	—	—	SOSCCR	Sub-Clock Oscillator Control Register	0x480	8	R/W	0x01	0xFF
SYSC	—	—	—	SOMCR	Sub-Clock Oscillator Mode Control Register	0x481	8	R/W	0x00	0xFF
SYSC	—	—	—	SOMRG	Sub-Clock Oscillator Margin Check Register	0x482	8	R/W	0x00	0xFF
SYSC	—	—	—	LOCOCR	Low-Speed On-Chip Oscillator Control Register	0x490	8	R/W	0x00	0xFF
SYSC	—	—	—	LOCOUTCR	LOCO User Trimming Control Register	0x492	8	R/W	0x00	0xFF
PORT0,3-8	—	—	—	PCNTR1	Port Control Register 1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT0,3-8	—	—	—	PODR	Port Control Register 1	0x000	16	R/W	0x0000	0xFFFF
PORT0,3-8	—	—	—	PDR	Port Control Register 1	0x002	16	R/W	0x0000	0xFFFF
PORT0,3-8	—	—	—	PCNTR2	Port Control Register 2	0x004	32	R	0x00000000	0xFFFF0000
PORT0,3-8	—	—	—	PIDR	Port Control Register 2	0x006	16	R	0x0000	0x0000
PORT0,3-8	—	—	—	PCNTR3	Port Control Register 3	0x008	32	W	0x00000000	0xFFFFFFFF
PORT0,3-8	—	—	—	PORR	Port Control Register 3	0x008	16	W	0x0000	0xFFFF
PORT0,3-8	—	—	—	POSR	Port Control Register 3	0x00A	16	W	0x0000	0xFFFF
PORT1-2	—	—	—	PCNTR1	Port Control Register 1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT1-2	—	—	—	PODR	Port Control Register 1	0x000	16	R/W	0x0000	0xFFFF
PORT1-2	—	—	—	PDR	Port Control Register 1	0x002	16	R/W	0x0000	0xFFFF
PORT1-2	—	—	—	PCNTR2	Port Control Register 2	0x004	32	R	0x00000000	0xFFFF0000
PORT1-2	—	—	—	EIDR	Port Control Register 2	0x004	16	R	0x0000	0xFFFF
PORT1-2	—	—	—	PIDR	Port Control Register 2	0x006	16	R	0x0000	0x0000
PORT1-2	—	—	—	PCNTR3	Port Control Register 3	0x008	32	W	0x00000000	0xFFFFFFFF
PORT1-2	—	—	—	PORR	Port Control Register 3	0x008	16	W	0x0000	0xFFFF
PORT1-2	—	—	—	POSR	Port Control Register 3	0x00A	16	W	0x0000	0xFFFF
PORT1-2	—	—	—	PCNTR4	Port Control Register 4	0x00C	32	R/W	0x00000000	0xFFFFFFFF
PORT1-2	—	—	—	EORR	Port Control Register 4	0x00C	16	R/W	0x0000	0xFFFF
PORT1-2	—	—	—	EOSR	Port Control Register 4	0x00E	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (4 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
PFS	9	0x4	0-8	P00%sPFS	Port 00%s Pin Function Select Register	0x000	32	R/W	0x00000000	0xFFFFFFFD
PFS	9	0x4	0-8	P00%sPFS_HA	Port 00%s Pin Function Select Register	0x002	16	R/W	0x0000	0xFFFD
PFS	9	0x4	0-8	P00%sPFS_BY	Port 00%s Pin Function Select Register	0x003	8	R/W	0x00	0xFD
PFS	6	0x4	10-15	P0%sPFS	Port 0%s Pin Function Select Register	0x028	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	10-15	P0%sPFS_HA	Port 0%s Pin Function Select Register	0x02A	16	R/W	0x0000	0xFFFD
PFS	6	0x4	10-15	P0%sPFS_BY	Port 0%s Pin Function Select Register	0x02B	8	R/W	0x00	0xFD
PFS	8	0x4	0-7	P10%sPFS	Port 10%s Pin Function Select Register	0x040	32	R/W	0x00000000	0xFFFFFFFD
PFS	8	0x4	0-7	P10%sPFS_HA	Port 10%s Pin Function Select Register	0x042	16	R/W	0x0000	0xFFFD
PFS	8	0x4	0-7	P10%sPFS_BY	Port 10%s Pin Function Select Register	0x043	8	R/W	0x00	0xFD
PFS	—	—	—	P108PFS	Port 108 Pin Function Select Register	0x060	32	R/W	0x00010010	0xFFFFFFFD
PFS	—	—	—	P108PFS_HA	Port 108 Pin Function Select Register	0x062	16	R/W	0x0010	0xFFFD
PFS	—	—	—	P108PFS_BY	Port 108 Pin Function Select Register	0x063	8	R/W	0x10	0xFD
PFS	—	—	—	P109PFS	Port 109 Pin Function Select Register	0x064	32	R/W	0x00000000	0xFFFFFFFD
PFS	—	—	—	P109PFS_HA	Port 109 Pin Function Select Register	0x066	16	R/W	0x0000	0xFFFD
PFS	—	—	—	P109PFS_BY	Port 109 Pin Function Select Register	0x067	8	R/W	0x00	0xFD
PFS	6	0x4	10-15	P1%sPFS	Port 1%s Pin Function Select Register	0x068	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	10-15	P1%sPFS_HA	Port 1%s Pin Function Select Register	0x06A	16	R/W	0x0000	0xFFFD
PFS	6	0x4	10-15	P1%sPFS_BY	Port 1%s Pin Function Select Register	0x06B	8	R/W	0x00	0xFD
PFS	—	—	—	P200PFS	Port 200 Pin Function Select Register	0x080	32	R/W	0x00000000	0xFFFFFFFD
PFS	—	—	—	P200PFS_HA	Port 200 Pin Function Select Register	0x082	16	R/W	0x0000	0xFFFD
PFS	—	—	—	P200PFS_BY	Port 200 Pin Function Select Register	0x083	8	R/W	0x00	0xFD
PFS	—	—	—	P201PFS	Port 201 Pin Function Select Register	0x084	32	R/W	0x00000010	0xFFFFFFFD
PFS	—	—	—	P201PFS_HA	Port 201 Pin Function Select Register	0x086	16	R/W	0x0010	0xFFFD
PFS	—	—	—	P201PFS_BY	Port 201 Pin Function Select Register	0x087	8	R/W	0x10	0xFD
PFS	7	0x4	2-8	P20%sPFS	Port 20%s Pin Function Select Register	0x088	32	R/W	0x00000000	0xFFFFFFFD
PFS	7	0x4	2-8	P20%sPFS_HA	Port 20%s Pin Function Select Register	0x08A	16	R/W	0x0000	0xFFFD
PFS	7	0x4	2-8	P20%sPFS_BY	Port 20%s Pin Function Select Register	0x08B	8	R/W	0x00	0xFD
PFS	4	0x4	12-15	P2%sPFS	Port 2%s Pin Function Select Register	0x0B0	32	R/W	0x00000000	0xFFFFFFFD
PFS	4	0x4	12-15	P2%sPFS_HA	Port 2%s Pin Function Select Register	0x0B2	16	R/W	0x0000	0xFFFD
PFS	4	0x4	12-15	P2%sPFS_BY	Port 2%s Pin Function Select Register	0x0B3	8	R/W	0x00	0xFD
PFS	—	—	—	P300PFS	Port 300 Pin Function Select Register	0x0C0	32	R/W	0x00010000	0xFFFFFFFD
PFS	—	—	—	P300PFS_HA	Port 300 Pin Function Select Register	0x0C2	16	R/W	0x0000	0xFFFD
PFS	—	—	—	P300PFS_BY	Port 300 Pin Function Select Register	0x0C3	8	R/W	0x00	0xFD
PFS	7	0x4	1-7	P30%sPFS	Port 30%s Pin Function Select Register	0x0C4	32	R/W	0x00000000	0xFFFFFFFD
PFS	7	0x4	1-7	P30%sPFS_HA	Port 30%s Pin Function Select Register	0x0C6	16	R/W	0x0000	0xFFFD
PFS	7	0x4	1-7	P30%sPFS_BY	Port 30%s Pin Function Select Register	0x0C7	8	R/W	0x00	0xFD
PFS	10	0x4	0-9	P40%sPFS	Port 40%s Pin Function Select Register	0x100	32	R/W	0x00000000	0xFFFFFFFD
PFS	10	0x4	0-9	P40%sPFS_HA	Port 40%s Pin Function Select Register	0x102	16	R/W	0x0000	0xFFFD
PFS	10	0x4	0-9	P40%sPFS_BY	Port 40%s Pin Function Select Register	0x103	8	R/W	0x00	0xFD
PFS	6	0x4	10-15	P4%sPFS	Port 4%s Pin Function Select Register	0x128	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	10-15	P4%sPFS_HA	Port 4%s Pin Function Select Register	0x12A	16	R/W	0x0000	0xFFFD
PFS	6	0x4	10-15	P4%sPFS_BY	Port 4%s Pin Function Select Register	0x12B	8	R/W	0x00	0xFD
PFS	6	0x4	0-5	P50%sPFS	Port 50%s Pin Function Select Register	0x140	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	0-5	P50%sPFS_HA	Port 50%s Pin Function Select Register	0x142	16	R/W	0x0000	0xFFFD
PFS	6	0x4	0-5	P50%sPFS_BY	Port 50%s Pin Function Select Register	0x143	8	R/W	0x00	0xFD

Table 3.4 Register description (5 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
PFS	4	0x4	0-3	P60%sPFS	Port 60%s Pin Function Select Register	0x180	32	R/W	0x00000000	0xFFFFFFFD
PFS	4	0x4	0-3	P60%sPFS_HA	Port 60%s Pin Function Select Register	0x182	16	R/W	0x0000	0xFFFD
PFS	4	0x4	0-3	P60%sPFS_BY	Port 60%s Pin Function Select Register	0x183	8	R/W	0x00	0xFD
PFS	2	0x4	8-9	P60%sPFS	Port 60%s Pin Function Select Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFD
PFS	2	0x4	8-9	P60%sPFS_HA	Port 60%s Pin Function Select Register	0x1A2	16	R/W	0x0000	0xFFFD
PFS	2	0x4	8-9	P60%sPFS_BY	Port 60%s Pin Function Select Register	0x1A3	8	R/W	0x00	0xFD
PFS	—	—	—	P610PFS	Port 610 Pin Function Select Register	0x1A8	32	R/W	0x00000000	0xFFFFFFFD
PFS	—	—	—	P610PFS_HA	Port 610 Pin Function Select Register	0x1AA	16	R/W	0x0000	0xFFFD
PFS	—	—	—	P610PFS_BY	Port 610 Pin Function Select Register	0x1AB	8	R/W	0x00	0xFD
PFS	—	—	—	P708PFS	Port 708 Pin Function Select Register	0x1E0	32	R/W	0x00000000	0xFFFFFFFD
PFS	—	—	—	P708PFS_HA	Port 708 Pin Function Select Register	0x1E2	16	R/W	0x0000	0xFFFD
PFS	—	—	—	P708PFS_BY	Port 708 Pin Function Select Register	0x1E3	8	R/W	0x00	0xFD
PFS	—	—	—	P714PFS	Port 714 Pin Function Select Register	0x1F8	32	R/W	0x00000000	0xFFFFFFFD
PFS	—	—	—	P714PFS_HA	Port 714 Pin Function Select Register	0x1FA	16	R/W	0x0000	0xFFFD
PFS	—	—	—	P714PFS_BY	Port 714 Pin Function Select Register	0x1FB	8	R/W	0x00	0xFD
PFS	2	0x4	8-9	P80%sPFS	Port 80%s Pin Function Select Register	0x220	32	R/W	0x00000000	0xFFFFFFFD
PFS	2	0x4	8-9	P80%sPFS_HA	Port 80%s Pin Function Select Register	0x222	16	R/W	0x0000	0xFFFD
PFS	2	0x4	8-9	P80%sPFS_BY	Port 80%s Pin Function Select Register	0x223	8	R/W	0x00	0xFD
PFS	—	—	—	PWPR	Write-Protect Register	0x503	8	R/W	0x80	0xFF
PFS	—	—	—	PRWCNTR	Port Read Wait Control Register	0x50F	8	R/W	0x01	0xFF
ELC	—	—	—	ELCR	Event Link Controller Register	0x00	8	R/W	0x00	0xFF
ELC	2	0x02	0-1	ELSEGR%s	Event Link Software Event Generation Register %s	0x02	8	R/W	0x80	0xFF
ELC	4	0x04	0-3	ELSR%s	Event Link Setting Register %s	0x10	16	R/W	0x0000	0xFFFF
ELC	2	0x04	8-9	ELSR%s	Event Link Setting Register %s	0x30	16	R/W	0x0000	0xFFFF
ELC	—	—	—	ELSR12	Event Link Setting Register 12	0x40	16	R/W	0x0000	0xFFFF
ELC	2	0x04	14-15	ELSR%s	Event Link Setting Register %s	0x48	16	R/W	0x0000	0xFFFF
ELC	—	—	—	ELSR18	Event Link Setting Register 18	0x58	16	R/W	0x0000	0xFFFF
POEG	—	—	—	POEGGA	POEG Group A Setting Register	0x000	32	R/W	0x00000000	0xFFFFFFFF
POEG	—	—	—	POEGGB	POEG Group B Setting Register	0x100	32	R/W	0x00000000	0xFFFFFFFF
RTC	—	—	—	R64CNT	64-Hz Counter	0x00	8	R	0x00	0x00
RTC	4	0x02	0-3	BCNT%s	Binary Counter %s	0x02	8	R/W	0x00	0x00
RTC	—	—	—	RSECCNT	Second Counter (in Calendar Count Mode)	0x02	8	R/W	0x00	0x00
RTC	—	—	—	RMINCNT	Minute Counter (in Calendar Count Mode)	0x04	8	R/W	0x00	0x00
RTC	—	—	—	RHRCNT	Hour Counter (in Calendar Count Mode)	0x06	8	R/W	0x00	0x00
RTC	—	—	—	RWKCNT	Day-of-Week Counter (in Calendar Count Mode)	0x08	8	R/W	0x00	0x00
RTC	—	—	—	RDAYCNT	Day Counter	0x0A	8	R/W	0x00	0xC0
RTC	—	—	—	RMONCNT	Month Counter	0x0C	8	R/W	0x00	0xE0
RTC	—	—	—	RYRCNT	Year Counter	0x0E	16	R/W	0x0000	0xFF00
RTC	4	0x02	0-3	BCNT%sAR	Binary Counter %s Alarm Register	0x10	8	R/W	0x00	0x00
RTC	—	—	—	RSECAR	Second Alarm Register (in Calendar Count Mode)	0x10	8	R/W	0x00	0x00
RTC	—	—	—	RMINAR	Minute Alarm Register (in Calendar Count Mode)	0x12	8	R/W	0x00	0x00
RTC	—	—	—	RHRAR	Hour Alarm Register (in Calendar Count Mode)	0x14	8	R/W	0x00	0x00

Table 3.4 Register description (6 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
RTC	—	—	—	RWKAR	Day-of-Week Alarm Register (in Calendar Count Mode)	0x16	8	R/W	0x00	0x00
RTC	2	0x02	0-1	BCNT%sAER	Binary Counter %s Alarm Enable Register	0x18	8	R/W	0x00	0x00
RTC	—	—	—	RDAYAR	Date Alarm Register (in Calendar Count Mode)	0x18	8	R/W	0x00	0x00
RTC	—	—	—	RMONAR	Month Alarm Register (in Calendar Count Mode)	0x1A	8	R/W	0x00	0x00
RTC	—	—	—	BCNT2AER	Binary Counter 2 Alarm Enable Register	0x1C	16	R/W	0x0000	0xFF00
RTC	—	—	—	RYRAR	Year Alarm Register (in Calendar Count Mode)	0x1C	16	R/W	0x0000	0xFF00
RTC	—	—	—	BCNT3AER	Binary Counter 3 Alarm Enable Register	0x1E	8	R/W	0x00	0x00
RTC	—	—	—	RYRAREN	Year Alarm Enable Register (in Calendar Count Mode)	0x1E	8	R/W	0x00	0x00
RTC	—	—	—	RCR1	RTC Control Register 1	0x22	8	R/W	0x00	0x0A
RTC	—	—	—	RCR2	RTC Control Register 2 (in Calendar Count Mode)	0x24	8	R/W	0x00	0x0E
RTC	—	—	—	RCR2	RTC Control Register 2 (in Binary Count Mode)	0x24	8	R/W	0x00	0x0E
RTC	—	—	—	RCR4	RTC Control Register 4	0x28	8	R/W	0x00	0x7E
RTC	—	—	—	RFRH	Frequency Register H	0x2A	16	R/W	0x0000	0xFFFE
RTC	—	—	—	RFRL	Frequency Register L	0x2C	16	R/W	0x0000	0x0000
RTC	—	—	—	RADJ	Time Error Adjustment Register	0x2E	8	R/W	0x00	0x00
WDT	—	—	—	WDTRR	WDT Refresh Register	0x00	8	R/W	0xFF	0xFF
WDT	—	—	—	WDTCR	WDT Control Register	0x02	16	R/W	0x0000	0xFFFF
WDT	—	—	—	WDTSR	WDT Status Register	0x04	16	R/W	0x0000	0xFFFF
WDT	—	—	—	WDTRCR	WDT Reset Control Register	0x06	8	R/W	0x80	0xFF
WDT	—	—	—	WDTCSTPR	WDT Count Stop Control Register	0x08	8	R/W	0x80	0xFF
IWDT	—	—	—	IWDTRR	IWDT Refresh Register	0x00	8	R/W	0xFF	0xFF
IWDT	—	—	—	IWDTSR	IWDT Status Register	0x04	16	R/W	0x0000	0xFFFF
CAC	—	—	—	CACR0	CAC Control Register 0	0x00	8	R/W	0x00	0xFF
CAC	—	—	—	CACR1	CAC Control Register 1	0x01	8	R/W	0x00	0xFF
CAC	—	—	—	CACR2	CAC Control Register 2	0x02	8	R/W	0x00	0xFF
CAC	—	—	—	CAICR	CAC Interrupt Control Register	0x03	8	R/W	0x00	0xFF
CAC	—	—	—	CASTR	CAC Status Register	0x04	8	R	0x00	0xFF
CAC	—	—	—	CAULVR	CAC Upper-Limit Value Setting Register	0x06	16	R/W	0x0000	0xFFFF
CAC	—	—	—	CALLVR	CAC Lower-Limit Value Setting Register	0x08	16	R/W	0x0000	0xFFFF
CAC	—	—	—	CACNTBR	CAC Counter Buffer Register	0x0A	16	R	0x0000	0xFFFF
MSTP	—	—	—	MSTPCRB	Module Stop Control Register B	0x000	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	—	—	—	MSTPCRC	Module Stop Control Register C	0x004	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	—	—	—	MSTPCRD	Module Stop Control Register D	0x008	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	—	—	—	LSMRWDIS	Low Speed Module R/W Disable Control Register	0x00C	16	R/W	0x0000	0xFFFF
CAN0	32	0x10	0-31	MB%s_ID	Mailbox ID Register %s	0x200	32	R/W	0x00000000	0x00000001
CAN0	32	0x10	0-31	MB%s_DL	Mailbox Data Length Register %s	0x204	16	R/W	0x0000	0x0000
CAN0	32	0x10	0-31	MB%s_D0	Mailbox Data Register %s	0x206	8	R/W	0x00	0x00
CAN0	32	0x10	0-31	MB%s_D1	Mailbox Data Register %s	0x207	8	R/W	0x00	0x00
CAN0	32	0x10	0-31	MB%s_D2	Mailbox Data Register %s	0x208	8	R/W	0x00	0x00
CAN0	32	0x10	0-31	MB%s_D3	Mailbox Data Register %s	0x209	8	R/W	0x00	0x00
CAN0	32	0x10	0-31	MB%s_D4	Mailbox Data Register %s	0x20A	8	R/W	0x00	0x00

Table 3.4 Register description (7 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
CAN0	32	0x10	0-31	MB%s_D5	Mailbox Data Register %s	0x20B	8	R/W	0x00	0x00
CAN0	32	0x10	0-31	MB%s_D6	Mailbox Data Register %s	0x20C	8	R/W	0x00	0x00
CAN0	32	0x10	0-31	MB%s_D7	Mailbox Data Register %s	0x20D	8	R/W	0x00	0x00
CAN0	32	0x10	0-31	MB%s_TS	Mailbox Time Stamp Register %s	0x20E	16	R/W	0x0000	0x0000
CAN0	8	0x04	—	MKR[%s]	Mask Register %s	0x400	32	R/W	0x00000000	0x00000000
CAN0	2	0x04	0-1	FIDCR%s	FIFO Received ID Compare Register %s	0x420	32	R/W	0x00000000	0x00000000
CAN0	—	—	—	MKIVLR	Mask Invalid Register	0x428	32	R/W	0x00000000	0x00000000
CAN0	—	—	—	MIER	Mailbox Interrupt Enable Register	0x42C	32	R/W	0x00000000	0x00000000
CAN0	—	—	—	MIER_FIFO	Mailbox Interrupt Enable Register for FIFO Mailbox Mode	0x42C	32	R/W	0x00000000	0x00000000
CAN0	32	0x01	—	MCTL_RX[%s]	Message Control Register for Receive	0x820	8	R/W	0x00	0xFF
CAN0	32	0x01	—	MCTL_TX[%s]	Message Control Register for Transmit	0x820	8	R/W	0x00	0xFF
CAN0	—	—	—	CTLR	Control Register	0x840	16	R/W	0x0500	0xFFFF
CAN0	—	—	—	STR	Status Register	0x842	16	R	0x0500	0xFFFF
CAN0	—	—	—	BCR	Bit Configuration Register	0x844	32	R/W	0x00000000	0xFFFFFFFF
CAN0	—	—	—	RFCR	Receive FIFO Control Register	0x848	8	R/W	0x80	0xFF
CAN0	—	—	—	RFPCR	Receive FIFO Pointer Control Register	0x849	8	W	0x00	0x00
CAN0	—	—	—	TFCR	Transmit FIFO Control Register	0x84A	8	R/W	0x80	0xFF
CAN0	—	—	—	TFPCR	Transmit FIFO Pointer Control Register	0x84B	8	W	0x00	0x00
CAN0	—	—	—	EIER	Error Interrupt Enable Register	0x84C	8	R/W	0x00	0xFF
CAN0	—	—	—	EIFR	Error Interrupt Factor Judge Register	0x84D	8	R/W	0x00	0xFF
CAN0	—	—	—	RECR	Receive Error Count Register	0x84E	8	R	0x00	0xFF
CAN0	—	—	—	TECR	Transmit Error Count Register	0x84F	8	R	0x00	0xFF
CAN0	—	—	—	ECSR	Error Code Store Register	0x850	8	R/W	0x00	0xFF
CAN0	—	—	—	CSSR	Channel Search Support Register	0x851	8	R/W	0x00	0x00
CAN0	—	—	—	MSSR	Mailbox Search Status Register	0x852	8	R	0x80	0xFF
CAN0	—	—	—	MSMR	Mailbox Search Mode Register	0x853	8	R/W	0x00	0xFF
CAN0	—	—	—	TSR	Time Stamp Register	0x854	16	R	0x0000	0xFFFF
CAN0	—	—	—	AFSR	Acceptance Filter Support Register	0x856	16	R/W	0x0000	0x0000
CAN0	—	—	—	TCR	Test Control Register	0x858	8	R/W	0x00	0xFF
IIC0-1	—	—	—	ICCR1	I2C Bus Control Register 1	0x00	8	R/W	0x1F	0xFF
IIC0-1	—	—	—	ICCR2	I2C Bus Control Register 2	0x01	8	R/W	0x00	0xFF
IIC0-1	—	—	—	ICMR1	I2C Bus Mode Register 1	0x02	8	R/W	0x08	0xFF
IIC0-1	—	—	—	ICMR2	I2C Bus Mode Register 2	0x03	8	R/W	0x06	0xFF
IIC0-1	—	—	—	ICMR3	I2C Bus Mode Register 3	0x04	8	R/W	0x00	0xFF
IIC0-1	—	—	—	ICFER	I2C Bus Function Enable Register	0x05	8	R/W	0x72	0xFF
IIC0-1	—	—	—	ICSER	I2C Bus Status Enable Register	0x06	8	R/W	0x09	0xFF
IIC0-1	—	—	—	ICIER	I2C Bus Interrupt Enable Register	0x07	8	R/W	0x00	0xFF
IIC0-1	—	—	—	ICSR1	I2C Bus Status Register 1	0x08	8	R/W	0x00	0xFF
IIC0-1	—	—	—	ICSR2	I2C Bus Status Register 2	0x09	8	R/W	0x00	0xFF
IIC0-1	3	0x02	0-2	SARL%s	Slave Address Register Ly	0x0A	8	R/W	0x00	0xFF
IIC0-1	3	0x02	0-2	SARU%s	Slave Address Register Uy	0x0B	8	R/W	0x00	0xFF
IIC0-1	—	—	—	ICBRL	I2C Bus Bit Rate Low-Level Register	0x10	8	R/W	0xFF	0xFF
IIC0-1	—	—	—	ICBRH	I2C Bus Bit Rate High-Level Register	0x11	8	R/W	0xFF	0xFF
IIC0-1	—	—	—	ICDRT	I2C Bus Transmit Data Register	0x12	8	R/W	0xFF	0xFF
IIC0-1	—	—	—	ICDRR	I2C Bus Receive Data Register	0x13	8	R	0x00	0xFF

Table 3.4 Register description (8 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
IIC0WU	—	—	—	ICWUR	I2C Bus Wakeup Unit Register	0x02	8	R/W	0x10	0xFF
IIC0WU	—	—	—	ICWUR2	I2C Bus Wakeup Unit Register 2	0x03	8	R/W	0xFD	0xFF
DOC	—	—	—	DOCR	DOC Control Register	0x00	8	R/W	0x00	0xFF
DOC	—	—	—	DODIR	DOC Data Input Register	0x02	16	R/W	0x0000	0xFFFF
DOC	—	—	—	DODSR	DOC Data Setting Register	0x04	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADCSR	A/D Control Register	0x000	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADANSA0	A/D Channel Select Register A0	0x004	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADANSA1	A/D Channel Select Register A1	0x006	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADADS0	A/D-Converted Value Addition/Average Channel Select Register 0	0x008	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADADS1	A/D-Converted Value Addition/Average Channel Select Register 1	0x00A	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADADC	A/D-Converted Value Addition/Average Count Select Register	0x00C	8	R/W	0x00	0xFF
ADC12	—	—	—	ADCER	A/D Control Extended Register	0x00E	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADSTRGR	A/D Conversion Start Trigger Select Register	0x010	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADEXICR	A/D Conversion Extended Input Control Registers	0x012	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADANSB0	A/D Channel Select Register B0	0x014	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADANSB1	A/D Channel Select Register B1	0x016	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADDBLDR	A/D Data Duplexing Register	0x018	16	R	0x0000	0xFFFF
ADC12	—	—	—	ADTSDR	A/D Temperature Sensor Data Register	0x01A	16	R	0x0000	0xFFFF
ADC12	—	—	—	ADOCDR	A/D Internal Reference Voltage Data Register	0x01C	16	R	0x0000	0xFFFF
ADC12	—	—	—	ADRD	A/D Self-Diagnosis Data Register	0x01E	16	R	0x0000	0xFFFF
ADC12	15	0x2	0-14	ADDR%s	A/D Data Registers %s	0x020	16	R	0x0000	0xFFFF
ADC12	—	—	—	ADCTDR	A/D CTSU TSCAP Voltage Data Register	0x040	16	R	0x0000	0xFFFF
ADC12	4	0x2	17-20	ADDR%s	A/D Data Registers %s	0x042	16	R	0x0000	0xFFFF
ADC12	—	—	—	ADDISCR	A/D Disconnection Detection Control Register	0x07A	8	R/W	0x00	0xFF
ADC12	—	—	—	ADACSR	A/D Conversion Operation Mode Select Register	0x07E	8	R/W	0x00	0xFF
ADC12	—	—	—	ADGSPCR	A/D Group Scan Priority Control Register	0x080	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADDBLDRA	A/D Data Duplexing Register A	0x084	16	R	0x0000	0xFFFF
ADC12	—	—	—	ADDBLDRB	A/D Data Duplexing Register B	0x086	16	R	0x0000	0xFFFF
ADC12	—	—	—	ADHVREFCNT	A/D High-Potential/Low-Potential Reference Voltage Control Register	0x08A	8	R/W	0x00	0xFF
ADC12	—	—	—	ADWINMON	A/D Compare Function Window A/B Status Monitor Register	0x08C	8	R	0x00	0xFF
ADC12	—	—	—	ADCMPCR	A/D Compare Function Control Register	0x090	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADCMPANSER	A/D Compare Function Window A Extended Input Select Register	0x092	8	R/W	0x00	0xFF
ADC12	—	—	—	ADCMPLER	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	0x093	8	R/W	0x00	0xFF
ADC12	—	—	—	ADCMPANSR0	A/D Compare Function Window A Channel Select Register 0	0x094	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADCMPANSR1	A/D Compare Function Window A Channel Select Register 1	0x096	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADCMPLR0	A/D Compare Function Window A Comparison Condition Setting Register 0	0x098	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (9 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ADC12	—	—	—	ADCMPLR1	A/D Compare Function Window A Comparison Condition Setting Register 1	0x09A	16	R/W	0x0000	0xFFFF
ADC12	2	0x2	0-1	ADCMPDR%s	A/D Compare Function Window A Lower-Side/Upper-Side Level Setting Register	0x09C	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADCMPSR0	A/D Compare Function Window A Channel Status Register 0	0x0A0	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADCMPSR1	A/D Compare Function Window A Channel Status Register1	0x0A2	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADCMPSER	A/D Compare Function Window A Extended Input Channel Status Register	0x0A4	8	R/W	0x00	0xFF
ADC12	—	—	—	ADCMPBNSR	A/D Compare Function Window B Channel Select Register	0x0A6	8	R/W	0x00	0xFF
ADC12	—	—	—	ADWINLLB	A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register	0x0A8	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADWINULB	A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register	0x0AA	16	R/W	0x0000	0xFFFF
ADC12	—	—	—	ADCMPBSR	A/D Compare Function Window B Status Register	0x0AC	8	R/W	0x00	0xFF
ADC12	—	—	—	ADSSTRL	A/D Sampling State Register	0x0DD	8	R/W	0x0D	0xFF
ADC12	—	—	—	ADSSTRT	A/D Sampling State Register	0x0DE	8	R/W	0x0D	0xFF
ADC12	—	—	—	ADSSTRO	A/D Sampling State Register	0x0DF	8	R/W	0x0D	0xFF
ADC12	15	0x1	0-14	ADSSTR%s	A/D Sampling State Register	0x0E0	8	R/W	0x0D	0xFF
DAC12	—	—	—	DADR0	D/A Data Register 0	0x00	16	R/W	0x0000	0xFFFF
DAC12	—	—	—	DACR	D/A Control Register	0x04	8	R/W	0x1F	0xFF
DAC12	—	—	—	DADPR	DADR0 Format Select Register	0x05	8	R/W	0x00	0xFF
DAC12	—	—	—	DAADSCR	D/A A/D Synchronous Start Control Register	0x06	8	R/W	0x00	0xFF
DAC12	—	—	—	DAVREFCR	D/A VREF Control Register	0x07	8	R/W	0x00	0xFF
SCI0	—	—	—	SMR	Serial Mode Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x00	8	R/W	0x00	0xFF
SCI0	—	—	—	SMR_SMCI	Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x00	8	R/W	0x00	0xFF
SCI0	—	—	—	BRR	Bit Rate Register	0x01	8	R/W	0xFF	0xFF
SCI0	—	—	—	SCR	Serial Control Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x02	8	R/W	0x00	0xFF
SCI0	—	—	—	SCR_SMCI	Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x02	8	R/W	0x00	0xFF
SCI0	—	—	—	TDR	Transmit Data Register	0x03	8	R/W	0xFF	0xFF
SCI0	—	—	—	SSR	Serial Status Register for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0)	0x04	8	R/W	0x84	0xFF
SCI0	—	—	—	SSR_FIFO	Serial Status Register for Non-Smart Card Interface and FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 1)	0x04	8	R/W	0x80	0xFD
SCI0	—	—	—	SSR_SMCI	Serial Status Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x04	8	R/W	0x84	0xFF
SCI0	—	—	—	RDR	Receive Data Register	0x05	8	R/W	0x00	0xFF
SCI0	—	—	—	SCMR	Smart Card Mode Register	0x06	8	R/W	0xF2	0xFF
SCI0	—	—	—	SEMR	Serial Extended Mode Register	0x07	8	R/W	0x00	0xFF
SCI0	—	—	—	SNFR	Noise Filter Setting Register	0x08	8	R/W	0x00	0xFF
SCI0	—	—	—	SIMR1	IIC Mode Register 1	0x09	8	R/W	0x00	0xFF
SCI0	—	—	—	SIMR2	IIC Mode Register 2	0x0A	8	R/W	0x00	0xFF
SCI0	—	—	—	SIMR3	IIC Mode Register 3	0x0B	8	R/W	0x00	0xFF
SCI0	—	—	—	SISR	IIC Status Register	0x0C	8	R	0x00	0xCB

Table 3.4 Register description (10 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SCI0	—	—	—	SPMR	SPI Mode Register	0x0D	8	R/W	0x00	0xFF
SCI0	—	—	—	TDRHL	Transmit Data Register	0x0E	16	R/W	0xFFFF	0xFFFF
SCI0	—	—	—	FRDRHL	Receive FIFO Data Register	0x10	16	R	0x0000	0xFFFF
SCI0	—	—	—	FTDRHL	Transmit FIFO Data Register	0x0E	16	W	0xFFFF	0xFFFF
SCI0	—	—	—	RDRHL	Receive Data Register	0x10	16	R	0x0000	0xFFFF
SCI0	—	—	—	FRDRH	Receive FIFO Data Register	0x10	8	R	0x00	0xFF
SCI0	—	—	—	FTDRH	Transmit FIFO Data Register	0x0E	8	W	0xFF	0xFF
SCI0	—	—	—	FRDRL	Receive FIFO Data Register	0x11	8	R	0x00	0xFF
SCI0	—	—	—	FTDRL	Transmit FIFO Data Register	0x0F	8	W	0xFF	0xFF
SCI0	—	—	—	MDDR	Modulation Duty Register	0x12	8	R/W	0xFF	0xFF
SCI0	—	—	—	DCCR	Data Compare Match Control Register	0x13	8	R/W	0x40	0xFF
SCI0	—	—	—	FCR	FIFO Control Register	0x14	16	R/W	0xF800	0xFFFF
SCI0	—	—	—	FDR	FIFO Data Count Register	0x16	16	R	0x0000	0xFFFF
SCI0	—	—	—	LSR	Line Status Register	0x18	16	R	0x0000	0xFFFF
SCI0	—	—	—	CDR	Compare Match Data Register	0x1A	16	R/W	0x0000	0xFFFF
SCI0	—	—	—	SPTR	Serial Port Register	0x1C	8	R/W	0x03	0xFF
SCI1-3,9	—	—	—	SMR	Serial Mode Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x00	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	SMR_SMCI	Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x00	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	BRR	Bit Rate Register	0x01	8	R/W	0xFF	0xFF
SCI1-3,9	—	—	—	SCR	Serial Control Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x02	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	SCR_SMCI	Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x02	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	TDR	Transmit Data Register	0x03	8	R/W	0xFF	0xFF
SCI1-3,9	—	—	—	SSR	Serial Status Register for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0)	0x04	8	R/W	0x84	0xFF
SCI1-3,9	—	—	—	SSR_SMCI	Serial Status Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x04	8	R/W	0x84	0xFF
SCI1-3,9	—	—	—	RDR	Receive Data Register	0x05	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	SCMR	Smart Card Mode Register	0x06	8	R/W	0xF2	0xFF
SCI1-3,9	—	—	—	SEMR	Serial Extended Mode Register	0x07	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	SNFR	Noise Filter Setting Register	0x08	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	SIMR1	IIC Mode Register 1	0x09	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	SIMR2	IIC Mode Register 2	0x0A	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	SIMR3	IIC Mode Register 3	0x0B	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	SISR	IIC Status Register	0x0C	8	R	0x00	0xCB
SCI1-3,9	—	—	—	SPMR	SPI Mode Register	0x0D	8	R/W	0x00	0xFF
SCI1-3,9	—	—	—	TDRHL	Transmit Data Register	0x0E	16	R/W	0xFFFF	0xFFFF
SCI1-3,9	—	—	—	RDRHL	Receive Data Register	0x10	16	R	0x0000	0xFFFF
SCI1-3,9	—	—	—	MDDR	Modulation Duty Register	0x12	8	R/W	0xFF	0xFF
SCI1-3,9	—	—	—	DCCR	Data Compare Match Control Register	0x13	8	R/W	0x40	0xFF
SCI1-3,9	—	—	—	CDR	Compare Match Data Register	0x1A	16	R/W	0x0000	0xFFFF
SCI1-3,9	—	—	—	SPTR	Serial Port Register	0x1C	8	R/W	0x03	0xFF
SPI0-1	—	—	—	SPCR	SPI Control Register	0x00	8	R/W	0x00	0xFF
SPI0-1	—	—	—	SSLP	SPI Slave Select Polarity Register	0x01	8	R/W	0x00	0xFF

Table 3.4 Register description (11 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SPI0-1	—	—	—	SPPCR	SPI Pin Control Register	0x02	8	R/W	0x00	0xFF
SPI0-1	—	—	—	SPSR	SPI Status Register	0x03	8	R/W	0x20	0xFF
SPI0-1	—	—	—	SPDR	SPI Data Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
SPI0-1	—	—	—	SPDR_HA	SPI Data Register	0x04	16	R/W	0x0000	0xFFFF
SPI0-1	—	—	—	SPBR	SPI Bit Rate Register	0x0A	8	R/W	0xFF	0xFF
SPI0-1	—	—	—	SPDCR	SPI Data Control Register	0x0B	8	R/W	0x00	0xFF
SPI0-1	—	—	—	SPCKD	SPI Clock Delay Register	0x0C	8	R/W	0x00	0xFF
SPI0-1	—	—	—	SSLND	SPI Slave Select Negation Delay Register	0x0D	8	R/W	0x00	0xFF
SPI0-1	—	—	—	SPND	SPI Next-Access Delay Register	0x0E	8	R/W	0x00	0xFF
SPI0-1	—	—	—	SPCR2	SPI Control Register 2	0x0F	8	R/W	0x00	0xFF
SPI0-1	—	—	—	SPCMD0	SPI Command Register 0	0x10	16	R/W	0x070D	0xFFFF
CRC	—	—	—	CRCCR0	CRC Control Register 0	0x00	8	R/W	0x00	0xFF
CRC	—	—	—	CRCCR1	CRC Control Register 1	0x01	8	R/W	0x00	0xFF
CRC	—	—	—	CRCDIR	CRC Data Input Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
CRC	—	—	—	CRCDIR_BY	CRC Data Input Register	0x04	8	R/W	0x00	0xFF
CRC	—	—	—	CRCDOR	CRC Data Output Register	0x08	32	R/W	0x00000000	0xFFFFFFFF
CRC	—	—	—	CRCDOR_HA	CRC Data Output Register	0x08	16	R/W	0x0000	0xFFFF
CRC	—	—	—	CRCDOR_BY	CRC Data Output Register	0x08	8	R/W	0x00	0xFF
CRC	—	—	—	CRCSAR	Snoop Address Register	0x0C	16	R/W	0x0000	0xFFFF
GPT320-3	—	—	—	GTWP	General PWM Timer Write-Protection Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTSTR	General PWM Timer Software Start Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTSTP	General PWM Timer Software Stop Register	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320-3	—	—	—	GTCLR	General PWM Timer Software Clear Register	0x0C	32	W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTSSR	General PWM Timer Start Source Select Register	0x10	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTPSR	General PWM Timer Stop Source Select Register	0x14	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTCSR	General PWM Timer Clear Source Select Register	0x18	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTCR	General PWM Timer Control Register	0x2C	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	R/W	0x00000001	0xFFFFFFFF
GPT320-3	—	—	—	GTIOR	General PWM Timer I/O Control Register	0x34	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTST	General PWM Timer Status Register	0x3C	32	R/W	0x00008000	0xFFFFFFFF
GPT320-3	—	—	—	GTBER	General PWM Timer Buffer Enable Register	0x40	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTCNT	General PWM Timer Counter	0x48	32	R/W	0x00000000	0xFFFFFFFF

Table 3.4 Register description (12 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
GPT320-3	—	—	—	GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320-3	—	—	—	GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320-3	—	—	—	GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320-3	—	—	—	GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320-3	—	—	—	GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320-3	—	—	—	GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320-3	—	—	—	GTPR	General PWM Timer Cycle Setting Register	0x64	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320-3	—	—	—	GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320-3	—	—	—	GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	R/W	0x00000000	0xFFFFFFFF
GPT320-3	—	—	—	GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	—	—	—	GTWP	General PWM Timer Write-Protection Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTSTR	General PWM Timer Software Start Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTSTP	General PWM Timer Software Stop Register	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	—	—	—	GTCLR	General PWM Timer Software Clear Register	0x0C	32	W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTSSR	General PWM Timer Start Source Select Register	0x10	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTPSR	General PWM Timer Stop Source Select Register	0x14	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTCSR	General PWM Timer Clear Source Select Register	0x18	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTCR	General PWM Timer Control Register	0x2C	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	R/W	0x00000001	0xFFFFFFFF
GPT164-9	—	—	—	GTIOR	General PWM Timer I/O Control Register	0x34	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTST	General PWM Timer Status Register	0x3C	32	R/W	0x00008000	0xFFFFFFFF
GPT164-9	—	—	—	GTBER	General PWM Timer Buffer Enable Register	0x40	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTCNT	General PWM Timer Counter	0x48	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	—	—	—	GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	R/W	0xFFFFFFFF	0xFFFFFFFF

Table 3.4 Register description (13 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
GPT164-9	—	—	—	GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	—	—	—	GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	—	—	—	GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	—	—	—	GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	—	—	—	GTPR	General PWM Timer Cycle Setting Register	0x64	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	—	—	—	GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	—	—	—	GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	—	—	—	GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT_OPS	—	—	—	OPSCR	Output Phase Switching Control Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
KINT	—	—	—	KRCTL	Key Return Control Register	0x00	8	R/W	0x00	0xFF
KINT	—	—	—	KRF	Key Return Flag Register	0x04	8	R/W	0x00	0xFF
KINT	—	—	—	KRM	Key Return Mode Register	0x08	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCRA	CTSU Control Register A	0x00	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUCRAL	CTSU Control Register A	0x00	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUCR0	CTSU Control Register A	0x00	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCR1	CTSU Control Register A	0x01	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCR2	CTSU Control Register A	0x02	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCR3	CTSU Control Register A	0x03	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCRB	CTSU Control Register B	0x04	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUCRBL	CTSU Control Register B	0x04	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUSDPRS	CTSU Control Register B	0x04	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUSST	CTSU Control Register B	0x05	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCRBH	CTSU Control Register B	0x06	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUDCLKC	CTSU Control Register B	0x07	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUMCH	CTSU Measurement Channel Register	0x08	32	R/W	0x00003F3F	0xFFFFFFFF
CTSU	—	—	—	CTSUMCHL	CTSU Measurement Channel Register	0x08	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUMCH0	CTSU Measurement Channel Register	0x08	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUMCH1	CTSU Measurement Channel Register	0x09	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUMCHH	CTSU Measurement Channel Register	0x0A	16	R/W	0x3F3F	0xFFFF
CTSU	—	—	—	CTSUMFAF	CTSU Measurement Channel Register	0x0A	8	R/W	0x3F	0xFF
CTSU	—	—	—	CTSUCHACA	CTSU Channel Enable Control Register A	0x0C	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUCHACAL	CTSU Channel Enable Control Register A	0x0C	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUCHAC0	CTSU Channel Enable Control Register A	0x0C	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCHAC1	CTSU Channel Enable Control Register A	0x0D	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCHACAH	CTSU Channel Enable Control Register A	0x0E	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUCHAC2	CTSU Channel Enable Control Register A	0x0E	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCHAC3	CTSU Channel Enable Control Register A	0x0F	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCHACB	CTSU Channel Enable Control Register B	0x10	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUCHACBL	CTSU Channel Enable Control Register B	0x10	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUCHAC4	CTSU Channel Enable Control Register B	0x10	8	R/W	0x00	0xFF

Table 3.4 Register description (14 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
CTSU	—	—	—	CTSUCHTRCA	CTSU Channel Transmit/Receive Control Register A	0x14	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUCHTRCAL	CTSU Channel Transmit/Receive Control Register A	0x14	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUCHTRC0	CTSU Channel Transmit/Receive Control Register A	0x14	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCHTRC1	CTSU Channel Transmit/Receive Control Register A	0x15	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCHTRCAH	CTSU Channel Transmit/Receive Control Register A	0x16	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUCHTRC2	CTSU Channel Transmit/Receive Control Register A	0x16	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCHTRC3	CTSU Channel Transmit/Receive Control Register A	0x17	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUCHTRCB	CTSU Channel Transmit/Receive Control Register B	0x18	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUCHTRCBL	CTSU Channel Transmit/Receive Control Register B	0x18	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUCHTRC4	CTSU Channel Transmit/Receive Control Register B	0x18	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUSR	CTSU Status Register	0x1C	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUSRL	CTSU Status Register	0x1C	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUSR0	CTSU Status Register	0x1C	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUST	CTSU Status Register	0x1D	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUSRH	CTSU Status Register	0x1E	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUSR2	CTSU Status Register	0x1E	8	R/W	0x00	0xFF
CTSU	—	—	—	CTSUSO	CTSU Sensor Offset Register	0x20	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUSO0	CTSU Sensor Offset Register	0x20	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUSO1	CTSU Sensor Offset Register	0x22	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUSCNT	CTSU Sensor Counter Register	0x24	32	R	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUSC	CTSU Sensor Counter Register	0x24	16	R	0x0000	0xFFFF
CTSU	—	—	—	CTSUCALIB	CTSU Calibration Register	0x28	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUDBGR0	CTSU Calibration Register	0x28	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUDBGR1	CTSU Calibration Register	0x2A	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUSUCLKA	CTSU Sensor Unit Clock Control Register A	0x2C	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUSUCLK0	CTSU Sensor Unit Clock Control Register A	0x2C	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUSUCLK1	CTSU Sensor Unit Clock Control Register A	0x2E	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUSUCLKB	CTSU Sensor Unit Clock Control Register B	0x30	32	R/W	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUSUCLK2	CTSU Sensor Unit Clock Control Register B	0x30	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUSUCLK3	CTSU Sensor Unit Clock Control Register B	0x32	16	R/W	0x0000	0xFFFF
CTSU	—	—	—	CTSUCFCCNT	CTSU CFC Counter Register	0x34	32	R	0x00000000	0xFFFFFFFF
CTSU	—	—	—	CTSUCFCCNTL	CTSU CFC Counter Register	0x34	16	R	0x0000	0xFFFF
AGT0-1	—	—	—	AGT	AGT Counter Register	0x00	16	R/W	0xFFFF	0xFFFF
AGT0-1	—	—	—	AGTCMB	AGT Compare Match B Register	0x04	16	R/W	0xFFFF	0xFFFF
AGT0-1	—	—	—	AGTCMA	AGT Compare Match A Register	0x02	16	R/W	0xFFFF	0xFFFF
AGT0-1	—	—	—	AGTCR	AGT Control Register	0x08	8	R/W	0x00	0xFF

Table 3.4 Register description (15 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
AGT0-1	—	—	—	AGTMR1	AGT Mode Register 1	0x09	8	R/W	0x00	0xFF
AGT0-1	—	—	—	AGTMR2	AGT Mode Register 2	0x0A	8	R/W	0x00	0xFF
AGT0-1	—	—	—	AGTIOC	AGT I/O Control Register	0x0C	8	R/W	0x00	0xFF
AGT0-1	—	—	—	AGTISR	AGT Event Pin Select Register	0x0D	8	R/W	0x00	0xFF
AGT0-1	—	—	—	AGTCMSR	AGT Compare Match Function Select Register	0x0E	8	R/W	0x00	0xFF
AGT0-1	—	—	—	AGTIOSEL	AGT Pin Select Register	0x00F	8	R/W	0x00	0xFF
ACMPLP	—	—	—	COMPMDR	ACMPLP Mode Setting Register	0x00	8	R/W	0x00	0xFF
ACMPLP	—	—	—	COMPFIR	ACMPLP Filter Control Register	0x01	8	R/W	0x00	0xFF
ACMPLP	—	—	—	COMPOCR	ACMPLP Output Control Register	0x02	8	R/W	0x00	0xFF
FLCN	—	—	—	DFLCTL	Data Flash Enable Register	0x0090	8	R/W	0x00	0xFF
FLCN	—	—	—	TSCDR	Temperature Sensor Calibration Data Register	0x0228	16	R	0x00	0x00
FLCN	—	—	—	CTSUTRIMA	CTSU Trimming Register A	0x03A4	32	R/W	0x00000000	0x00000000
FLCN	—	—	—	FLDWAITR	Memory Wait Cycle Control Register for Data Flash	0x3FC4	8	R/W	0x00	0xFF
FLCN	—	—	—	PFBER	Prefetch Buffer Enable Register	0x3FC8	8	R/W	0x00	0xFF

Note: Peripheral name = Name of peripheral
Dim = Number of elements in an array of registers
Dim inc. = Address increment between two simultaneous registers of a register array in the address map
Dim index = Sub string that replaces the %s placeholder within the register name
Register name = Name of register
Description = Register description
Address offset = Address of the register relative to the base address defined by the peripheral of the register
Size = Bit width of the register
Reset value = Default reset value of a register
Reset mask = Identifies which register bits have a defined reset value

Revision History

Revision 1.00 — Aug 06, 2020

First edition, issued

Revision 1.10 — Feb 26, 2021

Features:
- Changed from LFQFP to LQFP.

Overview:
- Changed from LFQFP to LQFP in Figure 1.2 Part numbering scheme.
- Added PWQN0048KC-A to Table 1.11 Product list.
- Changed from MISO0_A to MISO9_A for P202 in Table 1.14 Pin list.

Electrical Characteristics:
- Added Note 5 to Table 2.19 Clock timing.

Appendix 2. Package Dimensions:
- Added Figure 2.5 HWQFN 48-pin.

Revision 1.20 — May 20, 2022

Overview:
- Added Table 1.11 I/O ports to 1.1 Function Outline.
- Fixed Figure 1.2 Part numbering scheme in 1.3 Part Numbering.
- Fixed Table 1.13 Function comparison in 1.4 Function Comparison.
- Added I/O ports to Table 1.13 Function comparison.
- Fixed Figure 1.7 Pin assignment for QFN 48-pin (top view) in 1.6 Pin Assignments.

Electrical Characteristics:
- Fixed Table 2.4 I/O V_{IH}, V_{IL} in 2.2.2 I/O V_{IH}, V_{IL}.
- Fixed Table 2.11 Operating and standby current (2) in 2.2.5 Operating and Standby Current.
- Fixed Note 2 in Table 2.47 Power-on reset circuit and voltage detection circuit characteristics (1) in 2.8 POR and LVD Characteristics.

Revision 1.30 — November 30, 2022

1. Overview:
- Updated 1.3 Part Numbering.
- Updated Table 1.13 Function comparison.

2. Electrical Characteristics:
- Updated Table 2.32 SPI timing.
- Updated 2.11.1 Code Flash Memory Characteristics and 2.11.2 Data Flash Memory Characteristics.

Appendix 2. Package Dimensions:
- Updated the figure title of Figure 2.3 LQFP 64-pin (1).
- Added Figure 2.4 LQFP 64-pin (2).
- Updated the figure title of Figure 2.5 LQFP 48-pin (1).
- Added Figure 2.6 LQFP 48-pin (2).

Appendix 3. I/O Registers:
- Updated Table 3.2 Access cycles for non-GPT modules.
- Updated Table 3.4 Register description.

Revision 1.40 — October 31, 2023

1. Overview:
- Updated Figure 1.2 Part numbering scheme.
- Updated the Note in Figure 1.7.

2. Electrical Characteristics:
- Updated Table 2.4 I/O V_{IH}, V_{IL}.
- Added section 2.2.7 Thermal Characteristics.

Revision 1.50 — August 30, 2024

41. Electrical Characteristics:
- Updated Table 41.23 Timing of recovery from low power modes (2) and (3).
- Updated Note 3 in Table 41.52 Code flash characteristics (1).
- Updated Note 3 in Table 41.56 Data flash characteristics (1).

Revision 1.50 — August 30, 2024

Appendix 3. I/O Registers:
- Updated LPOPT reset value in Table 3.4 Register description.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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