THE DATASHEET OF

PI6CG330440ZUDIEX

A Product Line of
Diodes Incorporated

PI6CG330440

19-Output PCIe 5.0/6.0 Clock Generator With On-chip Termination

Description

The DIODES PI6CG330440 is a 19-output very low jitter clock generator. It takes an reference input to generate 25MHz and 100MHz outputs. The on-chip termination can save 80 external resistors and make layout easier. Individual OE pin for each output provides easier power management.

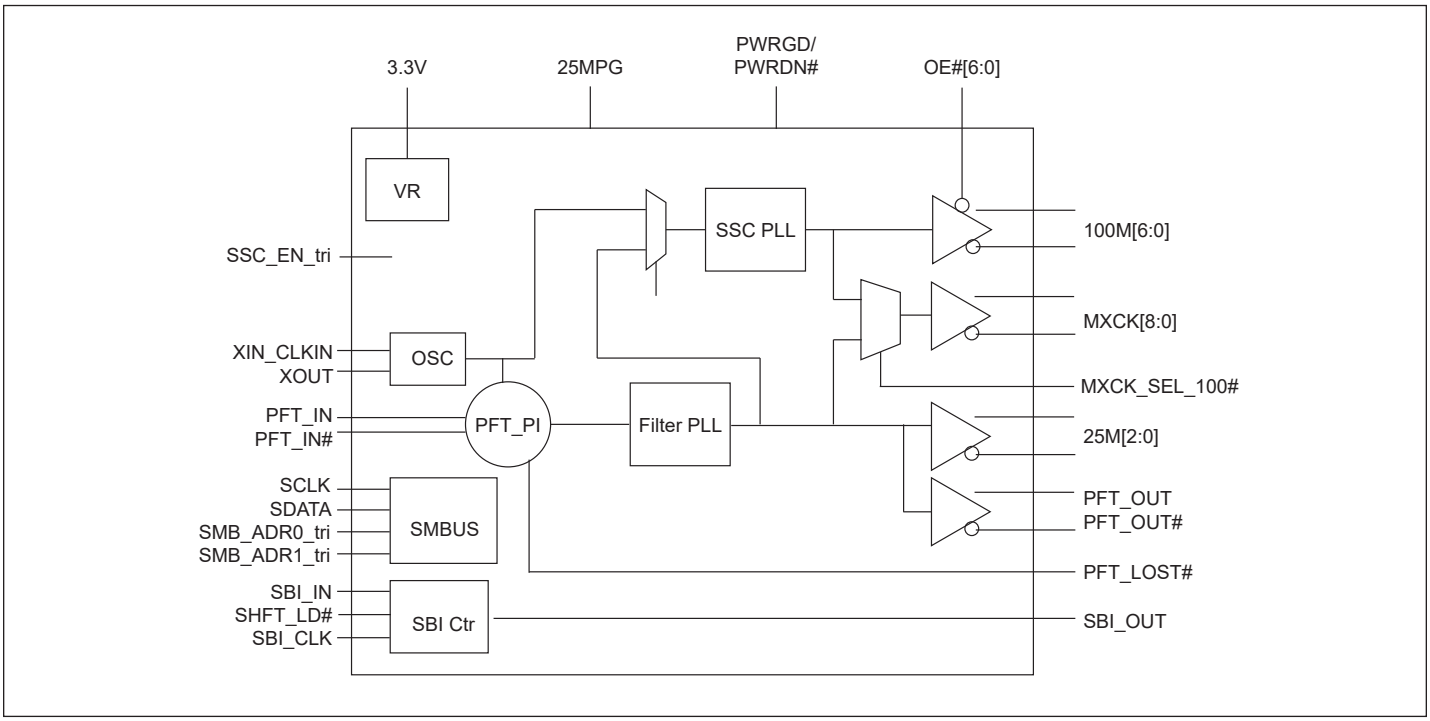
It uses Diodes' proprietary design to achieve very low jitter that meets PCIe® 1.0/2.0/3.0/4.0/5.0/6.0 clock requirements.

Features

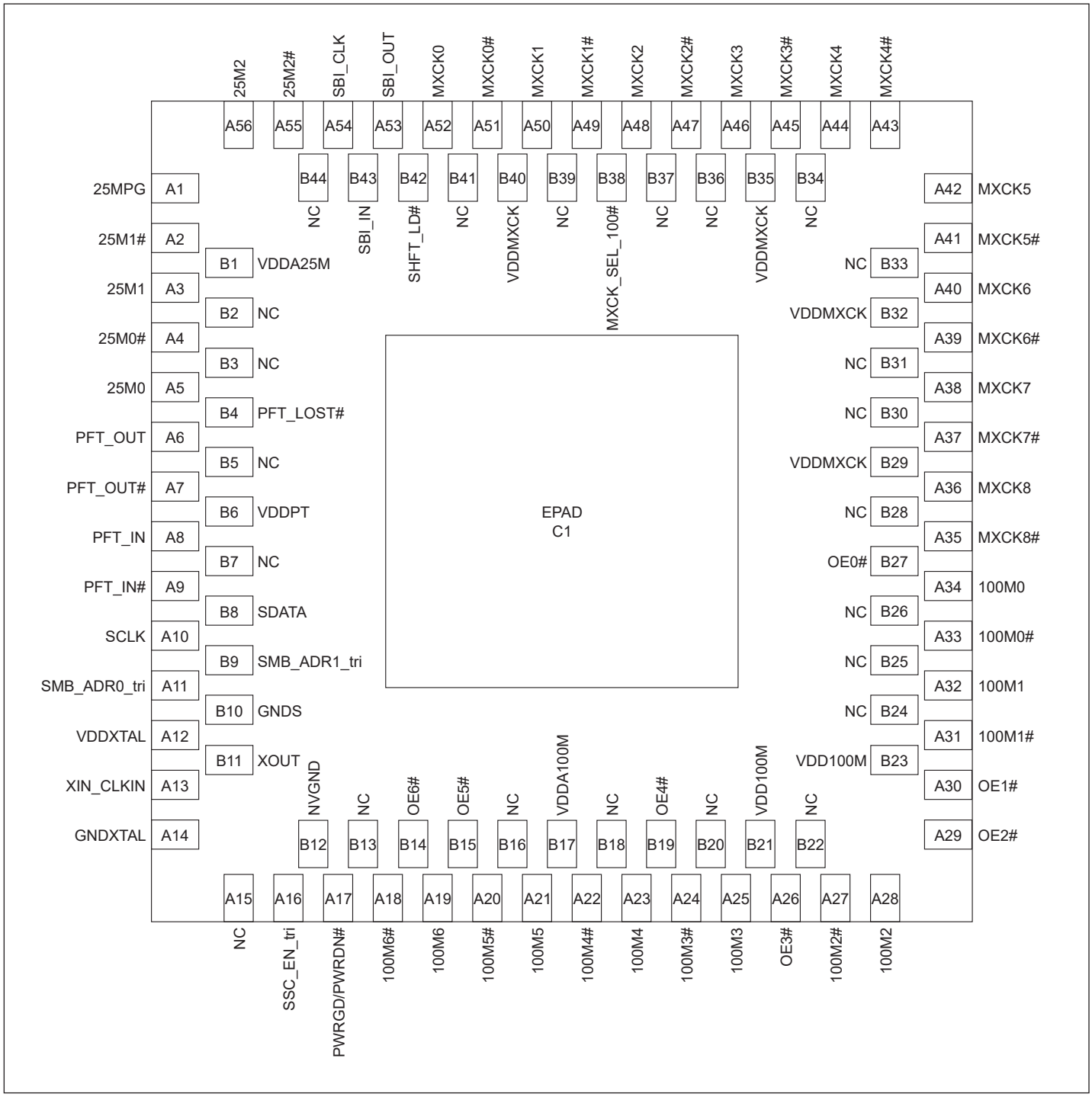
- Supports Intel's CK440Q spec
- 3.3V Supply Voltage
- 25MHz Crystal or an Input from a XO / TCXO / OCXO for meeting Customer Specific PPM Requirements
- 19 Differential Clock Output Pairs @ 1.4V Differential into PCI Express (PCIe) Compliant Test Load
  - 7 dedicated 100MHz outputs
  - 3 dedicated 25MHz outputs
  - 9 selectable outputs capable of driving 25M or 100MHz
- 85Ω Differential Drivers
- Programmable SSC on the 100 MHz
- SMBus Programmable Configurations with multiple SMBus addresses
- Two Tri-level Addresses Selection (9 SMBus Addresses)
- PCIe Compatible OE# control on 7 pins, and 3 wire shift / load control on all outputs
- PCIe 6.0 Common Clock (RMS) Jitter <22fs
- Dedicated pins for Platform Time Input & Output (PFT_IN & PFT_OUT) clocking. PFT function can be bypassed through SMBus Byte 49 for low jitter 25MHz output
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 100-Contact, 8 x 8 mm UQFN (ZUD)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Block Diagram



Pin Configuration



Pin Description

Pin Number	Pin Name	Type		Description
A1	25MPG	Input, PDT	LVTTL	Input to assert power good for the 25M2 output pair before PWRGD is asserted. It has internal pull down resistor.
A2	25M1#	Output	HCSL	±0.7V differential 25MHz clock complement output.
A3	25M1	Output	HCSL	±0.7V differential 25MHz clock true output.
A4	25M0#	Output	HCSL	±0.7V differential 25MHz clock complement output.
A5	25M0	Output	HCSL	±0.7V differential 25MHz clock true output.
A6	PFT_OUT	Output	HCSL	±0.7V 25MHz differential platform time output.
A7	PFT_OUT#	Output	HCSL	±0.7V 25MHz differential platform time complement output.
A8	PFT_IN	Input, PDT	HCSL	±0.7V 25MHz differential platform time input.
A9	PFT_IN#	Input, PDT	HCSL	±0.7V 25MHz differential platform time input.
A10	SCLK	Input, PDT	LVTTL	SMBus slave clock input.
A11	SMB_ADR0_tri	Input	LVTTL	Tri-level LVTTL input to select SMBus address. This pin has internal pull up and pull down resistors. Refer to tri-level input threshold table.
A12	VDDXTAL	Power		Power supply for crystal and clock input.
A13	XIN_CLKIN	Input, PDT		Crystal input/Single-ended input.
A14	GNDXTAL	GND		Ground for crystal
A15	NC	—		No connect
A16	SSC_EN_tri	Input	LVTTL	Tri-level input to enable or disable spread spectrum. Refer to tri-level input threshold table. 0 = SSC off, MID = -0.3% max, and HIGH = -0.5% max. It has internal pull down resistor."
A17	PWRGD/ PWRDN#	Input	LVTTL	Input to power up or power down the device. It has internal pull up resistor.
A18	100M6#	Output	HCSL	±0.7V differential 100MHz clock complement output.
A19	100M6	Output	HCSL	±0.7V differential 100MHz clock true output.
A20	100M5#	Output	HCSL	±0.7V differential 100MHz clock complement output.
A21	100M5	Output	HCSL	±0.7V differential 100MHz clock true output.
A22	100M4#	Output	HCSL	±0.7V differential 100MHz clock complement output.
A23	100M4	Output	HCSL	±0.7V differential 100MHz clock true output.
A24	100M3#	Output	HCSL	±0.7V differential 100MHz clock complement output.
A25	100M3	Output	HCSL	±0.7V differential 100MHz clock true output.
A26	OE3#	Input, PDT	LVTTL	Active low input for enabling 100M3. 1 = disable output, 0 = enable output. It has internal pull down resistor.
A27	100M2#	Output	HCSL	±0.7V differential 100MHz clock complement output.
A28	100M2	Output	HCSL	±0.7V differential 100MHz clock true output.

Pin Number	Pin Name	Type		Description
A29	OE2#	Input, PDT	LVTTL	Active low input for enabling 100M2. 1 = disable output, 0 = enable output. It has internal pull down resistor.
A30	OE1#	Input, PDT	LVTTL	Active low input for enabling 100M1. 1 = disable output, 0 = enable output. It has internal pull down resistor.
A31	100M1#	Output	HCSL	±0.7V differential 100MHz clock complement output.
A32	100M1	Output	HCSL	±0.7V differential 100MHz clock true output.
A33	100M0#	Output	HCSL	±0.7V differential 100MHz clock complement output.
A34	100M0	Output	HCSL	±0.7V differential 100MHz clock true output.
A35	MXCK8#	Output	HCSL	±0.7V differential multiplexable clock complement output.
A36	MXCK8	Output	HCSL	±0.7V differential multiplexable clock true output.
A37	MXCK7#	Output	HCSL	±0.7V differential multiplexable clock complement output.
A38	MXCK7	Output	HCSL	±0.7V differential multiplexable clock true output.
A39	MXCK6#	Output	HCSL	±0.7V differential multiplexable clock complement output.
A40	MXCK6	Output	HCSL	±0.7V differential multiplexable clock true output.
A41	MXCK5#	Output	HCSL	±0.7V differential multiplexable clock complement output.
A42	MXCK5	Output	HCSL	±0.7V differential multiplexable clock true output.
A43	MXCK4#	Output	HCSL	±0.7V differential multiplexable clock complement output.
A44	MXCK4	Output	HCSL	±0.7V differential multiplexable clock true output.
A45	MXCK3#	Output	HCSL	±0.7V differential multiplexable clock complement output.
A46	MXCK3	Output	HCSL	±0.7V differential multiplexable clock true output.
A47	MXCK2#	Output	HCSL	±0.7V differential multiplexable clock complement output.
A48	MXCK2	Output	HCSL	±0.7V differential multiplexable clock true output.
A49	MXCK1#	Output	HCSL	±0.7V differential multiplexable clock complement output.
A50	MXCK1	Output	HCSL	±0.7V differential multiplexable clock true output.
A51	MXCK0#	Output	HCSL	±0.7V differential multiplexable clock complement output.
A52	MXCK0	Output	HCSL	±0.7V differential multiplexable clock true output.
A53	SBI_OUT	Output	LVTTL	Side Band Interface data output.
A54	SBI_CLK	Input, PDT	LVTTL	Side Band Interface clock input for shifting/loading the SBI interface. It has internal pull down resistor.
A55	25M2#	Output	HCSL	±0.7V differential 25MHz clock complement output.
A56	25M2	Output	HCSL	±0.7V differential 25MHz clock true output.
B1	VDDA25M	Power		Analog power supply for 25M outputs.
B2	NC	—		No connect
B3	NC	—		No connect
B4	PFT_LOST#	Output	Open Drain	Asserts when PFT_IN, PFT_IN# clock is not present.
B5	NC	—		No connect
B6	VDDPT	Power		Power supply for platform time circuit and digital.
B7	NC	—		No connect

Pin Number	Pin Name	Type		Description
B8	SDATA	Input/ Output	Open Drain	Open drain bi-directional SMBus data pin.
B9	SMB_ADR1_tri	Input	LVTTL	Tri-level LVTTL input to select SMBus address. This pin has internal pull up and pull down resistors. Refer to tri-level input threshold table.
B10	GNDS	GND		Package shield ground for crystal oscillator circuit. This pin is not connected internally.
B11	XOUT	Output		Output of internal crystal oscillator. This pin should be left floating if CLK_IN function is being used.
B12	NVGND	GND		Ground
B13	NC	—		No connect
B14	OE6#	Input, PDT	LVTTL	Active low input for enabling 100M6. 1 = disable output, 0 = enable output. It has internal pull down resistor.
B15	OE5#	Input, PDT	LVTTL	Active low input for enabling 100M5. 1 = disable output, 0 = enable output. It has internal pull down resistor.
B16	NC	—		No connect
B17	VDDA100M	Power		Analog power supply for 100M outputs.
B18	NC	—		No connect
B19	OE4#	Input, PDT	LVTTL	Active low input for enabling 100M4. 1 = disable output, 0 = enable output. It has internal pull down resistor.
B20	NC	—		No connect
B21	VDD100M	Power		Power supply for 100M outputs.
B22	NC	—		No connect
B23	VDD100M	Power		Power supply for 100M outputs.
B24	NC	—		No connect
B25	NC	—		No connect
B26	NC	—		No connect
B27	OE0#	Input, PDT	LVTTL	Active low input for enabling 100M0. 1 = disable output, 0 = enable output. It has internal pull down resistor.
B28	NC	—		No connect
B29	VDDMXCK	Power		Power supply for MXCK outputs.
B30	NC	—		No connect
B31	NC	—		No connect
B32	VDDMXCK	Power		Power supply for MXCK outputs.
B33	NC	—		No connect
B34	NC	—		No connect
B35	VDDMXCK	Power		Power supply for MXCK outputs.
B36	NC	—		No connect
B37	NC	—		No connect
B38	MXCK_ SEL_100M#	Input	LVTTL	Input to select the source of the multiplexable clock outputs. 0 = 100 MHz, 1 = 25 MHz. It has internal pull down resistor.

Pin Number	Pin Name	Type		Description
B39	NC	—		No connect
B40	VDDMXCK	Power		Power supply for MXCK outputs.
B41	NC	—		No connect
B42	SHFT_LD#	Input, PDT	LVTTL	Input to control shifting and loading of the Side-Band Interface to the Output Enable Control Register. The pin has internal pull down resistor.
B43	SBI_IN	Input, PDT	LVTTL	Side Band Interface data input. It has internal pull down resistor.
B44	NC	—		No connect
C1	EPAD	GND		Connect EPAD to ground.

Power Down Tolerant (PDT)

The pins with PDT type may be driven by external signals when the device is in a power down or reset condition. The device must reset and power up properly if these pins are driven to any valid voltage prior to the assertion of VDD or PWRGD#.

Power Management Table for 100M[6:0] Outputs

PWRGD/PWRDN#	OEx# Pin	SMBus OE Bit	SBI Mask Bit	SBI Output Control Register	100M[6:0]
0	X	X	X	X	Disabled
1	1	X	X	X	Disabled
	X	0	X	X	Disabled
	X	X	0	0	Disabled
	0	1	X	1	Running
	0	1	1	X	Running

Power Management Table for 25M[2:0] and MXCK[8:0] Outputs

PWRGD/PWRDN#	SMBus OE Bit	SBI Mask Bit	SBI Output Control Register	25MPG	25M[1:0], MXCK[8:0]	25M[2]
0	X	X	X	0	Disabled	Disabled
	X	X	X	1	Disabled	Running
1	0	X	X	X	Disabled	Disabled
	1	0	0	X	Disabled	Disabled
	1	X	1	X	Running	Running
	1	1	X	X	Running	Running

Power Good and Power Down

PWRGD is asserted high and de-asserted low. De-assertion of PWRGD (pulling the signal low) is equivalent to indicating a power down condition. PWRGD (assertion) is used by the PI6CG330440 to sample initial configurations such as SMB_ADRn_tri selections.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power savings mode. PWRDN# is a completely asynchronous active low input. When entering power savings mode, PWRDN# should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When PWRDN# is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters. The assertion and de-assertion of PWRDN# is asynchronous.

When PWRDN# is sampled low by two consecutive rising edges of 100M#, all differential outputs must held low on the next 100M# high to low transition, as shown in Figure 1.

PWRGD to the clock buffer shall not be asserted before VDD reaches VDDmin. Prior to VDDmin it is recommended to hold PWRGD low (less than 0.5V).

The power-up latency TSTABLE is to be less than 5 ms. This is the time from the assertion of the PWRGD signal to the time that stable clocks are output from the buffer chip. All differential outputs stopped in a Low/Low condition resulting from power down must be driven high in less than 300 µs of PWRGD assertion to a voltage greater than 200 mV, as shown in Figure 2.

PWRDN# Assertion

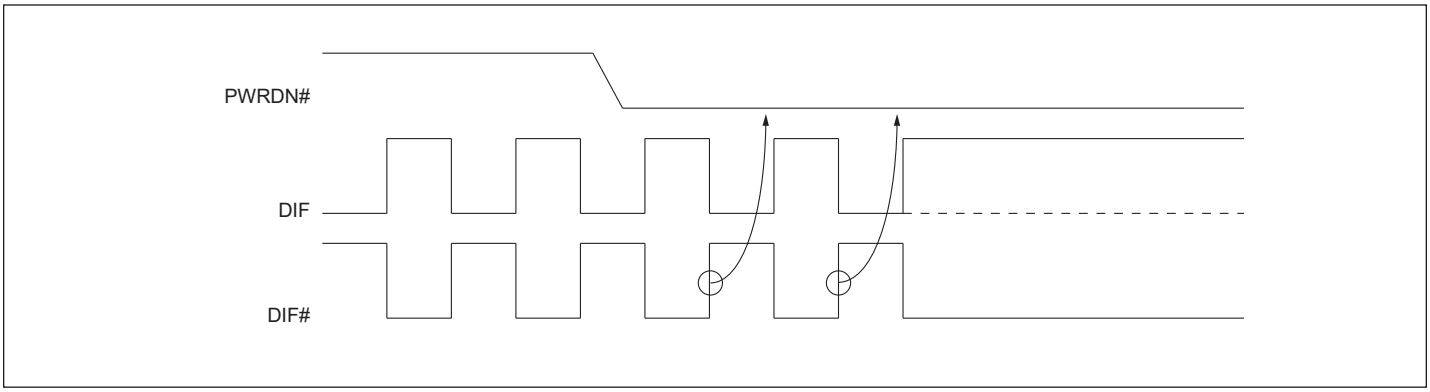


Figure 1. PWRDN# Assertion Timing

PWRGD Assertion

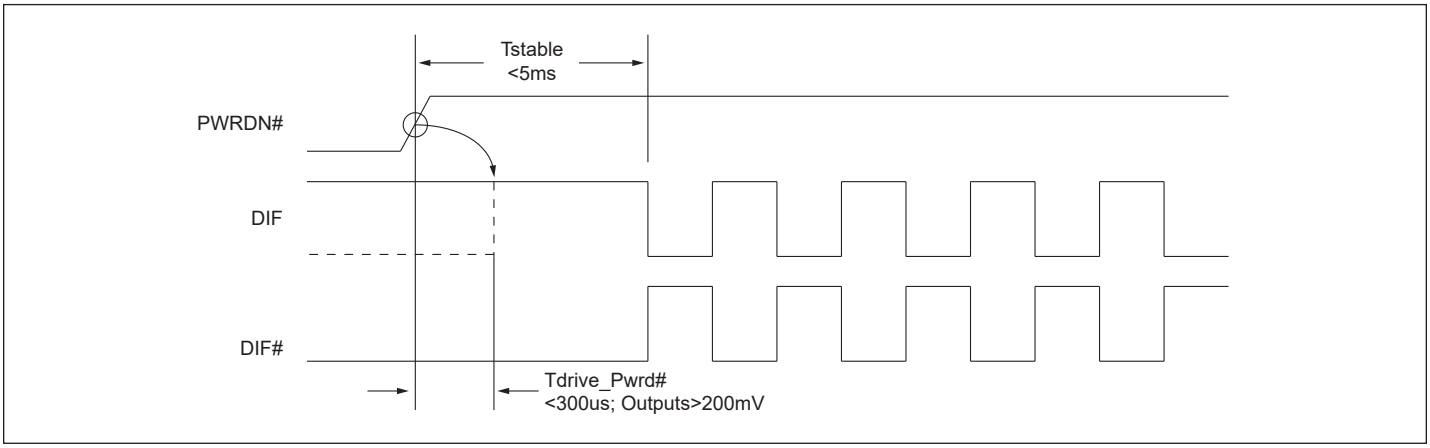


Figure 2. PWRGD Assertion Timing

Output Enable Control

The PI6CG330440 has three methods for enabling and disabling outputs. In order for an output to be enabled, ALL three methods must enable the output. If ANY method disables the output, the output will be disabled. Clocks always start and stop in a glitch free manner, meaning duty cycle requirements are still met.

The first is the traditional method of OE# pins that are used for PCI Express clock enabling at the PCIe connector. Each of the 7 dedicated 100MHz clock outputs can be enabled or disabled with the OE[6:0]# pins individually. The OE# pin must be pulled low to enable the output.

The second method is by using the SMBus output enable bits. Any of the 19 outputs have dedicated SMBus output enable bits in Bytes[0:2] of the SMBus register set that can enable or disable the clock outputs. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

The third is using the Side Band Interface (SBI). This is a DB2000QL compatible method of enabling outputs using a hardware shift / load method. Refer to Power Management Tables for the truth table for enabling and disabling outputs via hardware and software. All three methods must be set to "enable" for the clock to be active on that pin.

Side-Band Interface

This interface consists of SBI_IN, SBI_CLK, SHFT_LD#, and SBI_OUT pins. When the SHFT_LD# pin is high, the rising edge of SBI_CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT_LD# loads the shift register contents to the output control register.

Since the PI6CG330440 has dedicated pins for the SBI, both SBI and the traditional SMBus methods are active at the same time. There are SMBus registers for masking off the disable function of the SBI interface. When set to a one, the mask register forces the SBI interface for its respective output to indicate 'enabled'. This prevents accidentally disabling critical outputs when using the SBI. However the traditional SMBus enable bits and the OE# pins may still disable an output. If the application does not use the SBI, the SBI input pins may be tied 'Low'. Figure 3 provides a high level functional description of the SBI.

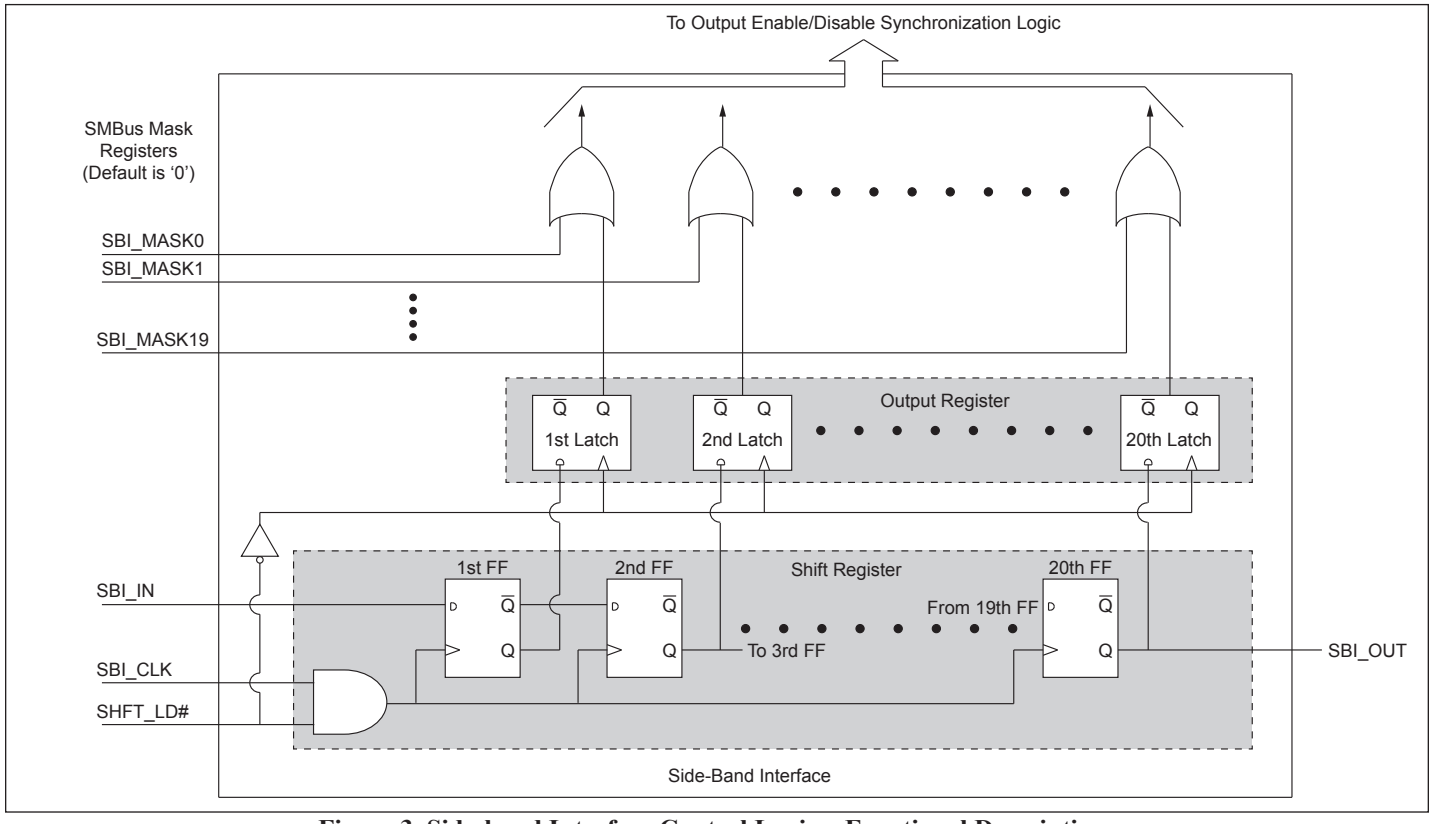


Figure 3. Side-band Interface Control Logic – Functional Description

Output Enable / Disable Priority

The PI6CG330440 requires that outputs be enabled by an 'AND' function of all methods of enabling the output. Figure 4 illustrates this. There are three enable/disable paths: OE# pin (if present), a SMBus OE bit and the Side-Band Interface. All three must indicate 'enable' for the output to be enabled. Conversely, any single enable/disable path can disable an output if it indicates 'disable'.

Additionally, the Side-Band Interface indicates a 'high' if the SBI_Mask_Bit OR the SBI_Output Register Bit are 'high'. This means that the SBI_MASK_Bit can prevent the SBI interface from disabling an output. Note that the SBI_MASK_Bits are SMBus registers. The shift order follows the order of the SMBus enable bits in Byte[2:0] as shown in Figure 5. The first bit shifted in would be the output enable for the PFT_OUT, which is in Byte 2 bit 3. The last bit shifted in would be the output enable for 100M0, which is in Byte 0, bit 0.

The SMBus registers for the SBI Output and SBI_Mask follow the same bit order. Note that the SBI Output register contains the value latched from the shift register. Software must apply the SBI Mask bits to this value to get the output of the Side-Band Interface OR gate in Figure 4. Figure 6 shows the basic timing of the side-band interface. The SHFT_LD# pin goes high to enable the SBI_CLK input. Next, the rising edge of SBI_CLK clocks SBI_IN data into the shift register. After the 20th clock, stop the clock low and drive the SHFT_LD# pin low. The falling edge of SHFT_LD# latches the shift register contents to the output control register, enabling or disabling the outputs. Always shift 20 bits of data into the shift register to control the outputs.

The SBI interface supports clock rates up to 25MHz. The PI6CG330440 allows two SBI connection topologies – star and daisy chain. In a star topology, multiple devices may share SBI_CLK and SBI_IN pins. In this topology, each PI6CG330440 has a dedicated SHFT_LD# pin. In a daisy-chain topology, the SBI_OUT of one device connects to the SBI_IN device of a downstream device. When using the daisy chain topology, the user must shift a complete set of bits for the combined devices. Two daisy-chained PI6CG330440 devices require shifting of 40 bits. When the SHFT_LD# pin is low, the SBI interface ignores any activity on the SBI_CLK and SBI_IN pins. Figure 7 illustrates a star topology connection for the PI6CG330440 SBI interface. The star topology allows independent configuration of each device. For PI6CG330440, this means shifting 20 bits at a time. A disadvantage is that a separate SHFT_LD# pin is required for each device.

The daisy chain topology allows configuration of any number of devices with only three signals from the SBI controller. It utilizes the SBI_OUT pin of one device to drive the SBI_IN pin of the next device in the daisy chain. Users must take care to shift the proper number of bits in this configuration. For the example shown in Figure 8, the SBI bit stream consists of 40 bits.

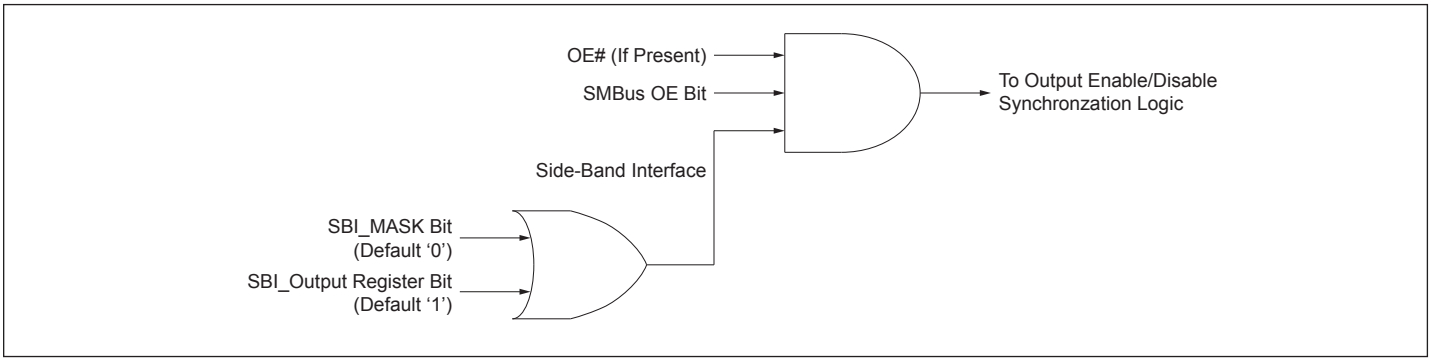


Figure 4. Output Enable Logic (per output)

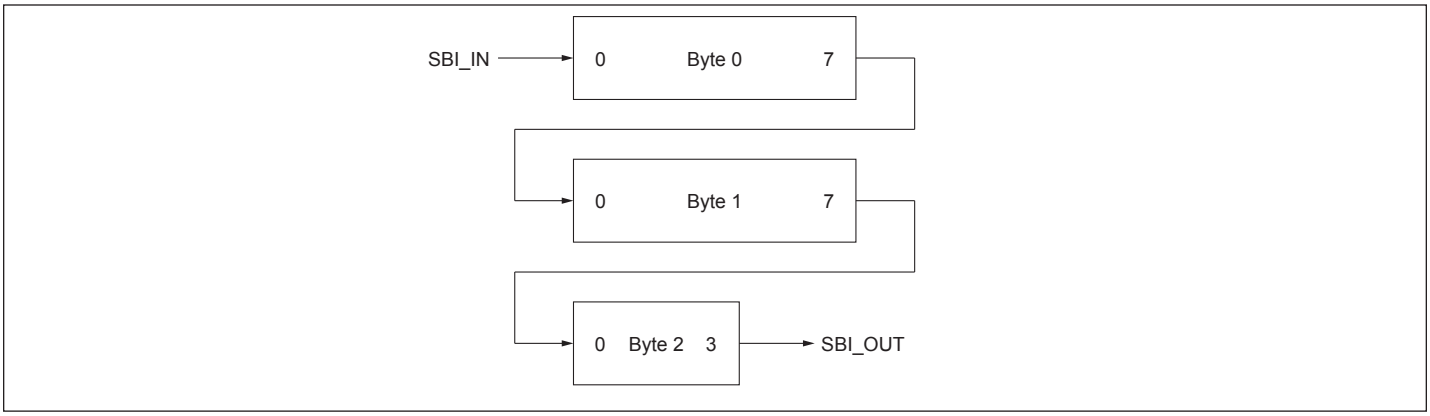


Figure 5. Side-Band Shift Order

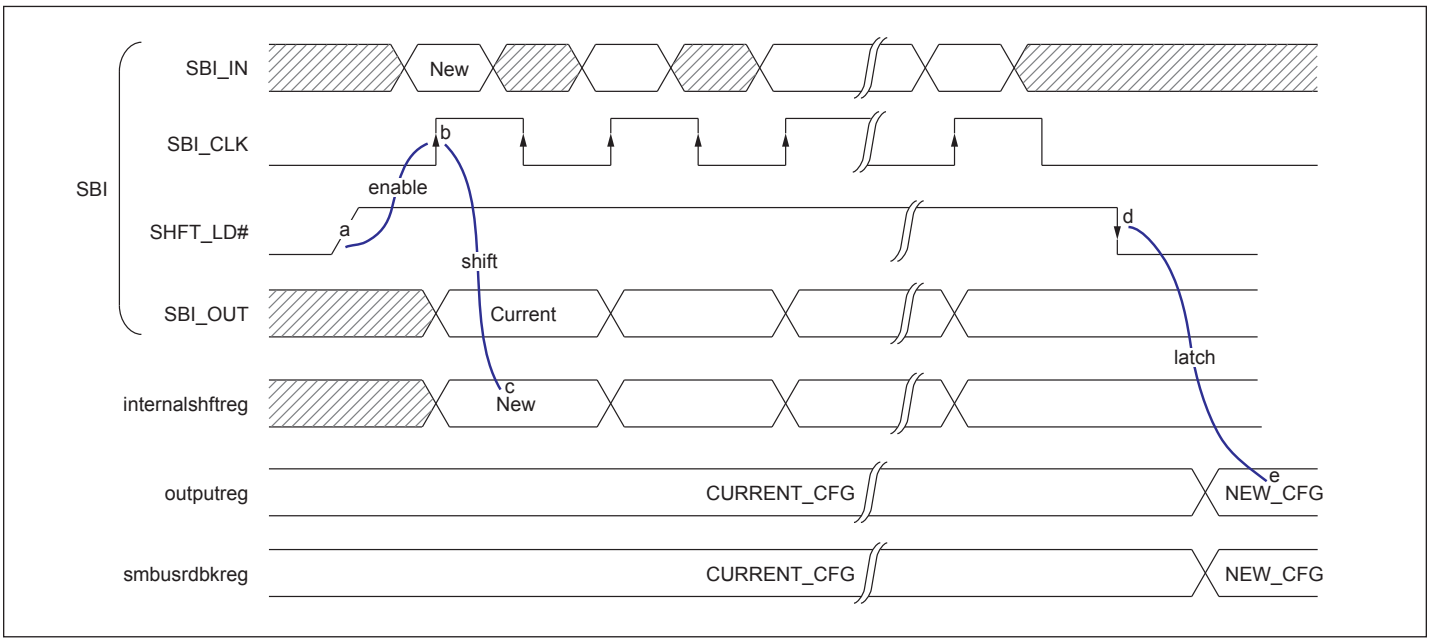


Figure 6. Side Band Interface Functional Timing

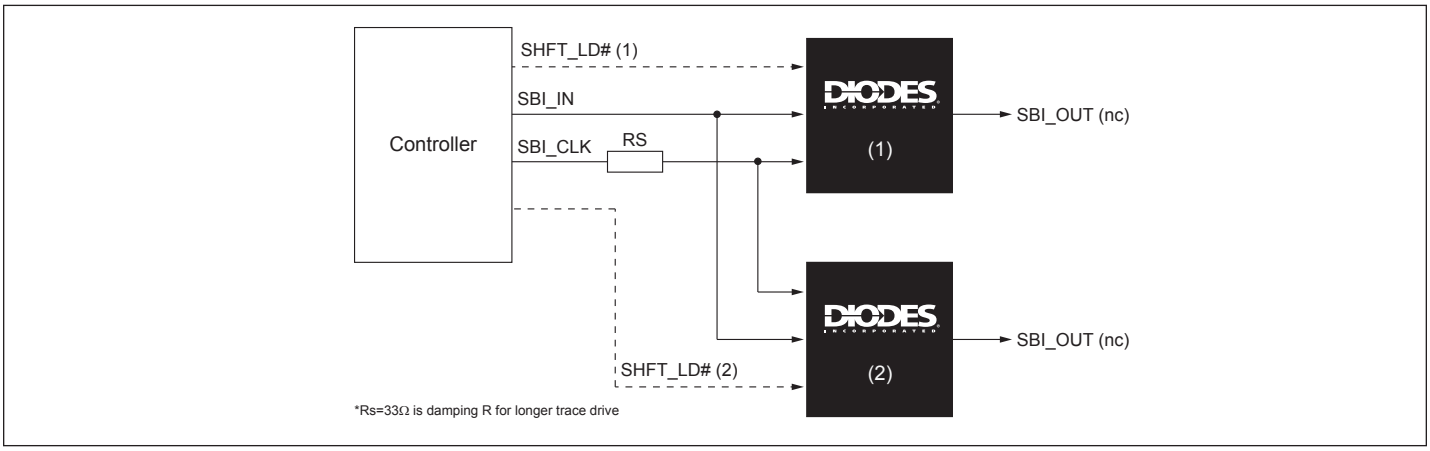


Figure 7. Star SBI Topology

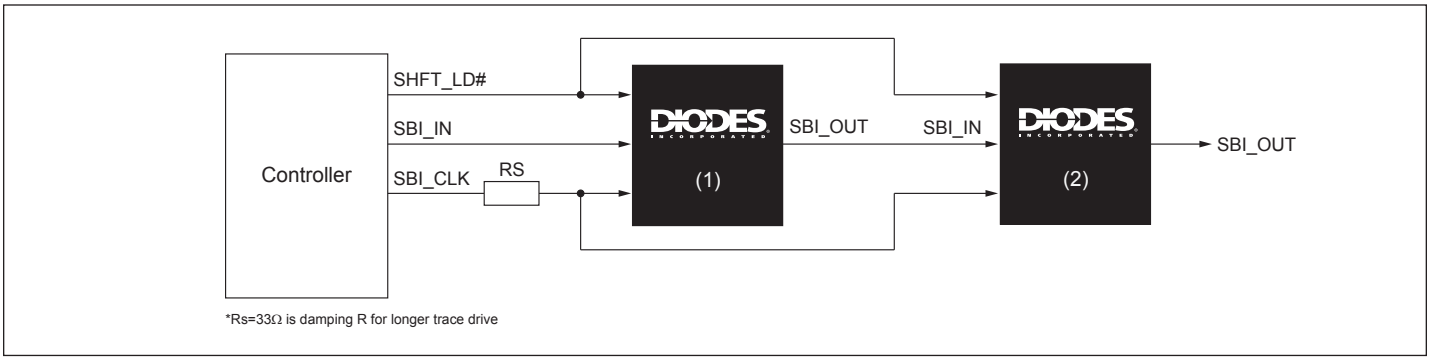


Figure 8. Daisy-Chain SBI Topology

Platform Time (PFT) Phase/Frequency Tracking

PFT_IN/OUT allows different CK440 compliant devices to frequency lock the 25 MHz clocks to a single time base. The system implementation is shown in Figure 9. The local 25 MHz frequency locks to the PFT_IN clock if it is present. If PFT_IN is not present, the local 25MHz frequency is sourced from the local crystal. The output signal PFT_LOST# asserts if the PFT_IN clock is not present. If the PFT_IN clock is lost during operation, PFT_OUT and all other clocks are continued without timing glitches. If the PFT_IN clock is applied during operation, the frequency lock occurs according to the PFT filter to ensure a glitchless output of PFT_OUT.

PFT_IN does not replace the need for the local crystal oscillator and may not be used as the oscillator source. If PFT function is not needed and a low jitter 25MHz output is needed, PI6CG330440 can be configured to bypass the PFT function using SMBus Byte 49.

The signed PPM difference between the supplied PFT_IN clock and the local crystal oscillator can be read in the SMBUS registers. The PPM difference is defined as the number of 1 ns steps that were required in the last 216 clocks, signed for direction.
The platform time tracking must be able to track ±125 PPM difference between the local clock and the PFT_IN clock. No phase relationship is needed between PFT_IN and any of the 25 MHz outputs, this is a frequency lock only. All 25 MHz clock specifications, such as min and max period, must be met during tracking. The PFT_OUT timing parameters are given in Table below.

Timing Parameters – Platform Time

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{PERIOD}	PFT_OUT Period	Clock period	38	40	42	ns
PFT_PPM	PPM tracking		+/-125			ppm

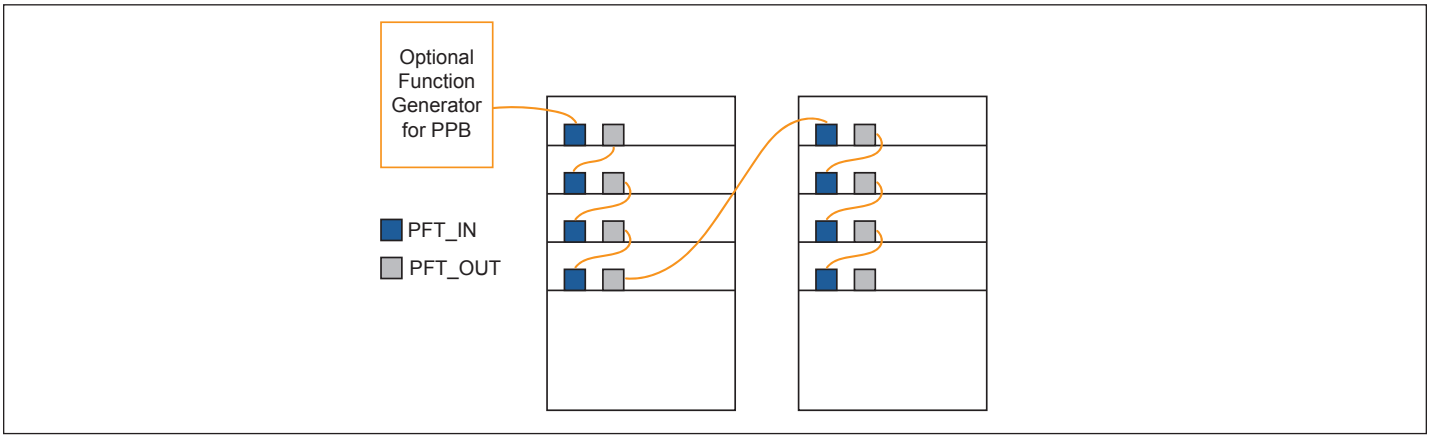


Figure 9. Frequency Lock

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, V_{DDxx} .....–0.5V to +4.0V
Input Control Pins Voltage ..... –0.5V to V_{DD}+0.5V
CLK+/- pins .....-0.5V to 2.5V
SMBus, Input High Voltage 3.6V
ESD Protection (HBM) 2000V
Junction Temperature ..... 125 °C Max.

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DD}, V_{DD_A}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DDMXCK}	Normal Operating Mode Power Supply Current(1)	V_{DDMXCK}, MXCK[8:0] at 100MHz		70	105	mA
I_{DD100M}		V_{DD100M}, 100M[6:0]		56	84	mA
I_{DDXTAL}		V_{DDXTAL}, 25MHz Xtal		18	27	mA
I_{DDPT}		V_{DDPT}, PFT circuit active		0.5	0.75	mA
		V_{DDPT}, PFT circuit not used (no PFT_IN)		0.5	0.75	mA
I_{DDA25M}		V_{DDA25M}, 25M[2:0] on		30	45	mA
$I_{DDA100M}$		$V_{DDA100M}$, 100M[6:0] on, SSC on		30	45	mA
I_{DDMXCK}	25MPG Mode Power Supply Current(2)	V_{DDMXCK}, MXCK[8:0]		2.5	3.75	mA
I_{DD100M}		V_{DD100M}, 100M[6:0]		2.5	3.75	mA
I_{DDXTAL}		V_{DDXTAL}, 25MHz Xtal		3.5	5.25	mA
I_{DDPT}		V_{DDPT}		0.5	0.75	mA
I_{DDA25M}		V_{DDA25M}, 25M[2] on		25	37.5	mA
$I_{DDA100M}$		$V_{DDA100M}$		0.5	0.75	mA
I_{DDMXCK}	Power Down Mode Power Supply Current(3)	V_{DDMXCK}, MXCK[8:0]		2.5	3.75	mA
I_{DD100M}		V_{DD100M}, 100M[6:0]		2.5	3.75	mA
I_{DDXTAL}		V_{DDXTAL}, 25MHz Xtal		4	6	mA
I_{DDPT}		V_{DDPT}		0.5	0.75	mA
I_{DDA25M}		V_{DDA25M}, 25M[2]off		10	13.5	mA
$I_{DDA100M}$		$V_{DDA100M}$		0.5	0.75	mA
T_A	Ambient Temperature	Industrial grade	–40		85	°C

Note:
1. PWRGD/PWRGDN# = 1, all outputs enabled.
2. PWRGD/PWRGDN# = 0, 25MPG = 1.
3. PWRGD/PWRGDN# = 0, 25MPG = 0.

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal pull up resistance			120		KW
R_{dn}	Internal pull down resistance			120		KW
$R_{dn\_PFT\_IN\#}$	Internal resistor to bias at 0.5V on PFT_IN#	Use internal resistor divider		50		KW
$R_{dn\_PFT\_IN}$	Internal pull down resistor on PFT_IN			50		KW
L_{PIN}	Pin inductance				7	nH

Crystal Characteristics

Symbol	Parameters	Min.	Typ.	Max.	Units
OSCmode	Mode of Oscillation		Fundamental		–
FREQ	Frequency		25		MHz
ESR(1)	Equivalent Series Resistance			50	W
Cload	Load Capacitance		8		pF
Cshunt	Shunt Capacitance			7	pF
–	Drive Level			200	µW

Note:

1. ESR value is dependent upon frequency of oscillation

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDSMB}	Nominal bus voltage		2.7		3.6	V
V_{IHSMB}	SMBus Input High Voltage	SMBus, V_{DDSMB} = 3.3V	2.1		3.6	V
		SMBus, V_{DDSMB} < 3.3V	0.65* V_{DDSMB}			
V_{ILSMB}	SMBus Input Low Voltage	SMBus, V_{DDSMB} = 3.3V			0.6	V
		SMBus, V_{DDSMB} < 3.3V			0.6	
$I_{SMBSINK}$	SMBus sink current	SMBus, at V_{OLSMB}	4			mA
V_{OLSMB}	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$			0.4	V
SMBus Standard Mode at 100kb/s (100k Class)						
f_{MAXSMB}	SMBus operating frequency	Maximum frequency			100	kHz
t_{BUF}	Bus Free Time	Between STOP and START	4.7			us
t_{HD_STA}	Hold Time	After (REPEATED) START	4			us
t_{SU_STA}	Setup Time	REPEATED START	4.7			us

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{SU_STO}	Setup Time	STOP	4			us
t_{HD_DAT}	Hold Time	Data	300			ns
t_{SU_DAT}	Setup Time	Data	250			ns
t_{TIMOUT}	Timeout	Detect SMBDAT Low	25		35	ms
t_{TIMOUT}	Timeout	Detect Clock Low	25		35	ms
t_{LOW}	Clock Low Period		4.7			us
t_{HIGH}	Clock High Period		4		50	us
t_{RMSB}	SMBus rise time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)			1000	ns
t_{FMSB}	SMBus fall time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)			300	ns
t_{POR}	Time after power on reset	Power on and PWRGD/PWRDN#= 1			5	ms
SMBus Fast Mode at 400kb/s (400k Class)						
f_{MAXSMB}	SMBus operating frequency	Maximum frequency			400	kHz
t_{BUF}	Bus Free Time	Between STOP and START	1.3			us
t_{HD_STA}	Hold Time	After (REPEATED) START	0.6			us
t_{SU_STA}	Setup Time	REPEATED START	0.6			us
t_{SU_STO}	Setup Time	STOP	0.6			us
t_{HD_DAT}	Hold Time	Data	300			ns
t_{SU_DAT}	Setup Time	Data	100			ns
t_{TIMOUT}	Timeout	Detect SMBDAT Low	25		35	ms
t_{TIMOUT}	Timeout	Detect Clock Low	25		35	ms
t_{LOW}	Clock Low Period		1.3			us
t_{HIGH}	Clock High Period		0.6		50	us
t_{RMSB}	SMBus rise time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)			300	ns
t_{FMSB}	SMBus fall time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)			300	ns
t_{POR}	Time after power on reset	Power on and PWRGD/PWRDN#= 1			5	ms

Note:

1. After this period, the first clock is generated.
2. The device maintains 300ns data hold time for backwards compatibility with the SMBus 2.0 specification. Newer versions of the SMBus specification call out 0ns data hold time for both 100kHz and 400kHz classes.
3. The device provided additional SMBus protection by implementing a timeout for SMBDATA being held low in excess of tTIMEOUT, in addition to the SMBCLK low timeout.
4. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of tTIMEOUT, Minimum. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than tTIMEOUT, Maximum. Typical device examples include the host controller, and embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for tTIMEOUT, Maximum or longer.
5. tHIGH, Maximum provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than tHIGH, Maximum.

LVCMOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs, except trilevel pins	2		V_{DD} +0.3	V
V_{IL}	Input Low Voltage	Single-ended inputs, except trilevel pins	-0.3		0.8	V
V_{IH}	Input High Voltage	Single-ended trilevel inputs	2.5		V_{DD} +0.3	V
V_{IM}	Input Mid Voltage	Single-ended trilevel inputs	1.2	$V_{DD/2}$	1.8	V
V_{IL}	Input Low Voltage	Single-ended trilevel inputs	-0.3		0.8	V
I_{IH}	Input High Current	Single-ended inputs, $V_{IN} = V_{DD}$			5	mA
		Single-ended inputs with pull down resistor, $V_{IN} = V_{DD}$			50	mA
I_{IL}	Input Low Current	Single-ended inputs, $V_{IN} = 0V$	-5			µA
		Single-ended inputs with pull up resistor, $V_{IN} = 0V$	-50			µA
C_{IN}	Input Capacitance(1)	Logic inputs, except differential inputs			4.5	pF
		Differential clock inputs	1.5		2.7	pF
C_{OUT}	Output Capacitance(1)	Output pin capacitance			4.5	pF

LVCMOS AC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency			25		MHz
t_{STAB}	Clock Stabilization	From VDD power-up and after input clock stabilization or de-assertion of PWRDN# to valid outputs.			5	ms
t_{PDLAT}	PD# de-assertion	Differential outputs enable after PD# de-assertion		100	200	us
t_{OELAT}	Output enable latency	100M start after OE# assertion 100M stop after OE# deassertion	4		10	clocks
t_{PDLAT}	PWRDN# de-assertion	Differential outputs enable after PWRDN# de-assertion		10	50	us
t_{RF}	Rise and Fall Time	Control inputs (2)			5	ns

Note:
1. Guaranteed by design and characterization, not 100% tested in production.
2. Control input must be monotonic from 20% to 80% of input swing.

PFT Differential Input Characteristics(1)

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency			25		MHz
V_{IHDIF}	Diff. Input High Voltage (3)	IN+, IN-, single-end measurement	330		1150	mV
V_{ILDIF}	Diff. Input Low Voltage (3)	IN+, IN-, single-end measurement	-300	0	300	mV
V_{SWING}	Diff. Input Swing Voltage	Peak to peak value (V_{IHDIF} - V_{ILDIF})	200		2000	mV
V_{COM}	Common Mode Voltage		100		1000	mV
t_{RF}	Diff. Input Slew Rate (2)		0.7			V/ns
I_{IN}	Diff. Input Leakage Current	$V_{IN} = V_{DD}$, V_{IN} = GND	-50		100	uA
t_{DC}	Diff. Input Duty Cycle	Measured differentially	45		55	%
tj_{c-c}	Diff. Input Cycle to cycle jitter	Measured differentially			125	ps

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Slew rate measured through +/-75mV window centered around differential zero
3. The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the Vbias, where Vbias is (V_{IH}-V_{IL})/2

HCSL Output Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
Outputs Driving High Impedance Receiver						
V_{MAX}	Maximum Output Voltage (1,5,6)	Measurement on single ended signal using absolute value	660	800	1150	mV
V_{MIN}	Minimum Output Voltage (1,5,6)		-150	20	150	mV
Vcross abs	Absolute Crossing Point Voltage	Scope averaging off.	250	400	500	mV
Vcross rel	Relative Crossing Point Voltage	Scope averaging off.		0	100	mV
t_{RF}	Slew Rate (1,2,3)	Scope averaging on, 10 inch trace	2	3.0	4	V/ns
Dt_{RF}	Slew Rate Matching (1,2,4)	Scope averaging on, 10 inch trace		6	19	%
Outputs Driving Terminated Receiver (Double Termination, see test setup in Figure 11)						
V_{MAX}	Maximum Output Voltage (1,5,6)	Measurement on single ended signal using absolute value			V_{OH} +75	mV
V_{MIN}	Minimum Output Voltage (1,5,6)		V_{OL} - 75			mV
V_{OH}	Output High Voltage		225		270	mV
V_{OL}	Output Low Voltage		10		150	mV
Vcross abs	Absolute Crossing Point Voltage	Scope averaging off.	130		200	mV
Diff-Z	Output Differential Impedance	Measured at V_{OL} / V_{OH}	85 - 5%		85 + 5%	W
Diff-$Z_{CROSS-ING}$	Output Differential Impedance	Measured during a transition	85 - 20%		85 + 20%	W
t_{SKEWGP}	Output Skew Within a Group (1,2)	Groups are 25M[2:0], MXCK[8:0], and 100M[6:0]		25		ps

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$t_{SKEWG-P2GP}$	Output Skew Across Groups (1,2)	Across 25M[2:0] and MXCK[8:0] set to 25MHz or 100M[6:0] and MXCK[8:0] set to 100MHz		100		ps
t_{DC100M}	Duty Cycle	100MHz Outputs and MXCLK outputs set to 100MHz.	45		55	%
t_{DC25M}	Duty Cycle	25MHz Outputs and MXCLK outputs set to 25MHz with XTAL as source	47		53	%
t_{DC100M}	Duty Cycle	25MHz Outputs and MXCLK outputs set to 25MHz with XO as source with 44/55% duty cycle	45		55	%
tj_{c-c25M}	Cycle to cycle jitter (1,2)	25MHz Outputs and MXCLK outputs set to 25MHz		0.5	1	ns
tj_{c-c25M}	Cycle to cycle jitter (1,2,7)	25MHz Outputs and MXCLK outputs set to 25MHz in PFT bypass mode		30	40	ps
$tj_{c-c100M}$	Cycle to cycle jitter (1,2)	100MHz Outputs and MXCLK outputs set to 100MHz		25	40	ps

Note:
1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within +/-150mV window
4. Slew rate matching is measured through +/-75mV window centered around differential zero
5. At default SMBus settings.
6. Includes 300mV of overshoot for Vmax and 300mV of undershoot for Vmin.
7. SMBus Byte 49 is set in PFT Bypass mode

PCIe Common Clock (CC) Architecture Jitter

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
t_{jPHASE}	Integrated phase jitter (RMS)	PCIe 1.0		20	60	86	ps (pkpk)
		PCIe 2.0 Low Band, 10kHz < f < 1.5MHz (PLL BW 5-16MHz or 8-5MHz, CDR = 10MHz)		0.06	0.15	3	ps
		PCIe 2.0 High Band, 1.5MHz < f < Nyquist (50MHz); (PLL BW 5-16MHz or 8-5MHz, CDR = 10MHz)		0.2	0.3	3.1	ps
		PCIe 3.0 (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0.07	0.12	1	ps
		PCIe 4.0 (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0.03	0.05	0.5	ps
		PCIe 5.0		0.03	0.05	0.15	ps
		PCIe 6.0		0.01	0.02	0.1	ps

PCIe Independent Reference Clock Architecture Jitter

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
t_{jPHASE}	Integrated phase jitter (RMS)	PCIe 3.0 SRIS (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0.1	0.3		ps
		PCIe 4.0 SRIS (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0.1	0.3		ps
		PCIe 5.0 SRIS		0.03	0.1		ps
		PCIe 6.0 SRIS		0.06	0.1		ps

Side Band Signal Characteristics

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
t_{PERIOD}	Clock Period		40			ns
t_{SETUP}	SHFT Setup Time to Clock	SHFT_LD# high to SBI_CLK rising edge	10			ns
t_{SHD} (1)	SHFT Hold Time to Clock	SHFT_LD# hold (high) after SBI_CLK rising edge (SBI_CLK to SHFT_LD# falling edge)	10			ns
t_{DSU} (1)	SBI_IN Setup Time	SBI_IN setup to SBI_CLK rising edge	5			ns
t_{DHD} (1)	SBI_IN Hold Time	SBI_IN hold after SBI_CLK rising edge	2			ns
t_{COUT} (1)	SBI_CLK to SBI_OUT	SBI_CLK rising edge to SBI_OUT valid	2			ns
t_{EN} (1)	Enable/Disable Time	Delay from SHFT_LD# falling edge to next output configuration taking effect. Refers to device differential input clock	4		10	clocks
t_{SLEW} (1,2)	Slew Rate	SBI_CLK input (between 20% and 80%)	0.7		4	V/ns

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Control input must be monotonic from 20% to 80% of input swing.

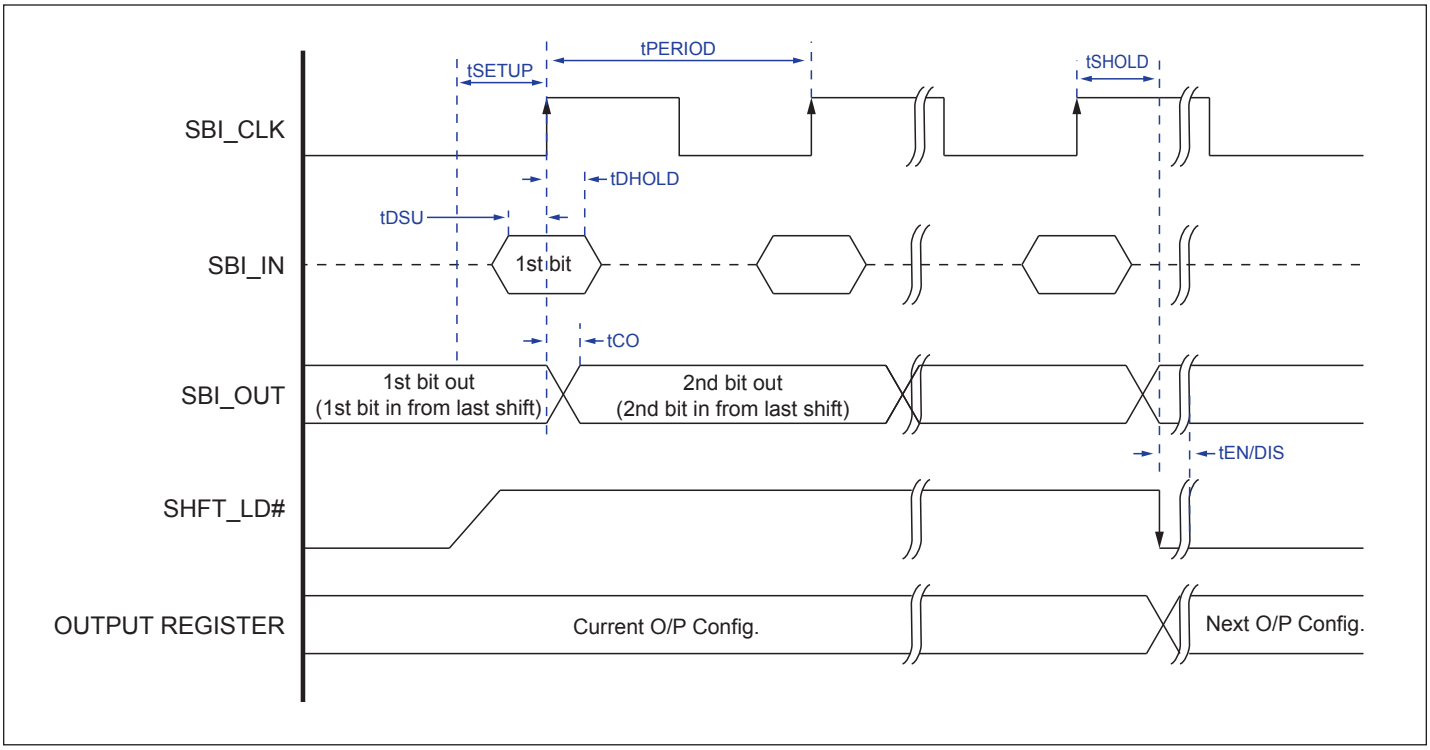
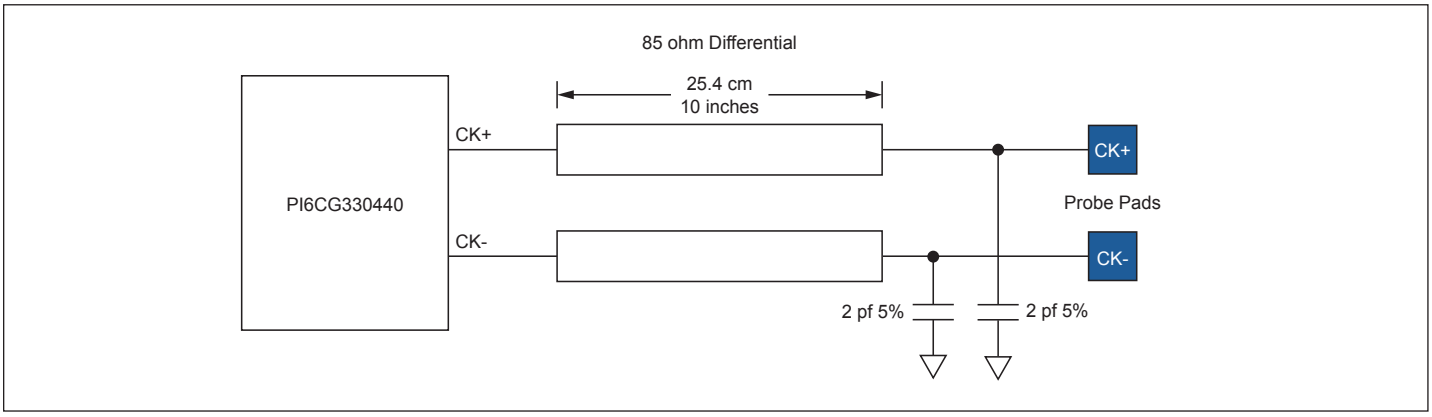


Figure 9. Side Band Interface Timing

AC/DC Test Load



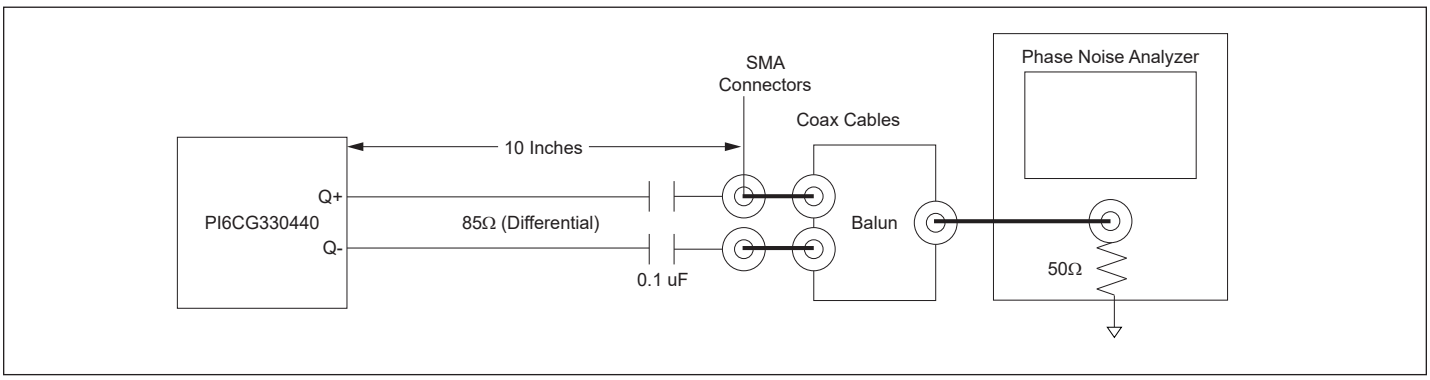


Figure 10. Test Setup for PCIe Jitter Measurement

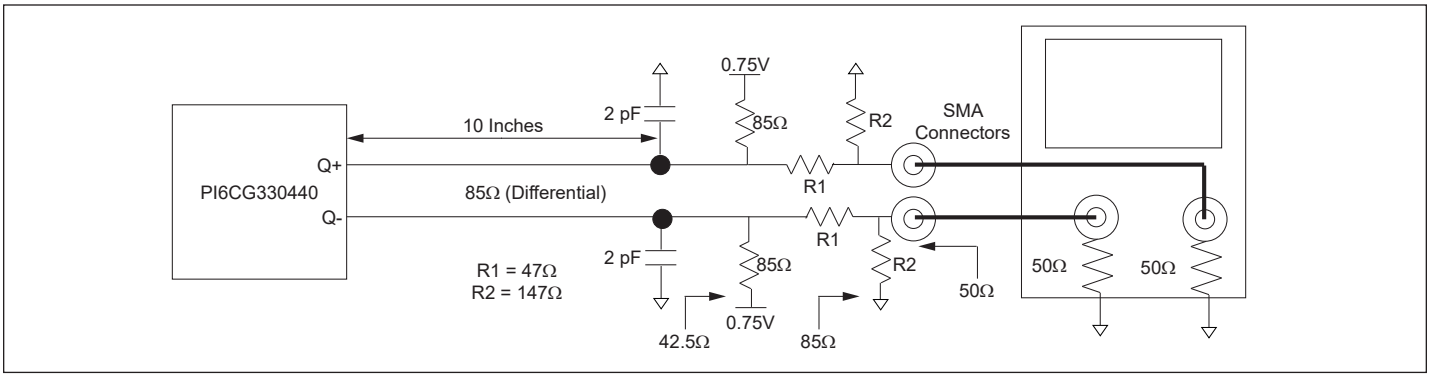


Figure 11. Test Setup for Double Termination

Power Supply Noise Profile

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{DD_AC}	Power Supply Noise	Single tone AC noise, swept		40		mV
V_{DDA_AC}	Power Supply Noise	VDDA electrical noise > 20MHz.		20		mV
V_{DDXTAL}	Power Supply Noise	VDDXTAL electrical noise 12kHz to 25MHz.		20		mV

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Control input must be monotonic from 20% to 80% of input swing.

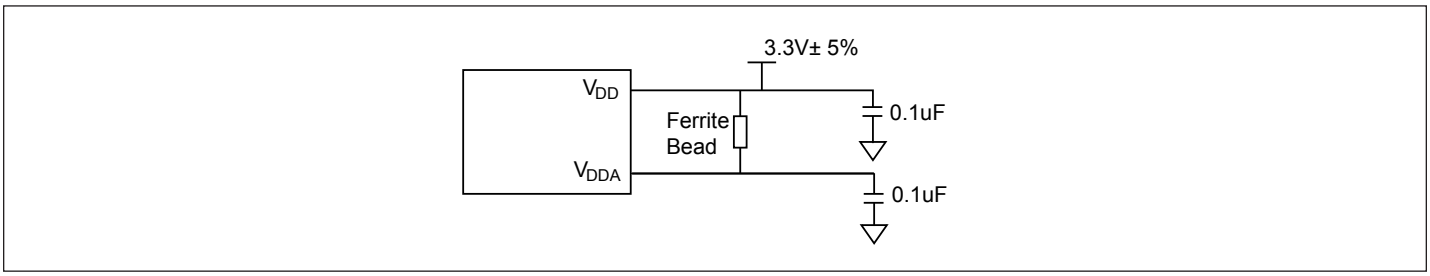


Figure 12. Power Supply Filter

SMBus Serial Data Interface

PI6CG330440 is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

SMBus Address Selection Table

SMB_ADR1_tri	SMB_ADR0_tri	SMBus Address
L	L	D2
L	M	D4
L	H	D6
M	L	B2
M	M	B4
M	H	B6
H	L	BA
H	M	BC
H	H	BE

How to Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	.....	Data Byte (N+X-1)	Ack	Stop bit

How to Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

	8 bits	1 bit	1 bit
.....	Data Byte (N+X-1)	NAck	Stop bit

Byte 0: Output Enable Register 0

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	OE_MXCK8	Output Enable for MXCK8	RW	1	Disabled	Enabled
6	OE_100M6	Output Enable for 100M6	RW	1	Disabled	Enabled
5	OE_100M5	Output Enable for 100M5	RW	1	Disabled	Enabled
4	OE_100M4	Output Enable for 100M4	RW	1	Disabled	Enabled
3	OE_100M3	Output Enable for 100M3	RW	1	Disabled	Enabled
2	OE_100M2	Output Enable for 100M2	RW	1	Disabled	Enabled
1	OE_100M1	Output Enable for 100M1	RW	1	Disabled	Enabled
0	OE_100M0	Output Enable for 100M0	RW	1	Disabled	Enabled

Byte 1: Output Enable Register 1

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	OE_MXCK7	Output Enable for MXCK7	RW	1	Disabled	Enabled
6	OE_MXCK6	Output Enable for MXCK6	RW	1	Disabled	Enabled
5	OE_MXCK5	Output Enable for MXCK5	RW	1	Disabled	Enabled
4	OE_MXCK4	Output Enable for MXCK4	RW	1	Disabled	Enabled
3	OE_MXCK3	Output Enable for MXCK3	RW	1	Disabled	Enabled
2	OE_MXCK2	Output Enable for MXCK2	RW	1	Disabled	Enabled
1	OE_MXCK1	Output Enable for MXCK1	RW	1	Disabled	Enabled
0	OE_MXCK0	Output Enable for MXCK0	RW	1	Disabled	Enabled

Byte 2: Output Enable Register 2

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	MXCK_SEL	MXCK[8:0] Frequency Select	RW	0	100MHz	25MHz
6	MXCK_SEL Control (1)	MXCK[8:0] Select control	RW	0	Pin control	Register control
5	MXCK_SEL_RB	Readback of latched MXCK_SEL pin at PWRGD	R	Latched	100MHz Selected	25 MHz Selected
4	Reserved	Reserved		0	-	-
3	OE_PFT_OUT	Output Enable for PFT_OUT	RW	1	Disabled	Enabled
2	OE_25M2	Output Enable for 25M2	RW	1	Disabled	Enabled
1	OE_25M1	Output Enable for 25M1	RW	1	Disabled	Enabled
0	OE_25M0	Output Enable for 25M0	RW	1	Disabled	Enabled

Note: If MXCK_SEL Control (bit 6) is set to '0' (default), MXCK[8:0] outputs are controlled with MXCK_SEL_100 pin. If MXCK_SEL Control (bit 6) is set to '1' then MXCK[8:0] outputs are controlled with MXCK_SEL bit (bit 7).

Byte 3: PFT Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	PFT_LOST#_RB	Realtime Readback of PFT_LOST#	R	Realtime	PFT_LOST# Low	PFT_LOST# High
6	Stop_Update	Stop Delta Frequency Update (Byte 4 and 5)	RW	0	Disabled	Enabled
5	Clear_Reg	Clear Delta Frequency Registers (Byte 4 and 5)	RW	0		All bits reset to 0 RW
4	Reserved	Reserved		0		
3	Reserved	Reserved		0		
2	Reserved	Reserved		0		
1	Reserved	Reserved		0		
0	Reserved	Reserved		0		

Note: Prior to reading the delta frequency between PFT_IN and local 25MHz XO (Bytes 4 and 5), user should set bit 6 to prevent the case where one of the PFT Frequency Delta Registers is read before and the other after the internal update. This bit should be cleared after the read has been completed.

Byte 4: PFT Frequency Delta Register 0 (Least Significant Byte)

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	PFT_DF7	PFT – 25 MHz XO bit 7	R	Realtime		
6	PFT_DF6	PFT – 25 MHz XO bit 6	R	Realtime		
5	PFT_DF5	PFT – 25 MHz XO bit 5	R	Realtime		
4	PFT_DF4	PFT – 25 MHz XO bit 4	R	Realtime		
3	PFT_DF3	PFT – 25 MHz XO bit 3	R	Realtime		
2	PFT_DF2	PFT – 25 MHz XO bit 2	R	Realtime		
1	PFT_DF1	PFT – 25 MHz XO bit 1	R	Realtime		
0	PFT_DF0	PFT – 25 MHz XO bit 0	R	Realtime		

Note: Byte 4 and 5 contain frequency difference between the PFT clock and the local 25MHz reference in two's complement format with resolution (step size) of 1ns × (25MHz / 215) = 0.763 ppm. Byte 4 contains the least significant byte.

Byte 5: PFT Frequency Delta Register 1 (Most Significant Byte)

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	PFT_SIGN	PFT – Sign Bit	R	Realtime	Positive	Negative
6	PFT_DF14	PFT – 25 MHz XO bit 14	R	Realtime		
5	PFT_DF13	PFT – 25 MHz XO bit 13	R	Realtime		
4	PFT_DF12	PFT – 25 MHz XO bit 12	R	Realtime		
3	PFT_DF11	PFT – 25 MHz XO bit 11	R	Realtime		
2	PFT_DF10	PFT – 25 MHz XO bit 10	R	Realtime		
1	PFT_DF9	PFT – 25 MHz XO bit 9	R	Realtime		
0	PFT_DF8	PFT – 25 MHz XO bit 8	R	Realtime		

Note: Byte 4 and 5 contain frequency difference between the PFT clock and the local 25MHz reference in two's complement format with resolution (step size) of 1ns × (25MHz / 215) = 0.763 ppm. Byte 5 contains the most significant byte.

Byte 6: SSC PLL Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved	Reserved		Reserved		
6	Reserved	Reserved		Reserved		
5	SSC_ENABLE_RB	Readback of SSC_ENABLE pin for 100M[6:0] and MXCK[8:0] if MXCK_SEL is low	R	Realtime	Bit[1:0]: SSC State 00: SSC Off 01: SSC = -0.3% 10: Reserved 11: SSC = -0.5%	
4			R	Realtime		
3	SSC PLL Input Source	SSC source for 100M[6:0] and MXCK[8:0] if MXCK_SEL is low	RW	0	Xtal	Filter PLL(1)
2	SSC Pin Control	SSC control for 100M[6:0] and MXCK[8:0] if MXCK_SEL is low	RW	0	Enabled	Disabled
1	SSC_SEL	100M[6:0] and MXCK[8:0] if MXCK_SEL is low	RW	Latch SSC pin on power-up	Bit[1:0]: SSC State 00: SSC Off 01: SSC = -0.3% 10: Reserved 11: SSC = -0.5%	
0		100M[6:0] and MXCK[8:0] if MXCK_SEL is low	RW	Latch SSC pin on power-up		

Note: 1. When "SSC PLL Input Source" selects "Filter PLL" option, there's no guarantee the outputs will be synchronized.

Byte 7: OE# Pin Realtime Readback Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved	0	R	0		
6	OE_6#_RB	Realtime Readback of OE_6# pin	R	Realtime	OE_6# Low	OE_6# High
5	OE_5#_RB	Realtime Readback of OE_5# pin	R	Realtime	OE_5# Low	OE_5# High
4	OE_4#_RB	Realtime Readback of OE_4# pin	R	Realtime	OE_4# Low	OE_4# High
3	OE_3#_RB	Realtime Readback of OE_3# pin	R	Realtime	OE_3# Low	OE_3# High
2	OE_2#_RB	Realtime Readback of OE_2# pin	R	Realtime	OE_2# Low	OE_2# High
1	OE_1#_RB	Realtime Readback of OE_1# pin	R	Realtime	OE_1# Low	OE_1# High
0	OE_0#_RB	Realtime Readback of OE_0# pin	R	Realtime	OE_0# Low	OE_0# High

Byte 8: Vendor/Revision Identification Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Revision Code Bit 3	Die Revision	R	0		
6	Revision Code Bit 2		R	0		
5	Revision Code Bit 1		R	0		
4	Revision Code Bit 0		R	0		
3	Vendor ID Bit 3	Diodes/Pericom ID: 0011	R	0		
2	Vendor ID Bit 2		R	0		
1	Vendor ID Bit 1		R	1		
0	Vendor ID Bit 0		R	1		

Byte 9: Device ID Control Register

Bit	Control Function	Description	Type	Power-up Condition	0	1
7	DTYPE1	Device type	R	0	'00' = CG, '01' = ZDB,	
6	DTYPE0		R	0	'10' = Reserve, '11' = NZDB	
5	DID5	Device ID	R	0	000111 binary, 07Hex	
4	DID4		R	0		
3	DID3		R	0		
2	DID2		R	1		
1	DID1		R	1		
0	DID0		R	1		

Byte 10: Byte Count Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	BC5	Writing to these registers configures how many bytes will be read back	RW	0		
4	BC4		RW	0		
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		

Byte 11: Side-Band Interface Mask Register 0

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Mask_MXCK8	SBI Mask for MXCK8	RW	0	Off	On
6	Mask_100M6	SBI Mask for 100M6	RW	0	Off	On
5	Mask_100M5	SBI Mask for 100M5	RW	0	Off	On
4	Mask_100M4	SBI Mask for 100M4	RW	0	Off	On
3	Mask_100M3	SBI Mask for 100M3	RW	0	Off	On
2	Mask_100M2	SBI Mask for 100M2	RW	0	Off	On
1	Mask_100M1	SBI Mask for 100M1	RW	0	Off	On
0	Mask_100M0	SBI Mask for 100M0	RW	0	Off	On

Note: If '0', the Side-Band Interface register may disable the output. If '1', the Side-Band Interface cannot disable the output. Such an output may only be disabled by the respective SMBus bit, or OE# pin (present only for 100M outputs).

Byte 12: Side-Band Interface Mask Register 1

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Mask_MXCK7	SBI Mask for MXCK7	RW	0	Off	On
6	Mask_MXCK6	SBI Mask for MXCK6	RW	0	Off	On
5	Mask_MXCK5	SBI Mask for MXCK5	RW	0	Off	On
4	Mask_MXCK4	SBI Mask for MXCK4	RW	0	Off	On
3	Mask_MXCK3	SBI Mask for MXCK3	RW	0	Off	On
2	Mask_MXCK2	SBI Mask for MXCK2	RW	0	Off	On
1	Mask_MXCK1	SBI Mask for MXCK1	RW	0	Off	On
0	Mask_MXCK0	SBI Mask for MXCK0	RW	0	Off	On

Note: If '0', the Side-Band Interface register may disable the output. If '1', the Side-Band Interface cannot disable the output. Such an output may only be disabled by the respective SMBus bit.

Byte 13: Side-Band Interface Mask Register 2

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	Reserved			0		
3	Mask_PFT_OUT	SBI Mask for PFT_OUT	RW	0	Off	On
2	Mask_25M2	SBI Mask for 25M2	RW	0	Off	On
1	Mask_25M1	SBI Mask for 25M1	RW	0	Off	On
0	Mask_25M0	SBI Mask for 25M0	RW	0	Off	On

Note: If '0', the Side-Band Interface register may disable the output. If '1', the Side-Band Interface cannot disable the output. Such an output may only be disabled by the respective SMBus bit.

Byte 14: Side-Band Interface Readback Register 0

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	MXCK8_RB	SBI Readback MXCK8	R	1	Disabled	Enabled
6	100M6_RB	SBI Readback 100M6	R	1	Disabled	Enabled
5	100M5_RB	SBI Readback 100M5	R	1	Disabled	Enabled
4	100M4_RB	SBI Readback 100M4	R	1	Disabled	Enabled
3	100M3_RB	SBI Readback 100M3	R	1	Disabled	Enabled
2	100M2_RB	SBI Readback 100M2	R	1	Disabled	Enabled
1	100M1_RB	SBI Readback 100M1	R	1	Disabled	Enabled
0	100M0_RB	SBI Readback 100M0	R	1	Disabled	Enabled

Note: If the Side-Band interface is used, this register latches the content of the shift register. A '0' indicates that the corresponding differential output is disabled unless the bit has been masked off in SBI Mask register. A '1' indicates that the output is enabled if the corresponding SMBus OE bit is set high and OE# pin (present only for 100M outputs) is pulled low.

Byte 15: Side-Band Interface Readback Register 1

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	MXCK7_RB	SBI Readback MXCK7	R	1	Disabled	Enabled
6	MXCK6_RB	SBI Readback MXCK6	R	1	Disabled	Enabled
5	MXCK5_RB	SBI Readback MXCK5	R	1	Disabled	Enabled
4	MXCK4_RB	SBI Readback MXCK4	R	1	Disabled	Enabled
3	MXCK3_RB	SBI Readback MXCK3	R	1	Disabled	Enabled
2	MXCK2_RB	SBI Readback MXCK2	R	1	Disabled	Enabled
1	MXCK1_RB	SBI Readback MXCK1	R	1	Disabled	Enabled
0	MXCK0_RB	SBI Readback MXCK0	R	1	Disabled	Enabled

Note: If '0', the Side-Band Interface register may disable the output. If '1', the Side-Band Interface cannot disable the output. Such an output may only be disabled by the respective SMBus bit

Byte 16: Side-Band Interface Readback Register 2

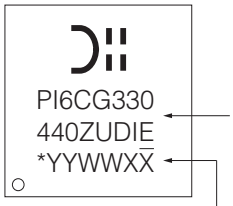
Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	Reserved			0		
3	PFT_OUT_RB	SBI Readback PFT_OUT	R	1	Disabled	Enabled
2	25M2_RB	SBI Readback 25M2	R	1	Disabled	Enabled
1	25M1_RB	SBI Readback 25M1	R	1	Disabled	Enabled
0	25M0_RB	SBI Readback 25M0	R	1	Disabled	Enabled

Note: If the Side-Band interface is used, this register latches the content of the shift register. A '0' indicates that the corresponding differential output is disabled unless the bit has been masked off in SBI Mask register. A '1' indicates that the output is enabled if the corresponding SMBus OE bit is set high and OE# pin (present only for 100M outputs) is pulled low.

Byte 49: PFT Function Bypass Mode

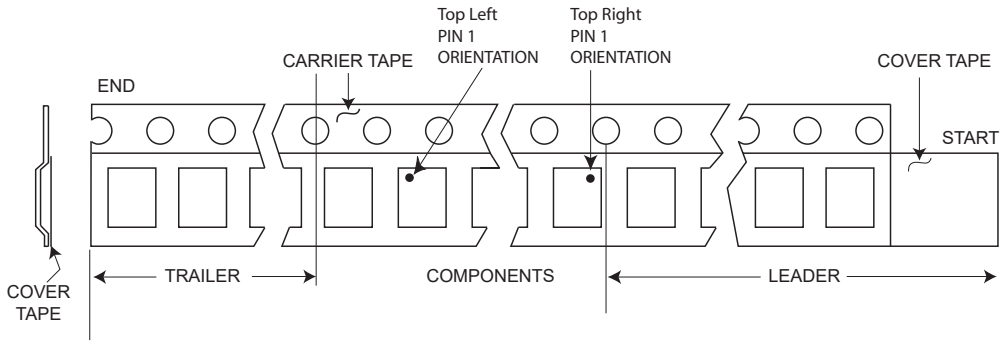
Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			1		
6	Reserved			0		
5	Reserved			0		
4	Reserved			1		
3	Reserved			0		
2	Reserved			1		
1	Reserved			0		
0	PFT function bypass		R/W	0	Normal mode	PFT Bypass mode

Part Marking



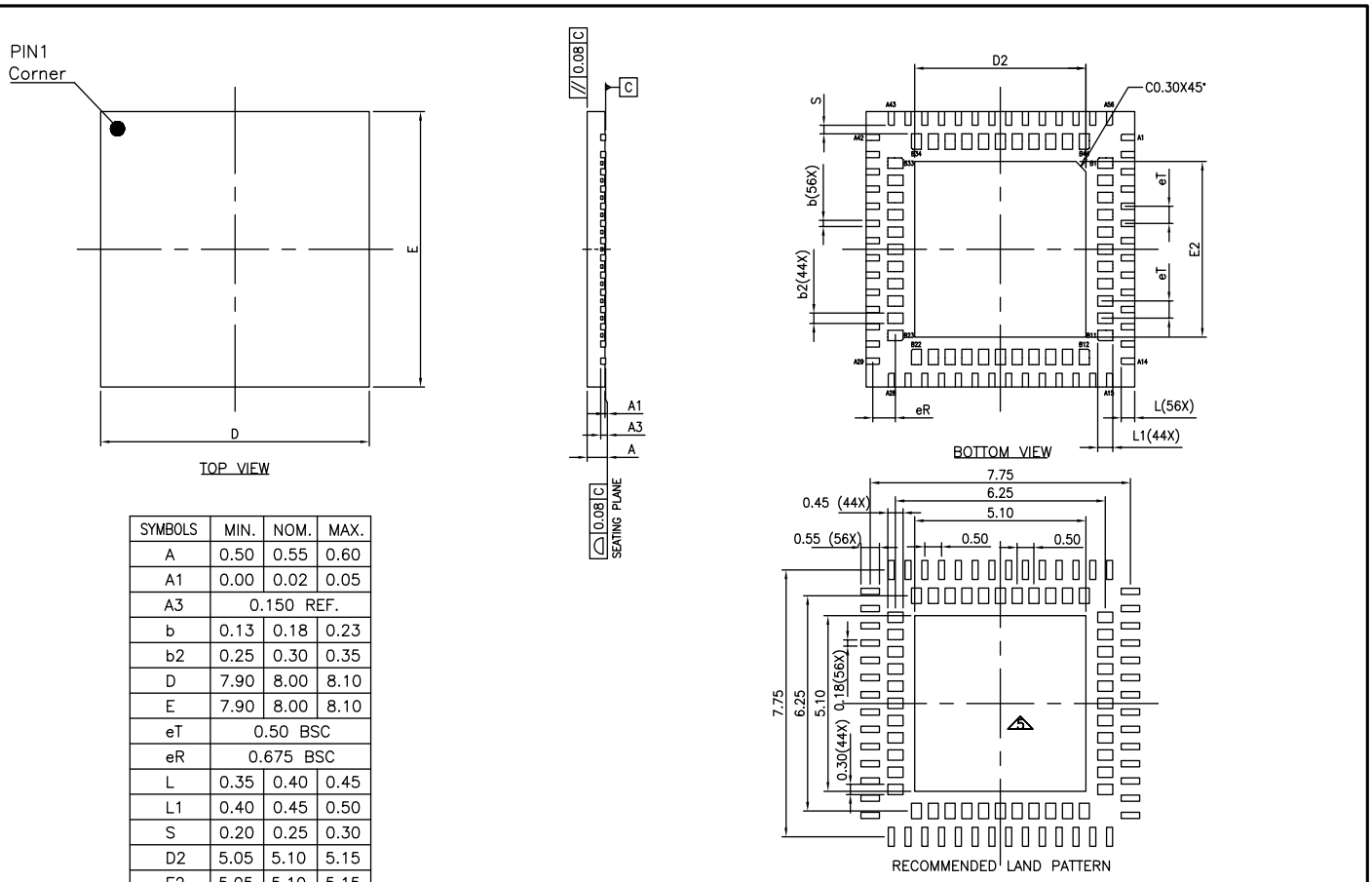
*: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code
Note: Date Code per MA-1251

Package Information



Packaging Mechanical

100-UQFN (ZUD)



SYMBOLS	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.150 REF.	
b	0.13	0.18	0.23
b2	0.25	0.30	0.35
D	7.90	8.00	8.10
E	7.90	8.00	8.10
eT		0.50 BSC	
eR		0.675 BSC	
L	0.35	0.40	0.45
L1	0.40	0.45	0.50
S	0.20	0.25	0.30
D2	5.05	5.10	5.15
E2	5.05	5.10	5.15

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-288
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

DATE: 07/27/21

DESCRIPTION: U-QFN8080-100

PACKAGE CODE: ZUD (ZUD100)

DOCUMENT CONTROL #: PD-2262 REVISION: B

21-1412

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description	Pin 1 Orientation
PI6CG330440ZUDIEX	ZUD	100-Contact, Ultra Thin Quad Flat No-Lead (UQFN)	Top Right Corner
PI6CG330440ZUDIEX-13R	ZUD	100-Contact, Ultra Thin Quad Flat No-Lead (UQFN)	Top Left Corner

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel
7. For packaging detail, go to our website at: https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf

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