THE DATASHEET OF

MG51FB9AE

www.win-source.net 0086-755-83957316

1T 8051

8-bit Microcontroller

NuMicro® Family
MS51 16K Series
Datasheet

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1 GENERAL DESCRIPTION

The MS51 is an embedded flash type, 8-bit high performance 1T 8051-based microcontroller. The instruction set is fully compatible with the standard 80C51 and performance enhanced.

The MS51 contains a up to 16K Bytes of main Flash called APROM, in which the contents of User Code resides. The MS51 Flash supports In-Application-Programming (IAP) function, which enables on-chip firmware updates. IAP also makes it possible to configure any block of User Code array to be used as non-volatile data storage, which is written by IAP and read by IAP or MOVC instruction, this function means whole 16K Bytes area all can be use as Data Flash through IAP command. MS51 support an function of configurationable Flash from APROM called LDROM, in which the Boot Code normally resides for carrying out In-System-Programming (ISP). The LDROM size is configurable with a maximum of 4K Bytes by CONFIG define. There is an additional include special 128 bytes security protection memory (SPROM) to enhance the security and protection of customer application. To facilitate programming and verification, the Flash allows to be programmed and read electronically by parallel Writer or In-Circuit-Programming (ICP). Once the code is confirmed, user can lock the code for security.

The MS51 provides rich peripherals including 256 Bytes of SRAM, 1K Bytes of auxiliary RAM (XRAM), Up to 18 general purpose I/O, two 16-bit Timers/Counters 0/1, one 16-bit Timer2 with three-channel input capture module, one Watchdog Timer (WDT), one Self Wake-up Timer (WKT), one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UARTs with frame error detection and automatic address recognition, one SPI, one I^2C, five enhanced PWM output channels, eight-channel shared pin interrupt for all I/O, and one 12-bit ADC. The peripherals are equipped with 18 sources with 4-level-priority interrupts capability.

The MS51 is equipped with three clock sources and supports switching on-the-fly via software. The three clock sources include external clock input, 10 kHz internal oscillator, and one 16 MHz internal precise oscillator that is factory trimmed to ±1% at room temperature. The MS51 provides additional power monitoring detection such as power-on reset and 4-level brown-out detection, which stabilizes the power-on/off sequence for a high reliability system design.

The MS51 microcontroller operation consumes a very low power with two economic power modes to reduce power consumption — Idle and Power-down mode, which are software selectable. Idle mode turns off the CPU clock but allows continuing peripheral operation. Power-down mode stops the whole system clock for minimum power consumption. The system clock of the MS51 can also be slowed down by software clock divider, which allows for a flexibility between execution performance and power consumption.

With high performance CPU core and rich well-designed peripherals, the MS51 benefits to meet a general purpose, home appliances, or motor control system accomplishment.

2 FEATURES

- CPU:
  - Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller.
  - Instruction set fully compatible with MCS-51.
  - 4-priority-level interrupts capability.
  - Dual Data Pointers (DPTRs).
- Operating:
  - Wide supply voltage from 2.4V to 5.5V.
  - Wide operating frequency up to 24 MHz.
  - Industrial temperature grade: -40℃ to +105℃.
- Memory:
  - Up to 16K Bytes of APROM for User Code.
  - 4/3/2/1 Kbytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP)
  - Flash Memory accumulated with pages of 128 Bytes from APROM by In-Application-Programmable (IAP) means whole APROM can be use as Data Flash
  - An additional 128 bytes security protection memory SPROM
  - Code lock for security by CONFIG
  - 256 Bytes on-chip RAM.
  - Additional 1K Bytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction.
- Clock sources:
  - Default16 MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25 ℃, 5 V), ±2% in all conditions.
  - Selectable 24MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25 ℃, 5 V), ±2% in all conditions.
  - 10 kHz low-speed internal oscillator (LIRC) calibrating to ±1% by software from high-speed internal oscillator.
  - On-the-fly clock source switch via software.
  - Programmable system clock divider from 1/2, 1/4, 1/6, 1/8…, up to 1/512.
- Peripherals:
  - Up to 17 GPIO pins and 1 input-only pin. All output pins have individual 2-level slew rate control.

- Standard interrupt pins $\overline{INT0}$ and $\overline{INT1}$.
- Eight channels of pin interrupt, shared for all I/O ports, with variable configuration of edge/level detection.
- Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051.
- One 16-bit Timer 2 with three-channel input capture module and 9 input pin can be selected.
- One 16-bit auto-reload Timer 3, which can be the baud rate clock source of UARTs.
- Three pairs, six channels of pulse width modulator (PWM) output, 10 output pins can be selected., up to 16-bit resolution, with different modes and Fault Brake function for motor control.PWM counter individual interrupt for timer.
- One programmable Watchdog Timer (WDT) with reset options
- One dedicated Self Wake-up Timer (WKT) for self-timed wake-up for power reduced modes.
- Two full-duplex UART ports with frame error detection and automatic address recognition. TXD and RXD pins of UART0 exchangeable via software.
- One SPI port with master and slave modes, up to 8 Mbps when system clock is 16 MHz.
- One I^2C bus with master and slave modes, up to 400 kbps data rate.
- One 12-bit ADC, up to 500 ksps converting rate, hardware triggered and conversion result compare facilitating motor control.

- Power management:
  - Two power reduced modes: Idle and Power-down mode.
- Power monitor:
  - Brown-out detection (BOD) with low power mode available, 4-level selection, interrupt or reset options.
  - Power-on reset (POR).
  - Low voltage reset (LVR).
- Strong ESD and EFT immunity.
  - ESD HBM pass 8 kV
  - EFT > ± 4.4 kV
  - Latch-up pass 150 mA
- Development Tools:
  - Nuvoton Nu-Link with KEIL™ and IAR development environment.
  - Nuvoton In-Circuit-Programmer (Nu-Link).
  - Nuvoton In-System-Programming (ISP) via UART.

3 BLOCK DIAGRAM

3.1 MS51 16K Series BLOCK DIAGRAM

Figure 3.1-1 Functional Block Diagramshows the MS51 functional block diagram and gives the outline of the device. User can find all the peripheral functions of the device in the diagram.

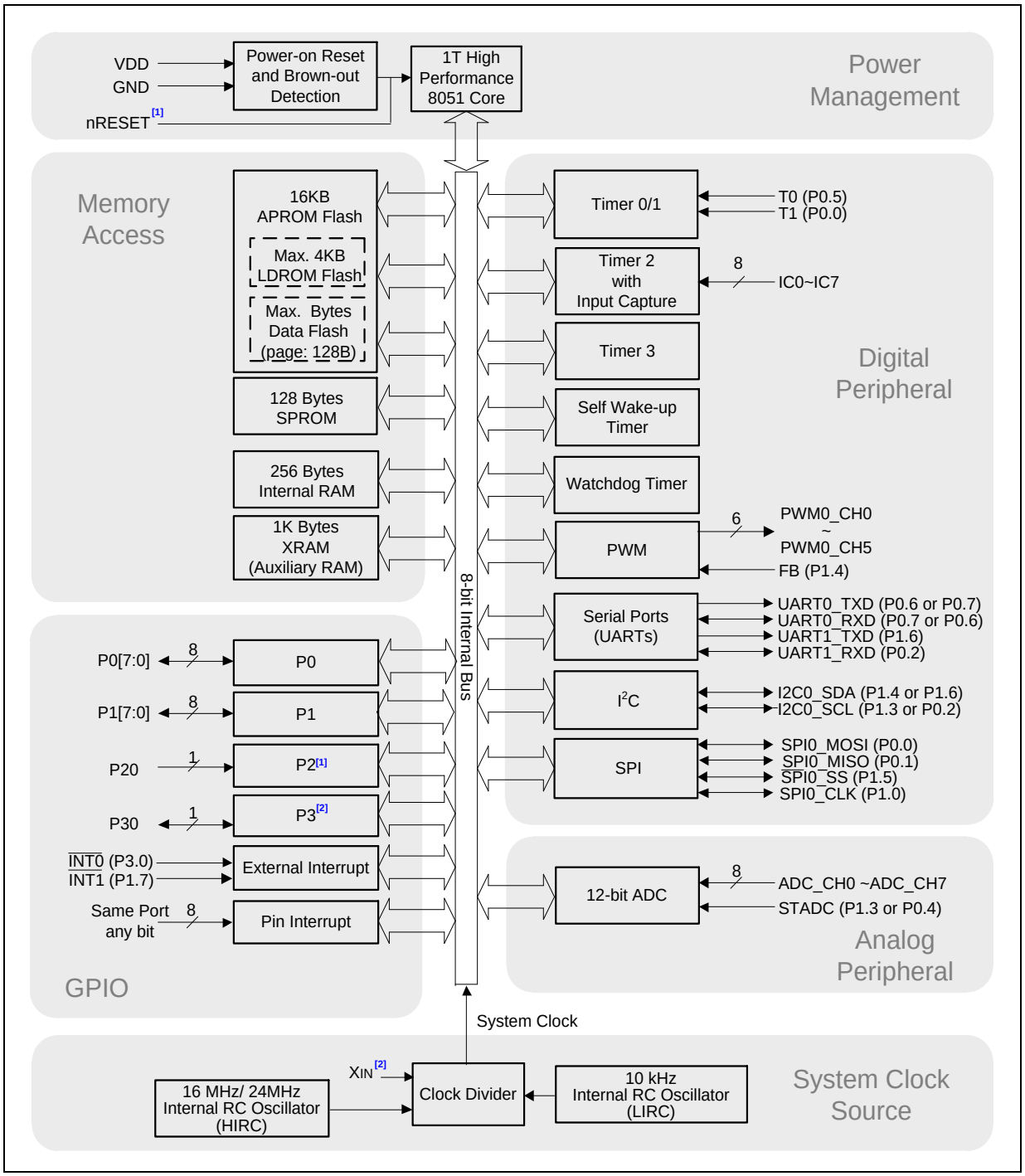


Figure 3.1-1 Functional Block Diagram

4 PARTS INFORMATION

4.1 MS51 Series selection gude

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB) [1]	I/O	Timer/	PWM	Connectivity				ADC(12-Bit)	Package
							ISO-7816 [2]	UART	SPI	I2C		
MS51BA9AE	8	1	4	8	4	5	-	2	1	1	5-ch	MSOP10
MS51DA9AE	8	1	4	12	4	5	-	2	1	1	7-ch	TSSOP14
MS51XB9AE	16	1	4	18	4	6	-	2	1	1	8-ch	QFN20 [3]
MS51XB9BE	16	1	4	18	4	6	-	2	1	1	8-ch	QFN20 [3]
MS51FB9AE	16	1	4	18	4	6	-	2	1	1	8-ch	TSSOP20
MS51FC0AE	32	2	4	18	4	8	3	2	1	1	10-ch	TSSOP20
MS51XC0AE	32	2	4	18	4	8	3	2	1	1	10-ch	QFN20
MS51EC0AE	32	2	4	26	4	10	3	2	1	1	15-ch	TSSOP28
MS51TC0AE	32	2	4	30	4	12	3	2	2	1	15-ch	QFN33
MS51PC0AE	32	2	4	30	4	12	3	2	2	1	15-ch	LQFP32

Note:

1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM.
2. ISO-7816 configurable as UART2.
3. Detailed package information please refer to Chapter 7
4. This Datasheet only for 16K flash size part number product

4.2 MS51 Series Selection Code

MS	51	F	B	9	A	E
Core	Line	Package	Flash	SRAM	Reserve	Temperature
1T 8051	51: Base	B: MSOP10 (3x3 mm) D: TSSOP14 (4.4x5.0 mm) F: TSSOP20 (4.4x6.5 mm) E:TSSOP28 (4.4x9.7 mm) U: SOP28 (300 mil) O: SOP20 (300 mil) T: QFN33 (4x4 mm) P: LQFP32 (7x7 mm) L: LQFP48 (7x7 mm) S: LQFP64 (7x7 mm) K: LQFP128 (14x14 mm)	A: 8 KB B: 16 KB C: 32 KB D: 64 KB E: 128 KB G: 256 KB I: 512 KB	0: 2 KB 1: 4 KB 2: 8/12 KB 3: 16 KB 6: 32 KB 8: 64 KB 9: 1 KB A: 96 KB		E:-40°C ~ 105°C

5 PIN CONFIGURATION

5.1 Pin Configuration

Users can find pin configuaration informations by using NuTool - PinConfigure. The NuTool - PinConfigure contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

5.1.1 MS51 16K Series Multi Function Pin Diagram

5.1.1.1 SOP20 Package

Corresponding Part Number: MS51FB9AE

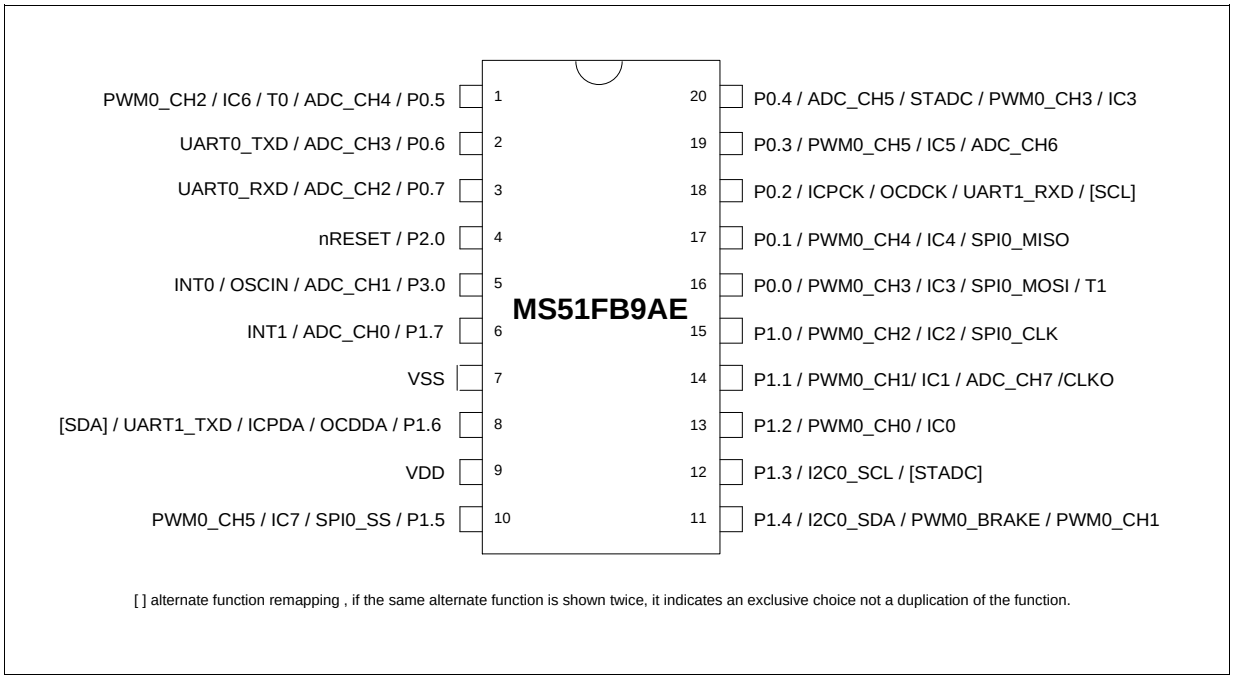


Figure 5.1-1 Pin Assignment of TSSOP-20 Package

5.1.1.2 QFN20 Package

Corresponding Part Number: MS51XB9AE

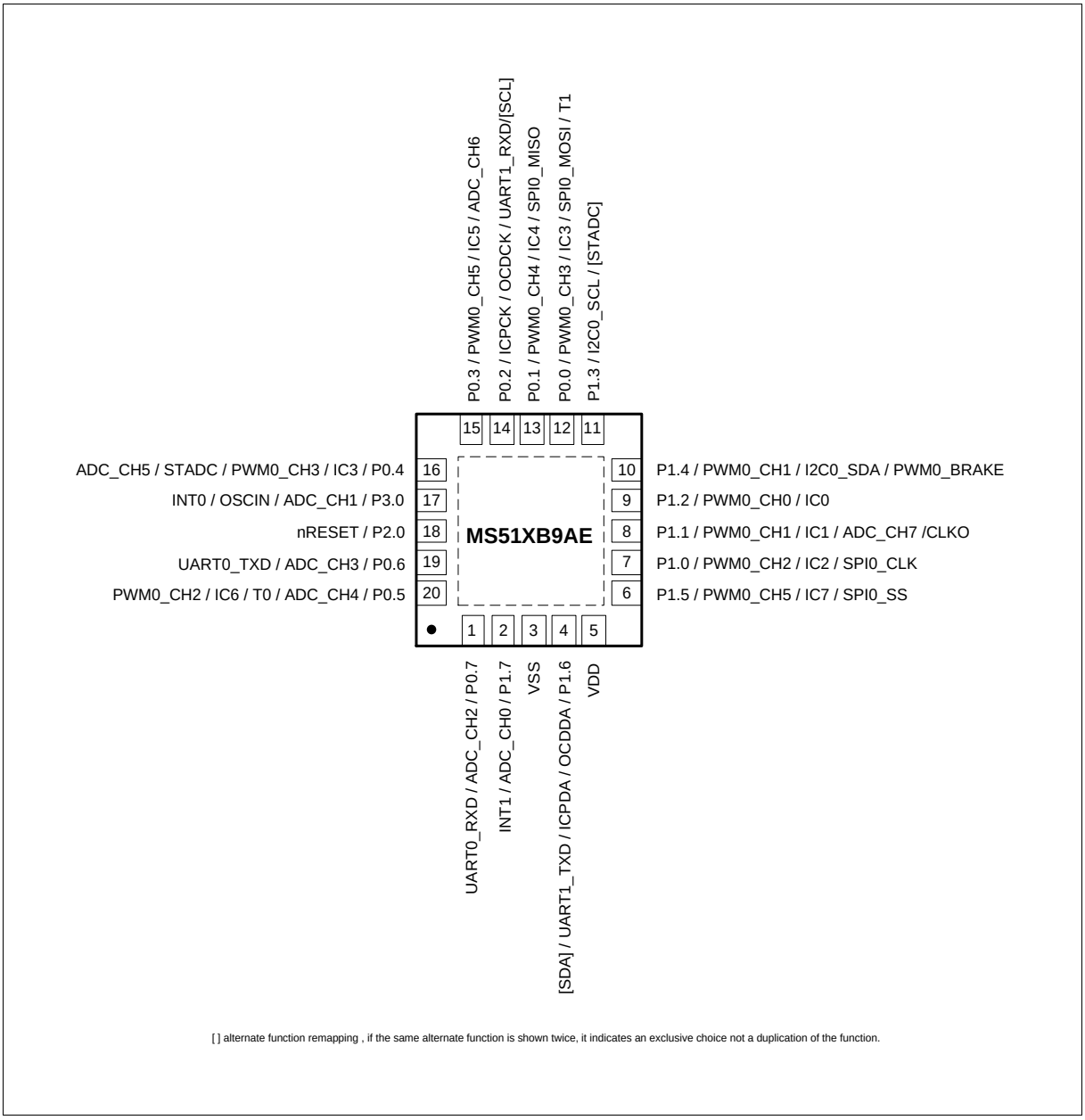


Figure 5.1-2 Pin Assignment of QFN-20 Package

5.1.1.3 QFN20 Package

Corresponding Part Number: MS51XB9BE

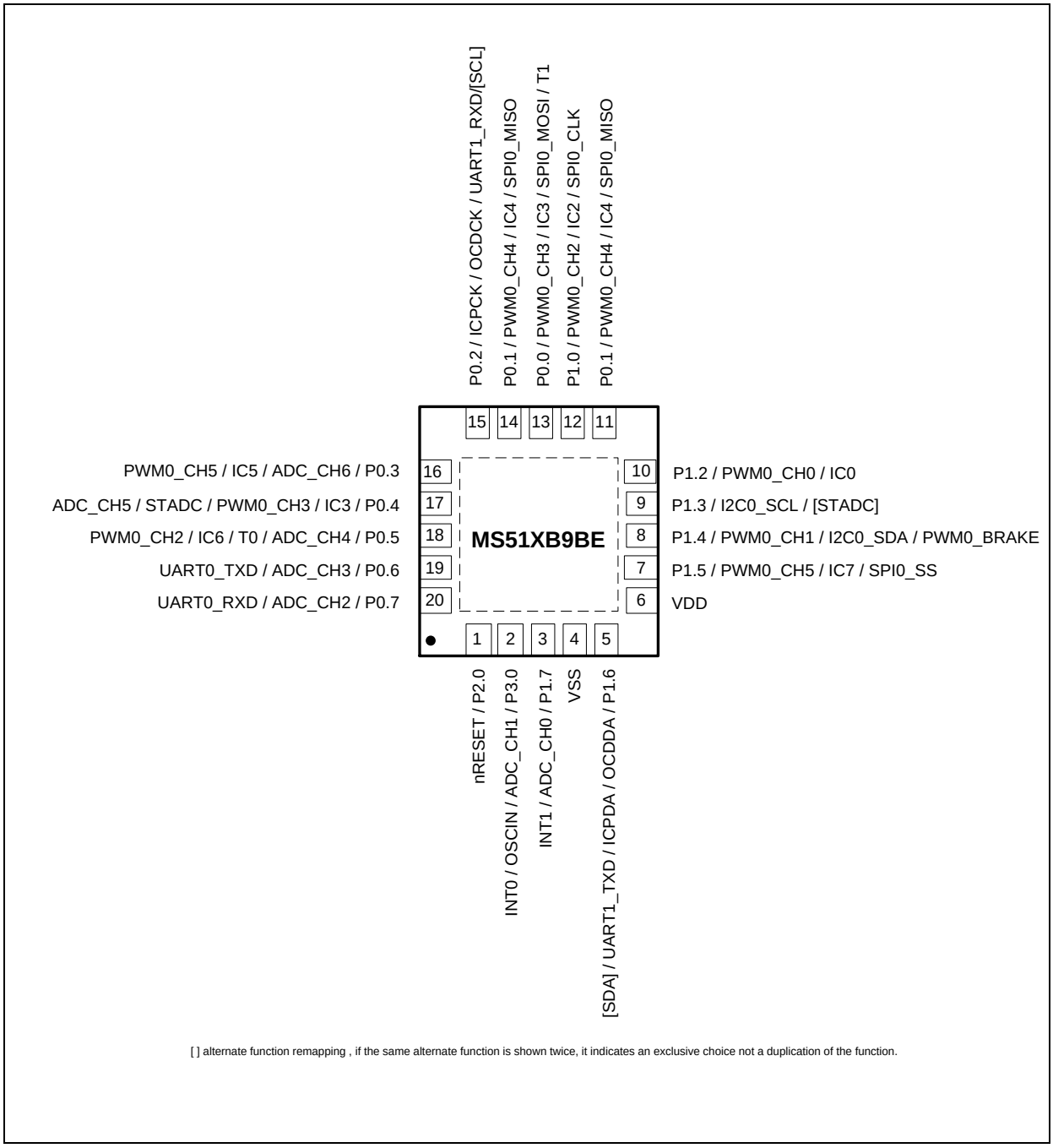


Figure 5.1-3 Pin Assignment of QFN-20 Package

5.2 MS51 16K Series Pin Description

Pin Number			Symbol	Multi-Function Description[1]
MS51FB9AE	MS51XB9AE	MS51XB9AE		
9	5	6	VDD	POWER SUPPLY: Supply voltage VDD for operation.
7	3	4	VSS	GROUND: Ground potential.
16	12	13	P0.0/ PWM0_CH3/ SPI0_MOSI/ IC3/ T1	P0.0: Port 0 bit 0.
				PWM0_CH3: PWM output channel 3.
				SPI0_MOSI: SPI master output/slave input.
				IC3: Input capture channel 3.
				T1: External count input to Timer/Counter 1 or its toggle output.
17	13	14	P0.1/ PWM0_CH4/ IC4/ SPI0_MISO	P0.1: Port 0 bit 1.
				PWM0_CH4: PWM output channel 4.
				IC4: Input capture channel 4.
				SPI0_MISO: SPI master input/slave output.
18	14	15	P0.2/ ICPCK/OCDCK/ UART1_RXD/ [SCL]	P0.2: Port 0 bit 2.
				ICPCK: ICP clock input.
				OCDCK: OCD clock input.
				UART1_RXD: Serial port 1 receive input.
				[SCL] [3]: I2C clock.
19	15	16	P0.3/ PWM0_CH5/ IC5/ ADC_CH6	P0.3: Port 0 bit 3.
				PWM0_CH5: PWM output channel
				IC5: Input capture channel 5.
				ADC_CH6: ADC input channel 6.
20	16	17	P0.4/ PWM0_CH3/ IC3/ ADC_CH5/ STADC	P0.4: Port 0 bit 4.
				PWM0_CH3: PWM output channel 3.
				IC3: Input capture channel 3.
				ADC_CH5: ADC input channel 5.
				STADC: External start ADC trigger
1	20	18	P0.5/ PWM0_CH2/ IC6/ T0/ ADC_CH4	P0.5: Port 0 bit 5.
				PWM0_CH2: PWM output channel 2.
				IC6: Input capture channel 6.
				T0: External count input to Timer/Counter 0 or its toggle output.
				ADC_CH4: ADC input channel 5.
2	19	19	P0.6/	P0.6: Port 0 bit 6.

Pin Number			Symbol	Multi-Function Description[1]
MS51FB9AE	MS51XB9AE	MS51XB9AE		
			UART0_TXD/ ADC_CH3	UART0_TXD [2]: Serial port 0 transmit data output.
				ADC_CH3: ADC input channel 3.
3	1	20	P0.7/ UART0_RXD/ ADC_CH2	P0.7: Port 0 bit 7.
				UART0_RXD: Serial port 0 receive input.
				ADC_CH2: ADC input channel 2.
15	7	12	P1.0/ PWM0_CH2/ IC2/ SPI0_CLK	P1.0: Port 1 bit 0.
				PWM0_CH2: PWM output channel 2.
				IC2: Input capture channel 2.
				SPI0_CLK: SPI clock.
14	8	11	P1.1/ PWM0_CH1/ IC1/ ADC_CH7/ CLKO	P1.1: Port 1 bit 1
				PWM0_CH1: PWM output channel 1.
				IC1: Input capture channel 1.
				ADC_CH7: ADC input channel 7.
				CLKO: System clock output.
13	9	10	P1.2/ PWM0_CH0/ IC0	P1.2: Port 1 bit 2.
				PWM0_CH0: PWM output channel 0.
				IC0: Input capture channel 0.
12	11	9	P1.3/ I2C0_SCL/ [STADC]	P1.3: Port 1 bit 3.
				I2C0_SCL: I2C clock.
				[STADC] [4]: External start ADC trigger
11	10	8	P1.4/ PWM0_CH1/ I2C0_SDA/ PWM0_BRAKE	P1.4: Port 1 bit 4.
				PWM0_CH1: PWM output channel 1.
				I2C0_SDA: I2C data.
				PWM0_BRAKE: Fault Brake input.
10	6	7	P1.5/ PWM0_CH5/ IC7/ SPI0_SS	P1.5: Port 1 bit 5.
				PWM0_CH5: PWM output channel 5.
				IC7: Input capture channel 7.
				SPI0_SS: SPI slave select input.
8	4	5	P1.6/ ICPDA/OCDDA/ UART1_TXD/ [SDA]	P1.6: Port 1 bit 6.
				ICPDA: ICP data input or output.
				OCDAT: OCD data input or output.
				UART1_TXD: Serial port 1 transmit data output.
				[SDA] [3]: I^2C data.

Pin Number			Symbol	Multi-Function Description[1]
MS51FB9AE	MS51XB9AE	MS51XB9AE		
6	2	3	P1.7/ $\overline{INT1}$/ ADC_CH0	P1.7: Port 1 bit 7.
				$\overline{INT1}$: External interrupt 1 input.
				ADC_CH0: ADC input channel 0.
4	18	1	P2.0/ nRESET	P2.0: Port 2 bit 0 input pin available when RPD (CONFIG0.2) is programmed as 0.
				nRESET: nRESET pin is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. nRESETpin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
5	17	12	P3.0/ $\overline{INT0}$/ OSCIN/ ADC_CH1	P3.0: Port 3 bit 0 available when the internal oscillator is used as the system clock.
				$\overline{INT0}$: External interrupt 0 input.
				OSCIN: If the ECLK mode is enabled, Xin is the external clock input pin.
				ADC_CH1: ADC input channel 1.

[1] All I/O pins can be configured as a interrupt pin. This feature is not listed in multi-function description.
[2] UART0_TXD and UART0_RXD pins are software exchangeable by UART0PX (AUXR1.2).
[3] [I2C] alternate function remapping option. I^2C pins is software switched by I2CPX (I2CON.0).
[4] [STADC] alternate function remapping option. STADC pin is software switched by STADCPX(ADCCON1.6).
[5] PIOx register decides which pins are PWM or GPIO.

6 APPLICATION CIRCUIT

6.1 Power supply scheme

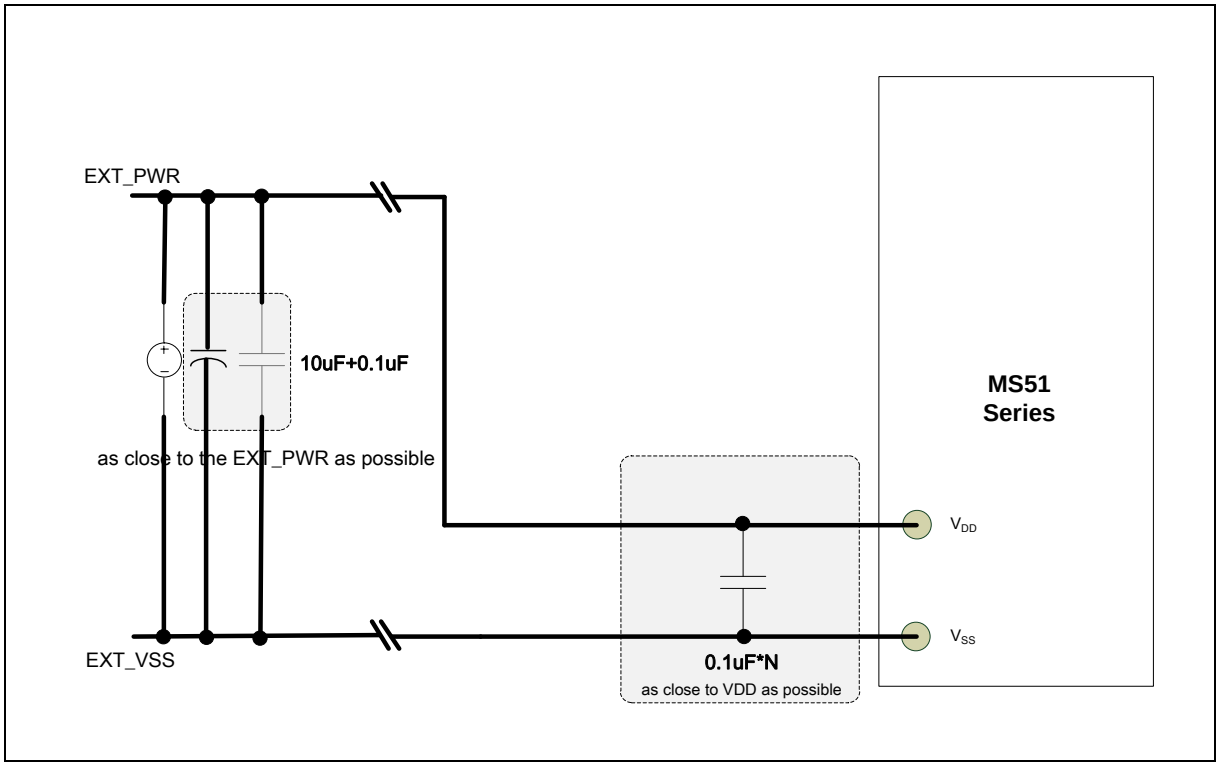


Figure 6.1-1 NuMicro® MS51 Power supply circuit

6.2 Peripheral Application scheme

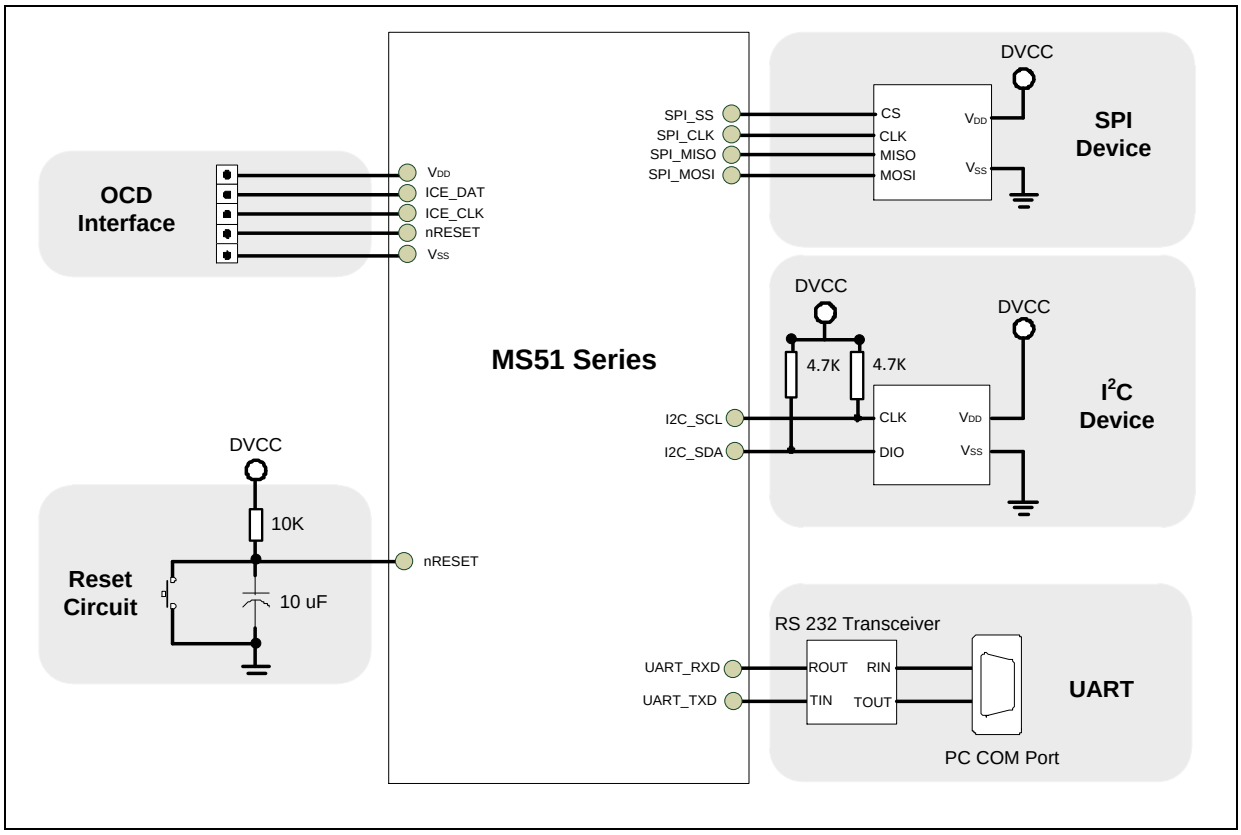


Figure 6.2-1 NuMicro® MS51 Peripheral interface circuit

6.3 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from several register to determine the reset source. Hardware reset sourcces are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset (WDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to SWRST (CHPCON [7])

6.3.1 Hardware Reset Sources

6.3.1.1 Power-On Reset and Low Voltage Reset

The MS51 incorporates an internal power-on reset (POR) and a low voltage reset (LVR). During a power-on process of rising power supply voltage V_{DD}, the POR or LVR will hold the MCU in reset mode when V_{DD} is lower than the voltage reference thresholds. This design makes CPU not access program flash while the V_{DD} is not adequate performing the flash reading. If an undetermined operating code is read from the program flash and executed, this will put CPU and even the whole system in to an erroneous state. After a while, V_{DD} rises above the threshold where the system can work, the selected oscillator will start and then program code will execute from 0000H. At the same time, a power-on flag POF (PCON.4) will be set 1 to indicate a cold reset, a power-on process complete. Note that the contents of internal RAM will be undetermined after a power-on. It is recommended that user gives initial values for the RAM block.

The POF is recommended to be cleared to 0 via software to check if a cold reset or warm reset performed after the next reset occurs. If a cold reset caused by power off and on, POF will be set 1 again. If the reset is a warm reset caused by other reset sources, POF will remain 0. User may take a different course to check other reset flags and deal with the warm reset event. For detailed electrical characteristics, refer to the table 35-7 and 35-8.

PCON – Power Control

7	6	5	4	3	2	1	0
SMOD	SMOD0	LPR	POF	GF1	GF0	PD	IDL
R/W	R/W	RW	R/W	R/W	R/W	R/W	R/W

Address: 87H, All pagessPOR reset value: 0001 000b, other reset value: 000U 0000b

Bit	Name	Description

Bit	Name	Description
4	POF	Power-on reset flag This bit will be set as 1 after a power-on reset. It indicates a cold reset, a power-on reset complete. This bit remains its value after any other resets. This flag is recommended to be cleared via software.

6.3.1.2 nRESET Reset Waveform

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 VDD and the state keeps longer than 32 system clock, chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 VDD and the state keeps longer than 200 us (glitch filter). The POF will be set 1. Figure 6.3-1 nRESET Reset Waveform**錯誤! 找不到參照來源。** shows the nRESET reset waveform.

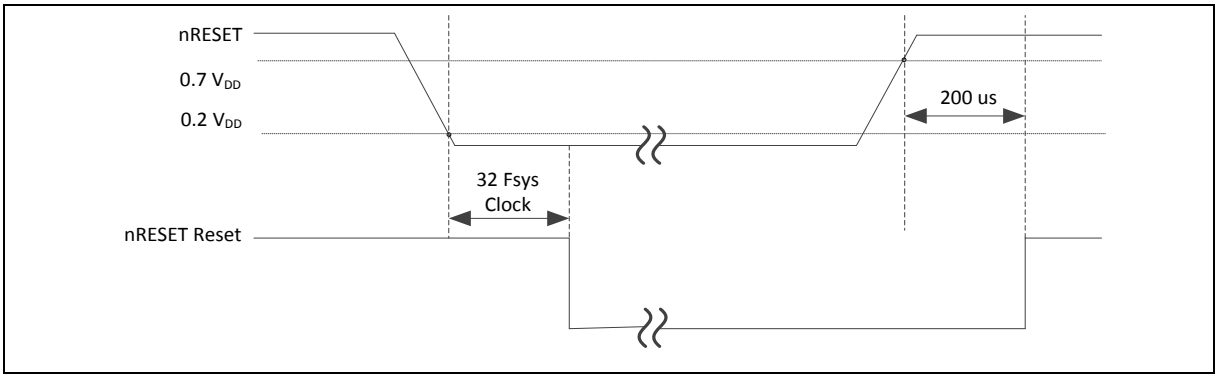


Figure 6.3-1 nRESET Reset Waveform

6.3.1.3 Low Voltage Reset (LVR) Waveform

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.3-4 shows the Low Voltage Reset waveform.

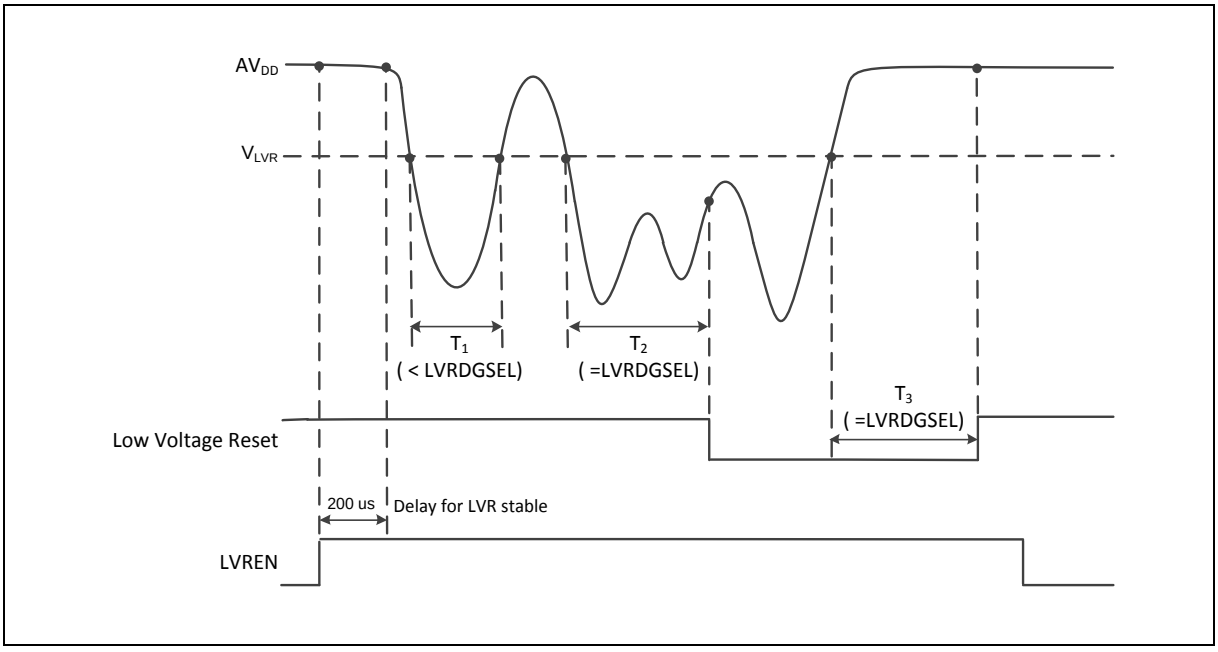


Figure 6.3-2 Low Voltage Reset (LVR) Waveform

6.3.1.4 Brown-Out Reset

The brown-out detection circuit is used for monitoring the V_{DD} level during execution. When V_{DD} drops to the selected brown-out trigger level (V_{BOD}), the brown-out detection logic will reset the MCU if BORST (BODCON0.2) setting 1. After a brown-out reset, BORF (BODCON0.1) will be set as 1 via hardware. BORF will not be altered by any reset other than a power-on reset or brown-out reset itself. This bit can be set or cleared by software.

BODCON0 – Brown-out Detection Control 0 (TA protected)

7	6	5	4	3	2	1	0
BODEN	BOV[2:0]			BOF	BORST	BORF	BOS
R/W	R/W			R/W	R/W	R/W	R

Address: A3H, Page 0 Reset value: POR: CCCC XC0Xb / BOD: UUUU XU1Xb / Others: UUUU XUUXb

Bit	Name	Description
1	BORF	Brown-out reset flag When the MCU is reset by brown-out event, this bit will be set via hardware. This flag is recommended to be cleared via software.

6.3.1.5 External Reset and Hard Fault Reset

The external reset pin nRESET is an input with a Schmitt trigger. An external reset is accomplished by holding the nRESET pin low for at least 24 system clock cycles to ensure detection of a valid hardware reset signal. The reset circuitry then synchronously applies the internal reset signal. Thus, the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain as long as nRESET pin is low. After the nRESET high is removed, the MCU will exit the reset state and begin code executing from address 0000H. If an external reset applies while CPU is in Power-down mode, the way to trigger a hardware reset is slightly different. Since the Power-down mode stops system clock, the reset signal will asynchronously cause the system clock resuming. After the system clock is stable, MCU will enter the reset state.

There is a RSTPINF (AUXR0.6) flag, which indicates an external reset took place. After the external reset, this bit will be set as 1 via hardware. RSTPINF will not change after any reset other than a power-on reset or the external reset itself. This bit can be cleared via software.

Hard Fault reset will occur if CPU fetches instruction address over flash size, HardF (AUXR0.5) flag will be set via hardware. HardF will not change after any reset other than a power-on reset or the external reset itself. This bit can be cleared via software. If MCU run in OCD debug mode and OCDEN = 0, hard fault reset will be disabled. Only HardF flag be asserted.

AUXR0 – Auxiliary Register 0

7	6	5	4	3	2	1	0
SWRF	RSTPINF	HardF	HardFInt	GF2	-	0	DPS
R/W	R/W	R/W	R/W	R/W	-	R	R/W

Address: A2H, Page:0
Reset value: POR: 0000 0000b / Software: 1UU0 0000b / Reset pin: U1U0 0000b / Hard fault: UU10 0000b / Others: UUU0 0000b

Bit	Name	Description
6	RSTPINF	External reset flag When the MCU is reset by the external reset, this bit will be set via hardware. It is recommended that the flag be cleared via software.
5	HardF	Hard Fault reset flag Once CPU fetches instruction address over flash size while EHFI (EIE1.4)=0, MCU will reset and this bit will be set via hardware. It is recommended that the flag be cleared via software. **Note:** If MCU run in OCD debug mode and OCDEN = 0, Hard fault reset will disable. Only HardF flag be asserted.

6.3.1.6 Watchdog Timer Reset

The WDT is a free running timer with programmable time-out intervals and a dedicated internal clock source. User can clear the WDT at any time, causing it to restart the counter. When the selected time-out occurs but no software response taking place for a while, the WDT will reset the system directly and CPU will begin execution from 0000H.

Once a reset due to WDT occurs, the WDT reset flag WDTRF (WDCON.3) will be set. This bit keeps unchanged after any reset other than a power-on reset or WDT reset itself. User can clear WDTRF via software.

WDCON – Watchdog Timer Control (TA protected)

7	6	5	4	3	2	1	0
WDTR	WDCLR	WDTF	WIDPD	WDTRF	WDPS[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W		

Address: AAH, Page 0 Reset value: POR: 0000 0111b / WDT: 0000 1UUUb / Others: 0000 UUUUb

Bit	Name	Description
3	WDTRF	WDT reset flag When the CPU is reset by WDT time-out event, this bit will be set via hardware. This flag is recommended to be cleared via software after reset.

6.3.1.7 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.3-3 shows the power-on reset waveform.

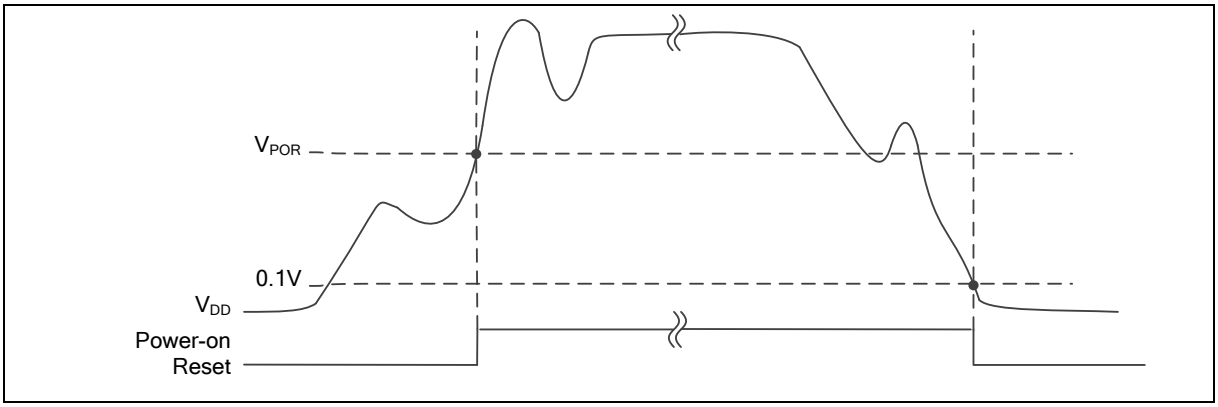


Figure 6.3-3 Power-on Reset (POR) Waveform

6.3.1.8 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.3-4 shows the Low Voltage Reset waveform.

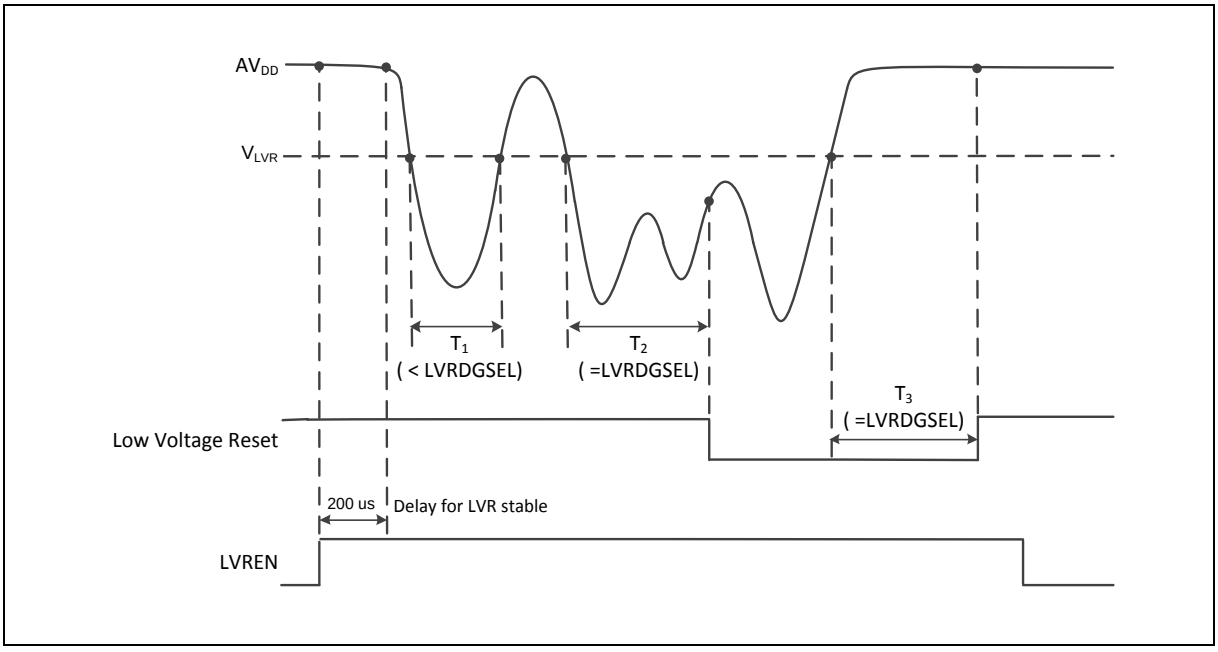


Figure 6.3-4 Low Voltage Reset (LVR) Waveform

6.3.1.9 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.3-5 shows the Brown-out Detector waveform.

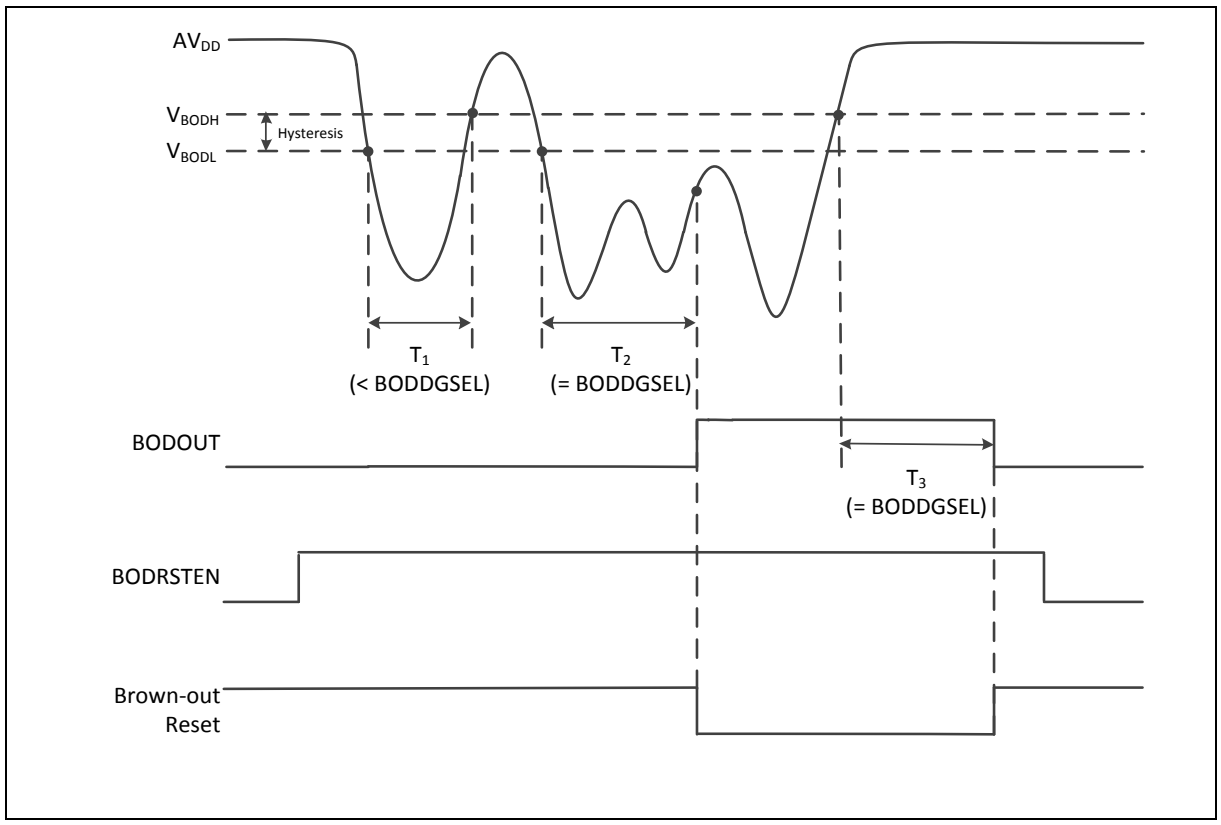


Figure 6.3-5 Brown-out Detector (BOD) Waveform

6.3.1.10 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

7 ELECTRICAL CHARACTERISTICS

7.1 General Operating Conditions

(V_{DD}-V_{SS} = 2.4 ~ 5.5V, T_A = 25°C, Fsys = 16 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operation voltage	2.4	-	5.5	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{BG}	Band-gap voltage[2]	1.17	1.22	1.30		T_A = 25 °C
		1.14		1.33		T_A = -40°C ~105 °C,

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. Based on characterization, tested in production.

Table 7.1-1 General operating conditions

7.2 DC Electrical Characteristics

7.2.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 2.4V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals clock base is the system clock Fsys.
- Program run “while (1);” in Flash.

Symbol	Conditions	Fsys	Typ [6]	Max[6][7]			Unit
			T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	3.6	4.2	4.6	4.8	mA
		24 MHz(HIRC)[1] @3.3V	3.2				
		24 MHz(HIRC)[1] @2.4V	2.9				
		16 MHz (HIRC) [1] @5.5V	3.3	3.4	3.9	4.6	
		16 MHz (HIRC) [1] @3.3V	3.1				
		16 MHz (HIRC) [1] @2.4V	2.8				
		10 kHz (LIRC)[2]	0.30	0.32	0.46	2.33	

Notes:

1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 7.2-1 Current consumption in Normal Run mode

Symbol	Conditions	Fsys	Typ [3]	Max[3][4]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	2.8	2.9	3.2	3.8	mA
		24 MHz(HIRC)[1] @3.3V	2.4				
		24 MHz(HIRC)[1] @2.4V	2.2				
		16 MHz (HIRC)[1] @5.5V	2.2	2.5	2.6	3.2	
		16 MHz (HIRC)[1] @3.3V	1.9				
		16 MHz (HIRC)[1] @2.4V	1.8				
		10 kHz (LIRC)[2]	0.3	0.5	0.9	2.3	

Notes:
1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 7.2-2 Current consumption in Idle mode

Symbol	Test Conditions	Typ[1]	Max[2]			Unit
		T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_PD}	Power down mode, all peripherals disable@5.5V	6.5	6.2	9	55	µA
	Power down mode, all peripherals disable@3.3V	6				
	Power down mode, all peripherals disable@2.4V	5.8				
	Power down mode, LVR enable all other peripherals disable	7.5	6.7	10[3]	57	
	Power down mode, LVR enable BOD enable all other peripherals disable	180	165	197	292	

Notes:
1. AV_{DD} = V_{DD} = 3.3V unless otherwise specified, LVR17 disabled, POR disabled and BOD disabled.
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

Table 7.2-3 Chip Current Consumption in Power down mode

7.2.2 Wakeup Time from Low-Power Modes

Symbol	Parameter		Typ	Max	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode		5	6	cycles
t_{WU_NPD}[2][3]	Wakeup from Power down mode	Fsys = HIRC @16MHz	-	30	µs
		Fsys = HIRC @ 24MHz		30	µs

Notes:

1. Measured on a wakeup phase with a 16 MHz HIRC oscillator.
2. Based on test during characterization, not tested in production.
3. The wakeup times are measured from the wakeup event to the point in which the application code reads the first.

Table 7.2-4 Low-power mode wakeup timings

7.2.3 I/O DC Characteristics

7.2.3.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	0	-	$0.3*V_{DD}$	V	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1		1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1		1		$V_{DD} < V_{IN} < 5.5$ V, Open-drain or input only mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 7.2-5 I/O input characteristics

7.2.3.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2]	Source current for quasi-bidirectional mode and high level	-7.4	-	-7.5	μA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	μA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	μA	V_{DD} = 2.4 V V_{IN} =(V_{DD}-0.4) V
		-57.2	-	-58.3	μA	V_{DD} = 5.5 V V_{IN} = 2.4 V
	Source current for push-pull mode and high level	-9	-	-9.6	mA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-6	-	-6.6	mA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-4.2	-	-4.9	mA	V_{DD} = 2.7 V V_{IN} =(V_{DD}-0.4) V
		-18	-	-20	mA	V_{DD} = 5.5 V V_{IN} = 2.4 V
I_{SK}[1] [2]	Sink current for push-pull mode and low level	18	-	20	mA	V_{DD} = 5.5 V V_{IN} = 0.4 V
		16	-	18	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
		9.7	-	11	mA	V_{DD} = 2.4 V V_{IN} = 0.4 V
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 7.2-6 I/O output characteristics

7.2.3.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	45	-	60	KΩ	V_{DD} = 5.5 V
		45	-	65		V_{DD} = 2.4 V
t_{FR}[1]	nRESET input response time	-	1.5	-	µs	Normal run and Idle mode
		10	-	25		Power down mode

Notes:
1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 7.2-7 nRESET Input Characteristics

7.3 AC Electrical Characteristics

7.3.1 Internal High Speed RC Oscillator (HIRC)

The 16 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	16[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +85 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	μA	
T_S[3]	Stable time	-	3	5	μs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:

1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

Table 7.3-1 16 MHz Internal High Speed RC Oscillator(HIRC) characteristics

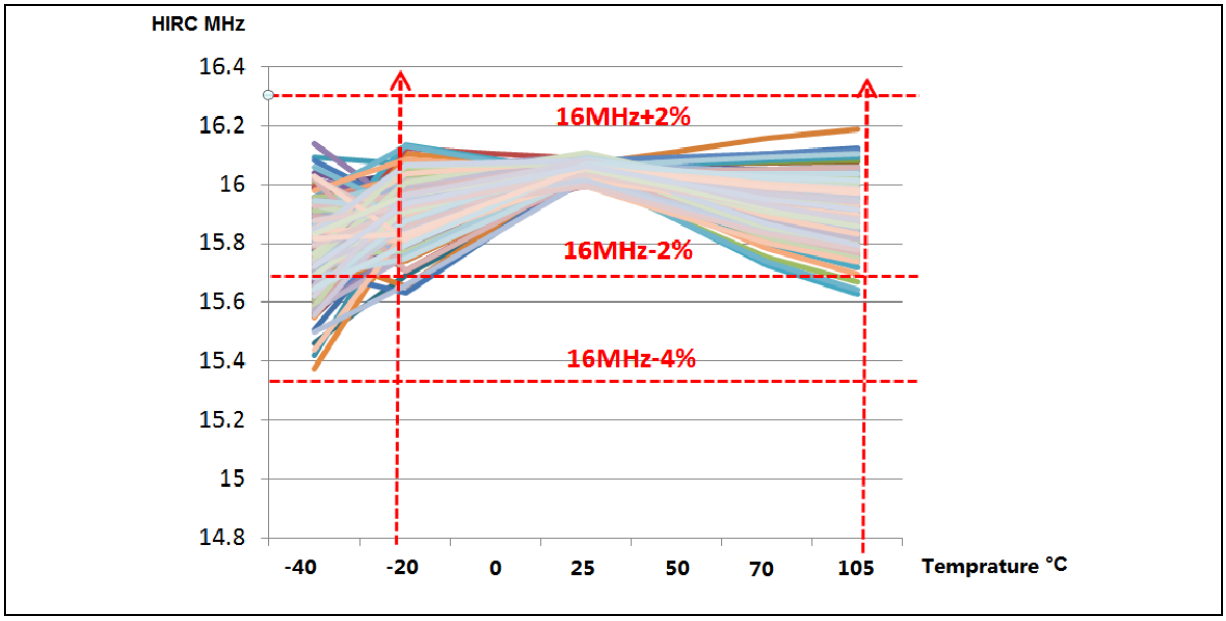


Figure 7.3-1 HIRC 16MHz deviation under V_{DD} = 5.5 V

The 24 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	24[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +85 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:

1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

Table 7.3-2 24MHz Internal High Speed RC Oscillator(HIRC) characteristics

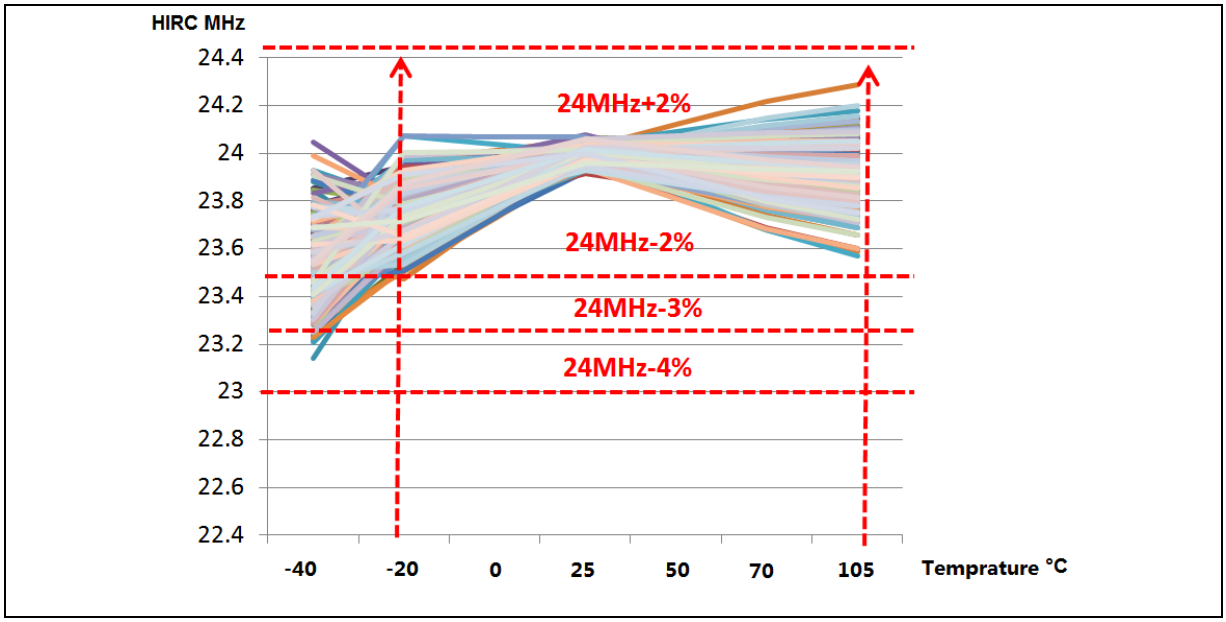


Figure 7.3-2 HIRC 24MHz deviation under V_{DD} = 5.5 V

7.3.2 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{LRC}	Oscillator frequnecy	-	10	-	kHz	
	Frequency drift over temperarure and volatge	-10[1]	-	10[1]	%	T_A = 25 °C, V_{DD} = 5V
		-35[2]	-	35[2]	%	T_A=-40~105°C Without software calibration
I_{LRC}[3]	Operating current	-	0.85	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C

Notes:

1. Guaranteed by characterization, tested in production.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design.

Table 7.3-3 10 kHz Internal Low Speed RC Oscillator(LIRC) characteristics

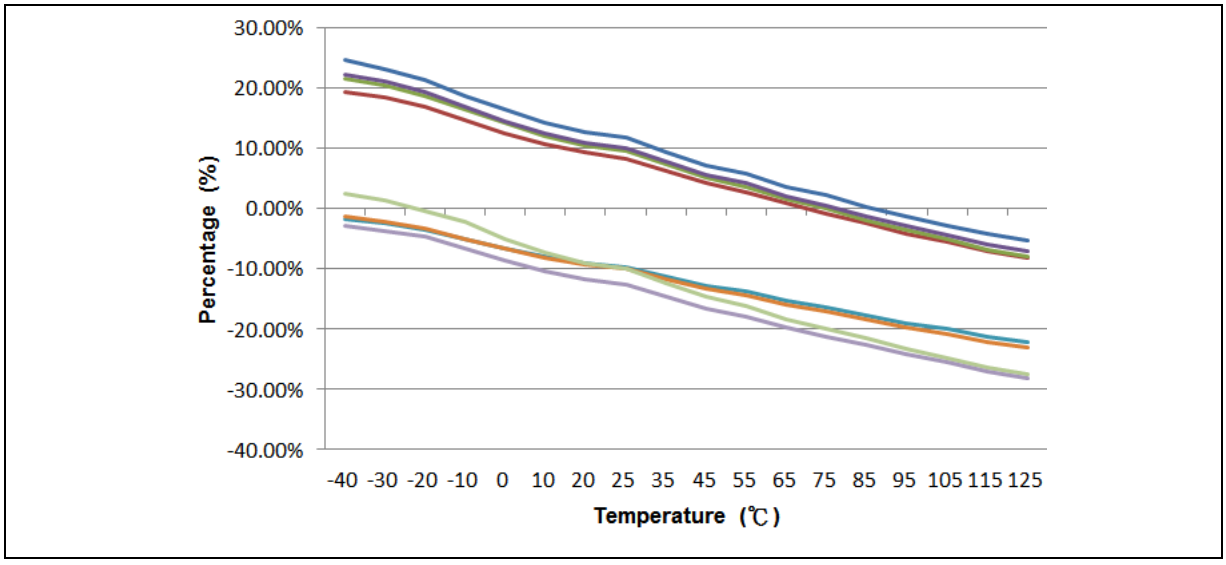


Figure 7.3-3 LIRC deviation under V_{DD} = 5.5 V

7.3.3 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Normal mode [4] output high (90%) to low level (10%) falling time	4.6	5.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.9	3.3		C_L = 10 pF, V_{DD} >= 5.5 V
		6.6	8		C_L = 30 pF, V_{DD} >= 3.3 V
		4.3	5		C_L = 10 pF, V_{DD} >= 3.3 V
		8.5	12.5		C_L = 30 pF, V_{DD} >= 2.4 V
		8.0	10.7		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{f(IO)out}$	High slew rate mode [5] output high (90%) to low level (10%) falling time	4.0	4.3	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		4.9	5.8		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		9.5	13.8		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	Normal mode [4] output low (10%) to high level (90%) rising time	5.6	6.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.4	3.7		C_L = 10 pF, V_{DD} >= 5.5 V
		8.1	9.4		C_L = 30 pF, V_{DD} >= 3.3 V
		5.1	5.8		C_L = 10 pF, V_{DD} >= 3.3 V
		15.1	20.3		C_L = 30 pF, V_{DD} >= 2.4 V
		9.6	12.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	High slew rate mode [5] output low (10%) to high level (90%) rising time	4.8	5.2	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		6.4	7.4		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		12.7	16.9		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$f_{max(IO)out}$ [*3]	I/O maximum frequency	24	24	MHz	C_L = 30 pF, V_{DD} >= 2.4 V
					C_L = 10 pF, V_{DD} >= 2.4 V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. PxSR.n bit value = 0, Normal output slew rate
5. PxSR.n bit value = 1, high speed output slew rate

Table 7.3-4 I/O AC characteristics

7.4 Analog Characteristics

7.4.1 Reset and Power Control Block Characteristics

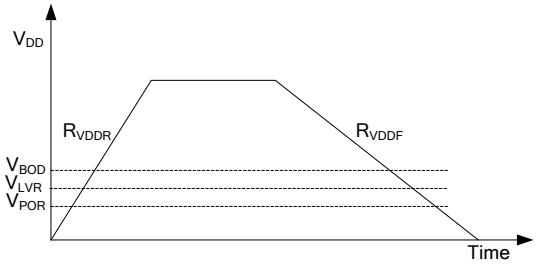
The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	10		20	μA	AV_{DD} = 5.5V
I_{LVR}[*1]	LVR operating current	0.5	-	1		AV_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-	0.5	2.9		AV_{DD} = 5.5V
V_{POR}	POR reset voltage	1	1.15	1.3	V	-
V_{LVR}	LVR reset voltage	1.7	2.0	2.4		-
V_{BOD}	BOD brown-out detect voltage	4.25	4.4	4.55		BOV[1:0] = [0,0]
		3.55	3.7	3.85		BOV[1:0] = [0,1]
		2.60	2.7	2.80		BOV[1:0] = [1,0]
		2.10	2.2	2.30		BOV[1:0] = [1,1]
T_{LVR_SU}[*1]	LVR startup time	60	-	80	μs	-
T_{LVR_RE}[1]	LVR respond time	0.4	-	4		Fsys = HIRC@16MHz
		180	-	350		Fsys = LIRC
T_{BOD_SU}[1]	BOD startup time	180	-	320		Fsys = HIRC@16MHz
T_{BOD_RE}[1]	BOD respond time	2.5	-	5		Fsys = HIRC@16MHz

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 7.4-1 Reset and power control unit



BODFLT (BODCON1.1)	BOD Operation Mode	System Clock Source	Minimum Brown-out Detect Pulse Width
0	Normal mode (LPBOD[1:0] = [0,0])	Any clock source	Typ. 1μs
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	16 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	64 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	256 ($1/F_{LIRC}$)
1	Normal mode (LPBOD[1:0] = [0,0])	HIRC/ECLK	Normal operation: 32 ($1/F_{SYS}$) Idle mode: 32 ($1/F_{SYS}$) Power-down mode: 2 ($1/F_{LIRC}$)
		LIRC	2 ($1/F_{LIRC}$)
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	18 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	66 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	258 ($1/F_{LIRC}$)

Table 7.4-2 Minimum Brown-out Detect Pulse Width

7.4.2 12-bit SAR ADC

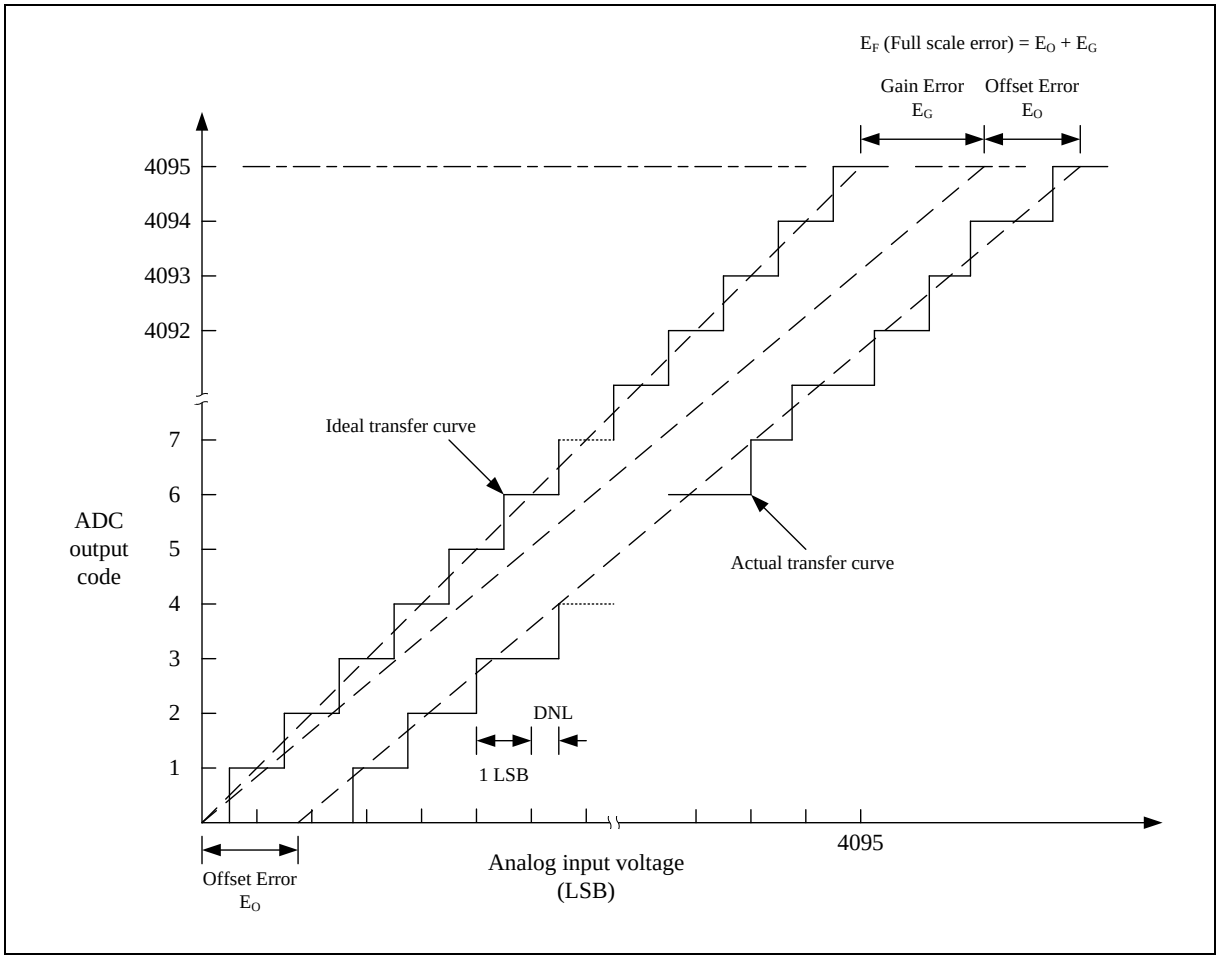
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	2.7	-	5.5	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference voltage	2.7	-	AV_{DD}	V	$V_{REF} = AV_{DD}$
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	Operating current (AV_{DD} + V_{REF} current)	-	-	418	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5.5 V F_{ADC} = 500 kHz $T_{CONV} = 17 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[1] $1/T_{ADC}$	ADC Clock frequency	-	500	-	kHz	
T_{SMP}	Sampling Time	1	-	38	$1/F_{ADC}$	$T_{SMP} = \frac{4 * ADCAQT + 10}{F_{ADC}}$
T_{CONV}	Conversion time	1	-	128	$1/F_{ADC}$	
T_{EN}	Enable to ready time	20	-	-	μs	
INL[*1]	Integral Non-Linearity Error	-3	-	+3	LSB	$V_{REF} = AV_{DD} = V_{DD}$
DNL[*1]	Differential Non-Linearity Error	-2	-	+4	LSB	$V_{REF} = AV_{DD} = V_{DD}$

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
E_G[*1]	Gain error	-3.5	-	+0.4	LSB	$V_{REF} = AV_{DD}=V_{DD}$
E_O[*1]$_T$	Offset error	-2	-	+2.8	LSB	$V_{REF} = AV_{DD}=V_{DD}$
E_A[*1]	Absolute Error	-7		+7	LSB	$V_{REF} = AV_{DD}=V_{DD}$

Notes:

1. Guaranteed by characterization result, not tested in production.

Table 7.4-3 ADC characteristics



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

7.5 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.62	1.8	1.98	V	T_A = 25℃
T_{ERASE}	Page erase time	-	5	-	ms	
T_{PROG}	Program time	-	10	-	μs	
I_{DD1}	Read current	-	4	-	mA	
I_{DD2}	Program current	-	4	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Endurance	100,000	-		cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	50	-	-	year	100 kcycle[3] T_A = 55℃
		25	-	-	year	100 kcycle[3] T_A = 85℃
		10	-	-	year	100 kcycle[3] T_A = 105℃

Notes:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.

Table 7.5-1 Flash memory characteristics

7.6 Absolute Maximum Ratings

Volrage Stesses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

7.6.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on I/O	V_{SS}-0.3	5.5	V

Notes:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.

Table 7.6-1 Voltage characteristics

7.6.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	200	
I_{IO}	Maximum current sunk by a I/O Pin	-	22	
	Maximum current sourced by a I/O Pin	-	10	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by V_{IN}>A_{VDD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 7.6-2 Current characteristics

7.6.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 20-pin QFN(3x3 mm)	-	68	-	℃ /Watt
	Thermal resistance junction-ambient 20-pin TSSOP(4.4x6.5 mm)	-	38	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 7.6-3 Thermal characteristics

7.6.4 EMC Characteristics

7.6.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

7.6.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

7.6.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-8000	-	+8000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[*3]	Pin current for latch-up[*3]	-400	-	+400	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4	-	+4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 7.6-4 EMC characteristics

7.6.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
20-pin QFN(3x3 mm) [*1]	MSL 3
20-pin TSSOP(4.4x6.5 mm) [*1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 7.6-5 Package Moisture Sensitivity(MSL)

7.6.6 Soldering Profile

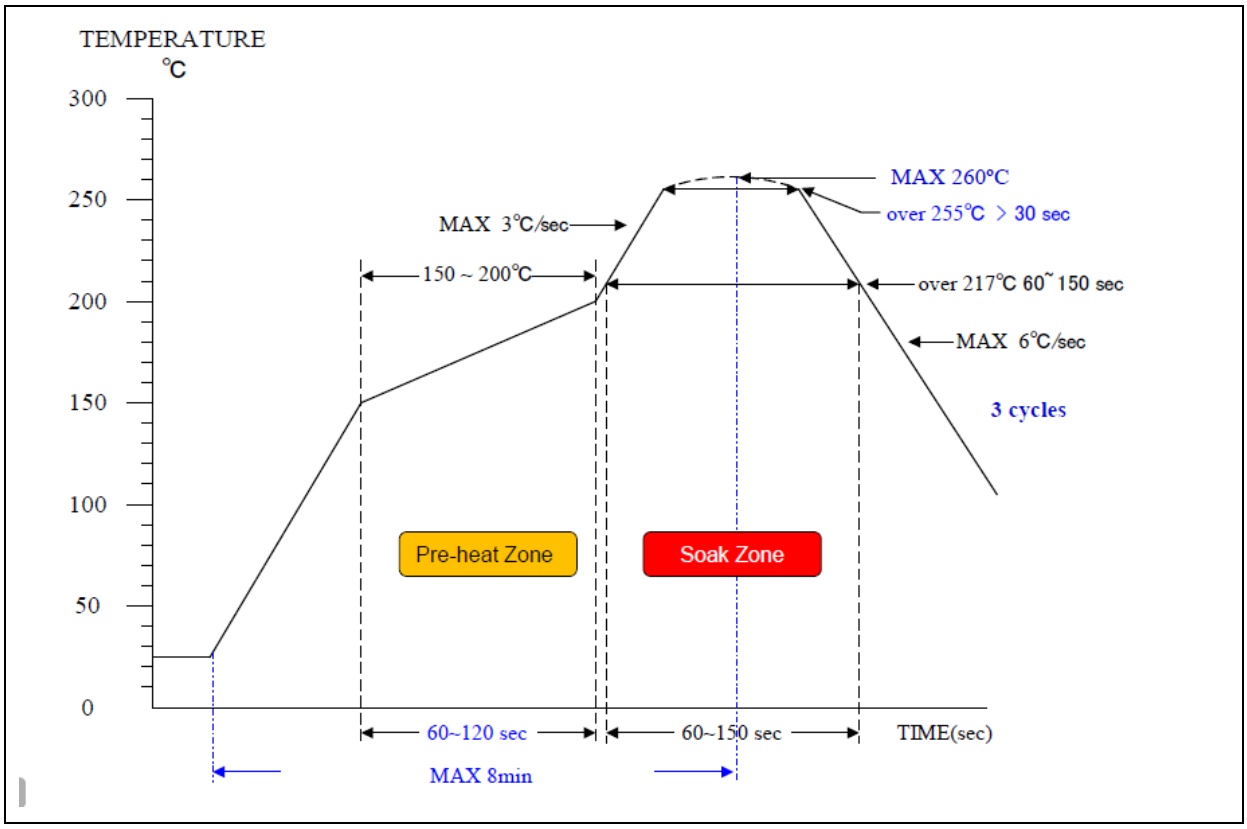


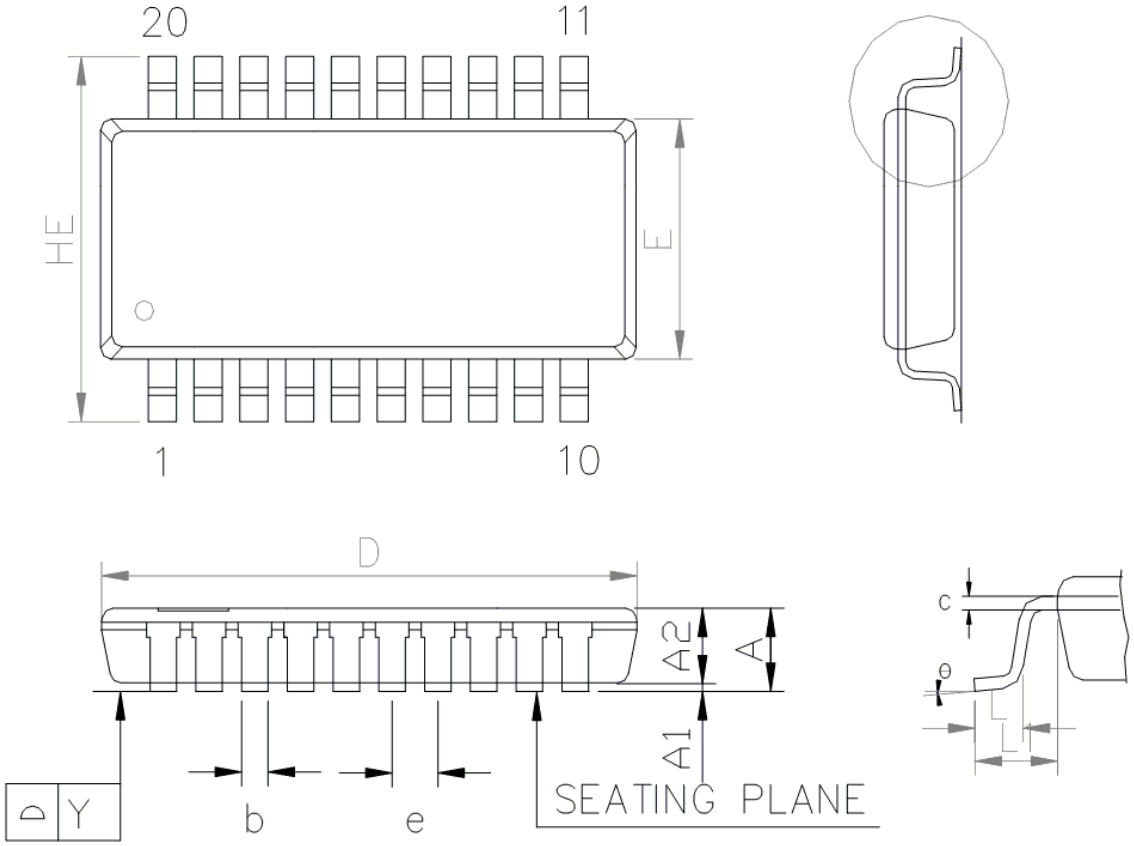
Figure 7.6-1 Soldering profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 7.6-6 Soldering Profile

8 PACKAGE DIMENSIONS

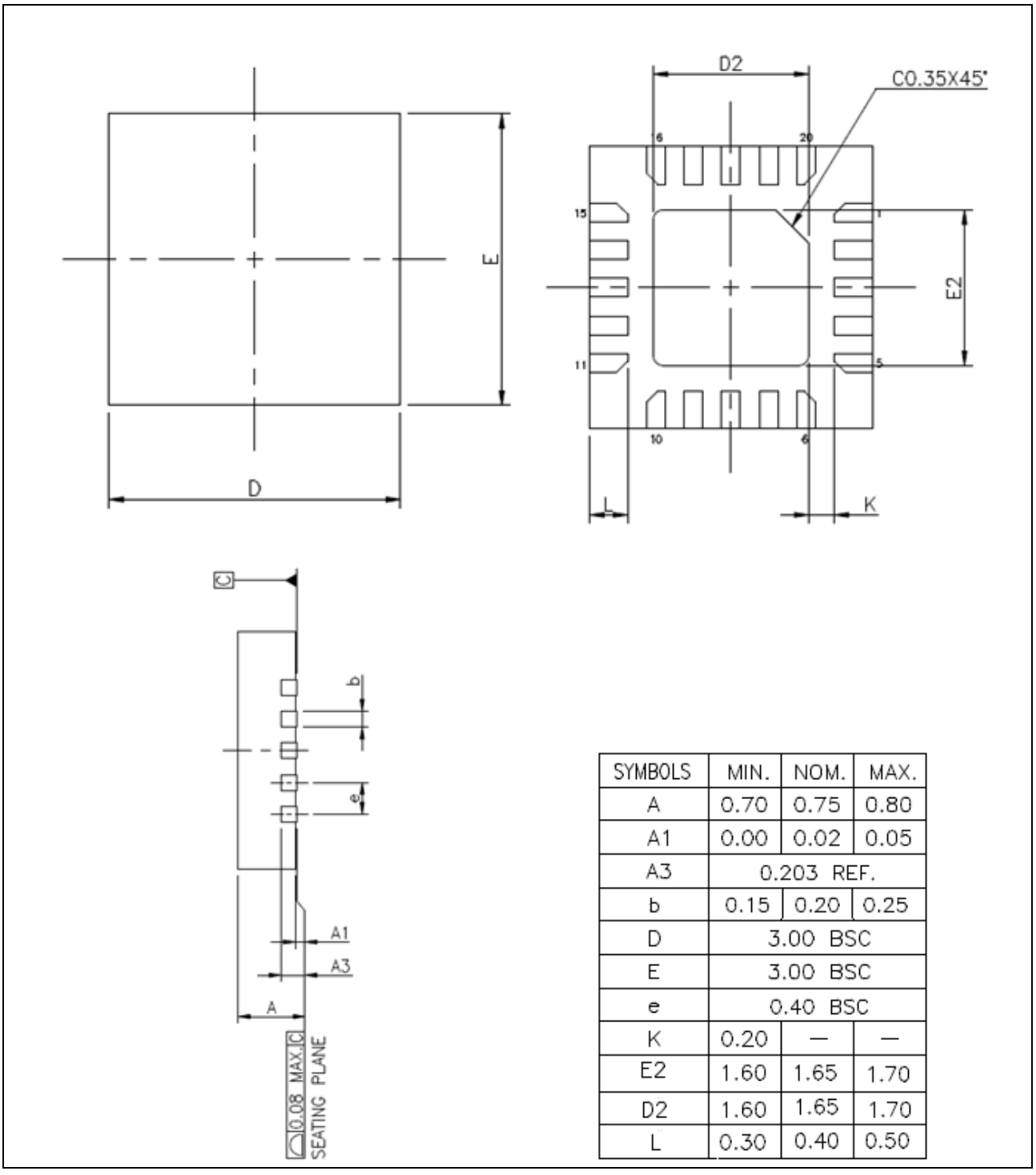
8.1 TSSOP 20 (4.4 X 6.5 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

Figure 8.1-1 TSSOP-20 Package Dimension

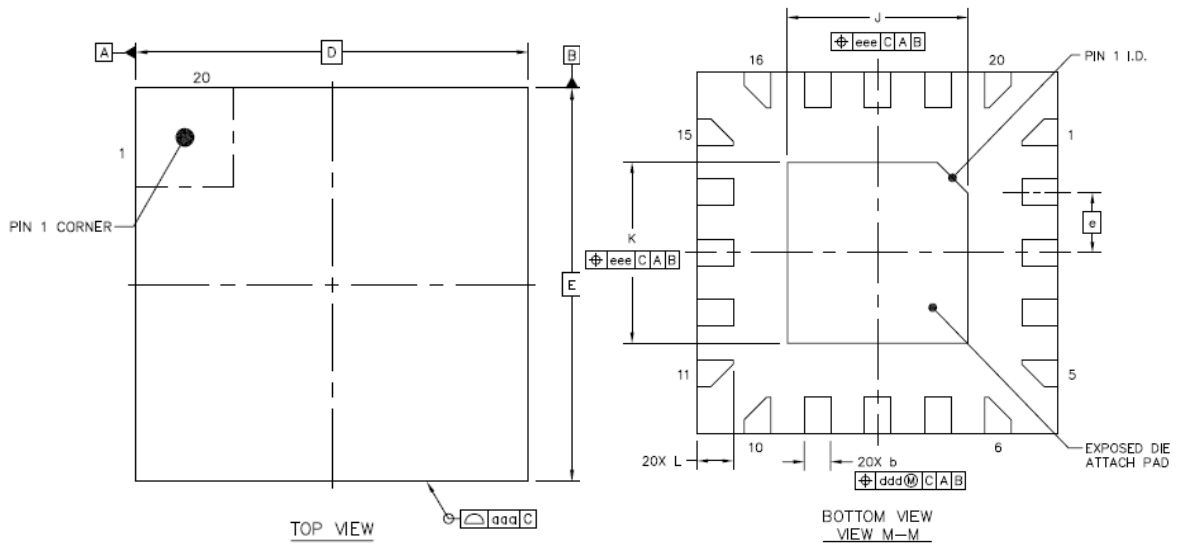
8.2 20-pin QFN 3.0 X 3.0 mm for MS51XB9AE

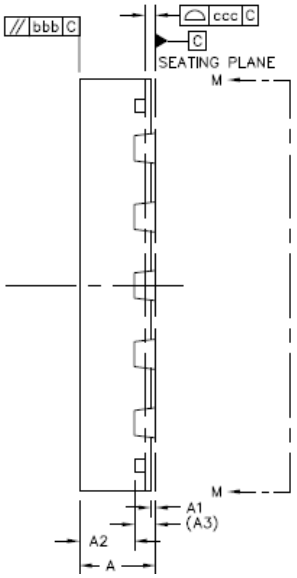


SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
e		0.40 BSC	
K	0.20	—	—
E2	1.60	1.65	1.70
D2	1.60	1.65	1.70
L	0.30	0.40	0.50

Figure 8.2-1 QFN-20 Package Dimension for MS51XB9AE

8.3 20-pin QFN 3.0 X 3.0 mm for MS51XB9BE





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.40	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.17	0.22	0.27
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	1.4	1.50	1.6
	Y	K	1.4	1.50	1.6
LEAD LENGTH		L	0.25	0.30	0.35
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 8.3-1 QFN-20 Package Dimension for MS51XB9BE

9 ABBREVIATIONS

9.1 Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BOD	Brown-out Detection
GPIO	General-Purpose Input/Output
Fsys	Frequency of system clock
HIRC	12 MHz Internal High Speed RC Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LVR	Low Voltage $eset
PDMA	Peripheral Direct Memory Access
POR	Power On Reset
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WKT	Wakeup Timer
WDT	Watchdog Timer

Table 9.1-1 List of Abbreviations

10 REVISION HISTORY

Date	Revision	Description
2019.1.29	1.00	Initial release.

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