



**THE DATASHEET OF  
SLB9672AU20FW1610XTMA1**



# OPTIGA™ TPM

## SLB 9672 TPM2.0

### Data Sheet

#### Devices

- SLB 9672XU2.0 FW16.xx
- SLB 9672AU2.0 FW16.xx

#### Key features

- Optimized TPM device for IoT and ICT applications
- PQC-protected firmware update mechanism
- Compliant to TPM Main Specification, Family "2.0", Level 00, Revision 01.59
- Certifications:
  - CC, Version 3.1 Rev.5, level EAL4+, AVA\_VAN.4 (moderate) according to TCG PC Client TPM Protection Profile
  - FIPS 140-2 level 2 (physical security level 3) (targeted)
- SPI interface
- Meeting Intel TXT and Microsoft Windows certification criteria for successful platform qualification
- Random Number Generator (RNG) implemented according to NIST SP800-90A using entropy source according to NIST SP800-90B
- Full personalization with 4 Endorsement Keys (EK) and 4 EK certificates (RSA 2048, RSA 3072, ECC NIST P256, ECC NIST P384)
- Enhanced temperature range (-40°C .. +85°C or -40°C .. +105°C)
- PG-UQFN-32-1,-2 package
- Optimized for battery operated devices: low standby power consumption (typ. 120 µA)
- 24 PCRs (SHA-1, SHA-256 or SHA384)
- 51 kByte NV memory
- Unlimited amount of NV counters (only depending on NV memory utilization)
- Up to 3 loaded sessions (TPM\_PT\_HR\_LOADED\_MIN)
- Up to 64 active sessions (TPM\_PT\_ACTIVE\_SESSIONS\_MAX)
- Up to 3 loaded transient Objects (TPM\_PT\_HR\_TRANSIENT\_MIN)
- Up to 7 loaded persistent Objects (TPM\_PT\_HR\_PERSISTENT\_MIN)
- Pre-generation of up to 7 RSA key pairs
- RSA (1024, 2048, 3072 and 4096 bit)
- ECC (NIST P256, BN P256, NIST P384)
- SHA-1, SHA-256, SHA-384
- AES-128, AES-192, AES-256

## **About this document**

### **Scope and purpose**

This data sheet describes the OPTIGA™ TPM SLB 9672 FW16.xx Trusted Platform Module together with its features, functionality and programming interface.

### **Intended audience**

This data sheet is primarily intended for system developers.

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**Overview**

**1 Overview**

The OPTIGA™ TPM SLB 9672 is a Trusted Platform Module. It is available in PG-UQFN-32-1,-2 package. It supports an SPI interface with a transfer rate of up to 33 MHz (typical). The OPTIGA™ TPM SLB 9672 is a TPM based on TCG family 2.0 specifications (see [1] and [2]).

This TPM product is targeted to be certified, using the Common Criteria for Information Technology Security Evaluation (CC), Version 3.1 Rev.5, in the level EAL4+, AVA\_VAN.4 (moderate), ALC\_FLR.1 according to the Protection Profile PC Client Specific TPM, TPM Library Specification Family "2.0" Level 0 Revision 1.59 (CERTIFICATE ANSSI-CC-PP-2020/01).

**1.1 Power management**

In the OPTIGA™ TPM SLB 9672, power management is handled internally; no explicit power-down or standby mode is available. The device automatically enters a low-power state after each successful command/response transaction. If a transaction is started on the SPI bus from the host platform, the device will wake immediately and will return to the low-power mode after the transaction has been finished.

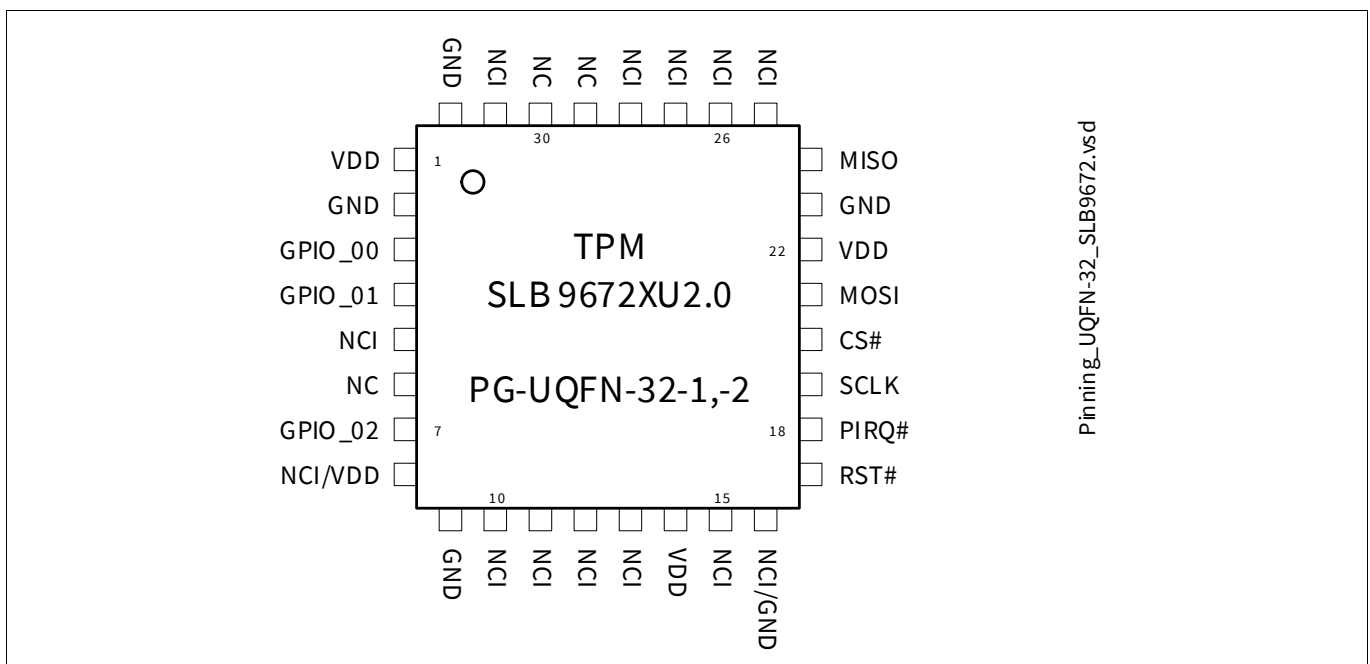
**2 Device types and ordering information**

The OPTIGA™ TPM SLB 9672 product family features devices using an UQFN package. **Table 1** shows the different versions.

**Table 1 Device configuration**

Device Name	Package	Remarks
SLB 9672XU2.0 FW16.xx	PG-UQFN-32-1,-2	Enhanced temperature range -40°C - 85°C
SLB 9672AU2.0 FW16.xx	PG-UQFN-32-1,-2	Enhanced temperature range -40°C - 105°C

**3 Pin description**



**Figure 1 Pinout of the OPTIGA™ TPM SLB 9672 (PG-UQFN-32-1,-2 package, top view)**

Pin description

**Table 2 Buffer types**

Buffer type	Description
TS	Tri-state pin
ST	Schmitt-trigger pin
OD	Open-drain pin

**Table 3 I/O Signals**

Pin number	Name	Pin type	Buffer type	Function
PG-UQFN-32-1,-2				
20	CS#	I	ST	<b>Chip select</b> The SPI chip select signal (active low).
19	SCLK	I	ST	<b>SPI clock</b> The SPI clock signal. Only SPI mode 0 is supported by the device.
21	MOSI	I	ST	<b>Master out slave in (SPI data)</b> SPI data which is received from the master.
24	MISO	O	TS	<b>Master in slave out (SPI data)</b> SPI data which is sent to the SPI bus master.
18	PIRQ#	O	OD	<b>Interrupt request</b> Interrupt request signal to the host. The pin has no internal pull-up resistor. The interrupt is active low.
17	RST#	I	ST	<b>Reset</b> External reset signal. Asserting this pin unconditionally resets the device. The signal is active low and is typically connected to the PCIRST# signal of the host. This pin has a weak internal pull-up resistor.
3	GPIO_00	I/O	TS	<b>General purpose IO</b> This pin may be left unconnected; it has an internal pull-up resistor. It can be controlled via TPM NV GPIO functionality.
4	GPIO_01	I/O	TS	<b>General purpose IO</b> This pin may be left unconnected; it has an internal pull-up resistor. It can be controlled via TPM NV GPIO functionality.
7	GPIO_02	I/O	TS	<b>General purpose IO</b> This pin may be left unconnected; it has an internal pull-up resistor. It can be controlled via TPM NV GPIO functionality.

Pin description

**Table 4 Power supply**

Pin number	Name	Pin type	Buffer type	Function
<b>PG-UQFN-32-1,-2</b>				
1, 14, 22	VDD	PWR	—	<b>Power supply</b> All VDD pins must be connected externally and should be bypassed to GND via 100 nF capacitors.
2, 9, 23, 32	GND	GND	—	<b>Ground</b> All GND pins must be connected externally.

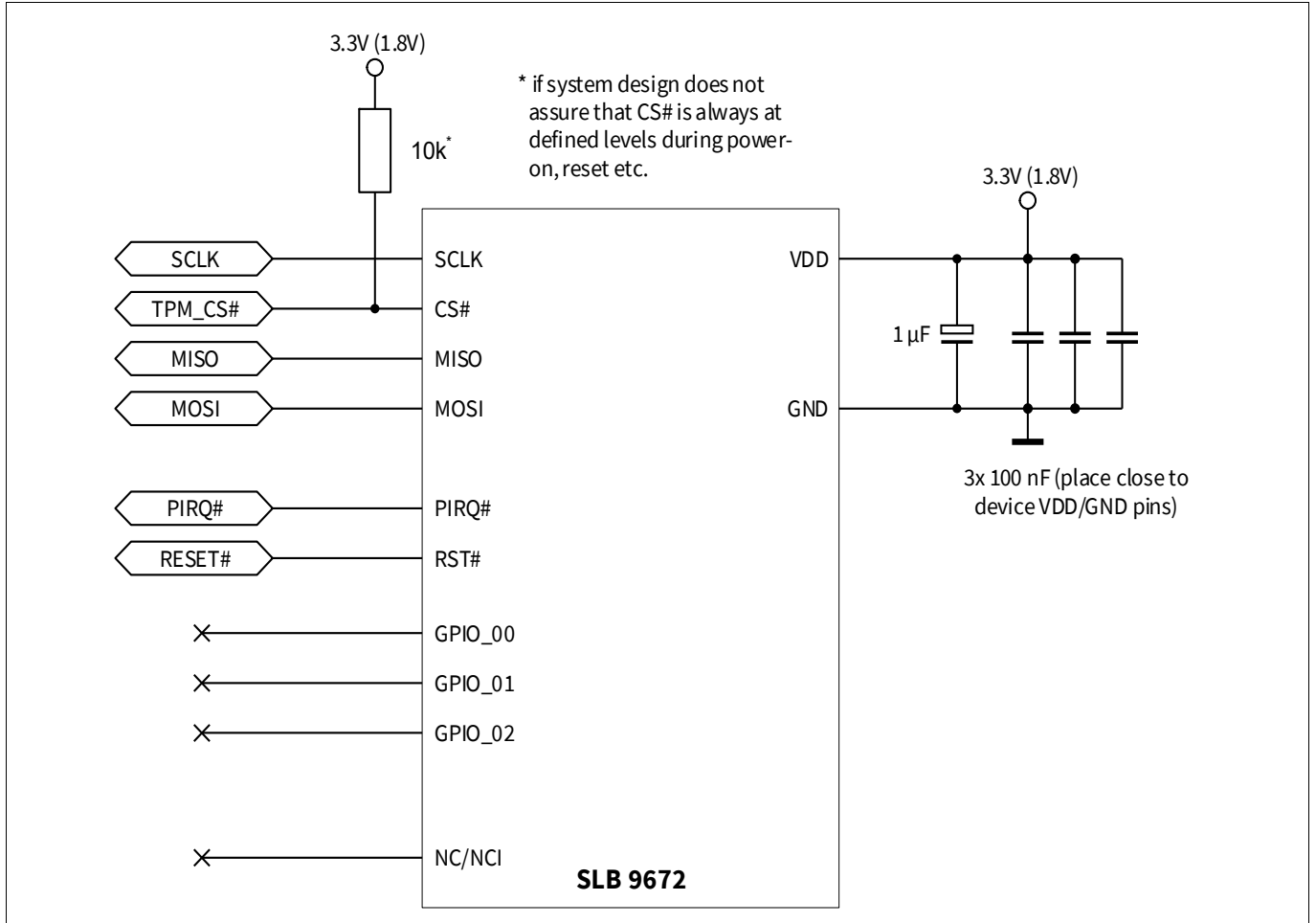
**Table 5 Not connected**

Pin number	Name	Pin type	Buffer type	Function
<b>PG-UQFN-32-1,-2</b>				
6, 29, 30	NC	NU	—	<b>No connect</b> All pins must not be connected externally (must be left floating).
5, 10 - 13, 15, 25 - 28, 31	NCI	—	—	<b>Not connected internally</b> All pins are not connected internally (can be connected externally).
8	NCI/VDD	—	—	<b>Not connected internally/VDD</b> This pin is not connected internally (can be connected externally). Note that pin 8 is defined as VDD in the TCG specification [2]. To be compliant, VDD can be connected to this pin.
16	NCI/GND	—	—	<b>Not connected internally/GND</b> This pin is not connected internally (can be connected externally). Note that pin 16 is defined as GND in the TCG specification [2]. To be compliant, GND can be connected to this pins.

**Pin description**

**3.1 Typical schematic**

**Figure 2** shows the typical schematic for the OPTIGA™ TPM SLB 9672. The power supply pins should be bypassed to GND with capacitors located close to the device.



**Figure 2 Typical schematic**

**TPM properties**

**4 TPM properties**

Properties defined within the TPM can be read with the command TPM2\_GetCapability. The values are vendor dependent or determined by a platform-specific specification. The following properties are returned by the Infineon OPTIGA™ TPM SLB 9672 using the command TPM2\_GetCapability (capability = TPM\_CAP\_TPM\_PROPERTIES):

**Table 6 Infineon TPM property values**

TPM_PT_MANUFACTURER	“IFX”
TPM_PT_VENDOR_STRING_1	“SLB9”
TPM_PT_VENDOR_STRING_2	“672”
TPM_PT_VENDOR_STRING_3	NULL
TPM_PT_VENDOR_STRING_4	NULL
TPM_PT_FIRMWARE_VERSION_1	Major and minor version (for instance, 0x0010000D indicates V16.13) <sup>1)</sup>
TPM_PT_FIRMWARE_VERSION_2	Build number and Common Criteria certification state (for instance, 0x00454500 or 0x00454502) <sup>1)</sup> Byte 1: reserved for future use (0x00) Byte 2 and 3: Build number (for instance, 0x4545) <sup>1)</sup> Byte 4: Common Criteria certification state/mode: 0x00 = TPM operational mode/TPM is CC certified 0x02 = TPM operational mode/TPM is not certified 0x60 = Manually entered TPM firmware recovery mode (triggered externally for testing purposes) 0x61 = TPM firmware recovery mode (triggered by code integrity failure detection) 0x62 = TPM firmware update mode
TPM_PT_MODES	Bit 0 (FIPS_140_2) = 1 Bits 1..31 = 0

1) The build- and version numbers given here are examples and do not necessarily match the numbers of the device this datasheet has been provided for.

Electrical characteristics

## 5 Electrical characteristics

This chapter lists the maximum and operating ranges for various electrical and timing parameters.

### 5.1 Absolute maximum ratings

**Table 7 Absolute maximum ratings**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply Voltage	$V_{DD}$	-0.3	–	4.1	V	–
Voltage on any pin	$V_{max}$	-0.5	–	4.1	V	–
Ambient temperature	$T_A$	-40	–	85	°C	Enhanced temperature SLB 9672XU2.0 devices
Ambient temperature	$T_A$	-40	–	105	°C	Enhanced temperature SLB 9672AU2.0 devices
Storage temperature	$T_S$	-40	–	125	°C	–
ESD robustness HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	–	–	2000	V	According to EIA/JESD22-A114-B
ESD robustness	$V_{ESD,CDM}$	–	–	500	V	According to ESD Association Standard STM5.3.1 - 1999
Latchup immunity	$I_{latch}$			100	mA	According to EIA/JESD78

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

### 5.2 Functional operating range

**Table 8 Functional operating range**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply Voltage	$V_{DD}$	3.0	3.3	3.6	V	–
		1.65	1.8	1.95	V	–
Ambient temperature	$T_A$	-40	–	85	°C	Enhanced temperature SLB 9672XU2.0 devices
Ambient temperature	$T_A$	-40	–	105	°C	Enhanced temperature SLB 9672AU2.0 devices
Useful lifetime		–	–	10	y	
Operating lifetime		–	–	10	y	
Average $T_A$ over lifetime		–	55	–	°C	

**Electrical characteristics**

**5.3 DC characteristics**

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$  or  $V_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$  unless otherwise noted.

**Table 9 Current consumption**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Current Consumption in Active Mode	$I_{VDD\_Active}$			35	mA	
Current Consumption in Sleep Mode	$I_{VDD\_Sleep}$		120		$\mu\text{A}$	Pins GPIO, RST# and PIRQ# = $V_{DD}$ , CS# inactive (= $V_{DD}$ ), MOSI, MISO and SCLK don't care
Current Consumption during reset	$I_{VDD\_Reset}$		130		$\mu\text{A}$	Pin RST# active (= GND), GPIO, PIRQ#, CS#, MOSI, MISO and SCLK don't care

Note: Current consumption does not include any currents flowing through resistive loads on output pins!

Note: Device sleep mode will be entered after 50 milliseconds of inactivity after the last TPM command was executed.

**Table 10 DC characteristics of SPI interface pins (SCLK, CS#, MISO, MOSI, RST#, PIRQ#)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage high	$V_{IH}$	$0.7 V_{DD}$		$V_{DD}+0.5$	V	$V_{DD,typ} = 3.3\text{ V}$ , only pins SCLK, MISO, MOSI and CS#
		$0.7 V_{DD}$		$V_{DD}+0.3$	V	$V_{DD,typ} = 3.3\text{ V}$ , pin RST#
		$0.7 V_{DD}$		$V_{DD}+0.3$	V	$V_{DD,typ} = 1.8\text{ V}$
Input voltage low	$V_{IL}$	-0.5		$0.3 V_{DD}$	V	$V_{DD,typ} = 3.3\text{ V}$
		-0.3		$0.3 V_{DD}$	V	$V_{DD,typ} = 1.8\text{ V}$
Input leakage current	$I_{LEAK}$	-4		4	$\mu\text{A}$	$0\text{ V} < V_{IN} < V_{DD}$
		-4.5			mA	Pins SCLK, CS#, MISO, MOSI $-0.5\text{ V} < V_{IN} < V_{DD}+0.5\text{ V}$ $V_{DD,typ} = 3.3\text{ V}$
		-4.5			mA	Pins SCLK, CS#, MISO, MOSI $-0.3\text{ V} < V_{IN} < V_{DD}+0.3\text{ V}$ $V_{DD,typ} = 1.8\text{ V}$
		-2		2	$\mu\text{A}$	Pin RST# $0\text{ V} < V_{IN} < V_{DD}$
Output high voltage	$V_{OH}$	$0.9 V_{DD}$			V	$I_{OH} = -100\text{ }\mu\text{A}$
Output low voltage	$V_{OL}$			$0.1 V_{DD}$	V	$I_{OL} = 1.5\text{ mA}$
Pad input capacitance	$C_{IN}$			10	pF	
Output load capacitance	$C_{LOAD}$			30	pF	

Electrical characteristics

**Table 11 DC characteristics of GPIO pins**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage high	$V_{IH}$	$0.7 V_{DD}$		$V_{DD}+0.3$	V	Pins GPIO
Input voltage low	$V_{IL}$	-0.5		$0.3 V_{DD}$	V	Pins GPIO
Input leakage current	$I_{LEAK}$	-2		2	$\mu A$	$0 V < V_{IN} < V_{DD}$
Output high voltage	$V_{OH}$	$V_{DD}-0.3$			V	$I_{OH} = -1 \text{ mA}$ , pins GPIO
Output low voltage	$V_{OL}$			0.3	V	$I_{OL} = 1 \text{ mA}$ , pins GPIO
Pad input capacitance	$C_{IN}$			10	pF	Pins GPIO

**5.4 AC characteristics**

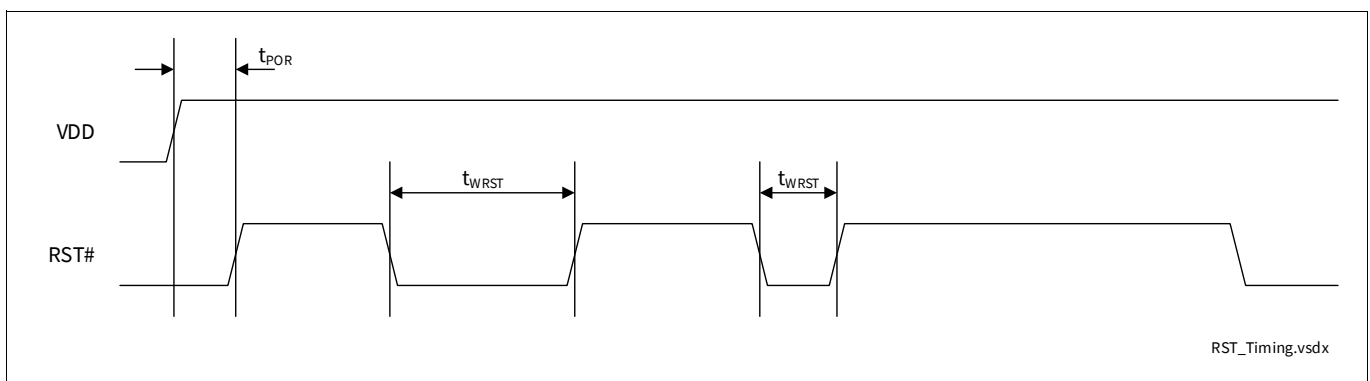
$T_A = 25^\circ C$ ,  $V_{DD} = 3.3V \pm 0.3V$  or  $V_{DD} = 1.8V \pm 0.15V$  unless otherwise noted.

**Table 12 Power supply**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage rise time	$t_{VDDR}$			1.0	V/ns	

**Table 13 Device reset**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Cold (Power-On) Reset	$t_{POR}$	80			$\mu s$	
Warm Reset	$t_{WRST}$	2			$\mu s$	



**Figure 3 Reset timing**

**Table 14 AC characteristics of SPI interface**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
SCLK frequency	$f_{CLK}$		33	34.65	MHz	
SCLK period	$t_{CLK}$	$1/f_{CLK} - 5\%$	$1/f_{CLK}$	$1/f_{CLK} + 5\%$	$\mu s$	Rising edge to rising edge, measured at $V_{IN} = 0.5 V_{DD}$

**Electrical characteristics**

**Table 14 AC characteristics of SPI interface (continued)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
SCLK low time	$t_{CLKL}$	$0.45 t_{CLK}$			$\mu s$	Falling edge to rising edge, measured at $V_{IN} = 0.5 V_{DD}$
SCLK high time	$t_{CLKH}$	$0.45 t_{CLK}$			$\mu s$	Rising edge to falling edge, measured at $V_{IN} = 0.5 V_{DD}$
SCLK slew rate (rising/falling)	$t_{SLEW}$	0.216		4	V/ns	$f_{CLK} < 20$ MHz, between $0.2 V_{DD}$ and $0.6 V_{DD}$
		0.4		4	V/ns	$f_{CLK} \geq 20$ MHz, between $0.2 V_{DD}$ and $0.6 V_{DD}$
CS# high time	$t_{CS}$	50			ns	Rising edge to falling edge
		60			ns	$V_{DD,typ} = 1.8$ V and $t_{SLEW} < 1$ V/ns, rising edge to falling edge, TPM protocol abort only
CS# setup time	$t_{CSS}$	5			ns	CS# falling edge to SCLK rising edge
		7			ns	$V_{DD,typ} = 1.8$ V and $t_{SLEW} < 1$ V/ns, CS# falling edge to SCLK rising edge
CS# hold time	$t_{CSH}$	5			ns	SCLK falling edge to CS# rising edge
MOSI setup time	$t_{SU}$	2			ns	Data setup time to SCLK rising edge
MOSI hold time	$t_H$	3			ns	Data hold time from SCLK rising edge
MISO hold time	$t_{HO}$	0			ns	Output hold time from SCLK falling edge
MISO valid delay time	$t_V$	0		$0.7 t_{CLKL}$	ns	Output valid delay from SCLK falling edge
MISO active time	$t_{DRV}$	0			ns	Delay from chip select assertion to driving of MISO

**5.5 Timing**

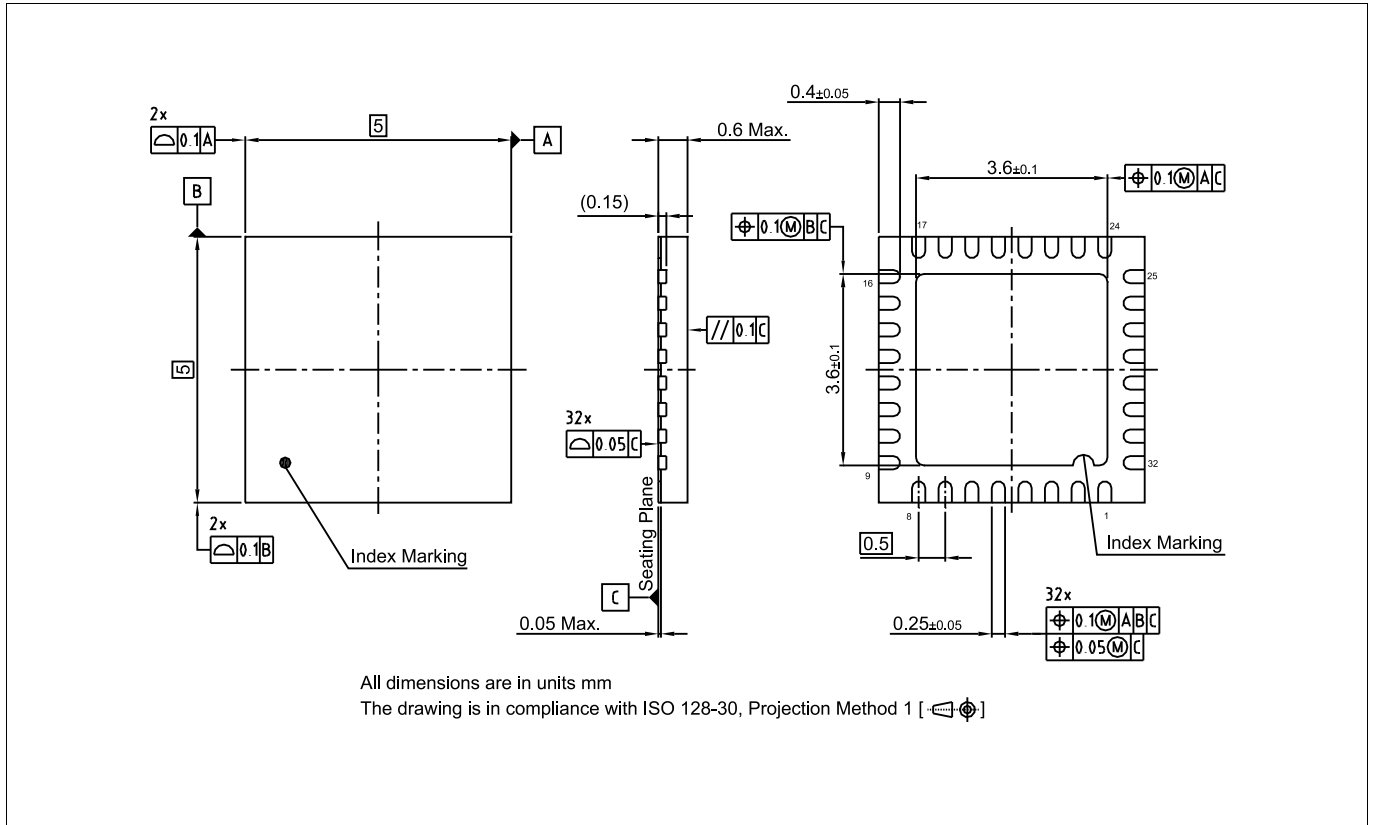
Some pads are disabled after deassertion of the reset signal for up to 500  $\mu s$ .

The OPTIGA™ TPM SLB 9672 features security mechanisms which detect and count all resets.

**Package dimensions (UQFN)**

**6 Package dimensions (UQFN)**

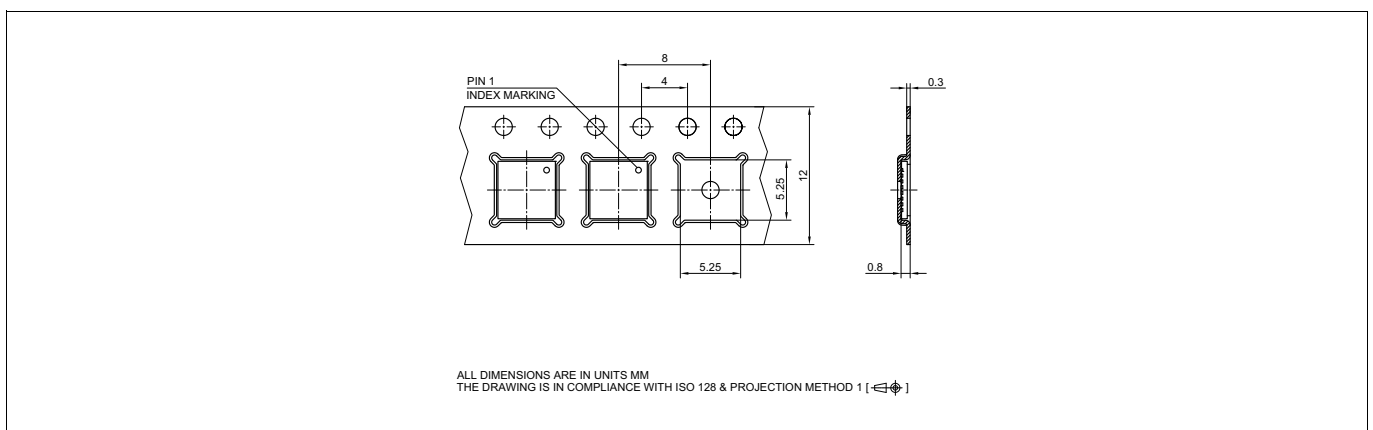
All dimensions are given in millimeters (mm) unless otherwise noted. The packages are “green” and RoHS compliant.



**Figure 4 Package dimensions PG-UQFN-32-1,-2**

**6.1 Packing type**

PG-UQFN-32-1,-2: Tape & Reel (reel diameter 330mm), 5000 pcs. per reel

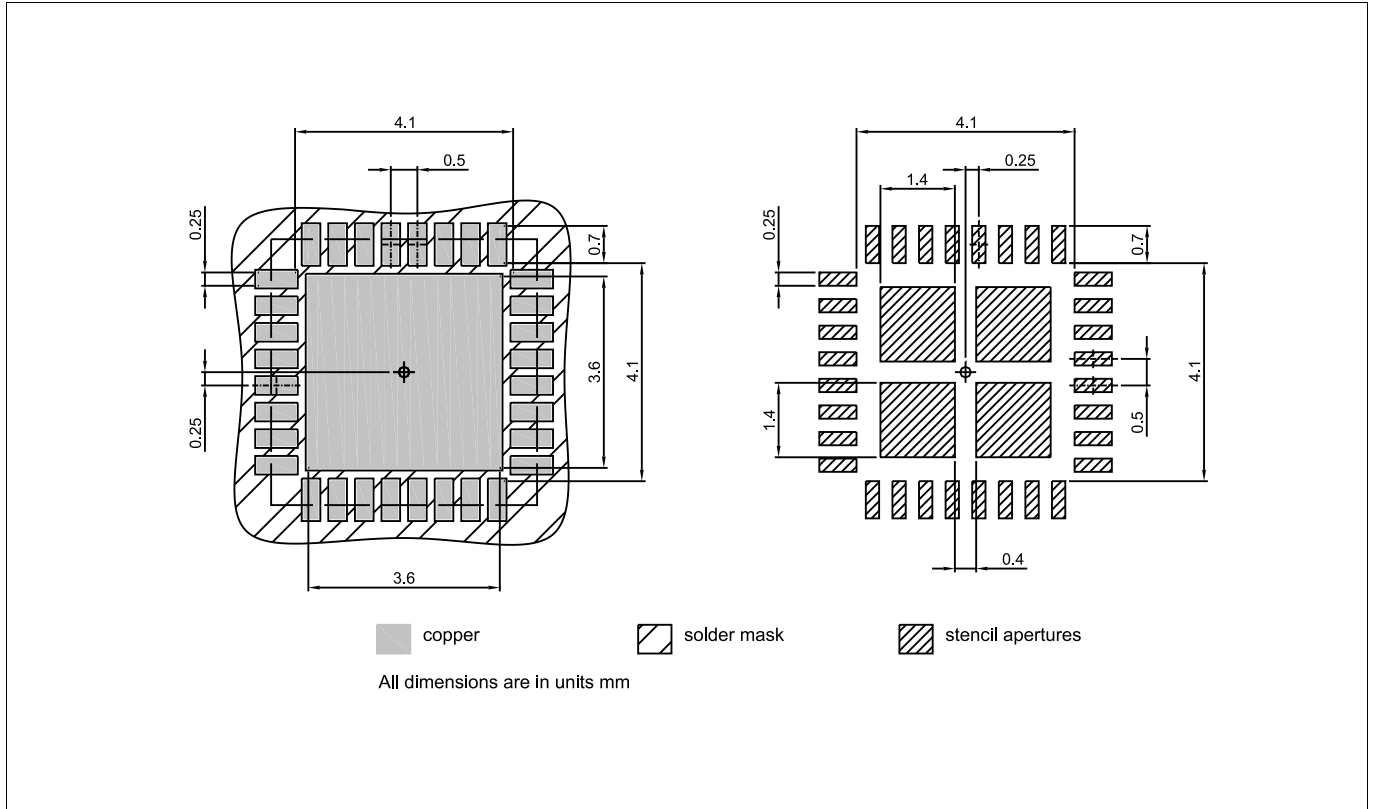


**Figure 5 Tape & reel dimensions PG-UQFN-32-1,-2**

**Package dimensions (UQFN)**

**6.2 Recommended footprint**

**Figure 6** shows the recommended footprint for the PG-UQFN-32-1,-2 package. The exposed pad of the package is internally connected to GND. It shall be connected to GND externally as well.



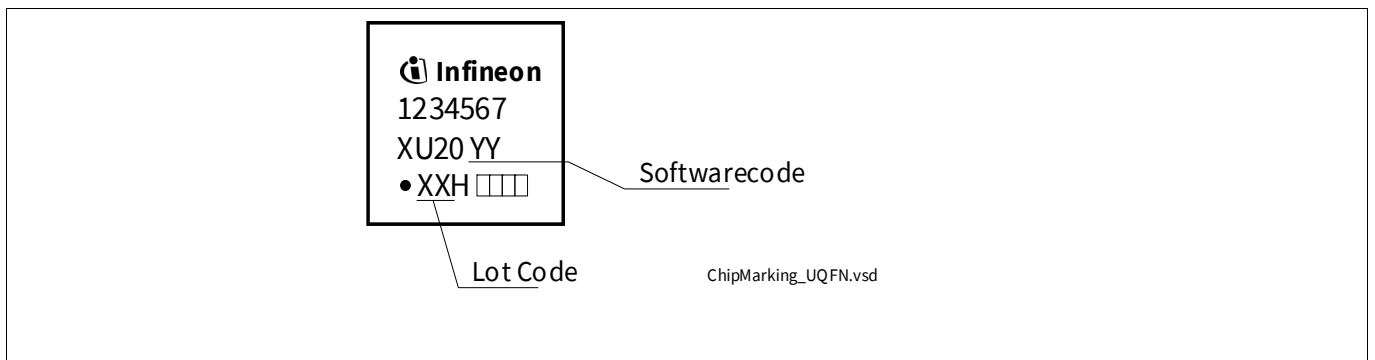
**Figure 6 Recommended footprint PG-UQFN-32-1,-2**

**6.3 Chip marking**

Line 1: SLB9672

Line 2: XU20 yy or AU20 yy (see **Table 1**), the <yy> is an internal FW indication (only at manufacturing due to field upgrade option)

Line 3: <Lot number> H <datecode>



**Figure 7 Chip marking**

For details and recommendations regarding assembly of packages on PCBs, please refer to <http://www.infineon.com/cms/en/product/technology/packages/>

---

**References**

**References**

- [1] —, “Trusted Platform Module Library (Part 1-4)”, Family 2.0, Level 00, Rev. 01.59, November 8, 2019, TCG
- [2] —, “TCG PC Client Platform TPM Profile (PTP) Specification”, Family 2.0, Level 00, Rev. 01.05 v14, September 4, 2020, TCG
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- [4] —, “Errata for PC Client Platform TPM Profile for TPM 2.0 Version 1.05 Revision 14”, Errata Version 1.0, September 04, 2020, TCG
- [5] —, “Registry of reserved TPM 2.0 handles and localities”, Version 1.1, Rev. 1.00, February 6, 2019, TCG
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- [7] —, "NIST Special Publication 800-193, Platform Firmware Resiliency Guidelines", May, 2018, NIST

**Terminology**

**Terminology**

ESW	Embedded Software
HMAC	Hashed Message Authentication Code
PCR	Platform Configuration Register
PUBEK	Public Endorsement Key
SPI	Serial Peripheral Interface (bus)
TCG	Trusted Computing Group
TPM	Trusted Platform Module
TSS	TCG Software Stack

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**Revision history**

Page or item	Subjects (major changes since previous revision)
<b>Revision 1.1, 2023-04-27</b>	
	Added features to front page Fixed wrong revision number in <b>Section 1</b> Changed <b>Figure 2</b> (additional decoupling capacitor) Updated version and build numbers in <b>Section 4</b> Minor editorial changes
<b>Revision 1.0, 2022-01-20</b>	
	Initial document version

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