

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

RF power transistor suitable for industrial heating applications from 728 to 2700 MHz. Device is capable of both CW and pulse operation.

2300 MHz

- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Vdc, $I_{DQ} = 90$ mA, $P_{out} = 1.26$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.⁽¹⁾

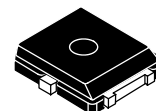
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2300 MHz	21.2	23.6	9.0	-40.9	-10
2350 MHz	21.6	22.6	8.6	-40.0	-22
2400 MHz	20.7	21.0	8.3	-40.1	-9

Features

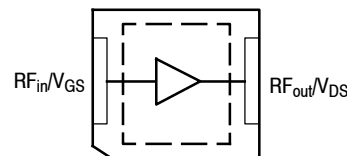
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Universal Broadband Driven Device with Internal RF Feedback

MHT1006NT1

**728–2700 MHz, 10 W CW, 28 V
INDUSTRIAL HEATING, RUGGED
RF POWER LDMOS TRANSISTOR**



**PLD-1.5W
PLASTIC**



(Top View)

Note: The center pad on the backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

1. All data measured in fixture with device soldered to heatsink.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +150	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 81°C, 10 W CW, 28 Vdc, $I_{DQ} = 90$ mA, 2140 MHz	$R_{\theta JC}$	3.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	I_{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 12.1$ μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ($V_{DD} = 28$ Vdc, $I_D = 90$ mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.5	1.8	2.3	Vdc
Drain-Source On-Voltage ($V_{GS} = 6$ Vdc, $I_D = 121$ mAdc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Typical Performance over Frequency ⁽¹⁾ (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 90\text{ mA}$, $P_{out} = 1.26\text{ W Avg.}$, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2300 MHz	21.2	23.6	9.0	-40.9	-10
2350 MHz	21.6	22.6	8.6	-40.0	-22
2400 MHz	20.7	21.0	8.3	-40.1	-9

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 90\text{ mA}$, $P_{out} = 1.26\text{ W Avg.}$, $f = 2170\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	20.0	21.7	—	dB
Drain Efficiency	η_D	18.5	21.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-40.6	-37.9	dBc
Input Return Loss	IRL	—	-14	-9	dB

Load Mismatch (In Freescale Test Fixture, 50 ohm system) $I_{DQ} = 90\text{ mA}$, $f = 2140\text{ MHz}$

VSWR 5:1 at 32 Vdc, 13.9 W CW Output Power (3 dB Input Overdrive from 10 W CW Rated Power)	No Device Degradation
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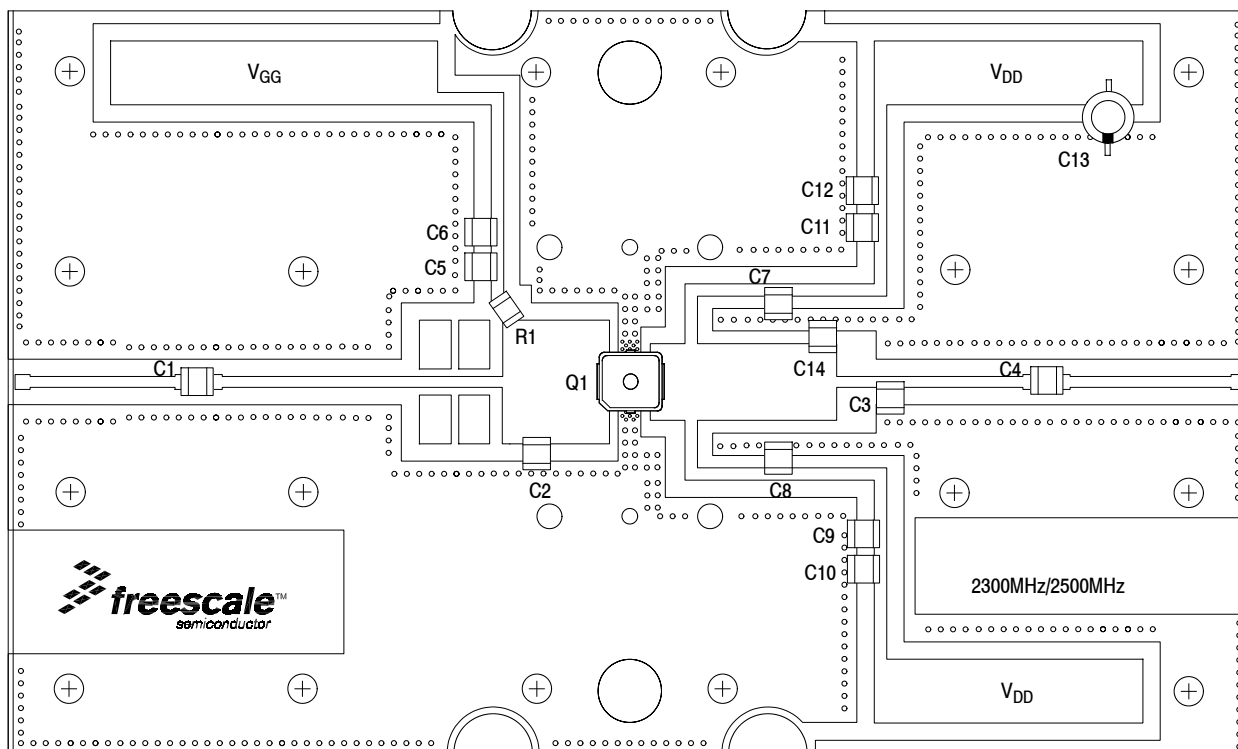
Typical Performance ⁽¹⁾ (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 90\text{ mA}$, 2110–2170 MHz Bandwidth

P_{out} @ 1 dB Compression Point, CW	P_{1dB}	—	10	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz frequency range.)	Φ	—	-12.6	—	$^\circ$
VBW Resonance Point (IMD Seventh Order Intermodulation Inflection Point)	VBW_{res}	—	120	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 1.26\text{ W Avg.}$	G_F	—	0.20	—	dB
Gain Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔG	—	0.011	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔP_{1dB}	—	0.004	—	dB/ $^\circ\text{C}$

Table 6. Ordering Information

Device	Tape and Reel Information	Package
MHT1006NT1	T1 Suffix = 1000 Units, 16 mm Tape Width, 7-inch Reel	PLD-1.5W

1. All data measured in fixture with device soldered to heatsink.



NOTE: All data measured in fixture with device soldered to heatsink.

Figure 2. MHT1006NT1 Test Circuit Component Layout — 2300–2400 MHz

Table 7. MHT1006NT1 Test Circuit Component Designations and Values — 2300–2400 MHz

Part	Description	Part Number	Manufacturer
C1, C4, C5, C7, C8	6.8 pF Chip Capacitors	ATC100B6R8JT500XT	ATC
C2, C14	1 pF Chip Capacitors	ATC100B1R0JT500XT	ATC
C3	1.2 pF Chip Capacitor	ATC100B1R2JT500XT	ATC
C6, C9, C10, C11, C12	10 μ F Chip Capacitors	GRM32ER61H106KA12L	Murata
C13	220 μ F, 50 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
Q1	RF Power LDMOS Transistor	MHT1006NT1	Freescale
R1	4.75 Ω , Chip Resistor	CRCW12064R75FKEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	—	MTL

TYPICAL CHARACTERISTICS — 2300–2400 MHz

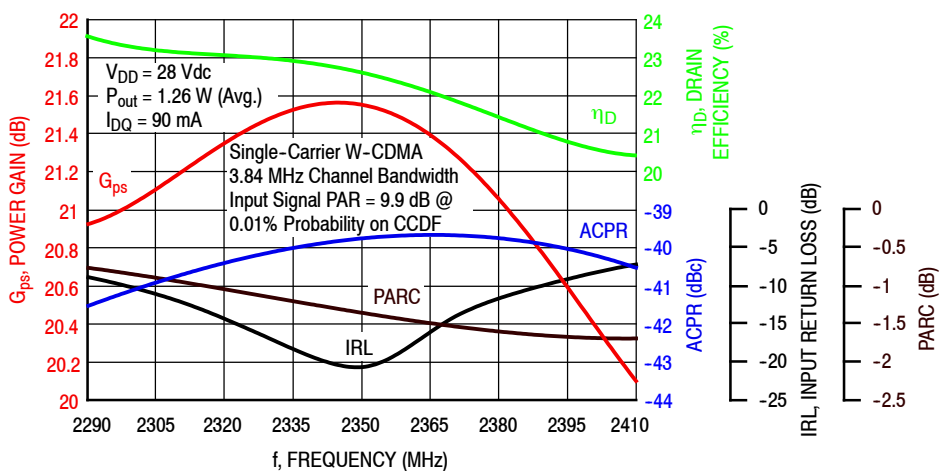


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 1.26$ W Avg.

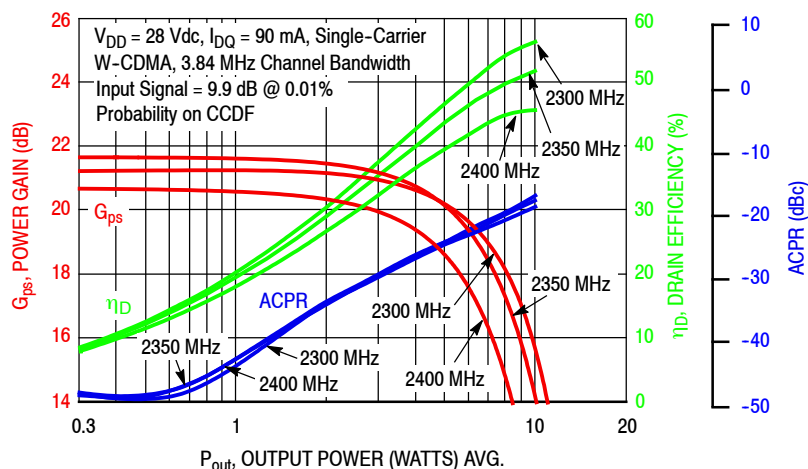


Figure 4. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

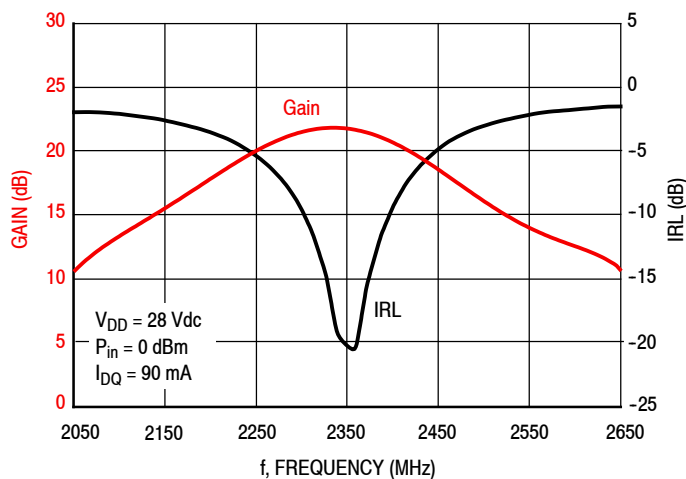


Figure 5. Broadband Frequency Response

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 87 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	1.12 - j1.10	0.995 + j1.38	5.39 + j2.23	20.1	40.9	12	55.9	-12
2400	1.06 - j1.59	0.948 + j1.96	5.09 + j1.86	19.8	40.9	12	55.1	-12
2500	1.00 - j1.60	1.29 + j1.95	4.51 + j1.56	19.2	40.8	12	55.8	-10
2600	0.985 - j3.50	0.743 + j3.66	4.81 + j1.10	19.0	41.3	13	56.2	-14
2690	1.10 - j3.13	1.48 + j2.98	4.14 + j0.987	19.0	41.0	13	57.5	-12

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	1.12 - j1.10	0.919 + j1.64	6.28 + j1.74	17.8	41.7	15	55.0	-19
2400	1.06 - j1.59	0.861 + j2.23	5.86 + j1.41	17.5	41.7	15	54.4	-19
2500	1.00 - j1.60	1.37 + j2.32	5.40 + j1.17	16.9	41.7	15	55.8	-17
2600	0.985 - j3.50	0.579 + j3.82	5.37 + j0.912	16.9	42.0	16	55.8	-22
2690	1.10 - j3.13	1.74 + j3.43	5.04 + j0.759	16.8	41.8	15	57.1	-18

(1) Load impedance for optimum P1dB power. (2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 6. Load Pull Performance — Maximum Power Tuning

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 87 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	1.12 - j1.10	0.855 + j1.22	3.36 + j4.23	21.6	39.8	9	61.9	-20
2400	1.06 - j1.59	0.829 + j1.80	3.34 + j3.53	21.2	39.9	10	60.4	-19
2500	1.00 - j1.60	1.04 + j1.82	3.21 + j3.00	20.8	40.0	10	61.1	-16
2600	0.985 - j3.50	0.709 + j3.49	3.17 + j2.53	20.0	40.5	11	60.7	-20
2690	1.10 - j3.13	1.14 + j2.91	2.87 + j2.16	20.4	40.2	10	62.0	-18

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	1.12 - j1.10	0.803 + j1.51	3.96 + j4.10	19.4	40.7	12	61.1	-27
2400	1.06 - j1.59	0.757 + j2.07	3.70 + j3.45	19.1	40.6	12	59.8	-27
2500	1.00 - j1.60	1.15 + j2.18	3.58 + j2.94	18.7	40.8	12	61.2	-24
2600	0.985 - j3.50	0.556 + j3.73	4.15 + j2.29	17.8	41.5	14	59.7	-26
2690	1.10 - j3.13	1.43 + j3.33	3.40 + j2.01	18.2	41.1	13	61.7	-25

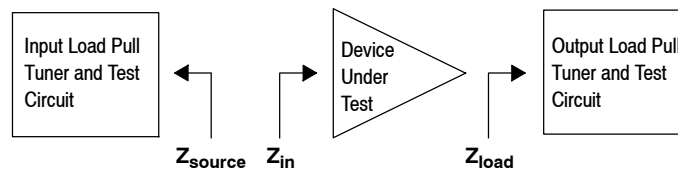
(1) Load impedance for optimum P1dB efficiency. (2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 7. Load Pull Performance — Maximum Drain Efficiency Tuning



P1dB - TYPICAL LOAD PULL CONTOURS — 2500 MHz

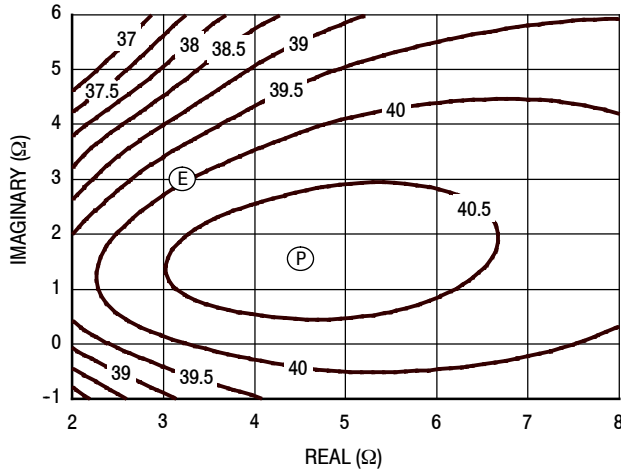


Figure 8. P1dB Load Pull Output Power Contours (dBm)

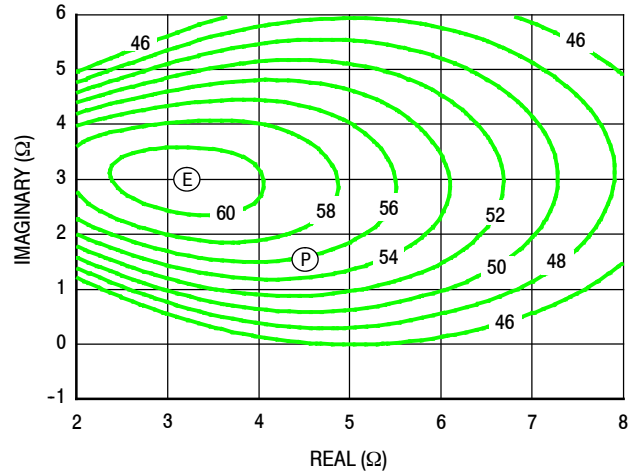


Figure 9. P1dB Load Pull Efficiency Contours (%)

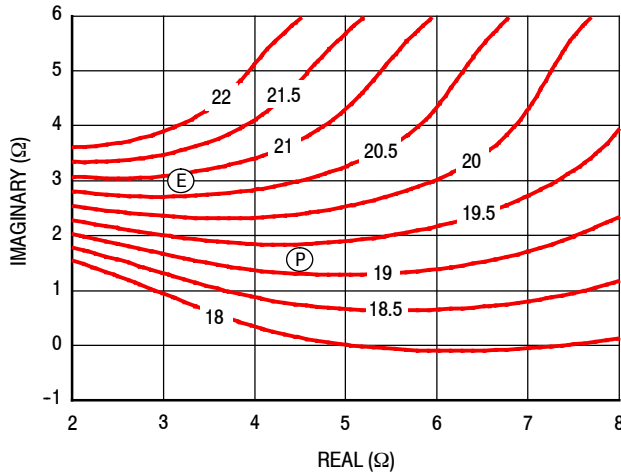


Figure 10. P1dB Load Pull Gain Contours (dB)

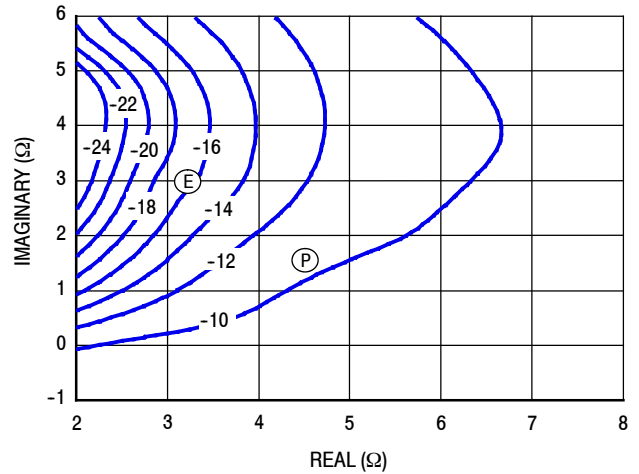


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 2500 MHz

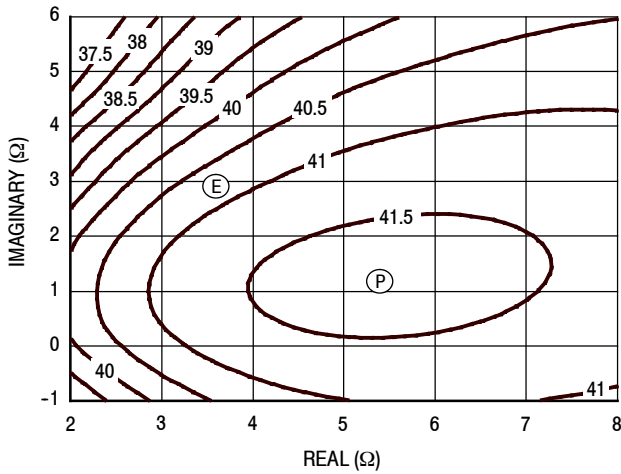


Figure 12. P3dB Load Pull Output Power Contours (dBm)

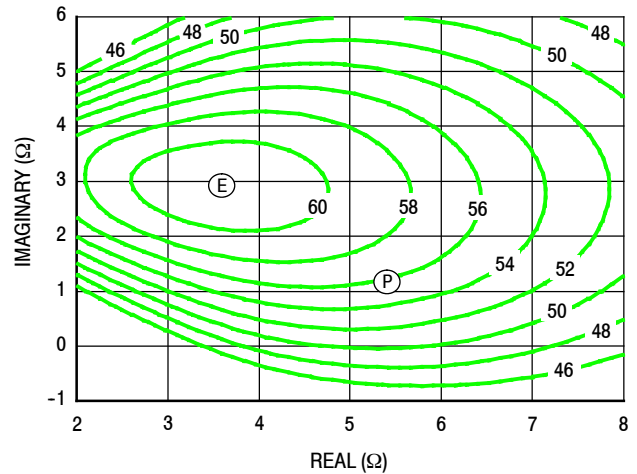


Figure 13. P3dB Load Pull Efficiency Contours (%)

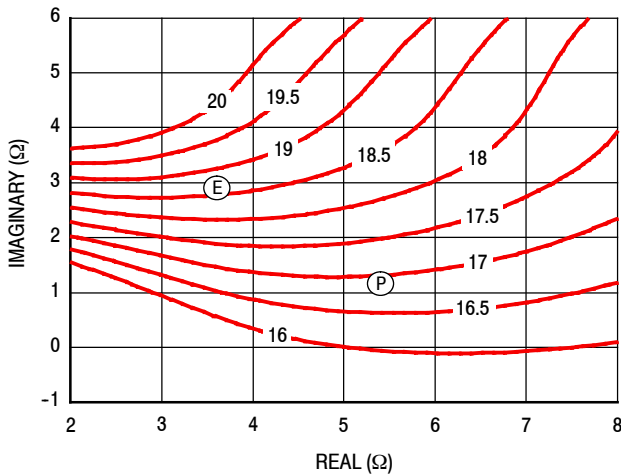


Figure 14. P3dB Load Pull Gain Contours (dB)

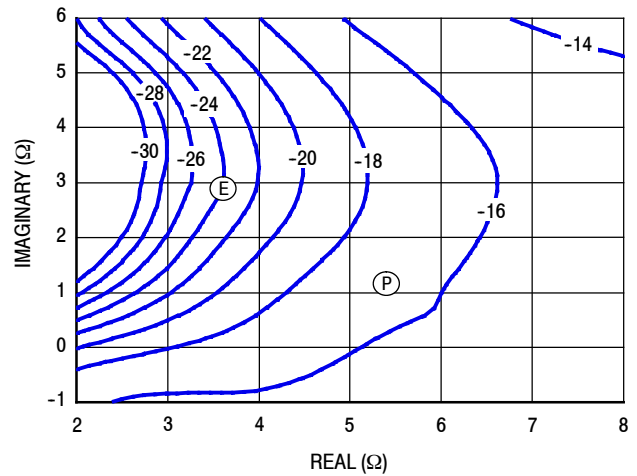


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

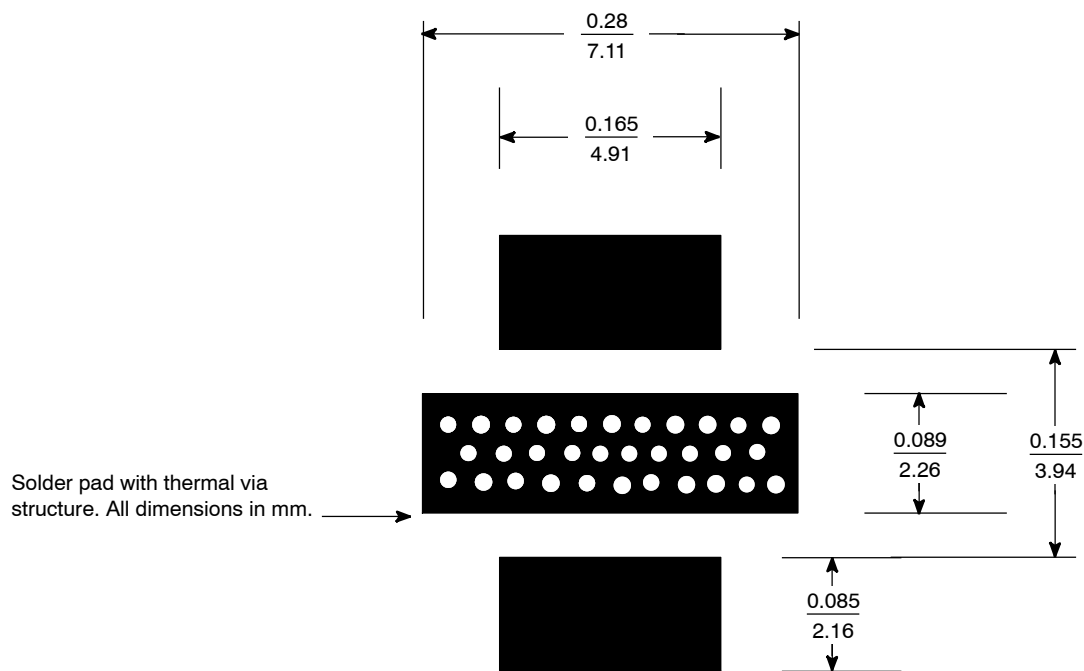


Figure 16. PCB Pad Layout for PLD-1.5W

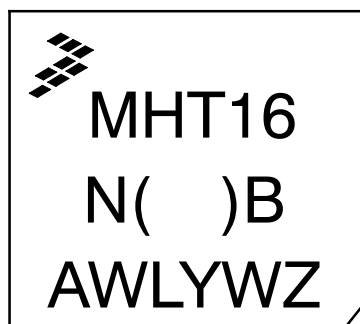
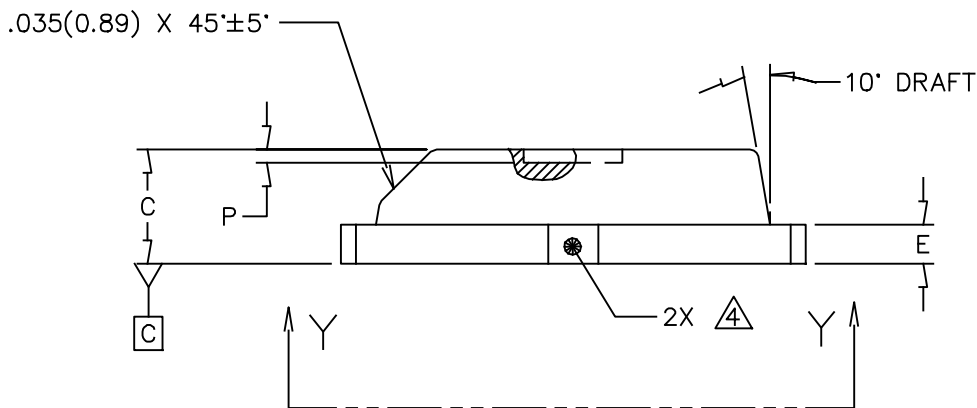
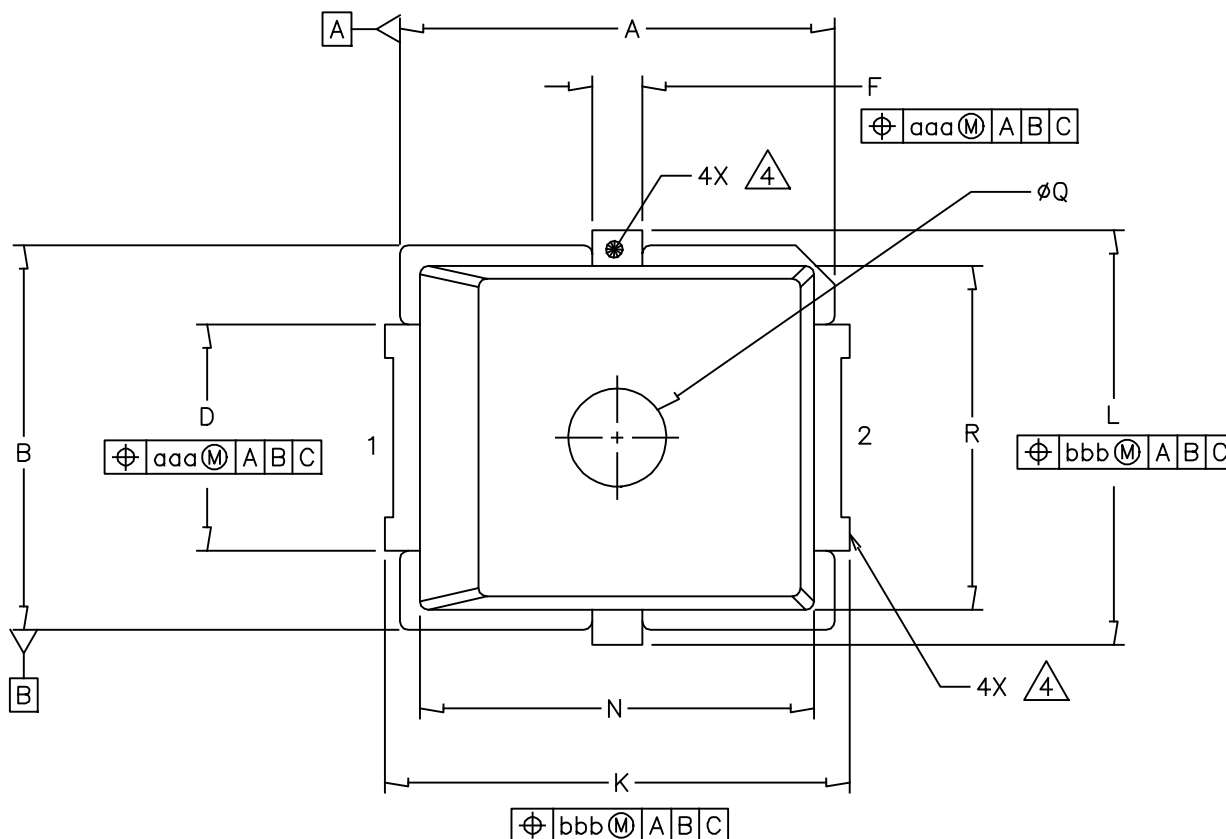
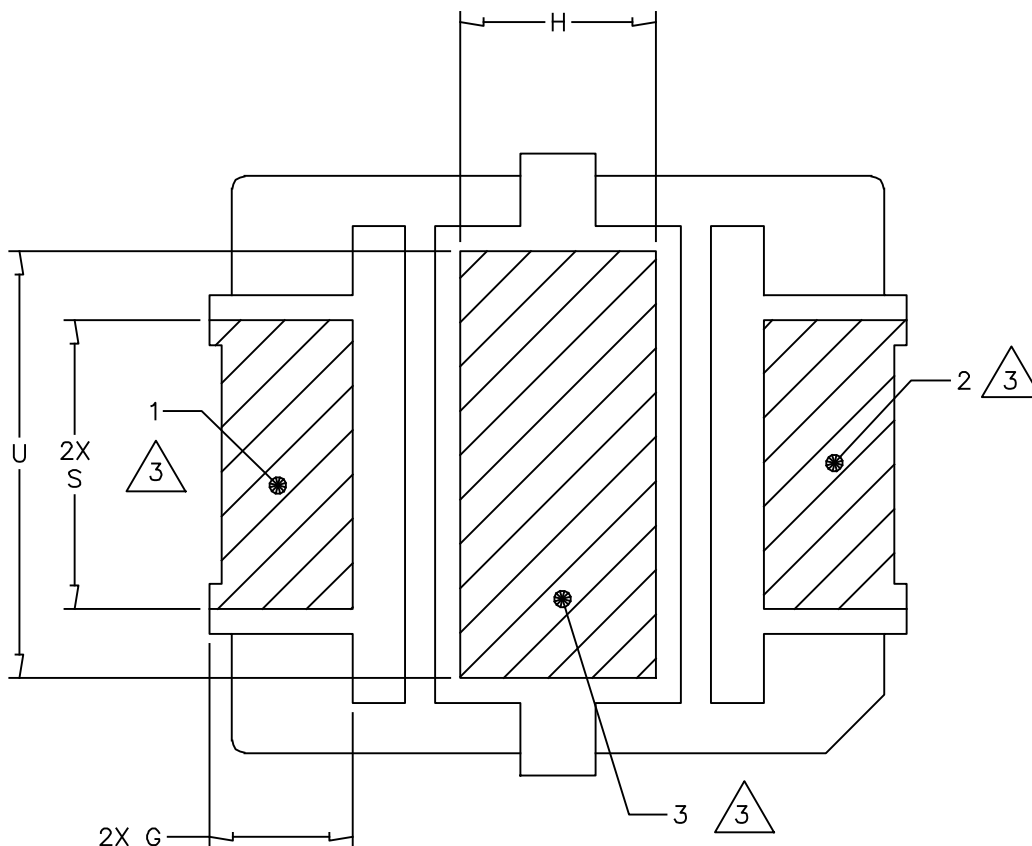


Figure 17. Product Marking

PACKAGE DIMENSIONS



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TITLE: PLD-1.5W		DOCUMENT NO: 98ASA00476D		REV: 0	
		CASE NUMBER: 2297-01		14 JUN 2012	
		STANDARD: NON-JEDEC			



VIEW Y-Y

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TITLE: PLD-1.5W	DOCUMENT NO: 98ASA00476D	REV: 0	
	CASE NUMBER: 2297-01	14 JUN 2012	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA. DIMENSIONS G, S, H AND U REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA.

4. THESE SURFACES ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.255	.265	6.48	6.73	Q	.055	.063	1.40	1.60
B	.225	.235	5.72	5.97	R	.200	.210	5.08	5.33
C	.065	.072	1.65	1.83	S	.110	—	2.79	—
D	.130	.150	3.30	3.81	U	.156	—	3.96	—
E	.021	.026	0.53	0.66	aaa		.004		0.10
F	.026	.044	0.66	1.12	bbb		.005		0.13
G	.038	—	0.97	—					
H	.069	—	1.75	—					
J	.160	.180	4.06	4.57					
K	.273	.285	6.93	7.24					
L	.245	.255	6.22	6.48					
N	.230	.240	5.84	6.10					
P	.000	.008	0.00	0.20					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: PLD-1.5W					DOCUMENT NO: 98ASA00476D			REV: 0	
					CASE NUMBER: 2297-01			14 JUN 2012	
					STANDARD: NON-JEDEC				

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator

For Software, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

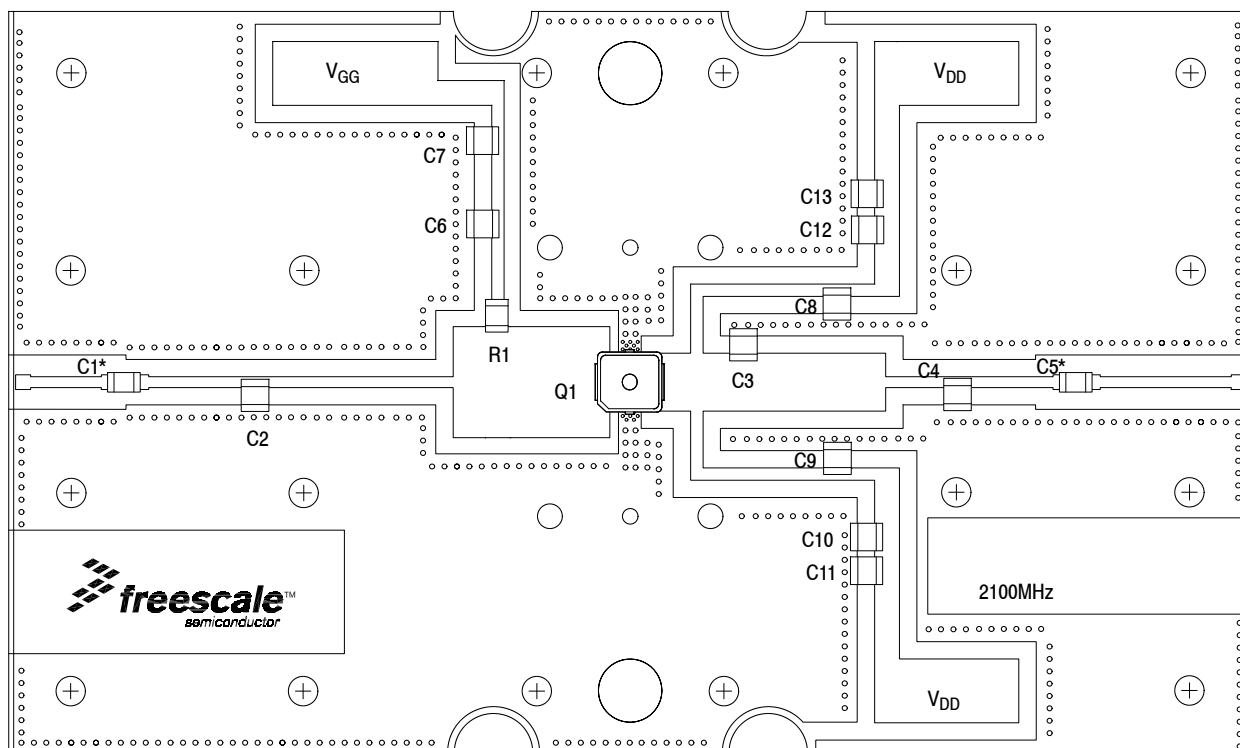
The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2014	<ul style="list-style-type: none"> • Initial Release of Data Sheet
1	Dec. 2015	<ul style="list-style-type: none"> • Table 1, Maximum Ratings: corrected operating junction temperature range upper limit, p. 2 • Table 5, Electrical Characteristics, On Characteristics $V_{DS(on)}$: updated I_D unit of measure to mA_{dc} to reflect actual unit of measure, p. 2 • Added Ordering Information Table 6, p. 3

APPENDIX A: 2110–2170 MHz TYPICAL PERFORMANCE DATA, LAYOUT AND PARTS LIST

Typical Performance over Frequency ⁽¹⁾ (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28$ Vdc, $I_{DQ} = 90$ mA, $P_{out} = 1.26$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	21.6	23.2	9.1	-42.0	-11
2140 MHz	21.8	23.0	9.0	-41.5	-15
2170 MHz	21.7	22.6	8.7	-41.7	-15



*C1 and C5 are mounted vertically.

1. All data measured in fixture with device soldered to heatsink.

Figure A-1. MHT1006NT1 Test Circuit Component Layout — 2110–2170 MHz

Table A-1. MHT1006NT1 Test Circuit Component Designations and Values — 2110–2170 MHz

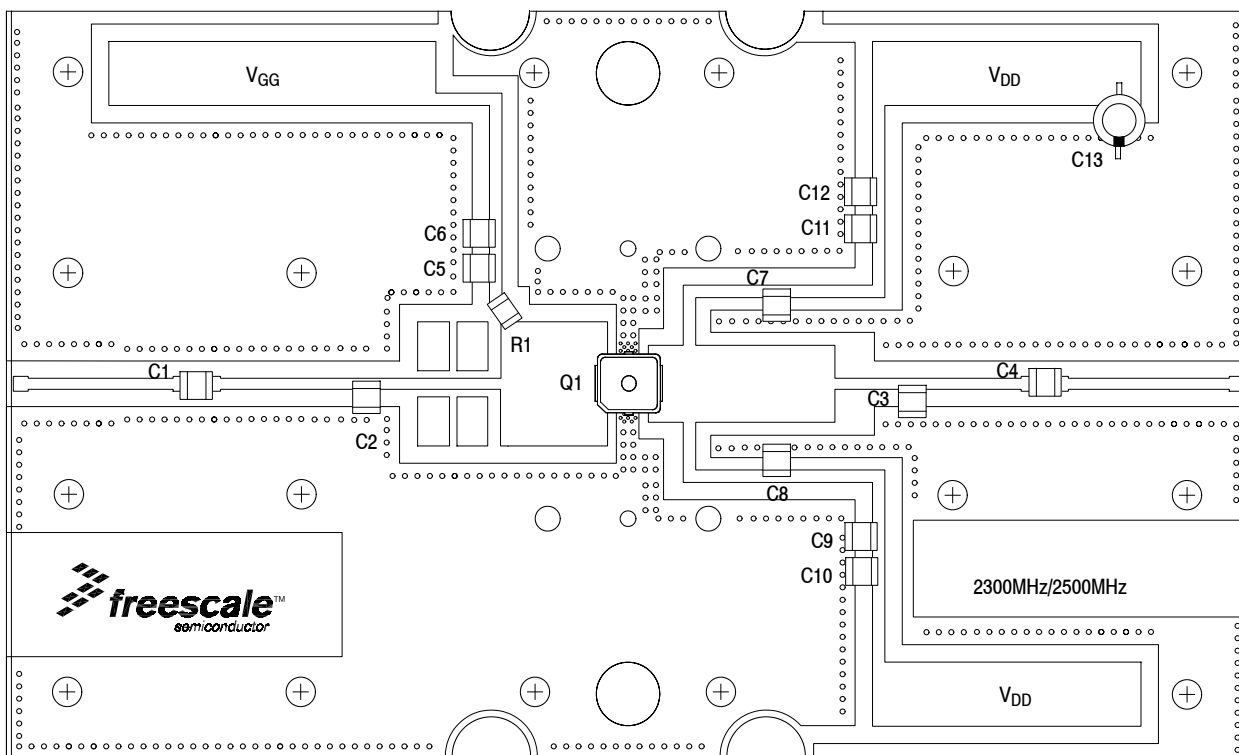
Part	Description	Part Number	Manufacturer
C1, C5, C6, C8, C9	9.1 pF Chip Capacitors	ATC100B9R1JT500XT	ATC
C2	1.1 pF Chip Capacitor	ATC100B1R1JT500XT	ATC
C3	2.0 pF Chip Capacitor	ATC100B2R0JT500XT	ATC
C4	1.0 pF Chip Capacitor	ATC100B1R0JT500XT	ATC
C7, C10, C11, C12, C13	10 μ F Chip Capacitors	GRM32ER61H106KA12L	Murata
Q1	RF Power LDMOS Transistor	MHT1006NT1	Freescale
R1	2.37 Ω Chip Resistor	CRCW12062R37FKEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	—	MTL

APPENDIX B: 2500–2700 MHz

TYPICAL PERFORMANCE DATA AND GRAPHS, LAYOUT AND PARTS LIST

Typical Performance over Frequency ⁽¹⁾ (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28$ Vdc, $I_{DQ} = 90$ mA, $P_{out} = 1.26$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2500 MHz	19.6	22.0	9.8	-44.8	-7
2600 MHz	21.0	22.7	9.4	-41.4	-15
2700 MHz	19.6	21.2	8.9	-39.7	-5



1. All data measured in fixture with device soldered to heatsink.

Figure B-1. MHT1006NT1 Test Circuit Component Layout — 2500–2700 MHz

Table B-1. MHT1006NT1 Test Circuit Component Designations and Values — 2500–2700 MHz

Part	Description	Part Number	Manufacturer
C1, C4, C5, C7, C8	6.8 pF Chip Capacitors	ATC100B6R8JT500XT	ATC
C2	1.2 pF Chip Capacitor	ATC100B1R2JT500XT	ATC
C3	1 pF Chip Capacitor	ATC100B1R0JT500XT	ATC
C6, C9, C10, C11, C12	10 μ F Chip Capacitors	GRM32ER61H106KA12L	Murata
C13	220 μ F, 50 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
Q1	RF Power LDMOS Transistor	MHT1006NT1	Freescale
R1	4.75 Ω Chip Resistor	CRCW12064R75FKEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	—	MTL

TYPICAL CHARACTERISTICS — 2500–2700 MHz

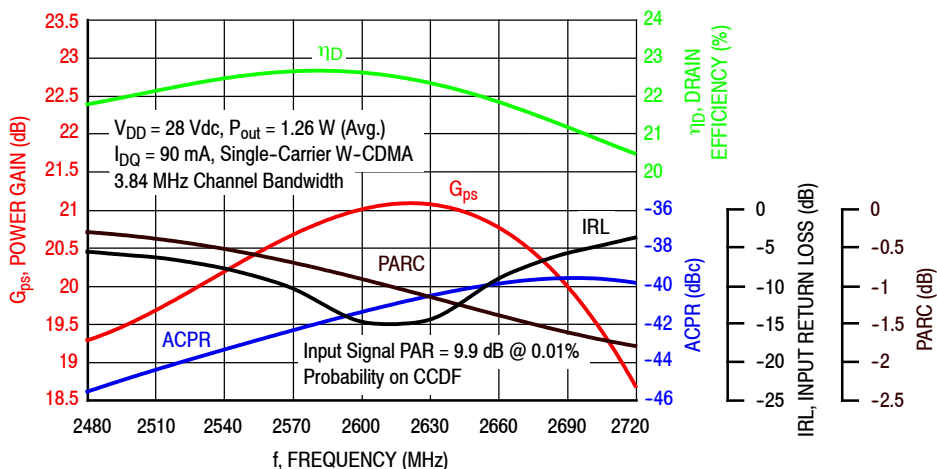


Figure B-2. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 1.26$ W Avg.

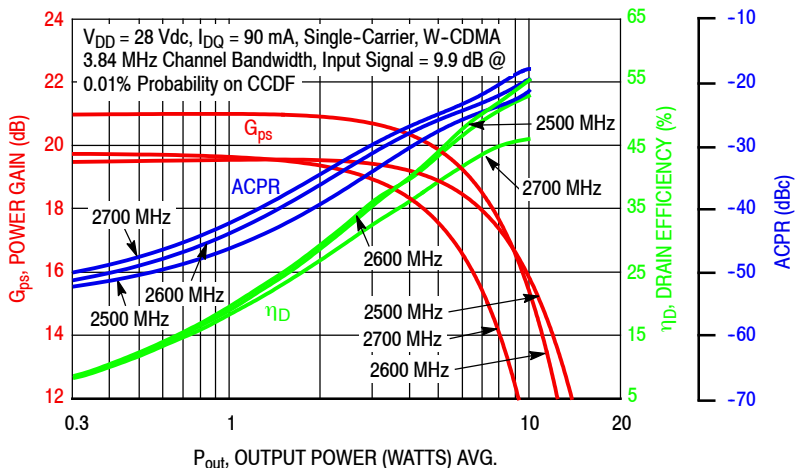


Figure B-3. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

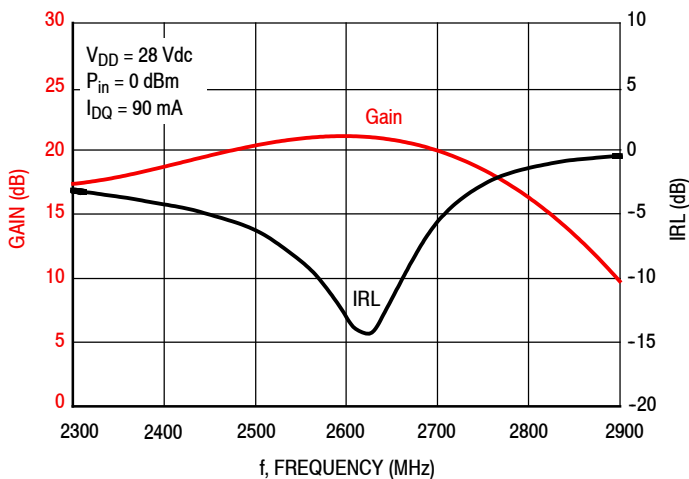


Figure B-4. Broadband Frequency Response

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