



# THE DATASHEET OF SL4275



## 1. Function Description

The SL4275 is a monolithically integrated low-dropout fixed voltage regulator in a 5-pin TO package. Input voltages up to 55V are regulated to an output voltage V<sub>Q</sub> of 5.0V. The chip can drive 450mA load and has short circuit protection and over temperature protection. When the output voltage V<sub>Q</sub> is lower than the typical value of 4.65V, the R<sub>Q</sub> pin of the chip will generate a low-level reset signal, and the reset delay time can be set by the D pin delay capacitor.

### 1.1, External component information

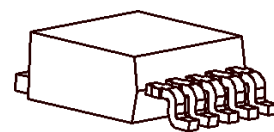
The SL4275 requires an input capacitor C<sub>I</sub> to compensate for trace effects. In order to ensure the stability of the regulation circuit, the output capacitor C<sub>O</sub> is necessary. Output capacitors with C<sub>O</sub> ≥ 22uF and ESR ≤ 5Ω guarantee stability over the operating temperature range.

### 1.2. Circuit description

The control op amp compares the reference voltage with a voltage proportional to the output voltage and drives the gate of the series MOS transistor through a buffer. In addition, a current-limiting control unit for the load current prevents oversaturation of the power components. The chip also integrates many internal circuits for overload, over-temperature, and other protections.

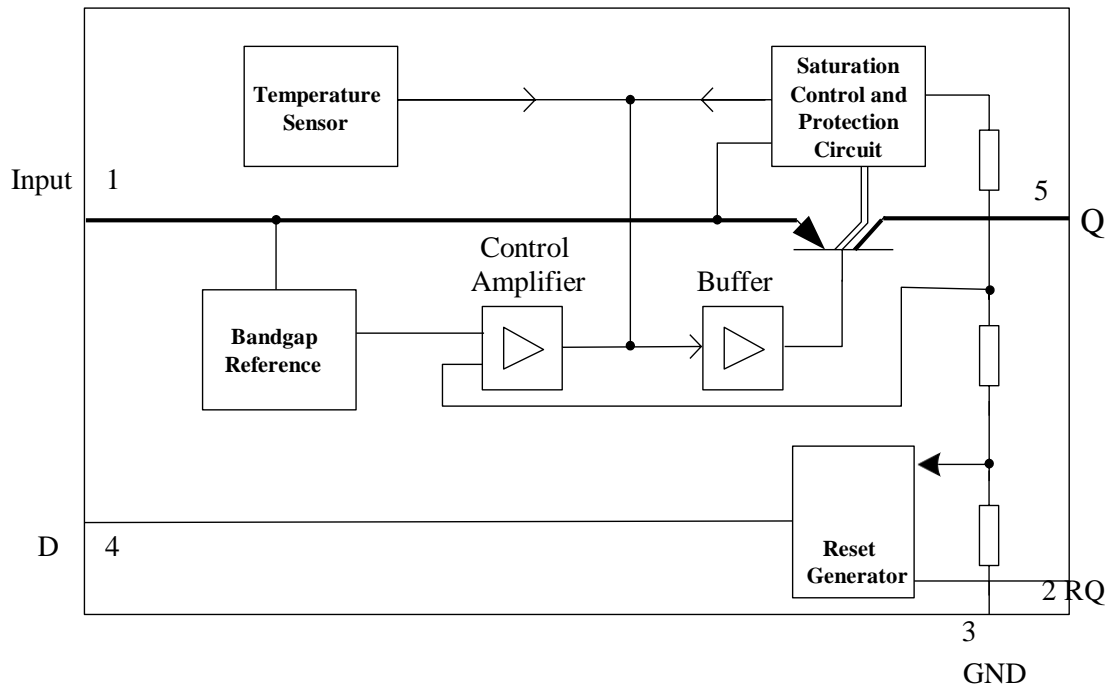
### 1.3. Features

- Rated output voltage 5V, accuracy range ±2%
- Ultra-low power consumption: 80uA
- Power-on and Brown-out Reset
- Low drop
- Short circuit protection
- RoHS



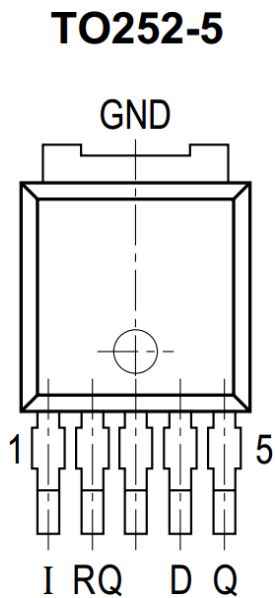
TO252-5

**2. Principle block diagram**



**Figure 2-1 Module block diagram**

**3. Definitions of pins**



**Figure 3-1 Pin configuration (top view)**

**Table 3.1 Pin definition and functions**

No. of pin	Symbol	Function
1	I	<b>Input:</b> Use a ceramic capacitor to ground directly near the IC side.
2	RQ	<b>Reset output:</b> Open-drain output pin requires an external pull-up resistor. When the output voltage is lower than the reset threshold VRT, RQ is pulled low; it can be floated when not in use.
3	GND	<b>Ground:</b> Connect to the cooling fin in the device
4	D	<b>Reset delay</b> Connect the capacitor to ground to set the reset delay time; it can be left floating when not in use.
5	Q	<b>Output:</b> Use a capacitor with $CQ \geq 22\mu F$ and $ESR < 5\Omega$ at 10KHz to connect to ground.

## 4. General product characteristics

**Table 4.1 Absolute Maximum Ratings**

$T_j = -40^\circ C$  to  $150^\circ C$ . All the voltage values are relative to ground unless otherwise specified.

Parameters	Symbols	Limiting value		Unit	Note
		Min	Max		
Input Voltage	VI	-0.3	60	V	
Output voltage	VQ	-0.3	12	V	
Reset output	RQ	-0.3	36	V	
Reset delay	D	-0.3	12	V	
Temperature	Tj	-40	150	°C	Junction temperature
	Tstg	-40	150	°C	Storage temperature
ESD withstanding voltage	VESD-HBM	-2000	2000	V	Human body mode <sup>1)</sup>
	VESD-CDM	-1000	1000	V	Enabling equipment model <sup>2)</sup>

1) The ESD withstanding voltage human body model is designed according to JESD22-A114.

2) ESD withstanding voltage equipment model is designed according to JESD22-C101E.

**Table 4.2 Thermal Resistance**

Parameters	Symbols	Limiting value			Unit	Conditions
		Min	Type	Max		

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Junction-to-Case Thermal Resistance	RthJC		3.6		K/W	Measurement of the cooling foundation
Junction to ambient thermal resistance	RthJA		27		K/W	
			115		K/W	Only pin
			52		K/W	Cooling fin of 300mm <sup>2</sup>
			42		K/W	Cooling fin of 600mm <sup>2</sup>

1) It does not refer to production testing, but specially refers to design;

## 5 Electrical Characteristics

**Table5.1 Electrical Characteristics**
 $V_I = 13.5V$ ;  $-40^{\circ}C \leq T_j \leq 150^{\circ}C$ , unless otherwise specified.

Parameters	Symbols	Parameter values			Unit	Testing conditions
		Min	Type	Max		
Working voltage	$V_I$	5.5	13.5	55	V	
Output voltage	$V_Q$	4.9	5.0	5.1	V	$I_Q < 450m$ ; $V_I < 55V$
Output current limiting	$I_Q$	450	800		mA	$V_I = 13.5V$
Quiescent current	$I_{q1}$		80	100	uA	$I_Q = 5mA$
Quiescent current	$I_{q2}$		130	160	uA	$I_Q = 400mA$
Voltage difference	$V_{dr}$		0.3	0.5	V	$I_Q = 300mA$
Load regulation ratio	$\Delta V_{QLo}$		33	50	mV	$5mA < I_Q < 450mA$
Linear adjustment rate	$\Delta V_{QLi}$		2	10	mV	$8V < V_I < 55V, I_Q = 5mA$
Power supply rejection ratio	PSRR		70		dB	100HZ@0.5Vpp
Output Capacitance	$C_Q$	1			uF	$ESR \leq 5\Omega @ 10KHZ$

**Reset output RQ:**

Reset threshold	$V_{RT}$	4.5	4.65	4.8	V	output voltage drop
Reset hysteresis	$V_{hys}$		0.2		V	
Reset response time	$t_{rr}$			2	us	
Reset output low voltage	$V_{RQL}$			0.4	V	$R_{ext} \geq 5K\Omega$ ; $V_Q < V_{RT}$
Reset output leakage current	$I_{RQ}$		0	1	uA	$V_{RQ} = 5V$

**Reset delay D:**

Upper trigger threshold	$V_{DT}$		1.8		V	
Lower trigger threshold	$V_{DL}$	0.2	0.4	0.6	V	
Delay capacitor charging current	$I_{Charge}$	3	6	9	uA	$V_D = 0V$
Reset delay time	$t_{rd}$	10	15	20	ms	$C_D = 47nF$
	$t_{rd}$		8		us	No capacitors on pins

1) Dropout voltage=  $V_I - V_Q$  ( $V_I - V_Q$  when  $V_Q$  drops 100mV from the rated output voltage value at  $V_I = 13.5V$ ).

## 6. Reset function

### 6.1. Reset threshold ( $V_{RT}$ )

RQ must be connected to an external pull-up resistor. After the chip starts, when the output voltage VQ is lower than VRT, the chip will pull down the reset output pin RQ internally.

When the chip output is shorted to ground, the chip is thermally shut down, or the power supply is under-voltage, this function can feed back a reset low level signal to the MCU.

### 6.2. Reset response time ( $t_{rr}$ )

When the output voltage VQ drops below VRT, after  $t_{rr}$  time, RQ will be set low;

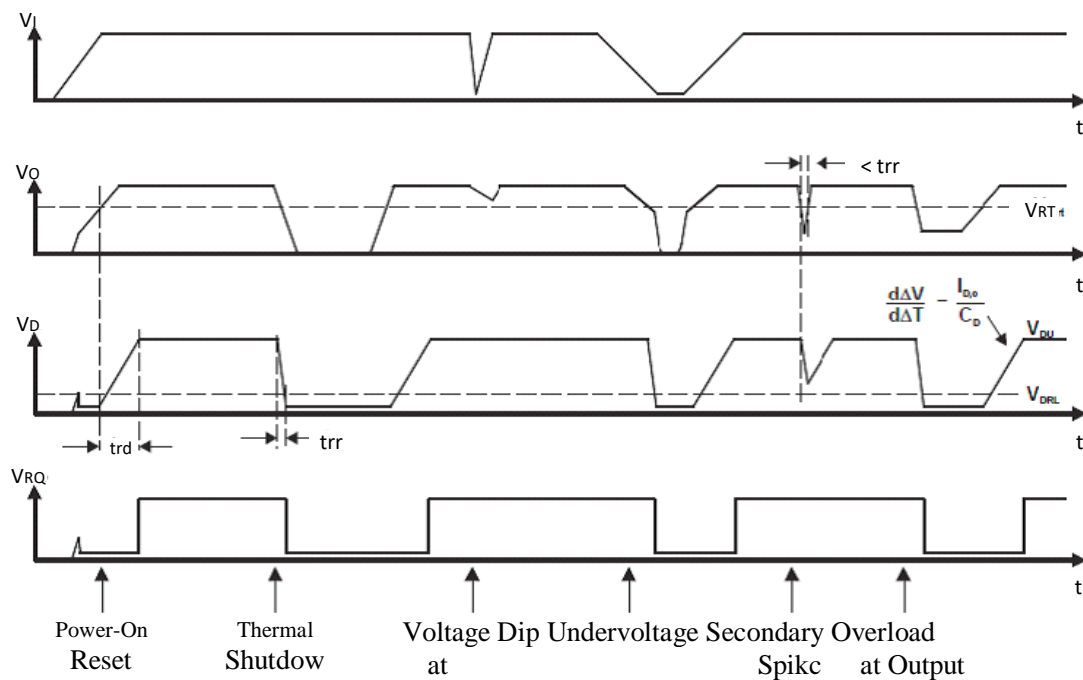
### 6.3. Reset delay time ( $t_{rd}$ )

Before the reset pin (RQ) is set high, connect an external capacitor to the reset delay pin (D). At this time, the D pin will output a constant current (about 6uA) to continuously charge the external capacitor. Until the voltage of pin D exceeds the upper trigger threshold VDT of the internal comparator, at this time RQ will be set high;

If this pin is left floating, the default reset delay time is about 8us.

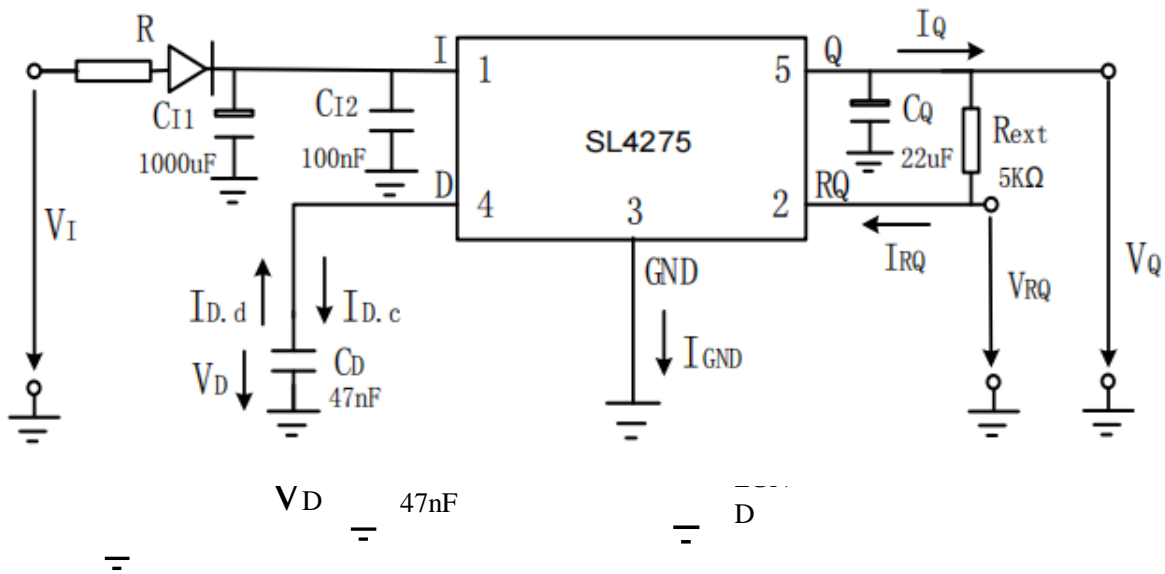
The reset delay time  $t_{rd}$  is determined by the external capacitor charging time:

$$t_{rd} = \frac{C_D * 1.8V}{6\mu A}$$



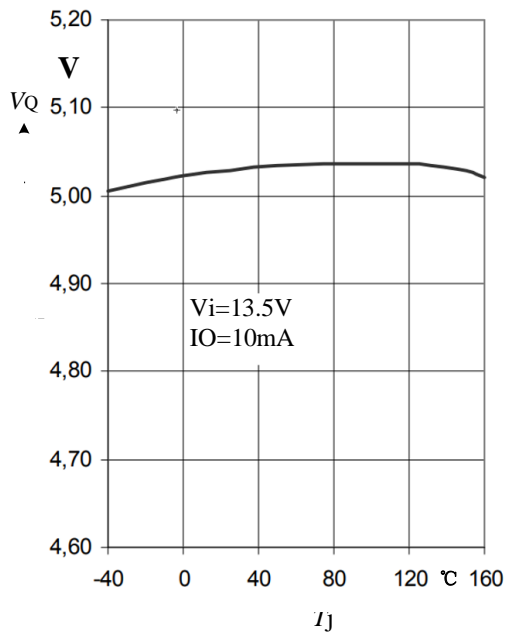
**Figure6-1 Reset Timing**

**7. Applications Information**

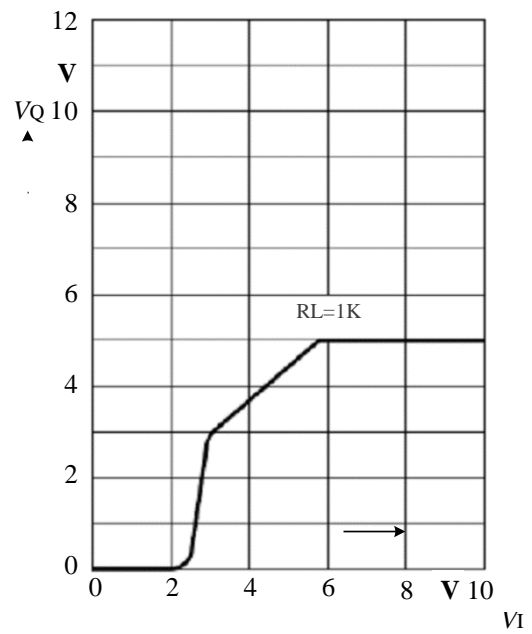


**Figure 7-1 application circuit**

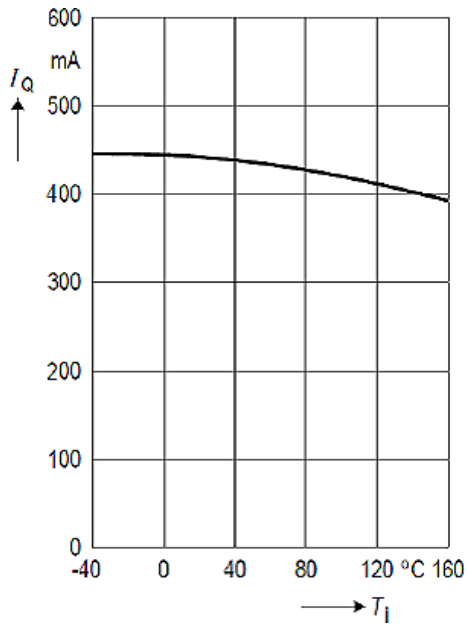
**8. Typical characteristic curve**



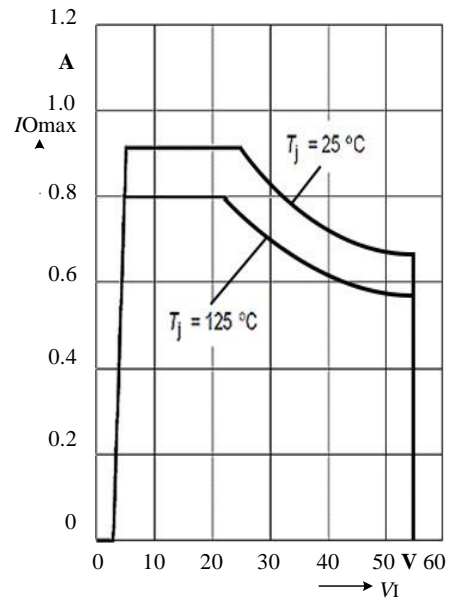
**Figure 8-1-output voltage VS Junction temperature**



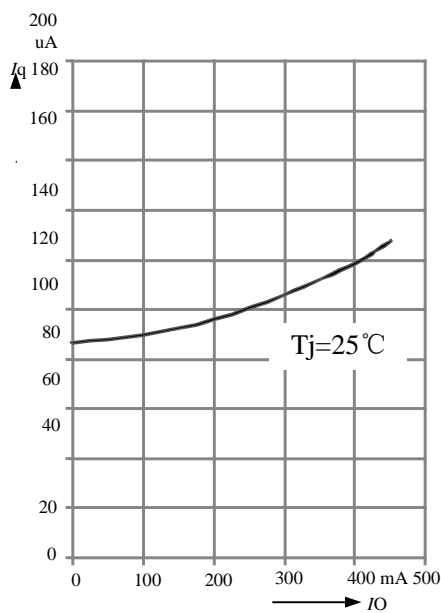
**Figure 8-2 Output Voltage VS Input Voltage**



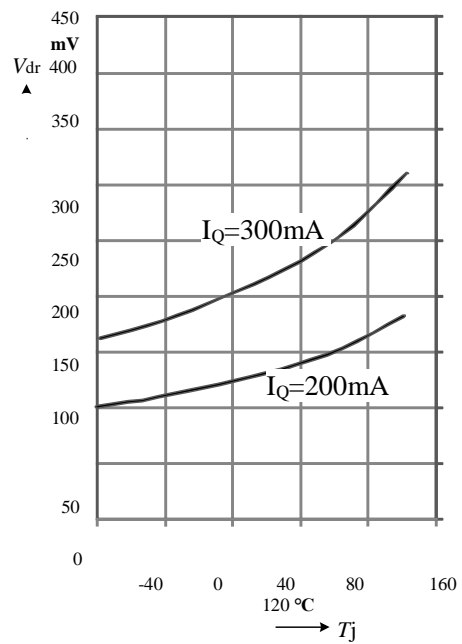
**Figure 8-3** output voltage VS Junction temperature



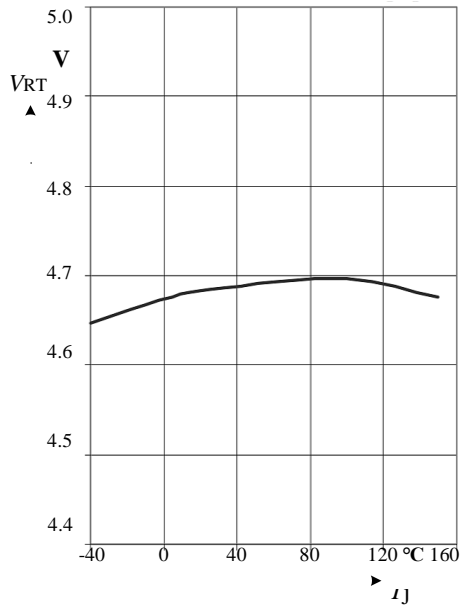
**Figure 8-4** Output Current Limit VS Input Voltage



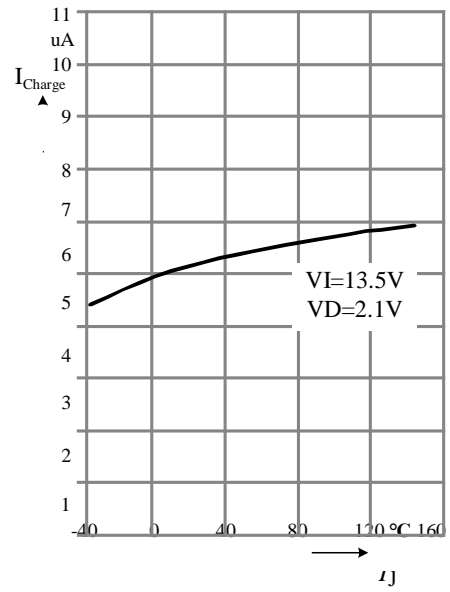
**Figure 8-5** Quiescent Current VS Output Current



**Figure 8-6** Voltage difference VS Junction Temperature



**Figure 8-7 Reset Threshold Junction Temperature**



**Figure 8-8 Reset Delay Charge Current VS Junction Temperature**

### 9. Package dimension

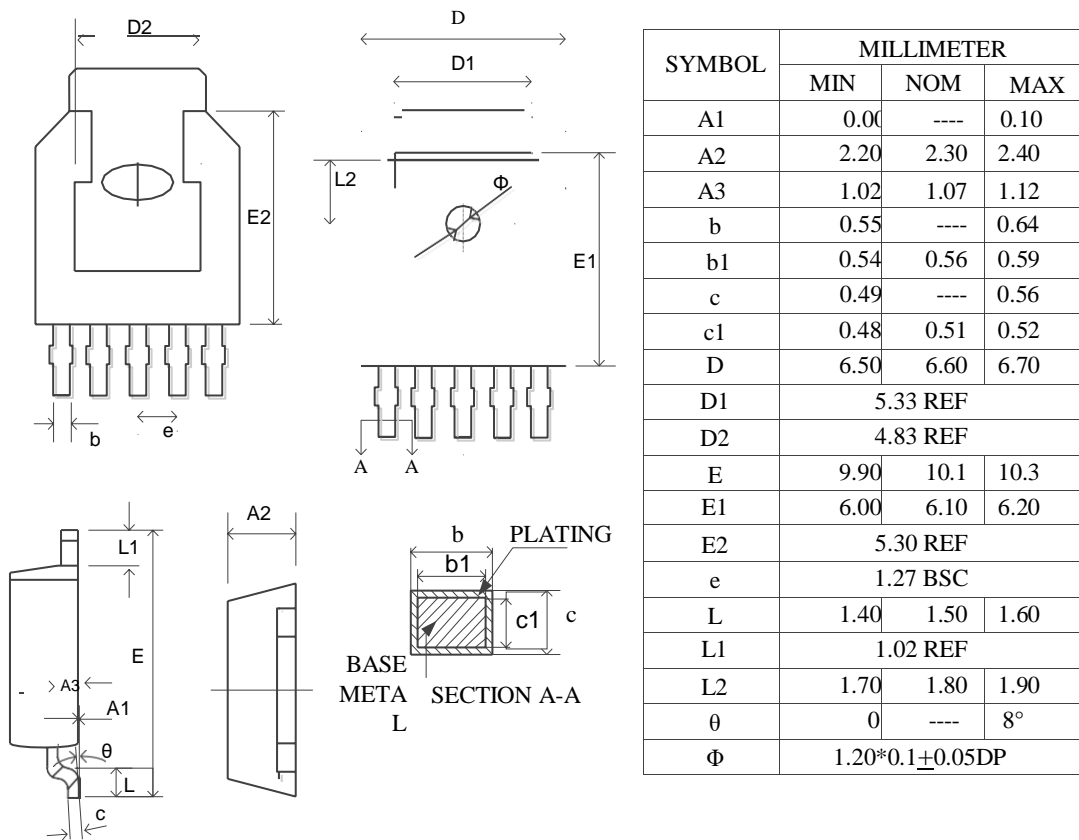


Figure 9-1 TO252-3 Package

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