THE DATASHEET OF

MPM3683GMN-10-T

MPM3683-10

2.7V to 16V, 10A, Step-Down Power Module

DESCRIPTION

The MPM3683-10 is an easy-to-use, fully integrated, DC/DC step-down power module, with 10A of continuous output current (I_{OUT}). The MPM3683-10 integrates a DC/DC converter, power inductor, and passive components. It can deliver I_{OUT} across a wide input voltage (V_{IN}) supply range, with excellent load and line regulation.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. The operating switching frequency (f_{SW}) can be easily set to 600kHz, 800kHz, or 1000kHz using the MODE configuration. This allows the MPM3683-10's f_{SW} to remain constant regardless of V_{IN} and the output voltage (V_{OUT}).

The MPM3683-10 features a configurable soft-start time (t_{SS}) with a capacitor. An open-drain power good (PG) signal indicates whether V_{OUT} is within the nominal voltage range.

Fully integrated, non-latched protections include over-current protection (OCP), over-voltage protection (OVP), and over-temperature protection (OTP).

The MPM3683-10 is available in a compact FCM LGA-29 (7mmx7mmx4.4mm) package.

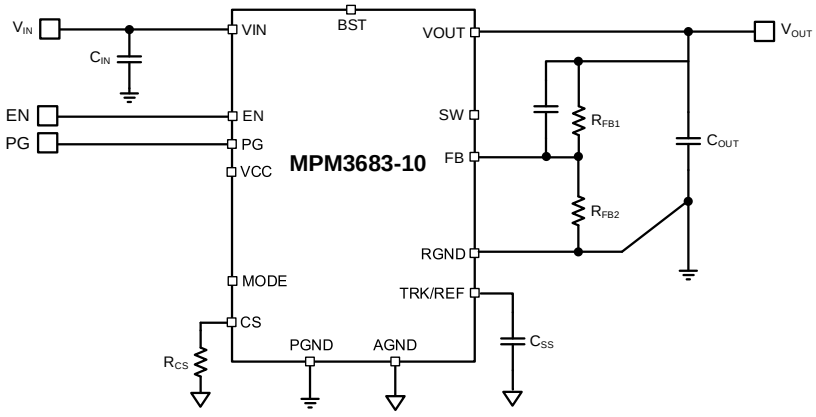
FEATURES

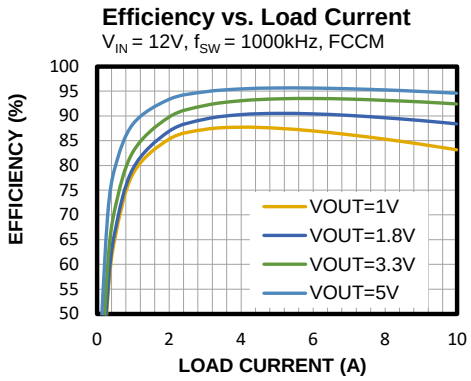
- Wide Input Voltage (V_{IN}) Range
  - 2.7V to 16V with External 3.3V Bias
  - 4V to 16V with Internal Bias or External 3.3V Bias
- Output Voltage (V_{OUT}) Range: 0.6V to 5.5V
- Differential V_{OUT} Remote Sense
- Adaptive Constant-On-Time (COT) for Ultra-Fast Transient Response
- Stable with Zero-ESR Output Capacitor (C_{OUT})
- Selectable Pulse-Skip Mode (PSM) or Forced Continuous Conduction Mode (FCCM)
- V_{OUT} Tracking
- V_{OUT} Discharge
- Power Good (PG) Active Clamped Low during Power Failure
- Configurable Soft-Start Time (t_{SS})
- Pre-Biased Start-Up
- Selectable Switching Frequency (f_{SW}): 600kHz, 800kHz, and 1000kHz
- Non-Latch Over-Current Protection (OCP), Under-Voltage Lockout (UVLO), Thermal Shutdown, and Over-Voltage Protection (OVP)
- Available in an FCM LGA-29 (7mmx7mmx4.4mm) Package

APPLICATIONS

- Telecom and Networking Systems
- Base Stations
- Industrial Systems
- Servers and Storage
- FPGA and ASIC Cards

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3683GMN-10	LGA-29 (7mmx7mmx4.4mm)	*See Below*	3

* For tray, add suffix -T (e.g. MPM3683GMN-10-T).

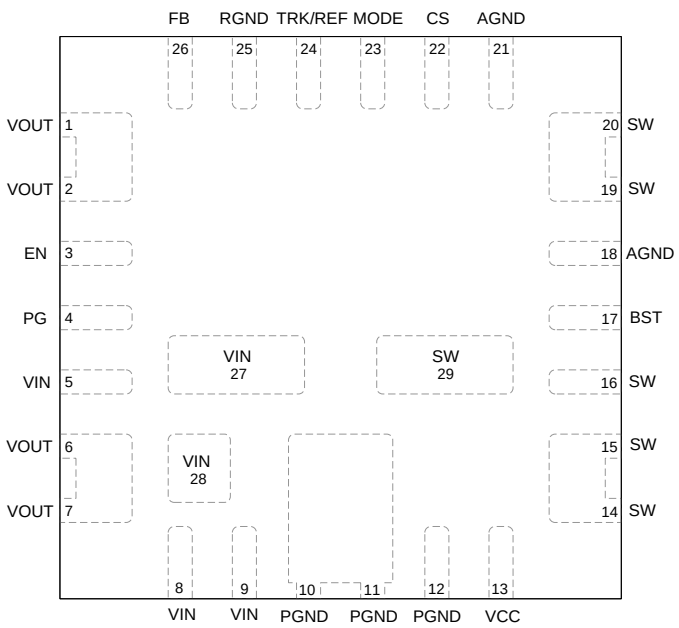
TOP MARKING

MPS YYWW
MP3683-10
LLLLLLLLL
M

MPS: MPS prefix
YY: Year code
WW: Week code
MP3683-10: Product code of the MPM3683GMN-10
LLLLLLLLL: Lot number
M: Module

PACKAGE REFERENCE

TOP VIEW



LGA-29 (7mmx7mmx4.4mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 2, 6, 7	VOUT	**Module output voltage (V_{OUT}) node.**
3	EN	**Enable.** The EN pin is a digital input that turns the regulator on and off. Pull EN high to turn on the regulator; pull EN low to turn off the regulator. Connect EN to VIN via a pull-up resistor or a voltage resistor divider for automatic start-up. Do not float EN.
4	PG	**Power good output.** The PG pin is an open-drain signal. A pull-up resistor connected to a DC voltage indicates high if V_{OUT} is within regulation.
5, 8, 9, 27, 28	VIN	**Input voltage (V_{IN}).** The VIN pin supplies power for the internal MOSFET and regulator. Input capacitors (C_{IN}) are required at VIN to decouple the input rail. Use wide PCB traces to make the connection.
10, 11, 12	PGND	**System ground.** PGND is the regulated V_{OUT}'s reference ground, and requires careful consideration during PCB layout. Use wide PCB traces to make the connection.
13	VCC	**Internal 3V low-dropout (LDO) output.** The driver and control circuits are powered from the VCC voltage (V_{CC}). The MPM3863-10 integrates a 1µF capacitor and does not require an additional external capacitor.
14, 15, 16, 19, 20, 29	SW	**Switch output.** A large copper plane is recommended on the SW pin to improve thermal performance.
17	BST	**Bootstrap (BST).** A BST capacitor (C_{BST}) is integrated internally, and does not require an external connection.
18, 21	AGND	**Analog ground.** Select the AGND pin as the control circuit reference point.
22	CS	**Current limit.** Connect a resistor to ground to set the current limit trip point.
23	MODE	**Operation mode selection**. Configure the MODE pin to select forced continuous conduction mode (FCCM), pulse-skip mode (PSM), and the operating switching frequency (f_{SW}). See Table 1 on page 15 for more details.
24	TRK/REF	**External tracking voltage input.** V_{OUT} tracks the TRK/REF pin input signal. Decouple TRK/REF using a ceramic capacitor as close to TRK/REF as possible. This capacitance determines the soft-start time (t_{SS}). See the Application Information section on page 19 for more details.
25	RGND	**Differential remote sense negative input.** Connect the RGND pin directly to the voltage sense point's negative side. If remote sense is not used, short RGND to GND.
26	FB	**Feedback (differential remote sense positive input).** To set V_{OUT}, connect an external resistor divider from the output to RGND, where RGND is tapped to the FB pin. It is recommended to place the resistor divider as close to FB as possible.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN} to GND) .....-0.3V to +18V
$V_{SW(DC)}$ to GND .....-0.3V to V_{IN} + 0.3V
$V_{SW(25ns)}$ to GND (2).....-3V to +25V
V_{CC} 4.5V
V_{BST} ..... V_{SW} + 4V
V_{OUT}..... 6V
All other pins .....-0.3V to +4.3V
Continuous power dissipation (T_A= 25°C) (3) (6)
…….....9W
Junction temperature .....170°C
Lead temperature .....260°C
Storage temperature..... -55°C to +170°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....4V to 16V
$V_{IN(DC)}$ - $V_{SW(DC)}$ .....-0.3V to V_{IN} + 0.3V
$V_{SW(DC)}$.....-0.3V to V_{IN} + 0.3V
Output voltage (V_{OUT}).....0.6V to 5.5V
External VCC bias (V_{CC_EXT}).....3.12V to 3.6V
EN voltage (V_{EN}) (5)..... 3.6V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

EVM3683-10-MN-01A (6) ..... 16.2....5.1 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured by using a differential oscilloscope probe.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance. θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature.
4) The device is not guaranteed to function outside of its operating conditions.
5) The EN pin has an embedded Zener diode to clamp the voltage at 3.6V. See the Operation section on page 14 for more details on current limiting.
6) Measured on the EVM3683-10-MN-01A, a 4-layer PCB (64mmx64mm).

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, T_J = -40°C to +125°C (7), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Shutdown supply current	I_S	V_{EN} = 0V		10		μA
Quiescent supply current	I_Q	V_{EN} = 2V, V_{FB} = 0.62V		650	850	μA
MOSFET						
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		0	30	
Current Limit						
Current limit threshold	V_{LIM}		1.15	1.2	1.25	V
Low-side (LS) negative current limit	I_{LIM_NEG}			-7.5		A
Negative current limit time-out (8)	t_{NCL_TIMER}			200		ns
Switching Frequency						
Switching frequency (8)	f_{SW}	MODE = GND, I_{OUT} = 0A, V_{OUT} = 1V, T_J = 25°C	480	600	720	kHz
		MODE = 34.8kΩ, I_{OUT} = 0A, V_{OUT} = 1V, T_J = 25°C	680	800	920	kHz
		MODE = 80.6kΩ, I_{OUT} = 0A, V_{OUT} = 1V, T_J = 25°C	850	1000	1150	kHz
Minimum on time (8)	t_{ON_MIN}	V_{FB} = 500mV			50	ns
Minimum off time (8)	t_{OFF_MIN}	V_{FB} = 500mV			180	ns
Over-Voltage Protection (OVP)						
OVP threshold	V_{OVP}		113	116	119	% of V_{REF}
Feedback Voltage and Soft Start (SS)						
Feedback voltage	V_{REF}	T_J = -40°C to +125°C	594	600	606	mV
		T_J = 0°C to 70°C	597	600	603	mV
TRK/REF source current	I_{TRACK_SOURCE}	$V_{TRK/REF}$ = 0V		42		μA
TRK/REF sink current	I_{TRACK_SINK}	$V_{TRK/REF}$ = 1V		12		μA
Soft-start time	t_{SS}	C_{TRACK} = 100nF, T_J = 25°C		1.6		ms
Error Amplifier (EA)						
Feedback current	I_{FB}	V_{FB} = V_{REF}		50	100	nA
Enable (EN) and Under-Voltage Lockout (UVLO)						
EN input rising threshold	V_{EN_RISING}		1.19	1.22	1.25	V
EN hysteresis	V_{EN_HYS}		160	200	280	mV
EN input current	I_{EN}	V_{EN} = 2V		0		μA
Soft shutdown discharge MOSFET	$R_{DS(ON)\_DISCH}$			80		Ω
V_{IN} Under-Voltage Lockout (UVLO)						
V_{IN} UVLO rising threshold	$V_{IN\_UVLO\_RISING}$	V_{CC} = 3.3V	2.1	2.4	2.7	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		1.55	1.85	2.15	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, T_J = -40°C to +125°C (7), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Regulator						
V_{CC} UVLO rising threshold	$V_{CC\_UVLO\_RISING}$		2.65	2.8	2.95	V
V_{CC} UVLO falling threshold	$V_{CC\_UVLO\_FALLING}$		2.35	2.5	2.65	V
VCC regulator	V_{CC}		2.88	3	3.12	V
VCC load regulation		I_{CC} = 25mA		0.5		%
Power Good (PG)						
PG high threshold	PG_{HIGH_RISE}	Pull FB from low to high	89.5	92.5	95.5	% of V_{REF}
	PG_{HIGH_FALL}	Pull FB from high to low	92	101	108	% of V_{REF}
PG low threshold	PG_{LOW_RISE}	Pull FB from low to high	113	116	119	% of V_{REF}
	PG_{LOW_FALL}	Pull FB from high to low	77	80	83	% of V_{REF}
PG low to high delay time	t_{PG_TD}	T_J = 25°C		0.9		ms
PG sink current capability	V_{PG}	I_{PG} = 10mA			0.4	V
PG leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			3	µA
PG low output voltage	$V_{OUT\_LOW\_100}$	V_{IN} = 0V, pull PG up to 3.3V via a 100kΩ resistor at 25°C		650	850	mV
	$V_{OUT\_LOW\_10}$	V_{IN} = 0V, pull PG up to 3.3V via a 10kΩ resistor at 25°C		800	1000	mV
Thermal Protection						
Thermal shutdown (8)	T_{SD}			160		°C
Thermal shutdown hysteresis (8)				30		°C

Notes:

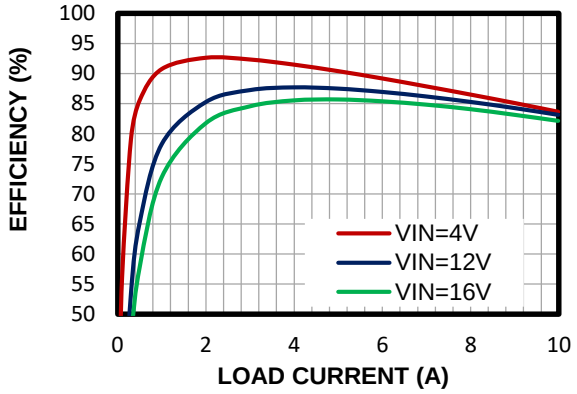
7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, FCCM, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.

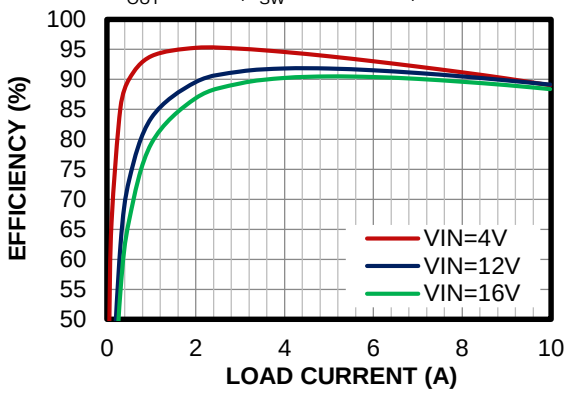
Efficiency vs. Load Current

V_{OUT} = 1V, f_{SW} = 1000kHz, FCCM



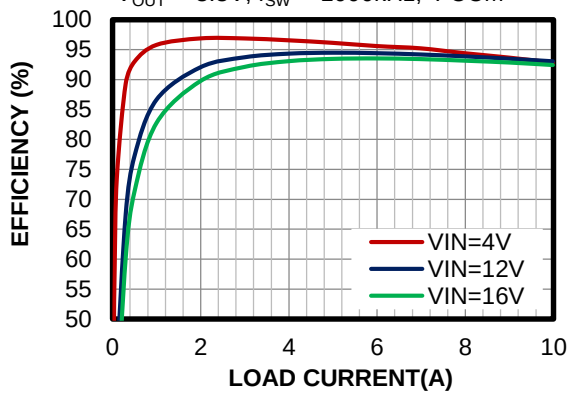
Efficiency vs. Load Current

V_{OUT} = 1.8V, f_{SW} = 1000kHz, FCCM



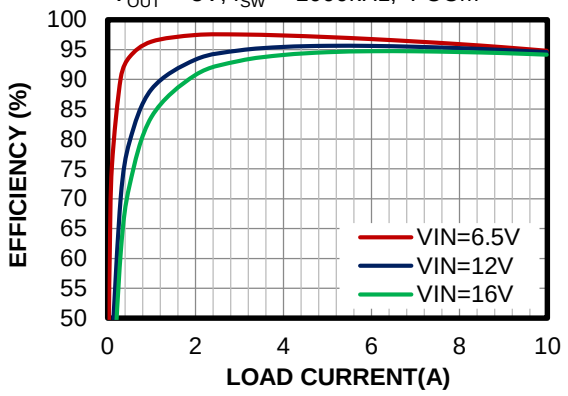
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 1000kHz, FCCM



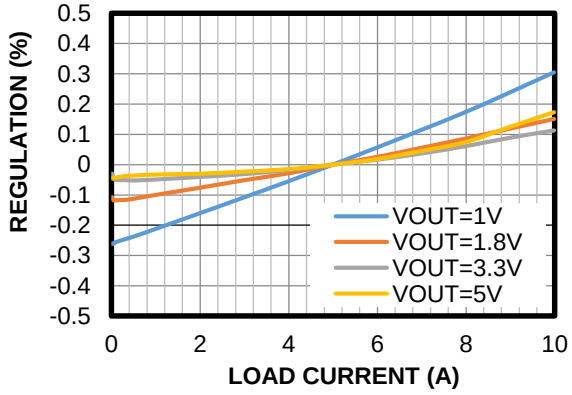
Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 1000kHz, FCCM



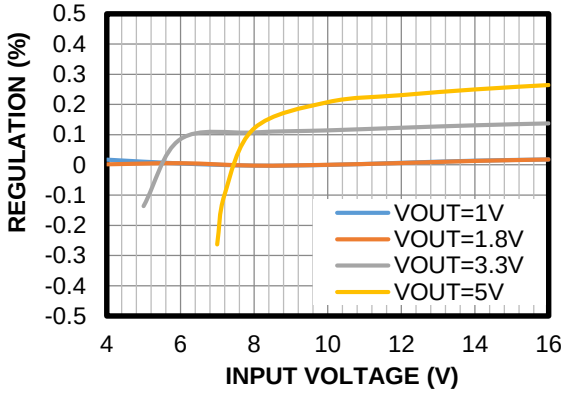
Load Regulation

V_{IN} = 12V, f_{SW} = 1000kHz, FCCM



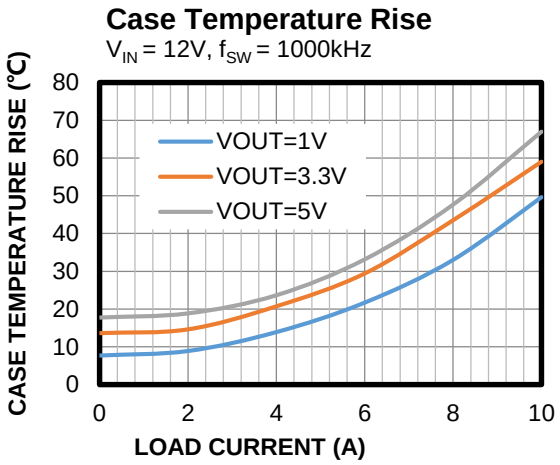
Line Regulation

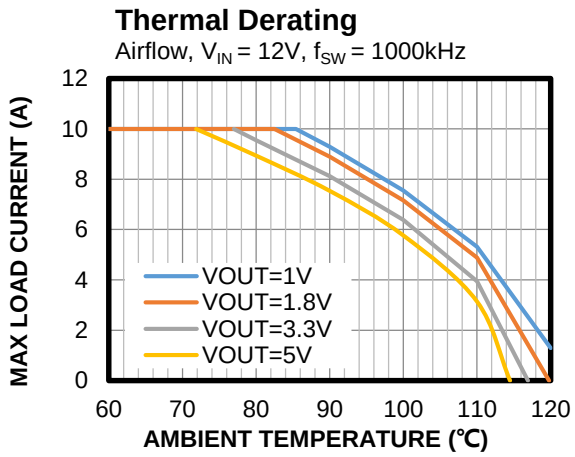
f_{SW} = 1000kHz, FCCM, I_{OUT} = 10A



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, FCCM, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.



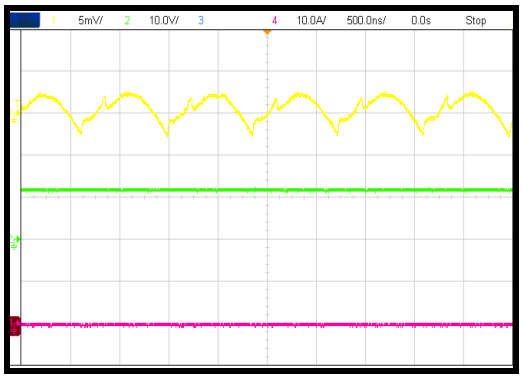


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, FCCM, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.

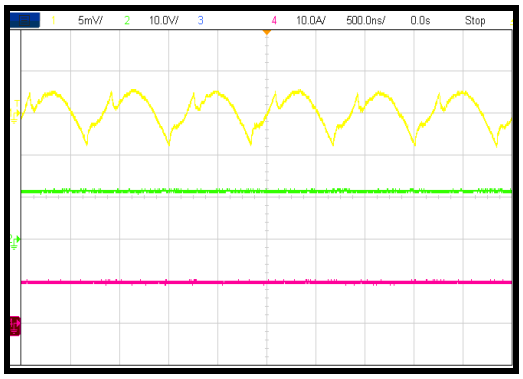
Ripple

I_{OUT} = 0A, C_{OUT} = 9 x 47µF ceramic capacitor



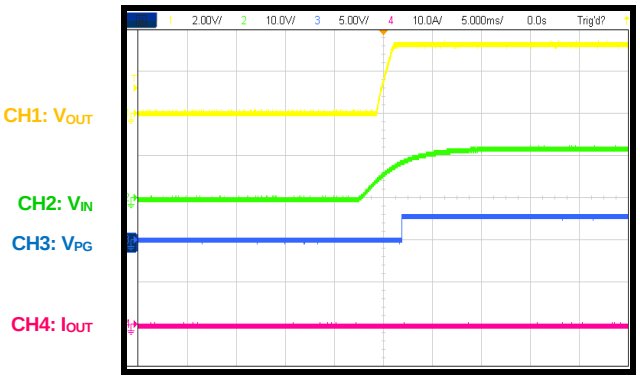
Ripple

I_{OUT} = 10A, C_{OUT} = 9 x 47µF ceramic capacitor



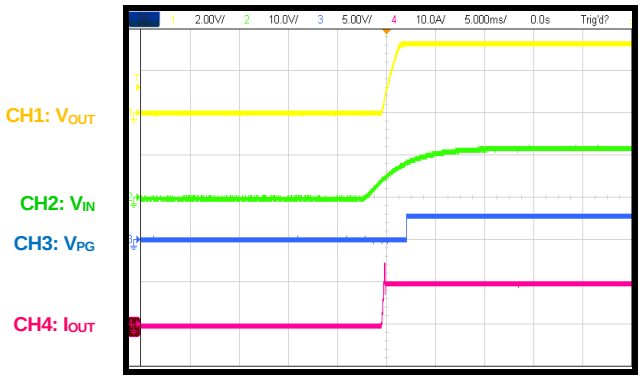
Start-Up through VIN

I_{OUT} = 0A



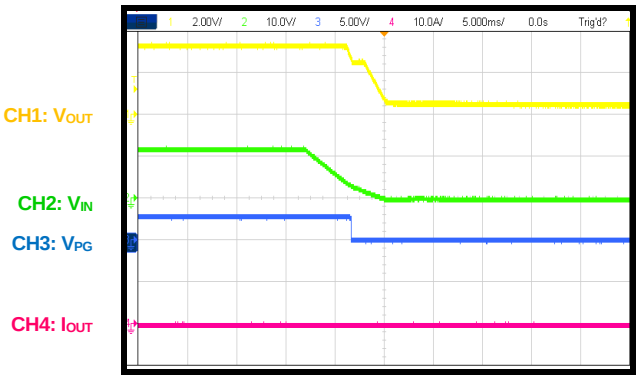
Start-Up through VIN

I_{OUT} = 10A



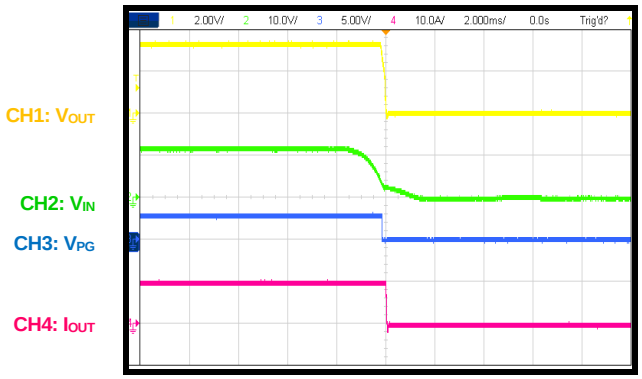
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 10A

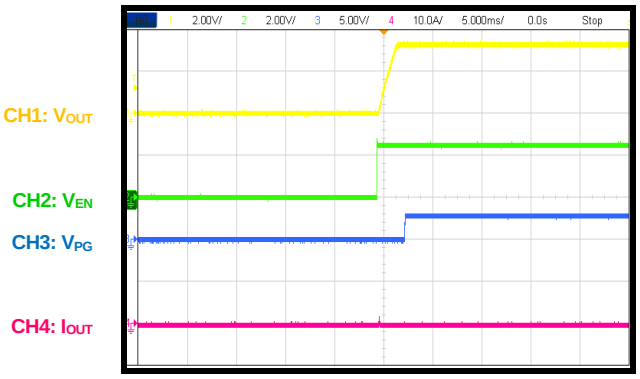


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, FCCM, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.

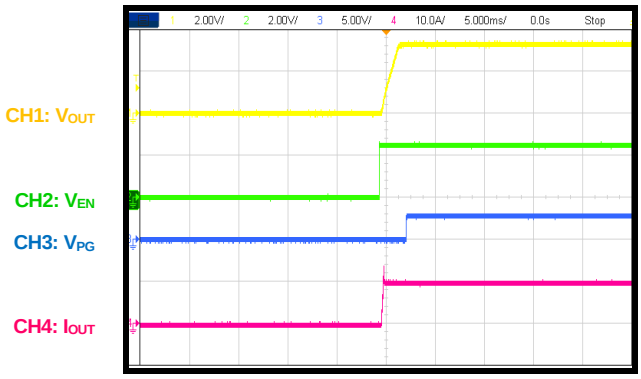
Start-Up through EN

I_{OUT} = 0A



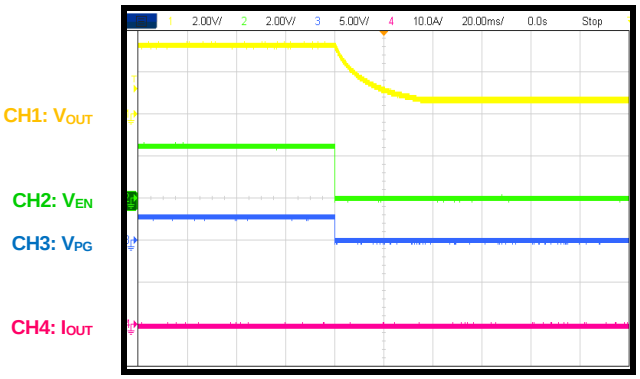
Start-Up through EN

I_{OUT} = 10A



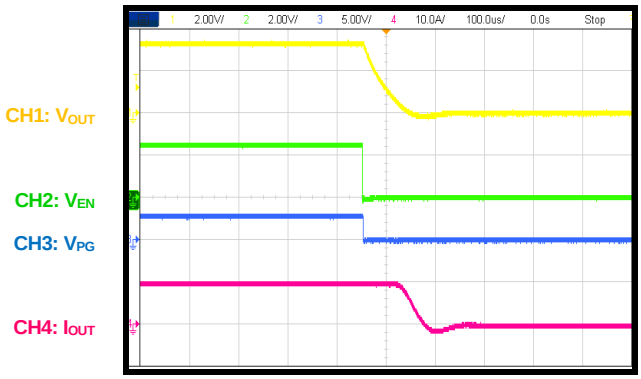
Shutdown through EN

I_{OUT} = 0A



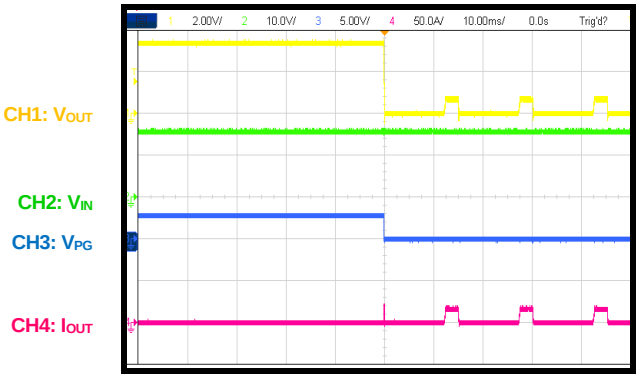
Shutdown through EN

I_{OUT} = 10A



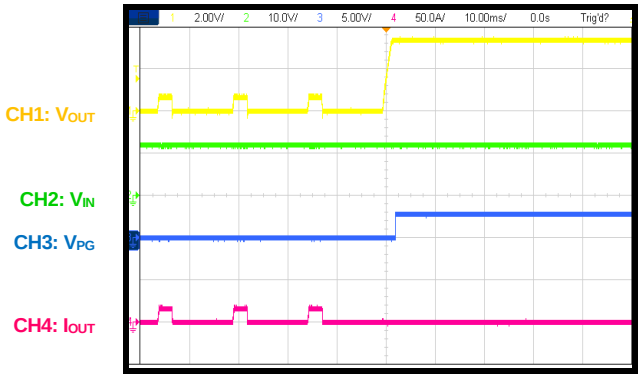
SCP Entry

I_{OUT} = 0A



SCP Recovery

I_{OUT} = 0A

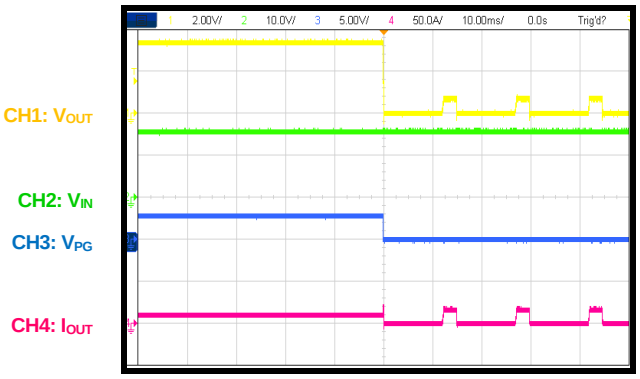


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, FCCM, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.

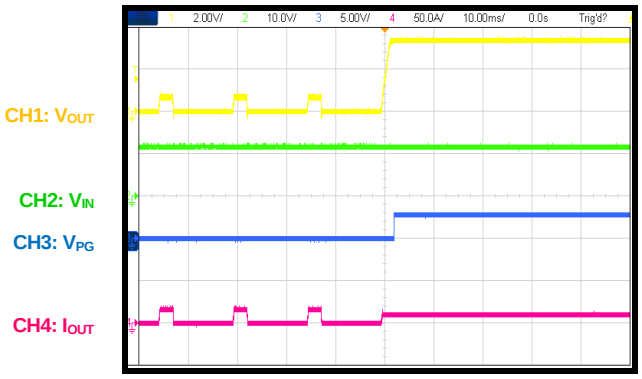
SCP Entry

I_{OUT} = 10A

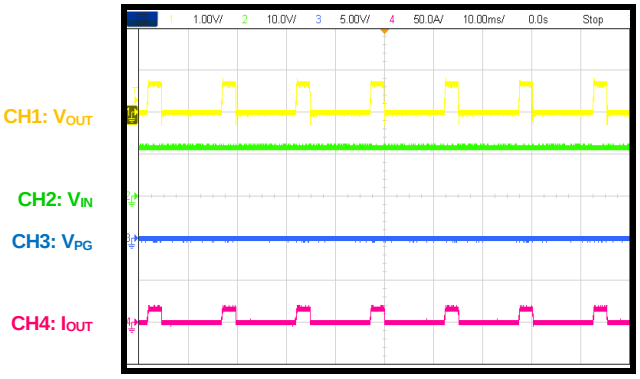


SCP Recovery

I_{OUT} = 10A

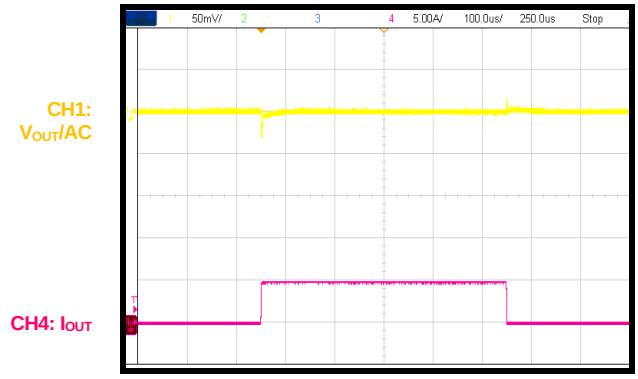


SCP Steady State



Load Transient

5A load step, 5A/µs, C_{OUT} = 9 x 47µF ceramic capacitor, C_{FF} = 4.7nF



FUNCTIONAL BLOCK DIAGRAM

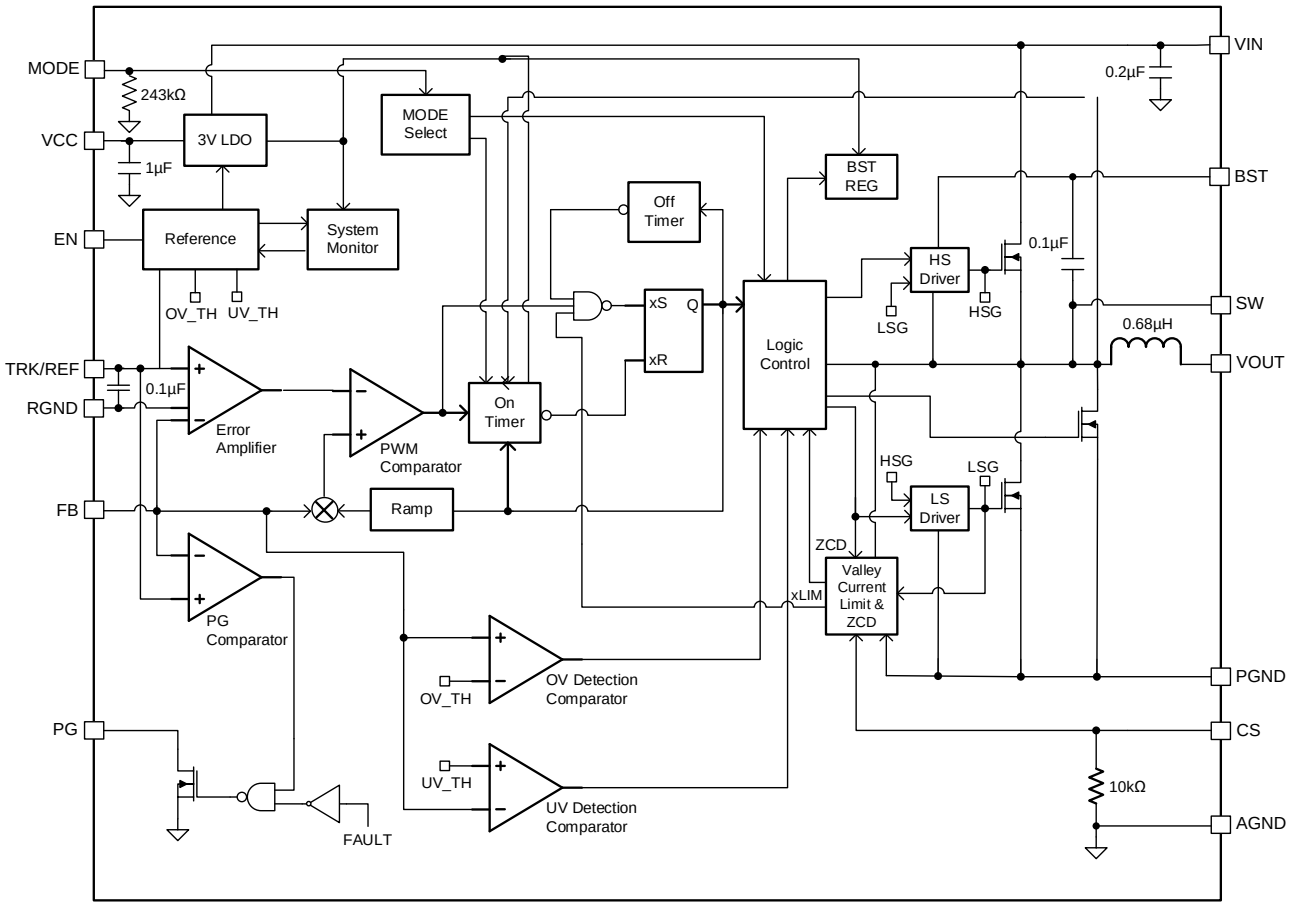


Figure 1: Functional Block Diagram

OPERATION

Constant-On-Time (COT) Control

The MPM3683-10 employs constant-on-time (COT) control to achieve fast load transient response (see Figure 2).

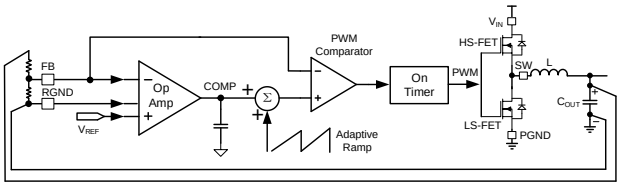


Figure 2: COT Control

The operational amplifier (op amp) corrects any error voltage between the FB pin and the feedback voltage (V_{REF}). Using the op amp, the MPM3683-10 can provide excellent load regulation across the entire load range, regardless of whether it is operating in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM).

The dedicated RGND pin helps provide feedback remote ground sensing. The MPM3683-10 also uses internal ramp compensation to support low ESR, multi-layer ceramic capacitor (MLCC) solutions. The adaptive, internal ramp is optimized so that the MPM3683-10 is stable across the entire operating input voltage (V_{IN}) and output voltage (V_{OUT}) ranges, provided the proper design of the output LC filter.

Pulse-Width Modulation (PWM) Operation

Figure 3 shows how the pulse-width modulation (PWM) is generated during heavy-load operation.

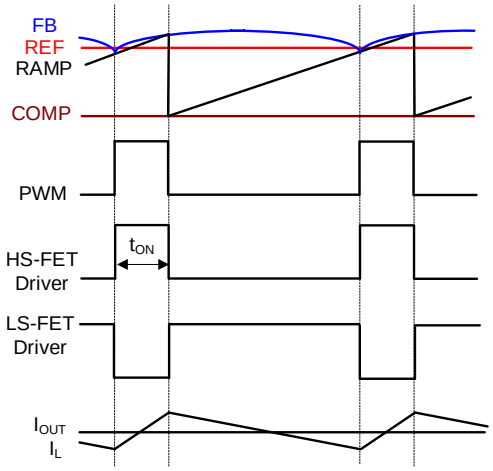


Figure 3: PWM during Heavy-Load Operation

The op amp corrects any error between FB and REF, and generates a fairly smooth DC voltage (V_{COMP}). The internal ramp is superimposed onto V_{COMP}, then the superimposed V_{COMP} is compared with the FB signal.

Whenever the FB voltage (V_{FB}) drops below the superimposed V_{COMP}, the integrated high-side MOSFET (HS-FET) turns on. The HS-FET remains on for a fixed on time, which is determined by V_{IN}, V_{OUT}, and the selected switching frequency (f_{SW}). After the on period elapses, the HS-FET turns off. It turns on again when V_{FB} drops below the superimposed V_{COMP}. By repeating this operation, the MPM3683-10 regulates V_{OUT}.

The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. If the HS-FET and LS-FET are turned on simultaneously, then a dead short occurs between VIN and PGND; this is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period, or vice versa.

Continuous Conduction Mode (CCM)

Continuous conduction mode (CCM) occurs when the output current (I_{OUT}) is high and the inductor current (I_L) remains above 0A. The MPM3683-10 can also be configured to operate in FCCM when I_{OUT} is low (see the Mode Selection section on page 14 for details).

In CCM, f_{SW} is fairly constant (PWM mode), so the output ripple remains almost constant across the entire load range.

Pulse-Skip Mode (PSM)

Under light-load conditions, the MPM3683-10 can be configured to work in PSM to optimize efficiency. When the load decreases, I_L also decreases. Once I_L reaches 0A, the MPM3683-10 transitions from CCM to PSM, provided that it has been configured accordingly (see the Mode Selection section on page 15 for more details).

Figure 4 shows PSM under light-load conditions.

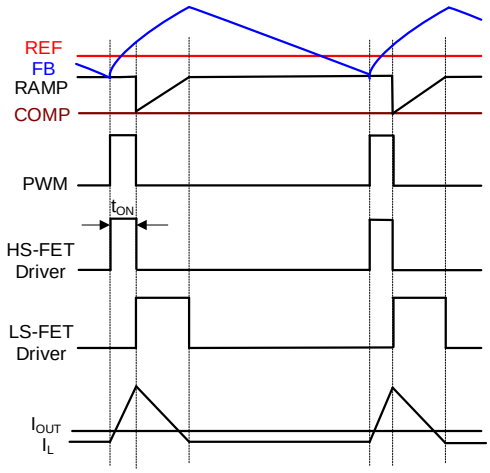


Figure 4: PSM under Light-Load Operation

When V_{FB} drops below the superimposed V_{COMP}, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until I_L reaches 0A. In PSM, V_{FB} does not reach the superimposed V_{COMP} while I_L is approaching 0A.

The LS-FET driver enters tri-state (Hi-Z) when I_L reaches 0A. A current modulator takes over control of the LS-FET and limits I_L below -1mA. Therefore, the output capacitor (C_{OUT}) discharges slowly to PGND through the LS-FET. Under light-load conditions, the HS-FET does not turn on as frequently in PSM compared to FCCM. As a result, efficiency improves significantly in PSM compared to FCCM.

As I_{OUT} increases under light-load conditions, the current modulator regulation period becomes shorter, the HS-FET turns on more frequently, and f_{SW} increases accordingly. I_{OUT} reaches its critical level when the current modulator time is 0s. The I_{OUT} critical level ($I_{OUT\_CRITICAL}$) can be calculated using Equation (1):

$$I_{OUT\_CRITICAL} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

Where L = 0.68µH, representing the integrated inductor.

The MPM3683-10 enters PWM mode once I_{OUT} exceeds $I_{OUT\_CRITICAL}$. Afterward, f_{SW} remains fairly constant across the I_{OUT} range.

The MPM3683-10 can be configured to operate in FCCM even under light-load conditions (see Table 1).

Mode Selection

The MPM3683-10 provides both FCCM and PSM for light-load conditions. The MPM3683-10 has three options for f_{SW} selection: 600kHz, 800kHz, and 1000kHz. Select the operation for light-load conditions and f_{SW} by choosing the value of the resistor placed between MODE and GND or VCC (see Table 1).

Table 1: MODE Selection

MODE	Light-Load Mode	f_{SW} (kHz)
VCC	PSM	600
Float	PSM	800
243kΩ (±20%) to GND	PSM	1000
GND	FCCM	600
34.8kΩ (±20%) to GND	FCCM	800
80.6kΩ (±20%) to GND	FCCM	1000

Soft Start (SS)

With the integrated, 100nF, soft-start (SS) capacitor (C_{SS}), the minimum SS time (t_{SS}) is limited to 1.6ms. t_{SS} can be increased by adding an external capacitor between TRK/REF and AGND.

C_{SS} can be calculated using Equation (2):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times 36\mu A}{0.6V} - 100nF \quad (2)$$

Output Voltage (V_{OUT}) Tracking and Reference

The MPM3683-10 provides TRK/REF, an analog input pin, to track another power supply or accept an external reference. When an external voltage signal is connected to TRK/REF, it acts as a reference for the MPM3683-10 V_{OUT}. V_{FB} follows this external voltage signal exactly, and the SS settings are ignored. The TRK/REF input signal can be in the 0.3V to 1.4V range. During initial start-up, TRK/REF must first reach or exceed 600mV to ensure proper operation. Afterward, TRK/REF can be any value between 0.3V and 1.4V.

Pre-Biased Start-Up

The MPM3683-10 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables the HS-FET and LS-FET switching until the TRK/REF voltage ($V_{TRK/REF}$) exceeds the sensed V_{OUT} at FB. Before $V_{TRK/REF}$ reaches the pre-biased FB level, if the BST voltage (V_{BST}) from BST to SW is below 2.3V, the LS-FET turns on to allow V_{BST} to be charged through VCC. The LS-FET turns on for very narrow pulses, so the drop in the pre-biased level is negligible.

Output Voltage (V_{OUT}) Discharge

When the MPM3683-10 is disabled through EN, V_{OUT} discharge mode is enabled, causing the HS-FET and LS-FET to latch off. A discharge MOSFET connected between SW and PGND is turned on to discharge V_{OUT}. The discharge MOSFET's typical switch-on resistance is about 80Ω. Once V_{FB} drops below 10% of V_{REF}, the discharge MOSFET turns off.

Current Sense and Over-Current Protection (OCP)

The MPM3683-10 features on-die current sensing and a configurable over-current protection (OCP) threshold for the inductor valley current.

OCP is active when MPM3683-10 is enabled. When the LS-FET is on, I_L is sensed and mirrored to the CS pin with the current-sense gain (G_{CS}) ratio. By connecting the external current-sense resistor (R_{CS}) between CS and AGND, the CS voltage (V_{CS}) is generated in proportional with the I_L cycle by cycle. The HS-FET is allowed to turn on only when V_{CS} is below the current limit threshold (V_{LIM}) while the LS-FET is on. This limits the inductor valley current cycle by cycle. The MPM3683-10 integrates an 10kΩ current-sense resistor between CS and AGND.

The inductor valley current's OCP threshold (I_{VALLEY}) can be determined using Equation (3):

$$I_{VALLEY} = \frac{V_{LIM}}{R_{CS}(M\Omega)//0.01M\Omega \times G_{CS}} \quad (3)$$

R_{CS} for the desired I_{OUT} limit (I_{LIM}) can be calculated using Equation (4):

$$R_{CS}(M\Omega)//0.01M\Omega = \frac{V_{LIM}}{G_{CS} \times (I_{LIM}(A) - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{2 \times L(\mu H) \times f_{SW}(MHz)})} \quad (4)$$

Where V_{LIM} = 1.2V, G_{CS} = 20μA/A, and L = 0.68μH.

It should be noted that the MPM3683-10 provides accurate cycle-by-cycle OCP for the inductor valley current. However, the conversion between the inductor valley current and I_{OUT} may involve error that is introduced by the tolerance of the integrated inductor and f_{SW} variation due to COT operation. Table 2 shows the recommended R_{CS} selection for typical applications.

Table 2: R_{CS} for Typical Applications

Conditions	R_{CS} (kΩ)
V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 1000kHz, I_{LIM} = 8A	249
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1000kHz, I_{LIM} = 8A	78.7
V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 1000kHz, I_{LIM} = 10A	16.2
V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 1000kHz, I_{LIM} = 10A	16
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1000kHz, I_{LIM} = 10A	15

OCP with hiccup mode is active for 3ms after the MPM3683-10 is enabled. Once OCP with hiccup mode is active, the MPM3683-10 enters hiccup mode if it detects an over-current (OC) condition for 31 consecutive cycles.

In hiccup mode, the HS-FET latches off the immediately, and the LS-FET latches off after zero-current detection (ZCD) is detected. The TRK/REF capacitor ($C_{TRK/REF}$) is discharged as well. After about 11ms, the MPM3683-10 attempts to soft start automatically. If the OC condition remains after 3ms, the MPM3683-10 repeats this operation cycle until the OC condition is removed, and V_{OUT} rises back to the regulation level smoothly.

Negative Inductor Current Limit

When the LS-FET detects a -7.5A (typical) current, the MPM3683-10 turns off the LS-FET for 200ns to limit the negative current.

Output Sinking Mode (OSM)

The MPM3683-10 employs output sinking mode (OSM) to regulate V_{OUT} to the target value. If V_{FB} exceeds 104% of V_{REF} but remains below the over-voltage protection (OVP) threshold, OSM is triggered. During OSM, the LS-FET remains on until it reaches the -5.5A negative current limit. Afterward, the LS-FET is turned off momentarily (200ns) before turning on again. The MPM3683-10 repeats this operation until V_{FB} drops below 102% of V_{REF}. Afterward, the MPM3683-10 exits OSM after 15 consecutive cycles of FCCM.

Over-Voltage Protection (OVP)

The MPM3683-10 monitors V_{OUT} by connecting FB to the V_{OUT} feedback resistor divider's tap to detect an over-voltage (OV) condition.

If V_{FB} exceeds 116% of V_{REF}, OVP is triggered. The LS-FET turns on until it reaches the low-side negative current limit (I_{LIM_NEG}). Then the LS-FET turns off momentarily for 200ns. During this period, the HS-FET turns on. After 200ns, the LS-FET turns on again. The MPM3683-10 repeats this operation to discharge any over-voltage on the output. Once V_{REF} drops below 101% of V_{REF}, the MPM3683-10 exits OVP discharge mode.

Over-Temperature Protection (OTP)

The MPM3683-10 features over-temperature protection (OTP), and monitors the junction temperature (T_J) internally. If T_J exceeds the threshold (typically 160°C), the converter shuts down and discharges $C_{TRK/REF}$. OTP is a non-latch protection with a hysteresis of about 30°C. Once T_J drops to about 130°C, SS is initiated.

OTP is effective once the MPM3683-10 is enabled.

Power Good (PG)

The MPM3683-10 has a power good (PG) output. PG is the MOSFET's open drain. Connect PG to VCC or another external voltage source (below 3.6V) via a pull-up resistor (typically 10kΩ). After applying V_{IN}, the MOSFET turns on, and PG is pulled to GND before TRK/REF is ready. After V_{FB} reaches 92.5% of V_{REF}, PG is pulled high after a 0.9ms delay.

If V_{FB} drops to 80% of V_{REF} or exceeds 116% of the nominal V_{REF}, PG is pulled low. Once V_{FB} increases to 92.5% of V_{REF} or drops to 101% of V_{REF}, PG is pulled high again.

If the input supply fails to start up the MPM3683-10, PG is clamped low, even though PG is tied to an external DC source via a pull-up resistor. Figure 5 shows the relationship between the PG voltage (V_{PG}) and the pull-up current (I_{PG}).

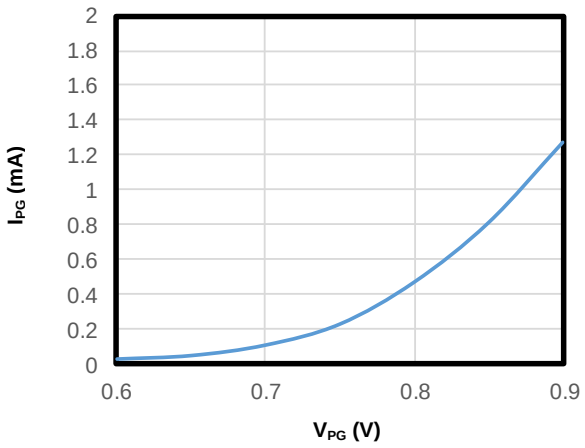


Figure 5: PG Clamped Voltage vs. Pull-Up Current

Enable (EN) Configuration

The MPM3683-10 turns on when EN goes high; the MPM3683-10 turns off when EN goes low. For proper operation, EN cannot be left floating. EN can be driven by an analog or digital control logic signal to enable or disable the MPM3683-10.

The MPM3683-10 provides accurate EN thresholds to allow a resistor divider placed between VIN and AGND to be used to configure V_{IN} at the point when the MPM3683-10 is enabled.

This is highly recommended for applications without a dedicated EN control logic signal to avoid possible under-voltage lockout (UVLO) bouncing during start-up and shutdown.

The resistor divider values (V_{IN_START}) can be calculated using Equation (5):

$$V_{IN\_START}(V) = V_{EN\_RISING} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (5)$$

Where V_{EN_RISING} is the EN input rising threshold (typically 1.22V), R_{UP} is the pull-up resistor, and R_{DOWN} is the pull-down resistor.

R_{UP} and R_{DOWN} should be chosen so that the EN voltage (V_{EN}) does not exceed 3.6V when V_{IN} reaches the maximum value (V_{IN_MAX}).

EN can also be connected to VIN directly via R_{UP}. R_{UP} should be chosen so that the maximum current going into EN is 50μA. R_{UP} can be calculated using Equation (6):

$$R_{UP}(k\Omega) = \frac{V_{IN\_MAX}(V)}{0.05mA} \quad (6)$$

APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

Figure 6 shows the circuit connection.

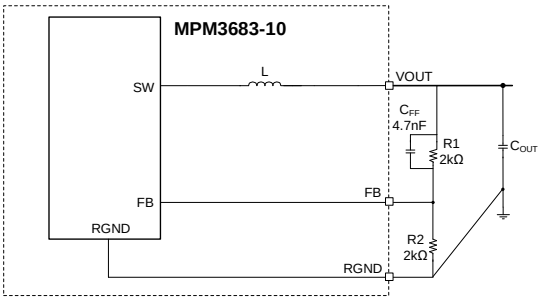


Figure 6: Circuit Connection

R2 can be calculated using Equation (7):

$$R2\,(k\Omega) = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1\,(k\Omega) \quad (7)$$

Where V_{REF} = 0.6V.

Table 3 shows the recommended feedback resistor (R1 and R2) and feedforward capacitor (C_{FF}) values for common V_{OUT} values.

Table 3: Common V_{OUT} Values

V_{OUT} (V)	C_{FF} (nF)	R1 (kΩ)	R2 (kΩ)
1	4.7	2	3
1.2	4.7	2	2
1.8	4.7	2	1
3.3	4.7	10.2	2.26
5	4.7	7.5	1.02

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, it is recommended to use ceramic capacitors. Place C_{IN} as close to VIN as possible during PCB layout.

The capacitance can vary significantly with the temperature. Ceramic capacitors with X5R and X7R dielectrics are recommended due to their low ESR and stability across a wide temperature range.

The ripple current rating of the capacitors must exceed the converter's maximum input ripple current.

The input ripple current (I_{CIN}) can be estimated using Equation (8):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, where I_{CIN} can be calculated using Equation (9):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (9)$$

For simplification, choose C_{IN} with an RMS current rating that exceeds half of the maximum load current. C_{IN} determines the converter's input voltage ripple (ΔV_{IN}). If there is a system requirement for ΔV_{IN}, select C_{IN} to meet the relevant specifications. ΔV_{IN} can be estimated using Equation (10):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, where ΔV_{IN} can be calculated using Equation (11):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (11)$$

Selecting the Output Capacitor (C_{OUT})

C_{OUT} maintains the DC V_{OUT}. It is recommended to use POSCAP or ceramic capacitors. The output voltage ripple (ΔV_{OUT}) can be estimated using Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (12)$$

When using ceramic capacitors, the capacitance dominates ΔV_{OUT} and the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated using Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{\,2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

The ESR dominates the f_{SW} impedance for the POSCAP capacitors.

For simplification, ΔV_{OUT} can be estimated using Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (14)$$

Where L is fixed at 0.68μH internally.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 7 and follow the guidelines below:

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MPM3683-10.
3. Maximize the copper planes of VIN and PGND to minimize parasitic impedance.
4. Ensure that the high-current paths (PGND, VIN, and VOUT) have short, direct, and wide traces.
5. Place as many PGND vias as close to PGND as possible to minimize parasitic impedance and thermal resistance.
6. Place the external feedback resistors next to FB.
7. Keep the feedback network away from the switching node.

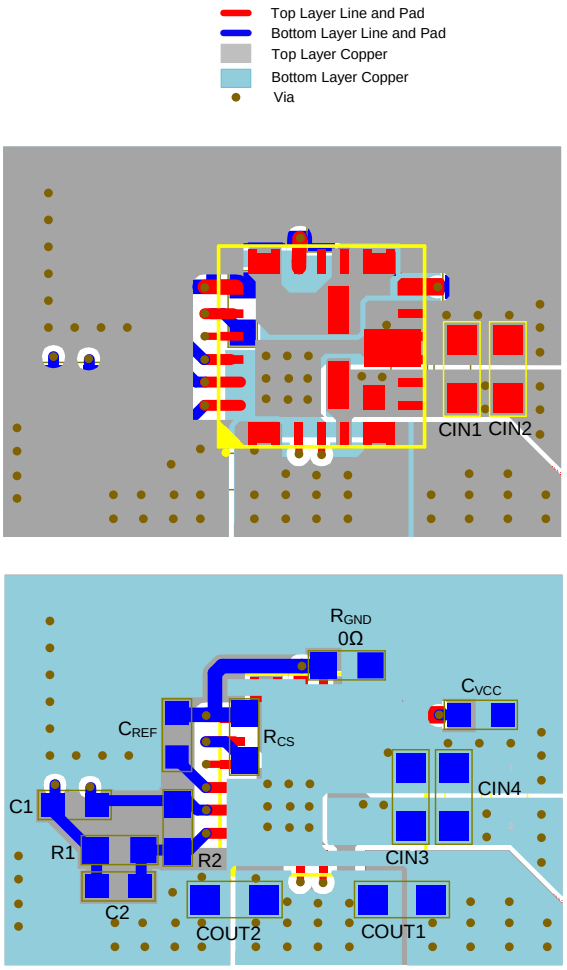


Figure 7: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

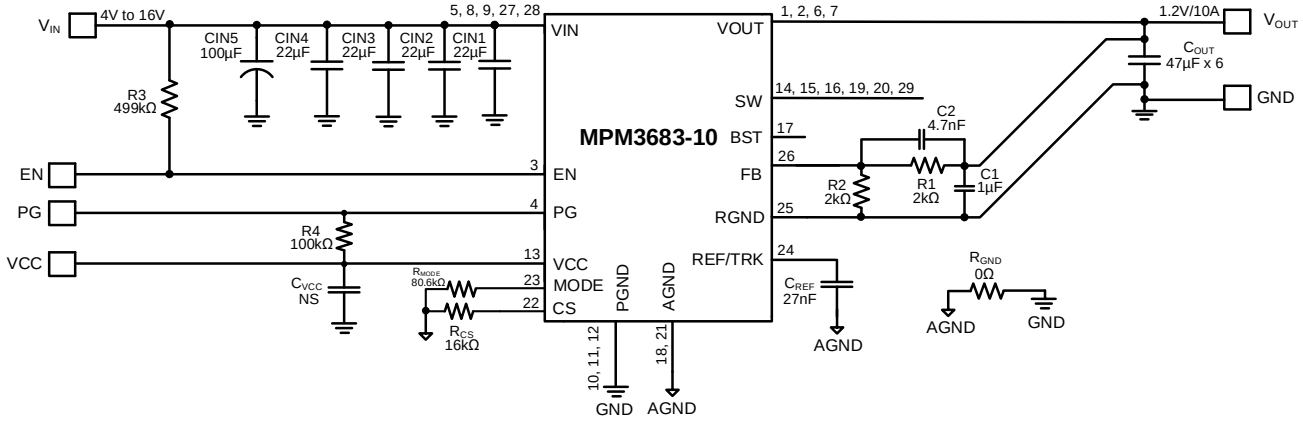
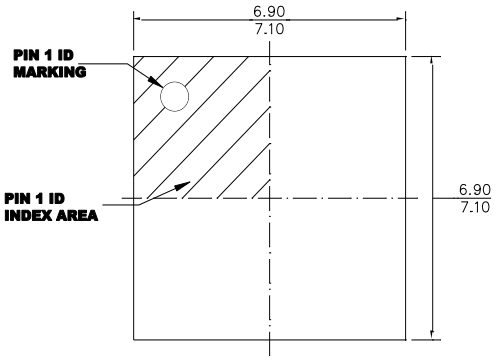


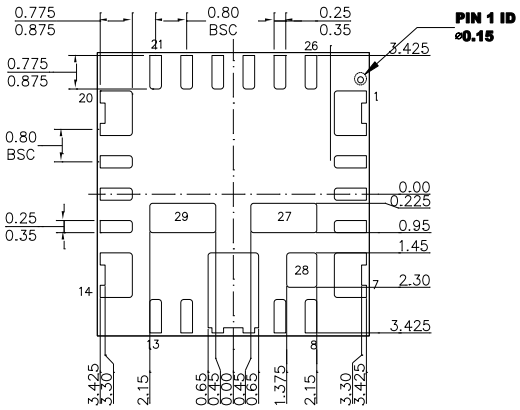
Figure 8: Typical Application (V_{IN} = 12V, 1.2V/10A Output, FCCM, 1000kHz)

PACKAGE INFORMATION

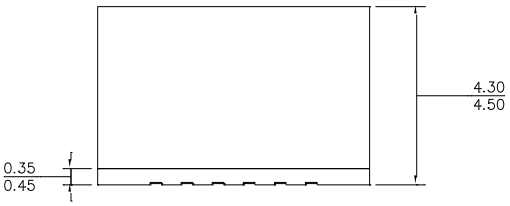
LGA-29 (7mmx7mmx4.4mm)



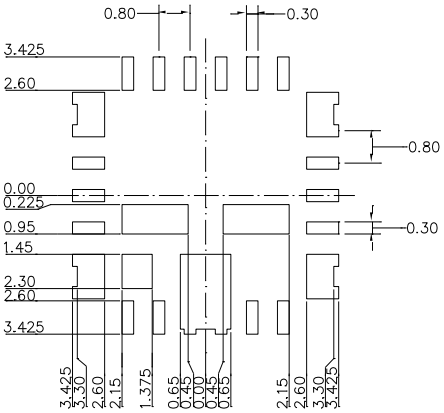
TOP VIEW



BOTTOM VIEW



SIDE VIEW

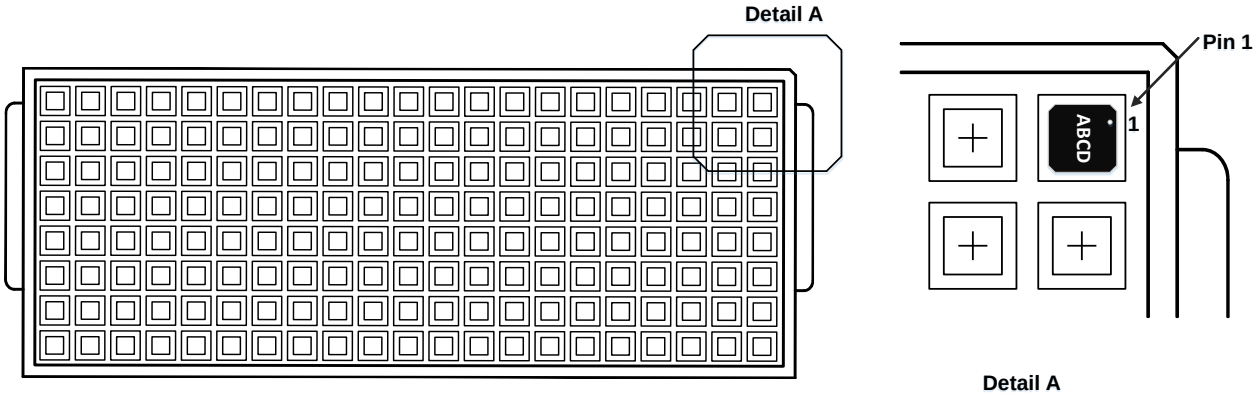


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION (9)



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3683GMN-10-T	LGA-29 (7mmx7mmx4.4mm)	N/A	N/A	260	N/A	N/A	N/A

Note:

9) This is a schematic diagram of the tray package. Different packages correspond to different trays with varying length, width, and height.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/6/2022	Initial Release	-

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- Alternative Solution
- Excess Inventory Management