



**THE DATASHEET OF
RCLAMP3391ZCTFT**



PROTECTION PRODUCTS

Description

RClamp®3391ZC is an ultra low capacitance “FemtoClamp™” ESD protection device specifically designed to protect high-speed differential lines. It offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp3391ZC features excellent ESD protection characteristics highlighted by low peak ESD clamping voltage, and high ESD withstand voltage ($\pm 8\text{kV}$ contact per IEC 61000-4-2). RClamp3391ZC has a maximum capacitance of 0.2pF allowing it to be used on Thunderbolt and USB 3.1 high speed lanes. These devices may also be used for EOS protection due to their high peak pulse current capability (7A, $t_p = 8/20\mu\text{s}$). Each device will protect one high-speed data line operating up to 3.3 volts.

RClamp3391ZC is in a DFN 0.60x0.30x0.25mm-2 Lead package. Leads are finished with NiAu. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical.

Features

- ESD and EOS Protection
- ESD withstand voltage
 - ♦ IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- Ultra-Low capacitance: 0.20pF Maximum
- Very small PCB area
- Protects one high-speed data line
- Working voltage: 3.3V
- Low reverse leakage current: 50nA max at $V_R = 3.3\text{V}$
- Solid-state silicon-avalanche technology

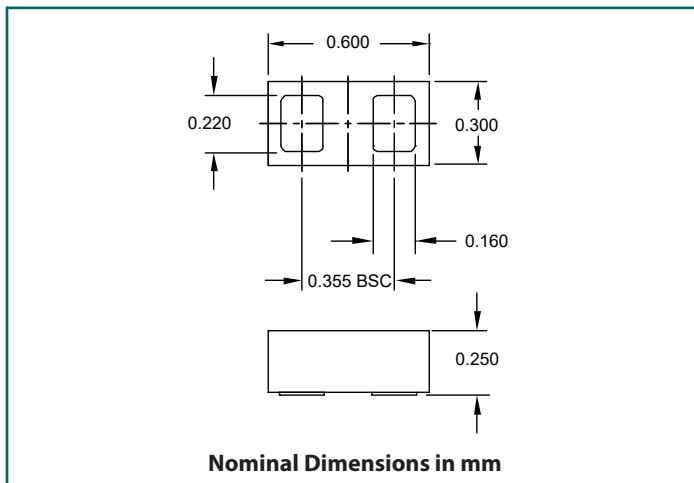
Mechanical Characteristics

- Package: DFN 0.60x0.30x0.25mm-2 Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: NiAu
- Marking : Marking Code
- Packaging : Tape and Reel

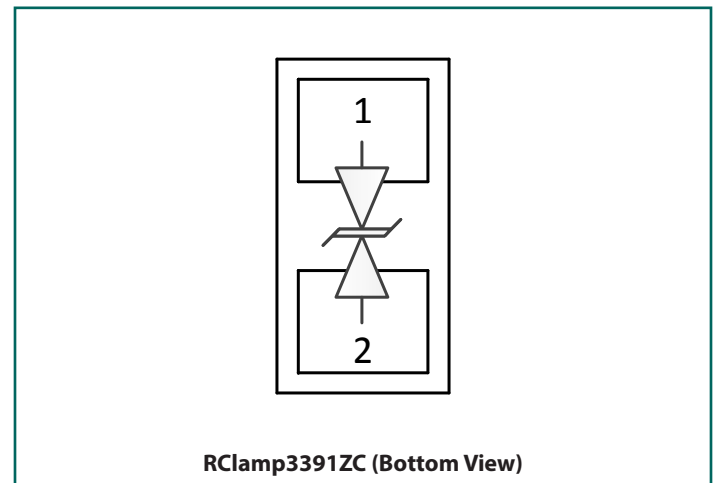
Applications

- Thunderbolt 3
- USB 3.1 and USB 3.0
- HDMI 1.4 and HDMI 2.0
- USB Type-C
- HD-SDI
- 10GbE

Nominal Dimensions



Schematic and Pin Configuration



Absolute Maximum Ratings

| Rating | Symbol | Value | Units |
|--|------------------|-------------|-------|
| Peak Pulse Power (tp = 8/20μs) | P _{PK} | 45 | W |
| Peak Pulse Current (tp = 8/20μs) | I _{PP} | 7 | A |
| ESD per IEC 61000-4-2 (Air) ⁽¹⁾ ESD per IEC 61000-4-2 (Contact) ⁽¹⁾ | V _{ESD} | ±15 ±8 | kV |
| Operating Temperature | T _{OP} | -40 to +85 | °C |
| Storage Temperature | T _{STG} | -55 to +150 | °C |

Electrical Characteristics (T=25°C unless otherwise specified)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|-------------------|--|-----------------------|------|------|-------|
| Reverse Stand-Off Voltage | V _{RWM} | -40°C to 85°C | | | 3.3 | V |
| Reverse Breakdown Voltage | V _{BR} | I _t = 1mA -40°C to 85°C | 5.5 | 8 | 10 | V |
| Reverse Leakage Current | I _R | V _{RWM} = 3.3V | | <5 | 50 | nA |
| Clamping Voltage ² | V _C | tp = 1.2/50μs (Voltage), 8/20μs (Current) Combination Waveform, R _s = 2 Ω I _{PP} = 7A | | 5 | 6.5 | V |
| ESD Clamping Voltage ³ | V _C | tp = 0.2/100ns (TLP) | I _{PP} = 4A | 3.3 | | V |
| | | | I _{PP} = 16A | 5.5 | | |
| Trigger Voltage ³ | V _{TRIG} | tp = 0.2/100ns (TLP) | | 9.4 | | V |
| Dynamic Resistance ^{3,4} | R _{DYN} | tp = 0.2/100ns (TLP) | | 0.18 | | Ohms |
| Junction Capacitance | C _J | V _R = 0V, f = 1MHz | | 0.17 | 0.20 | pF |

Notes:

(1): ESD gun return path connected to Ground Reference Plane (GRP)

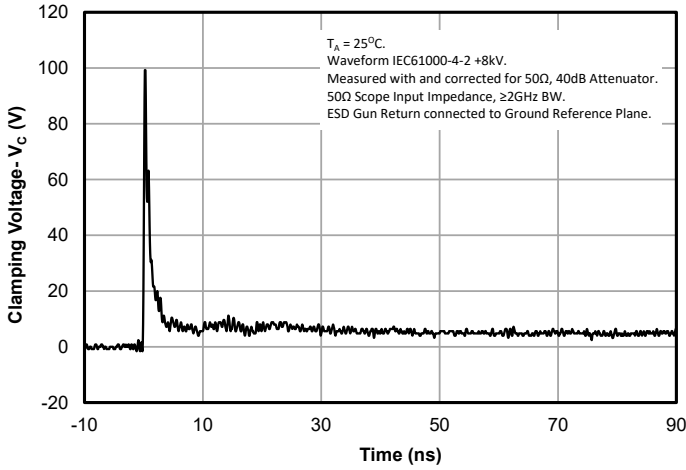
(2): Measured using a 1.2/50μs voltage, 8/20μs current combination waveform, R_s = 2 Ohms. Clamping voltage is defined as the peak voltage across the device after the device snaps back to a conducting state.

(3): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t₁ = 70ns to t₂ = 90ns

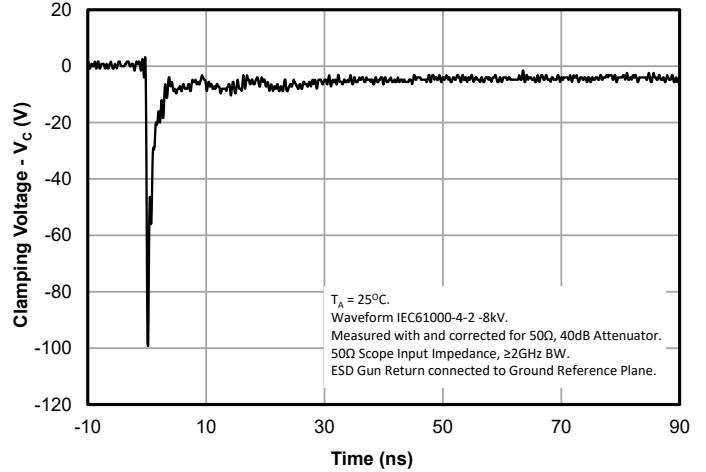
(4): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

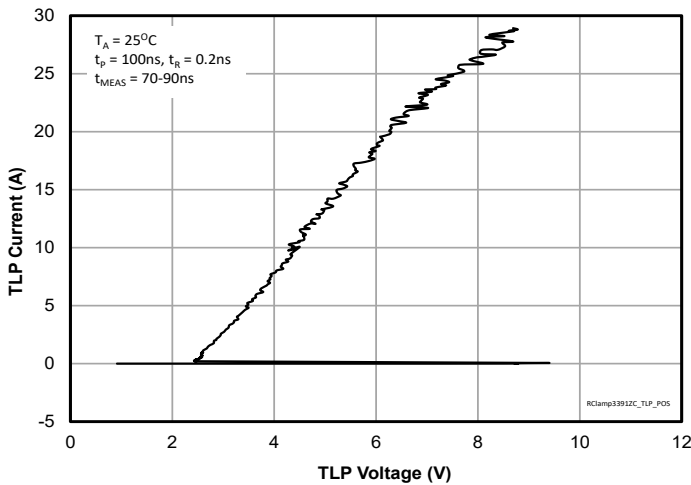
ESD Clamping (+8kV Contact per IEC 61000-4-2)



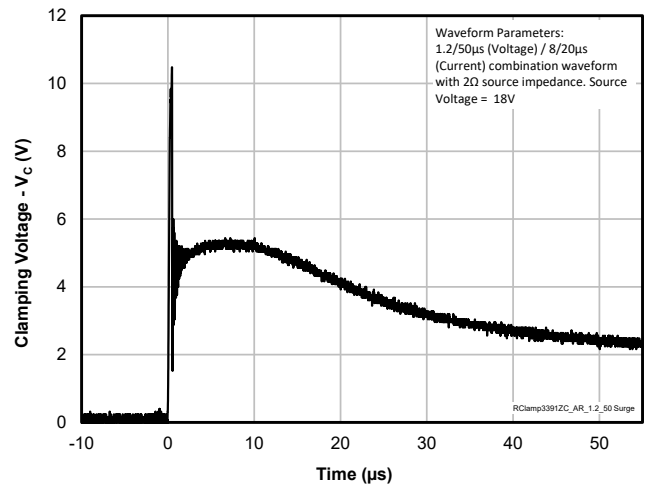
ESD Clamping (-8kV Contact per IEC 61000-4-2)



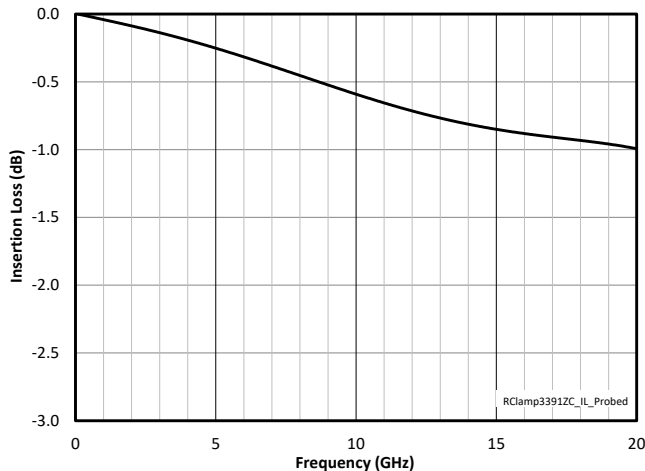
TLP IV Curve



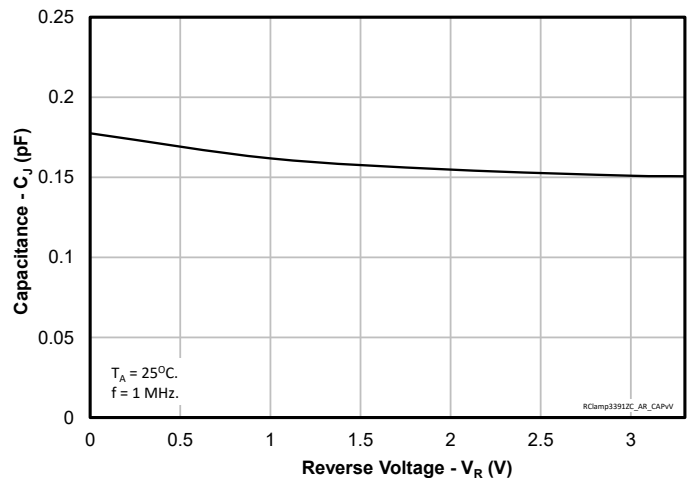
Clamping Characteristic (1.2/50 μs Waveform)



Insertion Loss (S21)



Capacitance vs. Reverse Voltage



Application Information

USB Type-C Interface Protection

USB Type-C is a 12-pin connector which supports USB 3.1 Gen 2 SuperSpeed+ (10Gb/s) connections and USB power delivery (USB PD). It is also backwards compatible (via an adapter) with USB 3.0 and USB 2.0. The USB Type-C connector does not imply the use of USB 3.1 technology. USB Type-C is a connector shape. The underlying technology may be USB 2.0, USB 3.0, or USB 3.1. USB Type-C plugs are reversible (i.e. can be either be inserted right-side up or upside-down position) so there are connections on both the top and bottom of the PCB. The USB Type-C receptacle consists of 24-pins including: SuperSpeed RX and TX signal pairs, USB 2.0 DP and DM data pins, Auxiliary pins, Configuration pins, and Power and Ground Pins. Any of these connections are capable of conducting ESD current and should be protected.

Protection Solutions

SuperSpeed data line pairs are located on both the top and bottom of the PCB to support Type-C plug reversal (i.e. flip-ability). ESD protection of the SuperSpeed line pairs is achieved using one RClamp3391ZC between each line and ground. The low capacitance of RClamp3391ZC (0.2pF maximum) exhibits minimal effect on the transmission line impedance and excellent insertion loss characteristics. Single line devices make it easier for the designer to route the traces and maintain equal distance between the differential pairs for maximum signal integrity.

RClamp3391ZC features very good ESD characteristics highlighted by low holding voltage after snapback, and extremely low dynamic resistance ($R_{DYN} = 0.18 \Omega$). Besides the SuperSpeed+ lines, USB 2.0 pins support Type-C plug reversal by shorting together the D+ pins and D- pins in the plug receptacle. This means RClamp3391ZC only needs to be placed on the side of the PCB where the traces are routed. RClamp3391ZC can also be used to protect the configuration channel (CC) and Sideband (SBU) pins. VBUS pins are connected together within the Type-C plug and bussed together on the PCB. USB Type-C default power is fixed at 5V. Single line power protection devices such as PClamp0501P are recommended for surge and ESD protection. Note that in power delivery(PD) applications, higher working voltage TVS devices may be needed.

Examples of USB Type-C ESD protection topology RClamp3391ZC and PClamp0501P are shown in Figures 1 and 2.

Device Placement

Placement of the protection component is a critical element for effective ESD suppression. TVS should be placed as close to the connector as possible. This helps reduce transient coupling to nearby traces. Ground connections should be made directly to the ground plane using micro-vias. This reduces parasitic inductance in the ground path and minimizes the clamping voltage seen by the protected device.

Figure 1 - USB Type-C Top Layer Protection Example

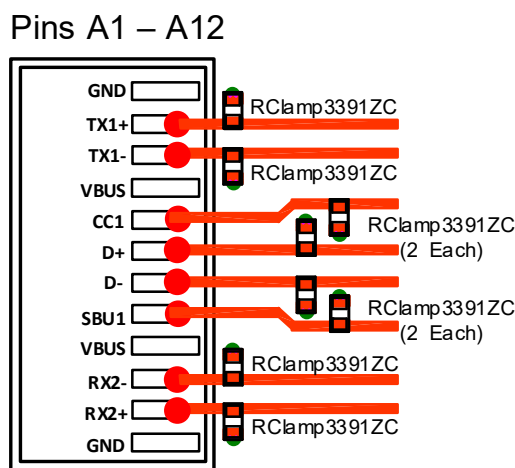
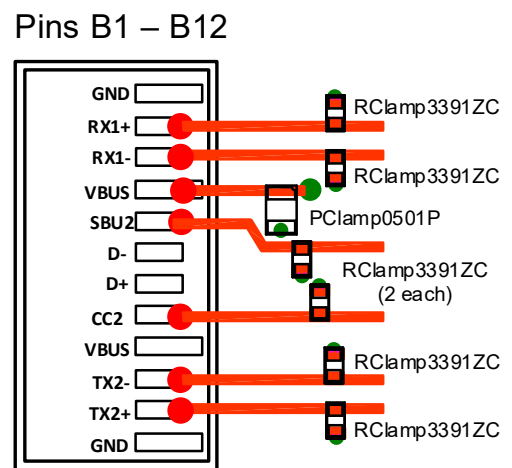


Figure 2 - USB Type-C Bottom Layer Protection Example



Application Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

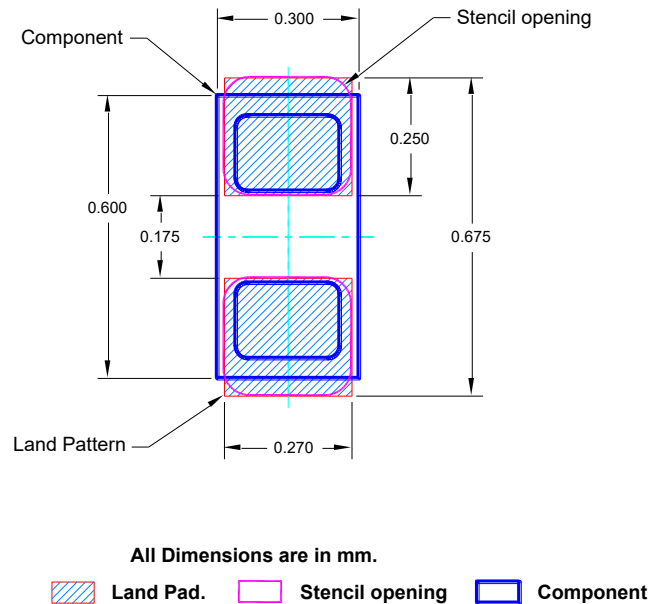
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.075mm (0.003") is recommended. A 0.100mm (0.004") stencil may be used, however the stencil opening may need to be increased slightly to achieve the desired area ratio to ensure proper solder coverage on the pad.

Recommended Mounting Pattern



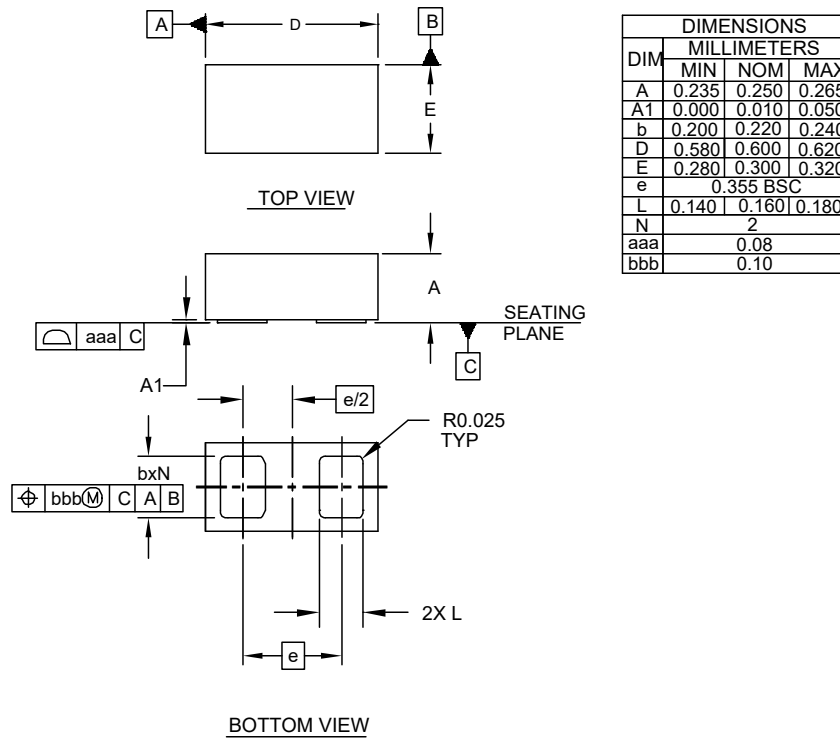
All Dimensions are in mm.

Land Pad. Stencil opening Component

Table 1 - Assembly Guidelines

| Assembly Parameter | Recommendation |
|--------------------------|--|
| Solder Stencil Design | Laser Cut, Electro-Polished |
| Aperture Shape | Rectangular with Rounded Corners |
| Solder Stencil Thickness | 0.075mm (0.003") or 0.100mm (0.004") |
| Solder Paste Type | Type 4 Size Sphere or Smaller |
| Solder Reflow Profile | Per JEDEC J-STD-020 |
| PCB Solder Pad Design | Solder Mask Defined or Non Solder Mask Defined |
| PCB Pad Finish | OSP or NiAu |

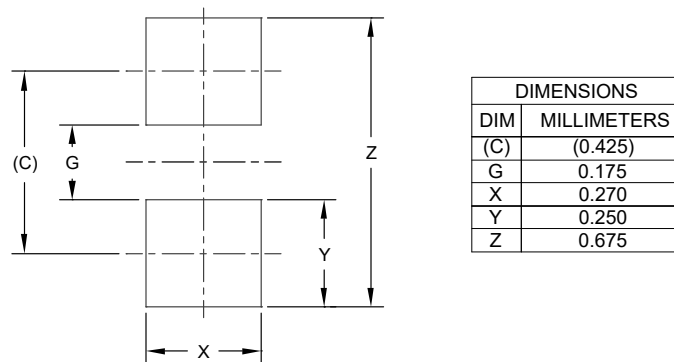
Outline Drawing - DFN 0.60x0.30x0.25mm-2 Lead



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - DFN 0.60x0.30x0.25mm-2 Lead



NOTES:

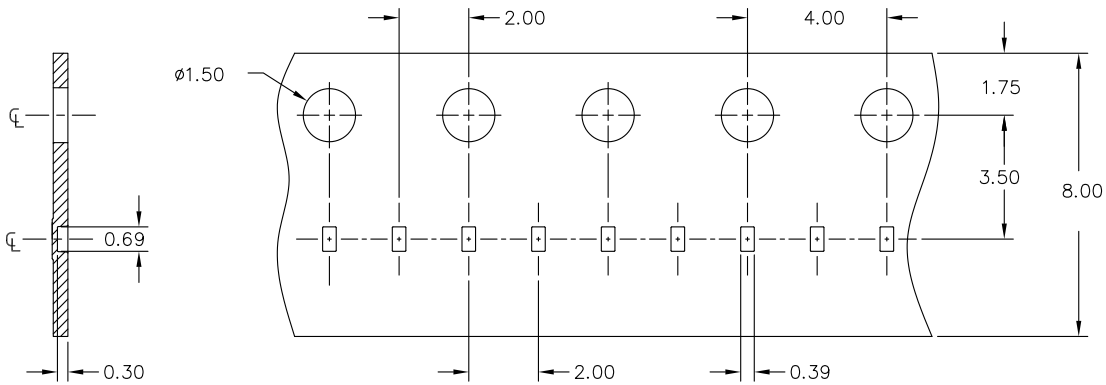
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

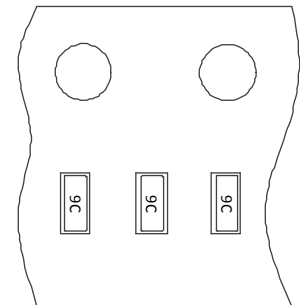
9C

Notes: Device is electrically symmetrical.

Tape and Reel Specification



Note: All dimensions are nominal dimensions in mm.



Ordering Information

| Part Number | Qty per Reel | Reel Size |
|--|--------------|-----------|
| RClamp3391ZCTFT | 15000 | 7 Inch |
| RailClamp and RClamp are registered trademarks of Semtech Corporation. | | |



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