



**THE DATASHEET OF
FDB075N15A**





ON Semiconductor®

FDP075N15A / FDB075N15A

N-Channel PowerTrench® MOSFET

150 V, 130 A, 7.5 mΩ

Description

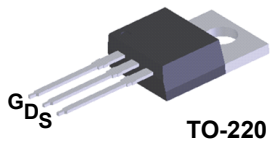
This N-Channel MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Features

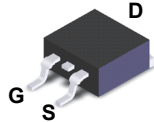
- $R_{DS(on)} = 6.25\text{ m}\Omega$ (Typ.) @ $V_{GS} = 10\text{ V}$, $I_D = 100\text{ A}$
- Fast Switching
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Applications

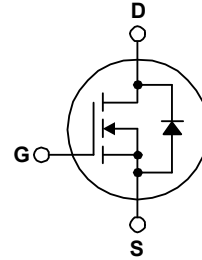
- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter



TO-220



D²-PAK



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDP075N15A-F102 FDB075N15A	Unit
V_{DSS}	Drain to Source Voltage	150	V
V_{GSS}	Gate to Source Voltage	- DC	± 20
		- AC (f > 1 Hz)	± 30
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	130*
		- Continuous ($T_C = 100^\circ\text{C}$)	92
I_{DM}	Drain Current	- Pulsed (Note 1)	522
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	588
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	333
		- Derate Above 25°C	2.22
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

* Package limitation current is 120 A.

Thermal Characteristics

Symbol	Parameter	FDP075N15A-F102 FDB075N15A	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.45	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient, D2-PAK (1 in ² Pad of 2-oz Copper), Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP075N15A-F102	FDP075N15A	TO-220	Tube	N/A	N/A	50 units
FDB075N15A	FDB075N15A	D ² -PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{V}$	150	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.1	-	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120 \text{V}, V_{GS} = 0 \text{V}$ $V_{DS} = 120 \text{V}, T_C = 150^\circ\text{C}$	-	-	1 500	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{V}, V_{DS} = 0 \text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{V}, I_D = 100 \text{A}$	-	6.25	7.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{V}, I_D = 100 \text{A}$	-	164	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 75 \text{V}, V_{GS} = 0 \text{V},$ $f = 1 \text{MHz}$	-	5525	7350	pF
C_{oss}	Output Capacitance		-	516	685	pF
C_{rSS}	Reverse Transfer Capacitance		-	21	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 75 \text{V}, V_{GS} = 0 \text{V}$	-	909	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 75 \text{V}, I_D = 100 \text{A},$ $V_{GS} = 10 \text{V}$	-	77	100	nC
Q_{gs}	Gate to Source Gate Charge		-	26	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	11	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	16	-
ESR	Equivalent Series Resistance(G-S)	$f = 1 \text{MHz}$	-	2.29	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75 \text{V}, I_D = 100 \text{A},$ $V_{GS} = 10 \text{V}, R_G = 4.7 \Omega$	-	28	66	ns
t_r	Turn-On Rise Time		-	37	84	ns
$t_{d(off)}$	Turn-Off Delay Time		-	62	134	ns
t_f	Turn-Off Fall Time		(Note 4)	-	21	52

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	130*	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	520	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{V}, I_{SD} = 100 \text{A}$	-	-	1.25	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{V}, V_{DD} = 75 \text{V}, I_{SD} = 100 \text{A},$	-	97	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100 \text{A}/\mu\text{s}$	-	264	-	nC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. Starting $T_J = 25^\circ\text{C}$, $L = 3 \text{mH}$, $I_{AS} = 19.8 \text{A}$.
3. $I_{SD} \leq 100 \text{A}$, $di/dt \leq 200 \text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

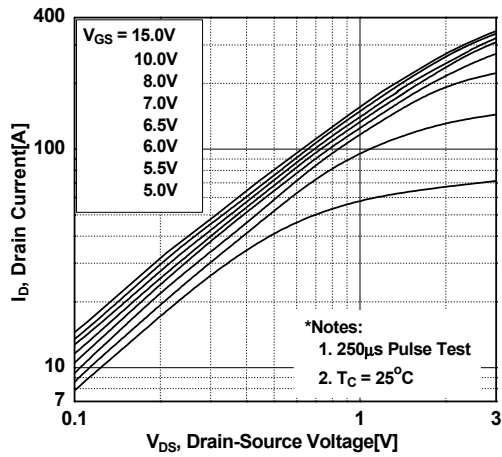


Figure 2. Transfer Characteristics

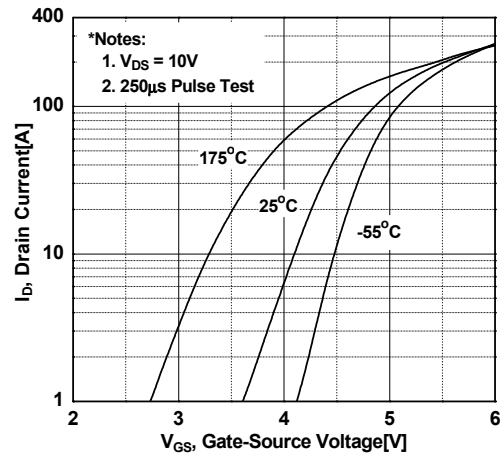


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

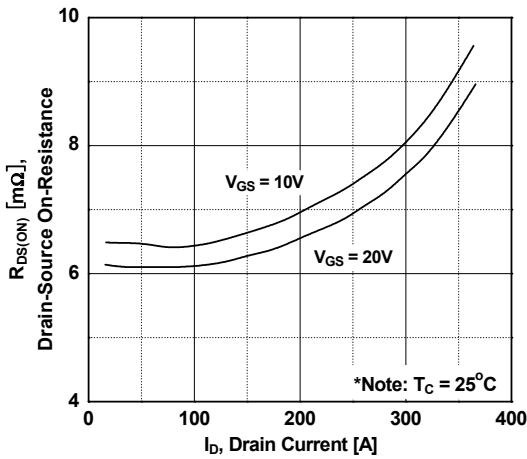


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

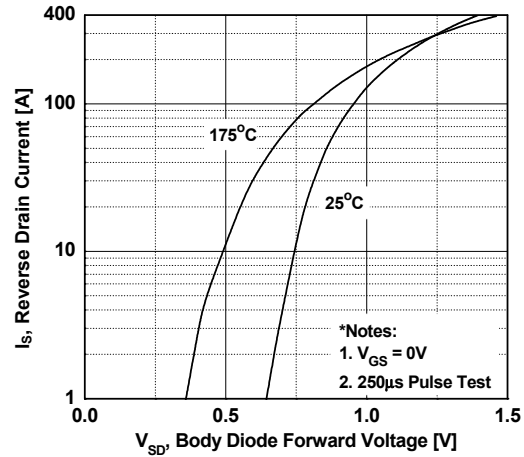


Figure 5. Capacitance Characteristics

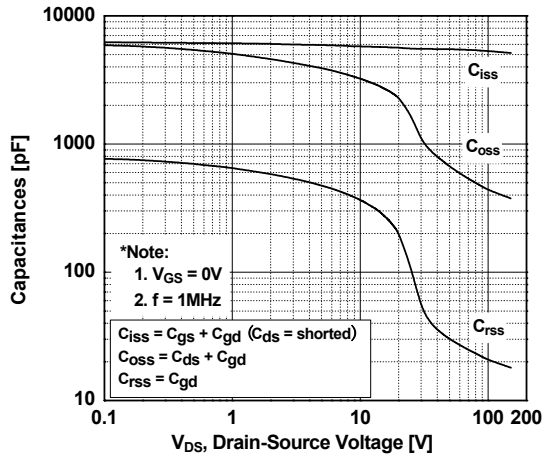
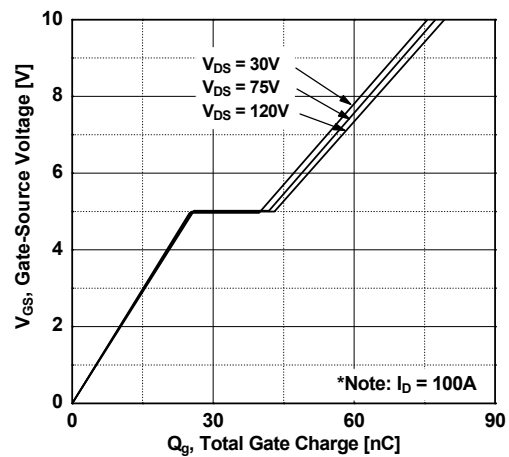


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

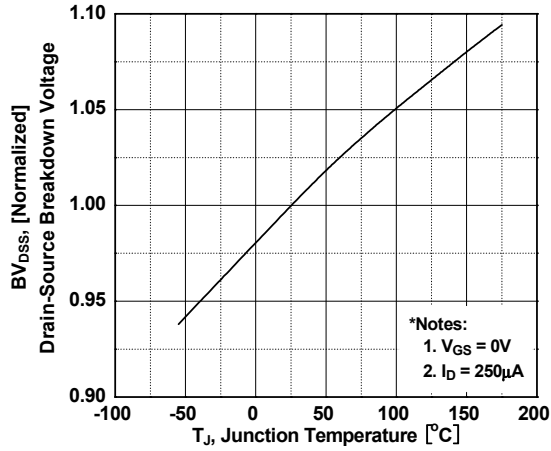


Figure 8. On-Resistance Variation vs. Temperature

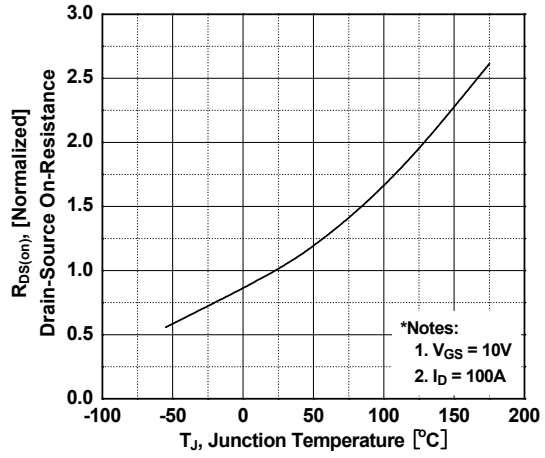


Figure 9. Maximum Safe Operating Area

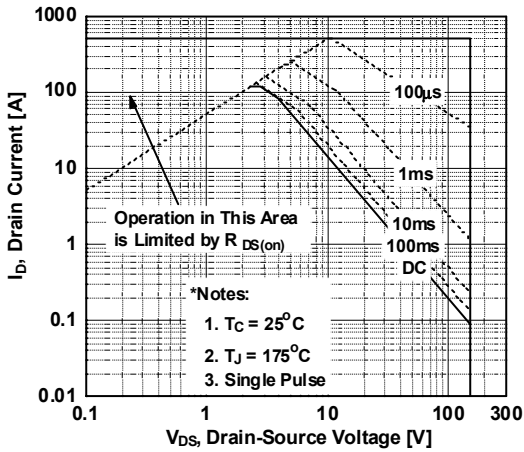


Figure 10. Maximum Drain Current vs. Case Temperature

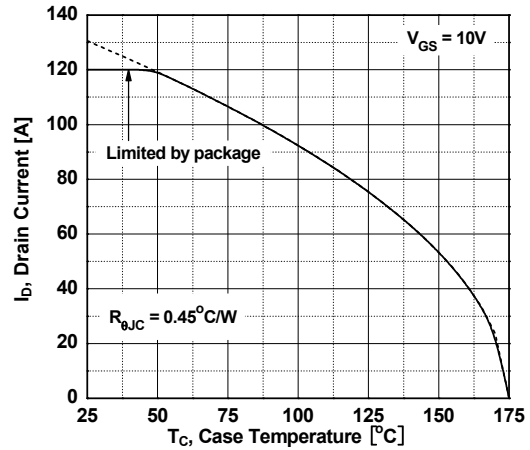


Figure 11. Eoss vs. Drain to Source Voltage

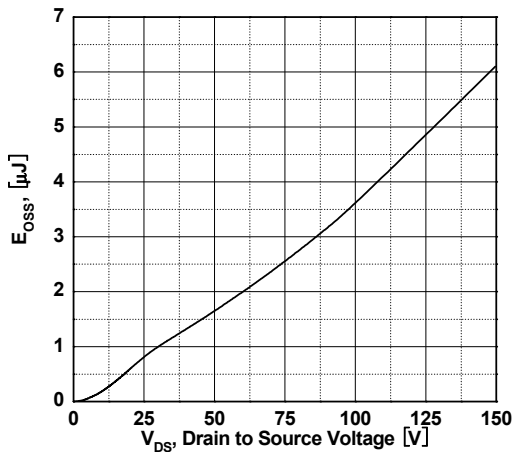
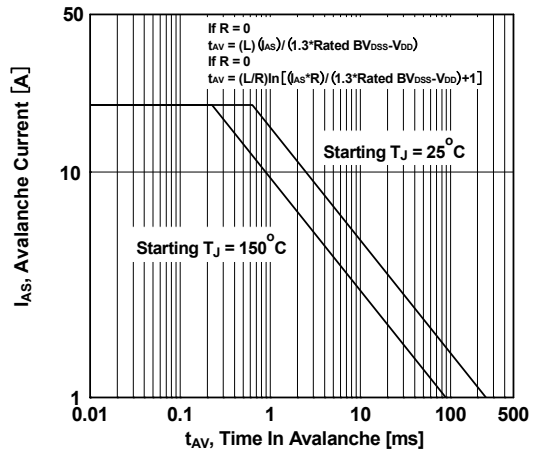
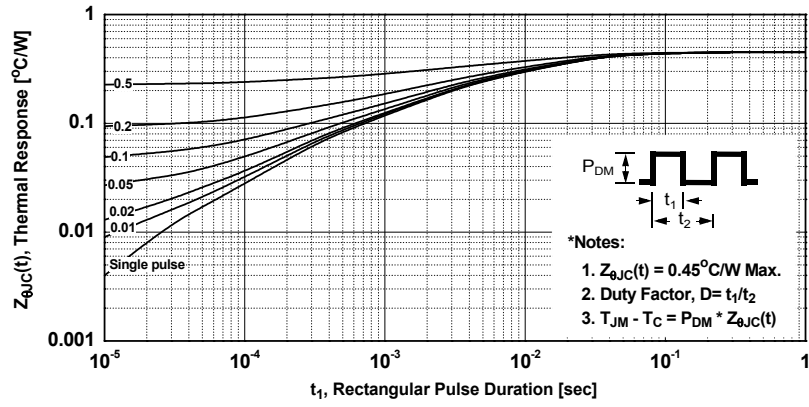


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve



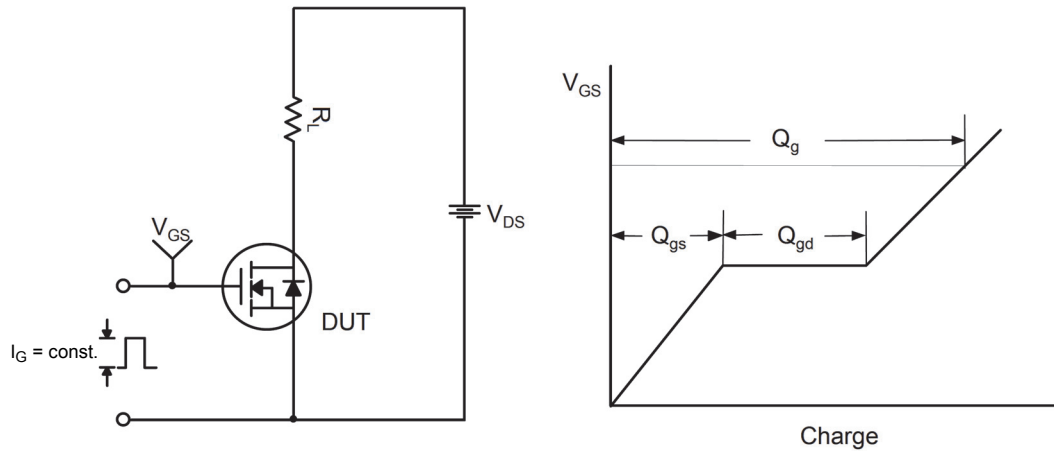


Figure 14. Gate Charge Test Circuit & Waveform

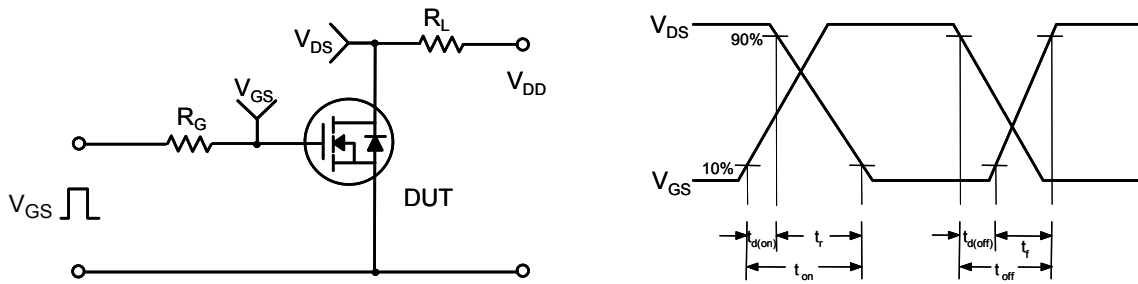


Figure 15. Resistive Switching Test Circuit & Waveforms



Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

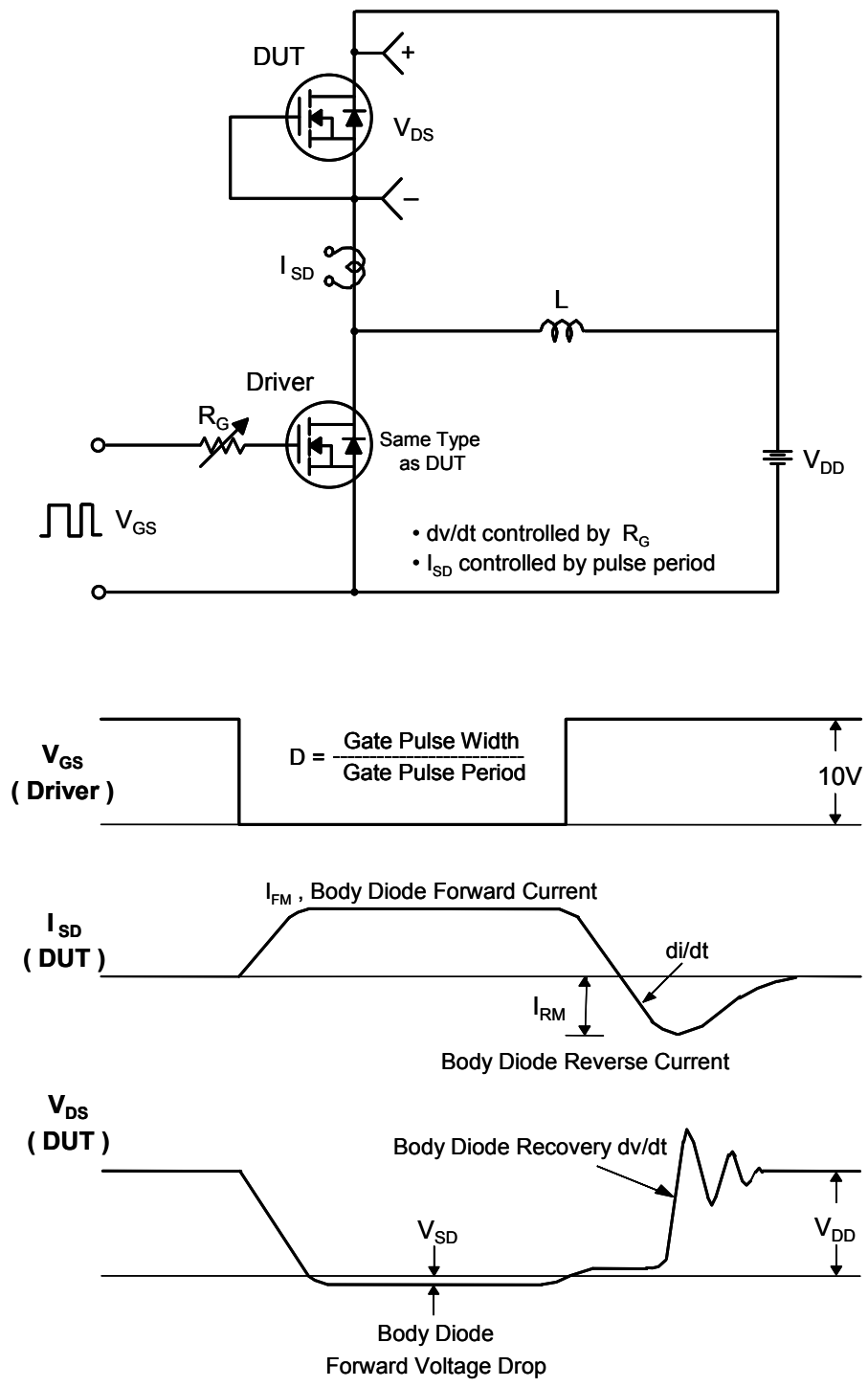


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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