



THE DATASHEET OF FDJ128N



FDJ128N

N-Channel 2.5 V_{GS} Specified PowerTrench® MOSFET

General Description

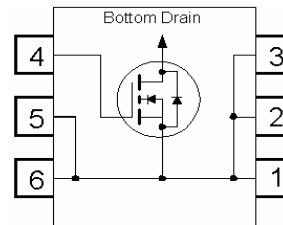
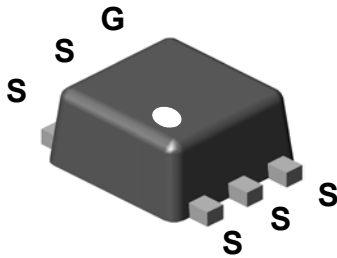
This N-Channel -2.5V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

Applications

- Battery management

Features

- 5.5 A, 20 V. $R_{DS(ON)} = 35\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
 $R_{DS(ON)} = 51\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- Compact industry standard SC75-6 surface mount package



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	20	V
V _{GSS}	Gate-Source Voltage	± 12	V
I _D	Drain Current – Continuous (Note 1a)	5.5	A
	– Pulsed	16	
P _D	Power Dissipation for Single Operation (Note 1a)	1.6	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	77	°C/W
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Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.B	FDJ128N	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		12		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-0.3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 5.5\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 4.7\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 5.5\text{ A}, T_J = 125^\circ\text{C}$		29 41 38	35 51 53	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	8			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 5.5\text{ A}$		19		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$		543		pF
C_{oss}	Output Capacitance	$f = 1.0\text{ MHz}$		125		pF
C_{riss}	Reverse Transfer Capacitance			65		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		2.0		Ω

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A}$		7	15	ns
t_r	Turn–On Rise Time	$V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		5	11	ns
$t_{d(off)}$	Turn–Off Delay Time			14	24	ns
t_f	Turn–Off Fall Time			3	7	ns
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 5.5\text{ A}$		5	8	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = 5\text{ V}$		1.2		nC
Q_{gd}	Gate–Drain Charge			1.4		nC

Drain–Source Diode Characteristics and Maximum Ratings

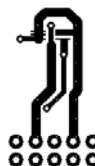
I_S	Maximum Continuous Drain–Source Diode Forward Current				1.3	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)		0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 5.5\text{ A}$		12		nS
Q_{rr}	Diode Reverse Recovery Charge	$dI_F/dt = 100\text{ A}/\mu\text{s}$		3		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) 77°C/W when mounted on a 1 in^2 pad of 2 oz copper.



- b) 115°C/W when mounted on a minimum pad of 2 oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

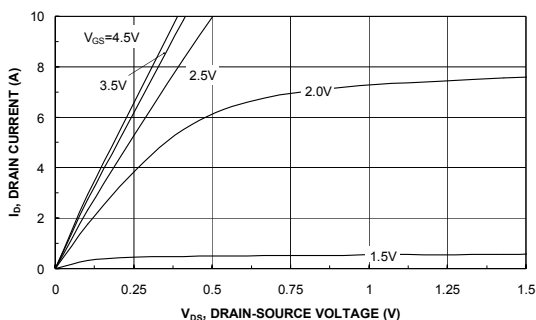


Figure 1. On-Region Characteristics.

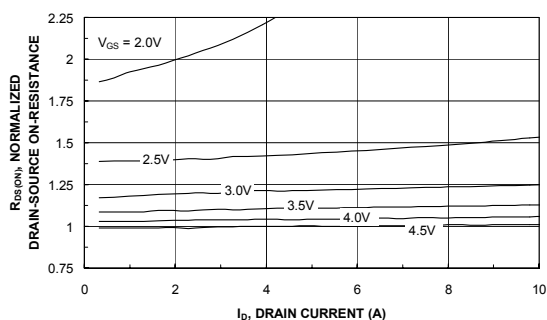


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

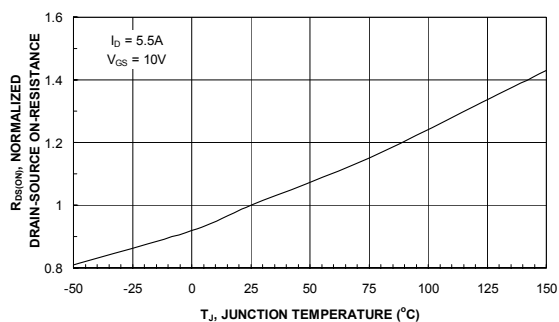


Figure 3. On-Resistance Variation with Temperature.

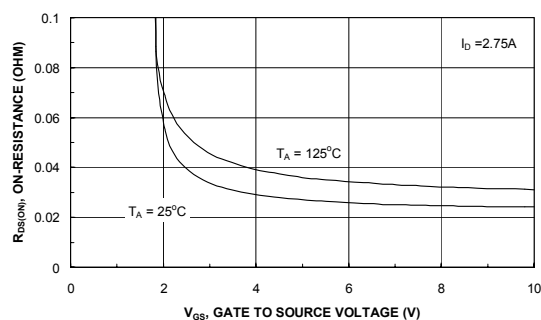


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

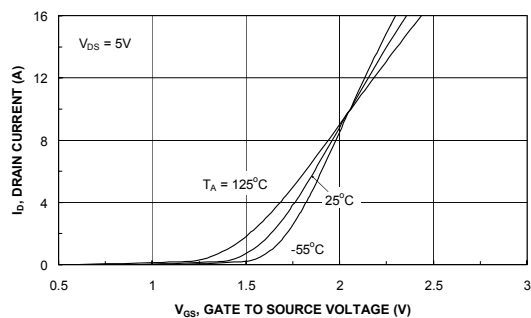


Figure 5. Transfer Characteristics.

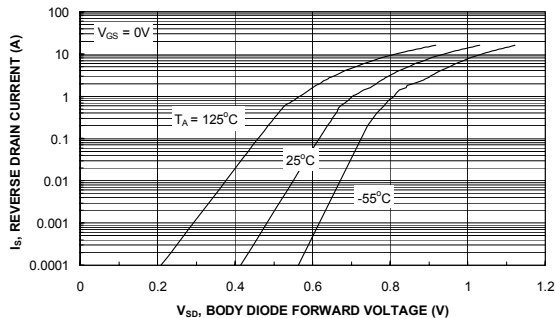


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

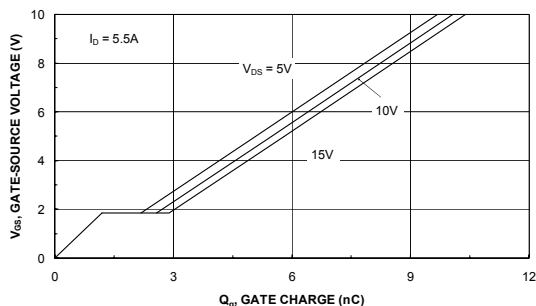


Figure 7. Gate Charge Characteristics.

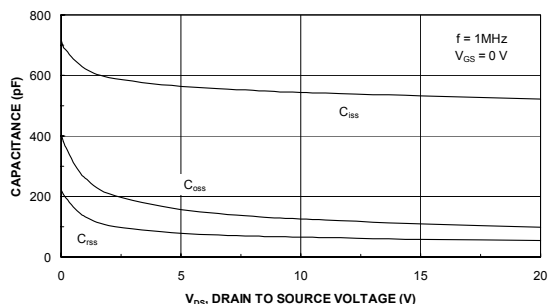


Figure 8. Capacitance Characteristics.

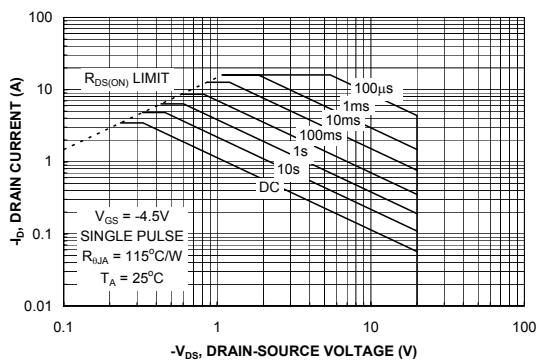


Figure 9. Maximum Safe Operating Area.

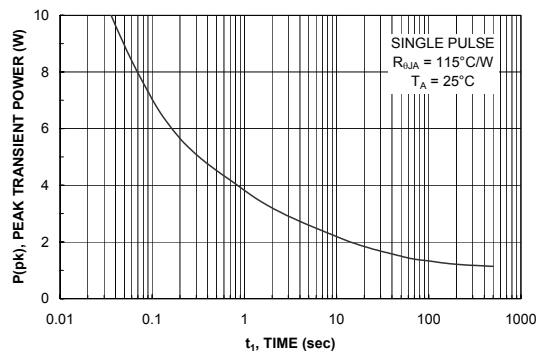


Figure 10. Single Pulse Maximum Power Dissipation.

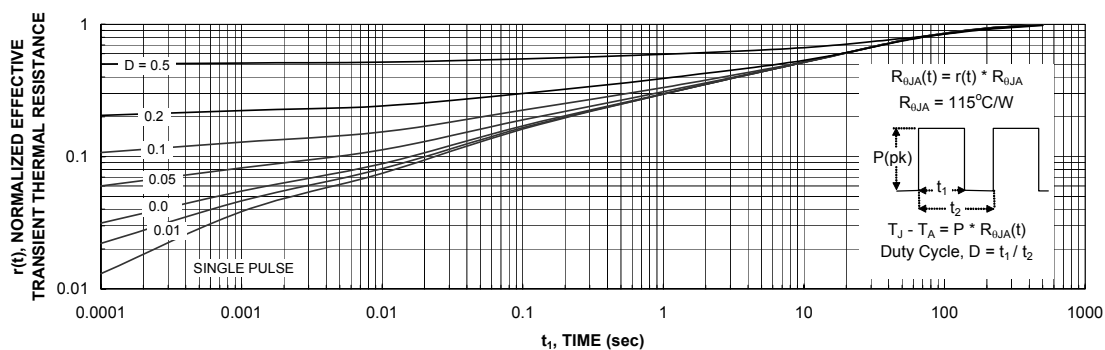
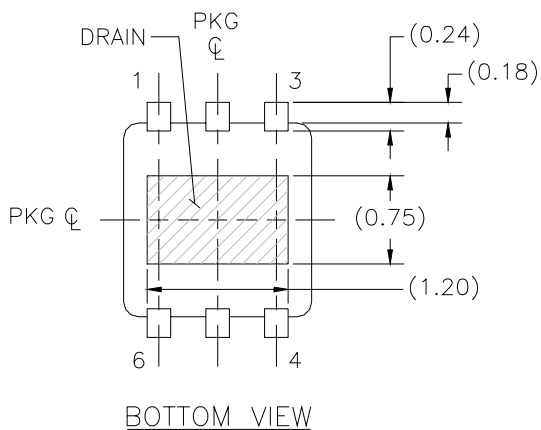
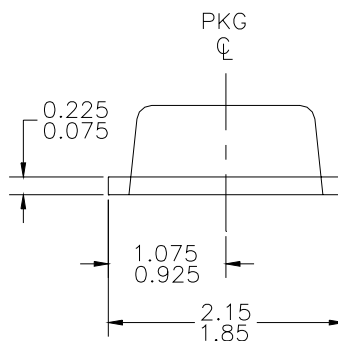
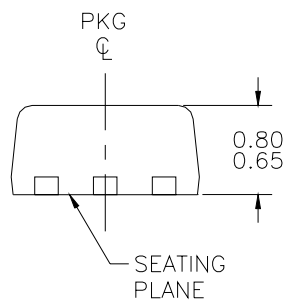
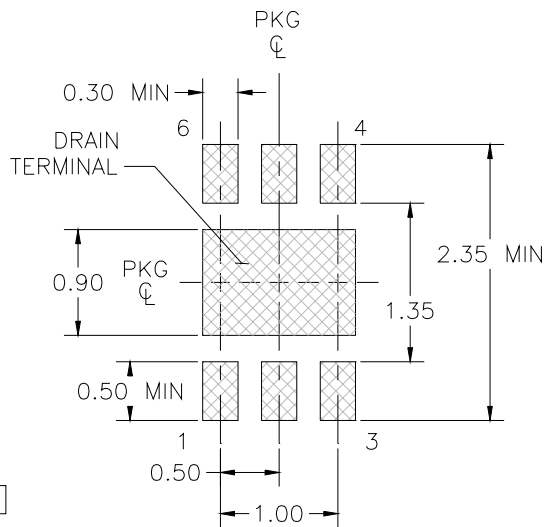
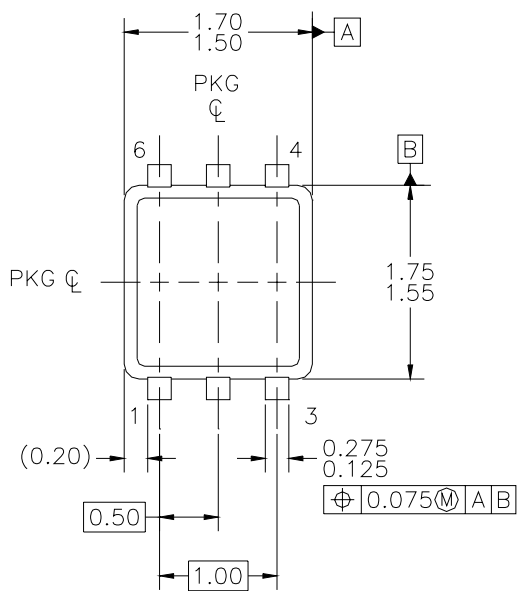


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) NO PACKAGE STANDARD REFERENCE AS OF JULY 13, 2000.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

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