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# FDMC2610

## N-Channel UltraFET Trench<sup>®</sup> MOSFET

200V, 9.5A, 200mΩ

### Features

- Max  $r_{DS(on)}$  = 200mΩ at  $V_{GS} = 10V$ ,  $I_D = 2.2A$
- Max  $r_{DS(on)}$  = 215mΩ at  $V_{GS} = 6V$ ,  $I_D = 1.5A$
- Low Profile - 1mm Max in a Power 33
- RoHS Compliant

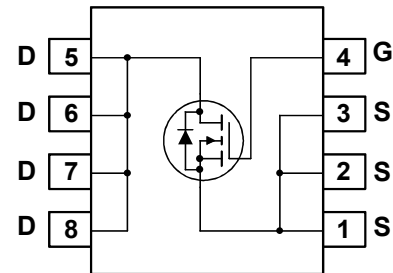
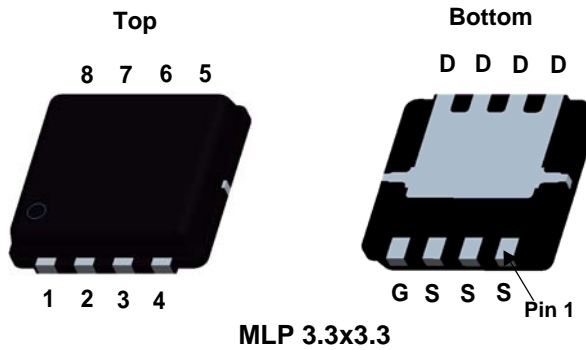


### General Description

This N-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced Power Trench process. It has been optimized for power management applications.

### Application

- DC - DC Conversion



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	200	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	9.5	A
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	2.2	
	-Pulsed	15	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	6	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	42	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC2610	FDMC2610	MLP 3.3x3.3	13"	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	200			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		199		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 160\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-9.9		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 2.2\text{A}$		175	200	$\text{m}\Omega$
		$V_{GS} = 6\text{V}, I_D = 1.5\text{A}$		188	215	
		$V_{GS} = 10\text{V}, I_D = 2.2\text{A}, T_J = 125^\circ\text{C}$		347	397	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 2.2\text{A}$		7		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		720	960	pF
$C_{oss}$	Output Capacitance			41	55	pF
$C_{rss}$	Reverse Transfer Capacitance			12	20	pF
$R_g$	Gate Resistance		$f = 1\text{MHz}$		0.7	$\Omega$

### Switching Characteristics

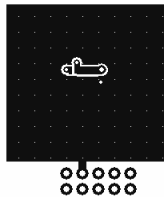
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{V}, I_D = 2.2\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 24\Omega$		17	31	ns
$t_r$	Rise Time			13	24	ns
$t_{d(off)}$	Turn-Off Delay Time			29	47	ns
$t_f$	Fall Time			16	29	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V to } 10\text{V}, V_{DD} = 100\text{V}, I_D = 2.2\text{A}$		12.3	18	nC
$Q_{gs}$	Gate to Source Gate Charge			3		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			3.6		nC

### Drain-Source Diode Characteristics

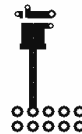
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 2.2\text{A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 2.2\text{A}, di/dt = 100\text{A}/\mu\text{s}$		69	104	ns
$Q_{rr}$	Reverse Recovery Charge			114	171	nC

#### Notes:

1:  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $60^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



b.  $135^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 3\text{mH}, I_{AS} = 2\text{A}, V_{DD} = 200\text{V}, V_{GS} = 10\text{V}$ .

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

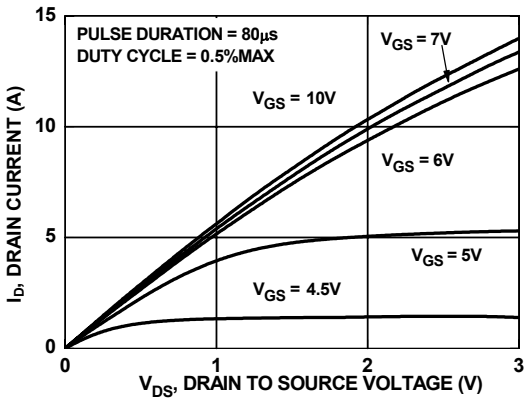


Figure 1. On-Region Characteristics

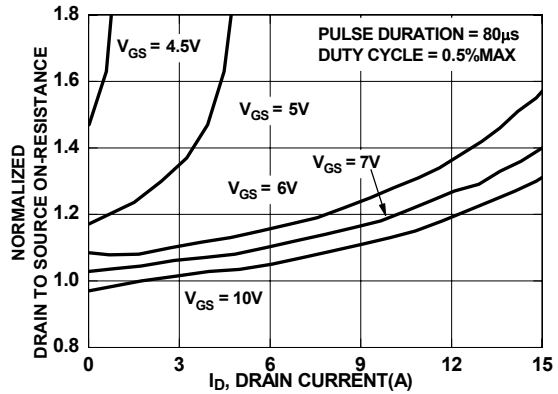


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

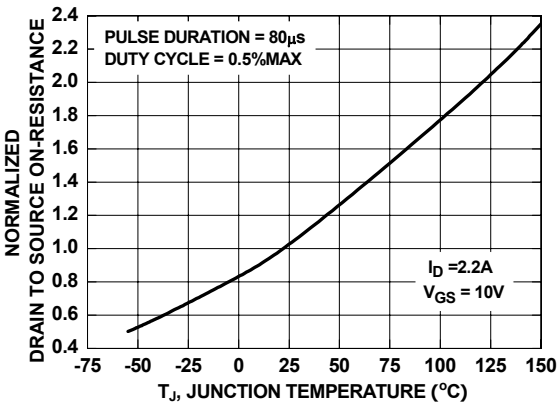


Figure 3. Normalized On-Resistance vs Junction Temperature

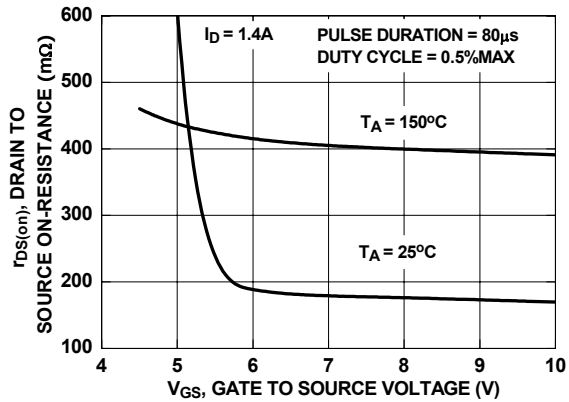


Figure 4. On-Resistance vs Gate to Source Voltage

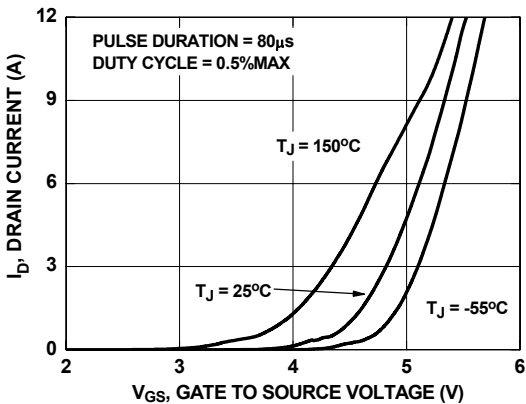


Figure 5. Transfer Characteristics

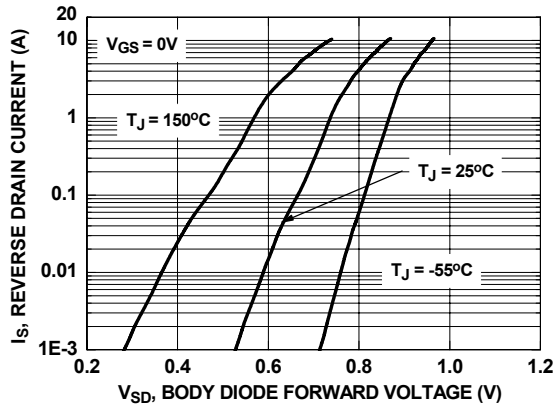
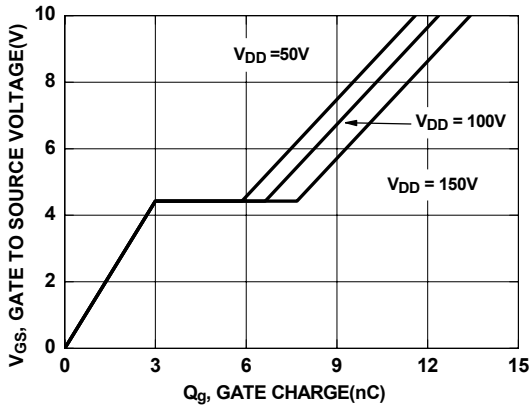
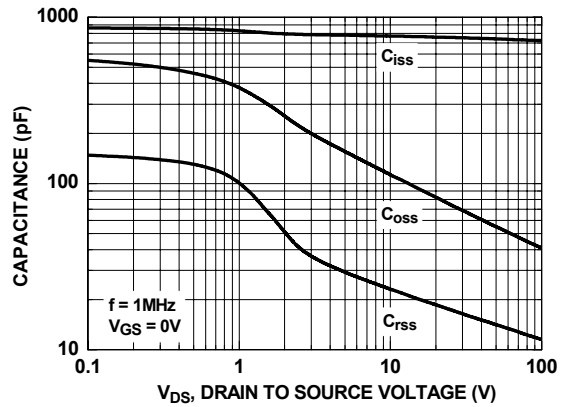


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

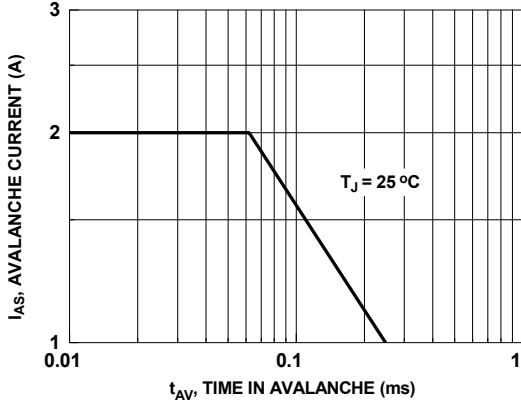
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



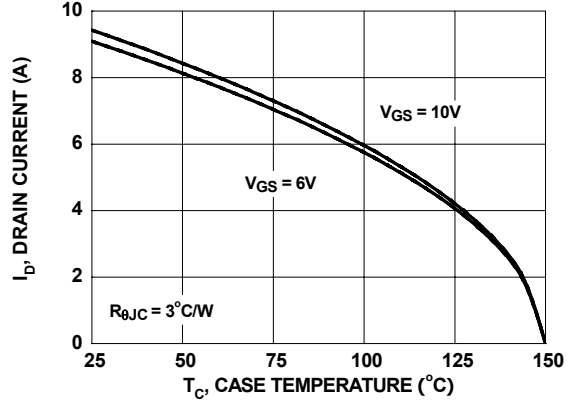
**Figure 7. Gate Charge Characteristics**



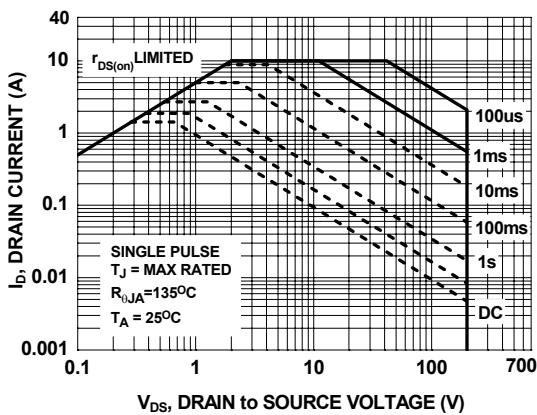
**Figure 8. Capacitance vs Drain to Source Voltage**



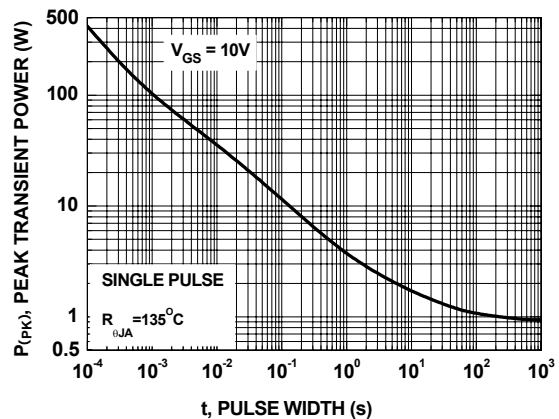
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

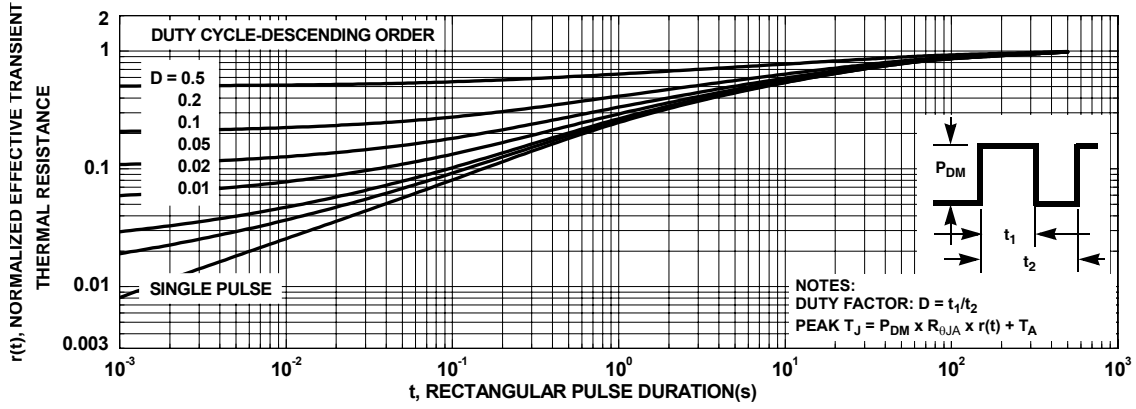


**Figure 11. Forward Bias Safe Operating Area**

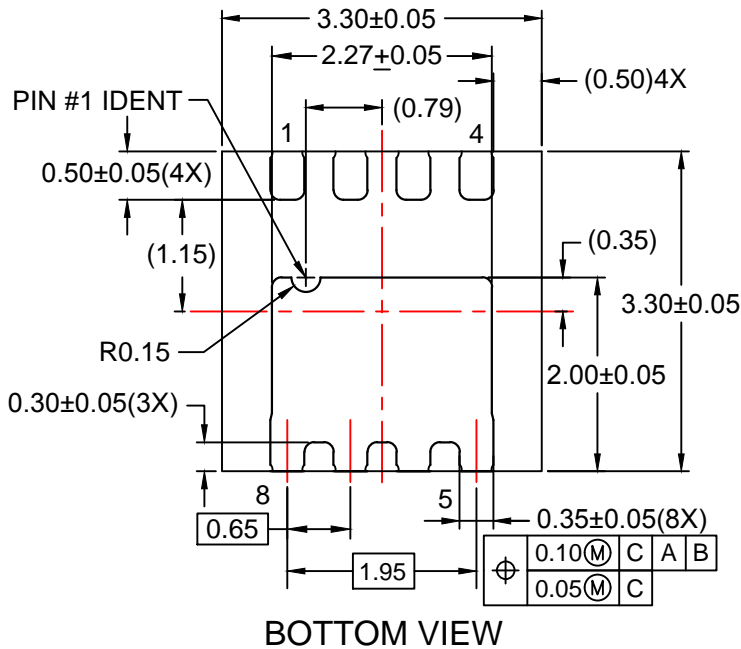
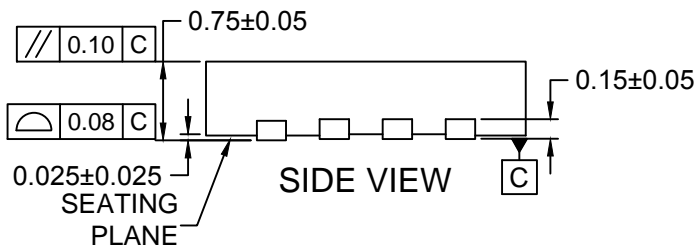
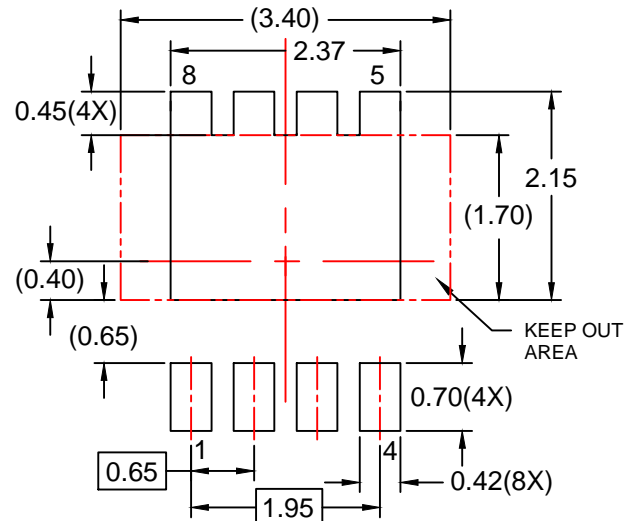
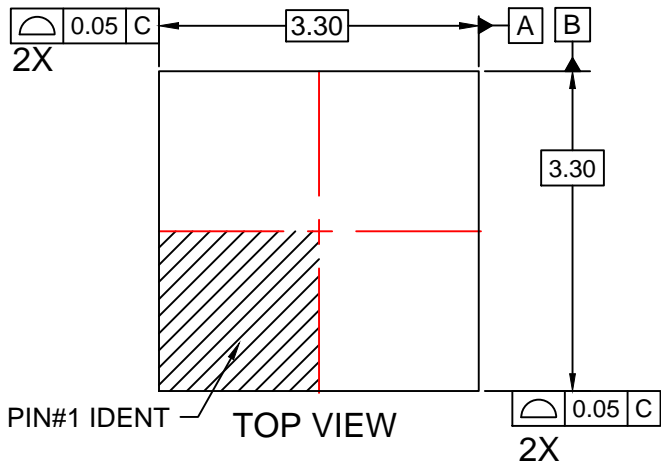


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



**Figure 13. Transient Thermal Response Curve**



NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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