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FDPF5N50NZF

N-Channel UniFET™ II FRFET® MOSFET

500 V, 4.2 A, 1.75 Ω

Features

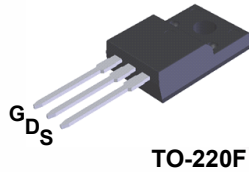
- $R_{DS(on)} = 1.57 \Omega$ (Typ.) @ $V_{GS} = 10 V, I_D = 2.1 A$
- Low Gate Charge (Typ. 9 nC)
- Low C_{rss} (Typ. 4 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Applications

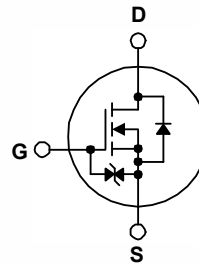
- LCD/LED TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. The body diode's reverse recovery performance of UniFET II FRFET® MOSFET has been enhanced by lifetime control. Its t_{rr} is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



TO-220F



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FDPF5N50NZF	Unit
V_{DSS}	Drain to Source Voltage	500	V
V_{GSS}	Gate to Source Voltage	±25	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ C$)	4.2*
		- Continuous ($T_C = 100^\circ C$)	2.5*
I_{DM}	Drain Current	- Pulsed (Note 1)	16*
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	165
I_{AR}	Avalanche Current	(Note 1)	4.2
E_{AR}	Repetitive Avalanche Energy	(Note 1)	7.8
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	20
P_D	Power Dissipation	($T_C = 25^\circ C$)	30
		- Derate above $25^\circ C$	0.24
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDPF5N50NZF	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDPF5N50NZF	FDPF5N50NZF	TO-220F	Tube	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_C = 25^\circ\text{C}$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.5	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$	-	-	10	μA
		$V_{DS} = 400\text{V}, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	-	-	100	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 2.1\text{A}$	-	1.57	1.75	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 2.1\text{A}$	-	4.2	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	365	485	pF
C_{oss}	Output Capacitance		-	50	65	pF
C_{rss}	Reverse Transfer Capacitance		-	4	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400\text{V}, I_D = 4.2\text{A}$ $V_{GS} = 10\text{V}$	-	9	12	nC
Q_{gs}	Gate to Source Gate Charge		-	2	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	4	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}, I_D = 4.2\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 25\Omega$	-	12	35	ns
t_r	Turn-On Rise Time		-	19	50	ns
$t_{d(off)}$	Turn-Off Delay Time		-	31	70	ns
t_f	Turn-Off Fall Time		(Note 4)	-	22	55

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	4.2	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	16	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 4.2\text{A}$	-	-	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 4.2\text{A}$	-	87	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$	-	0.15	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 18.7\text{mH}, I_{AS} = 4.2\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 4.2\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Figure 1. On-Region Characteristics

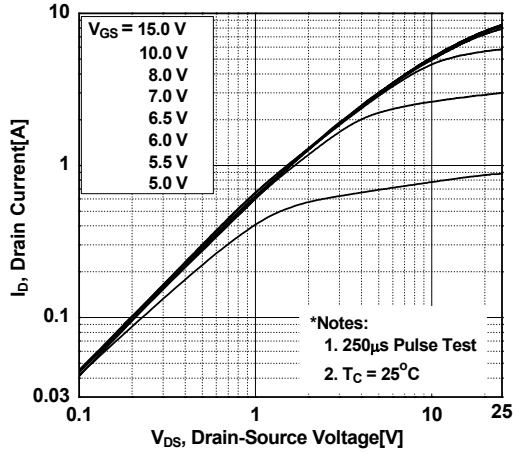


Figure 2. Transfer Characteristics

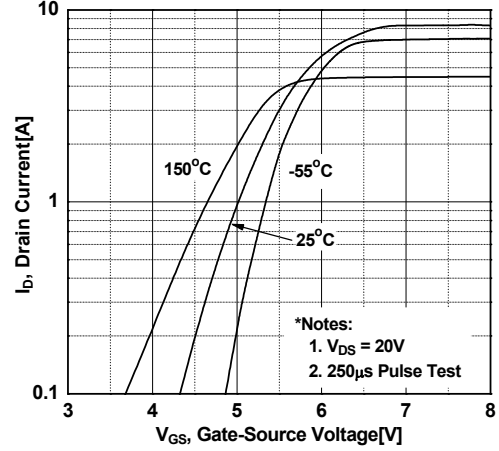


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

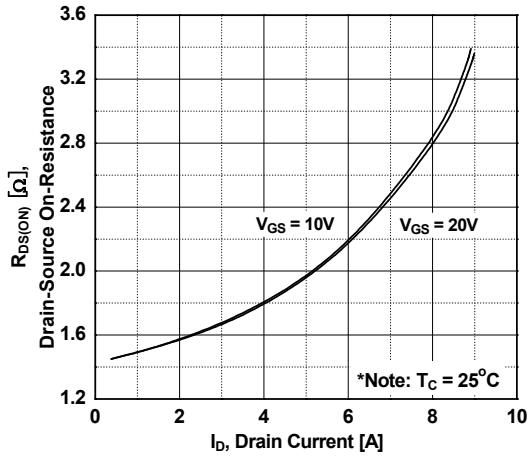


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

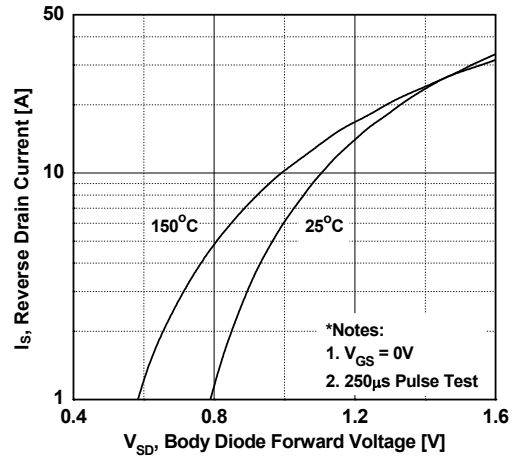


Figure 5. Capacitance Characteristics

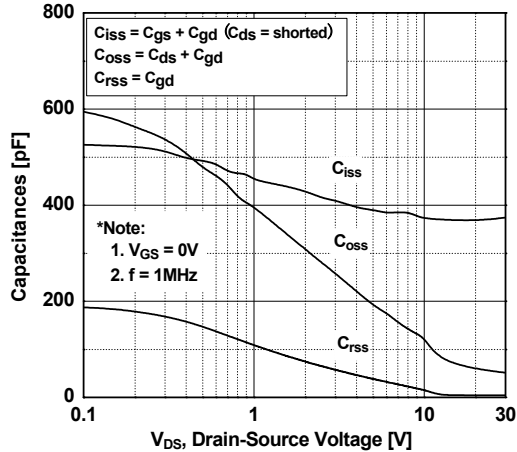
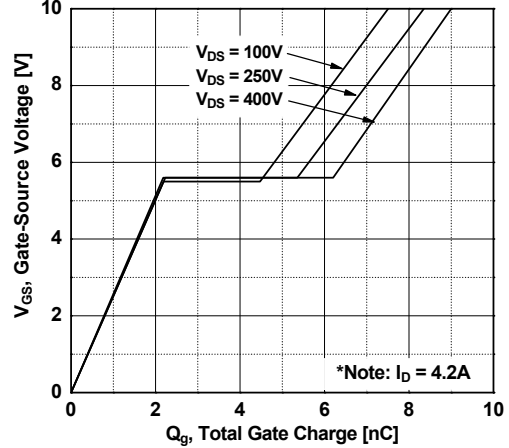


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

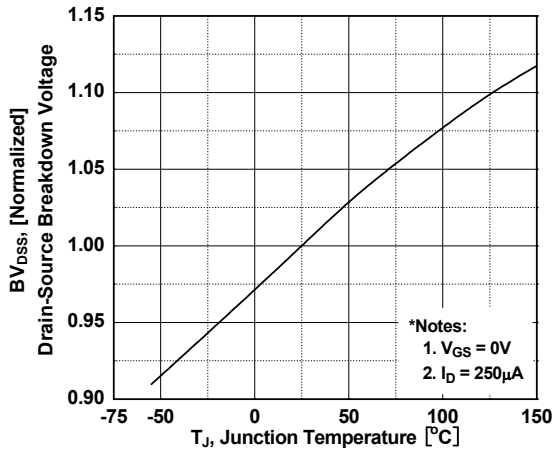


Figure 8. Maximum Safe Operating Area vs. Case Temperature-FDPF5N50NZF

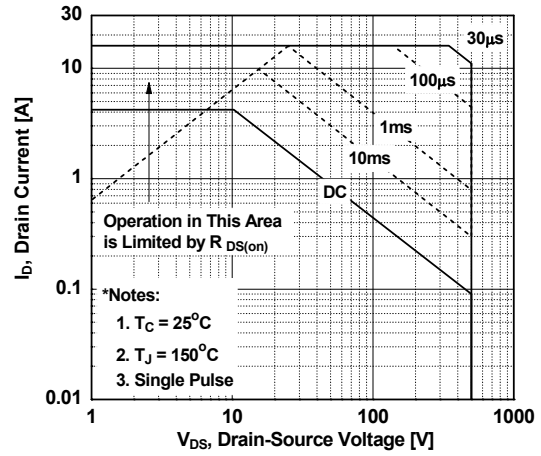


Figure 9. Maximum Drain Current

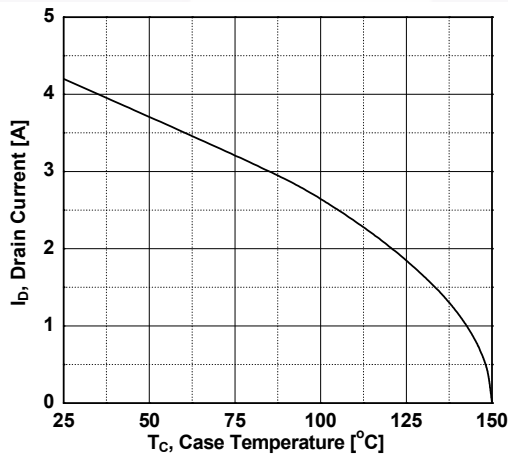


Figure 10. Transient Thermal Response Curve-FDPF5N50NZF

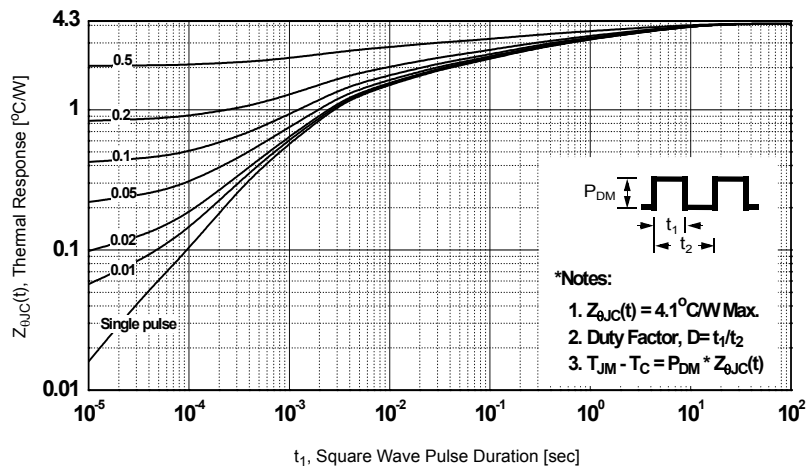


Figure 11. Gate Charge Test Circuit & Waveform

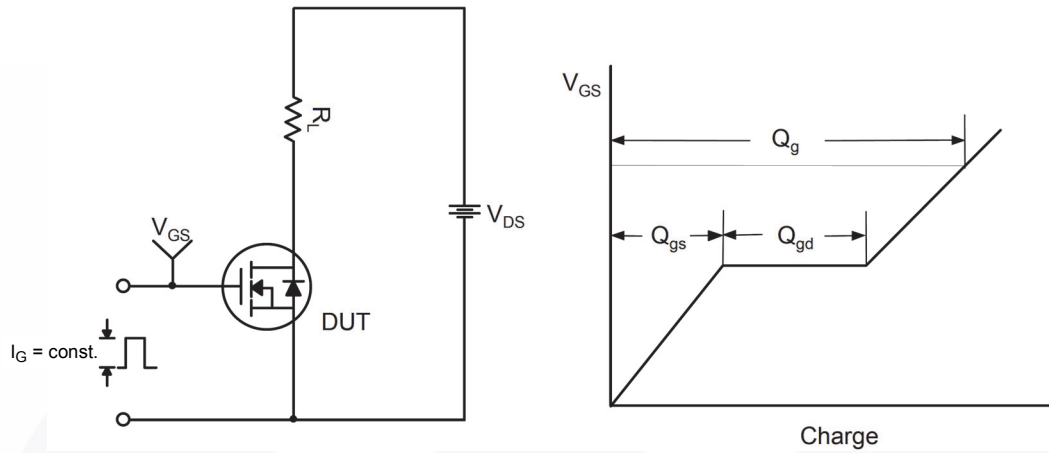


Figure 12. Resistive Switching Test Circuit & Waveforms

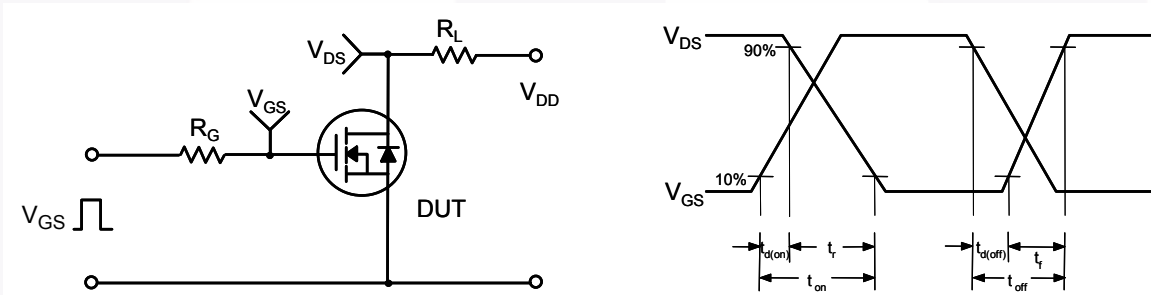


Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

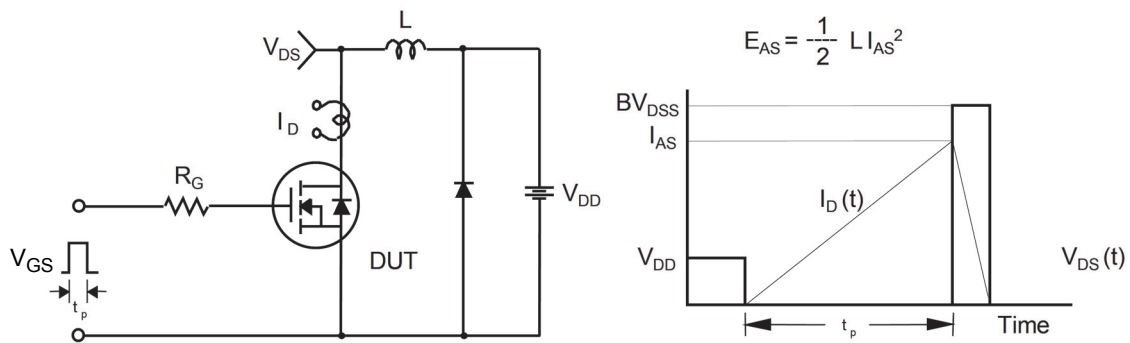
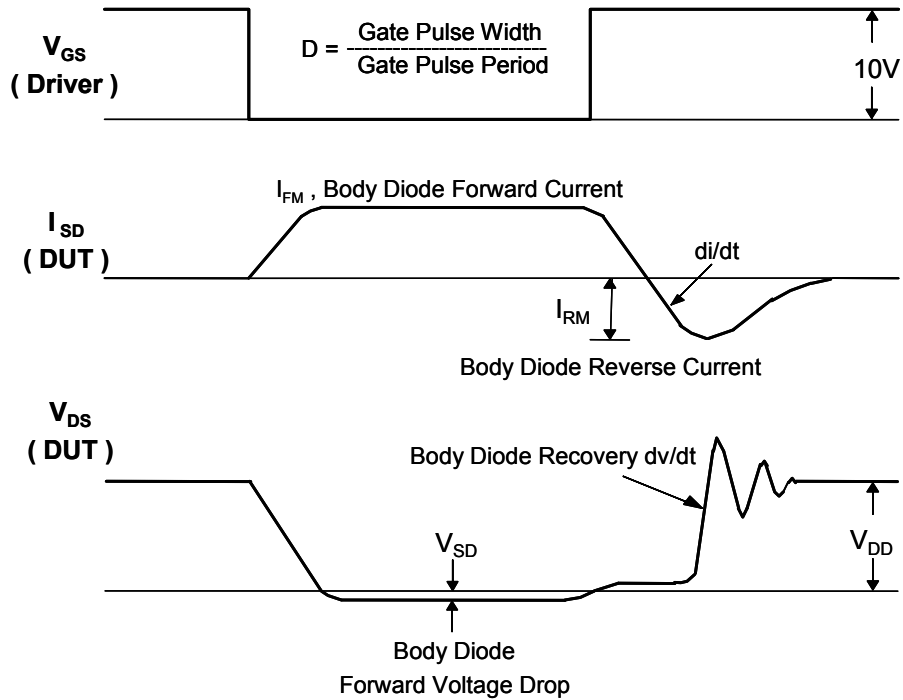
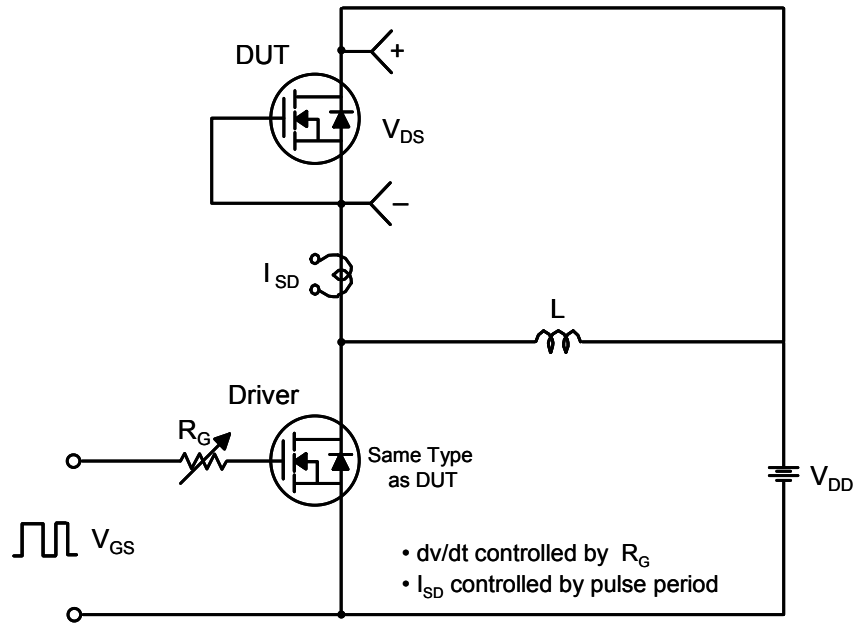


Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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