



**THE DATASHEET OF  
FDPF7N50U\_G**



# FDPF7N50U / FDPF7N50U\_G

## N-Channel UniFET™ Ultra FRFET™ MOSFET

500 V, 5 A, 1.5 Ω

### Features

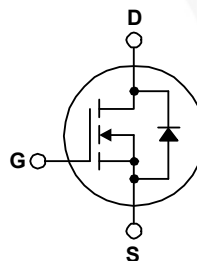
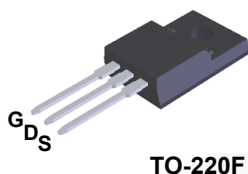
- $R_{DS(on)} = 1.5 \Omega$  (Max.) @  $V_{GS} = 10 V$ ,  $I_D = 2.5 A$
- Low Gate Charge (Typ. 12.8 nC)
- Low  $C_{rss}$  (Typ. 9 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability

### Applications

- LCD/LED TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

### Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. UniFET Ultra FRFET™ MOSFET has much superior body diode reverse recovery performance. Its  $t_{rr}$  is less than 50nsec and the reverse dv/dt immunity is 20V/nsec while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore UniFET Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FDPF7N50U / FDPF7N50U_G	Unit
$V_{DSS}$	Drain-Source Voltage	500	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ C$ )	5*
		- Continuous ( $T_C = 100^\circ C$ )	3*
$I_{DM}$	Drain Current	- Pulsed (Note 1)	20*
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	125	mJ
$I_{AR}$	Avalanche Current (Note 1)	5	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	8.9	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ C$ )	31.3
		- Derate above $25^\circ C$	0.25
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ C$

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	FDPF7N50U / FDPF7N50U_G	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	4.0	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDPF7N50U	FDPF7N50U	TO-220F	Tube	N/A	N/A	50 units
FDPF7N50U_G	FDPF7N50U	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

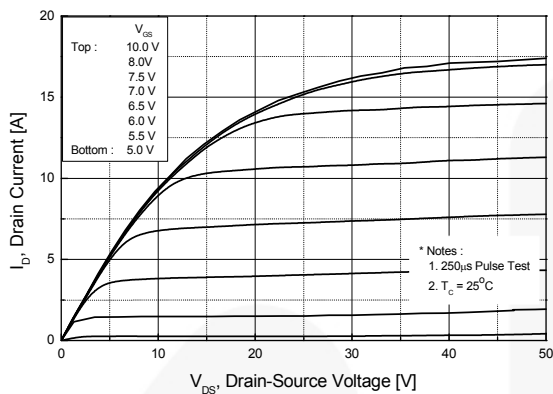
Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.5	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C	--	--	25 250	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.5 A	--	1.2	1.5	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 2.5 A	--	2.5	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	720	940	pF
C <sub>oss</sub>	Output Capacitance		--	95	190	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	9	13.5	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 5 A R <sub>G</sub> = 25 Ω	--	6	20	ns
t <sub>r</sub>	Turn-On Rise Time		--	55	120	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	25	60	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	--	35	80
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 5 A V <sub>GS</sub> = 10 V	--	12.8	16.6	nC
Q <sub>gs</sub>	Gate-Source Charge		--	3.7	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4)	--	5.8	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	5	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	20	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 5 A	--	--	1.6	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 5 A di <sub>F</sub> /dt = 100 A/μs	--	40	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.04	--	μC

### NOTES:

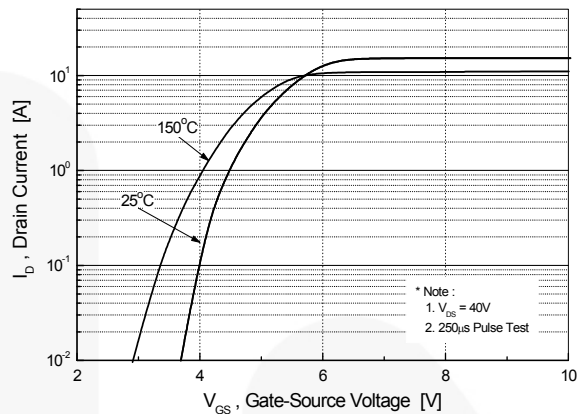
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 10 mH, I<sub>AS</sub> = 5 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 5 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

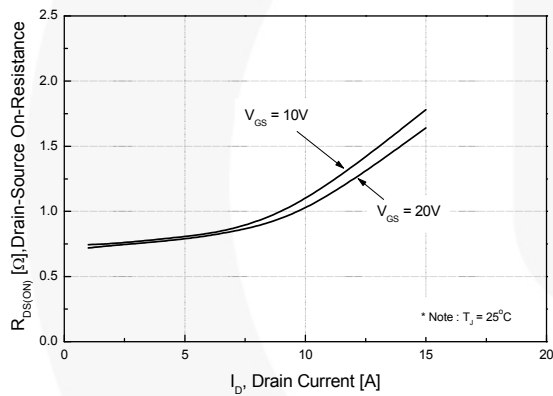
**Figure 1. On-Region Characteristics**



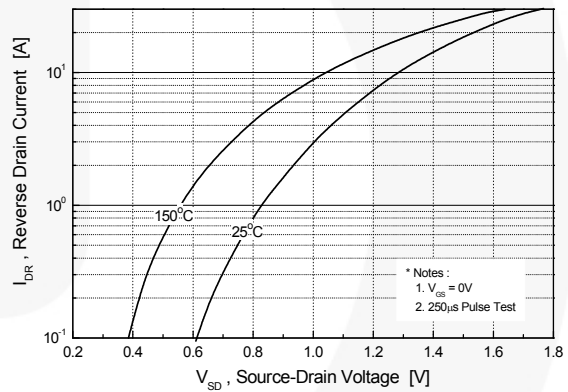
**Figure 2. Transfer Characteristics**



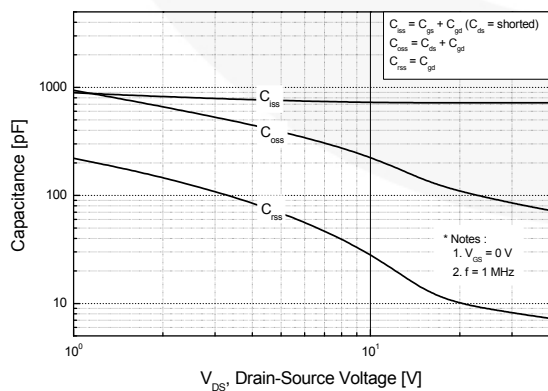
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



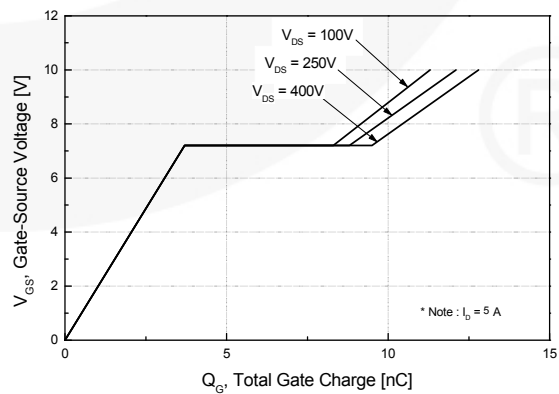
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

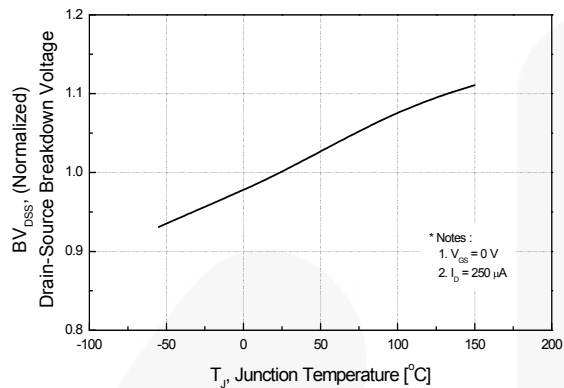


**Figure 6. Gate Charge Characteristics**

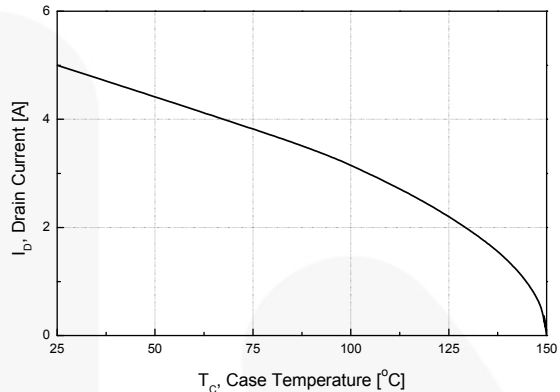


**Typical Performance Characteristics** (Continued)

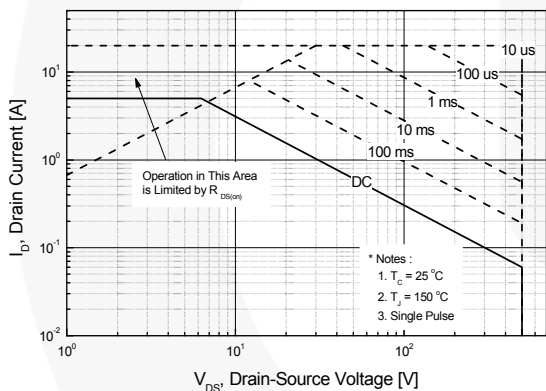
**Figure 7. Breakdown Voltage Variation vs. Temperature**



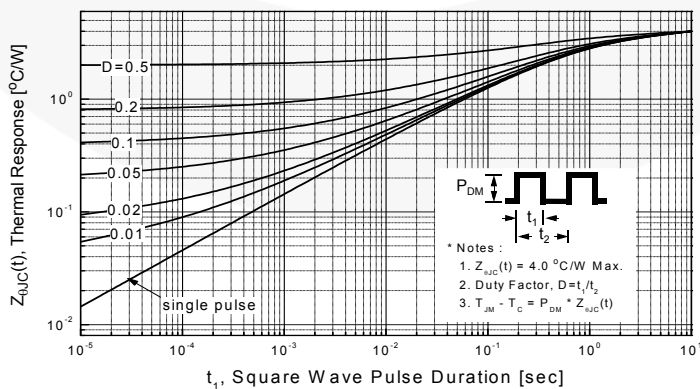
**Figure 8. Maximum Drain Current Vs. Case Temperature**

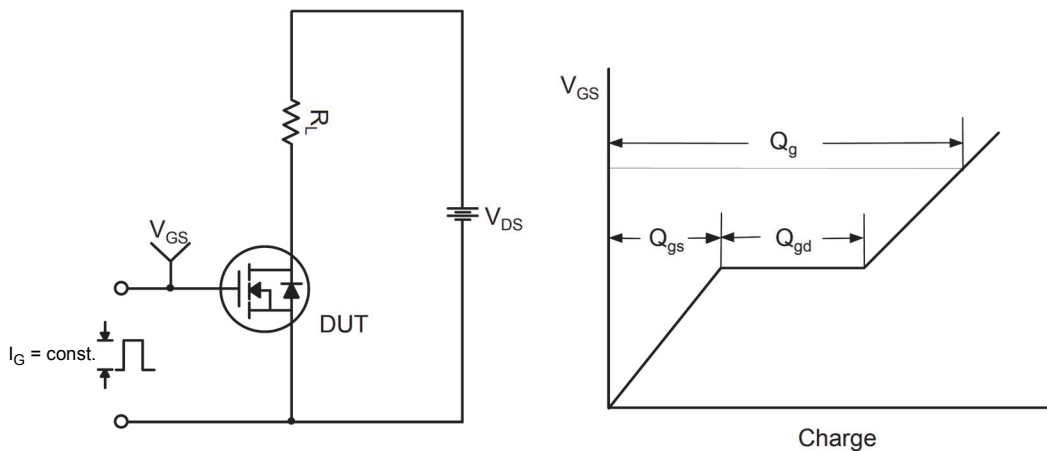


**Figure 9. Maximum Safe Operating Area**

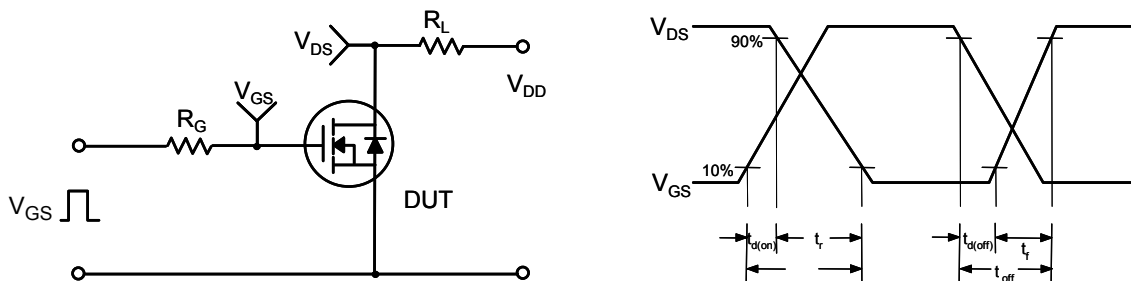


**Figure 10. Transient Thermal Response Curve**

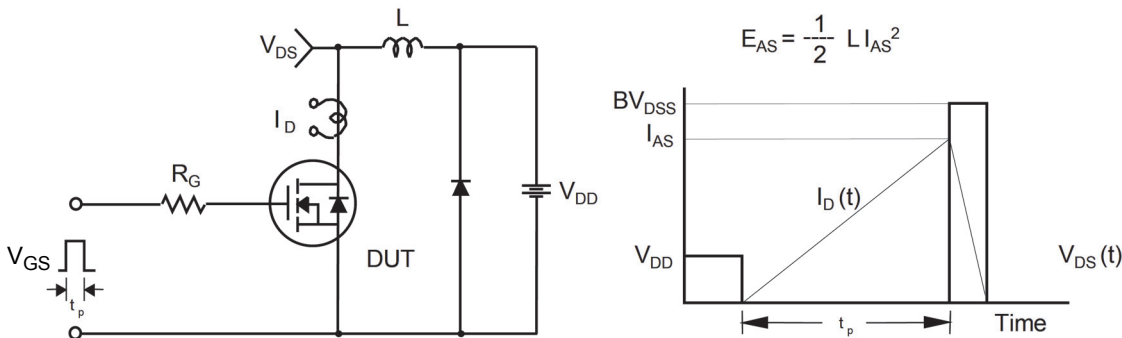




**Figure 11. Gate Charge Test Circuit & Waveform**



**Figure 12. Resistive Switching Test Circuit & Waveforms**



**Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms**

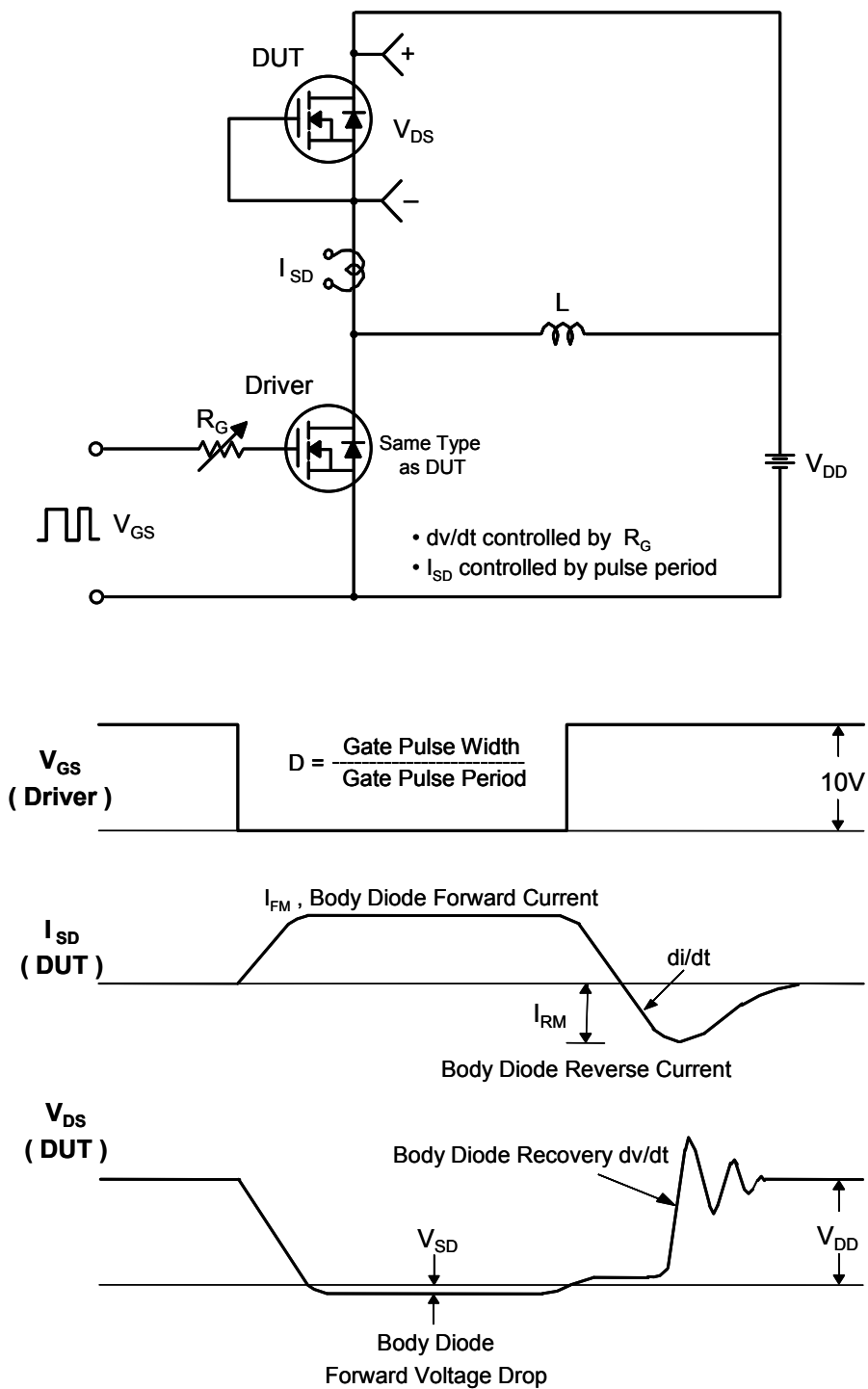
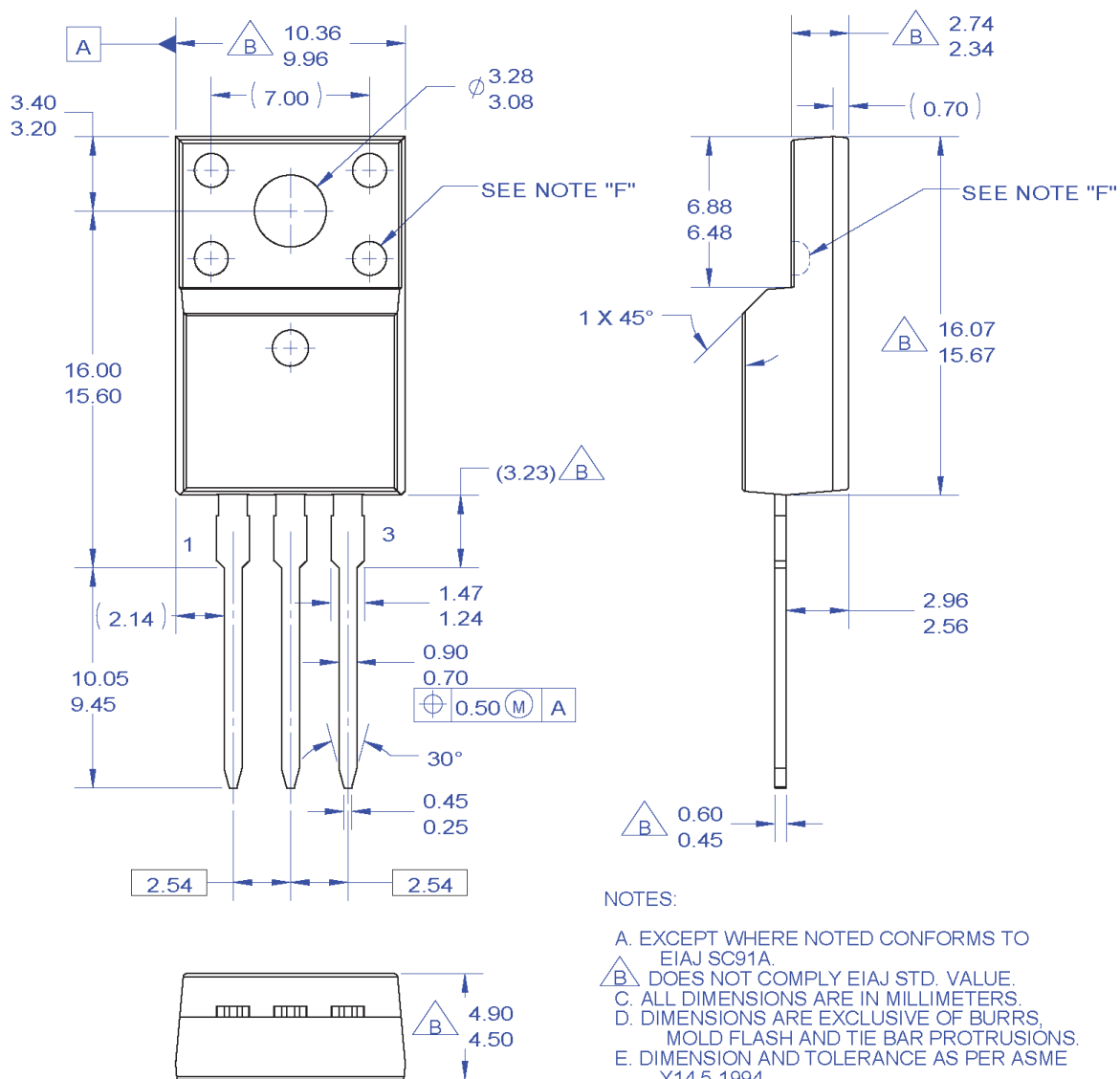


Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 15. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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