



**THE DATASHEET OF
FDQ7238AS**



FDQ7238AS

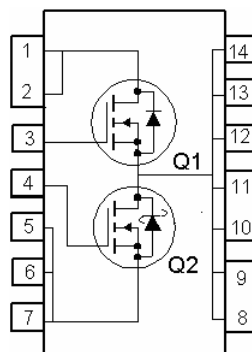
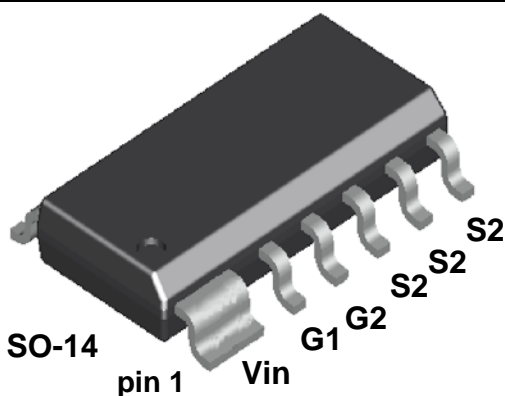
Dual Notebook Power Supply N-Channel PowerTrench® in SO-14 Package

General Description

The FDQ7238AS is designed to replace two single SO-8 MOSFETs in DC to DC power supplies. The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized to reduce conduction losses using Fairchild's SyncFET™ technology. The FDQ7238AS includes a patented combination of a MOSFET monolithically integrated with a Schottky diode.

Features

- **Q2:** 14 A, 30V. $R_{DS(on)} = 8.7\text{ m}\Omega @ V_{GS} = 10\text{V}$
 $R_{DS(on)} = 10.5\text{ m}\Omega @ V_{GS} = 4.5\text{V}$
- **Q1:** 11 A, 30V. $R_{DS(on)} = 13.2\text{ m}\Omega @ V_{GS} = 10\text{V}$
 $R_{DS(on)} = 16\text{ m}\Omega @ V_{GS} = 4.5\text{V}$



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q2	Q1	Units
V_{DSS}	Drain-Source Voltage	30	30	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Note 1a) - Pulsed	14	11	A
		50	50	
P_D	Power Dissipation for Single Operation (Note 1a & 1b) (Note 1c & 1d)	2.4	1.8	W
		1.3	1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a & 1b) (Note 1c & 1d)	Q2	Q1	$^\circ\text{C/W}$
		52	68	
		94	118	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDQ7238AS	FDQ7238AS	13"	16mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$ $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Q2 Q1	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C $I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	Q2 Q1		25 24		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	Q2 Q1			500 1	μA
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$	Q2 Q1		5.6 40		mA μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	ALL			± 100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$ $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Q2 Q1	1 1	1.8 1.7	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C $I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	Q2 Q1		-3 -4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 14\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 13\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 14\text{ A}, T_J = 125^\circ\text{C}$	Q2		7.2 8.7 10	8.7 10.5 12.5	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 11\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 11\text{ A}, T_J = 125^\circ\text{C}$	Q1		11 13 15	13.2 16 19	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	Q2 Q1	50 50			A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 14\text{ A}$ $V_{DS} = 10\text{ V}, I_D = 11\text{ A}$	Q2 Q1		58 43		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	Q2 Q1		1530 920		pF
C_{oss}	Output Capacitance		Q2 Q1		440 190		pF
C_{riss}	Reverse Transfer Capacitance		Q2 Q1		160 120		pF
R_g	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$	Q2 Q1		1.9 1.9		Ω

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

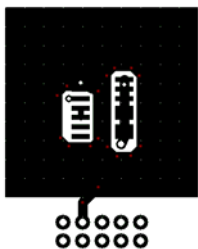
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	Q2		12	21	ns
			Q1		9	18	
t_r	Turn-On Rise Time		Q2		13	23	ns
			Q1		5	10	
$t_{d(off)}$	Turn-Off Delay Time		Q2		30	49	ns
			Q1		27	43	
t_f	Turn-Off Fall Time		Q2		19	35	ns
			Q1		4	8	
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q2		17	30	ns
			Q1		11	20	
t_r	Turn-On Rise Time		Q2		18	32	ns
			Q1		15	26	
$t_{d(off)}$	Turn-Off Delay Time		Q2		28	44	ns
			Q1		16	29	
t_f	Turn-Off Fall Time		Q2		13	23	ns
			Q1		9	18	
$Q_{g(TOT)}$	Total Gate Charge, $V_{GS} = 10\text{ V}$	Q2 $V_{DS} = 15\text{ V}, I_D = 14\text{ A}$	Q2		28	39	nC
			Q1		17	24	
$Q_{g(TOT)}$	Total Gate Charge, $V_{GS} = 5\text{ V}$	Q1	Q2		15	21	nC
			Q1		9	19	
Q_{gs}	Gate-Source Charge	$V_{DS} = 15\text{ V}, I_D = 11\text{ A}$	Q2		4.1		nC
			Q1		2.7		
Q_{gd}	Gate-Drain Charge		Q2		4.9		nC
			Q1		3.3		

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current		Q2			3.4	A
			Q1			2.1	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 3.4\text{ A}$ (Note 2)	Q2		0.5	0.7	V
		$V_{GS} = 0\text{ V}, I_S = 1.9\text{ A}$ (Note 2)			0.4		
		$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)	Q1		0.7	1.2	
t_{rr}	Diode Reverse Recovery Time	$I_F = 14\text{ A}$	Q2		22		ns
Q_{rr}	Diode Reverse Recovery Charge	$dI_F/dt = 300\text{ A}/\mu\text{s}$				15	nC
t_{rr}	Diode Reverse Recovery Time	$I_F = 11\text{ A}$	Q1		16		ns
Q_{rr}	Diode Reverse Recovery Charge	$dI_F/dt = 100\text{ A}/\mu\text{s}$				5	nC

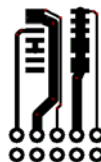
NOTE :

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $68^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper (Q1).

b) $52^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper (Q2).



c) $118^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper (Q1).

d) $94^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper (Q2).

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu\text{s}$, Duty Cycle < 2.0%

Typical Characteristics: Q2

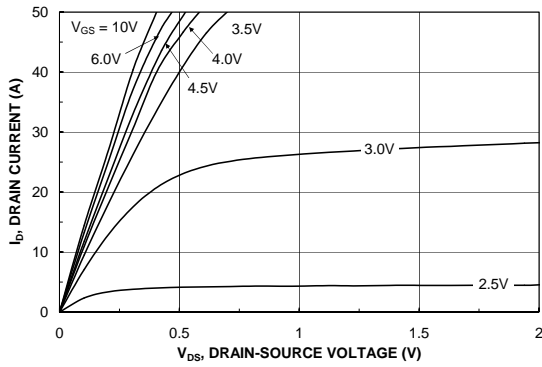


Figure 1. On-Region Characteristics.

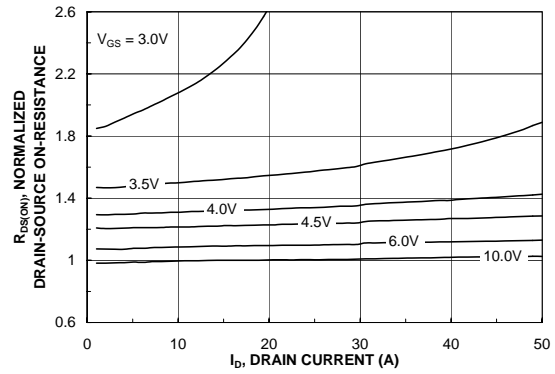


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

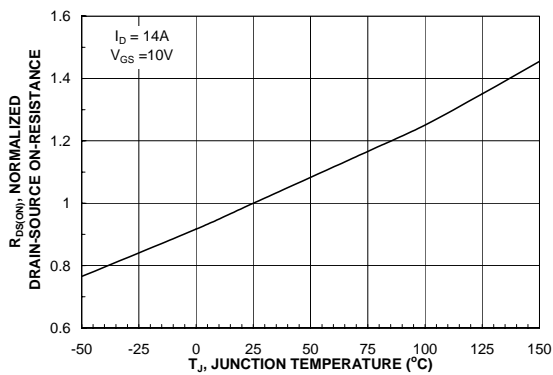


Figure 3. On-Resistance Variation with Temperature.

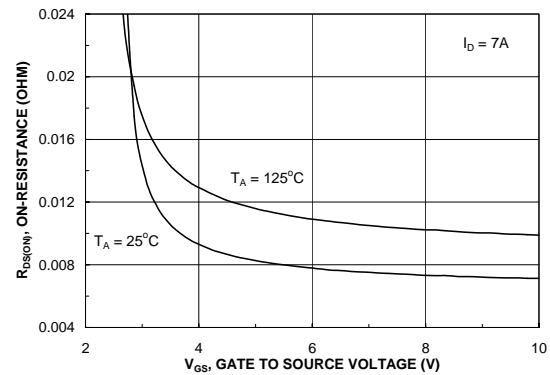


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

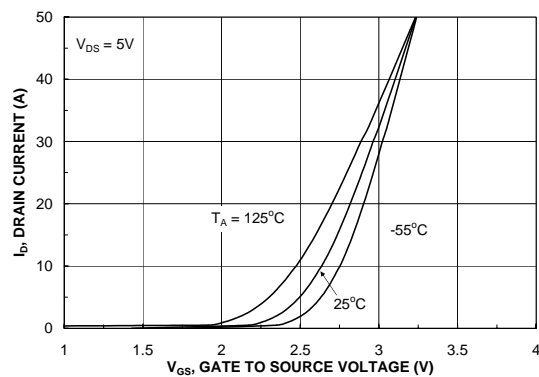


Figure 5. Transfer Characteristics.

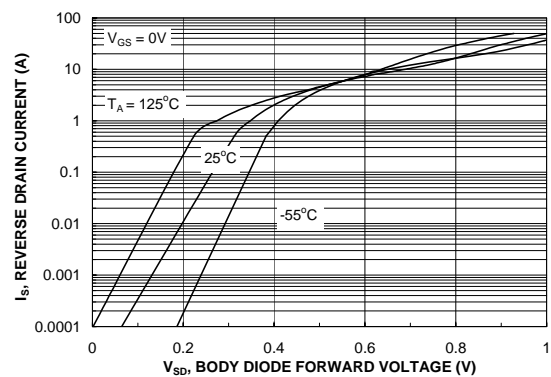


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics : Q2

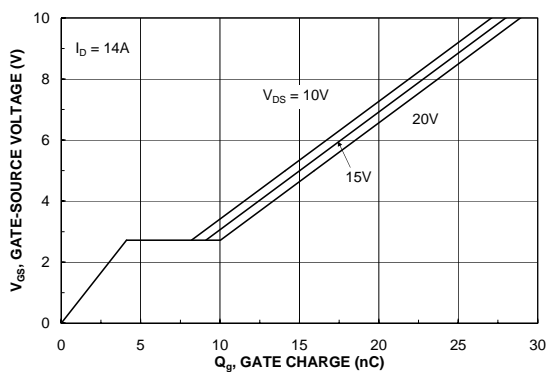


Figure 7. Gate Charge Characteristics.

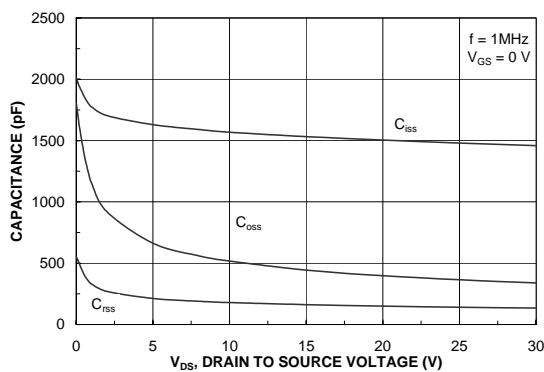


Figure 8. Capacitance Characteristics.

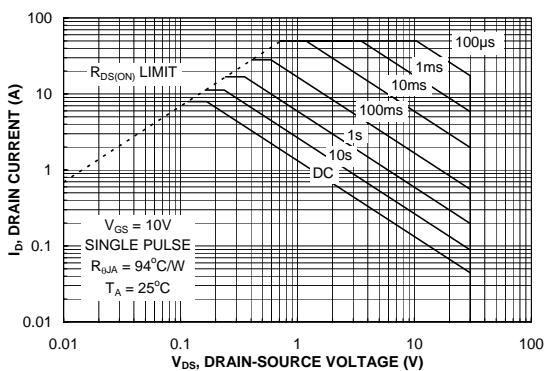


Figure 9. Maximum Safe Operating Area.

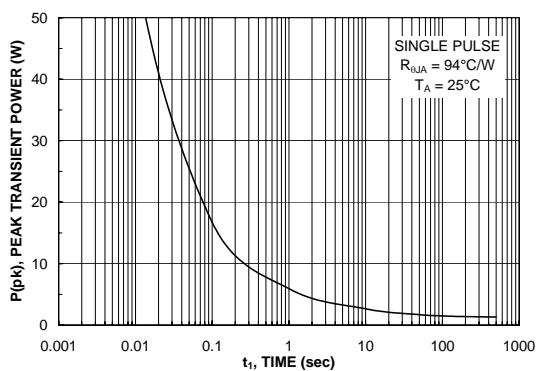


Figure 10. Single Pulse Maximum Power Dissipation.

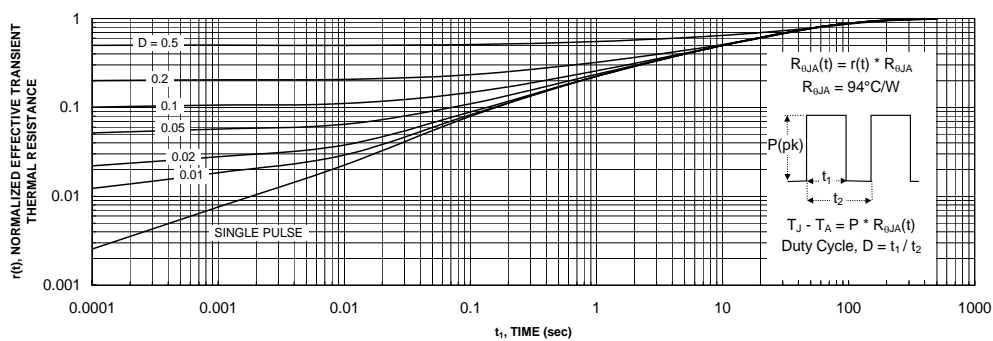


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1d.
Transient thermal response will change depending on the circuit board design

Typical Characteristics : Q2

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDQ7238AS Q2.

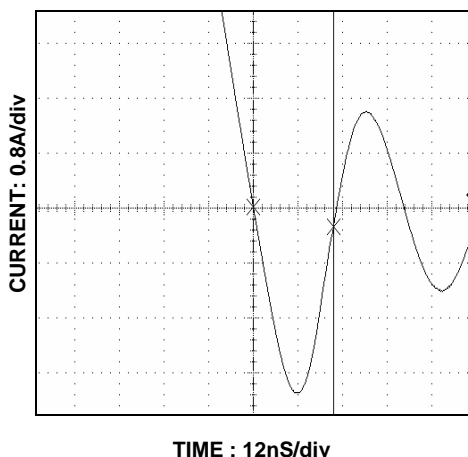


Figure 12. FDQ7238AS SyncFET body diode reverse recovery characteristic.

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET(FDS6670A).

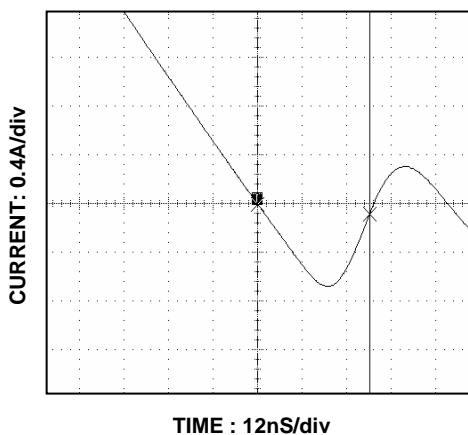


Figure 13. Non-SyncFET (FDS6670A) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power dissipated in the device.

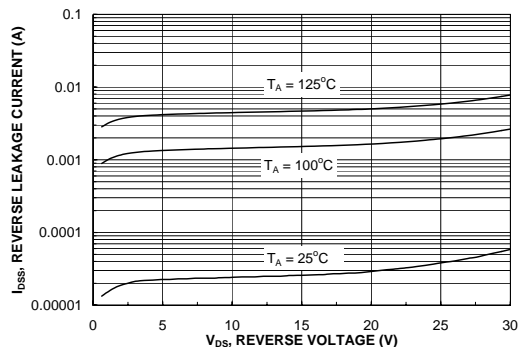


Figure 14. SyncFET body diode reverse leakage versus drain-source voltage and temperature.

Typical Characteristics: Q1

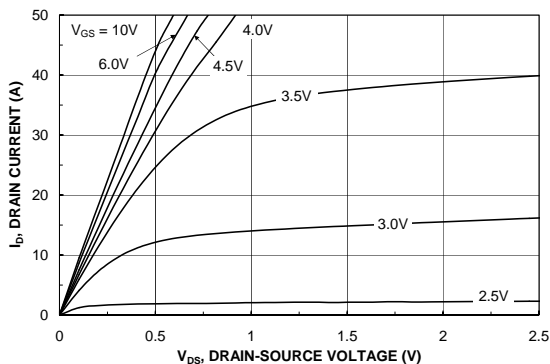


Figure 15. On-Region Characteristics.

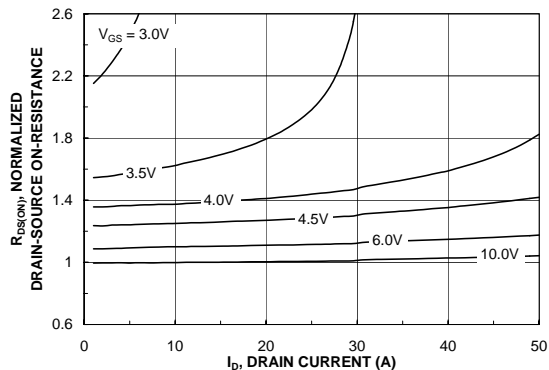


Figure 16. On-Resistance Variation with Drain Current and Gate Voltage.

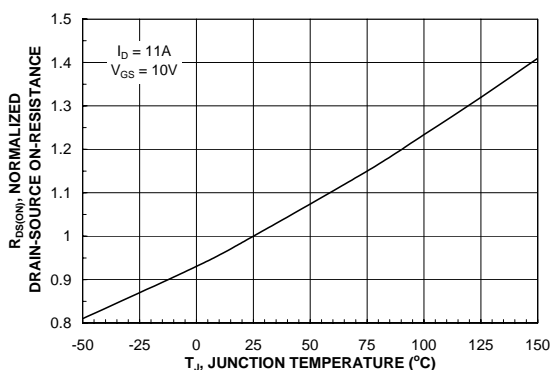


Figure 17. On-Resistance Variation with Temperature.

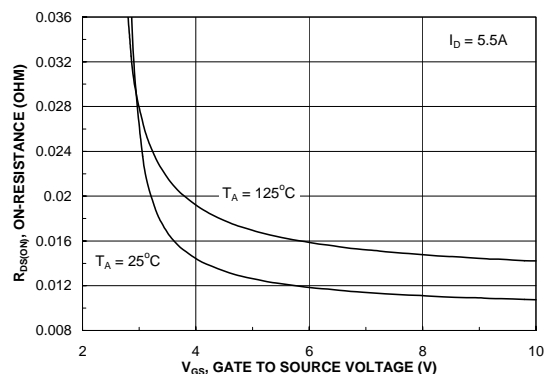


Figure 18. On-Resistance Variation with Gate-to-Source Voltage.

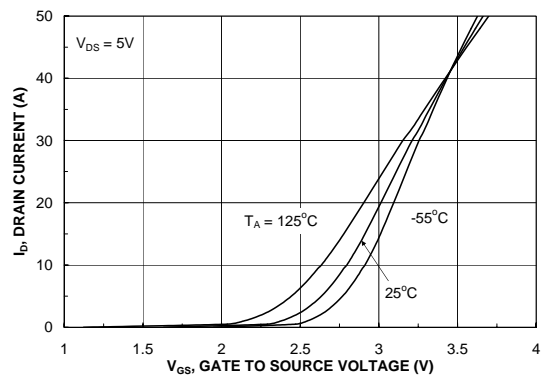


Figure 19. Transfer Characteristics.

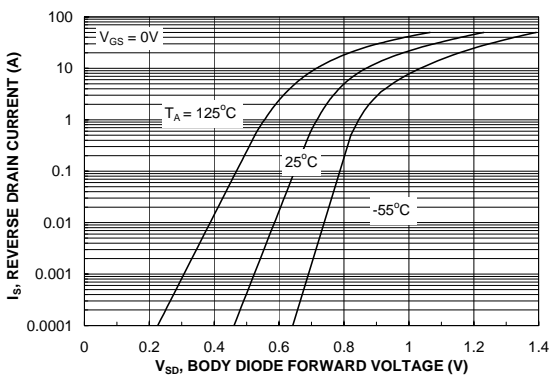


Figure 20. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1

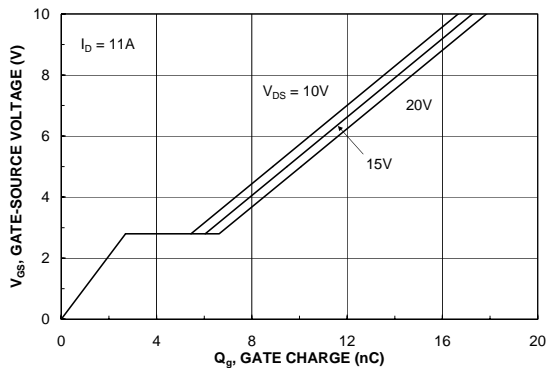


Figure 21. Gate Charge Characteristics.

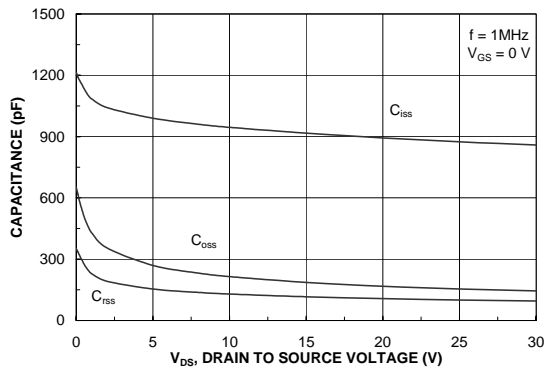


Figure 22. Capacitance Characteristics.

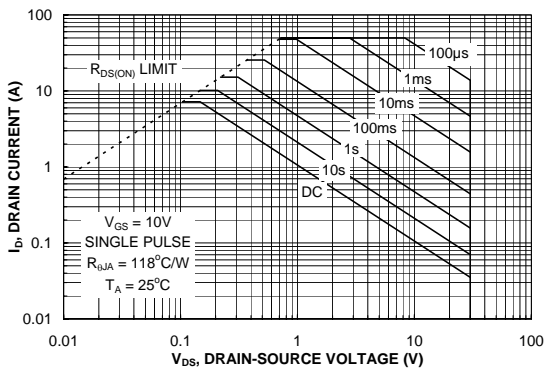


Figure 23. Maximum Safe Operating Area.

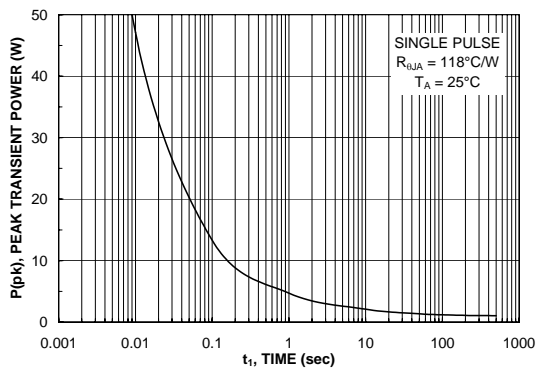


Figure 24. Single Pulse Maximum Power Dissipation.

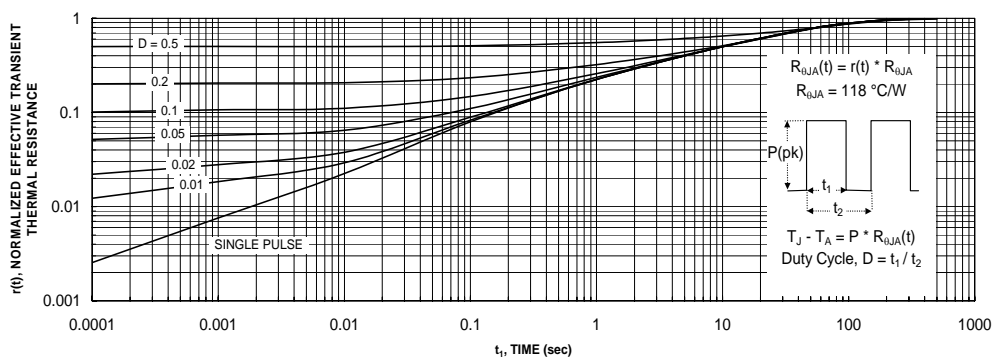


Figure 25. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c
Transient thermal response will change depending on the circuit board design.



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