THE DATASHEET OF

FDS7296N3

FAIRCHILD SEMICONDUCTOR®

September 2004

FDS7296N3

30V N-Channel PowerTrench® MOSFET

General Description

This N-Channel MOSFET in the thermally enhanced SO8 FLMP package has been designed specifically to improve the overall efficiency of DC/DC converters. Providing a balance of low $R_{DS(ON)}$ and Qg it is ideal for synchronous rectifier applications in both isolated and non-isolated topologies. It is also well suited for high and low side switch applications in Point of Load converters.

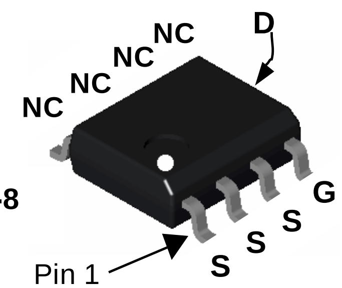
Applications

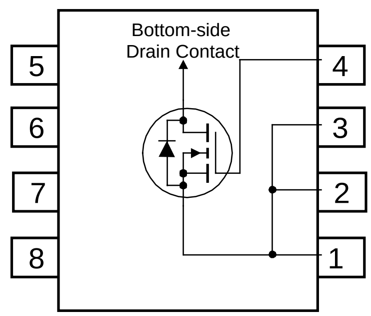
- Secondary side Synchronous rectifier
- Synchronous Buck VRM and POL Converters

Features

- 15 A, 30 V $R_{DS(ON)}$ = 8 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 11 mΩ @ V_{GS} = 4.5 V
- High performance trench technology for extremely low $R_{DS(ON)}$
- Optimized for low Qgd to enable fast switching and reduced CdV/dt gate coupling.
- SO-8 FLMP for enhanced thermal performance in an industry-standard package outline.

FLMP SO-8





Absolute Maximum Ratings $T_A=25^oC$ unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	15	A
	– Pulsed		60	
P_D	Power Dissipation for Single Operation	(Note 1a)	3.0	W
		(Note 1b)	1.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	0.5	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS7296N3	FDS7296N3	13''	12mm	2500 units

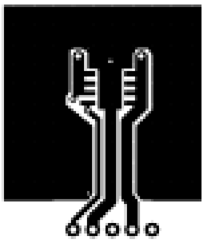
Electrical Characteristics

T_A = 25°C unless otherwise noted

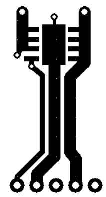
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings						
W_{DSS}	Drain-Source Avalanche Energy	Single Pulse, V_{DD} = 27 V, I_D=15 A			189	mJ
I_{AR}	Drain-Source Avalanche Current				15	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		28		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
I_{GSS}	Gate–Body Leakage	V_{GS} = ± 20 V, V_{DS} = 0 V			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		–0.5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 15 A V_{GS} = 4.5 V, I_D = 13 A V_{GS} = 10 V, I_D = 15 A, T_J = 125°C		6.5 8.2 9.7	8 11 13	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 15 A		58		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1540		pF
C_{oss}	Output Capacitance			430		pF
C_{rss}	Reverse Transfer Capacitance			140		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		1.0		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn–On Rise Time			4	9	ns
$t_{d(off)}$	Turn–Off Delay Time			27	44	ns
t_f	Turn–Off Fall Time			14	25	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 15 A, V_{GS} = 5 V		12.7	18	nC
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 15 A, V_{GS} =10 V		23	32	nC
Q_{gs}	Gate–Source Charge			4.2		nC
Q_{gd}	Gate–Drain Charge			3.5		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.5	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.5 A (Note 2)		0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 15 A, d_{iF}/d_t = 100 A/µs		27		nS
Q_{rr}	Diode Reverse Recovery Charge			19		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 40°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 85°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

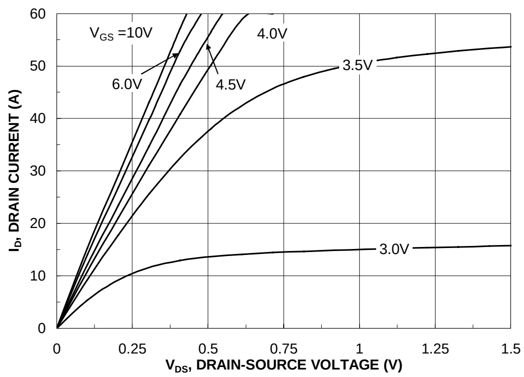


Figure 1. On-Region Characteristics.

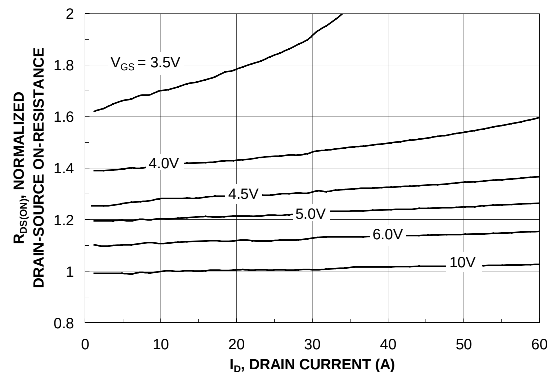


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

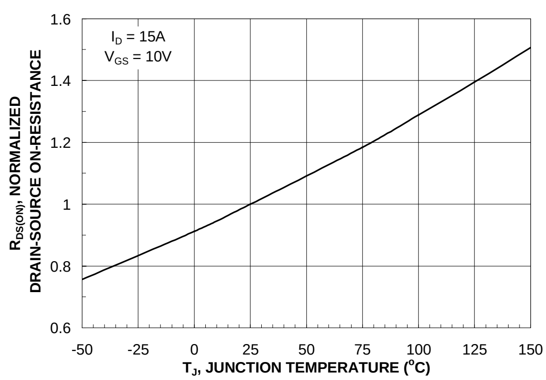


Figure 3. On-Resistance Variation withTemperature.

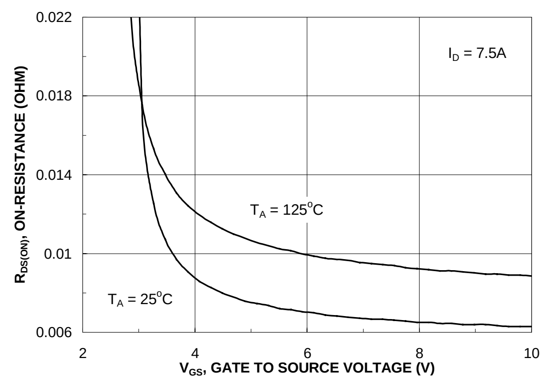


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

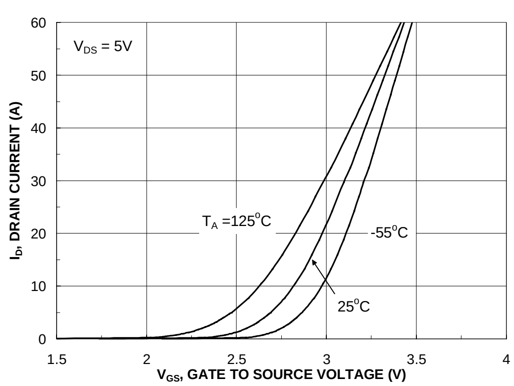


Figure 5. Transfer Characteristics.

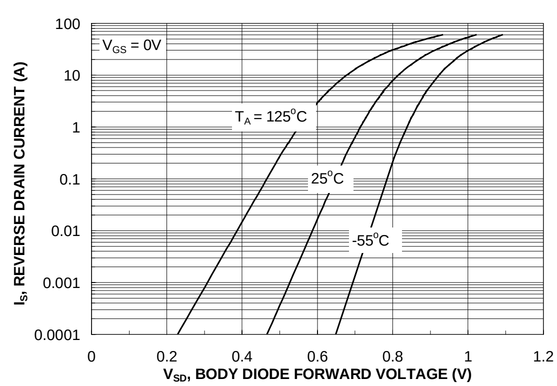


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

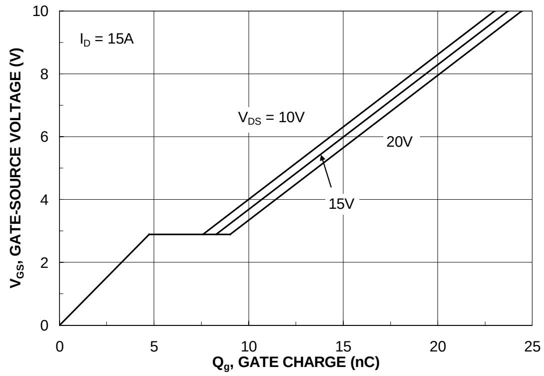


Figure 7. Gate Charge Characteristics.

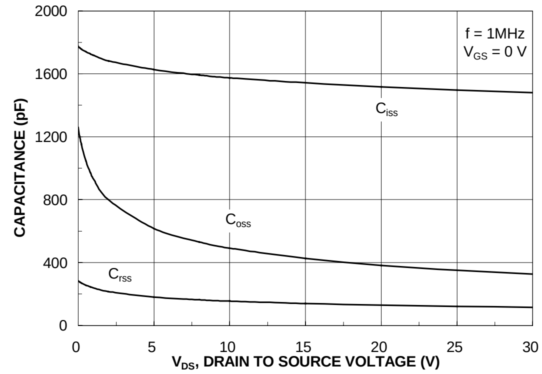


Figure 8. Capacitance Characteristics.

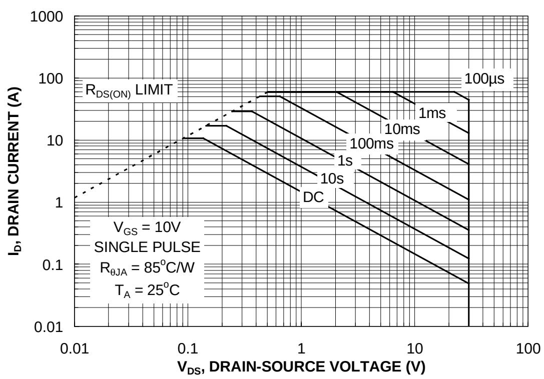


Figure 9. Maximum Safe Operating Area.

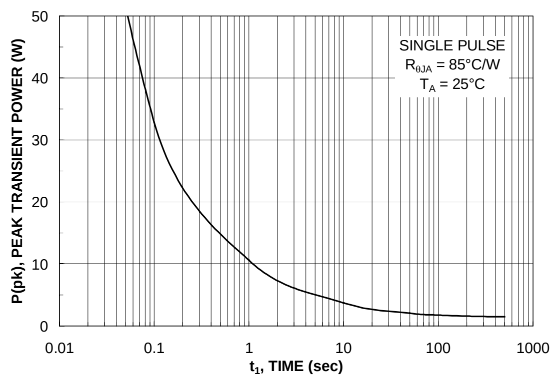


Figure 10. Single Pulse Maximum Power Dissipation.

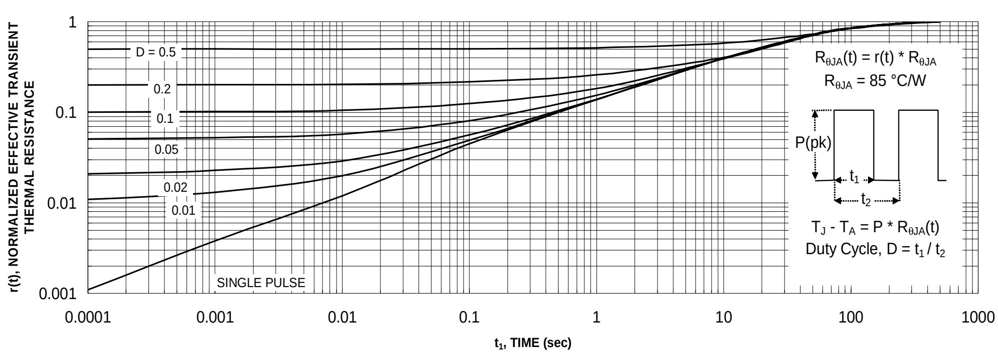
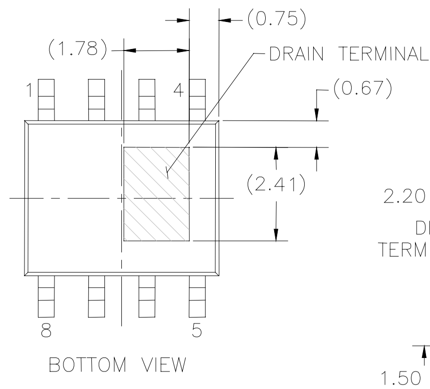
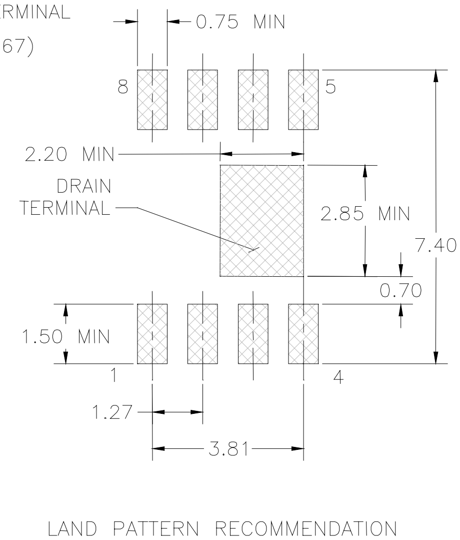


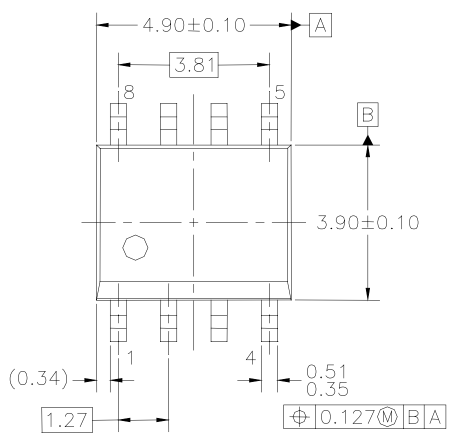
Figure 11. Transient Thermal Response Curve.

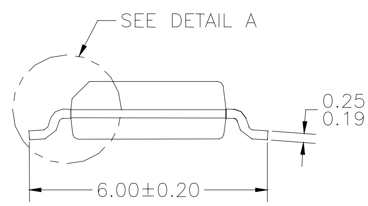
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

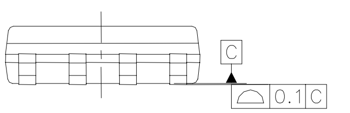
Dimensional Outline and Pad Layout





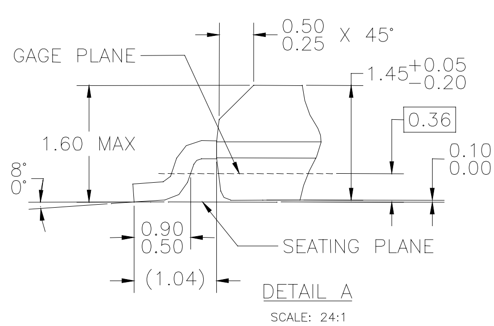






NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) STANDARD LEAD FINISH:
20–80 MICROINCHES NICKEL/
6 MICROINCHES MAX. PALLADIUM
AND GOLD FLASH.
C) NO JEDEC REGISTERED REFERENCE
AS OF MARCH 2, 2000.



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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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Rev. I13