



**THE DATASHEET OF  
FQA140N10**



# MOSFET – N-Channel QFET

100 V, 140 A, 10 mΩ

## FQA140N10

### Description

This N-Channel Enhancement Mode Power MOSFET is produced using onsemi’s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

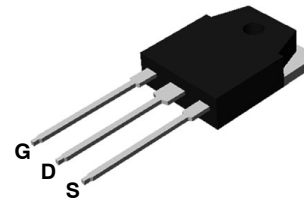
### Features

- 140 A, 100 V,  $R_{DS(on)} = 10\text{ m}\Omega$  (Max.) @  $V_{GS} = 10\text{ V}$ ,  $I_D = 70\text{ A}$
- Low Gate Charge (Typ. 220 nC)
- Low  $C_{rss}$  (Typ. 470 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating

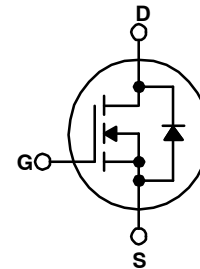
### MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage	100	V
$I_D$	Drain Current – Continuous ( $T_C = 25^\circ\text{C}$ ) – Continuous ( $T_C = 100^\circ\text{C}$ )	140 99	A
$I_{DM}$	Drain Current – Pulsed (Note 1)	560	A
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1500	mJ
$I_{AR}$	Avalanche Current (Note 1)	140	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	37.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.5	V/ns
$P_D$	Power Dissipation – ( $T_C = 25^\circ\text{C}$ ) – Derate Above 25°C	375 2.5	W W/°C
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	°C
$T_L$	Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	300	°C

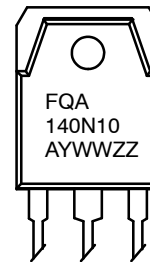
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



TO-3P-3LD  
CASE 340BZ



### MARKING DIAGRAM



FQA140N10 = Specific Device Code  
A = Assembly Location  
YWW = Date Code (Year and Week)  
ZZ = Assembly Lot Code

### ORDERING INFORMATION

Device	Package	Shipping
FQA140N10	TO-3P-3LD (Pb-Free)	450 Units / Tube

# FQA140N10

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to 25°C	-	0.08	-	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 64\text{ V}, T_C = 150^\circ\text{C}$	-	-	10	μA
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 70\text{ A}$	-	0.008	0.01	Ω
$g_{FS}$	Forward Transconductance	$V_{DS} = 30\text{ V}, I_D = 70\text{ A}$	-	80	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	6100	7900	pF
$C_{oss}$	Output Capacitance		-	2000	2600	pF
$C_{rss}$	Reverse Transfer Capacitance		-	420	550	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}, I_D = 140\text{ A}, R_G = 25\ \Omega$ (Note 4)	-	75	160	ns
$t_r$	Turn-On Rise Time		-	940	1890	ns
$t_{d(off)}$	Turn-Off Delay Time		-	350	710	ns
$t_f$	Turn-Off Fall Time		-	360	730	ns
$Q_g$	Total Gate Charge	$V_{DS} = 64\text{ V}, I_D = 140\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	220	285	nC
$Q_{gs}$	Gate-Source Charge		-	39	-	nC
$Q_{gd}$	Gate-Drain Charge		-	114	-	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current (Note 5)	-	-	140	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	-	-	560	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 140\text{ A}$	-	-	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 140\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	140	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	730	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $L = 0.115\text{ mH}, I_{AS} = 140\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 140\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.
5. Continuous drain current calculated by maximum junction temperature: limited by package.

TYPICAL CHARACTERISTICS

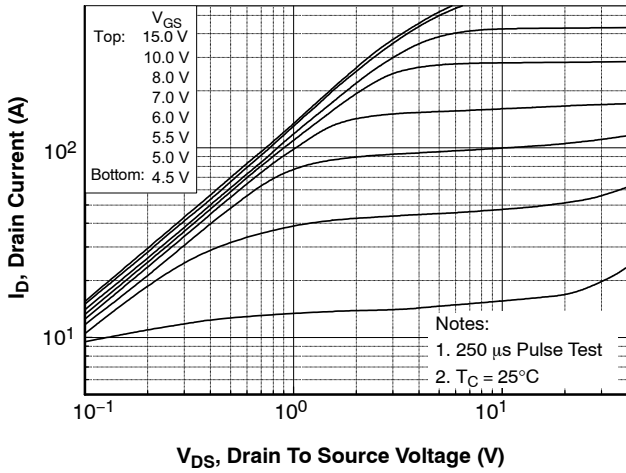


Figure 1. On-Region Characteristics

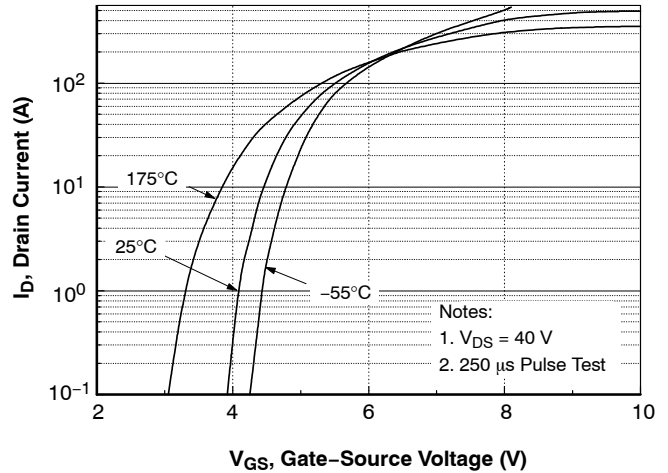


Figure 2. Transfer Characteristics

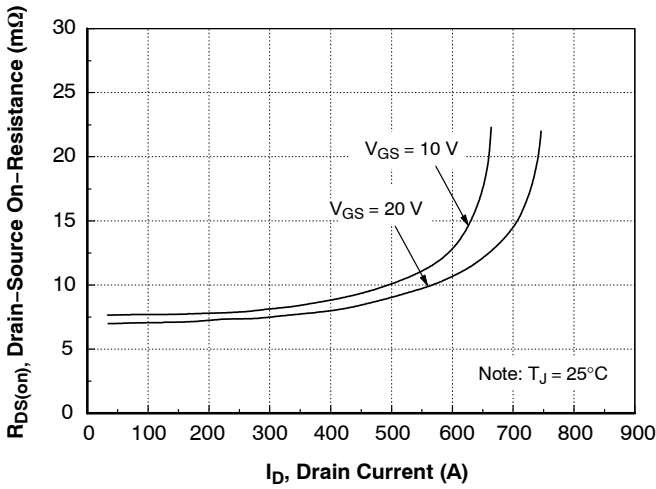


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

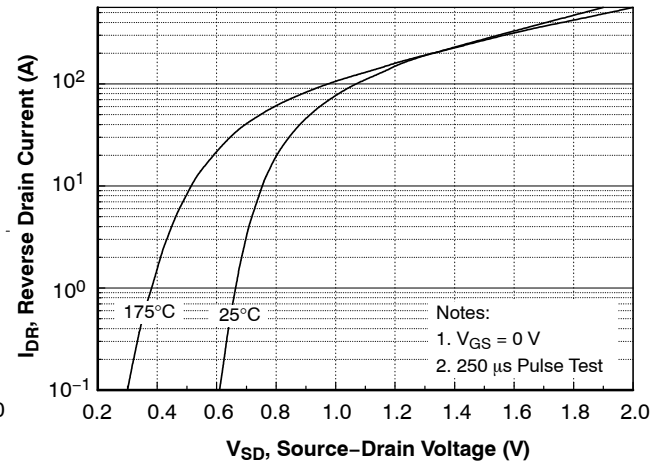


Figure 4. Body Diode Forward Voltage Variation vs Source Current and Temperature

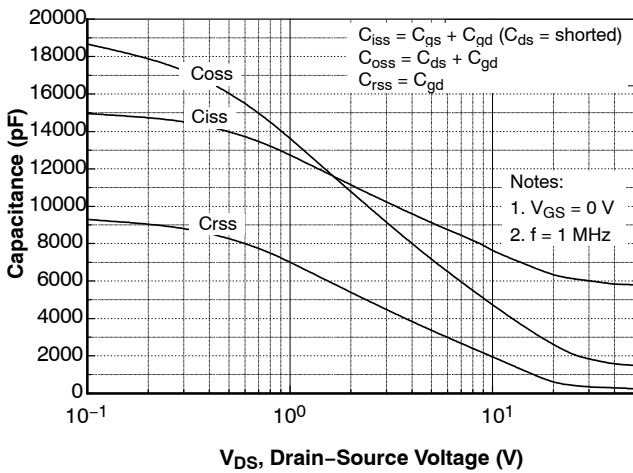


Figure 5. Capacitance Characteristics

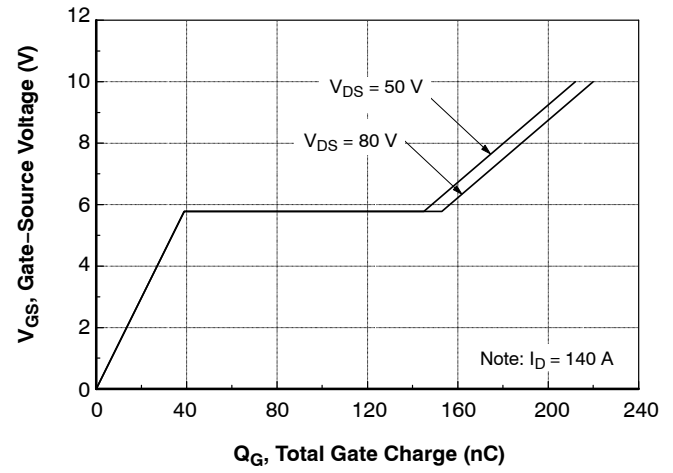


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

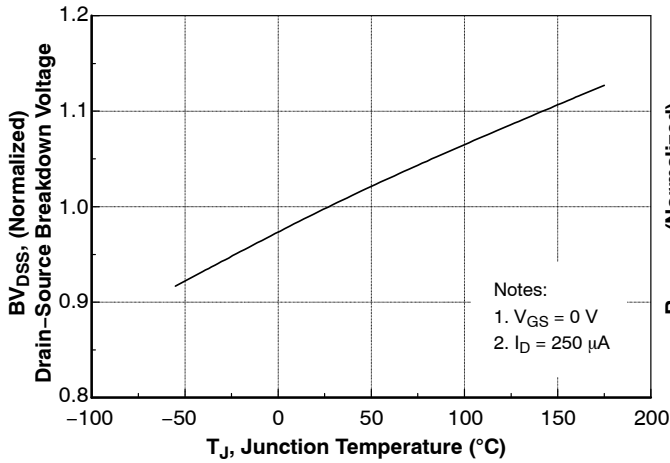


Figure 7. Breakdown Voltage Variation vs Temperature

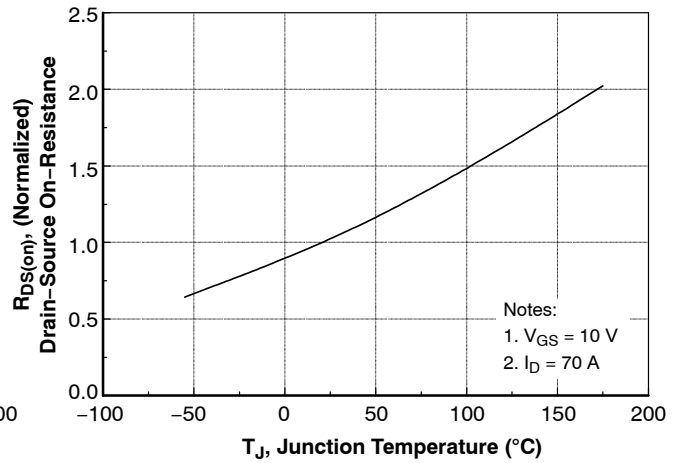


Figure 8. On-Resistance Variation vs Temperature

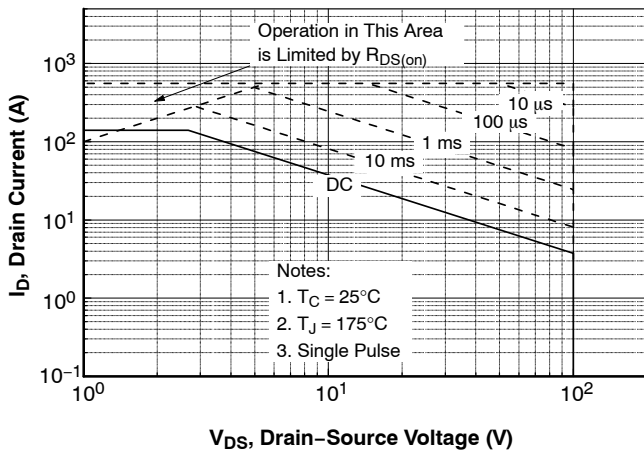


Figure 9. Maximum Safe Operating Area

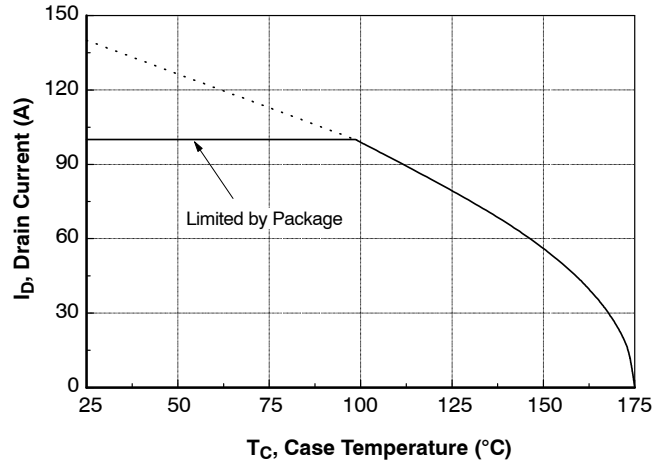


Figure 10. Maximum Drain Current vs. Case Temperature

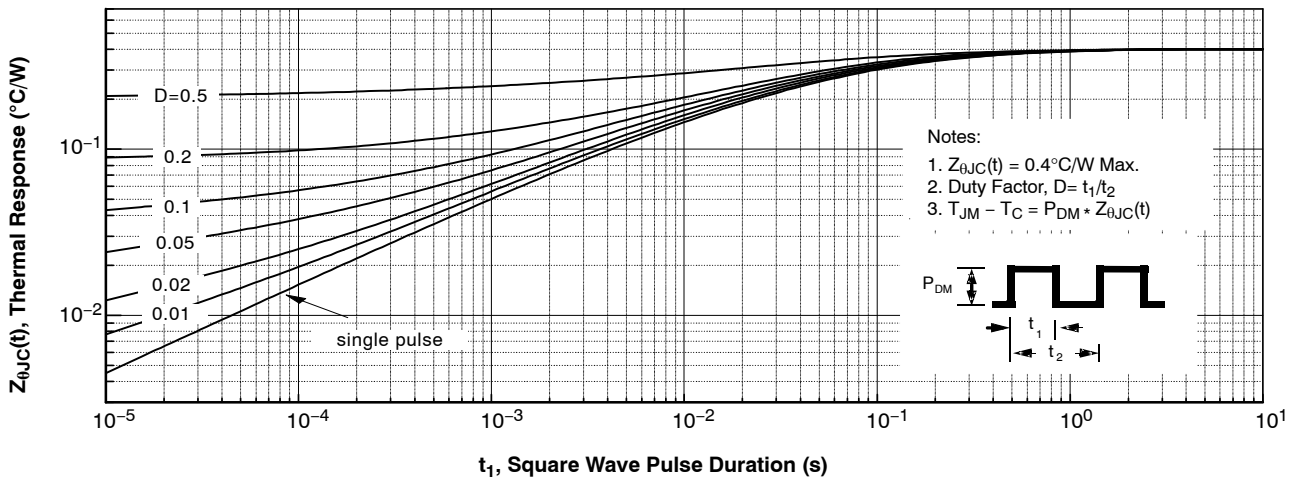


Figure 11. Transient Thermal Response Curve

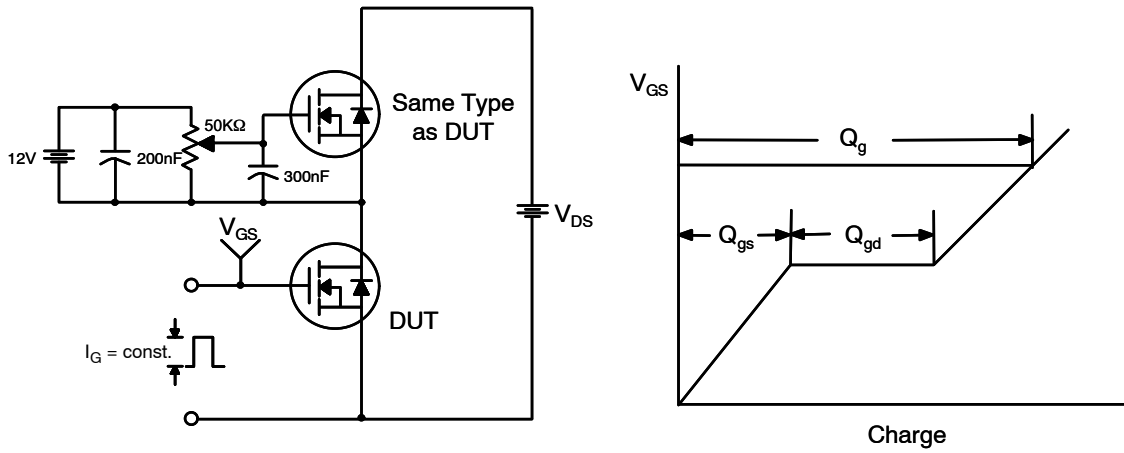


Figure 12. Gate Charge Test Circuit & Waveform

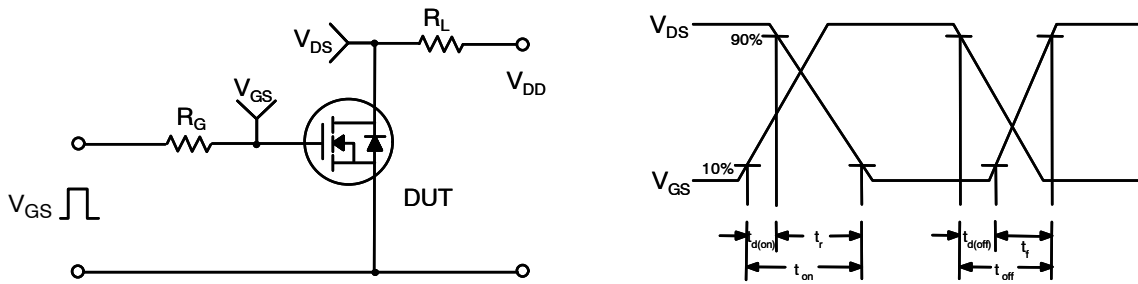


Figure 13. Resistive Switching Test Circuit & Waveforms

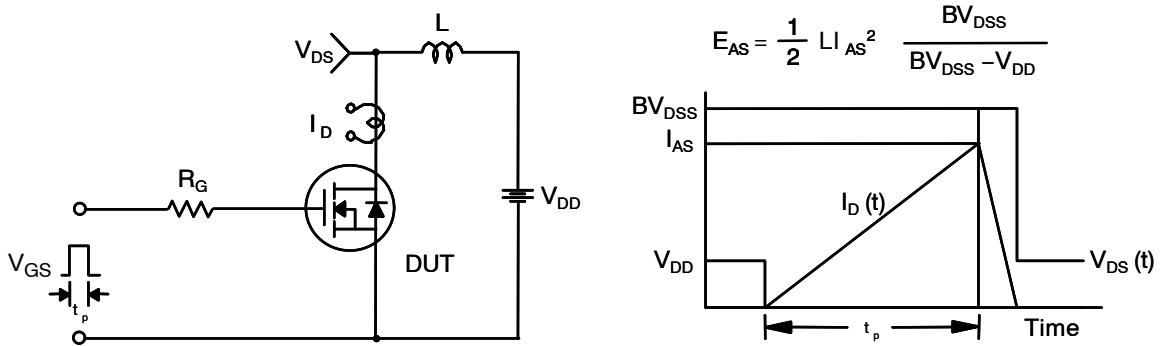


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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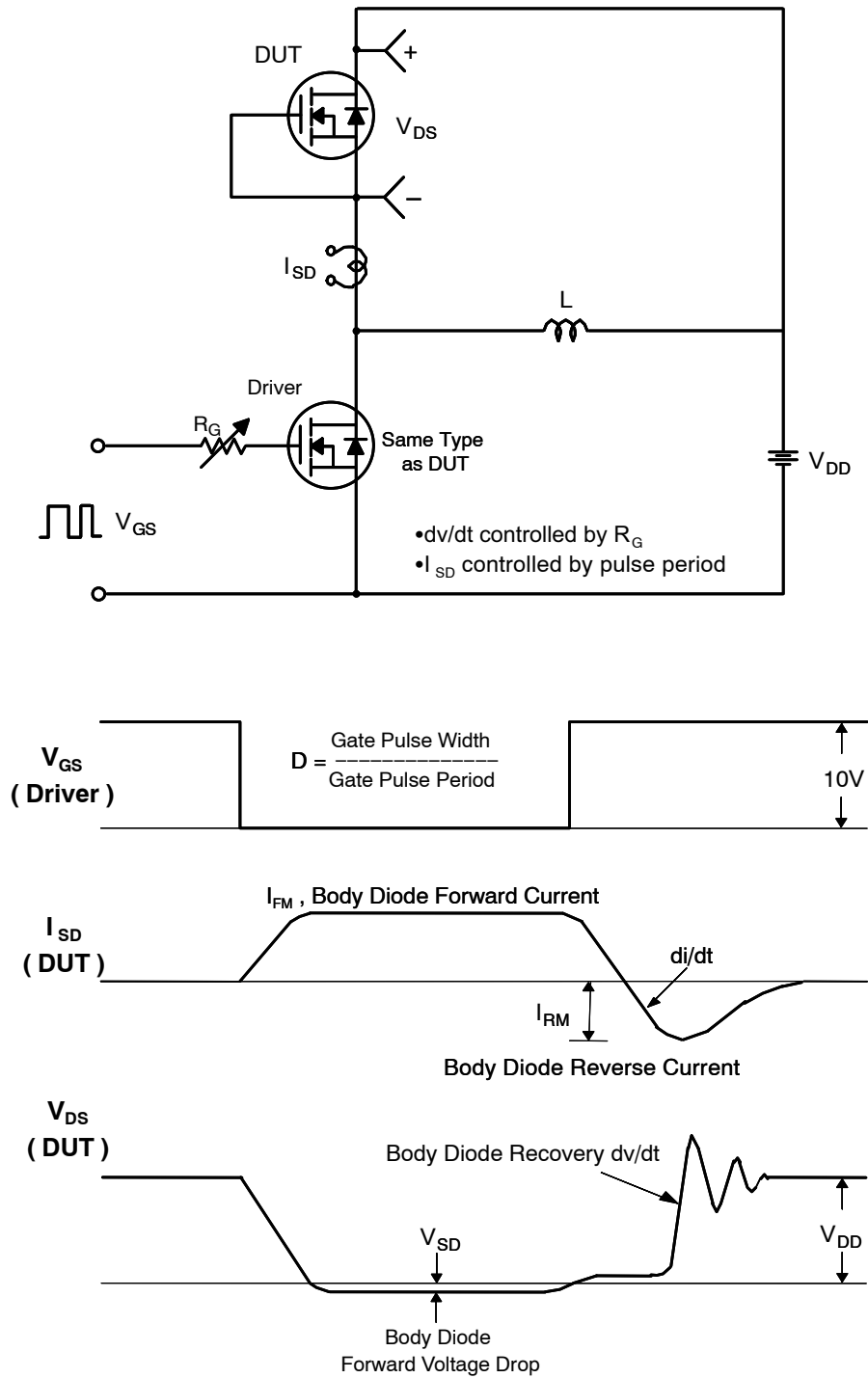


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

# MECHANICAL CASE OUTLINE

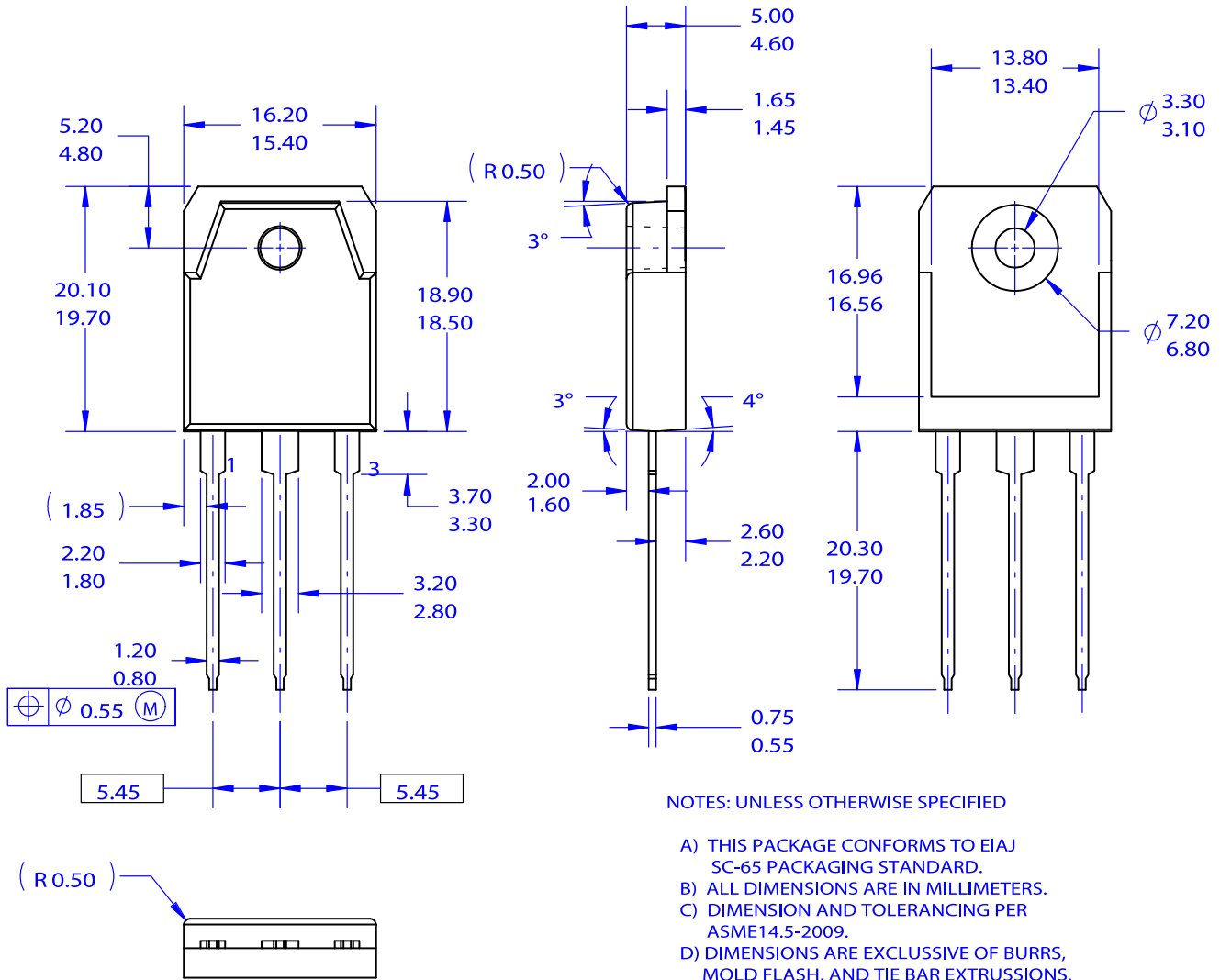
## PACKAGE DIMENSIONS

ON Semiconductor®



### TO-3P-3LD / EIAJ SC-65, ISOLATED CASE 340BZ ISSUE O

DATE 31 OCT 2016



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