



**THE DATASHEET OF
FQA24N60**



MOSFET – N-Channel, QFET

600 V, 23.5 A, 240 mΩ

FQA24N60

Description

This N-Channel Enhancement Mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology.

This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

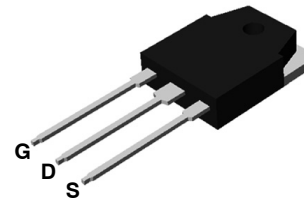
- 23.5 A, 600 V, $R_{DS(on)} = 240 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 11.8 \text{ A}$
- Low Gate Charge (Typ. 110 nC)
- Low C_{rSS} (Typ. 56 pF)
- 100% Avalanche Tested
- This Device is Pb-Free

ABSOLUTE MAXIMUM RATINGS

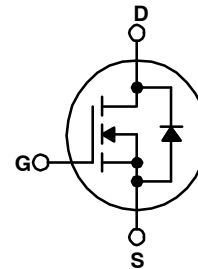
($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	600	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$) – Continuous ($T_C = 100^\circ\text{C}$)	23.5 14.9	A
I_{DM}	Drain Current – Pulsed (Note 1)	94	A
V_{GSS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (Note 2)	1300	mJ
I_{AR}	Avalanche Current (Note 1)	23.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	31	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation – ($T_C = 25^\circ\text{C}$) – Derate Above 25°C	310 2.5	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to $+150$	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

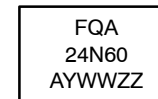
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



TO-3P-3L
CASE 340BZ



MARKING DIAGRAM



FQA24N60 = Specific Device Code
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping†
FQA24N60	TO-3P-3L (Pb-Free)	450 Units / Tube

FQA24N60

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max	0.4	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	600	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	0.6	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 11.8\text{ A}$	-	0.18	0.24	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 11.8\text{ A}$	-	22.5	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	4200	5500	pF
C_{oss}	Output Capacitance		-	550	720	pF
C_{rss}	Reverse Transfer Capacitance		-	56	75	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 23.5\text{ A}, R_G = 25\ \Omega$ (Note 4)	-	90	190	ns
t_r	Turn-On Rise Time		-	270	550	ns
$t_{d(off)}$	Turn-Off Delay Time		-	200	410	ns
t_f	Turn-Off Fall Time		-	170	350	ns
Q_g	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 23.5\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	110	145	nC
Q_{gs}	Gate-Source Charge		-	25	-	nC
Q_{gd}	Gate-Drain Charge		-	53	-	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	-	-	23.5	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	94	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 23.5\text{ A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 23.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	470	-	ns
Q_{rr}	Reverse Recovery Charge		-	6.2	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. Repetitive Rating: Pulse width-limited by maximum junction temperature.
2. $L = 4.3\text{ mH}, I_{AS} = 23.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 23.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

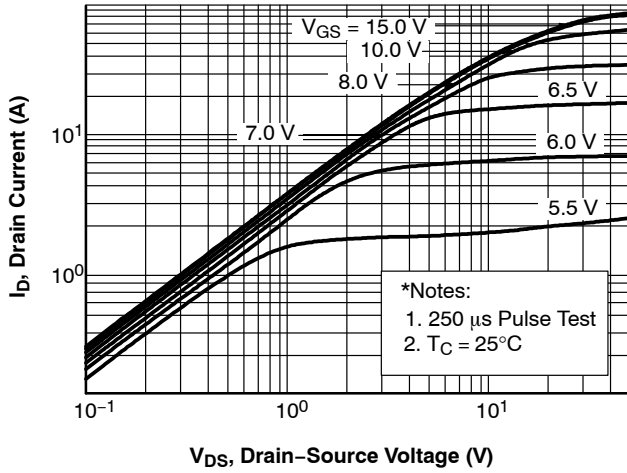


Figure 1. On-Region Characteristics

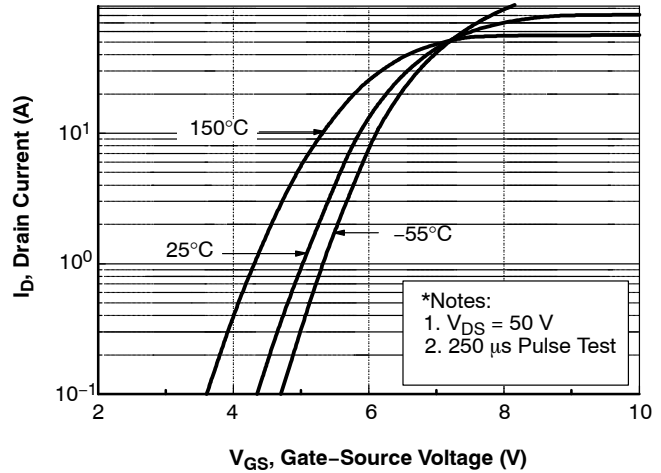


Figure 2. Transfer Characteristics

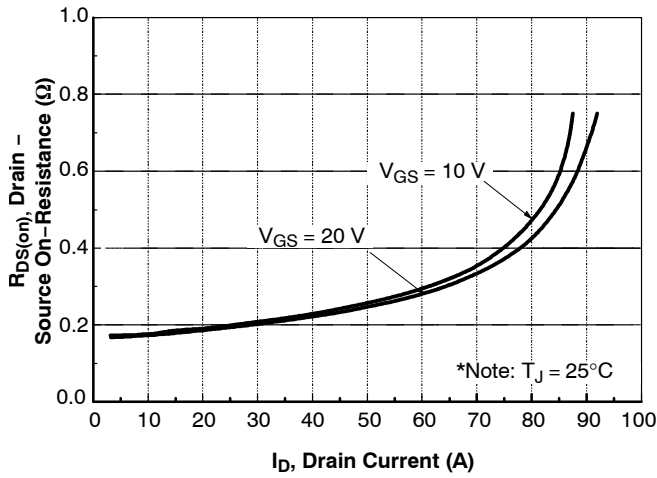


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

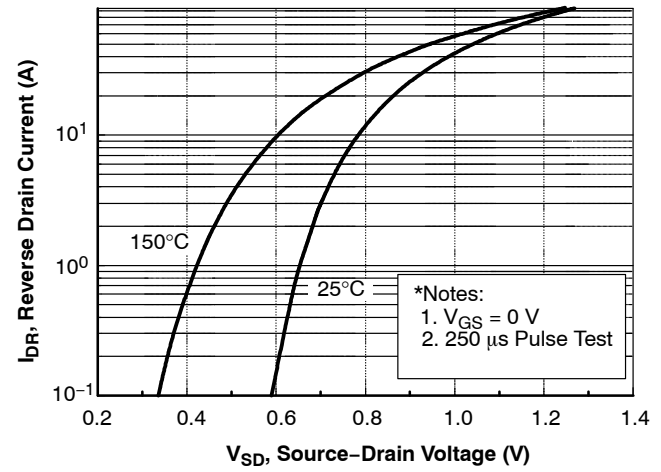


Figure 4. Body Diode Forward Voltage Variation vs Source Current and Temperature

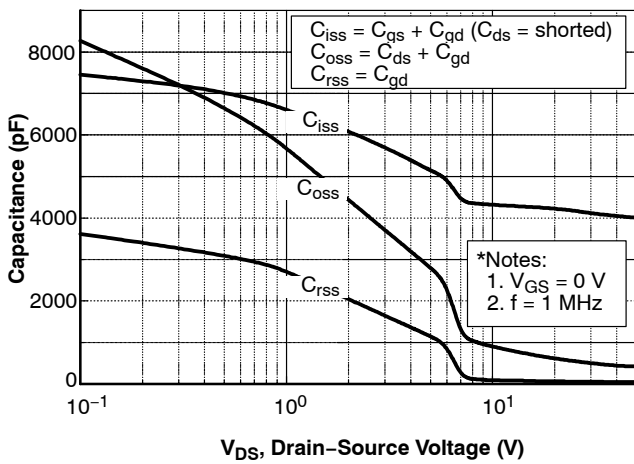


Figure 5. Capacitance Characteristics

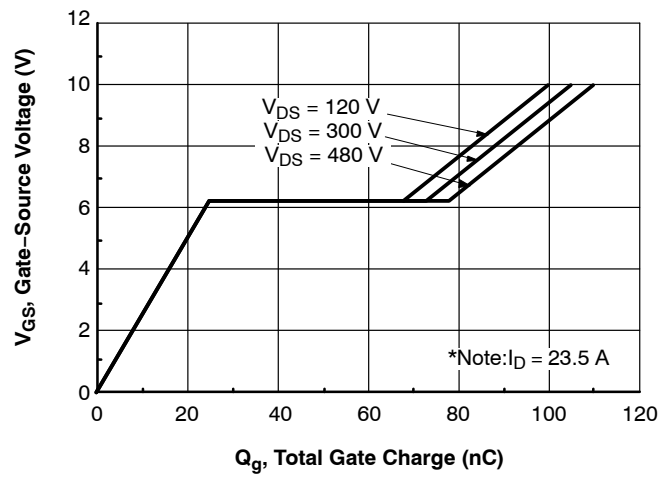


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS (CONTINUED)

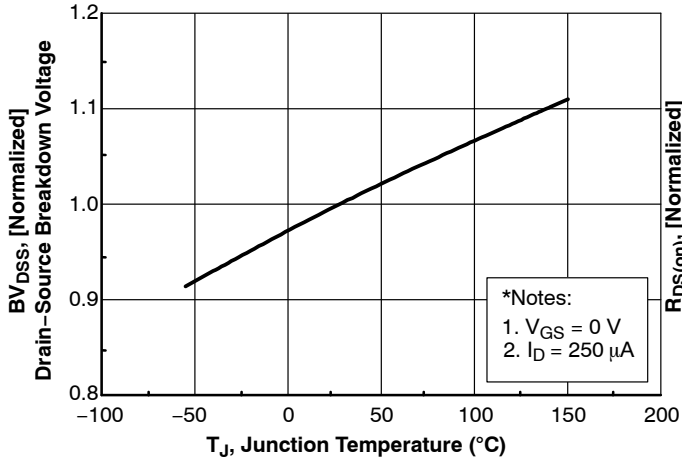


Figure 7. Breakdown Voltage Variation vs Temperature

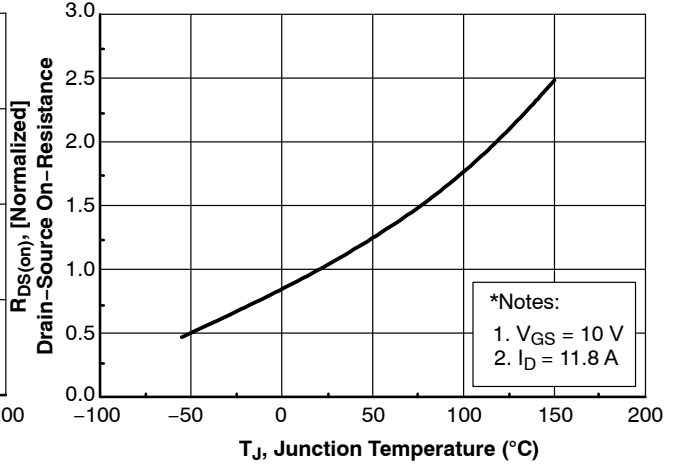


Figure 8. On-Resistance Variation vs Temperature

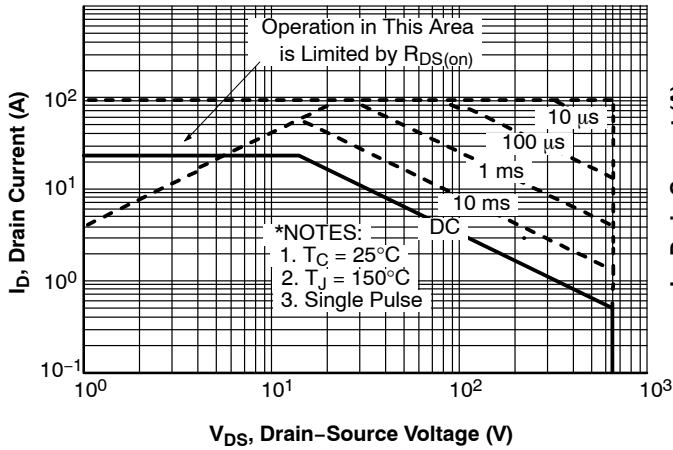


Figure 9. Maximum Safe Operating Area

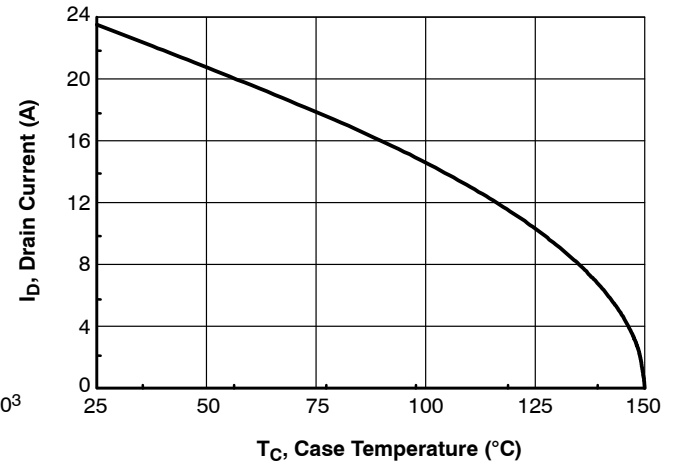


Figure 10. Maximum Drain Current vs. Case Temperature

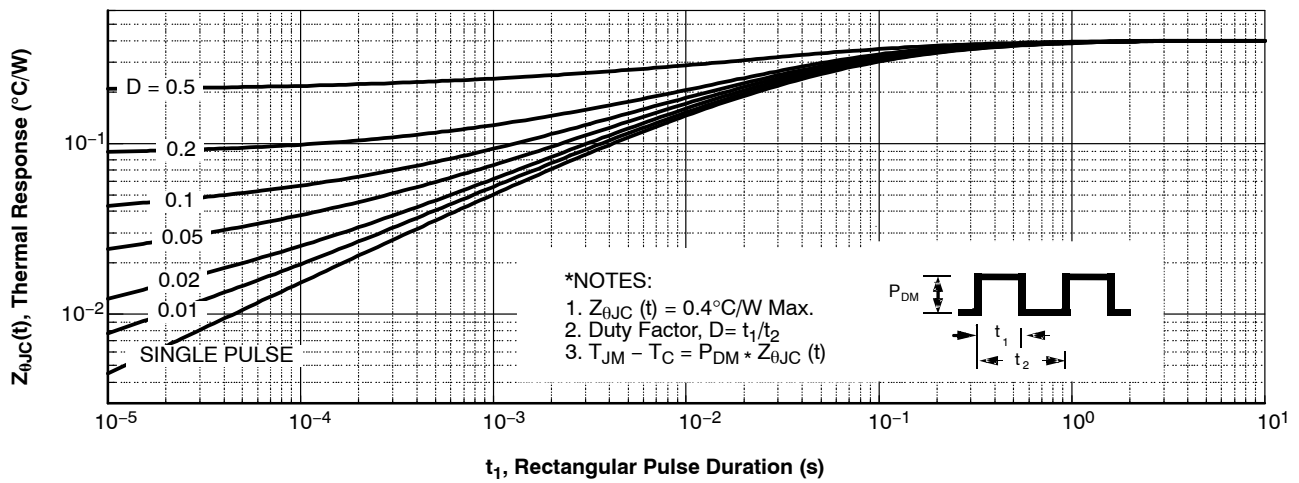


Figure 11. Transient Thermal Response Curve

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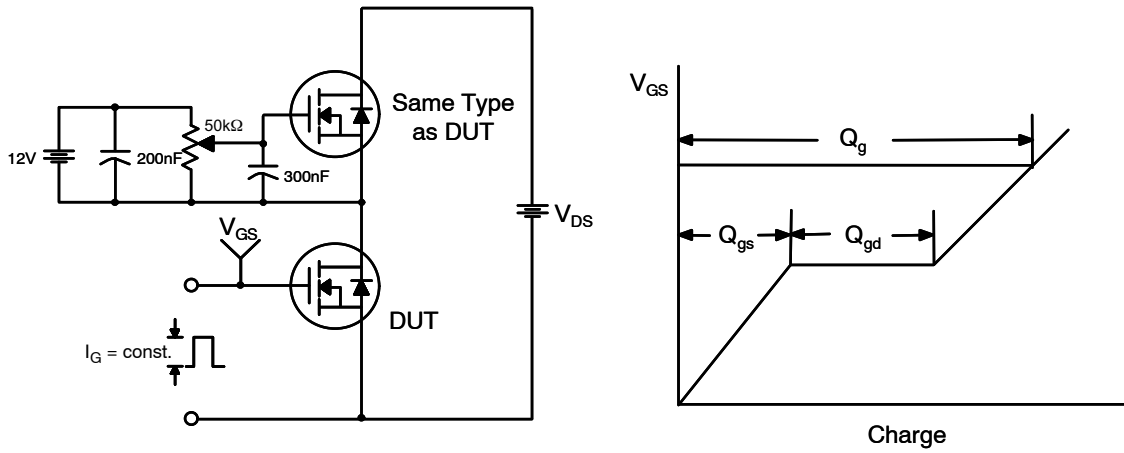


Figure 12. Gate Charge Test Circuit & Waveform

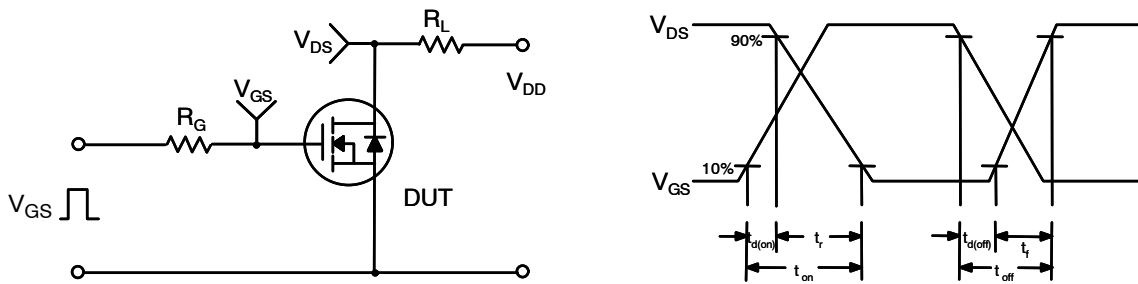


Figure 13. Resistive Switching Test Circuit & Waveforms

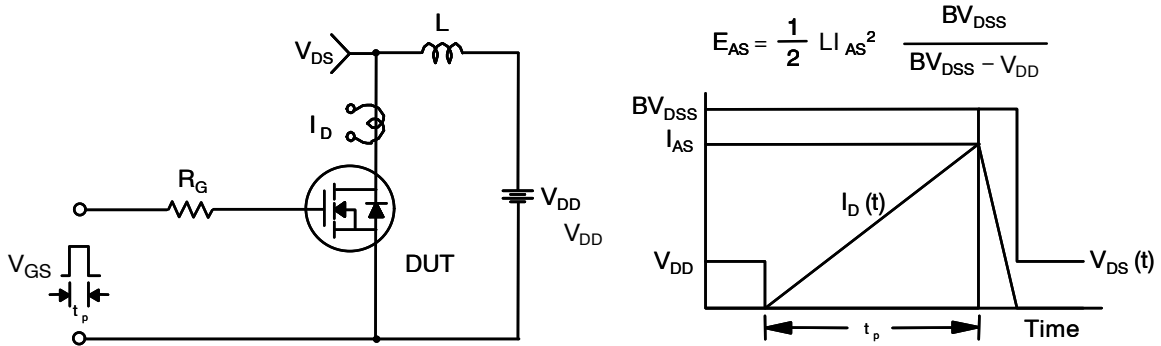


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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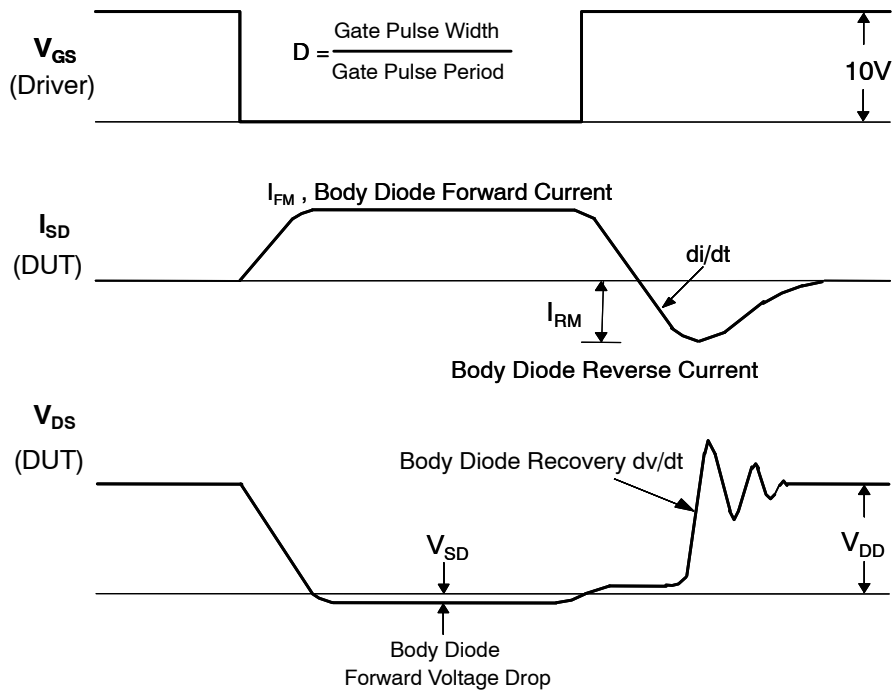
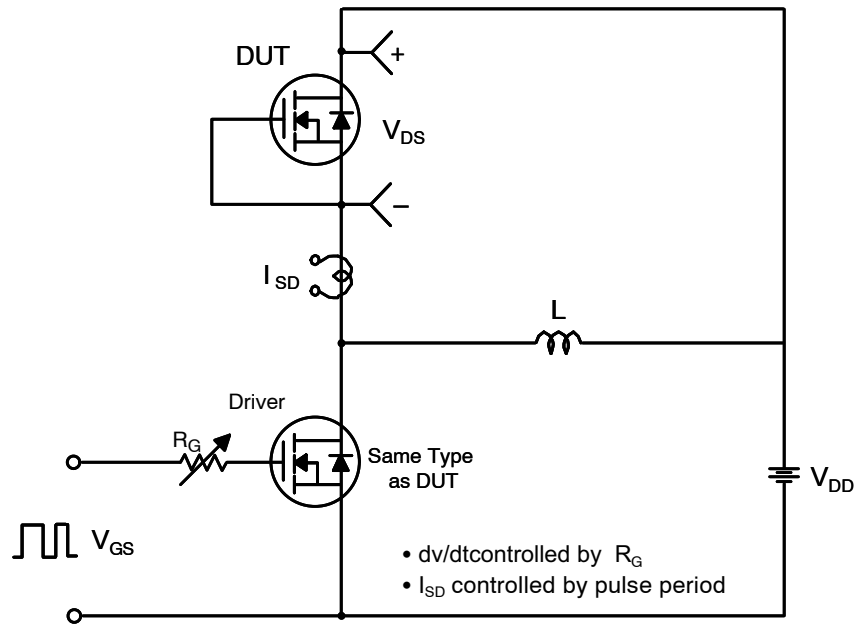


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

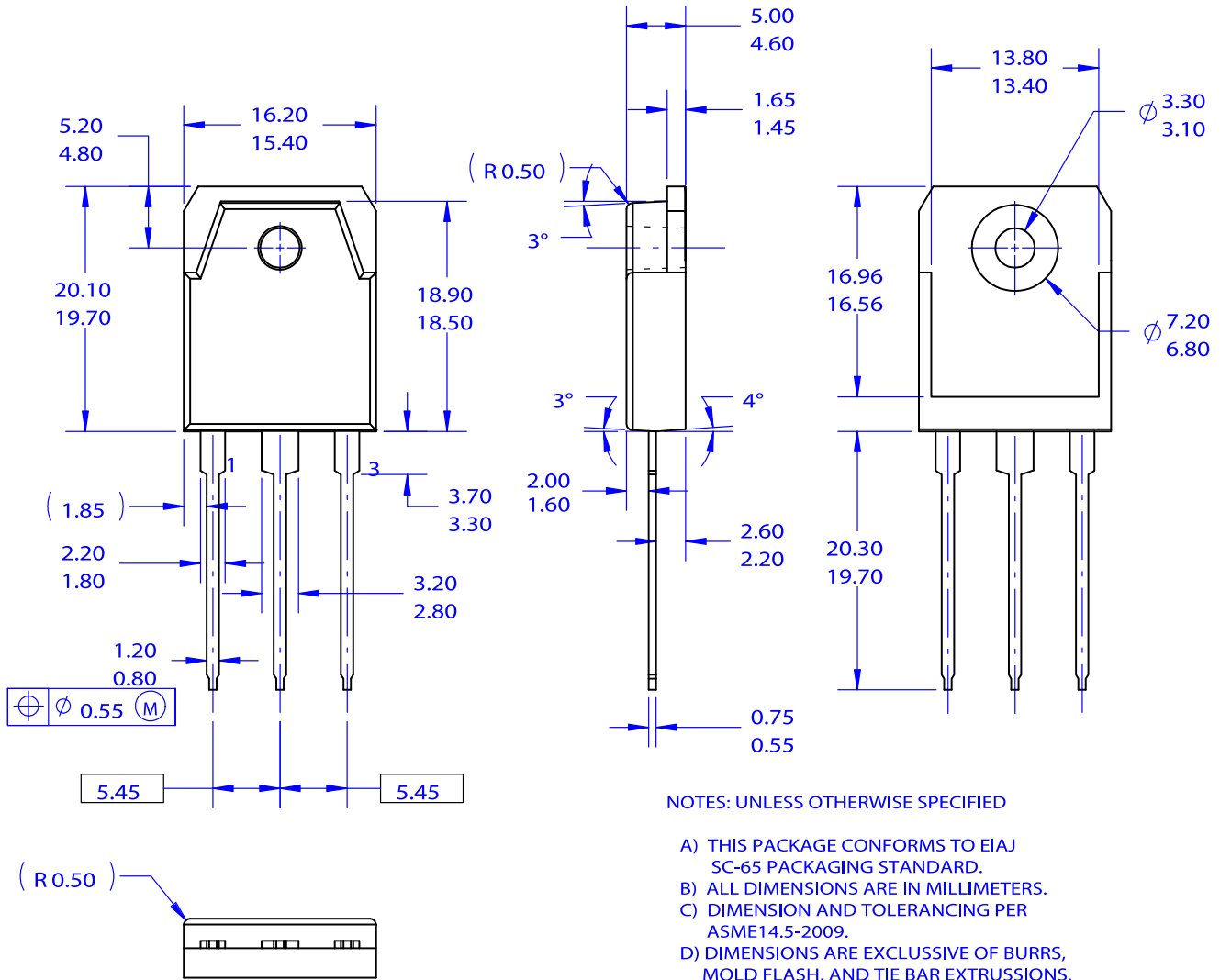
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