



**THE DATASHEET OF  
FQB7N65CTM**



# FQB7N65C

## 650V N-Channel MOSFET

### Features

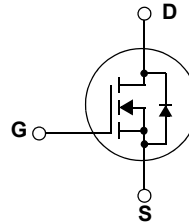
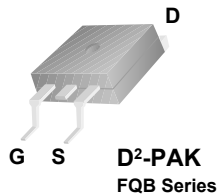
- 7A, 650V,  $R_{DS(on)} = 1.4\Omega @ V_{GS} = 10\text{ V}$
- Low gate charge ( typical 28 nC)
- Low Crss ( typical 12 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS Compliant



### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.



### Absolute Maximum Ratings

Symbol	Parameter	FQB7N65C	Units
$V_{DSS}$	Drain-Source Voltage	650	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	7	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	4.45	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	28	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	212	mJ
$I_{AR}$	Avalanche Current (Note 1)	7	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	17.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	173	W
	- Derate above $25^\circ\text{C}$	1.38	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQB7N65C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.75	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB7N65C	FQB7N65CTM	D2-PAK	330mm	24mm	800

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

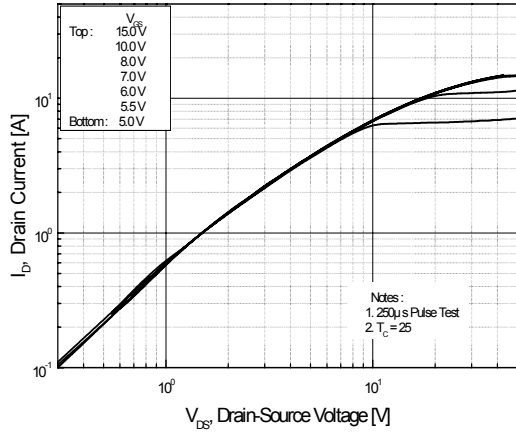
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	650	--	--	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.8	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 520 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A	--	1.2	1.4	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 3.5 A (Note 4)	--	8	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	955	1245	pF
C <sub>oss</sub>	Output Capacitance		--	100	130	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	12	16	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 325 V, I <sub>D</sub> = 7 A, R <sub>G</sub> = 25 Ω  (Note 4, 5)	--	20	50	ns
t <sub>r</sub>	Turn-On Rise Time		--	50	110	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	90	190	ns
t <sub>f</sub>	Turn-Off Fall Time		--	55	120	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 520 V, I <sub>D</sub> = 7 A, V <sub>GS</sub> = 10 V  (Note 4, 5)	--	28	36	nC
Q <sub>gs</sub>	Gate-Source Charge		--	4.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	12	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	7	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	28	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7 A, dI <sub>F</sub> / dt = 100 A/μs  (Note 4)	--	400	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	3.3	--	μC

### NOTES:

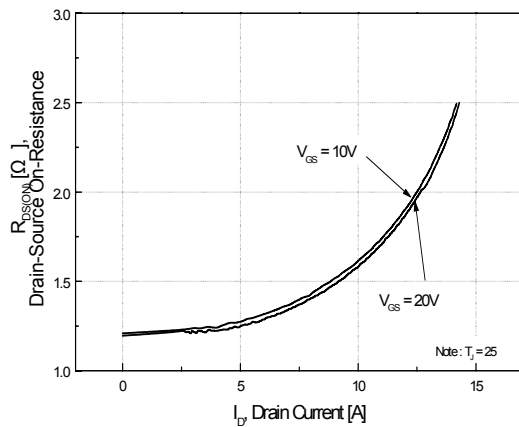
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 8mH, I<sub>AS</sub> = 7A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 7A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

## Typical Performance Characteristics

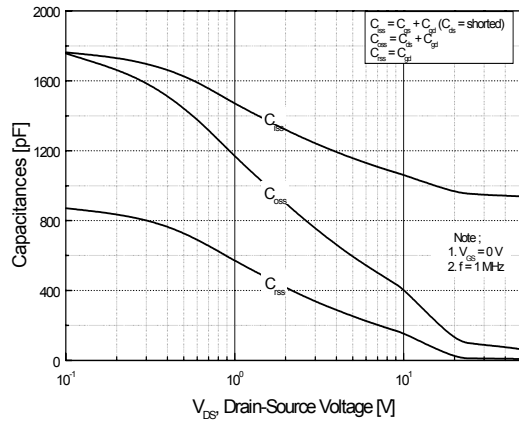
**Figure 1. On-Region Characteristics**



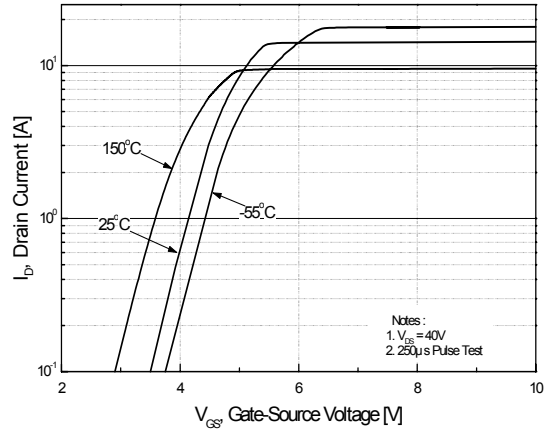
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



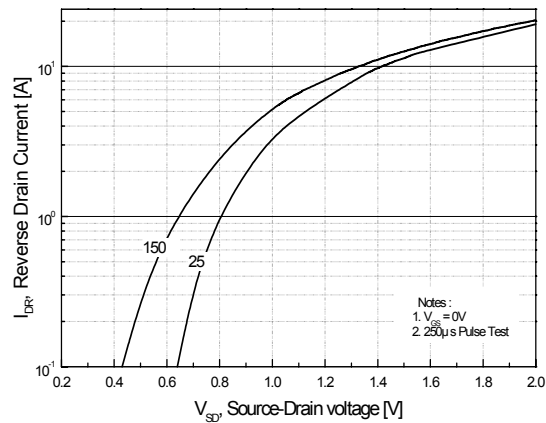
**Figure 5. Capacitance Characteristics**



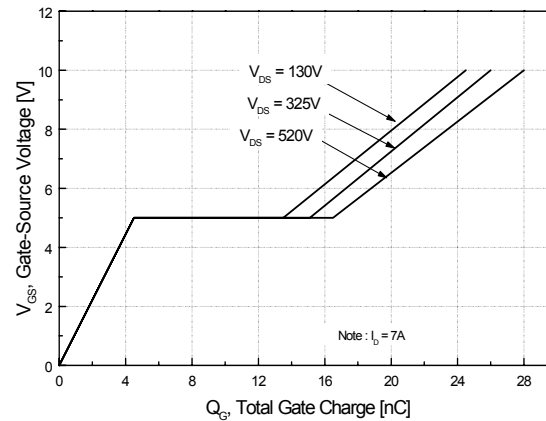
**Figure 2. Transfer Characteristics**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

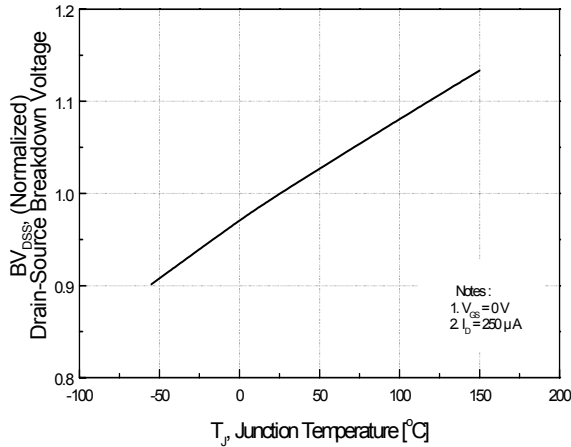


**Figure 6. Gate Charge Characteristics**

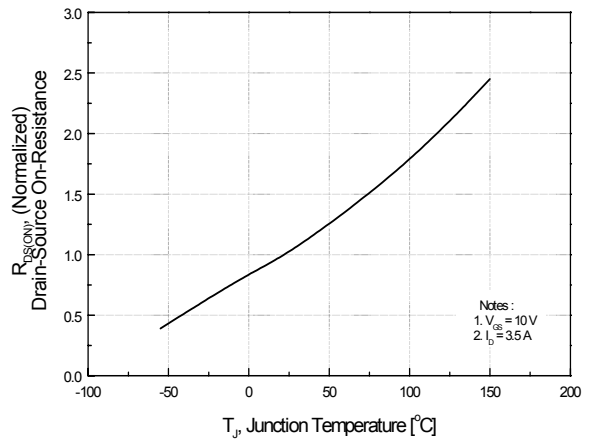


**Typical Performance Characteristics** (Continued)

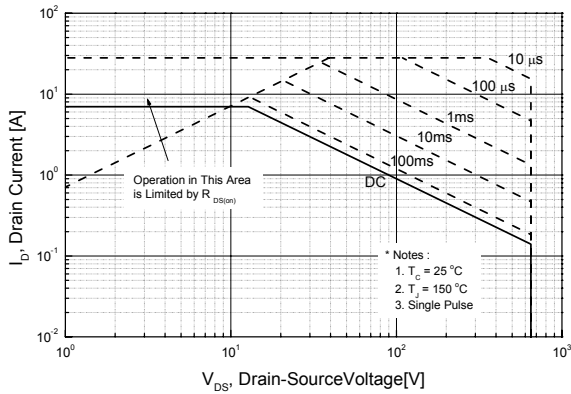
**Figure 7. Breakdown Voltage Variation vs. Temperature**



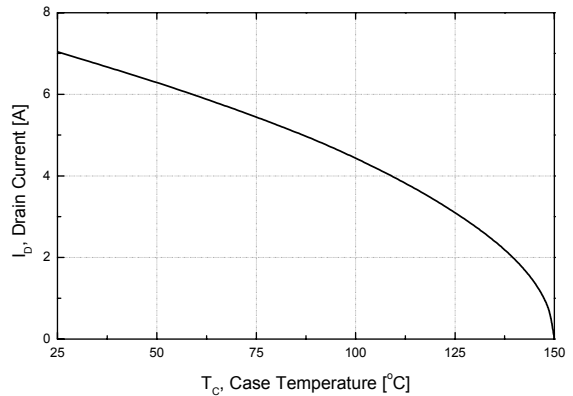
**Figure 8. On-Resistance Variation vs. Temperature**



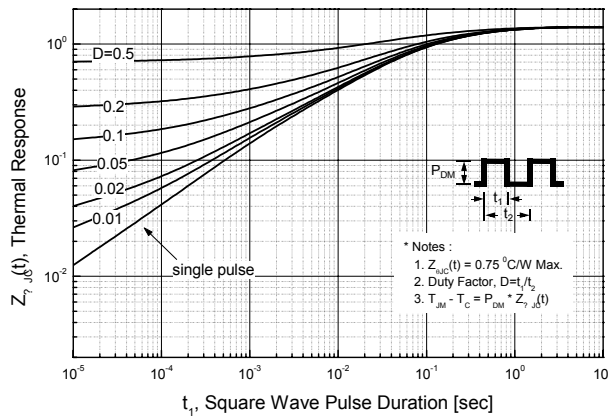
**Figure 9. Maximum Safe Operating Area**



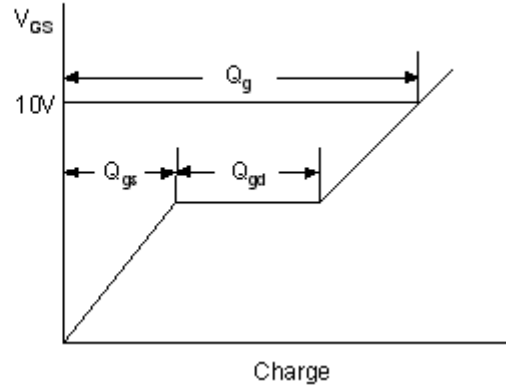
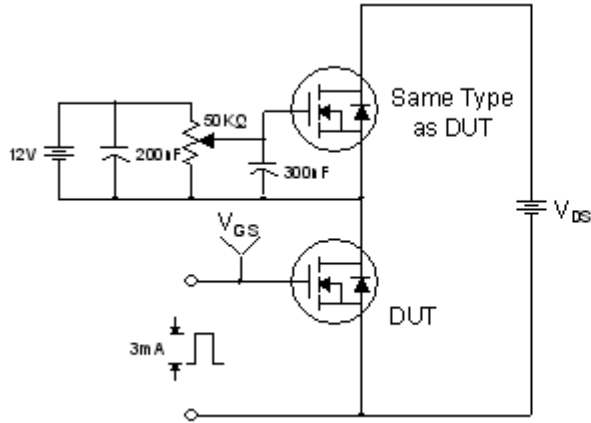
**Figure 10. Maximum Drain Current vs. Case Temperature**



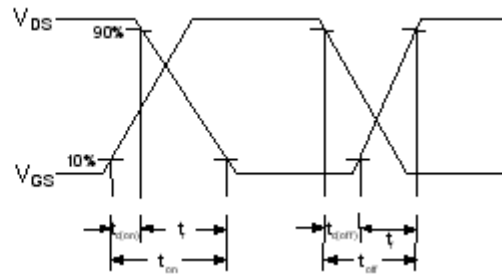
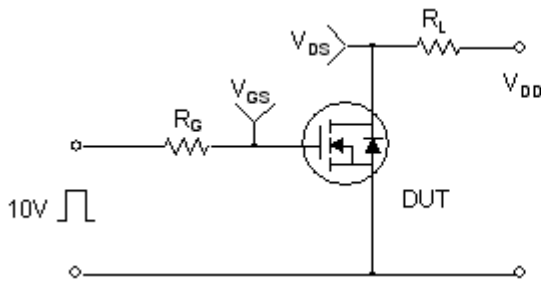
**Figure 11. Transient Thermal Response Curve**



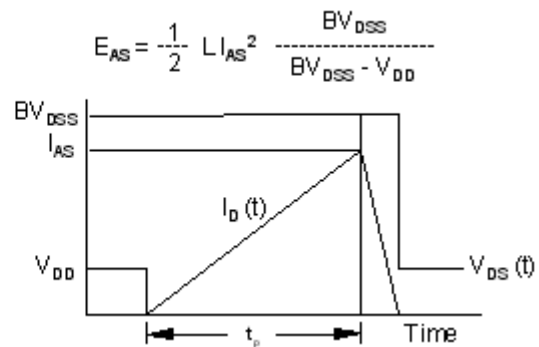
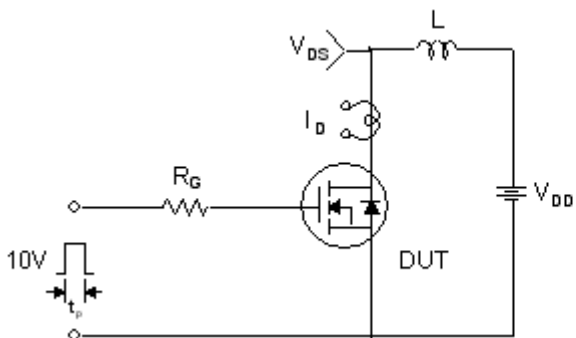
**Gate Charge Test Circuit & Waveform**



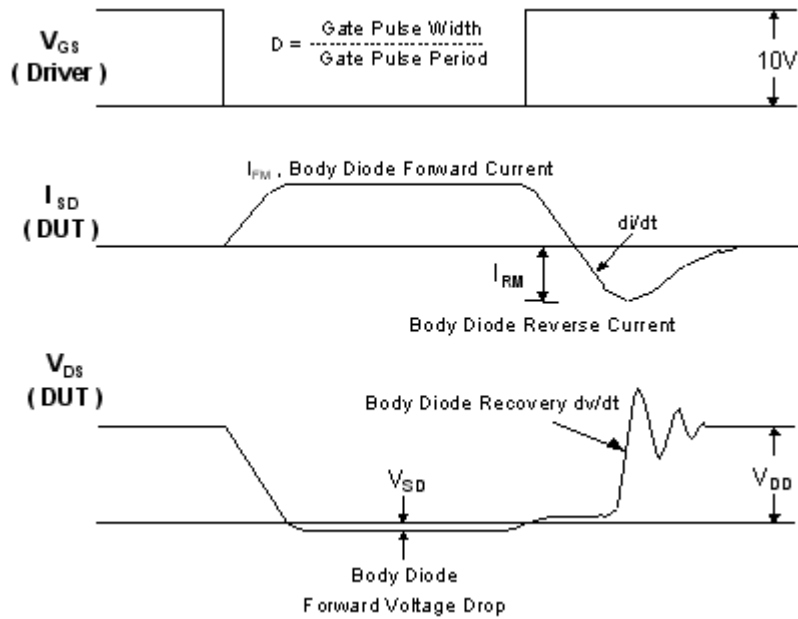
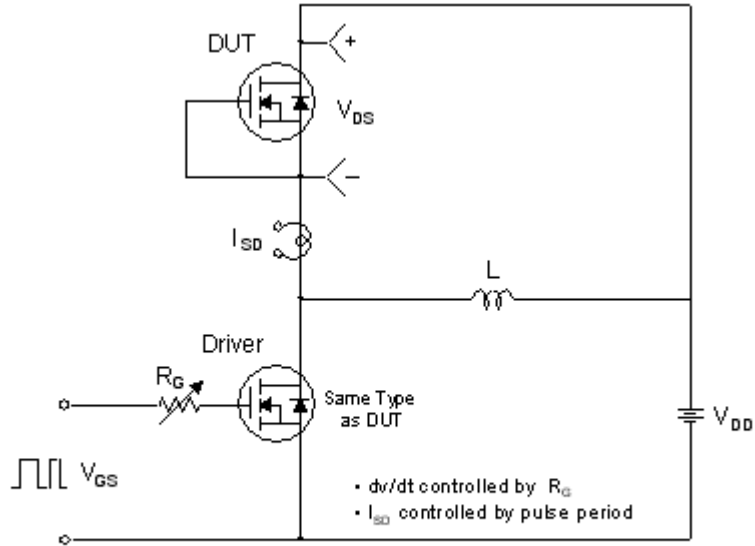
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

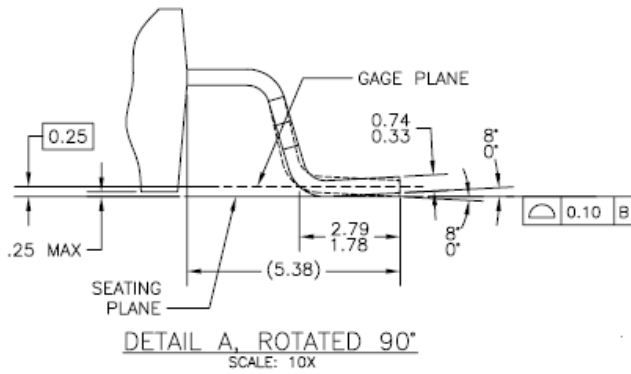
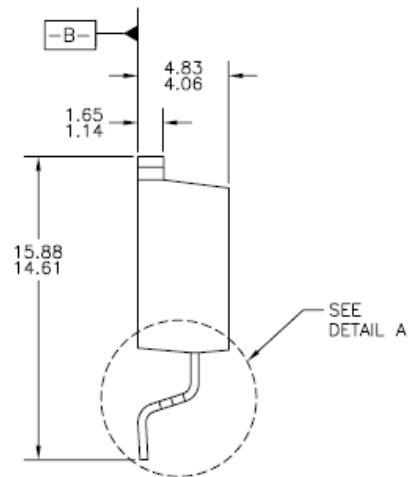
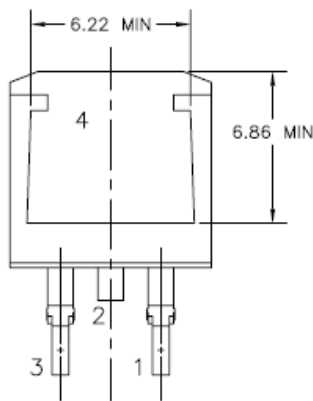
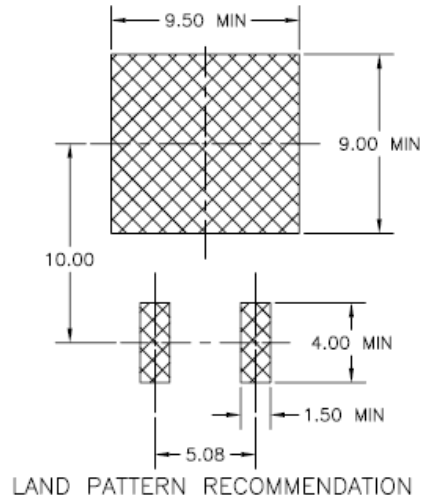
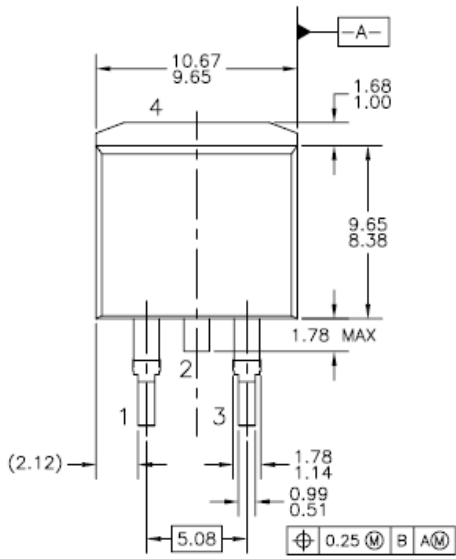


**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



**Mechanical Dimensions**

**D<sup>2</sup> - PAK**



Dimensions in Millimeters


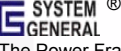


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