



**THE DATASHEET OF
FQD30N06LTM**



FQD30N06L / FQU30N06L

60V LOGIC N-Channel MOSFET

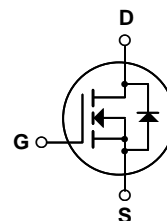
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

Features

- 24A, 60V, $R_{DS(on)} = 0.039\Omega @ V_{GS} = 10V$
- Low gate charge (typical 15 nC)
- Low Crss (typical 50 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 150°C maximum junction temperature rating
- Low level gate drive requirements allowing direct operation from logic drivers
- RoHS Compliant



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FQD30N06L / FQR30N06L	Units
V _{DSS}	Drain-Source Voltage	60	V
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C)	24	A
		15	A
I _{DM}	Drain Current - Pulsed (Note 1)	96	A
V _{GSS}	Gate-Source Voltage	± 20	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	400	mJ
I _{AR}	Avalanche Current (Note 1)	24	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	7.0	V/ns
P _D	Power Dissipation (T _A = 25°C) *	2.5	W
	Power Dissipation (T _C = 25°C) - Derate above 25°C	44	W
		0.35	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R _{θJC}	Thermal Resistance, Junction-to-Case	--	2.85	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.07	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 48\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = 5\text{ V}, I_D = 250\ \mu\text{A}$	1.0	--	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$	--	0.031	0.039	Ω
		$V_{GS} = 5\text{ V}, I_D = 12\text{ A}$	--	0.038	0.047	
g_{FS}	Forward Transconductance	$V_{DS} = 25\text{ V}, I_D = 12\text{ A}$ (Note 4)	--	23	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	800	1040	pF
C_{oss}	Output Capacitance		--	270	350	pF
C_{rss}	Reverse Transfer Capacitance		--	50	65	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 16\text{ A},$ $R_G = 25\ \Omega$	--	15	40	ns
t_r	Turn-On Rise Time		--	210	430	ns
$t_{d(off)}$	Turn-Off Delay Time		--	55	120	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	--	110	230
Q_g	Total Gate Charge	$V_{DS} = 48\text{ V}, I_D = 32\text{ A},$ $V_{GS} = 5\text{ V}$	--	15	20	nC
Q_{gs}	Gate-Source Charge		--	3.5	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4, 5)	--	8.5	--

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	24	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	96	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 24\text{ A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = 32\text{ A},$	--	55	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	80	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 0.8\text{ mH}, I_{AS} = 24\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 32\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

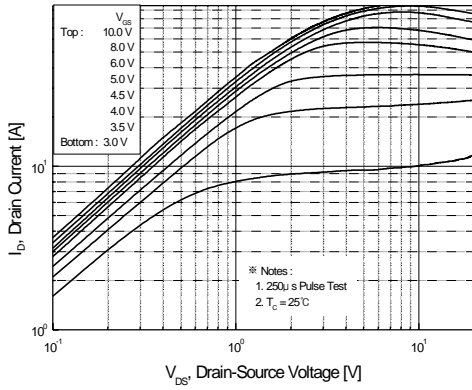


Figure 1. On-Region Characteristics

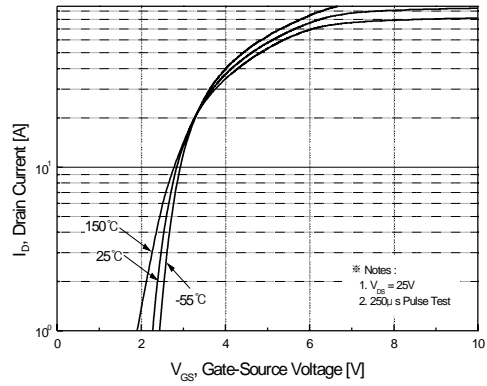


Figure 2. Transfer Characteristics

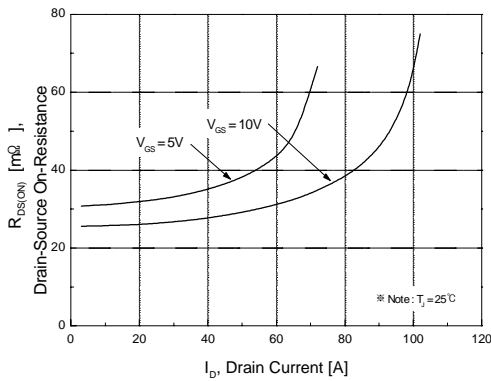


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

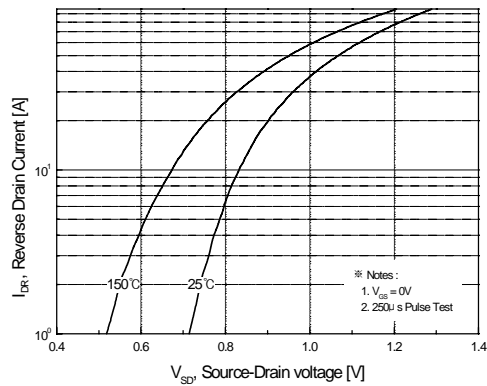


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

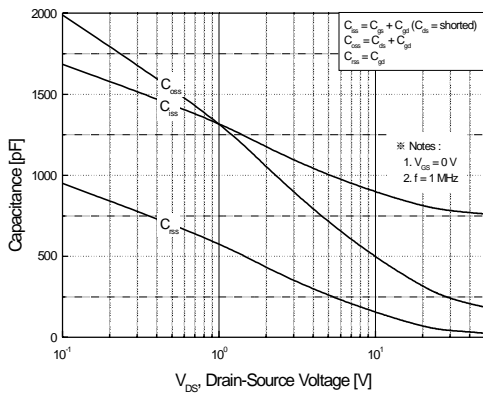


Figure 5. Capacitance Characteristics

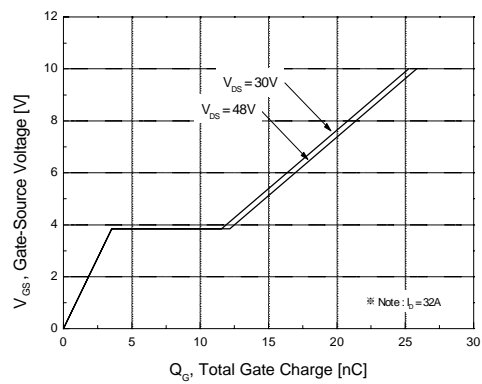


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

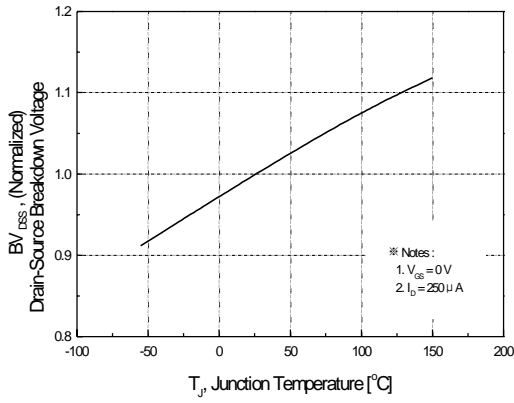


Figure 7. Breakdown Voltage Variation vs. Temperature

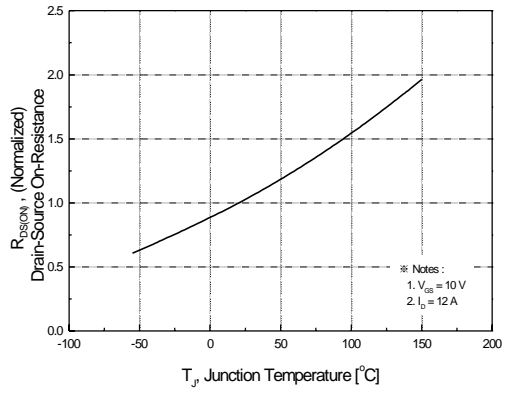


Figure 8. On-Resistance Variation vs. Temperature

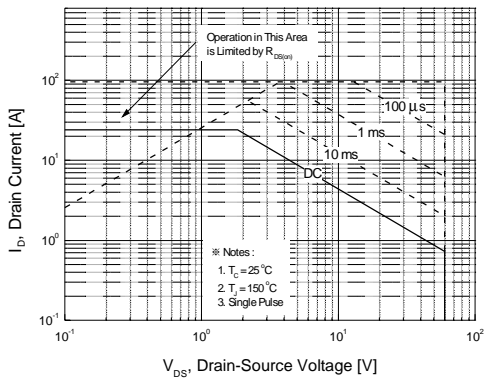


Figure 9. Maximum Safe Operating Area

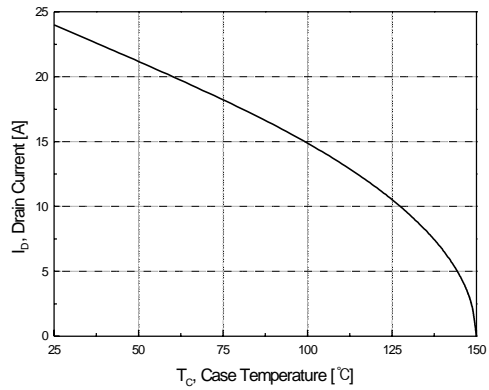


Figure 10. Maximum Drain Current vs. Case Temperature

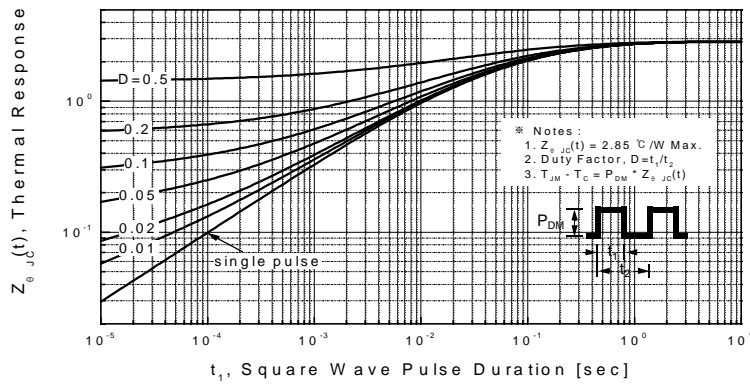
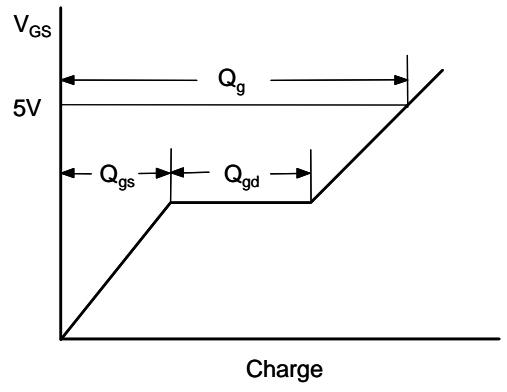
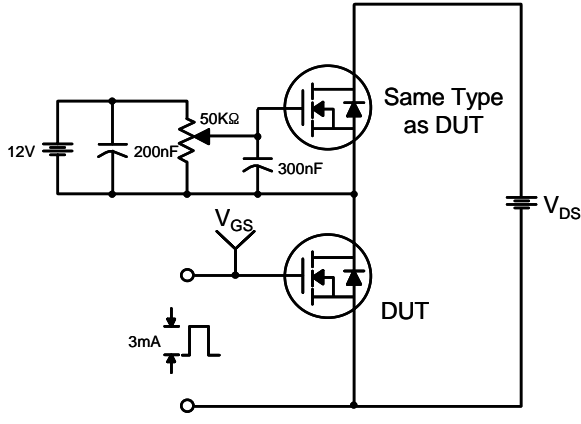
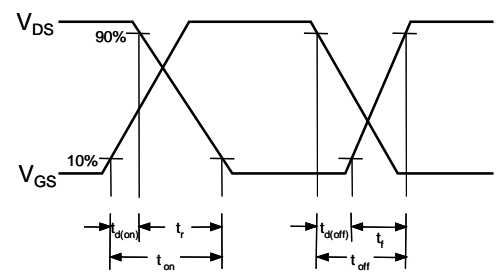
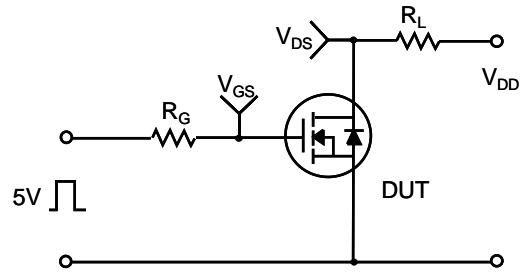


Figure 11. Transient Thermal Response Curve

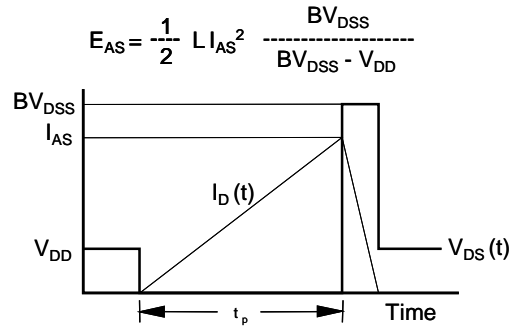
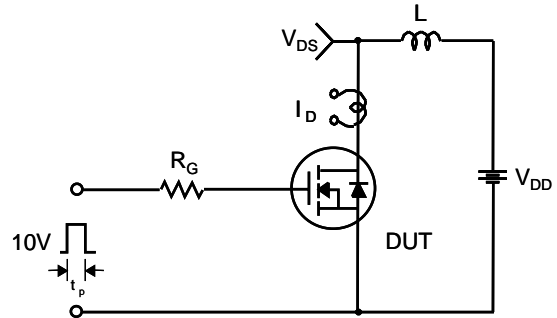
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

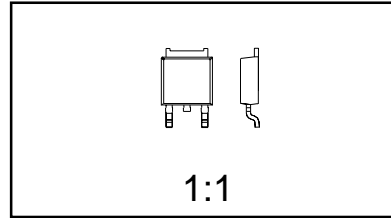
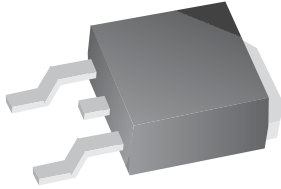


Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions

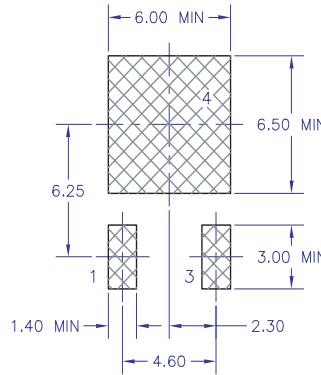
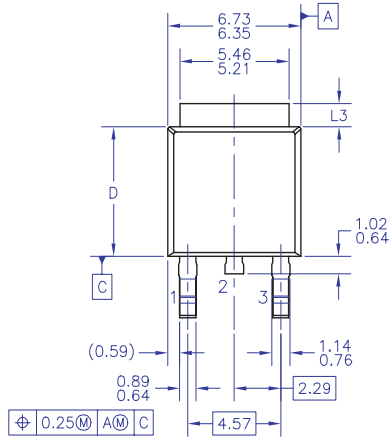
TO-252 (DPAK) (FS PKG Code 36)



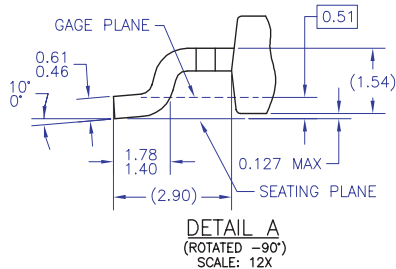
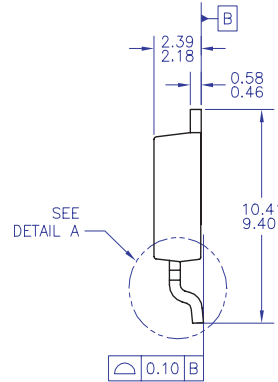
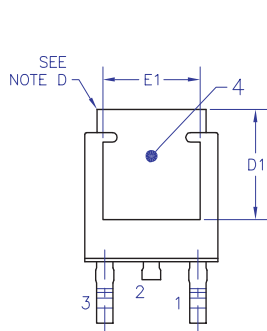
Scale 1:1 on letter size paper

Dimensions shown below are in:
millimeters

Part Weight per unit (gram): 0.33



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED






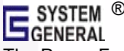
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89-1.27	1.52-2.03
D	5.97-6.22	5.33-5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN



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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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