



**THE DATASHEET OF
FQD6N60CTM_WS**



FQD6N60C

600V N-Channel MOSFET

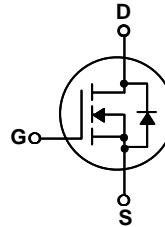
Features

- 4 A, 600 V, $R_{DS(on)} = 2.0 \Omega @ V_{GS} = 10 \text{ V}$
- Low gate charge (typical 16 nC)
- Low C_{rss} (typical 7 pF)
- Fast switching
- 100 % avalanche tested
- Improved dv/dt capability

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.



Absolute Maximum Ratings

Symbol	Parameter	FQD6N60C	Units
V_{DSS}	Drain-Source Voltage	600	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	4
		- Continuous ($T_C = 100^\circ\text{C}$)	2.4
I_{DM}	Drain Current - Pulsed (Note 1)	16	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	300	mJ
I_{AR}	Avalanche Current (Note 1)	4.0	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	8.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	80	W
		- Derate above 25°C	0.78
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	1.56	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C}/\text{W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQD6N60C	FQD6N60CTM	DPAK	380mm	16mm	2500
FQD6N60C	FQD6N60CTF	DPAK	380mm	16mm	2000

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	600	--	--	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.6	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 480 V, T _C = 125°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 2.0 A	--	1.7	2.0	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 2.0 A (Note 4)	--	4.8	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	620	810	pF
C _{oss}	Output Capacitance		--	65	85	pF
C _{rss}	Reverse Transfer Capacitance		--	7	10	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 300 V, I _D = 5.5 A, R _G = 25 Ω (Note 4, 5)	--	15	40	ns
t _r	Turn-On Rise Time		--	45	100	ns
t _{d(off)}	Turn-Off Delay Time		--	45	100	ns
t _f	Turn-Off Fall Time		--	45	100	ns
Q _g	Total Gate Charge	V _{DS} = 480 V, I _D = 5.5 A, V _{GS} = 10 V (Note 4, 5)	--	16	20	nC
Q _{gs}	Gate-Source Charge		--	3.5	--	nC
Q _{gd}	Gate-Drain Charge		--	6.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	4.0	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	16	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 4.0 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 5.5 A, dI _F / dt = 100 A/μs (Note 4)	--	310	--	ns
Q _{rr}	Reverse Recovery Charge		--	2.1	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 34.3 mH, I_{AS} = 4.0 A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 4.0 A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

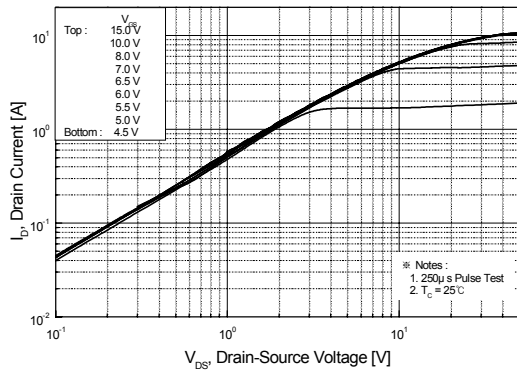


Figure 2. Transfer Characteristics

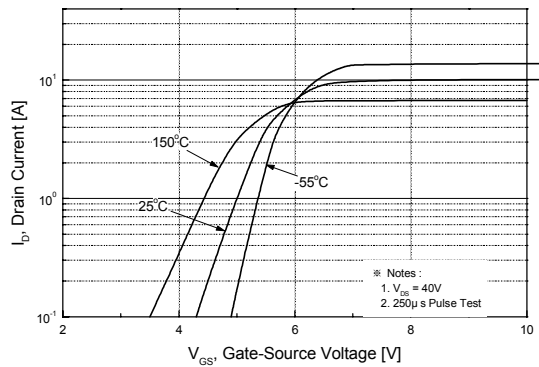


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

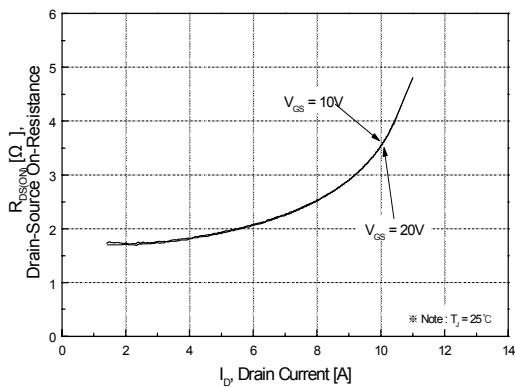


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

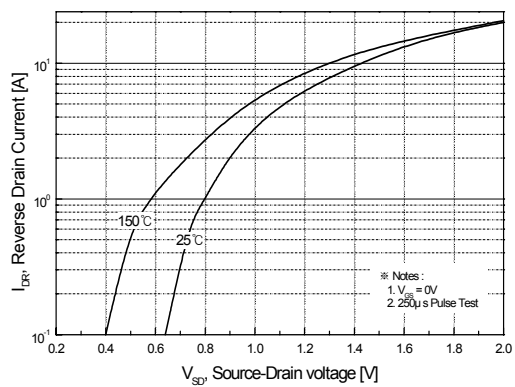


Figure 5. Capacitance Characteristics

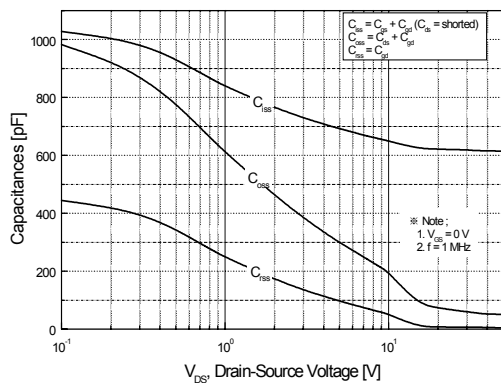
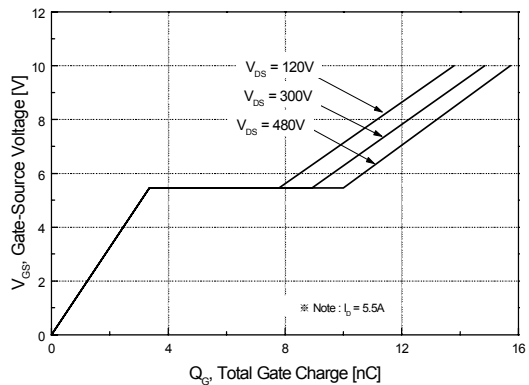


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

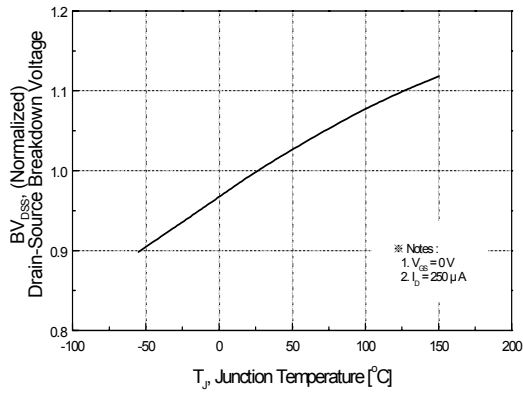


Figure 8. On-Resistance Variation vs. Temperature

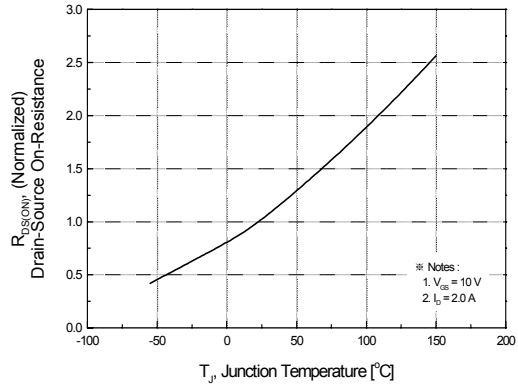


Figure 9. Maximum Safe Operating Area

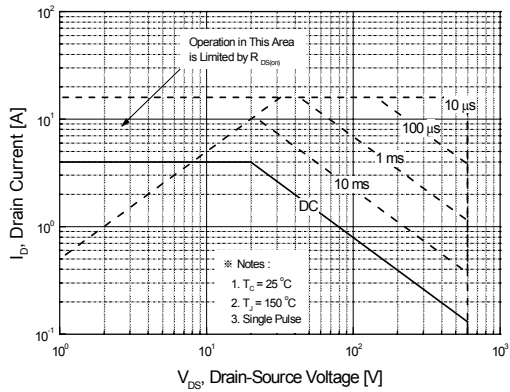


Figure 10. Maximum Drain Current vs. Case Temperature

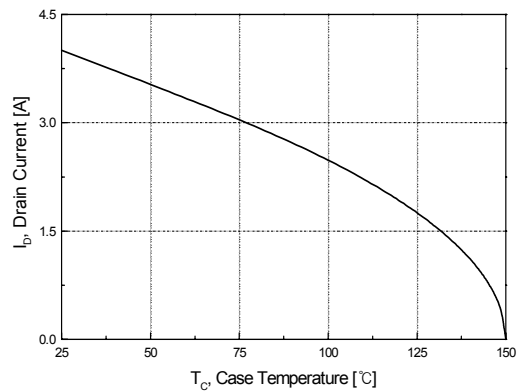
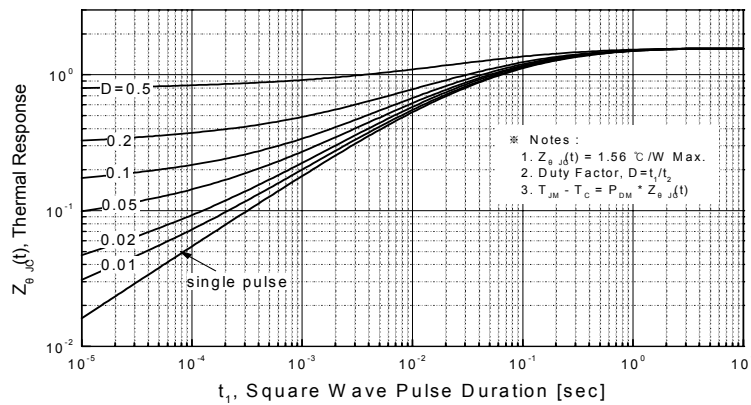
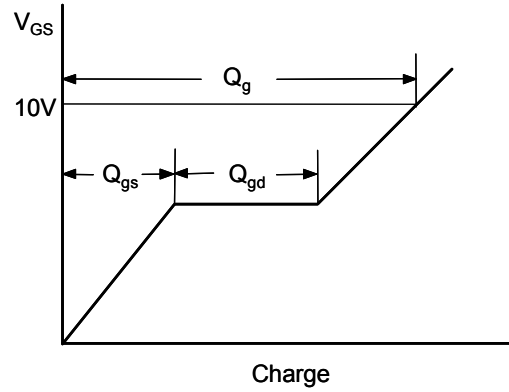
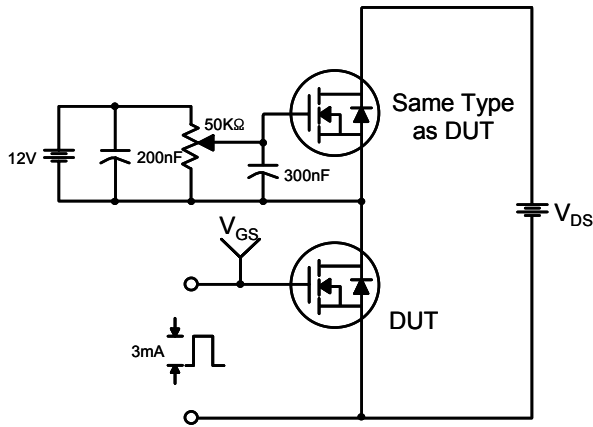


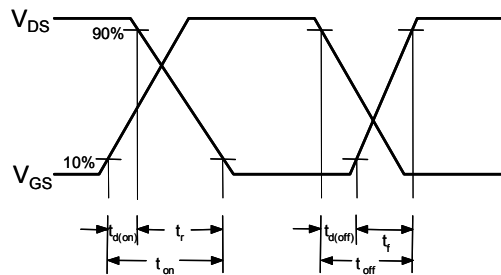
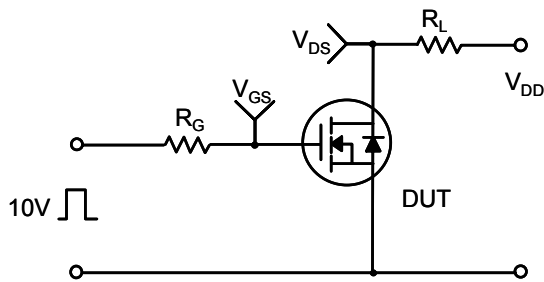
Figure 11. Transient Thermal Response Curve



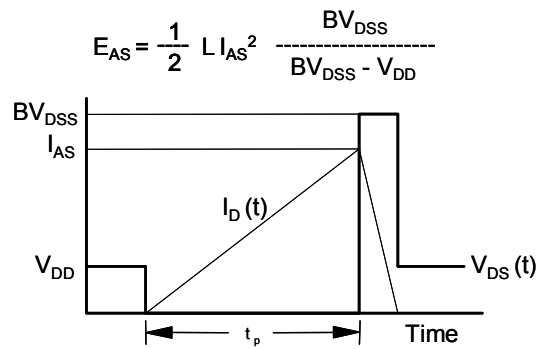
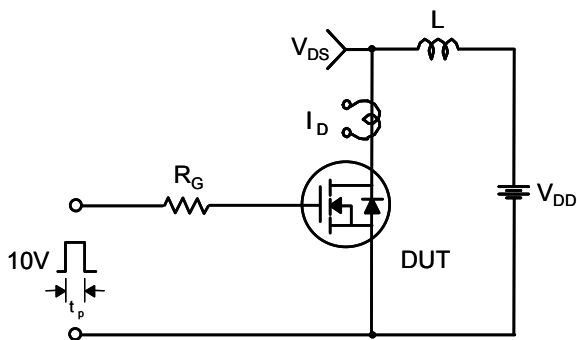
Gate Charge Test Circuit & Waveform



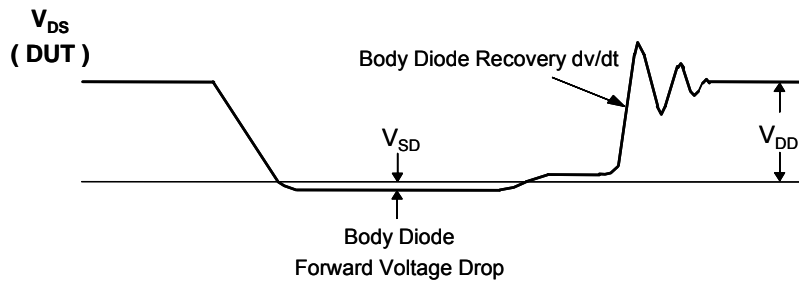
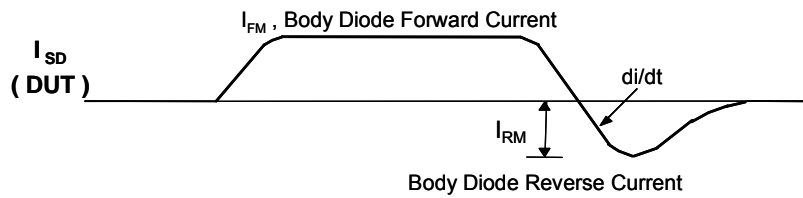
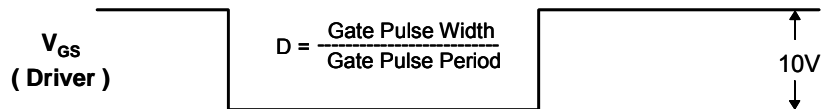
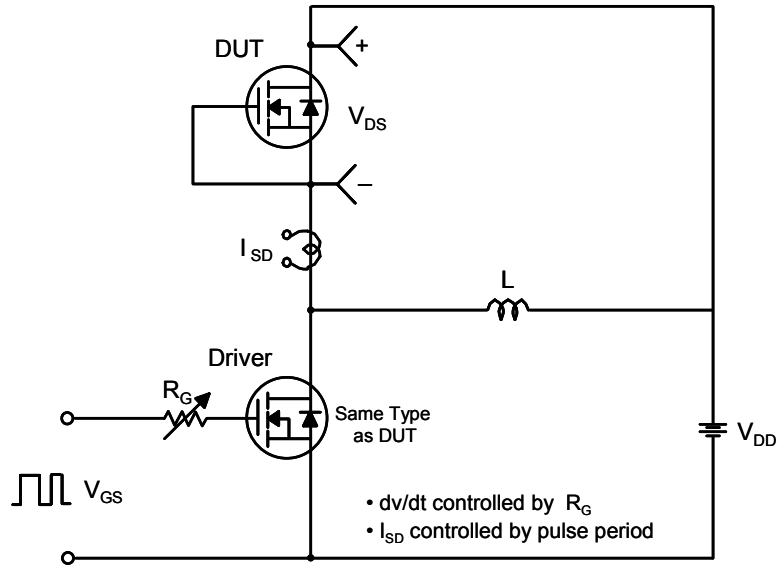
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

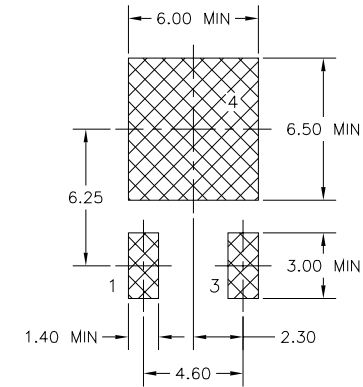
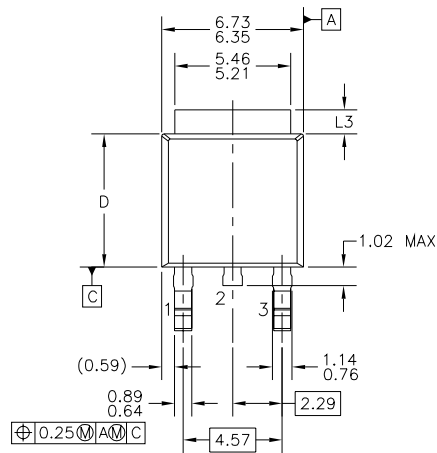


Peak Diode Recovery dv/dt Test Circuit & Waveforms

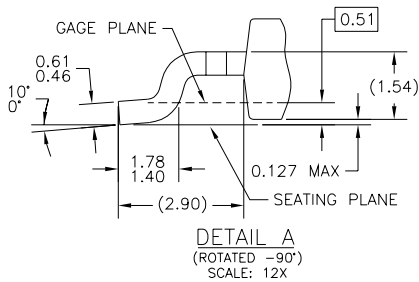
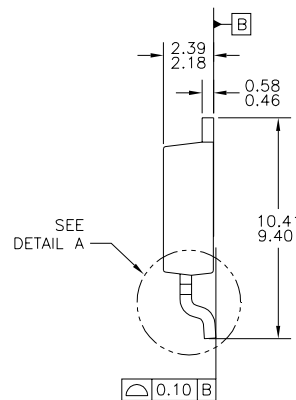
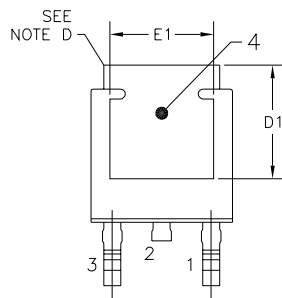


Mechanical Dimensions

D-PAK



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3, D, E1 & D1 TABLE:
- | | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN | 3.81 MIN |
| D1 | 5.21 MIN | 4.57 MIN |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	IntelliMAX™	POP™	SPM™
ActiveArray™	FASTr™	ISOPLANAR™	Power247™	Stealth™
Bottomless™	FPS™	LittleFET™	PowerEdge™	SuperFET™
CoolFET™	FRFET™	MICROCOUPLER™	PowerSaver™	SuperSOT™-3
CROSSVOLT™	GlobalOptoisolator™	MicroFET™	PowerTrench®	SuperSOT™-6
DOME™	GTO™	MicroPak™	QFET®	SuperSOT™-8
EcoSPARK™	HiSeC™	MICROWIRE™	QS™	SyncFET™
E ² C MOS™	I ² C™	MSX™	QT Optoelectronics™	TinyLogic®
EnSigna™	i-Lo™	MSXPro™	Quiet Series™	TINYOPTO™
FACT™	ImpliedDisconnect™	OCX™	RapidConfigure™	TruTranslation™
FACT Quiet Series™		OCXPro™	RapidConnect™	UHC™
Across the board. Around the world.™		OPTOLOGIC®	µSerDes™	UltraFET®
The Power Franchise®		OPTOPLANAR™	SILENT SWITCHER®	UniFET™
Programmable Active Droop™		PACMAN™	SMART START™	VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I15

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View FQD6N60CTM_WS](#) on WIN SOURCE
- ⊖ [Fairchild/ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management