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FT10001

Reset Timer with Fixed Delay and Reset Pulse

Features

- Fixed Reset Delay: 10 Seconds
- One Input Reset Pin
- Open-Drain Output Pin with Fixed 530ms Pulse
- 1.8V to 5.0V Operation ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)
- 1.7V to 5.0V Operation ($T_A = -25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)
- 1.65V to 5.00V Operation ($T_A = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)
- $<1\mu\text{A}$ I_{CCQ} Consumption
- Zero-Second Test-Mode Enable
- Integrated Pull-Up Resistor on /SRO

Applications

- Cell Phones
- Portable Media Players
- Tablets
- Mobile Devices
- Consumer Medical

Description

The FT10001 is a timer for resetting a mobile device where long reset times are needed. The long delay helps avoid unintended resets caused by accidental key presses. It has a fixed delay of $10 \pm 20\%$ seconds. The DSR pin enables Test Mode operation by immediately forcing /RST1 LOW for factory testing.

The FT10001 has one input for single-button resetting capability. The device has a single open-drain output with 0.5mA pull-down drive.

FT10001 draws minimal I_{CC} current when inactive and functions over a power supply range of 1.65V to 5.00V.

Ordering Information

| Part Number | Operating Temperature Range | Package | Packing Method |
|-------------|--|--|-----------------------------|
| FT10001L6X | -40°C to $+85^{\circ}\text{C}$ | 6-Lead, MicroPak™ 1.0 x 1.45mm, JEDEC MO-252 | 5000 Units on Tape and Reel |
| FT10001FHX | -40°C to $+85^{\circ}\text{C}$ | 6-Lead, MicroPak2™ 1.0 x 1.0mm Body, .35mm Pitch | 5000 Units on Tape and Reel |

Block Diagram

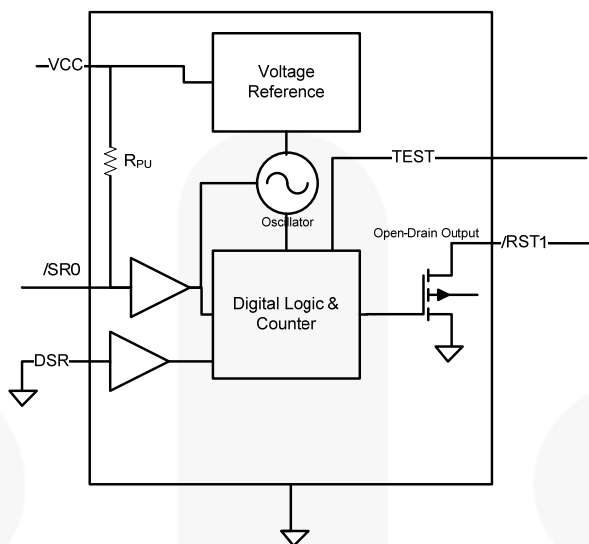


Figure 1. Block Diagram

Pin Configuration

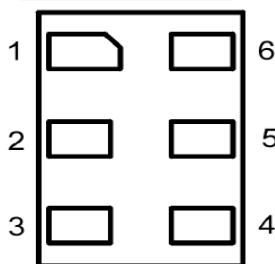


Figure 2. Pad Assignments (Top-Through View)

Pin Definitions

| Pin # | Name | Description | |
|-------|-------|---|--|
| | | Normal Operation | Zero-Second Factory-Test Mode |
| 1 | /RST1 | Open-drain output, active LOW | Open-drain output, active LOW |
| 2 | GND | GND | GND |
| 3 | /SR0 | Reset input with integrated pull-up, active LOW | Reset input with integrated pull-up, active LOW |
| 4 | VCC | Power supply | Power supply |
| 5 | DSR | Delay selection input; tie to GND during normal operation. ⁽¹⁾ | Delay selection input. Pull HIGH to enable Zero-second delay for factory test. |
| 6 | TEST | Used for device testing; tie to GND during normal operation. | Used for device testing; tie to GND during normal operation. |

Note:

1. This pin must always be tied to either GND or VCC. It must not float.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|------------------|---|-----------------------------------|------|------|------|
| V _{CC} | Supply Voltage | | -0.5 | 7.0 | V |
| V _{IN} | DC Input Voltage | /SR0, DSR | -0.5 | 7.0 | V |
| V _{OUT} | Output Voltage ⁽²⁾ | /RST1 | -0.5 | 7.0 | V |
| I _{IK} | DC Input Diode Current | V _{IN} < 0V | | -50 | mA |
| I _{OK} | DC Output Diode Current | V _{OUT} < 0V | | -50 | mA |
| I _{OL} | DC Output Sink Current | | | +50 | mA |
| I _{CC} | DC V _{CC} or Ground Current per Supply Pin | | | ±100 | mA |
| T _{STG} | Storage Temperature Range | | -65 | +150 | °C |
| T _J | Junction Temperature Under Bias | | | +150 | °C |
| T _L | Junction Lead Temperature, Soldering 10 Seconds | | | +260 | °C |
| P _D | Power Dissipation | | | 5 | mW |
| ESD | Electrostatic Discharge Capability | Human Body Model, JESD22-A114 | | 4 | kV |
| | | Charged Device Model, JESD22-C101 | | 2 | |

Note:

- All output current Absolute Maximum Ratings must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|------------------|--|--|------|------|------|
| V _{CC} | Supply Voltage | -40°C to +85°C | 1.8 | 5.0 | V |
| | | -25°C to +85°C | 1.7 | 5.0 | |
| | | 0°C to +85°C | 1.65 | 5.00 | |
| t _{RFC} | V _{CC} Recovery Time After Power Down | V _{CC} =0V After Power Down, Rising to 0.5V | 5 | | ms |
| V _{IN} | Input Voltage | /SR0 | 0 | 5 | V |
| V _{OUT} | Output Voltage | /RST1 | 0 | 5 | V |
| I _{OL} | DC Output Sink Current | /RST1, V _{CC} =2.0V to 5.0V | | +0.5 | mA |
| T _A | Free-Air Operating Temperature | | -40 | +85 | °C |
| θ _{JA} | Thermal Resistance | | | 350 | °C/W |

DC Electrical Characteristics

Conditions of $T_A = -40^{\circ}\text{C}$ to 80°C with $V_{CC} = 1.8\text{V} - 5.0\text{V}$ OR $T_A = -25^{\circ}\text{C}$ to 85°C with $V_{CC} = 1.7\text{V} - 5.0\text{V}$ OR $T_A = 0^{\circ}\text{C}$ to 85°C with $V_{CC} = 1.65\text{V} - 5.00\text{V}$ produce the performance characteristics below.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|----------|---|--|----------------------|------|----------------------|---------------|
| V_{IH} | Input High Voltage | DSR, /SR0 | $0.65 \times V_{CC}$ | | | V |
| V_{IL} | Input Low Voltage | DSR, /SR0 | | | $0.25 \times V_{CC}$ | V |
| V_{OL} | Low Level Output Voltage | RST, $I_{OL} = 500\mu\text{A}$ | | | 0.3 | V |
| R_{PU} | Integrated Pull-Up Resistor on /SR0 | | | 50 | | k Ω |
| I_{IN} | Input Leakage Current /SR0 | $V_{IN} = V_{CC}$ | | | ± 1 | μA |
| | Input Leakage Current DSR | $0\text{V} \leq V_{IN} \leq 5.0\text{V}$ | | | ± 1 | |
| I_{CC} | Quiescent Supply Current (Timer Inactive) | /SR0 = V_{CC} | | | 1 | μA |
| | Dynamic Supply Current (Timer Active) | /SR0 = 0V | | | 200 | |

AC Electrical Characteristics

Conditions of $T_A = -40^{\circ}\text{C}$ to 80°C with $V_{CC} = 1.8\text{V} - 5.0\text{V}$ OR $T_A = -25^{\circ}\text{C}$ to 85°C with $V_{CC} = 1.7\text{V} - 5.0\text{V}$ OR $T_A = 0^{\circ}\text{C}$ to 85°C with $V_{CC} = 1.65\text{V} - 5.00\text{V}$ produce the performance characteristics below.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|------------|----------------------------------|--|------|------|------|------|
| t_{PHL1} | Timer Delay, /SR0 to RST (DSR=0) | $C_L = 5\text{pF}$, $R_L = 5\text{k}\Omega$, See Figure 4 | 8 | 10 | 12 | s |
| t_{REC} | Reset Timeout Delay | | 420 | 530 | 635 | ms |

Capacitance Specifications

$T_A = +25^{\circ}\text{C}$.

| Symbol | Parameter | Condition | Typ. | Unit |
|-----------|--------------------|------------------------|------|------|
| C_{IN} | Input Capacitance | $V_{CC} = \text{GND}$ | 4 | pF |
| C_{OUT} | Output Capacitance | $V_{CC} = 5.0\text{V}$ | 5 | pF |

Functional Description

Default operation time N is 10s. If the DSR pin is pulled HIGH prior to V_{CC} ramp, the FT10001 enters Test Mode and the reset output, /RST1, is immediately pulled LOW for factory testing. The DSR pin MUST be forced to GND during normal operation. The DSR pin should never be driven HIGH or left to FLOAT during normal operation. The DSR PIN state should never be changed during device operation; it must be biased prior to supplying the V_{CC} supply. If there is a need to use the DSR= V_{CC} Test Mode, the /SR0 must be HIGH when the DSR pin is moved from LOW to HIGH to enter Zero-Second Factory-Test Mode. To return to the standard 10-second reset time, the same procedure must be followed with DSR=GND. The DSR pin should never be allowed to change state while the /SR0 pin is LOW.

Operation Modes

A low input signal on /SR0 starts the oscillator. There are two scenarios for counting: short duration and long duration. In the short-duration scenario, output /RST1 is not affected. In the long-duration scenario, the output /RST1 goes LOW after /SR0 has been held LOW for $\geq 10s$. The /RST1 output returns to its original HIGH

state 530ms after time t_{REC} has expired, regardless of the state of /SR0. The /RST1 output is an open-drain driver. When the count time exceeds time 10s, the /RST1 output pulls LOW.

Short Duration ($t_w < 10s$)

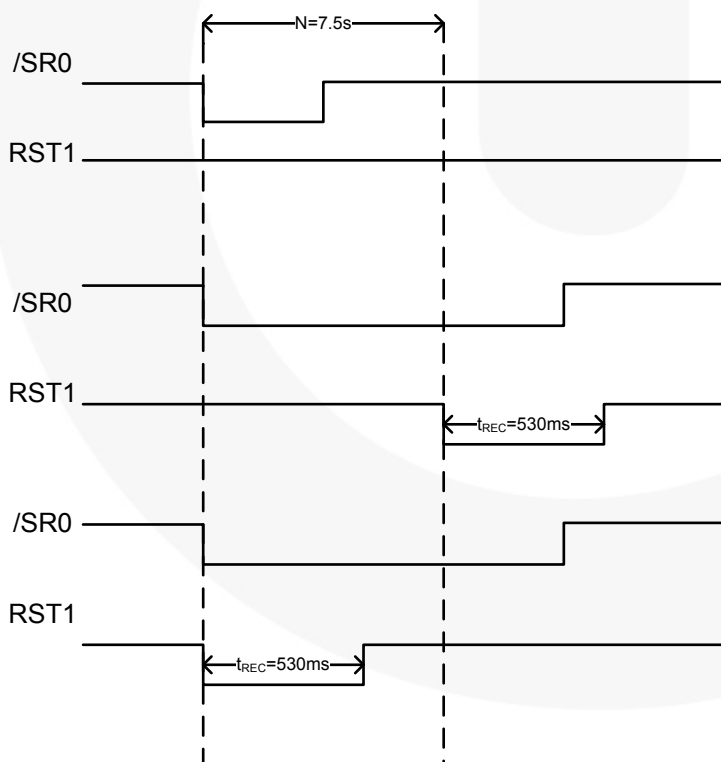
When the /SR0 input goes LOW, the internal timer starts counting. If the /SR0 input goes HIGH before 10s has elapsed, the timer stops counting and resets and no changes occur on the outputs.

Long Duration ($t_w > 10s$)

When the /SR0 input goes LOW, the internal timer starts counting. If the /SR0 input stays LOW for at least 10s, the RST output is enabled and pulled LOW. The output RST is held LOW for t_{REC} , 530ms, as soon as the reset time of 10s is met, regardless of the state of the /SR0 pin. When the /SR0 input has returned HIGH and t_{REC} has expired, the internal timer resets and awaits the next RESET event.

Zero-Second Test Mode

/RST1 goes LOW immediately after /SR0 goes LOW.



Short-Duration, Normal Operation
/RST1 never goes LOW because /SR0 LOW duration does not meet requirement: Reset Time N=10s

Long-Duration, Normal Operation
/RST1 goes LOW because /SR0 LOW duration exceeds requirement: Reset Time N=10s

Zero-Second Factory-Test Mode
/RST1 goes LOW immediately after /SR0 goes LOW

Figure 3. Reset Timing Waveforms

AC Test Circuit and Waveforms

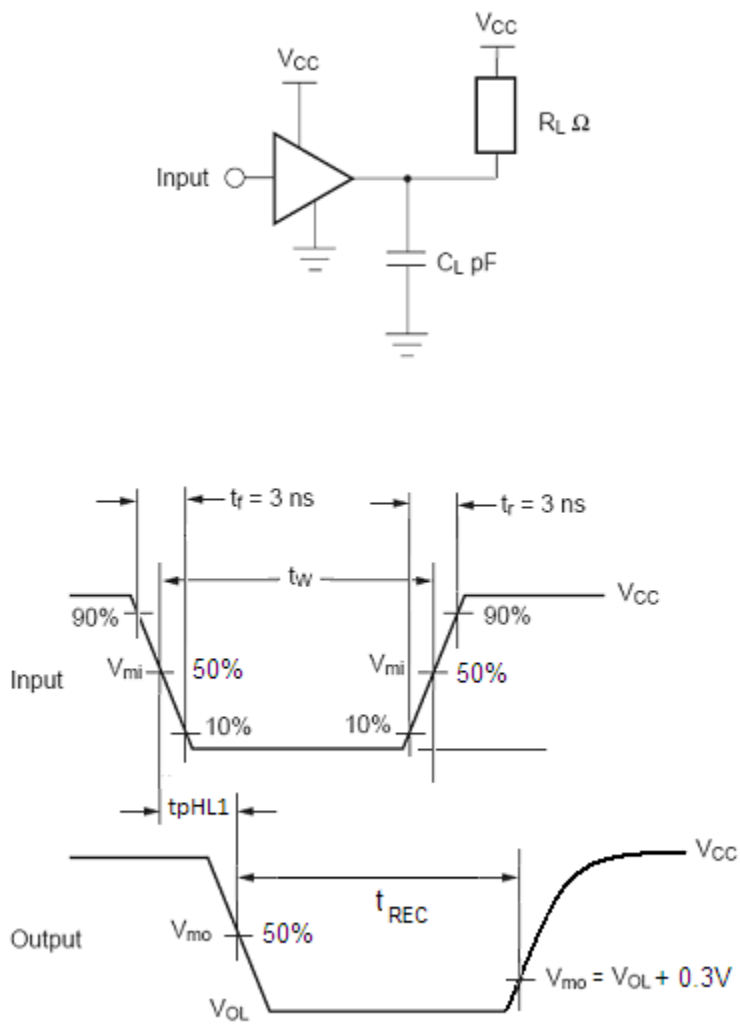
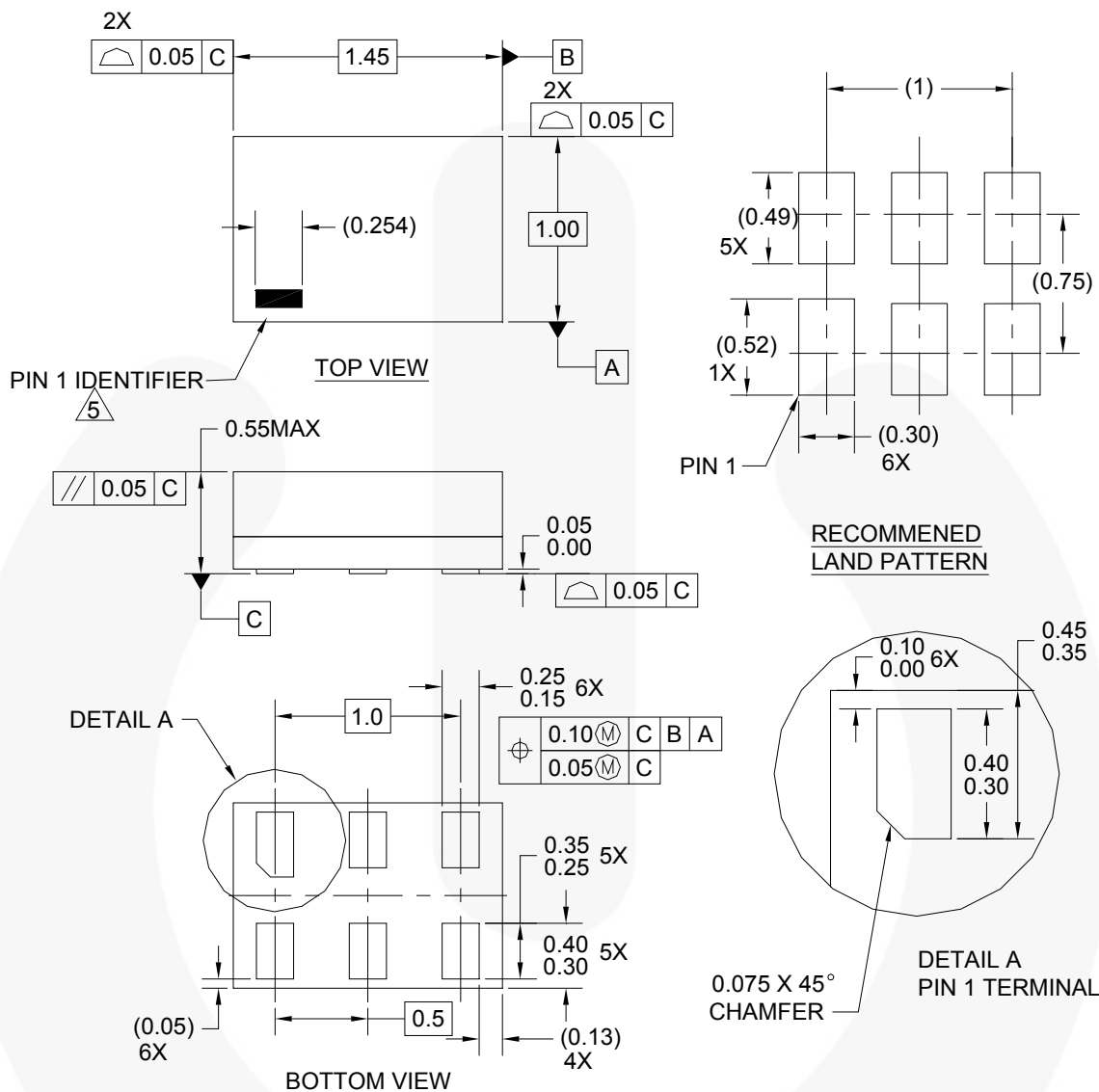


Figure 4. AC Test Circuit and Waveforms for /RST1 Output ST Output



Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 5. 6-Lead MicroPak™ 1.0 x 1.45mm, JEDEC MO-252

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Physical Dimensions

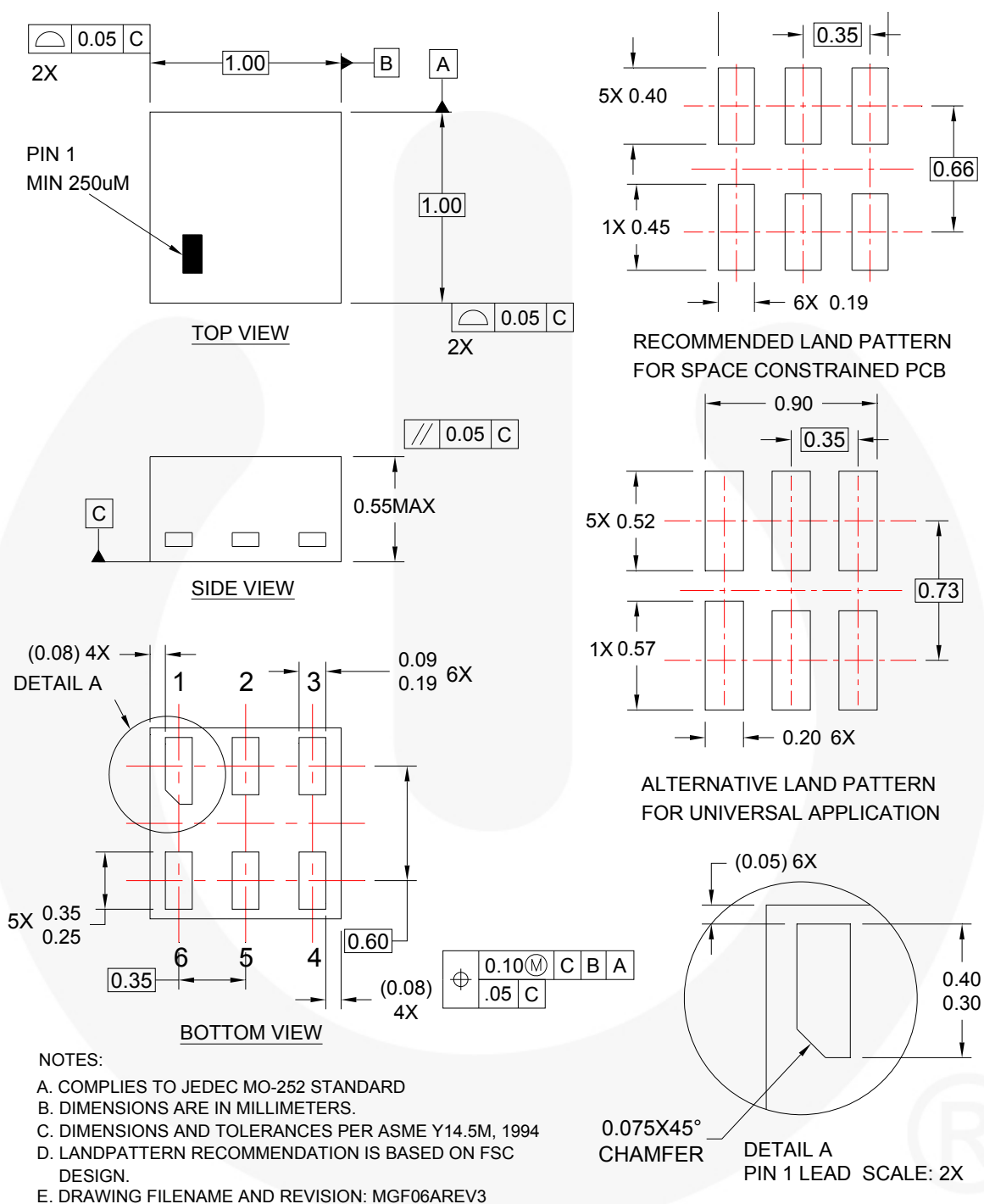


Figure 6. 6-Lead MicroPak2™ 1.0 x 1.0mm, .35mm Pitch

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Rev. I61

Revisions

| | | | |
|-----------|----------|-----------|--|
| Rev 0.0 | 8/1/11 | Sean Ryan | Initial Rev – created from FT7521 datasheet |
| Rev 0.1 | 8/11/11 | Sean Ryan | Updated the t_{REC} to align with reset time of 10sec. |
| Rev 0.2 | 8/24/11 | Alvan Lam | Added micropak2 information and marketing drawing |
| Rev 0.3 | 8/25/11 | Alvan Lam | Updated the NMOS symbol in block diagram |
| Rev 0.4 | 9/6/11 | Alvan Lam | Created revision table instead of using Hidden Text |
| Rev 1.0.0 | 12/6/11 | Alvan Lam | Changed ABS Max to 7V, initial datasheet released by Techdoc |
| Rev 1.0.1 | 12/14/11 | Alvan Lam | Added 1.7/-25C condition to align FT7521 datasheet |





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