

TOSHIBA Diode Silicon Epitaxial Planar Type

# 1SS403

## High Voltage Switching Applications

- AEC-Q101 Qualified (Note1)
- Two-pin small packages are suitable for higher mounting densities.
- Excellent in forward current and forward voltage characteristics :  $V_F(2) = 0.90V$  (typ.)
- Fast reverse recovery time :  $t_{rr} = 60ns$  (max)
- Small total capacitance :  $C_T = 1.5pF$  (typ.)

Note1: For detail information, please contact to our sales.

## Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	$V_{RM}$	250	V
Reverse voltage	$V_R$	200	V
Maximum (peak) forward current	$I_{FM}$	300	mA
Average forward current	$I_O$	100	mA
Surge current (10ms)	$I_{FSM}$	2	A
Power dissipation	P	200 *	mW
Junction temperature	$T_j$	125	°C
Storage temperature range	$T_{stg}$	-55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

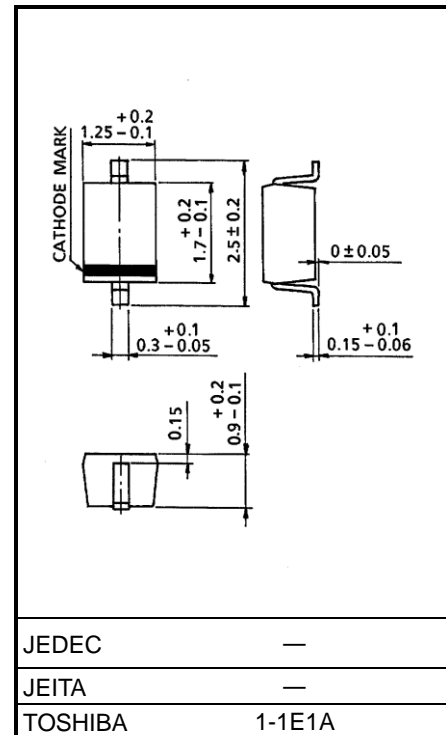
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

\*: When mounted on a glass epoxy board PCB: 20 mm × 20 mm, with copper pad 4 mm × 4 mm.

## Electrical Characteristics (Ta = 25°C)

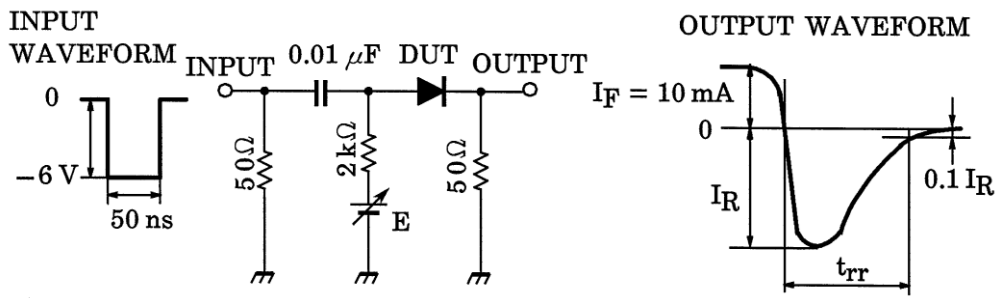
Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	—	$I_F = 10mA$	—	0.72	1.0	V
	$V_F(2)$	—	$I_F = 100mA$	—	0.90	1.2	
Reverse current	$I_R(1)$	—	$V_R = 50V$	—	—	0.1	μA
	$I_R(2)$	—	$V_R = 200V$	—	—	1.0	
Total capacitance	$C_T$	—	$V_R = 0, f = 1MHz$	—	1.5	3.0	pF
Reverse recovery time	$t_{rr}$	—	$I_F = 10mA$ (Fig. 1)	—	10	60	ns

Unit: mm

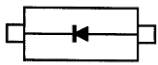


Start of commercial production  
1998-10

**Fig.1 Reverse Recovery Time ( $t_{rr}$ ) Test Circuit**

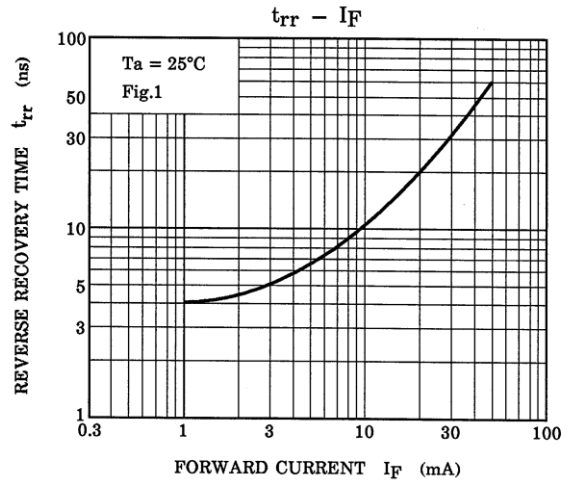
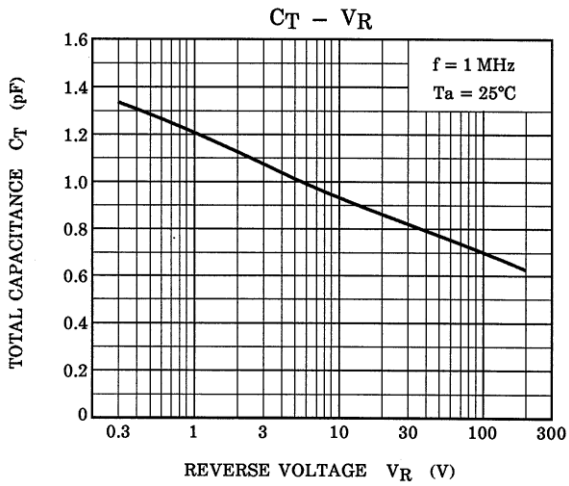
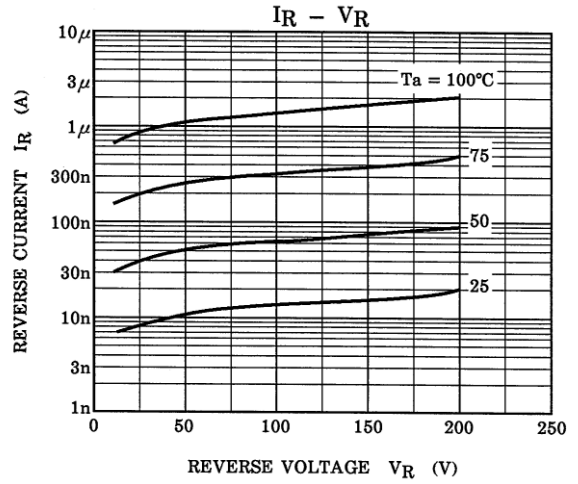
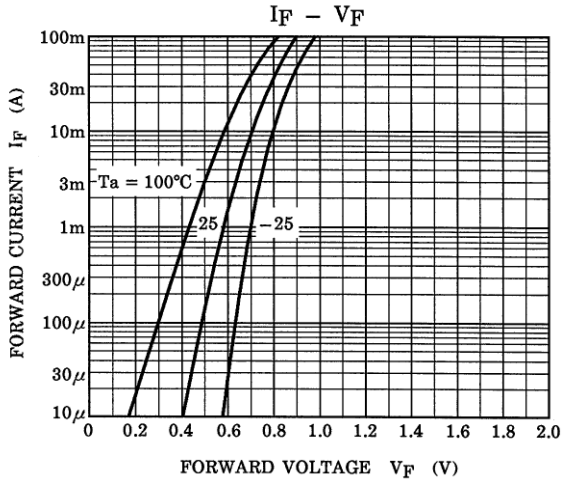


**Equivalent Circuit (Top View)**



**Marking**





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