



**THE DATASHEET OF  
GD75232DBRG4**

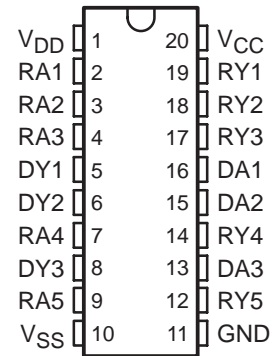


# GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS206J – MAY 1995 – REVISED NOVEMBER 2004

- **Single Chip With Easy Interface Between UART and Serial-Port Connector of IBM™ PC/AT and Compatibles**
- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Designed to Support Data Rates up to 120 kbit/s**
- **Pinout Compatible With SN75C185 and SN75185**

GD65232, GD75232 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



## description/ordering information

The GD65232 and GD75232 combine three drivers and five receivers from the Texas Instruments trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of an IBM™ PC/AT and compatibles. The bipolar circuits and processing of the GD65232 and GD75232 provide a rugged, low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The GD65232 and GD75232 comply with the requirements of the TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signaling rates up to 20 kbit/s. The switching speeds of these devices are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be expected unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbit/s, use of TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards is recommended.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP (N)	Tube of 20	GD65232N	GD65232N
	SOIC (DW)	Tube of 25	GD65232DW	GD65232
		Reel of 2000	GD65232DWR	
	SSOP (DB)	Reel of 2000	GD65232DBR	GD65232
TSSOP (PW)	Tube of 70	GD65232PW	GD65232	
	Reel of 2000	GD65232PWR		
0°C to 70°C	PDIP (N)	Tube of 20	GD75232N	GD75232N
	SOIC (DW)	Tube of 25	GD75232DW	GD75232
		Reel of 2000	GD75232DWR	
	SSOP (DB)	Reel of 2000	GD75232DBR	GD75232
	TSSOP (PW)	Tube of 70	GD75232PW	GD75232
		Reel of 2000	GD75232PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

IBM is a trademark of International Business Machines Corporation.

**PRODUCTION DATA** information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

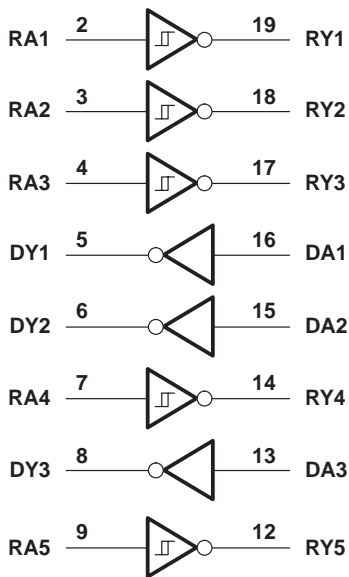


Copyright © 2004, Texas Instruments Incorporated

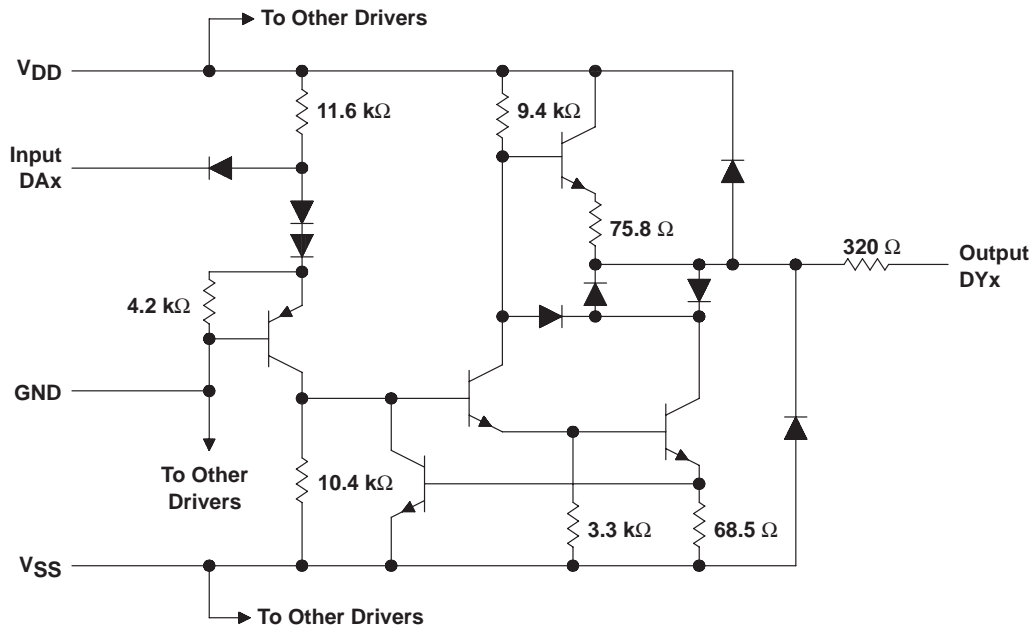
# GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS206J – MAY 1995 – REVISED NOVEMBER 2004

## logic diagram (positive logic)



## schematic (each driver)



Resistor values shown are nominal.



# GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS206J – MAY 1995 – REVISED NOVEMBER 2004

## recommended operating conditions

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage (see Note 4)	7.5	9	15	V
V <sub>SS</sub>	Supply voltage (see Note 4)	-7.5	-9	-15	V
V <sub>CC</sub>	Supply voltage (see Note 4)	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage (driver only)	1.9			V
V <sub>IL</sub>	Low-level input voltage (driver only)			0.8	V
I <sub>OH</sub>	High-level output current	Driver		-6	mA
		Receiver		-0.5	
I <sub>OL</sub>	Low-level output current	Driver		6	mA
		Receiver		16	
T <sub>A</sub>	Operating free-air temperature	GD65232	-40	85	°C
		GD75232	0	70	

NOTE 4: When powering up the GD65232 and GD75232, the following sequence should be used:

1. V<sub>SS</sub>
2. V<sub>DD</sub>
3. V<sub>CC</sub>
4. I/Os

Applying V<sub>CC</sub> before V<sub>DD</sub> may allow large currents to flow, causing damage to the device. When powering down the GD65232 and GD75232, the reverse sequence should be used.

## supply currents over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I <sub>DD</sub>	Supply current from V <sub>DD</sub>	All inputs at 1.9 V, No load	V <sub>DD</sub> = 9 V, V <sub>SS</sub> = -9 V		15	mA
			V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V		19	
			V <sub>DD</sub> = 15 V, V <sub>SS</sub> = -15 V		25	
		All inputs at 0.8 V, No load	V <sub>DD</sub> = 9 V, V <sub>SS</sub> = -9 V		4.5	
			V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V		5.5	
			V <sub>DD</sub> = 15 V, V <sub>SS</sub> = -15 V		9	
I <sub>SS</sub>	Supply current from V <sub>SS</sub>	All inputs at 1.9 V, No load	V <sub>DD</sub> = 9 V, V <sub>SS</sub> = -9 V		-15	mA
			V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V		-19	
			V <sub>DD</sub> = 15 V, V <sub>SS</sub> = -15 V		-25	
		All inputs at 0.8 V, No load	V <sub>DD</sub> = 9 V, V <sub>SS</sub> = -9 V		-3.2	
			V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V		-3.2	
			V <sub>DD</sub> = 15 V, V <sub>SS</sub> = -15 V		-3.2	
I <sub>CC</sub>	Supply current from V <sub>CC</sub>	All inputs at 5 V, No load, V <sub>CC</sub> = 5 V	GD65232		38	mA
			GD75232		30	



**DRIVER SECTION**

**electrical characteristics over recommended operating free-air temperature range,  $V_{DD} = 9\text{ V}$ ,  $V_{SS} = -9\text{ V}$ ,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$V_{IL} = 0.8\text{ V}$ ,	$R_L = 3\text{ k}\Omega$ ,	See Figure 1	6	7.5		V
$V_{OL}$	Low-level output voltage (see Note 5)	$V_{IH} = 1.9\text{ V}$ ,	$R_L = 3\text{ k}\Omega$ ,	See Figure 1		-7.5	-6	V
$I_{IH}$	High-level input current	$V_I = 5\text{ V}$ ,	See Figure 2				10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0$ ,	See Figure 2				-1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 6)	$V_{IL} = 0.8\text{ V}$ ,	$V_O = 0$ ,	See Figure 1	-4.5	-12	-19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	$V_{IH} = 2\text{ V}$ ,	$V_O = 0$ ,	See Figure 1	4.5	12	19.5	mA
$r_o$	Output resistance (see Note 7)	$V_{CC} = V_{DD} = V_{SS} = 0$ ,		$V_O = -2\text{ V to } 2\text{ V}$	300			$\Omega$

- NOTES: 5. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if  $-10\text{ V}$  is maximum, the typical value is a more negative voltage).  
6. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.  
7. Test conditions are those specified by TIA/EIA-232-F and as listed above.

**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $V_{DD} = 12\text{ V}$ ,  $V_{SS} = -12\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ ,	$C_L = 15\text{ pF}$ ,	See Figure 3		315	500	ns
$t_{PHL}$	Propagation delay time, high- to low-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ ,	$C_L = 15\text{ pF}$ ,	See Figure 3		75	175	ns
$t_{TLH}$	Transition time, low- to high-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$	$C_L = 15\text{ pF}$ ,	See Figure 3		60	100	ns
			$C_L = 2500\text{ pF}$ ,	See Figure 3 and Note 8		1.7	2.5	$\mu\text{s}$
$t_{THL}$	Transition time, high- to low-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$	$C_L = 15\text{ pF}$ ,	See Figure 3		40	75	ns
			$C_L = 2500\text{ pF}$ ,	See Figure 3 and Note 8		1.5	2.5	$\mu\text{s}$

NOTE 8: Measured between  $\pm 3\text{-V}$  and  $\pm 3\text{-V}$  points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

# GD65232, GD75232

## MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS206J – MAY 1995 – REVISED NOVEMBER 2004

### RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	T <sub>A</sub> = 25°C,	See Figure 5	1.75	1.9	2.3	V
		T <sub>A</sub> = 0°C to 70°C,	See Figure 5	1.55		2.3	
V <sub>IT-</sub>	Negative-going input threshold voltage			0.75	0.97	1.25	V
V <sub>hys</sub>	Input hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.5			V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -0.5 mA	V <sub>IH</sub> = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 10 mA,	V <sub>I</sub> = 3 V		0.2	0.45	V
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 25 V,	See Figure 5	GD65232	3.6	11	mA
				GD75232	3.6	8.3	
		V <sub>I</sub> = 3 V,	See Figure 5		0.43		
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = -25 V,	See Figure 5	GD65232	-3.6	-11	mA
				GD75232	-3.6	-8.3	
		V <sub>I</sub> = -3 V,	See Figure 5		-0.43		
I <sub>OS</sub>	Short-circuit output current	See Figure 4			-3.4	-12	mA

† All typical values are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5 V, V<sub>DD</sub> = 9 V, and V<sub>SS</sub> = -9 V.

switching characteristics, V<sub>CC</sub> = 5 V, V<sub>DD</sub> = 12 V, V<sub>SS</sub> = -12 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 5 kΩ, See Figure 6			107	250	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output				42	150	ns
t <sub>TLH</sub>	Transition time, low- to high-level output				175	350	ns
t <sub>THL</sub>	Transition time, high- to low-level output				16	60	ns
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1.5 kΩ, See Figure 6			100	160	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output				60	100	ns
t <sub>TLH</sub>	Transition time, low- to high-level output				90	175	ns
t <sub>THL</sub>	Transition time, high- to low-level output				15	50	ns



PARAMETER MEASUREMENT INFORMATION

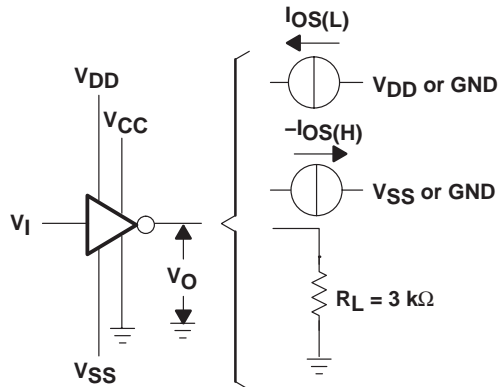


Figure 1. Driver Test Circuit for  $V_{OH}$ ,  $V_{OL}$ ,  $I_{OS(H)}$ , and  $I_{OS(L)}$

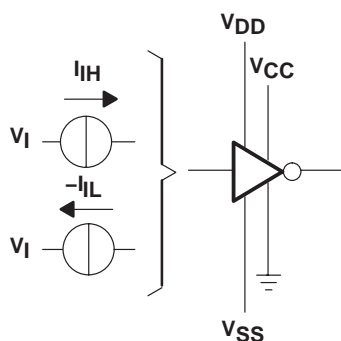
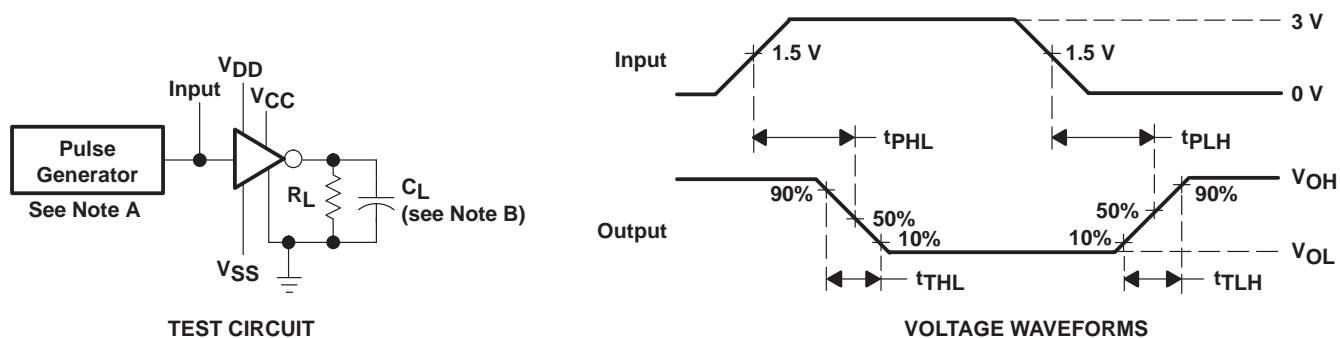


Figure 2. Driver Test Circuit for  $I_{IH}$  and  $I_{IL}$



NOTES: A. The pulse generator has the following characteristics:  $t_w = 25\ \mu\text{s}$ ,  $\text{PRR} = 20\ \text{kHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = t_f < 50\ \text{ns}$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

# GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS206J – MAY 1995 – REVISED NOVEMBER 2004

## PARAMETER MEASUREMENT INFORMATION

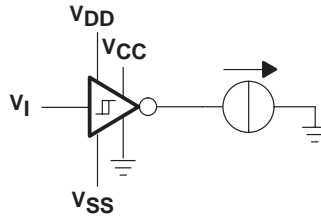


Figure 4. Receiver Test Circuit for  $I_{0S}$

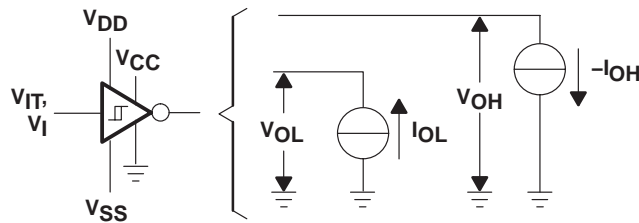
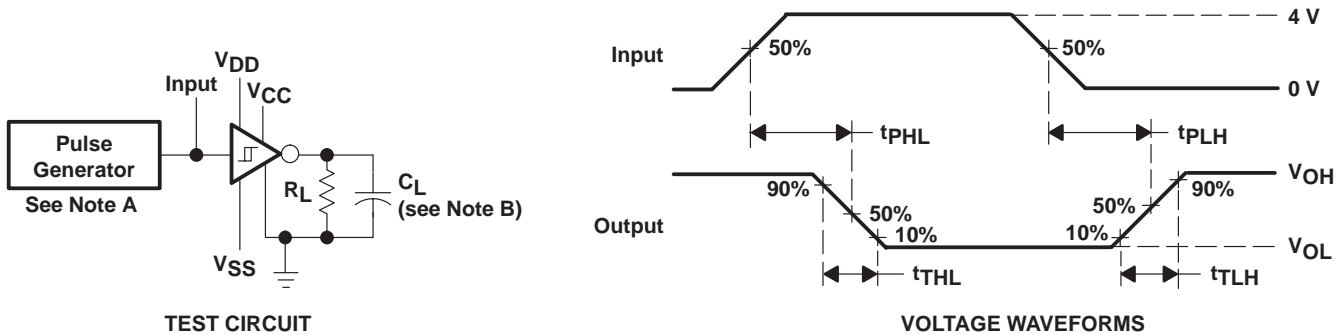


Figure 5. Receiver Test Circuit for  $V_{IT}$ ,  $V_{OH}$ , and  $V_{OL}$



NOTES: A. The pulse generator has the following characteristics:  $t_W = 25 \mu s$ ,  $PRR = 20 \text{ kHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = t_f < 50 \text{ ns}$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

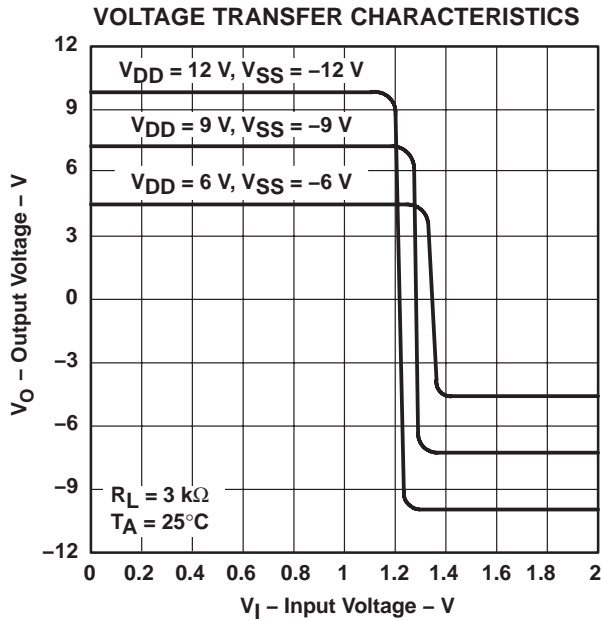


Figure 7

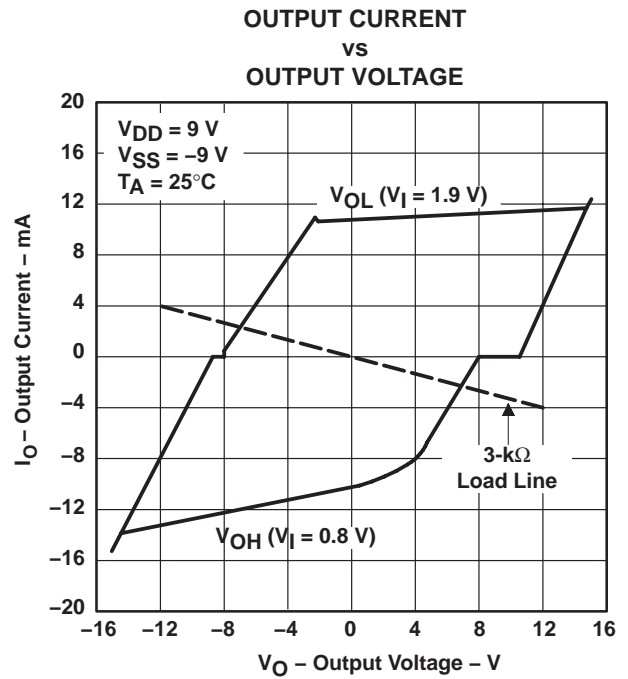


Figure 8

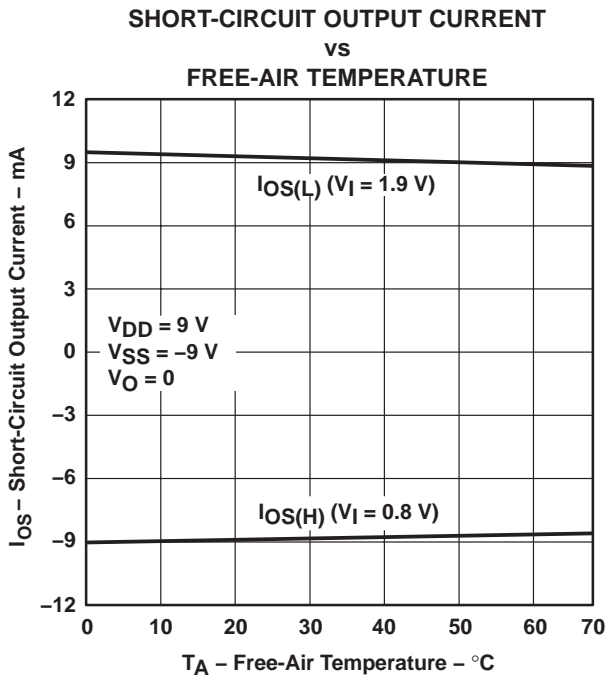


Figure 9

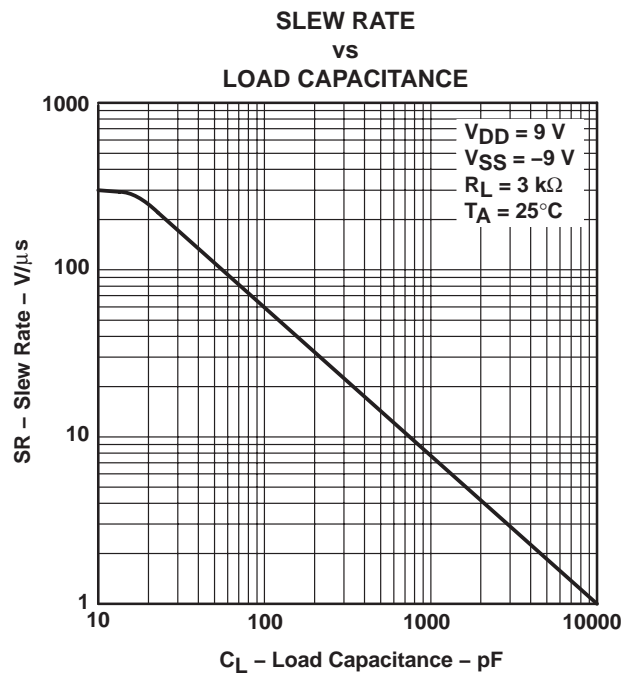
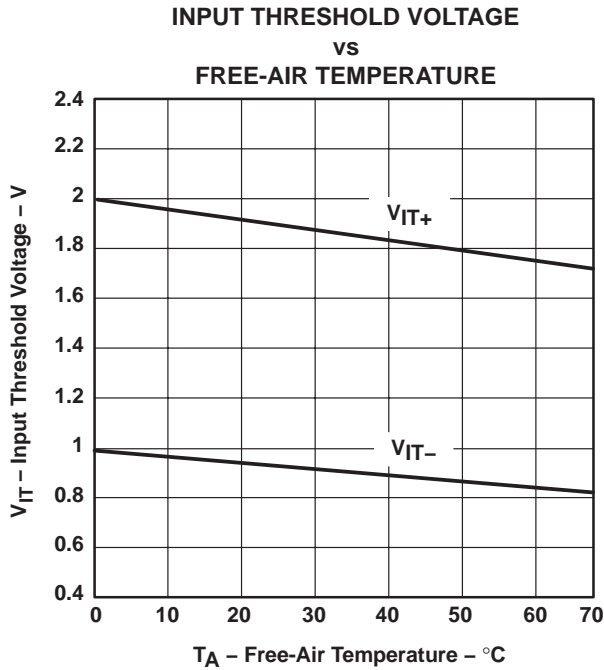
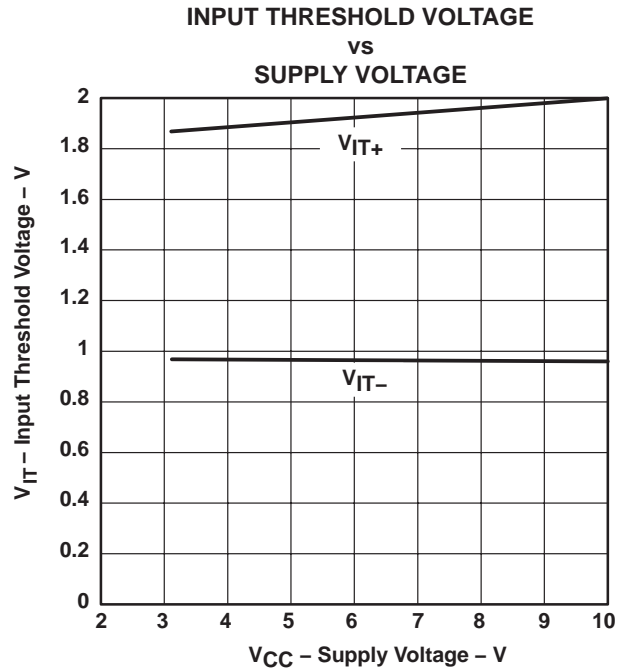


Figure 10

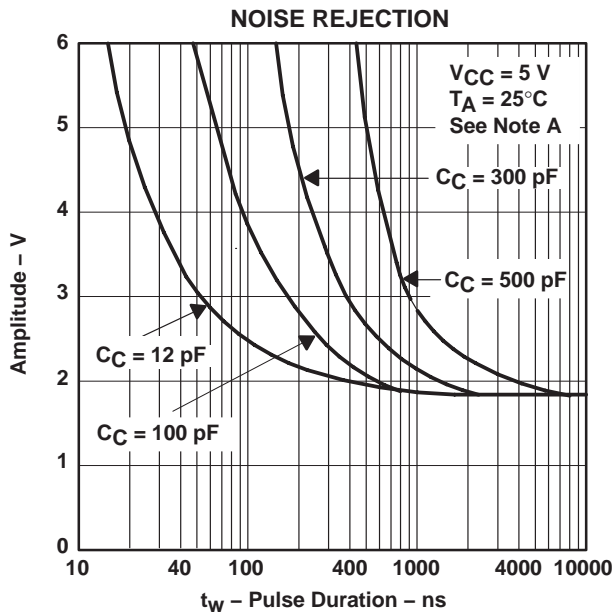
**TYPICAL CHARACTERISTICS**



**Figure 11**

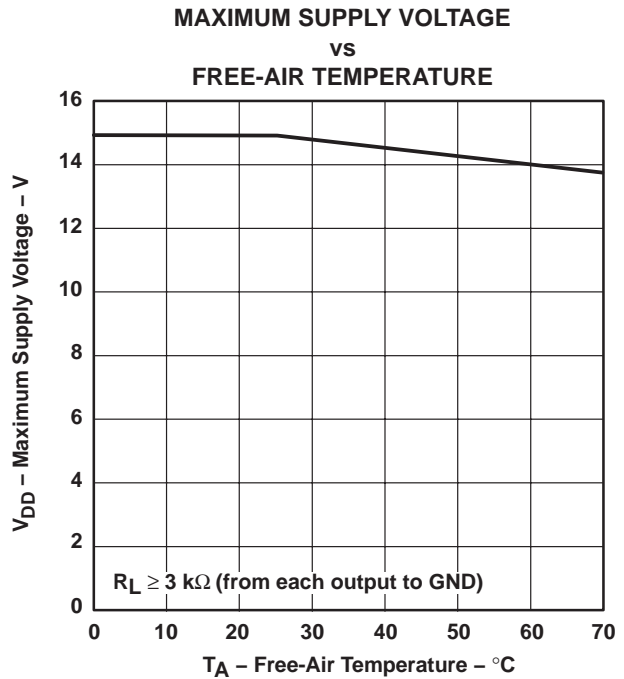


**Figure 12**



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.

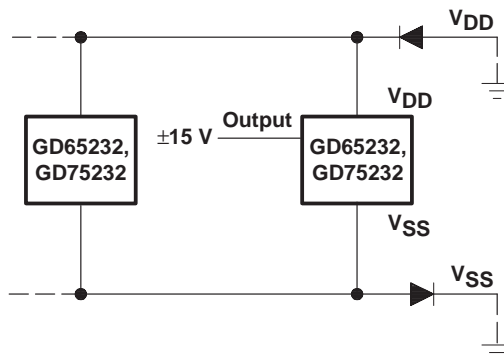
**Figure 13**



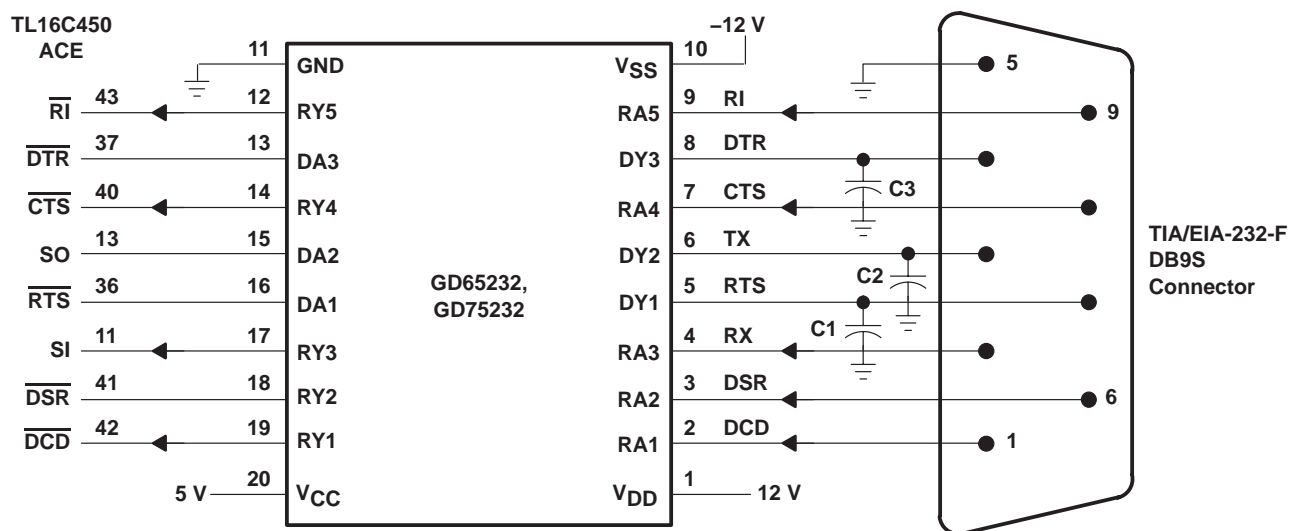
**Figure 14**

**APPLICATION INFORMATION**

Diodes placed in series with the  $V_{DD}$  and  $V_{SS}$  leads protect the GD65232 and GD75232 in the fault condition in which the device outputs are shorted to  $\pm 15$  V and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).



**Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F**



**Figure 16. Typical Connection**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
GD65232DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GD65232	<a href="#">Samples</a>
GD65232DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GD65232	<a href="#">Samples</a>
GD65232PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GD65232	<a href="#">Samples</a>
GD75232DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	<a href="#">Samples</a>
GD75232DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	<a href="#">Samples</a>
GD75232DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	<a href="#">Samples</a>
GD75232DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	<a href="#">Samples</a>
GD75232DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	<a href="#">Samples</a>
GD75232N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	GD75232N	<a href="#">Samples</a>
GD75232PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	<a href="#">Samples</a>
GD75232PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	<a href="#">Samples</a>
GD75232PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	GD75232	<a href="#">Samples</a>
GD75232PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
GD65232DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
GD75232DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
GD75232DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
GD75232PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
GD65232DWR	SOIC	DW	20	2000	367.0	367.0	45.0
GD75232DBR	SSOP	DB	20	2000	367.0	367.0	38.0
GD75232DWR	SOIC	DW	20	2000	367.0	367.0	45.0
GD75232PWR	TSSOP	PW	20	2000	364.0	364.0	27.0

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

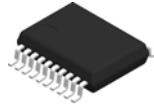
PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# DB0020A



# PACKAGE OUTLINE

## TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/A 12/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/A 12/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/A 12/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2018, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View GD75232DBRG4 on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management